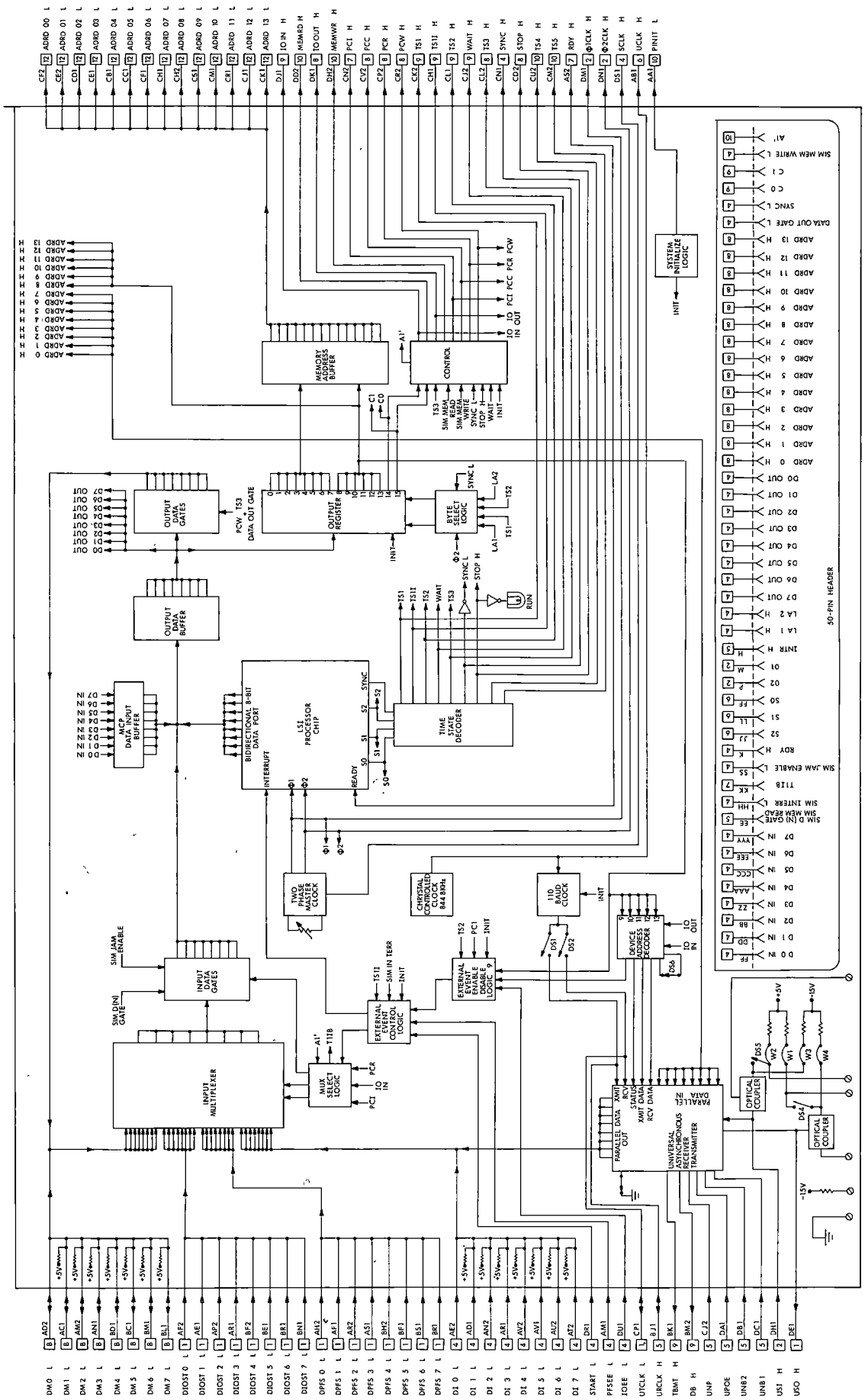

FIGURE 1. M7341 LOGIC BLOCK DIAGRAM

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SPECIFICATIONS SUMMARY

Performance Specifications

Operating Speed @ 500 kHz
Two-Phase Clock Period: 2μs
State Time: 4μs
Instruction Time: 12 to 44μs

Word Size
Data: 8-bit Word
Instruction: 1, 2, or 3 8-bit Words
Address: 14 bits

Input Data Ports
Memory Data: 8 bits
Peripheral Data: 8 bits
Power Fail/Stop: 8 bits Multiplexed
I/O External Event Interrupt/Start: 8 bits

Input/Output Lines
Memory Data: 8 bits bidirectional
Memory Address: 14 bits, output only
Peripheral Data: 8 bits input and output
Peripheral Address: 5 bits, output only
Communication Lines: 2, TTL or 20 mA current loop, active or passive.
Baud Rate
With Internal Clock: 110 baud (1.76 kHz)
With External Clock: 9600 baud (153.6 kHz), maximum (TTL)

Instruction Repertoire
Number of Basic Instructions: 48
Instruction Categories
Register Operation Instructions
Accumulator Operation Instructions
PC and Stack Control Instructions
I/O Instructions
Machine Instructions

MCP-PM Interface

Cable Length:

Φ Frequency (kHz)	Recommended BC05W cable length	
	Feet	Meters
500	8, 6, 4 or 2	2.4, 1.8, 1.2 or .6
600	6, 4 or 2	1.8, 1.2 or .6
700	4 or 2	1.2 or .6

Connector/Plug Types: 50-pin PC board connector/header
Cable Type: 50-conductor, flat, shielded

Electrical Specifications

Input Logic Levels
Logical Low: 0.8 Vdc max.
Logical High: 2.0 Vdc min.
Output Logic Levels
Logical Low: 0.4 Vdc max.
Logical High: 2.4 Vdc min.

Power Consumption: 1.6 A @ +5 V, 150 mA @ −15 V; 10.25 W

Mechanical Specifications
Board Type: Quad-height, extended-length, single-width
Dimensions: 10.436 x 8.50 x 0.50 inches (26.5 x 21.6 x 1.27 cm)

Environmental Specifications
Ambient Temperature
Operating: 5 to 50°C; (41 to 122°F)
Nonoperating: −40 to 66°C; (−40 to 150°F)
Humidity: 10 to 95%, noncondensing
Altitude
Operating: 0 to 8,000 ft. (2.4 km)
Nonoperating: 0 to 30,000 ft. (9.1 km)

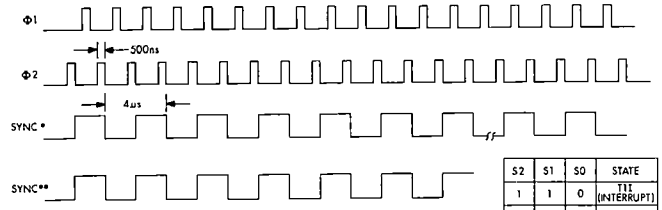
FUNCTIONS

Processor Module Timing

As shown in Figure 1, the basic timing signals for the Processor Module are produced by the two-phase clock. These signals, labeled Φ1 and Φ2, are symmetrical, nonoverlapping, positive-going clock pulses which drive the processor chip state counter.

This state counter controls all activity internal to the processor chip and produces the output signals S0, S1, S2, and SYNC. The timing signals available for external use are Φ1CLK H, Φ2CLK H, and SYNC H. SYNC H, along with S0, S1, and S2, serves to define processor module instruction execution states.

A typical PM machine cycle (see Figure 3) involves five sequential time states, TS1, TS2, TS3, TS4, and TS5. During time states TS1 and TS2, system memory is addressed by a lower and an upper address byte respectively to form a 14-bit address. During TS1, the program counter is incremented. In time state TS3, the instruction addressed during TS1, and TS2 is fetched, and during TS4 or TS4 and TS5 the fetched instruction is executed. The flow chart of time-state transitions shown in Figure 4 simplifies the progression through time states during a machine cycle.



S2	S1	S0	STATE
1	1	0	T1I (INTERRUPT)
0	1	0	T1
1	0	0	T2
0	0	0	WAIT
0	0	1	T3
0	1	1	STOPPED
1	1	1	T4
1	0	1	T5

FIGURE 3. INSTRUCTION EXECUTION STATES

The signal PFSEE L can be asserted by a power-fail sensing circuit, by a system start-stop switch, or by some other external logic. A power-fail circuit or external logic connected to the power-fail/stop port DPFS0 L to DPFS7 L can jam a one-byte Restart instruction into this port upon detection of a power failure or in reaction to some external event. This instruction would then be executed to initiate a service routine or sequence.

Activating an external system stop switch would also select the power-fail/stop port. However, in this case, all the data lines into this port would be normally High which is equivalent to a Halt instruction. When the signal PFSEE L is asserted, the power-fail/stop port is selected at time state TS3 following entry into time state TS1I which, as shown in Figure 4, occurs in the same manner as with a normal interrupt. During time state TS3, the instruction at this port is fetched by the processor for execution.

Output Data Paths

Processor Module output can be in the form of memory addresses, memory and I/O control information, I/O device addresses, data output to memory, and data output to peripherals. With the exception of data output to memory, all of these addresses and data are stored for output in the 16-bit multipurpose output register. Data words are latched into the register by the data selection logic during time states TS1 and TS2 (see Figure 1).

Memory addresses are issued as two separate words to form a 14-bit address word during machine cycles PCI, PCR, and PCW, the lower word at time state TS1 and the upper word at TS2 of these cycles.

During each one of the time states, the corresponding memory address word is loaded into the 16-bit output register by the address selection logic. At the end of time state TS2, the current memory address is present as output from the output register. These output lines are buffered to drive the address/data lines ADRD00 L to ADRD13 L which can be bused out to MPS ROMs, RAMs, and I/O devices.

Data to be written in read/write memory is gated onto the bidirectional memory bus DM0 L to DM7 L during time state TS1 and TS2 of a PCW cycle. Data must be accepted by the memory during time state TS3 of that cycle.

During a PCC cycle, the content of the accumulator and the instruction register are stored in output register bits 0 through 13 for use as peripheral device output data and address. At time state TS1 of a PCC cycle, the content of the accumulator, which is the data to be output to the addressed peripheral device, is placed in the output register bit positions 0 to 7.

At time state TS2, the content of the instruction register is transferred to output register bit positions 8 through 15, with bits 9 through 13 containing the address of the peripheral device being accessed during the PCC cycle. Once stored in the output register, these address and data fields are available to external peripheral devices over the lines ADRD00 L to ADRD13 L. This device address field permits the addressing of eight input devices and 22 output devices.

Control Logic

The control logic (see Figure 1) provides the various control signals necessary to memory accessing and to the performance of input/output operations with associated peripherals. Input to the control logic is the state of bits 14 and 15 of the output register.

During time state TS3 of every machine cycle, the I/O control signals pertinent to the machine cycle currently being executed are asserted (see Figure 5). For example, during PCI and PCR cycles where memory is addressed to fetch an instruction or data, the signal MEM RD H is asserted at the end of time state TS2 and throughout TS3. This signal controls the reading of data from that memory location addressed during the pertinent machine cycle.

During a PCC cycle, the signals I/O IN H or I/O OUT H are asserted during time state TS3 to control the storage and retrieval of data at external peripheral devices. When data is to be written into an addressed memory location during a PCW cycle, the signal MEM WR H is asserted by the control during time state TS3 of that machine cycle.

In addition to these signals, the control logic also asserts one of the signals PCI L, PCC L, PCR L, or PCW L during time state TS3 of the corresponding machine cycle.

Asynchronous Communications Receiver/Transmitter Logic

The PM is equipped with a full duplex communication receiver/transmitter implemented by a Universal Asynchronous Receiver/Transmitter (UAR/T). A 1.76-kHz clock driven by an 844.8-kHz crystal-controlled clock integral to the PM is input to this device to produce a 110-baud data transfer rate. The receiver/transmitter is addressed for transmission or receipt of data or for status information during time state TS3 by bits 9 to 13 of the output register. Data is transmitted and received at the module over 20-mA current loop or TTL-compatible lines (USI H and USO H) to interface with Teletype-like lines or to telephone lines through a modem.

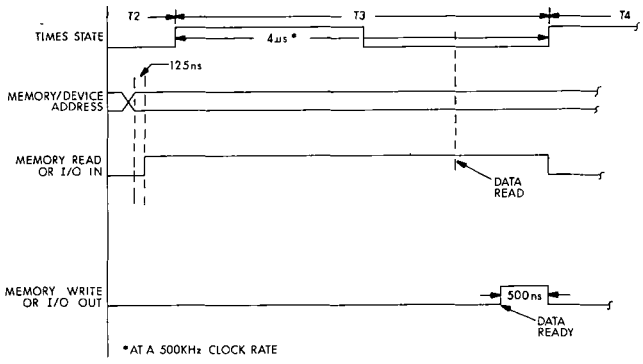


FIGURE 5. INPUT-OUTPUT TIMING

Input Signals

Symbol	*Description*	*Pin*	*Function*
START L	Start Processor Module	DR1	This pulse, having a period >50 ns, is asserted to place the Processor Module in the run state by multiplexing an appropriate instruction from the DIOST lines into the module for fetching.
IOEE L	External Event Line	DU1	This line is asserted by external event detection logic. When asserted, this signal multiplexes the instruction on the DIOST lines into the input multiplexer for fetching. This line can be enabled or disabled under program control.
DI0 L	I/O Device Input 0	AE2	These eight prallel input lines comprise the peripheral device data input port to the input multiplexer. Data must appear on these lines as a consequence of I/O device addressing resulting from execution of an INP instruction (see PROGRAMMING).
DI1 L	I/O Device Input 1	AD1	
DI2L	I/O Device Input 2	AN2	
DI3 L	I/O Device Input 3	AP1	
DI4 L	I/O Device Input 4	AV2	
DI5 L	I/O Device Input 5	AV1	
DI6 L	I/O Device Input 6	AU2	
DI7 L	I/O Device Input 7	AT2	
DPFS0 L	Power/Fail Stop Input 0	AH2	These eight parallel input lines comprise the power/fail stop port to the input multiplexer. An appropriate instruction must be multiplexed into the Processor Module from this port for fetching by the processor module by the assertion of the signal DFSEE L.
DPFS1 L	Power/Fail Stop Input 1	AF1	
DPFS2 L	Power/Fail Stop Input 2	AR2	
DPFS3 L	Power/Fail Stop Input 3	AS1	
DPFS4 L	Power/Fail Stop Input 4	BH2	
DPFS5 L	Power/Fail Stop Input 5	BF1	
DPFS6 L	Power/Fail Stop Input 6	BS1	
DPFS7 L	Power/Fail Stop Input 7	BR1	
PFSEE L	Power/Fail Stop External Event Line	AM1	This pulse, having a period >50 ns, is asserted in response to a power failure or some external stop switch. When asserted, this signal causes the appropriate instruction on the DPSF lines to be multiplexed into the processor module for fetching.
RDY H	READY	AS2	When true (High), this signal causes the Processor Module to be ready for operation which is the normal state of this signal. When false (Low), the Processor Module enters the Wait state and remains in this state until Ready is again asserted.
UPOE	Even-Odd Parity Select	DA1	When this input line to the Processor Module receiver/transmitter is asserted High, even parity is selected, and when asserted Low, odd parity is selected.

Output Signals

Symbol	*Description*	*Pin*	*Function*
MEM RD H	Memory Read Control Signal	DD2	When asserted, this signal designates that contents of the memory location currently addressed by ADRD00 L to ADRD13 L are at the bidirectional memory bus DM0 L to DM7 L are stable and ready for input multiplexing.
MEM WR H	Memory Write Control Signal	DH2	When asserted, this signal designates that the word to be written into the memory location currently addressed by ADRD00 L to ADRD13 L is on the bidirectional memory bus DM0 L to DM7 L and stable.
IO IN H	Peripheral Device Read Control	DJ1	When asserted, this signal strobes the data word from the peripheral device addressed by ADRD09 to ADRD13 onto lines DI0 to DI7 for input multiplexing.
IO OUT H	Peripheral Device Write Control	DK1	When asserted, this signal designates that the data on output lines ADRD00 to ADRD07 to be written to the peripheral device addressed by output lines ADRD09 to ADRD13 is stable and ready to be written into the device.
SCLK H	System Clock	DS1	This signal is the basic system clock frequency. The Processor Module is normally shipped with this clock frequency set to 1 MHz.
UCLK H	Crystal Controlled Clock	AB1	This output signal is a crystal-controlled 844.8-kHz clock frequency which can be the base frequency for deriving various operating frequencies up to 9600 baud.
Φ1CLK H Φ2CLK H	LSI Processor Clock	DM1 DN1	These output signals comprise the two-phase nonoverlapping clock frequency derived from SCLKH and serve to time the processor chip.
TS1 H TS1 IH TS2 H TS3 H TS4 H TS5 H STOP H WAIT H	Time States	CK2 CA1 CL1 CL2 CU2 CM2 CD2 CT2	These eight output signals provide an external reference to Processor Module time states. (See Processor Module Timing under FUNCTIONS.)
PCI L PCR L PCW L PCC L	Machine Cycles	CN2 CV2 CP2 CR2	These four output signals provide an external reference to Processor Module machine cycles. (See Processor Module Instruction Cycles under FUNCTIONS.)
SYNC H	Basic Timing Signal	CN1	This output signal is Φ2CLK H÷2 and provides the basic timing relationship within a given time state.
PINIT L	System Initialize Signal	AA1	This output signal supplies a power-up initialize pulse of approximately 10 ms in duration.
USO H	TTL Serial Output	DE1	This output signal line provides for the transfer of serial TTL data from the asynchronous communications controller.
TBMT H	Transmitter Buffer Empty	BK1	When asserted, this signal designates that the receiver/transmitter transmitter buffer is empty and therefore is ready to accept a word for transmission.
DA H	Data Available	BM2	When asserted, this signal designates that a word is ready for reading from the receiver/transmitter receive buffer.

TABLE 1

Processor Module Instruction Set Notational Standards

Symbol	*Definition*
<B2>	Second byte of an instruction
<B3>	Third byte of an instruction
r, r1, r2	Any of the 8-bit general-purpose registers A, B, C, D, E, H, L
A	A general-purpose register used as the accumulator
B, C, D, E	General-purpose registers
H, L	Two general-purpose registers used as memory address registers
C_3, C_4	Condition flip-flops:

Designation	Code C_4	Code C_3	Truth Condition
Carry (C)	0	0	Overflow, underflow
Zero (Z)	0	1	Result is ZERO
Sign (S)	1	0	MSB of result is ZERO
Parity (P)	1	1	Parity of result is even

C	One of the condition flip-flops—C, Z, S, or P
M	The memory location addressed by the content of registers H and L. The source/destination code for memory is 111.
( )	Content of a memory location, a register, or a condition flip-flop
$\wedge$	Logical AND
$\vee$	Inclusive OR
$\forall$	Exclusive OR
Am	Bit m of the Accumulator register
STACK	A group of eight 14-bit registers with seven organized as a LIFO pushdown stack to store nested subroutine addresses with the eighth storing the current program counter (P)
P	A 14-bit register which contains the address of the next instruction to be fetched
$\leftarrow$	Becomes
XXX	Don't care about the content of this field
SSS	Source register r code field
DDD	Destination register r code field:

Source/Destination register codes:

Register	Code
A	000
B	001
C	010
D	011
E	100
H	101
L	110

Add r to Accumulator
MNEMONIC ADr

7	6	5	3	2	0
1	0	0 0 0		S S S	

EXECUTION TIMES/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(A)←(A)+(r)

Add r to Accumulator and Carry Flip-Flop
MNEMONIC ACr

7	6	5	3	2	0
1	0	0 0 1		S S S	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(A)←(A)+(CARRY)+(r)

Subtract r from Accumulator
MNEMONIC SUr

7	6	5	3	2	1
1	0	0 1 0		S S S	

EXECUTION TIMES/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(A)←(A)−(r)

Subtract r and Carry Flip-Flop from Accumulator
MNEMONIC SBr

7	6	5	3	2	0
1	0	0 1 1		S S S	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20μs, PCI

FUNCTION
(A)←(A)−(r)−(BORROW)

Logically AND r and Accumulator
MNEMONIC NDr

7	6	5	3	2	0
1	0	1 0 0		S S S	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(A)←(A) ∧ (r)

Logically OR r and Accumulator
MNEMONIC ORr

7	6	5	3	2	0
1	0	1 1 0		S S S	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(A)←(A) ∨ (r)

Exclusive OR r and Accumulator
MNEMONIC XRr

7	6	5	3	2	0
1	0	1 0 1		S S S	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(A)←(A)⊻(r)

Compare r with Accumulator
MNEMONIC CPr

7	6	5	3	2	0
1	0	1 1 1		S S S	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20μs, PCI

FUNCTION
(A)−(r)

Arithmetic/Logical Operations with Memory

Arithmetic/logical operations involving the accumulator and a memory location addressed by registers H, L are implemented by the eight instructions described below. Content of the memory location addressed by registers H, L is unchanged by instruction execution. All instructions in this category have a one-byte format.

Add M to Accumulator
MNEMONIC ADM

7	6	5	3	2	0
1	0	0 0 0		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A)+(M)

Add M to Carry Flip-Flop and Accumulator
MNEMONIC ACM

7	6	5	3	2	0
1	0	0 0 1		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A)+(CARRY)+(M)

Subtract M from Accumulator
MNEMONIC SUM

7	6	5	3	2	0
1	0	0 1 0		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A)−(M)

Subtract M and Carry Flip-Flop from Accumulator
MNEMONIC SBM

7	6	5	3	2	0
1	0	0 1 1		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A)−(M)−(BORROW)

Logically AND M and Accumulator
MNEMONIC NDM

7	6	5	3	2	0
1	0	1 0 0		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A) ∧ (M)

Logically OR M and Accumulator
MNEMONIC ORM

7	6	5	3	2	0
1	0	1 1 0		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A) ∨ (M)

Exclusive OR M and Accumulator
MNEMONIC XRM

7	6	5	3	2	0
1	0	1 0 1		1 1 1	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCR

FUNCTION
(A)←(A)⊻(M)

Rotate Accumulator Right and Into Carry Flip-Flop
MNEMONIC RRC

7	6	5	3	2	0
0	0	0 0	1	0 1	0

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
Am←Am+1, A7←A0, (CARRY)←A0

Rotate Accumulator Left Through Carry Flip-Flop
MNEMONIC RAL

7	6	5	3	2	0
0	0	0 1	0	0 1	0

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
Am+1←Am, A0←(CARRY), (CARRY)←A7

Rotate Accumulator Right Through Carry Flip-Flop
MNEMONIC RAR

7	6	5	3	2	0
0	0	0 1	1	0 1	0

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
Am←Am+1, A7←(CARRY), CARRY)←A0

Program Counter and Stack Control Operations
Instructions in this class perform three basic programming functions, namely: jump to nonsequential memory locations, subroutine entry, and return from subroutine. The commonality which exists between the instructions performing these three functions is found in the use of the program counter.

The four condition flip-flops (carry, zero, sign, and parity) can be used by conditional jump, subroutine call, and subroutine return instructions.

All jump and subroutine call instructions are accompanied by the two 8-bit bytes <B2> and <B3> which are used during instruction execution to modify the program counter. Byte <B2> always contains the eight low-order bits of the memory address, and <B3> contains the six high-order bits. Since all memory addresses are 14 bits in length, bits 6 and 7 of <B3> are not used.

Jump Instructions
Jump instructions implement the transfer of program control to some nonsequential memory address either conditionally or unconditionally based on the state of a condition flip-flop as determined by prior processing. All jump instructions have a three-byte format.

Jump Unconditionally
MNEMONIC JMP

7	6	5	3	2	0
0	1	X X	X	1 0	0

7	0
<B2>	

7	0
<B3>	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
44 μs, PCI PCR PCR

FUNCTION
(P)←<B3><B2>

Jump if Condition True
MNEMONIC JTc

7	6	5	3	2	0
0	1	1	C_4 C_3	0 0	0

7	0
<B2>	

7	0
<B3>	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
44 μs, PCI PCR PCR
36 μs, PCI PCR PCR

FUNCTION
(P)←<B3><B2>IF C=1
(P)←(P)+3 IF C=0

Jump if Condition False
MNEMONIC JFc

7	6	5	3	2	0
0	1	0	C_4 C_3	0 0	0

7	0
<B2>	

7	0
<B3>	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
44 μs, PCI PCR PCR
36 μs, PCI PCR PCR

FUNCTION
(P)←<B3><B2>IF C=0
(P)←(P)+3 IF C=1

Subroutine Call Instructions
Call instructions initiate entry into a subroutine either unconditionally or conditionally based on the state of a designated condition flip-flop as determined by prior processing. When a call instruction is executed, and an attending condition is satisfied, the content of the program counter is automatically stored in the STACK to implement return to the program line when subroutine function is complete. The prior content of the program counter is then replaced by <B3> <B2> which is the starting address of the subroutine being called. All subroutine call instructions have a three-byte format. The RST instruction, which is a special one-byte call instruction used to perform calls to restart routines, is for purposes of functional presentation described under "Machine Instructions."

Call Subroutine Unconditionally
MNEMONIC CAL

7	6	5	3	2	0
0	1	X X	X	1 1	0

7	0
<B2>	

7	0
<B3>	

EXECUTION TIME/ MACHINE CYCLES EXECUTED
44 μs, PCI PCR PCR

FUNCTION
(STACK)←(P), (P)←<B3> <B2>

The restart instruction is a one-byte unconditional call on any one of eight reserved locations within the first 64 words of memory. These eight locations are addressed directly by the restart instruction at octave intervals within these 64 memory words. Each of the eight locations can be the starting location of eight word subroutines which are entered under application-defined conditions. This instruction stores the content of the program counter in the STACK to permit a return to the program line.

All four instructions in this category have a one-byte format.

Halt

MNEMONIC HLT

7						1	0
0	0	0	0	0	0	0	X

OR

7							0
1	1	1	1	1	1	1	1

EXECUTION TIME/ MACHINE CYCLES EXECUTED
16 μs, PCI

FUNCTION
HALT PROCESSOR

Enable Interrupts

MNEMONIC ION

7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	1

EXECUTION TIME/ MACHINE CYCLES EXECUTED
32 μs, PCI PCC

FUNCTION
ENABLE EXTERNAL EVENT INTERRUPT

Disable Interrupts

MNEMONIC IOF

7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	1

EXECUTION TIME/ MACHINE CYCLES EXECUTED
24 μs, PCI PCC

FUNCTION
DISABLE EXTERNAL EVENT INTERRUPT

Restart

MNEMONIC RST

7	6	5			2	1	0
0	0	A	A	A	1	0	1

EXECUTION TIME/ MACHINE CYCLES EXECUTED
20 μs, PCI

FUNCTION
(STACK)←(P), (P)←(00000000AAA000)

HARDWARE/ACCESSORIES

In order to be operational, a processor module must be equipped with a memory of sufficient size to contain the operating program. Such a memory can be configured from M7344 Read/Write Memory Modules and/or M7345 Read-Only Memory Modules. Programs can be bootstrapped into a Processor Module memory through use of the KC341-B Monitor/Control Panel (MCP).

The KC341-B serves as an address and data input station for operating Processor Modules and provides a visual display of addresses and data as well as a display of Processor Module machine states and operating status. The MCP also contains a 32-word random access scratchpad memory and a 256-word programmable read-only memory.

In a standard KC341-B Monitor/Control Panel, this programmable read-only memory contains a bootstrap loader program which occupies approximately 128 words of that memory. Figure 1 presents the signal names and shows the signal flow for the 50-pin header and cable assembly which connects the KC341-B Monitor/Control Panel with the processor module.

SPECIAL WIRING

The M7341 processor module is supplied with a set of special switches and factory-installed jumpers. Each of these switches and jumpers is depicted in the block diagram shown in Figure 1. The table presented summarizes the functions implemented by each switch and jumper.

INPUT/OUTPUT SYMBOLOGY

The direction of signal flow is indicated by arrows on the signal lines. Arrows toward the module indicate input signals; arrows away from the module indicate output signals (see Figure 1 and Figure 6).

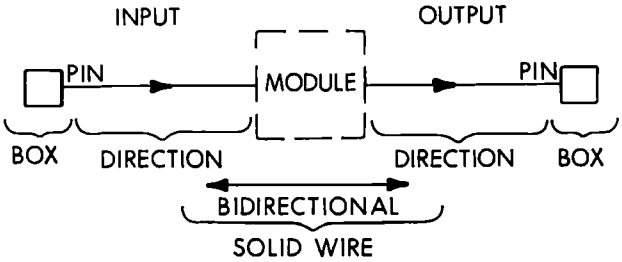


FIGURE 6. SIGNAL FLOW DIRECTION

Fan-in and fan-out (in TTL unit loads) are indicated by the number contained in the box associated with each pin. A box containing the letter B designates that the associated signal line is connected to a bus.

INPUT—The fan-in designation box always precedes the pin designation.

OUTPUT—The fan-out designation box always follows the pin designation.

digital

DIGITAL EQUIPMENT CORPORATION

COMPONENTS GROUP HEADQUARTERS

ONE IRON WAY, MARLBOROUGH, MASSACHUSETTS 01752

(617) 481-7400 TWX: 710-347-0348

For detailed information about products and policies, call 800-225-9480 toll-free (USA only); Massachusetts residents call (617) 481-7400.

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