Digital Semiconductor 21164 Alpha Microprocessor Motherboard

User's Manual

Order Number: EC–QLJLC–TE

Revision/Update Information: This document supersedes the *Alpha 21164 Microprocessor Motherboard User's Manual* (EC–QLJLB–TE).

Digital Equipment Corporation
Maynard, Massachusetts

March 1996

This document was prepared using VAX DOCUMENT Version 2.1.

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About This Manual

This manual describes Digital Semiconductor's 21164 Alpha microprocessor motherboard (EB164), a module for computing systems based on the 21164 Alpha microprocessor and the Digital Semiconductor 21171 chipset.

Audience

This manual is intended for users of the EB164 to assist them in installing the EB164 and populating it with memory modules and peripheral cards.

Scope

This manual describes the features, configuration, and installation of the EB164. This manual does not include specific bus specifications (for example, PCI or ISA buses). Additional information is available in the appropriate vendor and IEEE specifications. See Appendix B for information about how to obtain additional technical support and how to order additional documentation.

Content

This manual contains the following chapters and appendixes:

- Chapter 1, Introduction to the EB164, is an overview of the EB164, including its components, uses, and features.
- Chapter 2, System Configuration and Connectors, describes the user environment configuration; board connectors and functions; jumper functions; and identifies jumper and connector locations.
- Chapter 3, Starting and Using the EB164, lists additional hardware and software requirements, provides information on how to configure the hardware and software, and describes the motherboard startup procedures.
- Chapter 4, Functional Description, describes some of the functional elements of the EB164, such as flash ROM contents, interrupt assignments, and power distribution.

- Chapter 5, EB164 Requirements, Power, and Parameters, describes the EB164 power and environmental requirements, and identifies major board components.
- Appendix A, Supporting Vendor Products, lists suggested vendor sources for supporting components, such as, power supply, SIMMs, enclosure, and so forth.
- Appendix B, Technical Support and Ordering Information, describes how to obtain Digital Semiconductor information and technical support, and how to order Digital Semiconductor products and associated literature.

Document Conventions

This section provides the conventions used in this document.

Caution: Cautions indicate potential damage to equipment or data.

Note: Notes provide additional information.

Numbering: All numbers are decimal or hexadecimal unless otherwise indicated. In case of ambiguity, a subscript indicates the radix of nondecimal numbers. For example, 19 is a decimal number, but 19_{16} and 19A are hexadecimal numbers.

Extents: Extents are specified by a single number, or a pair of numbers in angle brackets (< >) separated by a colon (:) and are inclusive. For example, bits <7:3> specify an extent including bits 7, 6, 5, 4, and 3. Multiple bit fields are shown as extents.

Register Figures: Register figures have bit and field position numbering starting at the right (low-order) and increasing to the left (high-order).

Signal Names: Signal names in text are printed in boldface lowercase type. For example, " . . . bits **data<127:0>** are delivered to the Bcache SIMM connectors . . . "

1
Introduction to the EB164

This chapter provides an overview of the EB164 motherboard and describes the EB164, its components, features, and uses.

1.1 System Components and Features

The EB164 is implemented in industry-standard parts and uses a Digital Semiconductor 21164 Alpha microprocessor (21164) running at 266, 300, or 333 MHz. The functional components are shown in Figure 1–1 and are introduced in the following subsections.

1.1.1 Digital Semiconductor 21171 Core Logic Chipset

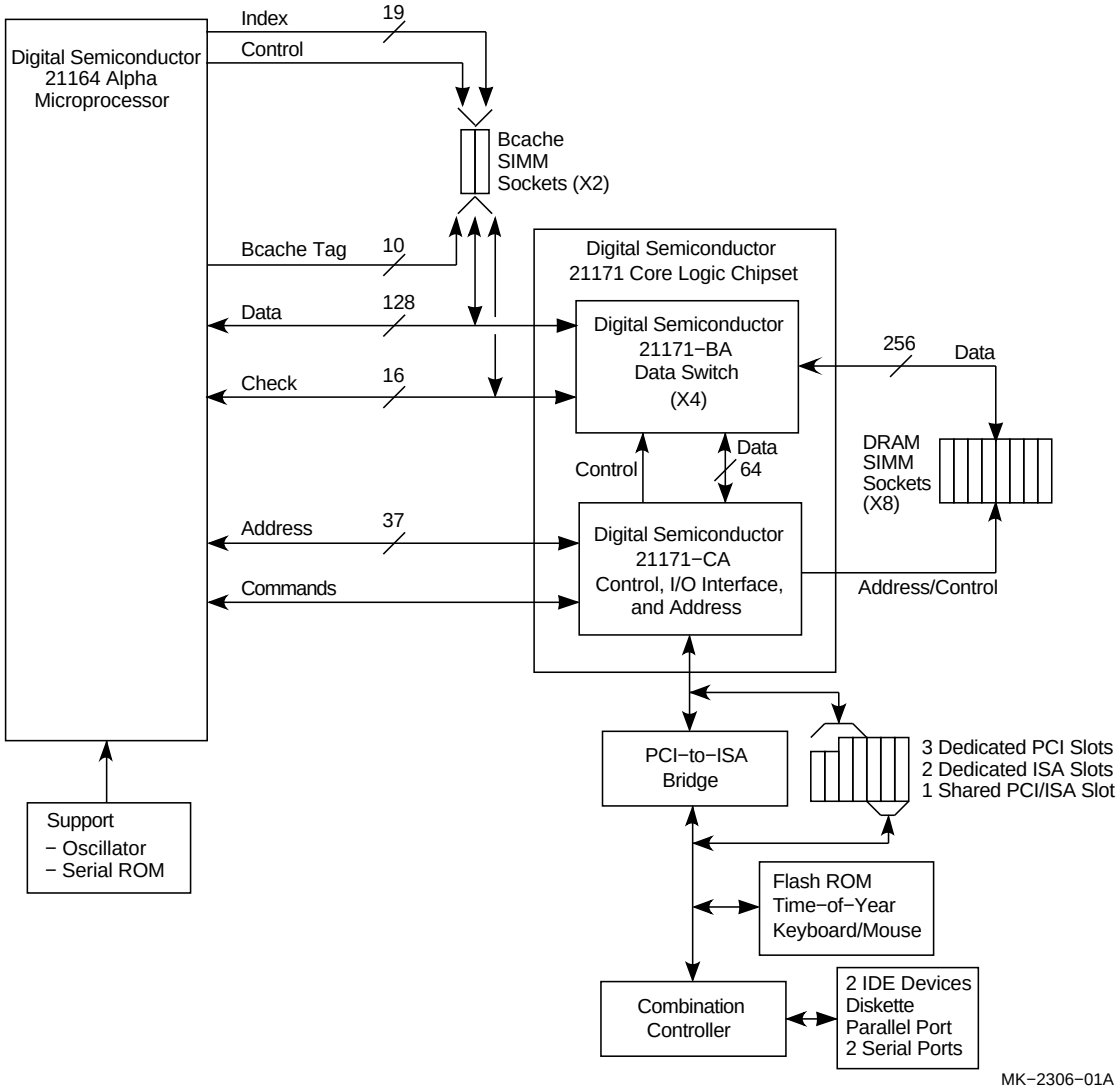
The 21164 is supported by the Digital Semiconductor 21171 (21171) chipset. The 21171 consists of the following two application-specific integrated circuit (ASIC) types:

- One copy of the 21171-CA control, I/O interface, and address chip (CIA) provides the interface between the 21164, main memory (addressing and control), and the peripheral component interconnect (PCI) bus. It also provides the data switch companion chips with control information to direct the data flow.
- Four copies of the 21171-BA data switch chip (DSW) provide the memory interface data path and route PCI data through the CIA chip.

The chipset includes the majority of functions required to develop a high-performance PC or workstation, requiring minimum discrete logic on the module. It provides flexible and generic functions to allow its use in a wide range of systems.

1.1 System Components and Features

Figure 1–1 EB164 Functional Block Diagram



1.1.2 Memory Subsystem

The dynamic random-access memory (DRAM) provides 32MB to 512MB with a 256-bit data bus. The memory is contained in one bank of eight commodity single inline memory modules (SIMMs). Single- or double-sided SIMMs may be used. Each SIMM is 36 bits wide, with 32 data bits and 4 check bits, with 70 ns or less access. Table 1–1 lists the SIMM sizes supported and the corresponding main memory size for 256-bit arrays.

Table 1–1 Main Memory Sizes

SIMM Size	Eight SIMMs (256-Bit Array)
1M × 36	32MB
2M × 36	64MB
4M × 36	128MB
8M × 36	256MB
16M × 36	512MB

All eight SIMM connectors (J3 through J10) must be populated. See Figure 2–3 and Table 2–2.

1.1.3 L3 Bcache Subsystem Overview

The board-level external L3 backup cache (Bcache) subsystem supports multiple cache sizes and access times. Cache sizes supported are 2MB with Alpha cache SIMMs populated with 128K × 8 SRAMs, and 4MB and 8MB with SIMMs populated with 512K × 8 SRAMs. Speeds of 6 ns to 15 ns can be used.

The EB164 has a 2MB 10-ns Bcache SIMM. See Appendix A for order information.

1.1.4 PCI Interface Overview

The EB164 PCI interface is the main I/O bus for the majority of functions (SCSI interface, graphics accelerator, and so on). The PCI interface provides a selectable PCI speed between 25 MHz and 33 MHz (based on the 21164 clock divisor). An onboard PCI-to-ISA bridge is provided through an Intel 82378ZB Saturn I/O (SIO) chip.

The PCI bus has three dedicated PCI expansion slots (one 64-bit and two 32-bit) and one shared 64-bit PCI/ISA slot.

1.1.5 ISA Interface Overview

The ISA bus has two dedicated slots and a third shared ISA/PCI slot. It provides the following system support functions:

- Mouse and keyboard controller functions—provided by an Intel 8242 chip.
- An IDE interface, a diskette controller, two universal asynchronous receiver–transmitters (UARTs) with full modem control, and a bidirectional parallel port—provided by a National 87312 combination chip.
- A time-of-year (TOY) function—provided by a Dallas Semiconductor DS1287 chip.
- Operating system support—provided by a 1MB flash ROM that contains firmware and debug monitor code.

  Users can develop code on a host system, and load software into the EB164 through a serial line, diskette, or Ethernet board. In addition, sectors of the flash ROM can be programmed for application-specific purposes.

1.1.6 Miscellaneous Logic

The EB164 contains the following miscellaneous components:

- Clocks

  A 26.66-MHz oscillator and phase-locked loop (PLL) clock generator provide a clock source to the 21164 microprocessor and system.

  A 14.3-MHz crystal and frequency generator provide a clock source for ISA devices.

- Serial ROM

  A Xilinx XC17128 serial ROM (SROM) contains initial code that is loaded into the 21164 instruction cache (Icache) on power-up. A serial line interface is also provided to allow direct connection to a terminal line for debugging purposes.

- Programmable array logic (PAL) devices for the following functions:
  - One PAL for utility bus (Ubus) decoding
  - One PAL for interrupts
  - Two PAL devices for memory row address strobe (RAS) bank generation and buffering

1.1.7 Software Support

Software support code, consisting of a debug monitor and Windows NT ARC firmware is contained in a 1MB flash ROM. The monitor provides functions that allow you to:

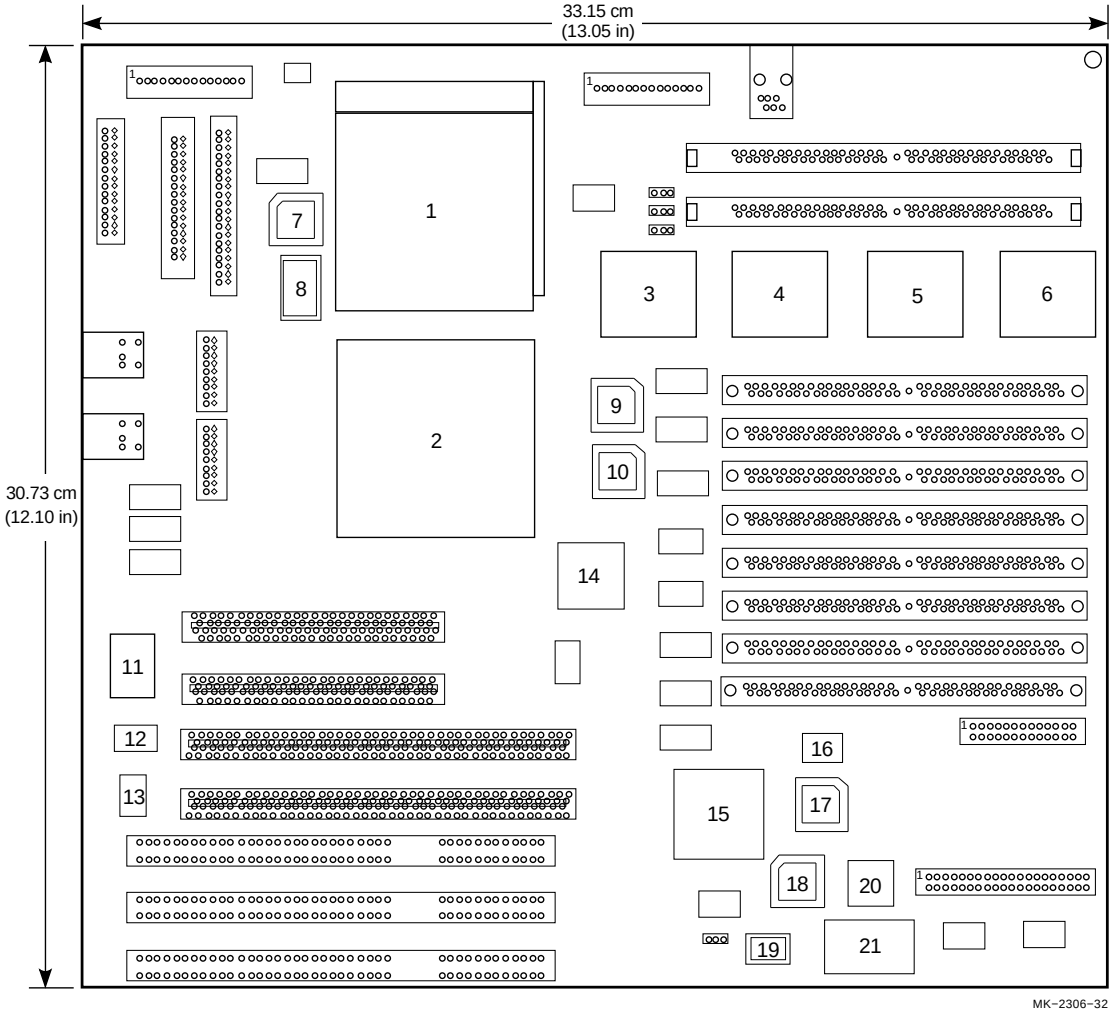
- Download files through serial and Ethernet ports and diskette.
- Load data from a ROM through the debug monitor.
- Examine and deposit the EB164 system registers, a few 21164 internal processor registers (IPRs), and I/O mapped registers.
- Examine and modify DRAM and I/O mapped memory.
- Disassemble CPU instructions in memory.
- Transfer control to programs in memory.
- Perform native debugging operations, including breakpoints and single stepping.
- Perform full source-level debugging operations by using DECladebug software running on a host communicating through an Ethernet connection.
- Perform a memory image dump.

1.1.8 Component Layout

Figure 1–2 shows the EB164 board component layout and dimensions.

1.1 System Components and Features

Figure 1–2 Board Component Layout



1.2 EB164 Summary

The features of the EB164 are listed and described in Table 1–2.

1.2 EB164 Summary

Table 1–2 EB164 Features Summary

Characteristic	Description
Operating Systems	
Supported operating systems	Microsoft Windows NT. For information on Digital UNIX operating system support, see your local distributor or your Digital sales representative.
System Characteristics	
CPU and clock speed	Digital Semiconductor 21164 Alpha microprocessor at 266, 300, or 333 MHz
CPU upgradable	ZIF socket for 21164 upgrade
Instruction issue	Up to 4 instructions issued per clock cycle
Word size	64 bits
Address size	40-bit physical address, 43-bit virtual address
Floating-point format	VAX (F and G) and IEEE (S and T) data types
Memory (DRAM)[1]	Minimum DRAM 32MB plus ECC Maximum DRAM 512MB plus ECC
Memory (ROM)	1MB flash ROM
External L2 cache	Configurable for 2MB, 4MB, 8MB (128-bit data)
Memory bus width	256 bits plus ECC
Performance metrics	The EB164 performance is listed here:

21164	Bcache	SPECint92	SPECfp92
266 MHZ	2MB, 10ns	300.6	417.4
300 MHZ	2MB, 10ns	335 (estimated)	460 (estimated)
333 MHZ	2MB, 10ns	365.2	518

Graphics	
Graphics options	Refer to the Microsoft *Hardware Compatibility List* for Windows NT to determine which graphics cards are supported. See Section B.4 for information on how to obtain the listing.

[1]Minimum DRAM recommended: 32MB for Windows NT and Digital UNIX.

(continued on next page)

1.2 EB164 Summary

Table 1–2 (Cont.) EB164 Features Summary

Characteristic	Description
Input/Output	
Input device interfaces	PS/2 style keyboard and mouse
Serial	Two RS423-compatible (9-position) serial communications ports
Parallel	One parallel (Centronics compatible) communications port
Bus options	Total of 6 option slots
PCI bus	Supports two 64-bit PCI options slots at 5V and two 32-bit PCI option slots at 5V
ISA bus	Supports three 16-bit ISA option slots
IDE	One IDE interface supporting up to 2 drives
Diskette	One 82077-compatible diskette controller supporting up to 2 drives with 1.44MB and 2.88MB formats
Environmental Characteristics (Operating)	
Operating temperature	10°C to 40°C (50°F to 104°F)
Maximum rate of (dry bulb) temperature change	11°C/hour ±2°C/hour (20°F/hour ±4°F/hour)
Relative humidity Maximum wet bulb Minimum dew point	10%–90% noncondensing 32°C (90°F) 2°C (36°F)
EMC compliance	Compliance certification is the responsibility of the system integrator. The EB164 was tested in industry-representative enclosures to prove feasibility of emissions compliance.
Shock and vibration	Passing of shock and vibration tests is dependent on the method used to mount the system board, the design of the enclosure, and how the enclosure is supported. Testing is the responsibility of the system integrator.
Physical Characteristics	
Form factor	Standard, full-size PC AT board
Width/depth	30.73 cm (12.10 in) × 33.15 cm (13.05 in)

2

System Configuration and Connectors

The EB164 uses jumpers to implement configuration parameters such as variations in backup cache (Bcache) size, access timing, and speed, as well as boot parameters. These jumpers must be configured for the user's environment. Onboard connectors are provided for the I/O interfaces, single inline memory modules (SIMMs), and serial and parallel peripheral ports.

After the module is configured, power can be applied, and the debug monitor can be run. The debug monitor and its commands are described in the *Alpha Microprocessors Evaluation Board Debug Monitor User's Guide*. Appendix B provides information about other software design tools.

2.1 Configuration Jumpers

Figure 2–1 identifies the location of the software and hardware configuration jumpers, and Table 2–1 provides descriptions. Figure 2–2 provides a detailed view of the configuration jumpers and their function.

2.1 Configuration Jumpers

Figure 2–1 EB164 Jumper Locations

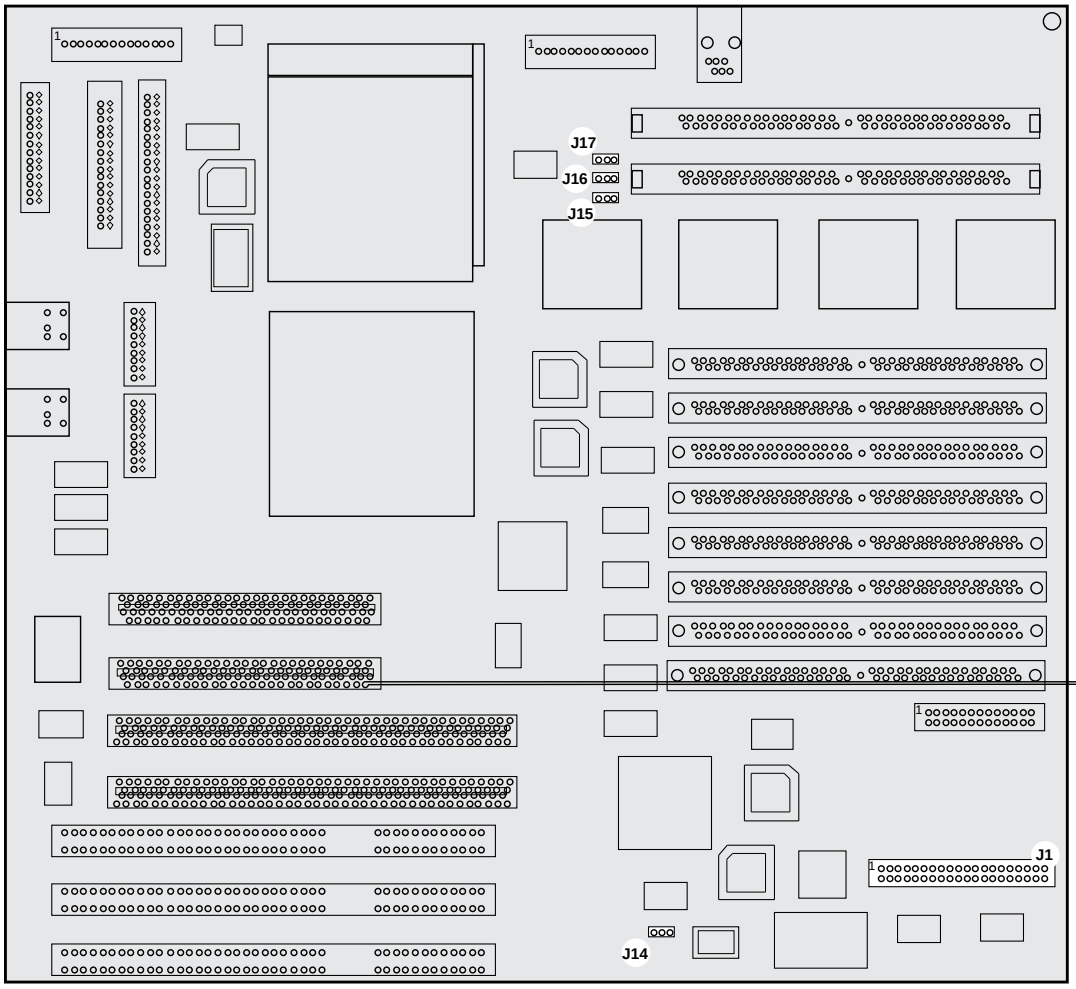


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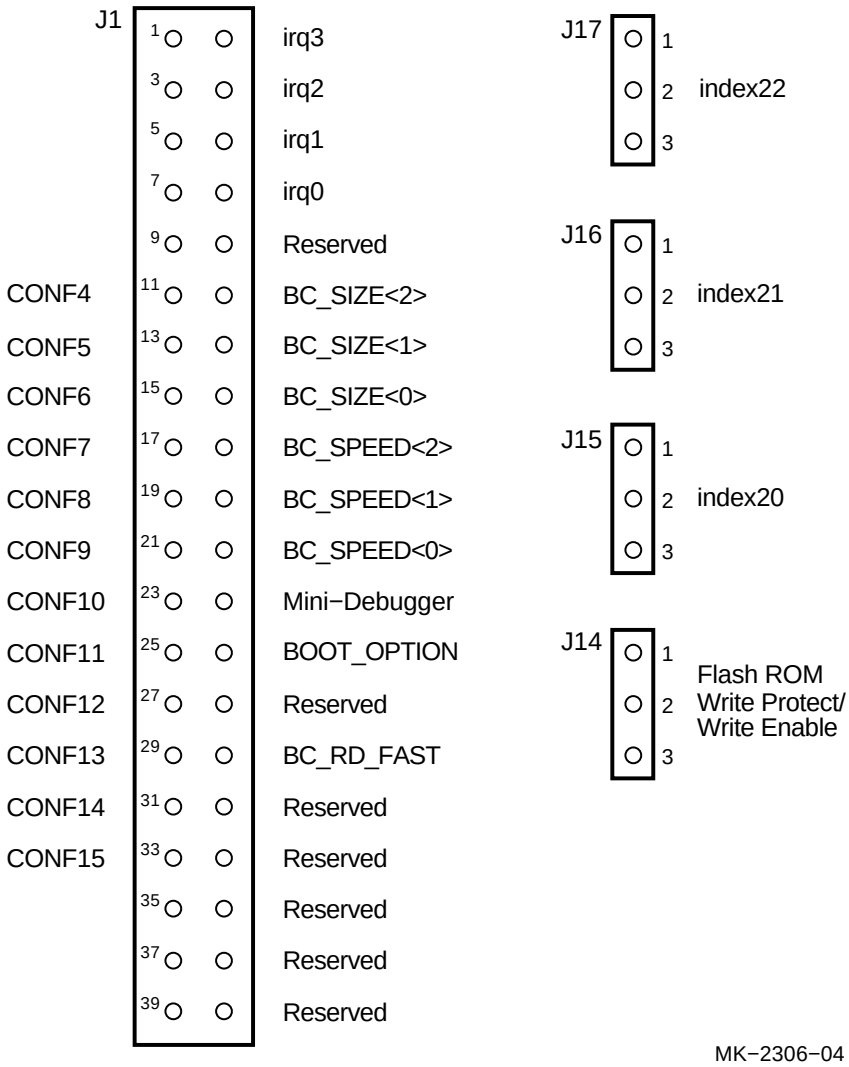
Figure 2–2 Configuration Jumpers



2.1 Configuration Jumpers

Table 2–1 Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description				
System clock divisor	J1—1/2, —3/4, —5/6, —7/8				
	J1—1/2 (irq3)	**J1—3/4 (irq2)**	**J1—5/6 (irq1)**	**J1—7/8 (irq0)**	**Ratio**
	In	In	Out	Out	3
	In	Out	In	In	4
	In	Out	In	Out	5
	In	Out	Out	In	6
	In	Out	Out	Out	7
	Out	In	In	In	8
	Divisor 8 is used for 266 MHz.				
	Out	In	In	Out	9
	Divisor 9 is used for 300 MHz.				
	Out	In	Out	In	10
	Divisor 10 is used for 333 MHz.				
	Out	In	Out	Out	11
	Out	Out	In	In	12
	Out	Out	In	Out	13
	Out	Out	Out	In	14
	Out	Out	Out	Out	15

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Table 2–1 (Cont.) Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description
BC_SIZE<2:0>	J1—11/12 (CONF4), —13/14 (CONF5), —15/16 (CONF6)

These jumpers allow the Bcache to emulate the sizes specified in the following table. These jumpers are changed in conjunction with the appropriate index jumpers J17, J16, and J15.

CONF4 Pins 11/12	CONF5 Pins 13/14	CONF6 Pins 15/16	Bcache
In	In	In	Reserved
In	In	Out	Reserved
In	Out	In	Reserved
In	Out	Out	2MB (default)
Out	In	In	4MB
Out	In	Out	8MB
Out	Out	In	Reserved
Out	Out	Out	Reserved

Bcache size–index address bits <22:20>

J17, J16, J15

Jumper	2MB[1] (default)	4MB[2]	8MB[2]
J17 (index22)	2 to 3	2 to 3	1 to 2
J16 (index21)	2 to 3	1 to 2	1 to 2
J15 (index20)	1 to 2	1 to 2	1 to 2

[1]SIMMs populated with 128K × 8 or 512K × 8 SRAMs

[2]SIMMs populated with 512K × 8 SRAMs

(continued on next page)

2.1 Configuration Jumpers

Table 2–1 (Cont.) Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description
BC_SPEED<2:0>	J1—17/18 (CONF7), —19/20 (CONF8), —21/22 (CONF9)

These jumpers select the Bcache timing parameters used to compute the BC_CONFIG register value. Select the jumper configuration that matches the access time for the SRAMs being used.

CONF7 Pins 17/18	CONF8 Pins 19/20	CONF9 Pins 21/22	Bcache Speed
In	In	In	Reserved
In	In	Out	6-ns SRAM timing
In	Out	In	8-ns SRAM timing
In	Out	Out	10-ns SRAM timing (default)
Out	In	In	12-ns SRAM timing
Out	In	Out	15-ns SRAM timing
Out	Out	In	Reserved
Out	Out	Out	Reserved

Mini-Debugger — J1—23/24 (CONF10)

The Alpha SROM Mini-Debugger is provided in the SROM. This jumper (In) causes the SROM initialization to trap to the Mini-Debugger (connector J13) after all initialization is complete, but before starting the execution of the system flash ROM code. The default position for this jumper is out.

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Table 2–1 (Cont.) Configuration Jumper Position Descriptions

Feature	Jack/Jumper—Pins and Description
BOOT_OPTION	J1—25/26 (CONF11) This jumper selects the image to be loaded into memory from the system flash ROM. With the jumper out (bit = 1), the first image (debug monitor) is loaded. With the jumper in (bit = 0), alternate images can be loaded depending upon the value stored in TOY RAM location 0x3F. The default position for this jumper is in. For system flash ROMs that contain a single image, the header is optional. If the header does not exist, the entire 1MB system flash ROM is loaded and executed at physical address zero. For more information on the system ROM header and boot images, refer to Section 4.5.1.
BC_RD_FAST	J1—29/30 (CONF13) This jumper forces a Bcache read speed setting of 1 cycle faster than nominal. **BC_RD_FAST** / **Bcache Speed** In / Make read speed 1 cycle faster Out / Nominal read speed (default)
Flash ROM write-protect/write-enable jumper	J14 **Jumper Pins** / **Function** 1 to 2 / Flash ROM write-protect 2 to 3 / Flash ROM write-enable (default)

2.2 EB164 Connectors

Figure 2–3 shows the EB164 connectors and Table 2–2 describes them. Figure 2–4 provides a detail of header connector J2.

Figure 2–3 EB164 Connector Locations

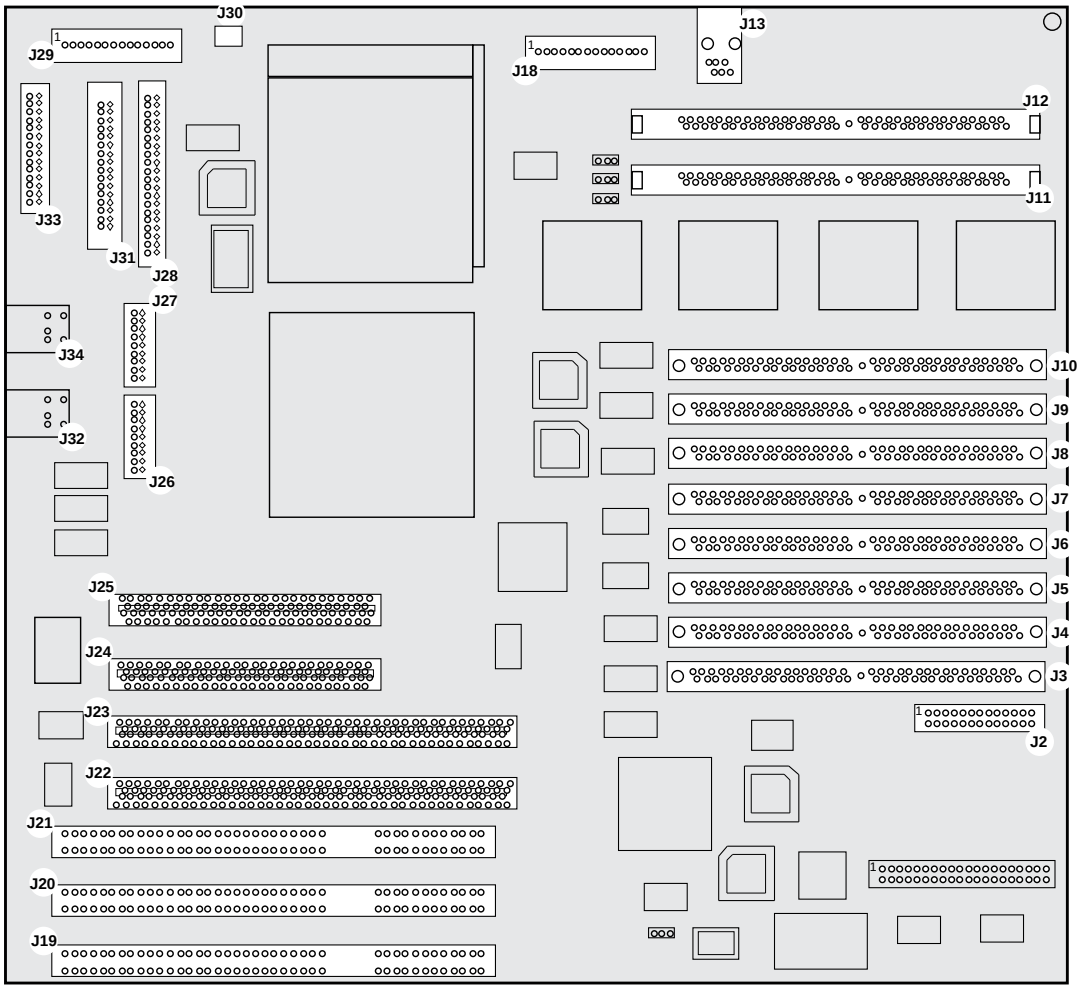

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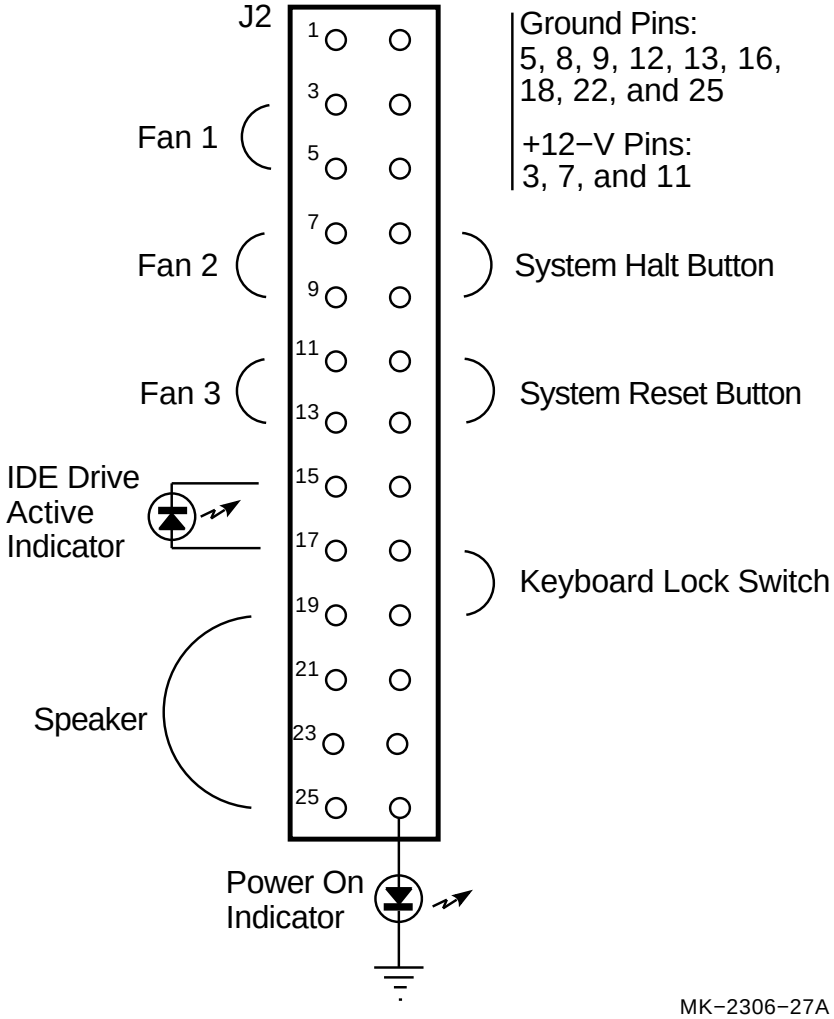
Figure 2–4 Detail of Header Connector J2



2.2 EB164 Connectors

Table 2–2 EB164 Connector Descriptions

Connector	Pins	Description
		Main Memory/Bcache SIMMs
J10	72	DRAM 0 SIMM
J9	72	DRAM 1 SIMM
J8	72	DRAM 2 SIMM
J7	72	DRAM 3 SIMM
J6	72	DRAM 4 SIMM
J5	72	DRAM 5 SIMM
J4	72	DRAM 6 SIMM
J3	72	DRAM 7 SIMM
		Note: To fill a 256-bit data path, all SIMM connectors J3 through J10 must be populated.
J11	60	Bcache 0 SIMM
J12	60	Bcache 1 SIMM
		Note: Both Bcache SIMM connectors must be populated.
		PCI Connectors
J22	184	PCI64 connector 0
J23	184	PCI64 connector 1
J24	124	PCI32 connector 2
J25	124	PCI32 connector 3
		ISA Connectors
J19	98	ISA connector slot 0
J20	98	ISA connector slot 1
J21	98	ISA connector slot 2
		Keyboard Connector
J32	6	Keyboard connector

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Table 2–2 (Cont.) EB164 Connector Descriptions

Connector	Pins	Description
		Mouse Connector
J34	6	Mouse connector
		National 87312 Combination Chip Connectors
J33	26	Parallel port connector Connects to an external 25-pin connector.
J27	10	Serial communication port 1 connector **Note:** This connector can be used as a terminal port for the debug monitor.
J26	10	Serial communication port 2 connector
J31	34	Diskette drive connector
J28	40	IDE drive connector
		SROM Data/Clock
J13	6	SROM data/clock serial port input connector **Note:** This connector can be used as a terminal port for the Mini-Debugger.
J2	26	Header connector J2 is a straight double-row header with standard 0.025-in pins on 0.10-in centers. Connections to it may be made by means of individual 2- or 4-pin female plugs. Figure 2–4 provides a detail of header connector J2.
		System Enclosure Fans
J2—3/5, —7/9, —11/13	2 each	Up to three 12-V cooling fans may be connected to these pins.
		IDE Drive Active Indicator
J2—15/17	2	IDE drive active indicator pins

(continued on next page)

2.2 EB164 Connectors

Table 2–2 (Cont.) EB164 Connector Descriptions

Connector	Pins	Description
		Speaker
J2—19/21/23/25	—	Speaker connector pins
		Power On Indicator
J2—26	1	Power on indicator pin
		Connect LED from this pin to ground.
		System Halt Button
J2—8/10	2	System halt button pins
		System Reset Button
J2–12/14	2	System reset button pins
		Keyboard Lock Switch
J2–18/20	2	Keyboard lock switch pins

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Table 2–2 (Cont.) EB164 Connector Descriptions

Connector	Pins	Description
		Power Connectors
J18	12	Board power connector

Pin	Voltage/Signal
1	+3.3 V
2	+3.3 V
3	+3.3 V
4	Ground
5	Ground
6	Ground
7	Ground
8	Ground
9	Ground
10	+3.3 V
11	+3.3 V
12	+3.3 V

(continued on next page)

2.2 EB164 Connectors

Table 2–2 (Cont.) EB164 Connector Descriptions

Connector	Pins	Description
J29	12	Board power connector

Pin	Voltage/Signal
1	**p_dcok**
2	**Vdd** (+5 V)
3	+12 V
4	–12 V
5	Ground
6	Ground
7	Ground
8	Ground
9	–5 V
10	**Vdd** (+5 V)
11	**Vdd** (+5 V)
12	**Vdd** (+5 V)

Note: Power for the EB164 is provided by a user-supplied power supply. Digital does not provide this power supply. (Refer to Chapter 5 for more information.)

J30 3 CPU fan power and sensor

Caution: Fan sensor required.

The fan *must* have a built-in sensor that drives a signal if the airflow stops. The sensor must be connected to pin J30—2. The fan supplied with the EB164 includes an airflow sensor.

3

Starting and Using the EB164

This chapter lists hardware, software, and accessories that users must obtain to completely furnish a functioning computer system. The chapter then describes how to configure the hardware and software. Finally, the chapter describes how to start and use the EB164.

3.1 Hardware Requirements

Before turning on the power to your EB164, you must provide the following components in addition to those supplied in the kit. The components needed depend upon the intended use of the EB164 board.

- A 21164 Alpha microprocessor (266-, 300-, or 333-MHz speed).
- If a 300-MHz or 333-MHz microprocessor is used, the oscillator must be changed. Refer to Appendix A for part numbers and sources. The board ships with parts to complement a 266-MHz microprocessor.
- Eight 72-pin, 36-bit, 5-V, DRAM SIMM memory modules (connectors J3 through J10). SIMMs must consist of identical devices. Digital recommends that all SIMMs be purchased from the same vendor.
- Two Alpha L3 cache SRAM SIMMs (connectors J11 and J12). Part numbers for 2MB cache sizes are listed in Appendix A.
- An industry-standard PC power supply that includes a 3.3-V dc output, rated at a minimum of 339 W (refer to Appendix A).
- A PS/2 compatible 101-key keyboard.
- A PS/2 compatible mouse.
- A supported PCI or ISA bus graphics card, cables, and a compatible monitor.
- A supported PCI or ISA bus SCSI controller and cables.
- A SCSI CD–ROM drive.
- An IDE or SCSI hard drive.

3.1 Hardware Requirements

- A 3.5-in diskette drive and cable.
- A 9-pin serial line cable.
- A terminal or a serial line connection to a host system with appropriate cables.

Refer to the *Alpha Microprocessors Evaluation Board Windows NT 3.51 Installation Guide* provided in the EB164 Windows NT 3.51 Installation Kit and the *Hardware Compatibility List* for Windows NT to determine which SCSI controllers and graphics cards are supported.

For more information about hardware requirements and for the location of board connectors and jumpers, see Chapter 2.

3.2 Software Requirements

The following software media is required to install and run the Windows NT operating system:

- A Windows NT 3.51 CD–ROM
- An EB164 Windows NT 3.51 installation diskette

3.3 Hardware Configuration

Once you have acquired the necessary hardware, it must be assembled into a system. This section lists the necessary steps. The system does not have to be assembled in the order presented. However, if you are installing the motherboard into an enclosure, Digital recommends that you install the microprocessor and heat sink first.

Caution: Static-Sensitive Component

Due to the sensitive nature of electronic components to static electricity, Digital strongly advises that anyone handling the 21164 Alpha microprocessor wear a properly grounded antistatic wrist strap. Use of antistatic mats, ESD approved workstation, or exercising other good ESD practices is recommended.

1. Install the 21164 Alpha microprocessor in ZIF socket U42.
   a. **Observe antistatic precautions.**
   b. Lift the ZIF socket actuator handle to a full 90° angle.
   c. Make sure that all the pins on the 21164 are straight.
   d. The ZIF socket and 21164 are keyed to allow for proper installation. Align the 21164, with its missing AD01 pin, with the corresponding plugged AD01 position on the ZIF socket. Gently lower into position.
   e. Close the ZIF socket actuator handle to its locked position.
2. If you are installing a 266-MHz microprocessor, you do not need to change any other components or associated jumper settings.

   If you are installing a 300-MHz or 333-MHz microprocessor, you must also reconfigure the clock divisor jumpers on header J1 as described in Table 2–1. You must also change the oscillator. Refer to Appendix A for part numbers and sources.
3. Install the heat sink and heat sink fan as directed in the following steps. Heat sinks and accompanying fans are available from Digital in kit form, or from recommended vendors as kits or component piece parts.

   A TS30 manual nut/torque driver with the following attachments is required to affix the heat sink and fan to a 21164:

   - 1/4-in hex bit
   - 7/16-in socket with 1/4-in hex drive
   - #2 Phillips screwdriver bit

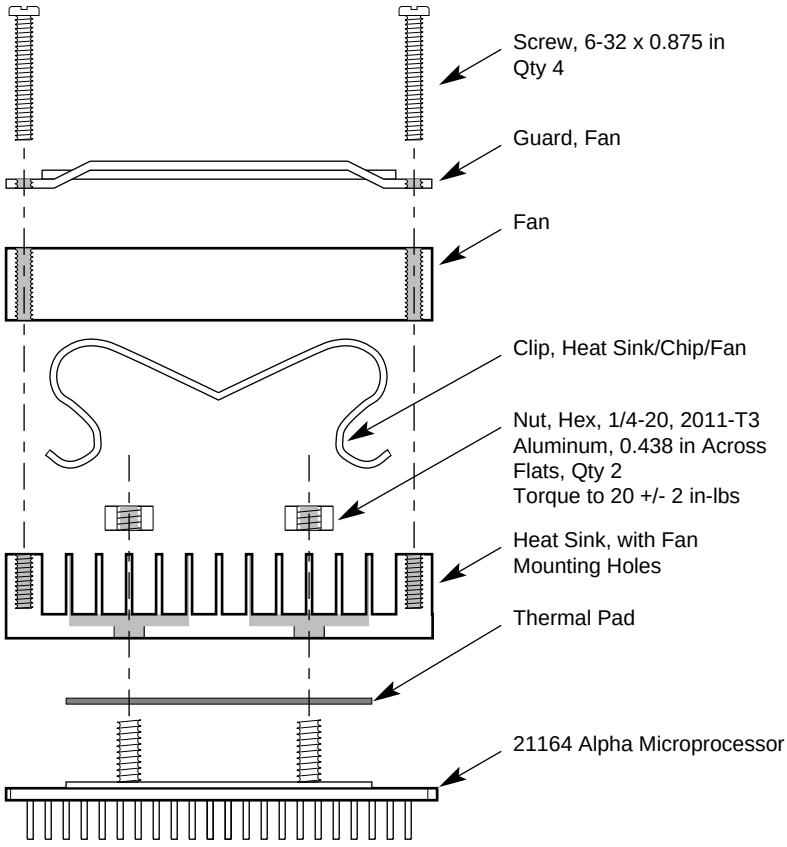
   Note

   Install the heat sink only after the 21164 has been assembled to the board ZIF socket.

3.3 Hardware Configuration

Refer to Figure 3–1 for heat sink and fan assembly details.

Figure 3–1 Fan/Heat Sink Assembly



a. Put the GRAFOIL thermal pad in place. The GRAFOIL pad is used to improve the thermal conductivity between the chip package and the heat sink by replacing micro air pockets with a less insulative material. Perform the following steps to position the GRAFOIL pad:

   1) Perform a visual inspection of the package slug to ensure that it is free of contamination.

2) Wearing clean gloves, pick up the GRAFOIL pad. Do *not* do this with bare hands because skin oils can be transferred to the pad.

3) Place the GRAFOIL pad on the gold-plated slug surface and align it with the threaded studs.

b. Attach the microprocessor heat sink. The heat sink material is clear anodized, hot-water-sealed, 6061-T6 aluminum. The nut material is 2011-T3 aluminum (this grade is critical). Perform the following steps to attach the heat sink:

1) **Observe antistatic precautions.**

2) Align the heat sink holes with the threaded studs on the ceramic package.

3) Handle the heat sink by the edges and lower it on to the chip package, taking care not to damage the stud threads.

4) Set a calibrated torque driver to 20 in-lb, ±2 in-lb, (2.3 N m, ±0.2 N m.) The torque driver should have a mounted 7/16-in socket.

5) Insert a nut into the 7/16-in socket, place on one of the studs, and tighten to the specified torque. Repeat for second nut.

6) If the sink/chip/fan clip is used, install it properly by positioning it over the assembly and hooking its ends around the ZIF socket retainers.

c. Perform the following steps to attach the heat sink fan assembly:

1) Place the fan assembly on top of the heat sink, aligning the fan mounting holes with the corresponding threaded heat sink holes. Align the fan so that the fan power/sensor wires exit the fan closest to connector J30 (see Figure 2–3). Fan airflow must be directed into the heat sink (fan label facing down toward the heat sink).

2) Place the fan guard on top of the fan. Orient the guard so that the corner mounting areas lay flush against the heat sink.

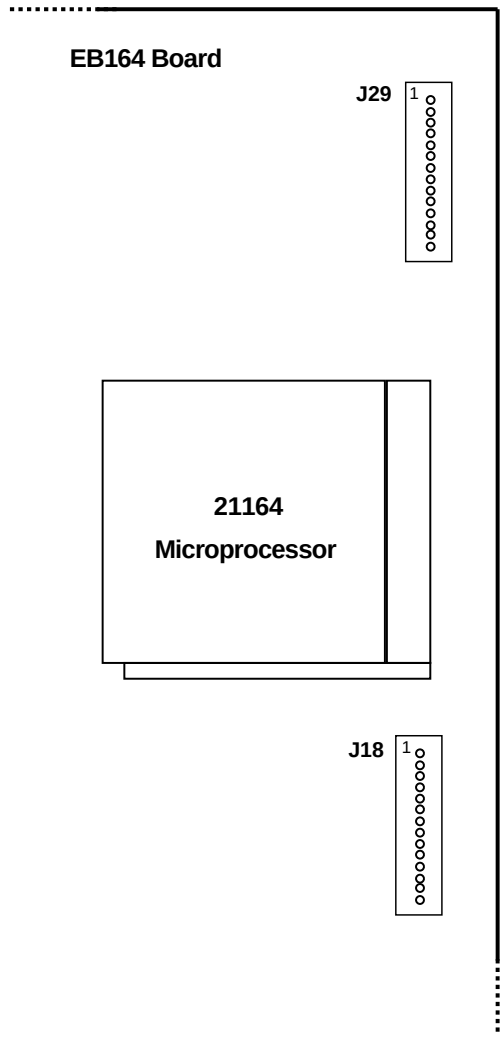
3) Secure the fan and fan guard to the heat sink with four 6–32 × 0.875-in screws.

4) Plug the fan power/sensor cable into connector J30 (see Figure 2–3).

3.3 Hardware Configuration

4. Install the two L3 cache SRAM SIMMs into sockets J11 and J12. Refer to Table 2–2 for socket locations.
5. Install eight system memory DRAM SIMMs. Refer to Table 2–2 for socket locations.
   a. **Observe antistatic precautions.** Handle SIMMs at the edges only to prevent damage.
   b. SIMMs must be installed in groups of eight consisting of identical devices.
   c. Hold the SIMM at an angle with the notch facing the key in the socket.
   d. Firmly push the module into the connector and stand the module upright.
   e. Make sure that the SIMM snaps into the metal locking clips on both ends.
6. If you intend to mount the motherboard in a system enclosure, do so now. Install the power supply into the enclosure first, then the motherboard. Appendix A lists a suggested enclosure and a suggested power supply. The enclosure you use should be able to accept a standard, full-size PC AT board.
7. Connect the power supply to the EB164 board, as shown in Figure 3–2, with standard power to J29, and with 3.3-V dc power to J18.
8. If you are using an enclosure, mount the 3.5-in diskette drive, hard drive, and CD–ROM drive. Refer to the manufacturer's instructions for installing these devices.
9. Connect the supplied 3.5-inch diskette drive. The 34-pin diskette drive cable goes from connector J31 on your EB164 to the diskette drive. The drive should be connected at the very end of the cable closest to the twist in the cable. Attach a power connector to the drive. Again, make sure to insert the connector in the proper orientation so that pin 1 on the cable matches pin 1 on the board header (as indicated on the module).
10. Install the SCSI controller in a free PCI or ISA connector and attach the CD–ROM drive. If you will be using a SCSI hard drive, install the hard drive now. Refer to the manufacturer's instructions for installing these devices. Verify that a unique SCSI ID is assigned to each device you attach to the SCSI bus.

Figure 3–2 EB164 Power Connectors



J29

Pin	Voltage/Signal
1	**p_dcok**
2	**Vdd** (+5 V)
3	+12 V
4	−12 V
5	Ground
6	Ground
7	Ground
8	Ground
9	−5 V
10	**Vdd** (+5 V)
11	**Vdd** (+5 V)
12	**Vdd** (+5 V)

J18

Pin	Voltage/Signal
1	+3.3 V
2	+3.3 V
3	+3.3 V
4	Ground
5	Ground
6	Ground
7	Ground
8	Ground
9	Ground
10	+3.3 V
11	+3.3 V
12	+3.3 V

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11. If you will be using an IDE hard drive, attach your IDE cable to connector J28 in the proper orientation and install your hard drive. The disk should be configured as the primary device on the IDE bus. Refer to the manufacturer's instructions for setting up the hard drive.
12. If you plan to use your EB164 on a network, install the Ethernet controller board (DE435) in one of the PCI connectors as outlined in the DE435 documentation.
13. Install the graphics card into either a PCI or ISA connector, depending on the card you are using. Connect the graphics card to a compatible monitor following the graphics card manufacturer's instructions.
14. Connect the keyboard cable to connector J32.
15. Connect the mouse cable to connector J34.
16. Connect the 9-pin serial port adapter cable, provided in the kit, to the COM1 connector at J27. Insert the connector in the proper orientation, so that pin 1 on the cable matches pin 1 on the board header (as indicated on the module).
17. Connect your terminal to the COM1 port, using a cable arrangement appropriate to your terminal. Set the terminal to 9600 baud, 8 data bits, 1 stop bit, no parity.
18. Connect miscellaneous items such as, enclosure fans, reset button, speaker, power indicator, hard drive active indicator (if using an IDE drive), keyboard lock switch, and so forth.

3.4 Software Configuration

Two firmware programs have been loaded into the EB164 1MB flash ROM. They are the debug monitor and the Windows NT ARC firmware. The debug monitor is a serial line monitor program used to perform software and hardware debug functions. The Windows NT ARC firmware is used to load and boot Windows NT. The EB164 system has been configured to start the Windows NT ARC firmware by default.

The serial ROM firmware uses a value stored in the nonvolatile RAM of the real-time clock to determine which firmware image to load. Once the Windows NT ARC firmware is running, you can switch to the debug monitor firmware.

3.4.1 Starting Windows NT ARC Firmware

Start the Windows NT ARC firmware using the following procedure.

1. Verify that the jumper from J14-2 to J14-3 is inserted, allowing the flash ROM to be written. If the Windows NT ARC firmware is unable to write to flash ROM, it prints the `device error` message and stops.
2. Verify that the jumper at J1–25/26 is installed (see CONF11 on the module). The presence of the jumper at J1–25/26 forces the serial ROM firmware to load the alternate image selected by the value in the nonvolatile TOY RAM. The absence of this jumper overrides the value stored in the TOY RAM and causes the first image, the debug monitor, to be loaded.
3. Turn on the power to the EB164. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display.

   If the ARC console boot menu does not appear, check the output of COM1 for error messages and review your hardware configuration.

   You are ready for software installation. Refer to the *Alpha Microprocessors Evaluation Board Windows NT 3.51 Installation Guide* for instructions.

3.4.2 Going to the Debug Monitor from Windows NT ARC Firmware

You may use either of these two methods to access the debug monitor from the Windows NT ARC firmware.

A. Use the ARC firmware menus to choose the debug monitor.
   1. At the Boot menu, choose **Supplementary menu...**.
   2. At the Supplementary menu, choose **Setup the system...**.
   3. At the Setup the system menu, choose **Machine specific setup...**.
   4. At the Machine specific setup menu, choose **Debug Monitor**.
   5. Turn off the power to the EB164, then turn the power back on.

B. Turn off the power to the EB164, remove the jumper from J1-25/26 (CONF11 on the module), then turn on the power to the EB164.

3.4.3 Returning to Windows NT ARC Firmware from the Debug Monitor

The following methods may be used to return to the Windows NT ARC firmware from the debug monitor.

A. If you used item A in section Section 3.4.2 to enter the debug monitor, then use this procedure to return to Windows NT ARC firmware.
The firmware contained in the serial ROM on your EB164 determines which firmware image is loaded from the flash ROM at power-up. The serial ROM firmware uses a value stored in the nonvolatile RAM of the real-time clock to determine which firmware image to load. At this point, you want the serial ROM to load the Windows NT ARC firmware.

1. Use the following debug monitor commands to select Windows NT ARC firmware, by writing the value 1 to the TOY RAM. and to verify the selection:

```
EB164> bootopt nt

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

EB164> bootopt

Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

EB164>
```

Note

The EB164 does not support the OpenVMS operating system.

2. Turn off power to the EB164. Verify the presence of a jumper at J1–25/26 (see CONF11 on the module).
3. Turn on the power to the EB164. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display.

B. If you used item B in section Section 3.4.2 to enter the debug monitor, then use this procedure to return to Windows NT ARC firmware.

   1. Turn off the power to the EB164, insert the jumper from J1-25/26 (CONF11 on the module).
   2. Turn on the power to the EB164. After the power-up diagnostics are run, the ARC console boot menu appears on the graphics display. If the ARC console boot menu does not appear, check the output of COM1 for error messages and review your hardware configuration.

4
Functional Description

This chapter describes the functional operation of the EB164. The description introduces the Digital Semiconductor 21171 ASIC support chipset and describes its implementation with the 21164 microprocessor, its supporting memory, and I/O devices. Figure 1–1 shows the EB164 major functional components.

Information, such as bus timing and protocol, found in other data sheets and reference documentation is not duplicated. See Appendix B for a list of supporting documents and order numbers.

Note

For detailed descriptions of bus transactions, chipset logic, and operation, refer to the *Alpha 21164 Microprocessor Hardware Reference Manual* and the *DECchip 21171 Core Logic Chipset Technical Reference Manual*.

For details of the PCI interface, refer to the *PCI System Design Guide*.

4.1 PCI Interrupts and Arbitration

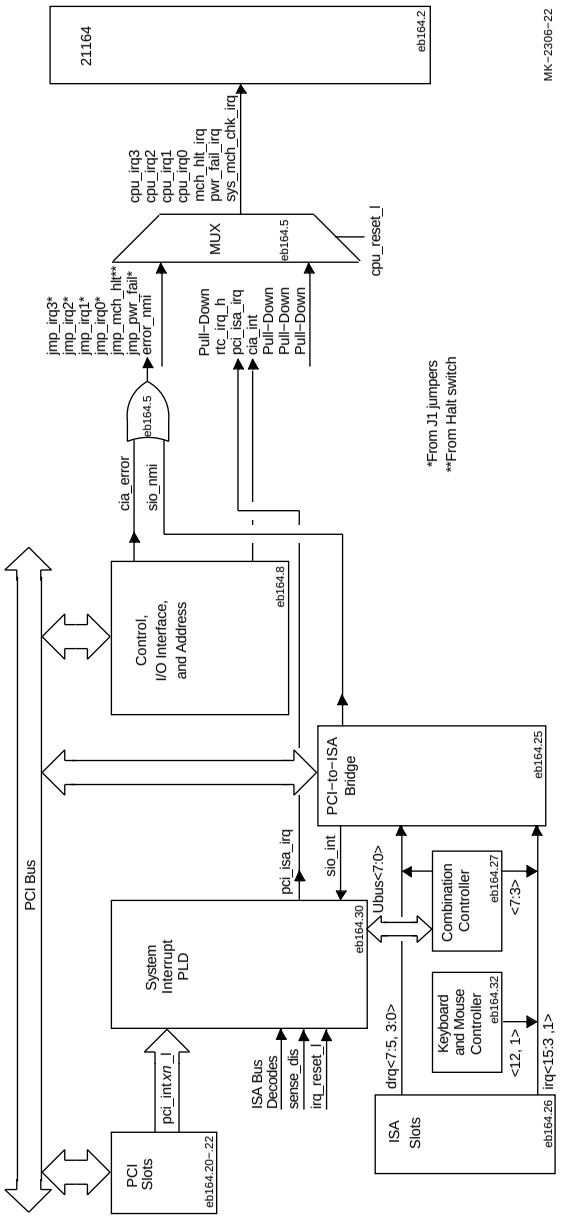
The following sections describe the EB164 interrupt and arbitration (arbiter) logic.

4.1.1 Interrupts

PCI-, ISA-, and CIA-generated interrupts are each described. Figure 4–1 shows the interrupt logic.

4.1 PCI Interrupts and Arbitration

Figure 4–1 Interrupt Logic



4.1 PCI Interrupts and Arbitration

The PCI-to-ISA SIO bridge chip provides the functionality of two 8259 interrupt control devices. These ISA-compatible interrupt controllers are cascaded such that 14 external and two internal interrupts are available. The PCI interrupt acknowledge command should be used to read the interrupt request vector from the SIO.

However, the EB164 has more interrupt signals than the 14 external interrupts the SIO can handle. Therefore, all the ISA interrupts are sent to the SIO except for the two CIA interrupts, the time-of-year (TOY) interrupt, and the 16 PCI interrupts. They are sent to an external interrupt PAL. This PAL takes these interrupts, as well as an OR of the nonexistent memory (NMI) and error signals from the SIO, and generates **cpu_irq<3:0>**. During reset, **cpu_irq<3:0>** convey the system clocking ratios and delays, which are set by jumpers on J1.

Table 4–1 lists each system interrupt, its fixed interrupt priority level (IPL), and its EB164 implementation. Table 4–2 lists each SIO interrupt and its EB164 implementation.

Table 4–1 EB164 System Interrupts

21164 Interrupt	IPL[1]	Suggested Usage	EB164 Usage
cpu_irq<0>	20	Corrected system error	Corrected ECC error and sparse space reserved encodings detected by CIA
cpu_irq<1>	21	—	PCI and ISA interrupts
cpu_irq<2>	22	Interprocessor and timer interrupts	Time-of-year clock interrupt
cpu_irq<3>	23	—	Reserved
pwr_fail_irq	30	Powerfail interrupt	Reserved
sys_mch_chk_irq	31	System machine check interrupt	SIO NMI and CIA errors
mch_hlt_irq	—	Halt	Reserved

[1]IPL = interrupt priority level (fixed)

4.1 PCI Interrupts and Arbitration

Table 4–2 PCI-to-ISA SIO Bridge Interrupts

Priority	Label	Controller	Internal/External	Interrupt Source
1	IRQ0	1	Internal	Internal timer 1
2	IRQ1	1	External	Keyboard
3–10	IRQ2	1	Internal	Interrupt from controller 2
3	IRQ8#[1]	2	External	Reserved
4	IRQ9	2	External	ISA bus pin B04
5	IRQ10	2	External	ISA bus pin D03
6	IRQ11	2	External	ISA bus pin D04
7	IRQ12	2	External	Mouse
8	IRQ13	2	External	Reserved
9	IRQ14	2	External	IDE
10	IRQ15	2	External	ISA bus pin D06
11	IRQ3	1	External	87312 combination controller
12	IRQ4	1	External	87312 combination controller
13	IRQ5	1	External	87312 combination controller
14	IRQ6	1	External	87312 combination controller
15	IRQ7	1	External	87312 combination controller

[1]The # symbol indicates an active low signal.

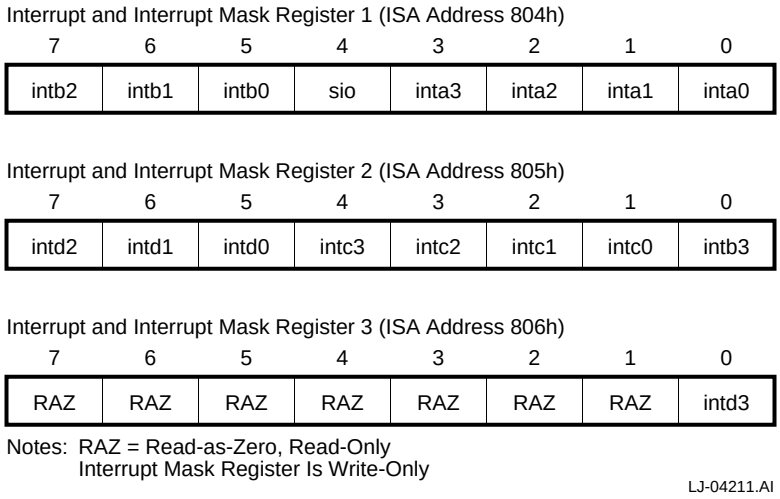
Interrupt PLDs Function

The MACH210A PLD is an 8-bit I/O slave on the ISA bus at hex addresses 804, 805, and 806. This is accomplished by a decode of the three ISA address bits **sa<2:0>** and the three **ecas_addr<2:0>** bits.

Each interrupt can be individually masked by setting the appropriate bit in the mask register. An interrupt is disabled by writing a 1 to the desired position in the mask register. An interrupt is enabled by writing a 0. For example, bit <7> set in interrupt mask register 1 indicates that the INTB2 interrupt is disabled. There are three mask registers located at ISA addresses 804, 805, and 806.

An I/O read transaction at ISA addresses 804, 805, and 806 returns the state of the 17 PCI interrupts rather than the state of the masked interrupts. On read transactions, a 1 means that the interrupt source shown in Figure 4–2 has asserted its interrupt. The mask register can be updated by writing addresses 804, 805, or 806. The mask register is write-only.

Figure 4–2 Interrupt and Interrupt Mask Registers



4.1.2 Arbitration

Arbitration logic is implemented in the Intel 82378ZB Saturn I/O (SIO) chip. The arbitration scheme is flexible and software programmable. Refer to the Intel *82420/82430 PCIset ISA and EISA Bridges* document for more information about programmable arbitration.

4.2 ISA Bus Devices

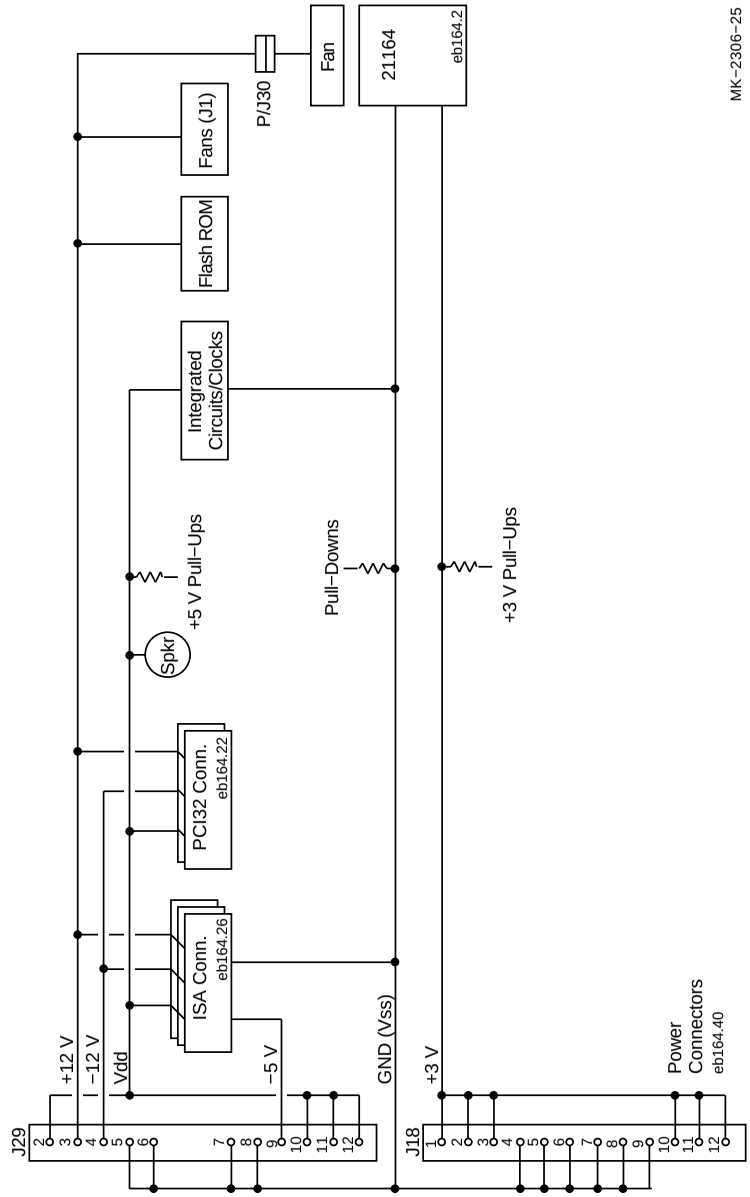
Two dedicated ISA expansion slots are provided in addition to the combination ISA/PCI slot. System support features such as serial lines, parallel port, integrated device electronics (IDE), and diskette controller are embedded on the module by means of an 87312 combination controller chip. Also shown is the utility bus (Ubus) with its system support devices.

4.3 dc Power Distribution

The EB164 derives its system power from a user-supplied PC power supply. The power supply must provide +12 V dc and –12 V dc, –5 V dc, +3 V dc, and **Vdd** (+5 V dc). The dc power is supplied through power connectors J18 and J29. (See Figure 4–3.) Power is distributed to the board logic through dedicated power planes within the 6-layer board structure.

4.3 dc Power Distribution

Figure 4–3 dc Power Distribution



As shown in Figure 4–3, the +12 V dc, –12 V dc, and –5 V dc are supplied to ISA connectors J19, J20, and J21. The +12 V dc and –12 V dc are supplied to ISA connectors and PCI32 connectors J24 and J25. The +12 V dc is also supplied to the CPU fan connector J30, auxiliary fan connector pins on header J2, and to the flash ROM write-enable conector J14. **Vdd** is supplied to ISA connectors, PCI32 connectors and most of the board's integrated circuits. The +3 V dc is supplied to the 21164 microprocessor.

4.4 PCI Devices

The EB164 uses the PCI bus as the main I/O bus for the majority of peripheral functions. The board implements the ISA bus as an expansion bus for system support functions and relatively slow peripheral devices.

The PCI bus supports multiplexed, burst mode, read and write transfers. It supports synchronous operation of between 25 MHz and 33 MHz. It also supports either a 32-bit or 64-bit data path with 32-bit device support in the 64-bit configuration. Depending upon the configuration and operating frequencies, the PCI bus supports anywhere between 100MB/s (25-MHz, 32-bit) to 264MB/s (33-MHz, 64-bit) peak throughput. The PCI provides parity on address and data cycles. Three physical address spaces are supported:

1. 32-bit memory space
2. 32-bit I/O space
3. 256-byte-per-agent configuration space

The bridge from the 21164 system bus to the 64-bit PCI bus is provided by the CIA chip. It generates the required 32-bit PCI address for 21164 I/O accesses directed to the PCI. It also accepts 64-bit double address cycles and 32-bit single address cycles. However, the 64-bit address support is subject to some constraints.

4.5 Flash ROM

The flash ROM, sometimes called the system ROM, is a 1MB, nonvolatile, writable ROM. After the serial ROM (SROM) code initializes the EB164 system, the flash ROM code prepares the system for booting. The flash ROM headers, structure, and access methods are described here.

4.5.1 Special ROM Header

The MAKEROM tool is used to place a special header on ROM image files. The SROM allows the system (flash) ROM to contain several different ROM images, each with its own header. The header informs the SROM where to load the image, and whether or not it has been compressed with the MAKEROM tool. The header is optional for system ROMs containing a single image. If the header does not exist, the complete 1MB system flash ROM is loaded and executed starting at physical address zero. Figure 4–4 shows the header content.

Figure 4–4 Special Header Content

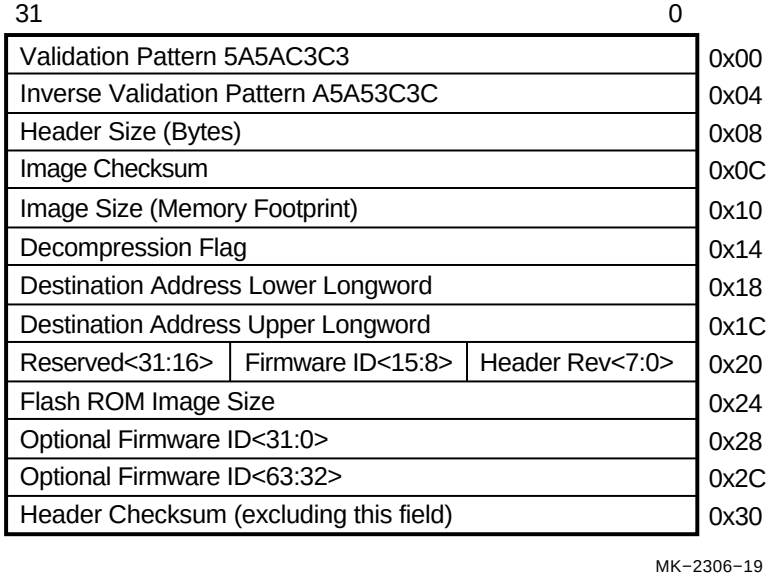


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Table 4–3 describes each entry in the special header.

Table 4–3 Special Header Entry Descriptions

Entry	Description
Validation and inverse validation pattern	This quadword contains a special signature pattern used to validate that the special ROM header has been located. The pattern is 5A5AC3C3A5A53C3C.
Header size (bytes)	This longword provides the size of the header block, which varies among versions of the header specification. When the header is located, SROM code determines where the image begins based on the header size. Additional data added to the header is ignored by older SROM code. A header size of 32 bytes implies version 0 of the header specifications.
Image checksum	This longword is used to verify the integrity of the ROM.
Image size	The image size is used by the SROM code to determine how much of the system flash ROM should be loaded.
Decompression flag	The decompression flag informs the SROM code whether the MAKEROM tool was used to compress the ROM image with a repeating byte algorithm. The SROM code contains routines that execute the decompression algorithm. Other compression and decompression schemes, which work independently from this scheme, may be employed.
Destination address	This quadword contains the destination address for the image. The SROM code loads the image at this address and begins execution.
Firmware ID	The firmware ID is a byte that specifies the firmware type. This information facilitates image boot options necessary to boot different operating systems.

Firmware Name	Firmware Type	Firmware Description
Debug monitor	0	Alpha evaluation board debug monitor
Windows NT	1	Windows NT ARC firmware
Alpha SRM	2	Alpha System Reference Manual console

(continued on next page)

4.5 Flash ROM

Table 4–3 (Cont.) Special Header Entry Descriptions

Entry	Description
Header revision	The revision of the header specification used in this header. This is necessary to provide for changes to the header specification. Version 0 headers are identified by the size of the header (32 bytes).
Flash ROM image size	The flash ROM image size reflects the size of the image as it is contained in the flash ROM.
Optional firmware ID	This optional field can be used to provide additional firmware information such as firmware revision or a character descriptive string of up to 8 characters.
Header checksum	The checksum of the header. This is used to validate the presence of a header beyond the validation provided by the validation pattern.

4.5.2 Flash ROM Structure

During the power-up and initialization sequence, the EB164 always loads the first image if BOOT_OPTION=1 (jumper J1—25/26 not installed). Then the first image (the debug monitor) will be booted.

If jumper J1—25/26 (BOOT_OPTION) is installed (see Figure 2–2), the EB164 reads the value at location 0x3F of the TOY RAM. The EB164 uses the value found there to determine which image will be selected (see Table 4–4). The selected image is loaded and executed.

Table 4–4 Flash ROM Image Selection

TOY RAM Value[1]	Firmware ID[2]	Image Description
0x00	0	Evaluation board debug monitor firmware
0x01	1	Windows NT ARC firmware
0x02	2	Alpha SRM firmware (OpenVMS)[3]
0x03	2	Alpha SRM firmware (Digital UNIX)[3]
0x8*n*	NA[4]	SROM code loads the *n*th image from flash ROM. If *n*=0, the SROM code loads the entire flash ROM contents. If *n*=1, 2, . . . , the SROM code loads the first image, second image, and so on.

[1]Operating system type. Found at TOY RAM address 0x3F.

[2]Found in image header.

[3]**Note:** SRM firmware is not included in the EB164 kit. The flash ROM contains only one of these images.

[4]Not applicable.

If an image is specified and is not found, the EB164 loads the first image found in the flash ROM with a valid header. If no valid header is found, the entire 1MB flash image is loaded at address 0x00000000.

The following sequence of steps describes how to change the value stored in TOY RAM location 0x3F by using either the basic debug monitor commands or the debug monitor `bootopt` command.

4.5 Flash ROM

Changing TOY RAM Location 0x3F—Debug Monitor `bootopt` Command

Use the debug monitor `bootopt` command to change the value in location 3F. In the example shown here, the `bootopt` command is used to change the value in location 3F from 0 to 1:

```
EB164> bootopt      ❶

Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"

O/S type selected: "Alpha Evaluation Board Debug Monitor"
....Firmware type: "DBM Firmware"

EB164> bootopt nt   ❷

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

EB164> bootopt      ❸

Predefined bootoptions are...
  "0" "Alpha Evaluation Board Debug Monitor" "DBM"
  "1" "The Windows NT Operating System" "NT"
  "2" "OpenVMS" "VMS"
  "3" "Digital UNIX" "UNIX"

O/S type selected: "The Windows NT Operating System"
....Firmware type: "Windows NT Firmware"

EB164>
```

❶ Use the debug monitor `bootopt` command to see the image choices and note which image is selected.

❷ Use the debug monitor `bootopt nt` command to change the selected image from 0 to 1.

❸ Use the debug monitor `bootopt` command to verify that the selected image has changed from 0 to 1.

4.5.3 Flash ROM Access

The flash ROM can be viewed as two banks of 512KB each. At power-up the lower 512KB bank is accessed using the address range 86.FFF8.0000 to 86.FFFF.FFFF.

Setting address bit 19 (**flash_adr19**) allows you to access the higher 512KB of flash ROM. Write a 1 to the register at address 0x800 to set address bit 19. Manually deposit a 1 to address 0x800 or enter the following command from the debug monitor:

```
> wb 800 1
```

The address range for the higher bank is 86.FFF8.0000 to 86.FFFF.FFFF, the same as for the lower bank. Access is now to the higher bank and will continue until the EB164 is reset, or a 0 is written to the register at address 0x800.

Note

The write-enable jumper must be installed at J14—2/3 (see Figure 2–1 and Figure 2–2). This enables writing to the flash ROM.

5

EB164 Requirements, Power, and Parameters

This chapter describes the EB164 environmental requirements, power, and physical board parameters.

5.1 Power Requirements

The EB164 derives its main dc power from a user-supplied power supply. The board has a total power dissipation of 116 W, excluding any plug-in PCI and ISA devices. Table 5–1 lists the power requirement for each dc supply voltage.

The power supply must supply a **dcok** signal to the system reset logic.

Table 5–1 Power Supply dc Current Requirements

Voltage	Current[1]
+3.3 V dc	16.0 A
+5 V dc	10.0 A
–5 V dc	0 A
+12 V dc	1.0 A
–12 V dc	100.0 mA

[1]Values indicated are for a fully populated EB164 system module excluding plug-in PCI and ISA devices, with a CPU clock speed of 266 MHz.

Caution: Fan Sensor Required

The 21164 cooling fan *must* have a built-in sensor that will drive a signal if the airflow stops. The sensor is connected to EB164 board connector J30. When the signal is generated, it resets the system.

5.2 Environmental Requirements

The 21164 microprocessor is cooled by a small fan blowing directly into the chip's heat sink. The EB164 motherboard is designed to run efficiently using only this fan. Additional fans may be necessary depending upon cabinetry and I/O board requirements.

The EB164 is specified to run within the following environment:

Parameter	Specification
Operating temperature	10°C to 40°C (50°F to 104°F)
Storage temperature	–55°C to 125°C (–67°F to 257°F)
Relative humidity	10% to 90% with maximum wet bulb temperature 28°C (82°F) and minimum dew point 2°C (36°F)
Rate of (dry bulb) temperature change	11°C/hour ±2°C/hour (20°F/hour ±4°F/hour)

5.3 Physical Board Parameters

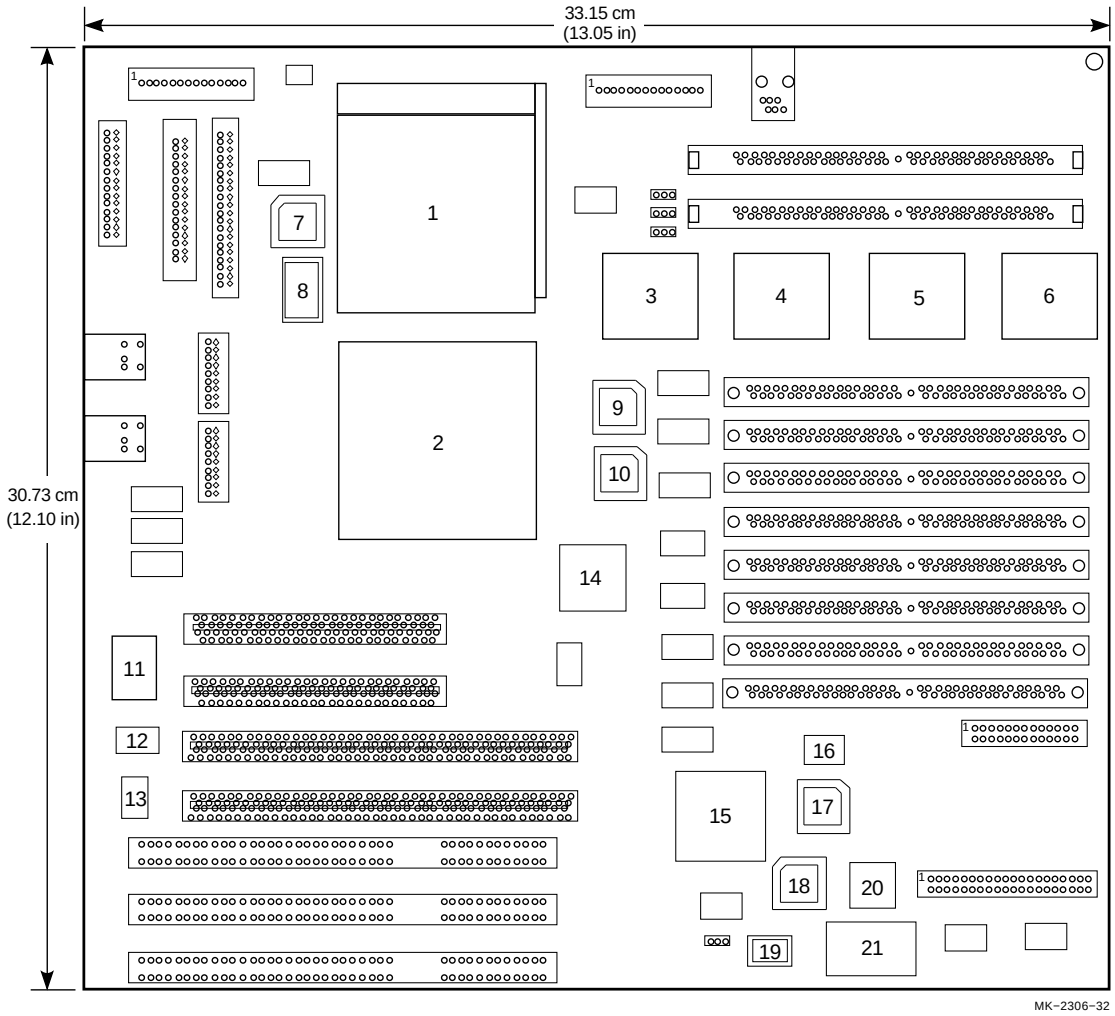
The EB164 board consists of a 6-layer printed-wiring board (PWB) with components mounted to side 1 only. The board is populated with integrated circuit packages together with supporting active and passive components. The EB164 is a standard, full-size PC AT board with the following dimensions:

- Width: 30.73 cm (12.10 in ±0.0005 in)
- Length: 33.15 cm (13.05 in ±0.0005 in)
- Height: 6.0 cm (2.375 in)

The board can be used in certain desktop and deskside systems that have adequate clearance for the 21164 heat sink and fan. All ISA and PCI expansion slots are usable in standard desktop or deskside enclosures.

Figure 5–1 shows the board and component outlines, and identifies the major components. Table 5–2 lists the components. Refer to Chapter 2 for jumper and connector functions and locations.

Figure 5–1 Board Component Layout



5.3 Physical Board Parameters

Table 5–2 Board Component List

Locator Number	Component Number	Component Description
1	U42	Digital Semiconductor 21164 Alpha microprocessor
2	U41	21171-CA control, I/O interface, and address (CIA) chip
3	U32	21171-BA data switch (DSW0) chip
4	U15	21171-BA data switch (DSW2) chip
5	U10	21171-BA data switch (DSW1) chip
6	U2	21171-BA data switch (DSW3) chip
7	U50	TriQuint TQ2061 phase-locked loop (PLL) clock chip
8	U49	26.66-MHz clock oscillator
9	U31	Main memory row address strobe (RAS) PAL
10	U30	Main memory row address strobe (RAS) PAL
11	U58	National 87312 combination chip
12	U57	ISA clock frequency generator chip
13	X2	14.318-MHz clock oscillator
14	U33	Motorola 88PL117 phase-locked loop (PLL) system clock chip
15	U17	Intel 82378ZB PCI-to-ISA SIO bridge chip
16	U12	Xilinx serial ROM (initialization code) chip
17	U11	MACH210A interrupt request and PCI arbiter PAL
18	U13	Ubus decoder PAL
19	U14	Flash ROM chip
20	U7	Intel 8242 mouse and keyboard controller chip
21	U6	Dallas Semiconductor DS1287 time-of-year (TOY) clock chip

A

Supporting Vendor Products

To obtain components and accessories that are not included with your EB164 motherboard, Digital Equipment Corporation suggests the following vendors. In doing so, Digital does not warrant these components or guarantee that they will function in all configurations.

A.1 Products Included

The following products are included in the EB164 motherboard kit.

- Alpha microprocessor clock solution. Components available from:

  TriQuint Semiconductor
  2300 Owen Street
  Santa Clara CA 95054
  Phone: 408–982–0900 ext 142
  FAX: 408–982–0222

  NEL Frequency (crystal oscillator source)

CPU Frequency	Oscillator Frequency	TriQuint PLL Part Number
21164-266	26.66 MHz (included)	TQ2061 (included)
21164-300	30.0 MHz (not supplied)	TQ2061 (included)
21164-333	33.33 MHz (not supplied)	TQ2061 (included)

- Heat sink and fan solution. Components included: heat sink, GRAFOIL pad, 2 hex nuts, heat sink clips, 60-mm fan, fan guard, and 4 screws. Components available from:

  United Machine and Tool Design
  River Road
  Fremont NH 03044
  Phone 603–642–5040
  FAX 603–642–5819

A.1 Products Included

- Bcache (Level 3) cache SIMMs

Cache Size	SIMM Configuration	Qty	Vendor/Part Number
2MB @10 ns	128K × 80	2	Digital PN, 21A04-M1

A.2 Products Not Included

The following products are not included in the EB164 motherboard kit.

- DRAM system memory—70 ns DRAM SIMMs (5 V, 72 pin)
  1M × 36, 2M × 36, 4M × 36, 8M × 36, 16M × 36.

  Note

  The DRAM SIMMs must be n × 36 SIMMs.

- Power supply—+3.3 V, +5 V, –5 V, +12 V, –12 V, available from:

  Emacs Electronics USA, Inc.
  1410 Gail Borden Place C-4
  El Paso TX 79935
  Phone: 915–599–2688
  Part number: AP2-5300F (300 W)

  Autec Power Systems
  69 Moreland Rd
  Simi Valley, CA 93065
  Phone: 805–522–0888
  Part number: PCB-3330-1010-D (339 W)

- Enclosure
  Axxion part number TL17 (modified for Digital applications).

B

Technical Support and Ordering Information

B.1 Obtaining Technical Support

If you need technical support or help deciding which literature best meets your needs, call the Digital Semiconductor Information Line:

United States and Canada	**1–800–332–2717**
Outside North America	**+1–508–628–4760**

B.2 Ordering Digital Semiconductor Products

To order the EB164, contact your local distributor.

The following table lists some of the semiconductor products available from Digital. To obtain a Digital Semiconductor Product Catalog, contact the Digital Semiconductor Information Line.

Product	Order Number
Digital Semiconductor 21164 Alpha Microprocessor Motherboard (EB164) 266-MHz Kit (Supports the Windows NT operating system.)	21A04-A0
Digital Semiconductor 21164 333-MHz Alpha Microprocessor	21164–333
Digital Semiconductor 21164 300-MHz Alpha Microprocessor	21164–300
Digital Semiconductor 21164 266-MHz Alpha Microprocessor	21164–266
Digital Semiconductor 21164 266-MHz Alpha Microprocessor for Windows NT	21164–P1

B.3 Ordering Digital Semiconductor Literature

The following table lists some of the available Digital Semiconductor literature. For a complete list, contact the Digital Semiconductor Information Line.

Title	Order Number
Alpha AXP Architecture Reference Manual[1]	EY–T132E–DP
Alpha AXP Architecture Handbook	EC–QD2KA–TE
Alpha 21164 Microprocessor Data Sheet	EC–QAEPC–TE
Alpha 21164 Microprocessor Hardware Reference Manual	EC–QAEQC–TE
Alpha 21164 Microprocessor Product Brief	EC–QAENB–TE
Alpha 21164 Microprocessor Evaluation Board Read Me First	EC–QD2VB–TE
Alpha 21164 Microprocessor Evaluation Board Product Brief	EC–QCZZD–TE
Digital Semiconductor 21164 Alpha Microprocessor Evaluation Board User's Guide	EC–QD2UD–TE
DECchip 21171 Core Logic Chipset Product Brief	EC–QC3EB–TE
DECchip 21171 Core Logic Chipset Technical Reference Manual	EC–QE18B–TE
Answers to Common Questions about PALcode for Alpha AXP Systems	EC–N0647–72
PALcode for Alpha Microprocessors System Design Guide	EC–QFGLB–TE
Alpha Microprocessors Evaluation Board Windows NT 3.51 Installation Guide	EC–QLUAD–TE
SPICE Models for Alpha Microprocessors and Peripheral Chips: An Application Note	EC–QA4XC–TE
Alpha Microprocessors SROM Mini-Debugger User's Guide	EC–QHUXA–TE
Alpha Microprocessors Evaluation Board Debug Monitor User's Guide	EC–QHUVC–TE
Alpha Microprocessors Evaluation Board Software Design Tools User's Guide	EC–QHUWA–TE

[1]To purchase the *Alpha AXP Architecture Reference Manual*, call **1–800–DIGITAL** from the U.S. or Canada, contact your local Digital office, or call Digital Press at 1–800–366–2665.

B.4 Ordering Third-Party Literature

You can order the following third-party literature directly from the vendor:

Title	Vendor
PCI System Design Guide	PCI Special Interest Group 1–800–433–5177 (U.S.) 1–503–797–4207 (International) 1–503–234–6762 (FAX)
PCI Local Bus Specification, Rev 2.1	PCI Special Interest Group (See previous entry.)
82420/82430 PCIset ISA and EISA Bridges (includes 82378IB/ZB SIO) PN 290483	Intel Corporation Literature Sales P.O. Box 7641 Mt. Prospect, IL 60056 USA 1–800–628–8686 FaxBACK® Service 1–800–628–2283 BBS 1–916–356–3600
UPI-41AH/42AH Universal Peripheral Interface 8-Bit Slave Microcontroller PN 210393	Intel Corporation (See previous entry.)
Flash Memory PN 210830	Intel Corporation (See previous entry.)
PC87311/PC87312 (SuperI/O II/III) Floppy Disk Controller with Dual UARTs, Parallel Port, and IDE Interface PN 11362	National Semiconductor Corporation 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052 USA 1–800–272–9959
Hardware Compatability List	Contact Microsoft's Customer Service representatives at 1–800–426–9400, or access CompuServe Information Systems in Library 1 of the WINNT forum (GO WINNT) or Library 17 of the MSWIN32 forum (GO MSWIN32).

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