CHAPTER 3
PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This chapter presents three levels of PDP-8/E System operation. First, a simplified block diagram presenting the primary parts of the processor is discussed. Second, a flow chart relating the processor instructions to time states is presented and discussed with appropriate references to the corresponding third-level discussion. The third-level discussion presents the logic theory and is divided into functional groups of logic. A reference to the modules is provided so that continuity between the principles of operation and the engineering drawings exists throughout the discussion.

NOTE

The component designations are for reference only and do not necessarily correspond to those designations on engineering drawings.

Chapter 3 is divided into eight functional sections:

Section 1 – System Introduction

Section 2 – System Flow Diagrams

Section 3 – Timing Generator

Section 4 – Memory System

Section 5 – Central Processor

Section 6 – I/O Transfer Logic

Section 7 – Teletype Control

Section 8 – Power Supply

This format is provided to aid the user in understanding the principles of operation and to distinguish the individual parts of the basic PDP-8/E processor.

3.2 PDP-8/E BASIC SYSTEM

The PDP-8/E processor contains eight functional areas and can accommodate as many as 60 options. A simplified block diagram, Figure 3-1, relates the OMNIBUS to the major signals and the eight functional areas. Each of the functional areas is contained on a single quad-size module with the exception of the MM8-E (three modules are provided).

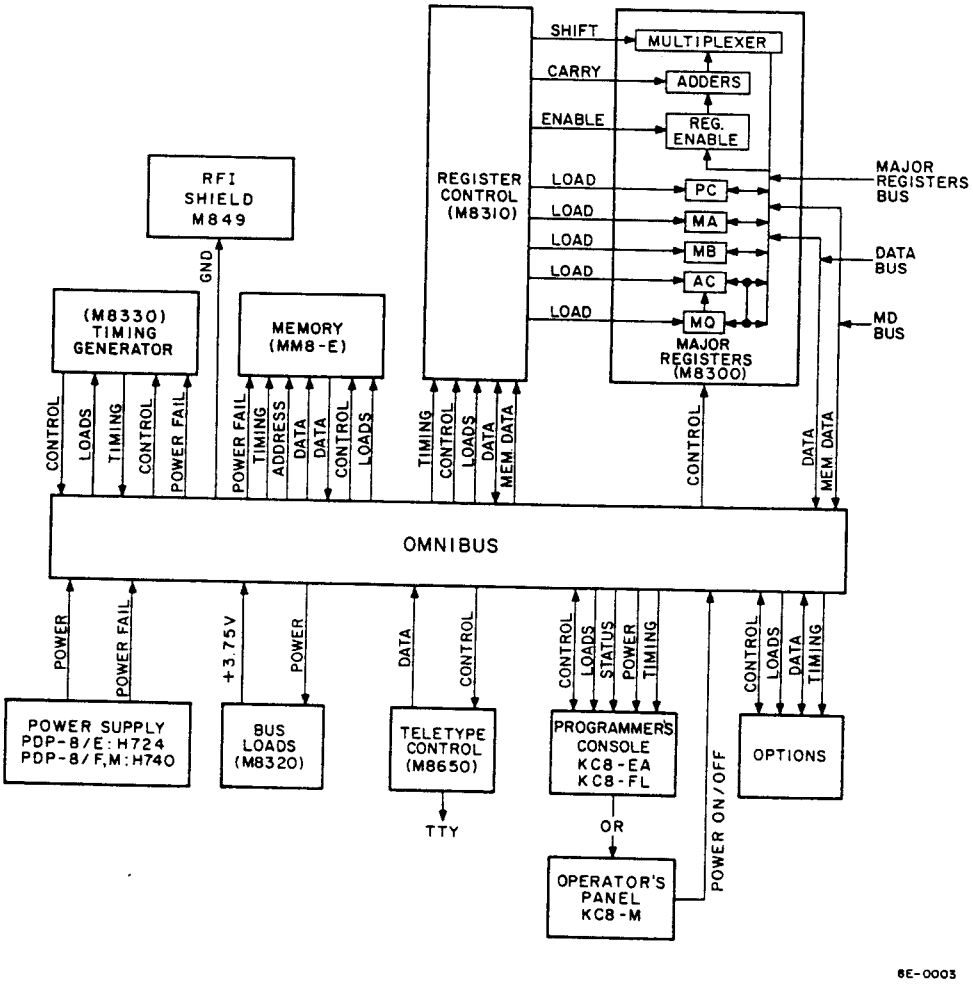


Figure 3-1 PDP-8/E Simplified Block Diagram

3.2.1 OMNIBUS

The OMNIBUS provides a two-way path between the corresponding connector pins of the modules that plug into it. To accommodate 96 signal lines plus ground and power at the module connectors, 144 pins are provided. In general, each signal line is kept at a +3.75 Vdc level and pulled to ground when the signal is asserted. However, exceptions occur, with respect to power levels and some timing and control signals. Bus loads provide this capability by applying +3.75 Vdc to the bus lines via load resistors. When a signal line is asserted, the output driver of that signal pulls the line to ground, the corresponding input circuits (on the same module or a different

module) are activated due to the low signal. This technique facilitates the interaction between modules and makes it possible to connect many modules to the same bus. Some signals do not use the OMNIBUS. The connection of the M8310 Register Control module and the M8300 Major Registers module is partially accomplished using an H851 Edge Connector for all of the control signals. Data is exchanged through the OMNIBUS.

3.2.2 Timing Generator (M8330)

The timing generator provides four time states (TS1 through TS4), four time pulses (TP1 through TP4) and memory timing signals. One memory cycle is accomplished between TS1 and TS4. A choice of two memory cycles is provided: a slow (1.4 μs) and a fast (1.2 μs) cycle. Control inputs are provided by the register control module and the power supply.

3.2.3 Memory (MM8-E)

Three memory modules are provided: the G619 Memory Stack, the G227 X/Y Driver and Current Source, and the G104 Sense/Inhibit.

The memory stack contains 12 core mats, each consisting of 4096 cores and selection diodes to provide a 12 bit-per-word, 4096 word storage capability.

The X/Y driver and current source module contains the selection switches, drivers, and current source required to fully select any one of the 4096 memory locations.

The sense/inhibit module is used to sense (read) any one of the 4096 memory locations and to write into any memory location.

3.2.4 Register Control (M8310)

The register control has many functional logic circuits that generate the major states of the processor, determine the instruction to be performed, and control the operation of the major registers (M8300). The register control receives a word from memory, decodes the word, and determines the operation to be performed. Functional logic is provided to gate bits into the major register adder circuit, shift right, or shift left. The M8310 develops register transfer signals and register load signals. The timing generator determines when these signals are generated.

3.2.5 Major Registers (M8300)

The major registers module provides the Program Counter (PC) Register, the Central Processor Memory Address (CPMA) Register, the Memory Buffer (MB) Register, the Accumulator (AC) Register, and the Multiply-Quotient (MQ) Register. Transfer of information in the AC to the MQ is accomplished directly through enabling logic. Transfer of all other registers is accomplished through the register enable logic, through the adders, and through the output multiplexers, where the information is placed onto the MAJOR REGISTERS BUS. Information can be brought into the MAJOR REGISTERS BUS from the DATA BUS and the MD BUS or transferred out to the same lines. Transfer of MB data to the MD lines is accomplished by MD DIR (H).

3.2.6 Power Supply (H724)

The power supply receives an input of 95 to 130 Vac, 47 to 63 Hz and provides 28 Vac, +8 Vdc, +5 Vdc, -15 Vdc, and +15 Vdc to the PDP-8/E System. The power system is interlocked with the front panel key switch. Power fail and overload detection are provided to ensure the protection of system components and system performance.

3.2.7 Bus Loads (M8320)

The bus loads receive +5 Vdc and +15 Vdc inputs from the power supply and provide a +3.75 Vdc output to the signal lines on the OMNIBUS.

3.2.8 Teletype Control (M8650)

The Teletype control module contains a receive register and transmit register, decoders, and interprets two flags. It performs the conversion of parallel computer words to serial Teletype words, assembles serial Teletype characters into data words for the computer and commands from the computer.

3.2.9 Programmer's Console (KC8-EA)

The programmer's console is a plug-in module, containing logic, lamps, and switches. The face panel, which contains openings for the switch levers and a silk-screened switch/indicator identification, is mounted in front of the programmer's console module. The panel OFF/POWER/PANEL LOCK switch is controlled by a key. The programmer's console enables the operator to deposit a 12-bit word into memory, read any memory location, observe the content of important registers, read the instruction currently being processed, and observe every primary activity the processor is currently performing.

3.2.10 RFI Shield (M849)

The RFI shield module ensures no interference of memory circuits with nonmemory options (those options not synchronized with memory).

3.2.11 Options

More than 60 options are available to the PDP-8/E user. The one option described in this volume is the Teletype control option. All other internal bus options are described in Volume 2. External bus options are described in Volume 3.

3.2.12 Signal Finder

The basic PDP-8/E signals and their descriptions are given in Table 3-1. If the reader desires to study the detailed logic as he is progressing through the flow diagrams, a corresponding paragraph reference to the detailed logic is provided. Refer to Appendix B for source-destination module designations.

Table 3-1
Signal Finder

Signal Name	Logic Reference	Signal Description
DATA T DATA F	3.35.3	Data Control GATE ENABLING signals – DATA BUS TO ADDERS: DATA T, DATA F COMPLEMENT OF DATA BUS TO ADDERS: DATA T, DATA F ZERO TO ADDERS: DATA T, DATA F*
AC → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the AC to be applied to the DATA BUS.
MQ → BUS L	3.35.2	Enables the Data Line MUX to allow the contents of the MQ to be applied to the DATA BUS.
SHL + LD ENA L AC → MQ ENA L	3.40	Enable signals applied to the MQ MUX to output either the MQ (one place to the left) or the contents of the AC. SHL + LD ENA L / AC → MQ ENA L / Output: L / L / MQ (left) L / H / MQ (left) H / L / AC H / H / 0
F SET L D SET L E SET L	3.34.1	Indicates the next major state. For example, F SET L means that the next major state is FETCH.
F L, D L, E L	3.34.1	Indicates the current major state.
DMA	3.8	Direct Memory Access State – asserted when MS, IR DISABLE is grounded.
INT IN PROG	3.42.1	Interrupt in Progress – this signal acknowledges an interrupt request and forces a JMS to the IR and EXECUTE to the Major State Register.
INT REQUEST L	3.42.1	Interrupt Request – when asserted (low) means that a device has set a flag and is requesting an Interrupt.
USER MODE	3.42.1	Used with the time-sharing option to prevent programmed halt, I/O PAUSE, OSR, or LAS.

*This condition cannot exist during OPERATE and TS3.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
INT BUS L	3.33.1.2 3.33.2.2	When the programmer's console STATUS switch is in STATUS, an INT REQUEST occurs, and the INT BUS indicator is illuminated.
LOAD, AC MQ MB CPMA PC	3.37	When data is to be placed into one of the Major Registers, the corresponding load signal is developed.
INT STROBE	3.41	Interrupt Strobe – Developed by BUS STROBE and NOT LAST XFER or TP3 to set the INTERRUPT SYNC flip-flop. Used by the interrupt and break systems.
I/O PAUSE L	3.41.2	Signifies that an IOT is being processed. It is used by the peripheral control modules to gate device selectors and to gate data onto the DATA BUS. This signal is used to initiate OUTPUT transfers; in the central processor, it is used to control IOT decoding.
BUS STROBE L	3.41.2	BUS STROBE L is used for IOT instructions to load data into the AC or PC and, with NOT LAST XFER L, generates INTERRUPT STROBE.
INTERNAL I/O L	3.41.4	Used to inhibit the generation of IOPS by the positive I/O bus interface.
C0 L, C1 L, C2 L	3.41.1	Controls the type of I/O data transfer between a device and the processor.
MS, IR DISABLE L	3.34	Major State, Instruction Register Disable – Used during Direct Memory Access to disable FETCH, DEFER, or EXECUTE major state and instruction register.
KEY CONT L	3.33.1.1	Key Control – A control signal developed in the front panel logic.
STOP L	3.16	Stop resets the RUN flip-flop and causes timing to halt at TS1.
CONT	3.33.1.1	Continue – A front panel key to force the processor into automatic timing.
ADDR LOAD L	3.33.1.1	Address Load – A front panel key used to manually load an address into the CPMA.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
EXTD ADDR L	3.33.1.1	Extended Address Load – A front panel key used to manually load the address of extended memory.
DATA 0–11 L		The DATA BUS containing 12 bits of information.
FIELD	3.27.4	Corresponds to extended memory up to 32K as follows: BASIC MEMORY: FIELD 0 EXTENDED MEMORY: FIELD 1 – FIELD 7
NOT LAST XFER L	3.41.2	Used primarily with the device on the positive I/O bus, requiring more than 1.2 μs to perform an IOT.
BRK DATA CONT L	3.8.2 and 3.33.1.1	Used to gate the contents of the MD BUS through the Register Input Multiplexer.
EN0 EN1 EN2	3.35.1	Register Input Multiplexer enabling signals to allow the contents of the Major Registers to be placed into the ADDERS.
OVERFLOW L	3.39	Overflow – Occurs when carry-out is asserted from adder state 0 at TP2.
CAR OUT L	3.39	Carry Out – Asserted when 7777_8 is incremented by 1 in the adder.
CAR IN L	3.36.1	Carry In – Developed to add a 1 to a register.
SKIP L	3.38	The output of the SKIP flip-flop is applied to carry-in logic. SKIP is set during a variety of conditions such as OVERFLOW during an ISZ instruction and programmed microinstructions (GROUP 2).
SHIFT– LEFT L RIGHT L TWICE L NO SHIFT L	3.36.2	Shift Signals that cause the adder output multiplexer to shift left, or right, or twice left or twice right, or byte swap.
PAGE Z L	3.36.2	Asserted when Page Zero is to be addressed. PAGE Z is applied to the adder output multiplexer to apply zeros to CPMA0-4.

Table 3-1 (Cont)
Signal Finder

Signal Name	Logic Reference	Signal Description
MD DIR L	3.28	Memory Data Direction – Used to control memory data during the read and write operation. MD DIR L: Places the contents of the MEM REG on the MD BUS. MD DIR: Places the contents of the MB Register on the MD BUS.
DEP	3.33.1.1	Deposit – A front panel key used to manually load information into memory.

3.3 DATA PATHS

Because the OMNIBUS concept is different from other PDP-8 family processors, the reader should understand the relationship of the data paths to the OMNIBUS.

The OMNIBUS should be considered a bus containing several buses. A bus is defined as a group of 12 signal lines, carrying information. With this definition, the PDP-8/E contains the MEMORY DATA (MD) BUS, the DATA BUS, the MEMORY ADDRESS (MA) BUS, and the MAJOR REGISTER BUS. All buses (except MAJOR REGISTER BUS) are on the OMNIBUS. The OMNIBUS also contains the transfer control signals for I/O operations.

Data paths are illustrated in Figure 3-2. Although the illustration does not show all of the signals on the OMNIBUS, it is obvious from the data paths that signal origins and destinations appear in many places. Using the MD BUS as an example, memory data is provided by the Memory Register, the MB Register, and memory options. The MA BUS receives the memory address from the CPMA Register and from some options that generate the 12 address bits. The MA BUS applies these 12 bits to the XY selection decoder of the memory. The DATA BUS is used to receive Switch Register data, provide status to the Programmer's Console, carry information to and from a peripheral or internal option, and provide a path for data to the MAJOR REGISTERS BUS.

The MAJOR REGISTERS BUS completes a return path to each of the major registers. The CPU controls inputs to the major registers, and the enabling logic causes operations such as swapping, shifting, ANDing, ORing, and loading to manipulate data and select one of the registers to place the results. If the results are to be stored in memory, for example, the MB Register is loaded and gated onto the MD BUS by MD DIR L. This same information is carried to the inhibit drivers and stored in the selected memory location. If an option such as the EAE that is plugged into the OMNIBUS wanted the results of the data manipulation, the data path is from the MAJOR REGISTERS BUS to the DATA BUS. This condition is caused by loading either the MQ or the AC with the data and enabling the transfer of the data onto the DATA BUS. To place the data contained in some memory location onto the DATA BUS, the memory location must first be selected. The content of the memory location must be sensed and applied to the Memory Register. Signal MD DIR L gates the Memory Register out to the MD BUS. From the MD BUS the data is applied to the Register Multiplexer and to the MAJOR REGISTERS BUS via the adder and output multiplexer. Signal AC → BUS L places the data onto the DATA BUS.

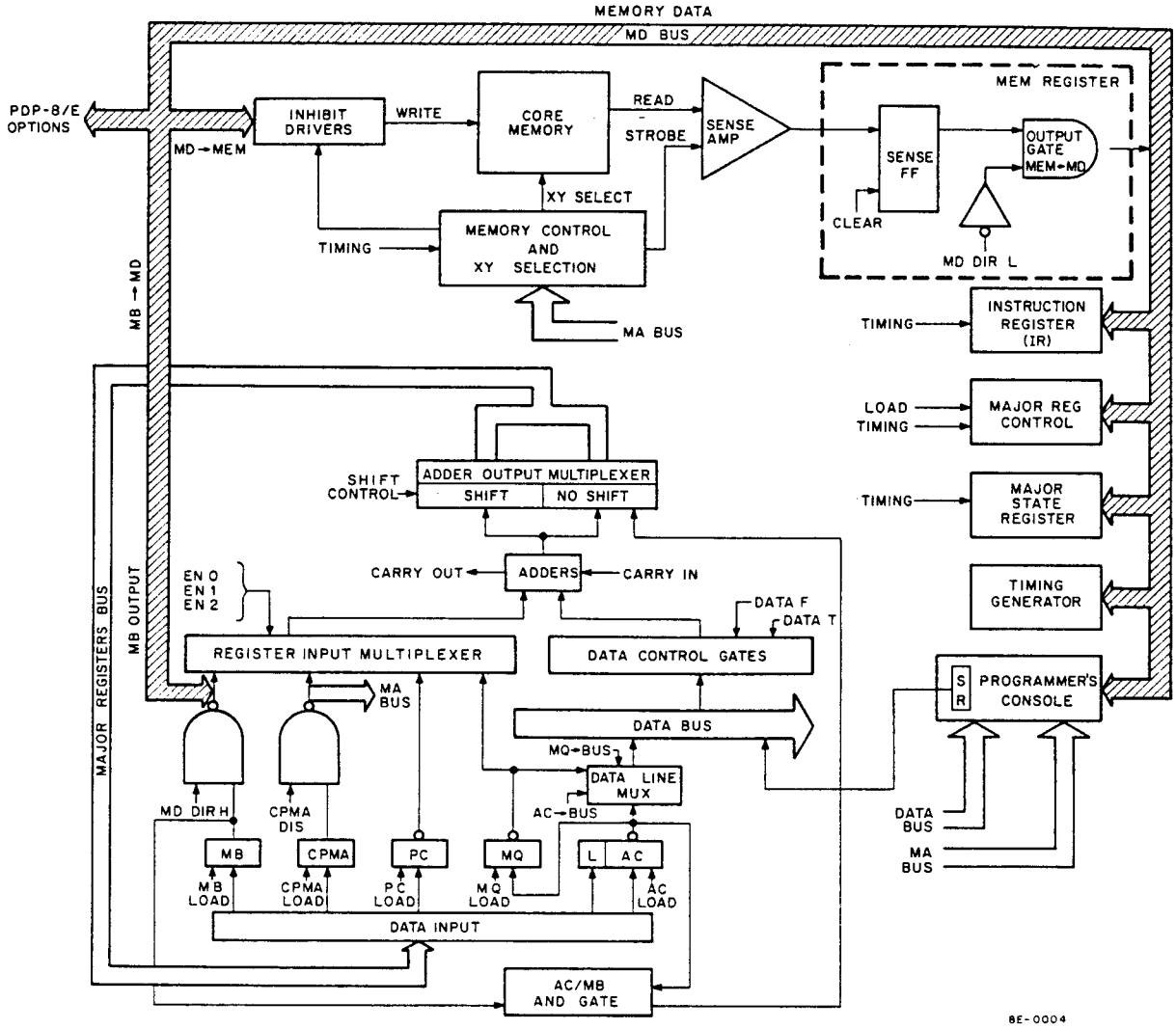


Figure 3-2 Basic Data Paths

3.3.1 Basic Transfer Control Signals

Table 3-2 traces the data paths (Figure 3-2) from the major registers through to the MAJOR REGISTERS BUS and returns to a selected register. Each control signal is referenced to the detailed logic description; thus, the reader can see how the control signal is developed.

Table 3-2
Basic Transfer Control Signals

From	To	Basic Control Signal	Logic Reference
SWITCH Register	DATA BUS	DEPOSIT	3.33.1.1
SWITCH Register	DATA BUS	LOAD ADDRESS	3.33.1.1
AC Register	DATA BUS	AC → BUS	3.35.2
MQ Register	DATA BUS	MQ → BUS	3.35.2
AC Register	MQ REG	AC → MQ ENA LOAD MQ	3.40
DATA BUS	ADDERS	DATA T DATA F	3.35.3
Complement of DATA BUS	ADDERS	DATA T DATA F	3.35.3
MQ Register	ADDERS	EN0 EN1 EN2	3.35.1
PC Register	ADDERS	EN0 EN1 EN2	3.35.1
CPMA Register	ADDERS	EN0 EN1 EN2 CPMA DIS L	3.35.1 asserted low by options
CPMA Register	MA BUS	CPMA DIS L	
MB Register	MD BUS	MD DIR L	3.28
MD BUS	ADDERS	EN0 EN1 EN2	3.35.1
MAJ REG BUS	MB REG	MB LOAD L	3.37.1

Table 3-2 (Cont)
Basic Transfer Control Signals

From	To	Basic Control Signal	Logic Reference
MAJ REG BUS	CPMA REG	CPMA LOAD L	3.37.4
MAJ REG BUS	PC REG	PC LOAD L	3.37.3
MQ MUX	MQ REG	MQ LOAD L	3.40
MAJ REG BUS	AC REG	AC LOAD L	3.37.2
CPMA	CPMA + 1	CARRY IN L	3.36.1
PC	PC + 1	CARRY IN L	3.36.1
MEM REG	MD BUS	MD DIR L	3.28

FROM	TO	Logic Reference
ADDERS	MAJOR REGISTERS BUS	3.36.2

Type of Operation	Shift Control Signals				
	PAGE Z L	RIGHT L	LEFT L	TWICE L	
ZEROs TO MA 0–4 (PAGE ZERO)	H	L	L	L	
AND MB WITH (MB•AC)	L	L	L	H	
SHIFT OUTPUT OF ADDERS RIGHT ONCE	L	L	H	H	
SHIFT OUTPUT OF ADDERS LEFT ONCE	L	H	L	H	
SHIFT OUTPUT OF ADDERS RIGHT TWICE	L	L	H	L	
SHIFT OUTPUT OF ADDERS LEFT TWICE	L	H	L	L	
BYTE SWAP (SWAP first six bits with last six bits)	L	H	H	L	
NO SHIFT	L	H	H	H	

3.4 PROCESSOR BASIC TIMING

Four time states, TS1 through TS4, are provided by the timing generator to divide the processor cycle into four parts (Figure 3-3). The major states control the flow of events during the execution of programmed instructions.

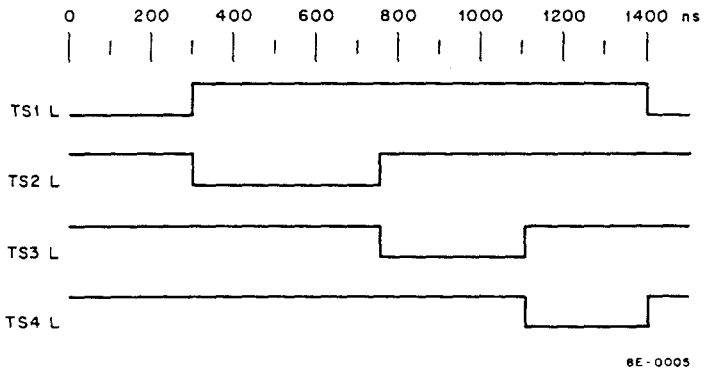


Figure 3-3 Processor Timing States (Slow Cycle)

3.5 PROCESSOR MAJOR STATES FLOW

The PDP-8/e provides four major states:

a. FETCH, to obtain the Memory Reference Instruction and Nonmemory Reference Instructions from memory, and perform Nonmemory Reference Instructions

b. DEFER, for indirect addressing or autoindexing

c. EXECUTE, for performing the Memory Reference Instruction

d. Direct Memory Access (DMA), for manual operation or data break.

The basic major state flow diagram is illustrated in Figure 3-4. This diagram also indicates the order in which the major states are implemented. For any type of processor instruction, the processor must bring the contents of some memory location to the MD BUS. The Instruction Register (IR) decodes the first three bits (0–2). With FETCH major state asserted and the instruction decoded, the Central Processor (CPU) follows a series of steps; these steps are controlled by timing and the logic of the CPU.

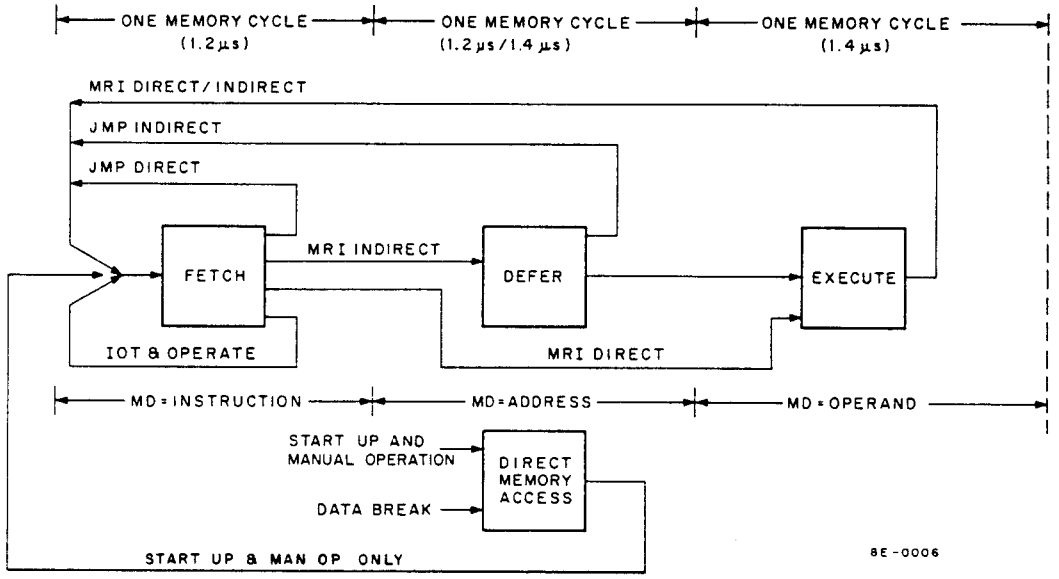


Figure 3-4 PDP-8/E Major State Flow Diagram

The FETCH major state is required for all instructions. For Memory Reference Instructions (MRI), the CPU enters the EXECUTE state via DEFER (for an indirect address) or the EXECUTE state (for a direct address). IOT and OPERATE instructions are completed in one memory cycle during FETCH. However, an MRI can take either 2 or 3 cycles (depending on a direct or indirect address). Most instructions, therefore, take 2.6 μs or 3.8 μs, depending on the addressing.

In Figure 3-4, during the FETCH cycle, the content of the MD BUS is the instruction and an address; during the DEFER cycle, the content of the MD BUS is an address; during the EXECUTE state, the MD BUS contains the operand (that data contained in the addressed location on which the instruction will manipulate or modify). The DEFER cycle is 1.2 μs for an indirect address and 1.4 μs for an autoindex.

A fourth major state is Direct Memory Access (DMA). During the DMA state, manual functions can be accomplished or the data break system can operate. Both the manual and data break operations require access to a memory location with little help from the CPU control.

3.6 START-UP FLOW DIAGRAM

The following information describes the events of the Start-Up flow diagram illustrated in Figure 3-5. A flow reference keys the flow diagram with the corresponding explanation.

Flow Reference	Explanation
(1)	TURN KEY TO POWER – The POWER position of the OFF-POWER-PANEL LOCK switch generates the INITIALIZE signal in the timing generator. INITIALIZE is used to clear the AC Register, the Link, the Skip circuit, flags, etc. Operation of the CLEAR key also generates INITIALIZE.
(2)	LOAD ADDRESS – The operator sets the switch register to the desired address and depresses the ADDR LOAD key. At the same time the address is loaded, signals MS IR DISABLE L and F SET L are asserted; consequently, the next cycle major state is FETCH. If restart is desired, the state of the AC Register, Link circuit, Skip circuit, and flags should be cleared immediately after the address is loaded. CLEAR develops signal INITIALIZE, as previously described.
(3)	EXAMINE OR DEPOSIT – To examine the contents of the addressed memory location or deposit a word into memory, branching into the Dep/Exam Flow (Paragraph 3.8.2) is required. When the operator has finished, the Start-Up flow is resumed.
(4)	DEPRESS CONT KEY – The assertion of the CONT (continue) key asserts MEM START (Paragraph 3.33.1.1) which, in turn, asserts signal RUN (Paragraph 3.16). Because RUN is necessary to start timing, the timing chain begins at the next clock pulse and continues as long as RUN is asserted.
(5)	FETCH CYCLE – The FETCH cycle is automatically entered if D SET L or E SET L of the Major State Register has not been asserted. Refer to Paragraph 3.9 for the FETCH state discussion.

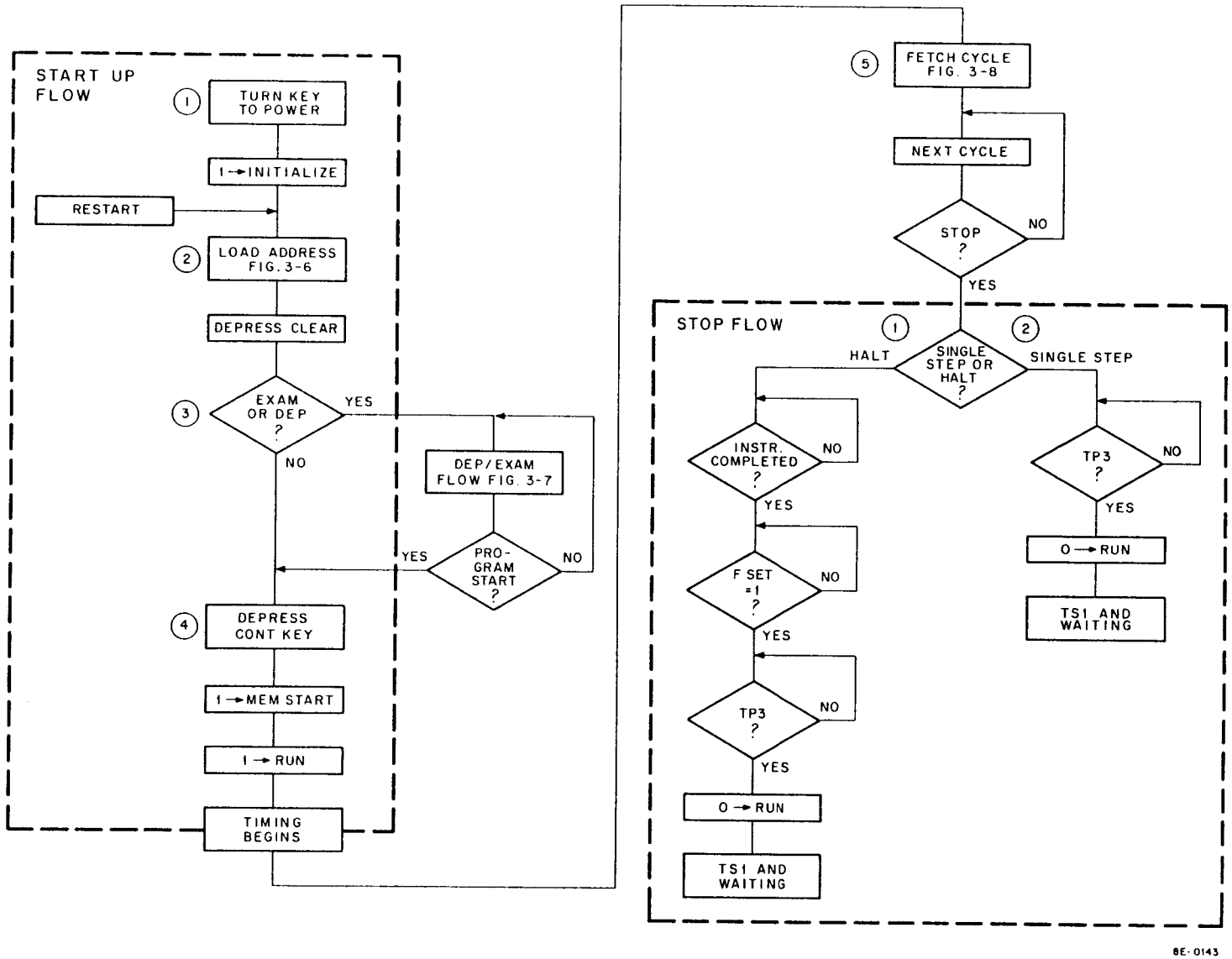


Figure 3-5 Start-Up/Stop Flow Diagram

3.7 STOP FLOW DIAGRAM

The Stop flow diagram is presented in Figure 3-5. The two methods of manually stopping the processor are indicated as either halt or single step.

Flow Reference	Explanation
(1)	HALT – There are two methods of generating a HALT command: (a) program the HALT instruction (Paragraph 3.9.2), or (b) depress the HALT key as shown in Figure 3-5. The HALT command allows the processor to complete the current instruction; this could take up to three processor cycles (FETCH, DEFER, EXECUTE), depending on the type of instruction being processed when the HALT command is received. At TP3 when F SET L is asserted, signal RUN is made inactive (Paragraph 3.16). Thus, the timing chain is interrupted, and the processor is halted in TS1.
(2)	SINGLE STEP – When the SING STEP key is depressed, the processor halts at the end of the current cycle. Because it does not wait until F SET L is asserted, the processor does not necessarily finish the current instruction. (This is the only difference between halt and single step.)

3.8 DIRECT MEMORY ACCESS (DMA) STATE FLOW DIAGRAMS

The Direct Memory Access (DMA) state allows accessing of memory when the Major State Register and Instruction Register of the CPU are disabled. Two types of DMA are available with the PDP-8/E System: (a) the basic type is the use of the Programmer's Console to either deposit into memory or retrieve from memory a 12-bit word, and (b) the second type is called data break and is used with mass storage equipments. A simplified flow diagram representing both types is provided in Figure 3-4. Refer to the *PDP-8/E & PDP-8/M Small Computer Handbook,* Chapter 6, and Volume 3 of this manual for a discussion of data break.

3.8.1 Load Address Flow Diagram

The Programmer's Console is used for manual addressing of memory. Using 12 switches, the operator can load the CPMA Register with a desired address whenever the ADDR LOAD key is depressed. In a similar manner, the Extended Address is loaded. A flow diagram representing the basic functions is presented in Figure 3-6.

Flow Reference	Explanation
(1)	LOAD ADDRESS – A 12-bit address is first set into the switch register, and the ADDR LOAD key is depressed. The following events occur: a. The contents of the Switch Register are transferred onto the DATA BUS. b. The outputs of the Major State (MS) Register and Instruction Register (IR) are disabled; F SET L is asserted. c. The register input multiplexer is disabled. d. The data control gate is enabled. e. Signal CPMA LOAD is asserted, loading CPMA, and setting the FETCH flip-flop in the MS Register.

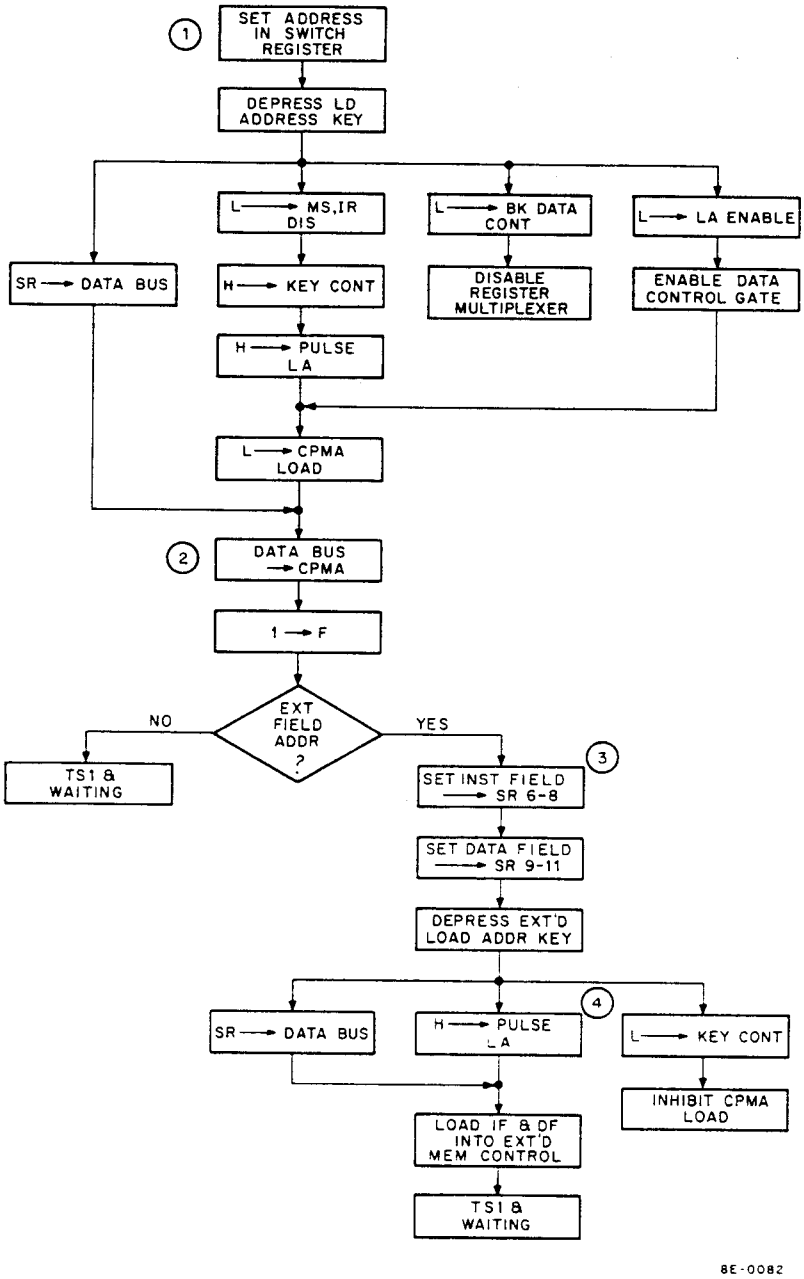


Figure 3-6 Manual ADDR LOAD/EXTD LOAD

Flow Reference	Explanation
(2)	DATA BUS → CPMA – The contents of the DATA BUS (Figure 3-2) follow the path through the data control gate into the adder, through the no shift portion of the output multiplexer, and onto the MAJOR REGISTERS BUS. Signal CPMA LOAD L then gates the contents of the MAJOR REGISTERS BUS into the CPMA Register. FETCH L is developed by CPMA LOAD L (Paragraph 3.34.1). Thus, the processor will be in the FETCH state during the next processor cycle unless direct memory access is again required. However, because the timing chain was never activated during LOAD ADDRESS events, the processor time state will be in TS1 and waiting.
(3)	If extended address is required, the following events must occur: a. Load the Instruction Field into Switch Register (SR) bits 6 through 8. b. Load Data Field into SR bits 9 through 11. c. Depress EXTD ADDR LOAD key.
(4)	The contents of the SR are then transferred to the DATA BUS and applied to the extended memory control module. All circuits within the major registers are inhibited.

3.8.2 Deposit/Examine Flow Diagram

The similarities and differences in the Deposit and Examine events are illustrated in Figure 3-7. For Examine (shown on the left of the figure), it is necessary to read the addressed memory location; for Deposit (shown on the right of the figure), it is necessary to write into the addressed memory location; common events are shown in the center of the figure.

Flow Reference	Explanation
(1)	EXAMINE – Depressing the EXAM key asserts both BRK DATA CONT L and MD DIR L. These signals are necessary to read from memory and also allow the contents of the MD BUS to be applied to the MB Register.
(1)	DEPOSIT – The data word must first be manually selected on the SR. The DEP key is then lifted and the contents of the SR are then applied to the DATA BUS (Figure 3-2).

3.8.2.1 Examine or Deposit Common Events – Depressing either the EXAM or DEP key causes the following events to occur:

Flow Reference	Explanation
(2)	The major states and Instruction Registers are disabled (Paragraph 3.33.1.1).
(3)	Signal RUN L is asserted by MEM START L (Paragraph 3.16) and timing begins.
(4)	Signal STOP is asserted by KEY CONT L. At TP3 time, STOP is used to 0 the RUN flip-flop.

Flow Reference	Explanation
(5)	The contents of the CPMA Register are gated through the Register Input Multiplexer (Figure 3-2) and placed onto the adder circuits. A CAR IN signal is developed (Paragraph 3.36.1), adding 1 to the sum of the adder inputs. The result is then loaded into the PC Register to provide "MA + 1 to the PC".
(6)	MEM TO MD – The READ operation (Paragraph 3.27.2) begins during TS1 and continues into a portion of TS2. This places the contents of the addressed memory location onto the MD BUS (Figure 3-2). Thus, the contents of memory are now ready to be gated onto the MAJOR REGISTERS BUS during TS2.
(7)	EXAMINE – The contents of the MD BUS (12 bits) are gated through the Register Input Multiplexer during TS2 (Paragraph 3.35.1) and placed onto the MAJOR REGISTERS BUS (Figure 3-2). The 12-bit word is now ready to be loaded into the MB Register at TP2. BRK DATA CONT L is pulled low to ENABLE DATA PLUS MD to the MB. The data lines, in this case, are 0s (high).
(8)	DEPOSIT – The contents of the DATA BUS are gated through the Data Control Gate and applied to the MAJOR REGISTERS BUS (Figure 3-2). The 12-bit word is now ready to be loaded into the MB Register.
(8)	MB load occurs at TP2 (Paragraph 3.37.1). At this time, the contents of the MAJOR REGISTERS BUS are loaded into the MB Register.
(9)	With the READ operation completed, it is necessary to write the same information back into memory or deposit new information. However, the contents of the MB Register must first be transferred to the MD BUS. This occurs when MD DIR L is negated (Figure 3-2).
(10)	A 0 is placed in the RUN flip-flop (Paragraph 3.33.1.1) when TP3 and STOP are both asserted. This prevents the processor from starting a new cycle until some action is taken by the operator.
(11)	The WRITE operation automatically starts during TS3 and continues into TS4. At this time, the contents of the MD BUS are written into the addressed memory location.
(12)	For the preparation of the next processor cycle, the next sequential address is automatically placed in the CPMA Register. Because the Program Counter (PC) contains the next address, the contents of the PC are loaded into the CPMA at TP4. If the operator desires to go into programmed operation, the CONT key must be depressed. Because the next active state will be either DMA or FETCH, depressing the EXAM key or raising the DEP key inhibits the Major State Register and allows one more DMA cycle. Otherwise, depressing the CONT key (Figure 3-6) causes a FETCH cycle.
(13)	During TS1 and when RUN = 0, the processor timing stops and waits for the next command from the operator. The contents of the MD BUS can be observed at this time. Also note that the CPMA shows the address for the next cycle and not the address from which the data was examined.

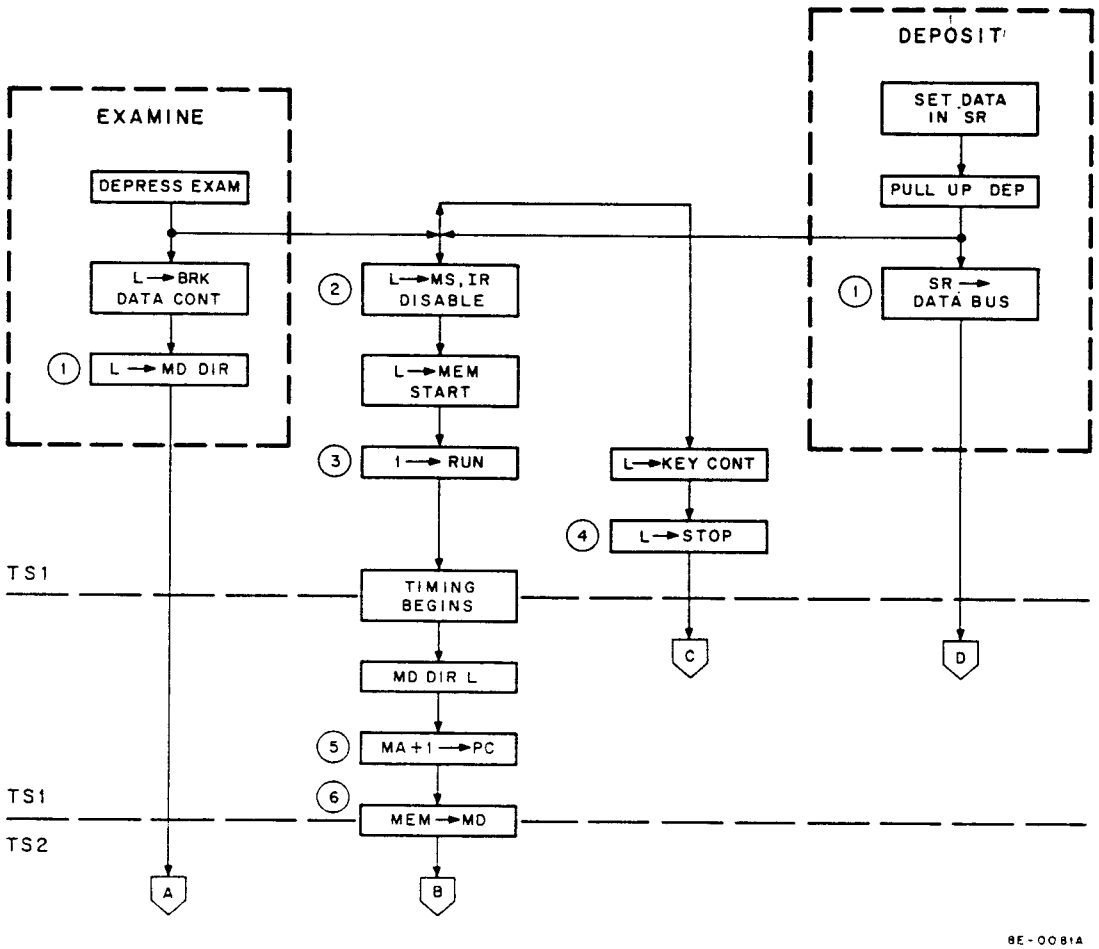


Figure 3-7 Deposit/Examine Flow Diagram (Sheet 1 of 2)

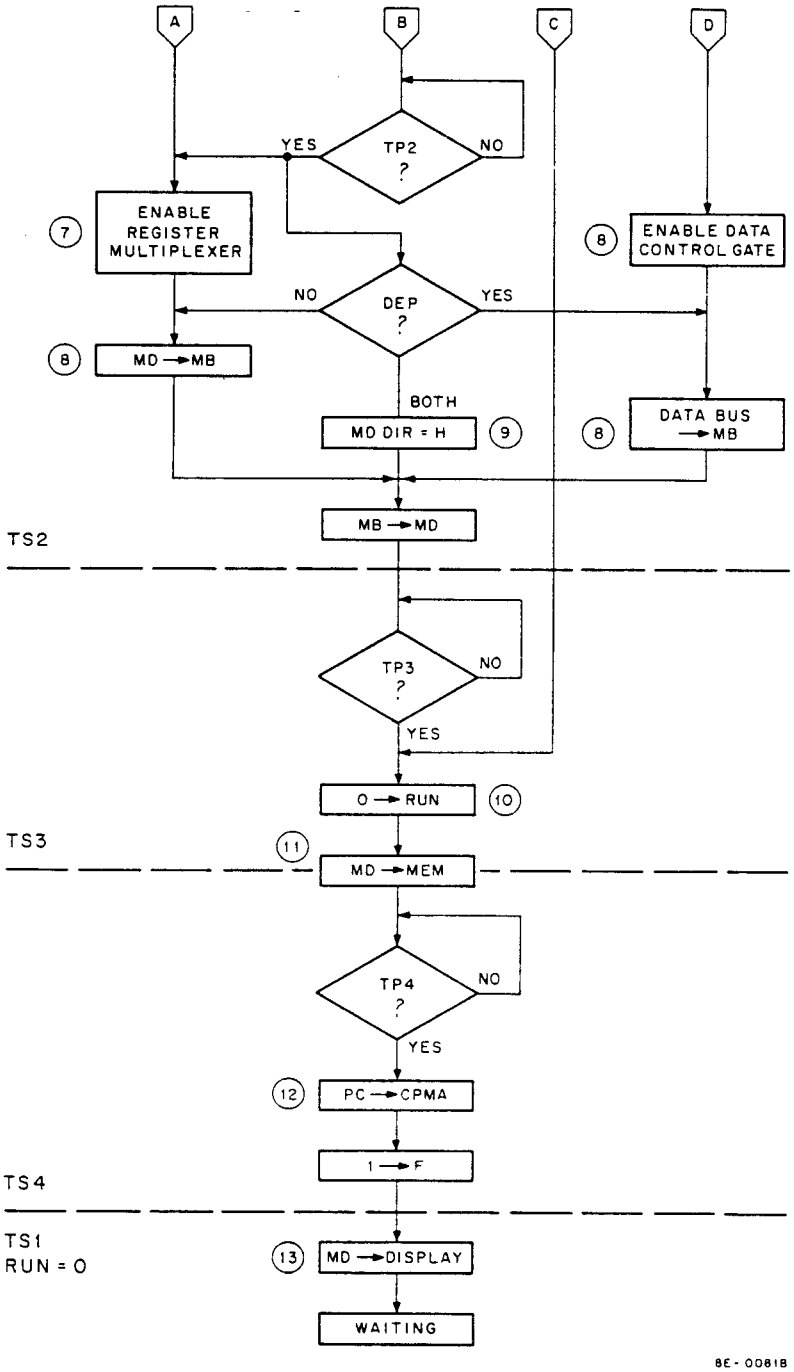


Figure 3-7 Deposit/Examine Flow Diagram (Sheet 2 of 2)

3.9 FETCH STATE INSTRUCTION FLOW DIAGRAM

The logic and instruction flow of events during FETCH is illustrated in Figure 3-8. Because of the complexity of the flow diagrams, the discussion is further divided into subflows as illustrated.

3.9.1 Common Events During FETCH (refer to Figure 3-2 for data paths)

Time State	Common Event
TS1	Update the PC Register, read the addressed memory location, and display the content of Major Registers.
TS2	Read the addressed memory location, transfer the content to the MD BUS, and decode the instruction.
TS3	Perform an augmented instruction (IOT or OPERATE), and begin writing the content of the MD BUS back into the addressed memory location or carry the Memory Reference Instruction to either the DEFER or EXECUTE state. Load the AC Register.
TS4	Update or modify the CPMA and complete the write operation. Enable the next processor major state (FETCH, DEFER, or EXECUTE).

Flow Reference	Explanation
(1)	CLEAR SKIP LOGIC – The SKIP flip-flop (Paragraph 3.38) is cleared during TS1.
(2)	INCREMENT PC – The Carry In logic (Paragraph 3.36.1) is asserted and applied to the adder circuit (bit 11). MA is then brought to the adder circuits and the results placed in the PC.
(3)	TRANSFER AC → PERIPHERAL – The content of the AC is placed on the DATA BUS to be used as determined by the user.
(4)	The content of the Memory Register is gated onto the MD BUS when MD DIR is low.
(5)	During FETCH, the first three bits of MD are decoded by the Instruction Register (Paragraph 3.34.2) to determine the type of instruction to be performed.
(6)	When MD bits 0–2 contain 1s, a 7 is decoded, indicating that an operate instruction is to be performed.
(6)	Three groups of operate instructions are available. The group selected depends on the state of MD3 and MD11. Refer to the following paragraphs for the flow diagrams: Group 1 Paragraph 3.9.2 Group 2 Paragraph 3.9.3 Group 3 Paragraph 3.9.4

Flow Reference	Explanation
(7)	Update CPMA – Before the CPMA can be updated, the interrupt system must be considered. If the INT IN PROG signal is asserted, a JMS is forced into the IR, the major state becomes EXECUTE, and 0s are placed into the CPMA. If the INT IN PROG signal is not asserted, the SKIP L signal is tested next. SKIP L may have been asserted as the result of one of the operate instructions or one of the IOT instructions during TS3. When SKIP L is asserted, a CAR IN L signal is generated which places a 1 in adder stage 11. The Register Input Multiplexer is enabled to allow the content of the PC Register (Figure 3-2) to be applied to the adders. The result is then transferred through the Adder Output Multiplexer to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. Without SKIP L, only the content of the PC will be loaded into the CPMA. The next major state will be FETCH if an IOT, OPERATE, or direct JUMP is performed. Signal F SET L enables the FETCH state.
(8)	IOT INSTRUCTIONS – When bits MD0 and 1 contain 1s and bit 2 is a 0, a 6 is decoded indicating that an IOT instruction is to be performed. Two types of programmed IOTs are available in the PDP-8/E System. Refer to the following paragraphs for the flow diagrams; I/O Transfers (IOTs) Paragraph 3.9.5 Programmed Interrupt System Paragraph 3.9.6
(9)	JUMP Instruction – When the decoded instruction is 5_8, the PC is modified during TS3. If MD3 L = 0, the new PC is transferred to the CPMA, and the next cycle is FETCH. If MD3 L = 1, the CPMA is modified in the same manner as the PC, and the next cycle is DEFER. Refer to Paragraph 3.9.7 for the flow diagram and an explanation of the JUMP instruction.
(10)	When instructions AND, TAD, ISZ, DCA, and JMS are decoded during FETCH, the processor examines the page bit (MD4 L) and the direct/indirect address bit (MD3 L) to determine if the next address is on Page 0 or the current page, and if the next address contains an address or data. The result is the entrance into the DEFER state or the EXECUTE state. No other operation is performed with these instructions during FETCH.
(11)	Modify CPMA – The page bit is first examined to determine if the next address is on the current page (MD4 L = 1) or Page 0 (MD4 L = 0). When MD4 L = 0, signal PAGE Z is asserted. This places 0s onto the first five stages of the Adder Output Multiplexer. The last seven bits of the MD BUS are applied directly to the Adder Output Multiplexer. All 12 bits are applied to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. If PAGE Z L is not asserted, MA0 L – MA4 L are applied to the output of the Adder Output Multiplexer. Bit 3 is then examined; if bit 3 = 1, signal D SET L is asserted and the next cycle is DEFER. Otherwise, E SET L is asserted, and the processor obtains data rather than a new address. NOTE **Refer to Jump Instruction (Paragraph 3.9.7) and the memory addressing discussion in Chapter 4 of the PDP-8/E & PDP-8/M Small Computer Handbook.**

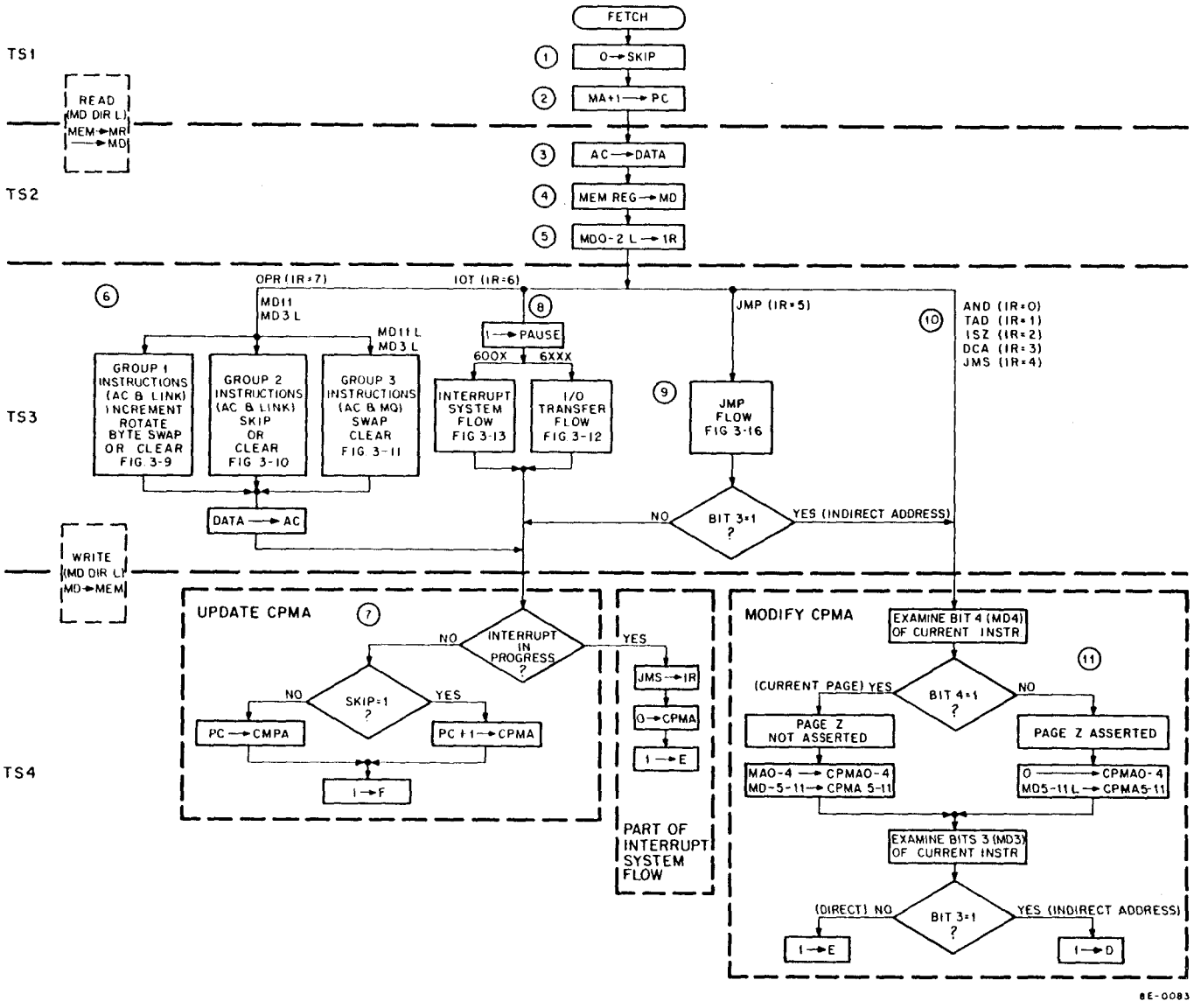


Figure 3-8 FETCH State Flow Diagram

3.9.2 Group 1 Operate Microinstructions Flow Diagram

Group 1 operate microinstructions are established when IR = 7 and when MD3 L = 0 is decoded. Eleven basic instructions are illustrated in Figure 3-9.

3.9.2.1 Data Paths – The data path for all Group 1 instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal		Source
AC to DATA BUS (exception is 7200)	AC → BUS L		Paragraph 3.35.3
DATA BUS to adders	True:	DATA T DATA F	Paragraph 3.35.3
	Complement:	DATA T DATA F	DATA T
Adder Output Multiplexer to MAJOR REGISTERS BUS	PAGE Z always L RIGHT L LEFT L TWICE L or none of these		Paragraph 3.36.2
LINK-ADDER-OUTPUT MUX to LINK	LINK data and clock		Paragraph 3.39
MAJOR REGISTERS BUS to AC Register	AC LOAD L		Paragraph 3.37.2

3.9.2.2 Basic Instructions

7000 – NOP – The NOP instruction allows the processor to cycle through one memory cycle with no important operation being implemented during TS3. Note that an AC-to-AC and LINK-to-LINK transfer is accomplished.

7001 – Increment AC – The content of the AC Register is applied to the DATA BUS when AC → BUS L is asserted. DATA F is high and DATA T L is low to allow the content of the bus to be applied to the adders. MD11 L forces a 1 into the adders from the carry in logic. The 1 is applied to bit 11 of the adders; the result is applied to the data input of the AC Register. AC and LINK are loaded during TP3.

7002 – BYTE SWAP – The first six bits of the AC Register are swapped with the last six bits. The content of the AC Register is placed on the DATA BUS and then applied to the adders by DATA T L and DATA F. AC → DATA BUS is enabled by MD4 L and MD7 L = 0. Signal TWICE L is asserted when MD10 L = 1 and will cause a parallel shift right six positions when MD8 L and MD9 L = 0. AC and LINK are loaded during TP3. However, LINK is unchanged.

7004 – Rotate Once Left – The contents of the AC are placed on the DATA BUS by signal AC → BUS L. DATA F and DATA T L apply the DATA BUS to the adders. MD9 L enables the shift left logic, and the asserted signal (LEFT) is applied to the Adder Output Multiplexer. AC and LINK are loaded during TP3.

7006 – Rotate Twice Left – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD9 L asserts the shift left logic signal and MD10 L asserts the TWICE signal; this moves the outputs of the adders two places to the left. The outputs at the output multiplexers are then loaded into the AC Registers and LINK at TP3.

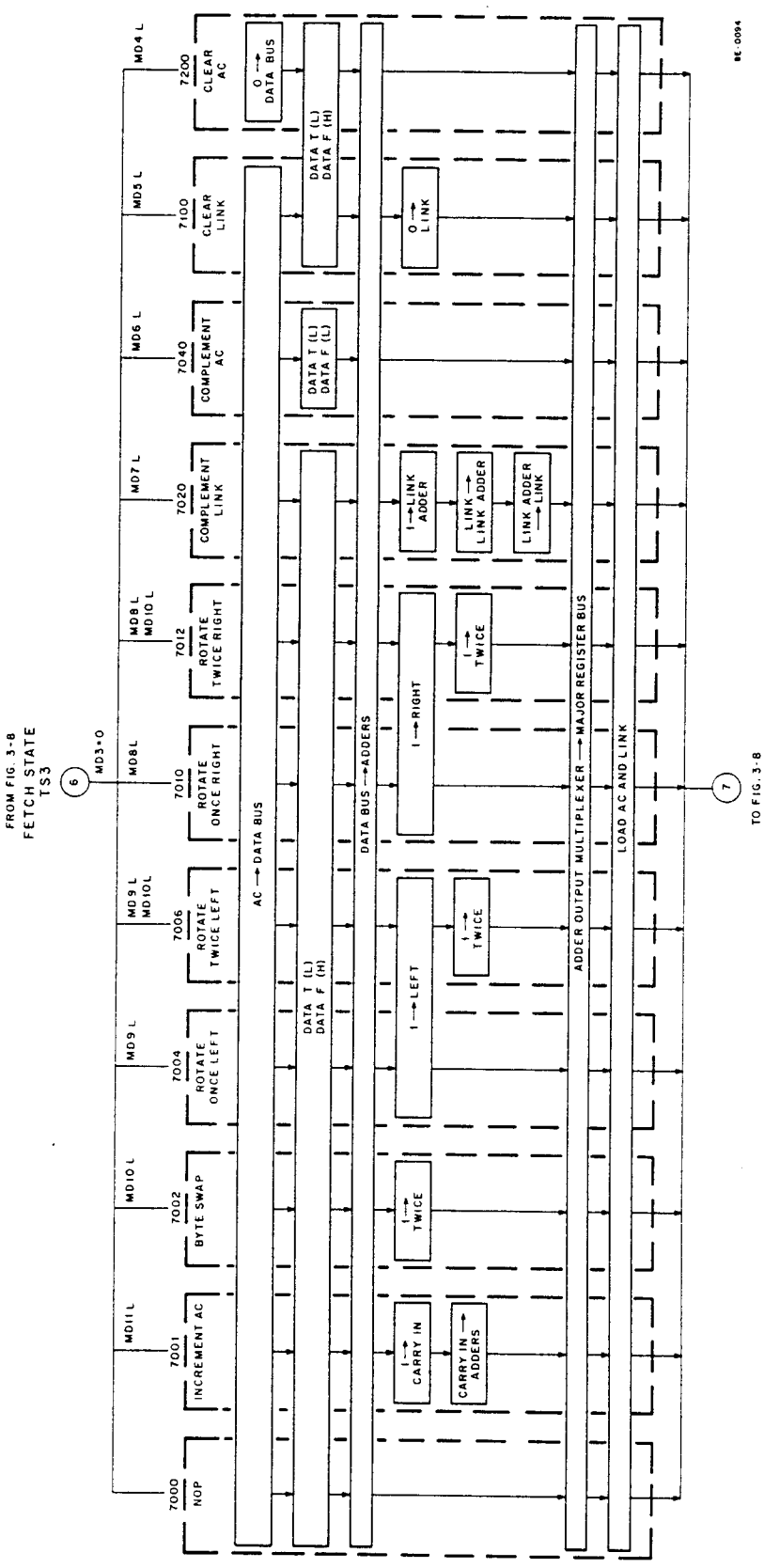


Figure 3-9 GROUP 1 Operate Microinstructions (1 Cycle)

7010 – Rotate Once Right – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD8 L develops signal RIGHT L of the shift right logic. Signal RIGHT L is applied to the output multiplexer circuit, which shifts the contents of the output multiplexers one place to the right. The outputs are then loaded into the AC Registers and LINK at TP3.

7012 – Rotate Twice Right – The content of the AC is placed on the DATA BUS. DATA F and DATA T L apply the DATA BUS to the adders. MD8 L develops signal RIGHT L and MD10 L develops TWICE L. When these two signals are applied to the Adder Output Multiplexer, the contents of the adders are shifted two places to the right. The result is loaded into the AC and LINK at TP3.

7020 – Complement LINK – MD7 L forces a 1 into the LINK circuit. The result will force a 1 to a 0 or a 0 to a 1.

7040 – Complement AC Register – The signal AC → DATA BUS L is first generated; DATA T L and DATA F are asserted so that if 1 is on the DATA BUS, a 0 is placed into the adder or if a 0 is on the DATA BUS, a 1 is placed into the adder. The AC Register is loaded at TP3.

7100 – Clear LINK – A 0 is forced into the LINK circuit when MD5 L = 1, during OPR 1.

7200 – Clear AC – DATA T L is low, DATA F is high. MD4 L disqualifies AC → BUS Logic. This causes 0s to be gated onto the DATA BUS. The contents of the DATA BUS are gated through the Data Control gate and applied to the adders and loaded into the AC Register at TP3 time.

3.9.2.3 Combining Group 1 Microinstructions – Because each instruction takes one memory cycle, it may be desirable to combine many of the instructions so that two instructions can be implemented in one memory cycle. For example, instruction 7001 can be combined with instruction 7040 to give 7041. This combines flow 7001 with flow 7040. The resulting instruction will now complement and increment the AC Register. If a 1 is to be placed into the LINK, instructions 7100 and 7020 can be combined to give 7120. The combined instruction list for commonly used Group 1 operate instructions is as follows:

7041	CIA	Complement and increment AC
7120	STL	Set LINK to a logical 1
7204	GLK	Get LINK and place content into AC bit 11
7300	CLA CLL	Clear AC and LINK
7240	CLA CMA	Set AC = -1
7201	CLA IAC	Set AC = 1
7110	CLL RAR	Shift positive 1 right
7104	CLL RAL	Shift positive 1 left
7106	CLL RTL	Clear LINK, rotate 2 left
7112	CLL RTR	Clear LINK, rotate 2 right

3.9.3 Group 2 Operate Microinstructions Flow Diagram

Group 2 operate microinstructions are established when MD3 L (1) and MD11 (L) 0 are decoded. Ten basic instructions are provided in Group 2 (Figure 3-10).

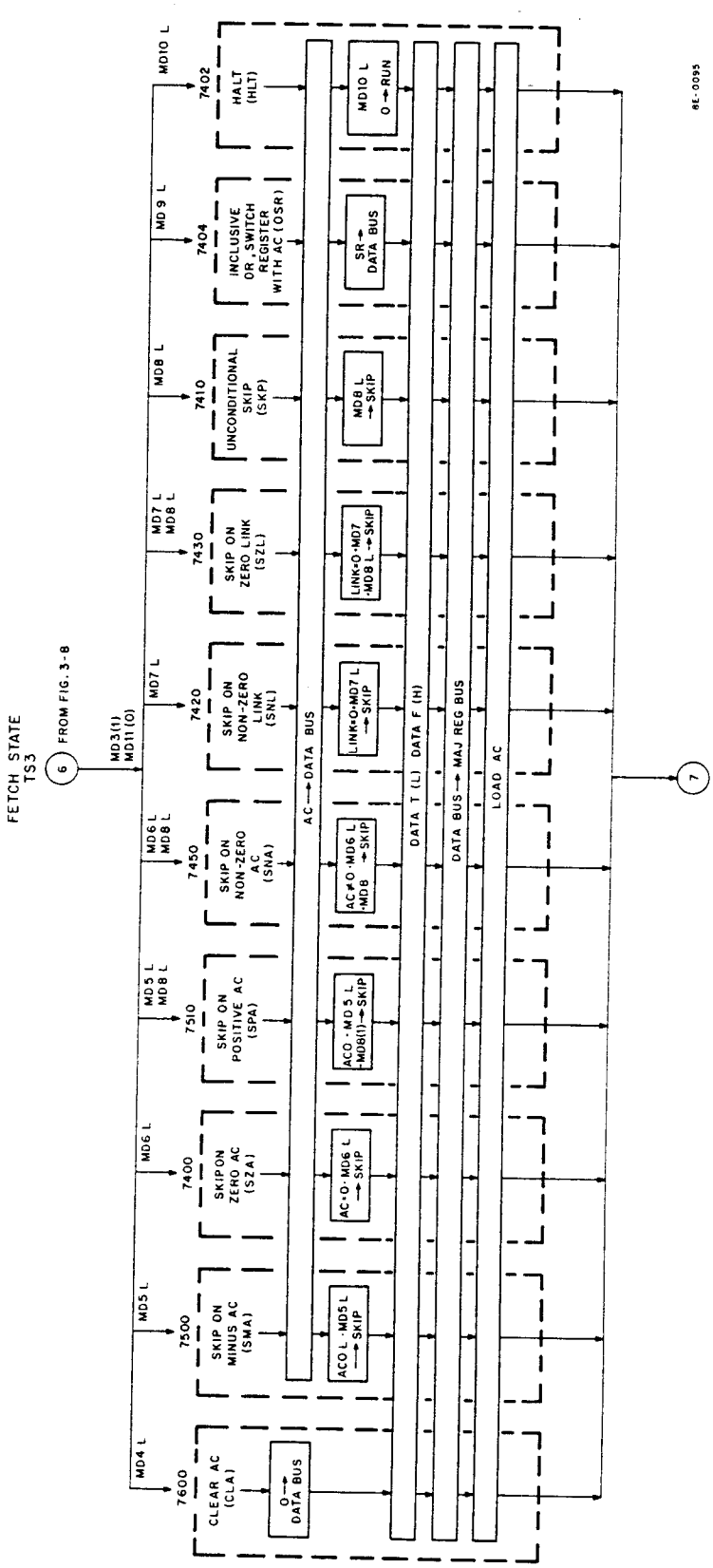


Figure 3-10 GROUP 2 Operate Microinstructions (1 Cycle)

3.9.3.1 Data Path – The data path for all Group 2 instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal	Source
AC to DATA BUS (the exception is 7600)	AC → BUS L	Paragraph 3.35.2
DATA BUS to Adders	DATA T DATA F	Paragraph 3.35.3
Adders to Adder Output Multiplexer	None	
Adder Output Multiplexer to MAJOR REGISTERS BUS	None	
MAJOR REGISTERS BUS to AC Register	AC LOAD L	Paragraph 3.37.2

3.9.3.2 Basic Group 2 Instructions

7600 – Clear AC (CLA) – Signal AC → BUS L is not asserted causing a 0 to be gated into the adder circuits. At TP3 time, 0s are loaded into the AC.

7500 – Skip on Minus AC (SMA) – The skip logic tests AC0 for a 1 when MD5 L = 1, indicating that the AC contains a negative 2's complement number. A 1 is then placed in the SKIP flip-flop. During TS4, the content of the PC is incremented by 1 so that the next sequential instruction is skipped.

7440 – Skip on Zero AC (SZA) – The skip logic tests the accumulator for all 0s when MD6 L is asserted with MD8 L (0). If AC = 0, the SKIP flip-flop is set.

7510 – Skip on Positive AC (SPA) – The skip logic tests AC0 for a 0 when MD5 L (1) and MD8 L (1) are asserted. If AC0 = 0, the SKIP flip-flop is set.

7450 – Skip on Non-Zero AC (SNA) – The skip logic tests the contents of the AC Register for all 0s. If one or more AC bits equal 0, a Skip signal is developed when MD6 L and MD8 L are asserted.

7420 – Skip on Non-Zero LINK (SNL) – The skip logic tests the LINK for 1. If LINK = 1, MD7 L = 1, and MD8 L = 0, the SKIP flip-flop will be set.

7430 – Skip on Zero LINK (SZL) – The skip logic tests the link for a 0. When LINK = 0, MD7 L = 1 and MD8 L = 1, the SKIP flip-flop is set.

7410 – Unconditional Skip (SKP) – When MD5 L – MD7 L = 0 and MD8 L = 1, the skip logic sets the SKIP flip-flop.

7404 – Inclusive OR – Switch Register with AC – (OSR) – The contents of the AC Register are transferred to the DATA BUS with signal AC →BUS L asserted. The content of the Switch Register is gated to the DATA BUS when MD9 L = 1 during a Group 2 operate instruction. Signals DATA F and DATA T L gate the ORed content of the DATA BUS through the adders and Output Multiplexers to the input of the AC Register. The AC is loaded during TP3 time. The Link circuit is not affected.

7402 – HALT (HLT) – MD10 L is used to generate a signal (STOP L) that clears the RUN flip-flop, located on the timing generator module. At the next TS1, the processor stops.

3.9.3.3 **Combining Group 2 Microinstructions** – Combinations of the 10 instructions are listed below:

7604	LAS	Clear AC, and load AC with Switch Register
7640	SZA CLA	Skip if AC = 0, then clear AC
7460	SZA SNL	Skip if AC = 0, or LINK is 1, or both
7650	SNA CLA	Skip if AC $\neq$ 0, then clear AC
7700	SMA CLA	Skip if AC is $<$ 0, then clear AC
7540	SMA SZA	Skip if AC $\leq$ 0
7520	SMA SNL	Skip if AC $<$ 0 or LINK = 1, or both
7530	SPA SZL	Skip if AC $\geq$ 0, and if LINK is 0
7550	SPA SNA	Skip if AC $>$ 0
7710	SPA CLA	Skip if AC $\geq$ 0, then clear AC
7470	SNA SZL	Skip if AC $\neq$ 0, and LINK = 0

NOTE

If Skip instructions are combined and MD8 L = 1, the Skip occurs only if all conditions are simultaneously met. (SPA, SNA, SZL are ANDed.)

If Skip instructions are combined and MD8 L = 0, the Skip occurs if any condition is met. (SMA, SZA, SNL are ORed.)

3.9.4 Group 3 Operate Microinstructions

Group 3 operate microinstructions are established when MD3 L (1) and MD11 L (1) are decoded. Eight Group 3 operate microinstructions are illustrated in Figure 3-11. Six instructions involve operations between the AC and MQ Registers.

3.9.4.1 Data Paths – The data path for all Group 3 operate instructions is illustrated in Figure 3-2. The common gating and control signals are listed below:

Data Path	Control Signal	Source
MQ to DATA BUS	MQ → BUS L	Paragraph 3.35.2
AC to DATA BUS	AC → BUS L	Paragraph 3.35.2
AC to MQ	AC → MQ EN L MQ LOAD L	Paragraph 3.40
DATA BUS to Adders	DATA T L DATA F	Paragraph 3.35.3
Adder Output Multiplexer to MAJOR REGISTERS BUS	None	
MAJOR REGISTERS BUS to AC Register	AC LOAD L	Paragraph 3.37.2
MQ MUX to MQ Register	MQ LOAD L	Paragraph 3.40

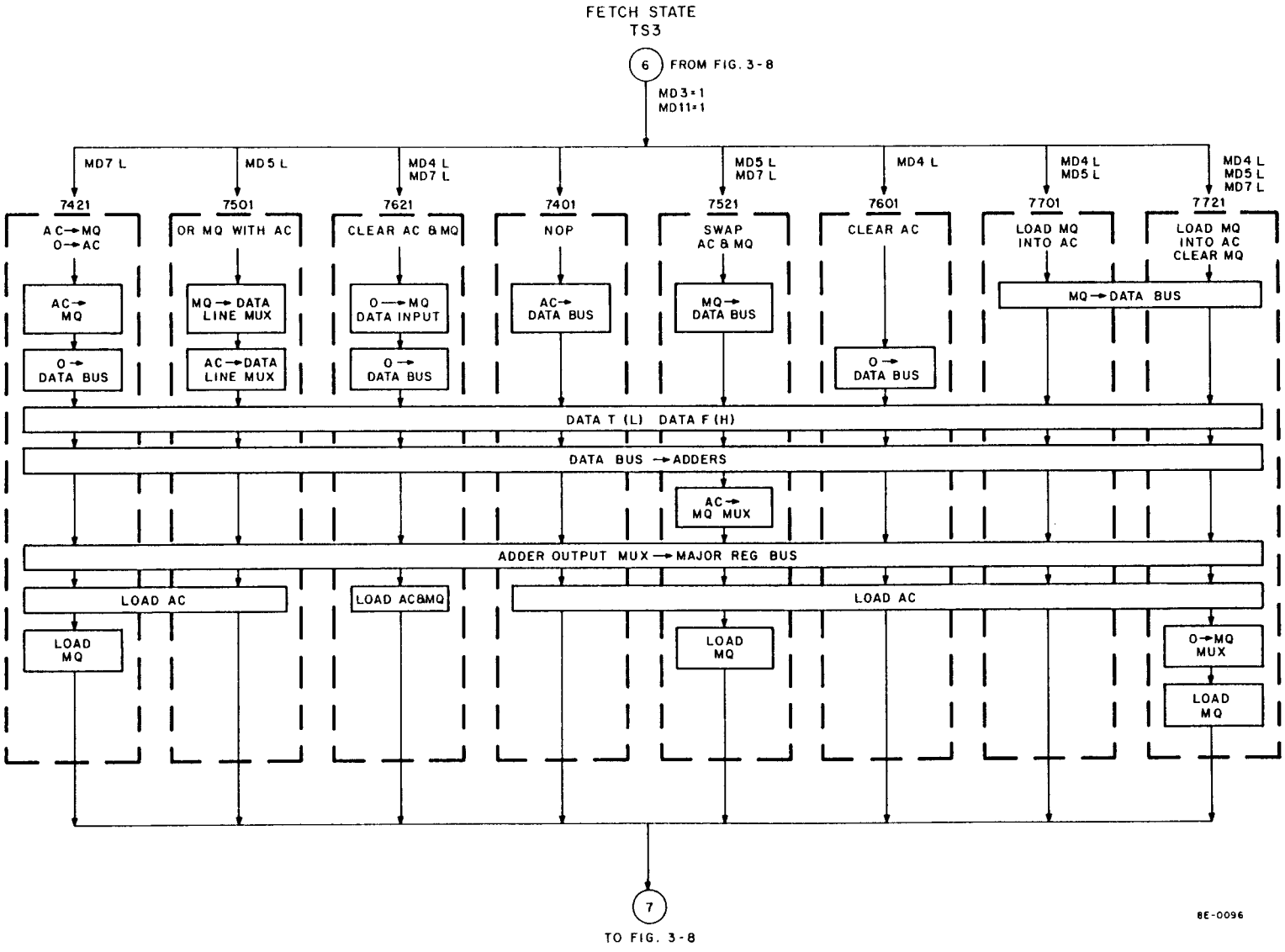


Figure 3-11 Group 3 Operate Microinstructions (1 Cycle)

3.9.4.2 Basic Group 3 Instructions

7421 – Load MQ from AC and Clear AC Register – The content of the AC Register is gated to the data inputs of the MQ Register by the MQ MUX. MQ is loaded by TP3, MD3 L – MD7 L, and MD11 L to clear the AC Register. AC → BUS L is not asserted; this places 0s on the DATA BUS. The 0s follow the data path through the Data Control Gate, through the adders, and are loaded into the AC Register at TP3.

7501 – OR MQ with AC – The contents of the MQ and AC Registers are transferred to the MAJOR REGISTERS BUS during TS3. ORing is accomplished in the Data Line MUX on a bit-by-bit basis. The result is applied to the adder and subsequently applied to the data input of the AC Register. At TP3, the AC Register is loaded.

7621 – Clear AC and MQ – Signal AC → BUS L is not asserted so that only 0s are applied to the adder circuits. AC → MQ EN L is high (MD4 L = 1), disabling the MQ MUX and, thus, placing 0s at the input to the MQ. The AC and MQ are both loaded at TP3.

7401 – NOP – No instructions are executed during NOP. The AC Register is loaded at TP3. The AC is on the DATA BUS and DATA T L is grounded.

7521 – SWAP AC and MQ – The outputs of the AC and MQ Registers take separate paths to accomplish a swap. The MQ Register output is allowed to go through the adders as a result of the MQ → BUS L control signal. The output of the AC Register is applied to the MQ MUX and gated into the MQ Register at TP3. The AC Register is also loaded at TP3.

7601 – Clear AC Register – Signal AC → BUS L is not asserted. Thus, 0s are passed through the adders and applied to the data inputs of the AC Register. At TP3 time, the AC Register is loaded.

7701 – Load MQ Register into AC Register – The contents of the MQ Register are brought into the Data Bus MUX and gated onto the Data Control Gate by MQ → BUS L enabling signal. Data enabling signals DATA T L and DATA F gate the data out to the adders and to the MAJOR REGISTERS DATA BUS. This places the data at the data input of the AC Registers. During TP3, the data is loaded into the AC Register.

7721 – Load MQ into AC and Clear MQ – The contents of the MQ Register are gated through the Data LINE MUX (Paragraph 3.34) to the Data Bus by signal MQ → BUS L. DATA T and DATA F, gate the contents to the adders and, hence, to the data input of the AC Registers. AC → MQ EN L is high, placing 0s at the input to the MQ Registers. The AC and MQ are loaded at TP3.

3.9.5 I/O Transfer Flow Diagram

The I/O transfer flow diagram is presented in Figure 3-12. There are seven sets of conditions to cause I/O transfers and six types of data transfers:

a. Data may be received from a device, ORed with the AC, and the result placed into the AC.
b. Data may be received from a device to be added to contents of the PC.
c. Data may be received from a device to replace the contents of the PC.
d. Data may be sent to a device, and the AC Register cleared.
e. Data may be received from a device and loaded into the AC.
f. Data may be sent to a device.

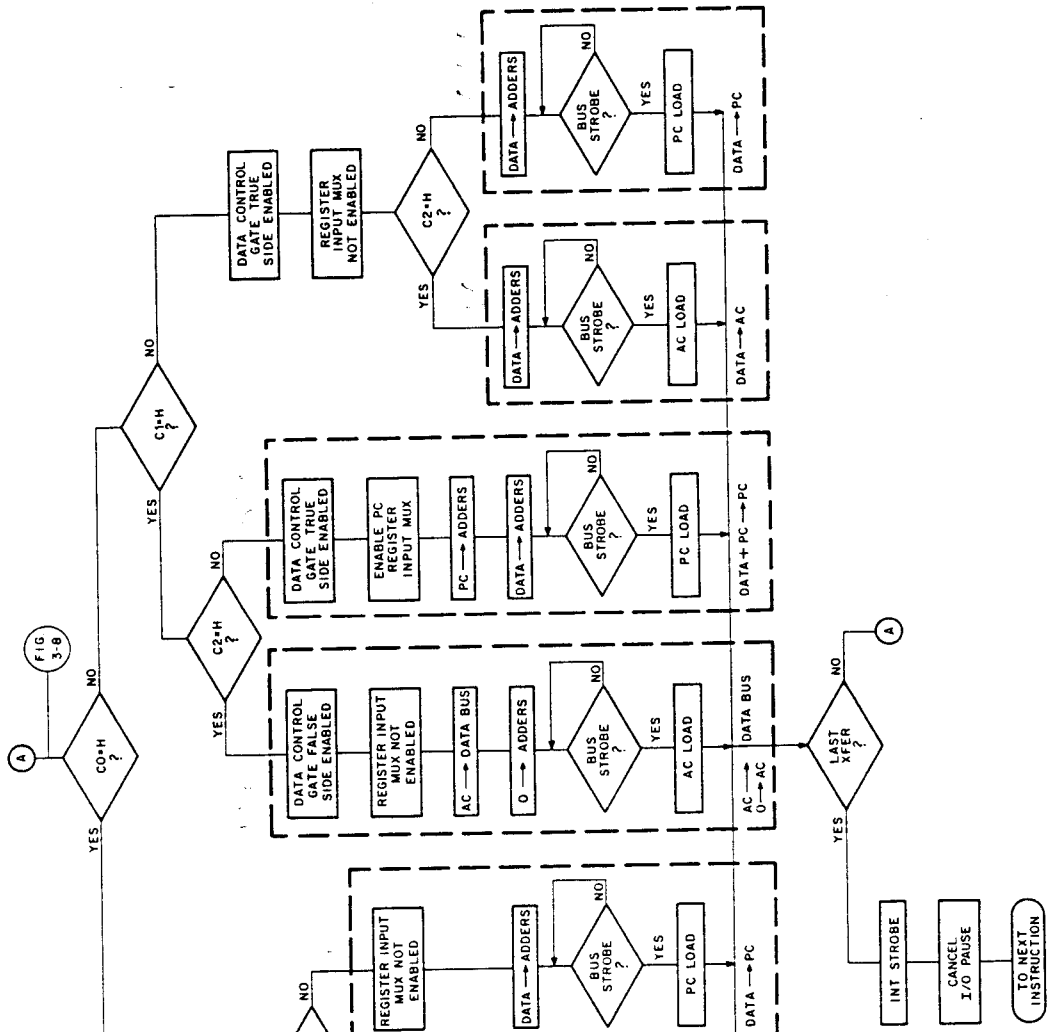


Figure 3-12 I/O Transfer Flow Diagram

The primary control signals for I/O transfer, C0 L, C1 L, C2 L, are generated by the device control logic. These signals are used to indirectly control the Register Input Multiplexer and the data control gate (Figure 3-2) through development of enabling signals EN0 L, EN1 L, EN2 L, for the Input Multiplexer and DATA T L/DATA F signals for the data control gate.

Any device control logic that is connected to the positive I/O bus interface module or requires longer than 1.2 μs provides an additional control signal called NOT LAST TRANSFER L. When this signal is asserted, the timing of the processor stops during TS3 and does not start again until the NOT LAST TRANSFER L signal is no longer asserted and BUS STROBE L is generated. At this time, INT STROBE is asserted, and I/O PAUSE L is negated. If the I/O is high-speed and internal (not involving the positive I/O bus interface), both I/O PAUSE L and INTERNAL I/O L are negated.

3.9.6 Programmed Interrupt System Flow Diagrams

The programmed interrupt system flow diagram is illustrated in Figure 3-13. The basic interrupt system includes:

a. If interrupted, complete instruction and JMS to location 0.

b. Store return address and turn off interrupt.

The interrupt service program handles the determining of the interrupting device, clearing of the flag causing the interrupt, and restoring of the processor to its original condition.

The flow diagram (Figure 3-13) assumes that the interrupt system was turned on during the restoration housekeeping routine.

Flow Reference	Explanation
(1)	CHECK INTERRUPT REQUEST LINE – During the next processor cycle, after the interrupt system was turned on (with instruction ION), the INT DELAY flip-flop is set at TP1 (Paragraph 3.42). This is a necessary condition to set the INT SYNC flip-flop. Because any instruction begins during FETCH and may take several cycles before completion, the last instruction cycle asserts F SET L. At this time, the Interrupt Request line may be tested. If there is no Interrupt Request, the processor returns to the beginning of the FETCH state for the next instruction. Otherwise, it will begin servicing the interrupt.
(2)	With the Interrupt Request line asserted, and the INT DELAY flip-flop set, the INT SYNC flip-flop is set. This asserts the INT IN PROG line which, in turn, forces a JMS into the IR and asserts F E SET. Thus, on the next processor cycle, the EXECUTE major state will be active to store the return address. Because the Register Input Multiplexer (Figure 3-2) is not enabled to allow the PC to transfer to the CPMA during TS4, 0 will be loaded into the CPMA at TP4.
(3)	TURN OFF INTERRUPT SYSTEM – During the EXECUTE major state, the Interrupt System is turned off by clearing the interrupt enable (INT EN) flip-flop, which clears the INT DELAY and INT SYNC flip-flops, negating INT IN PROG.

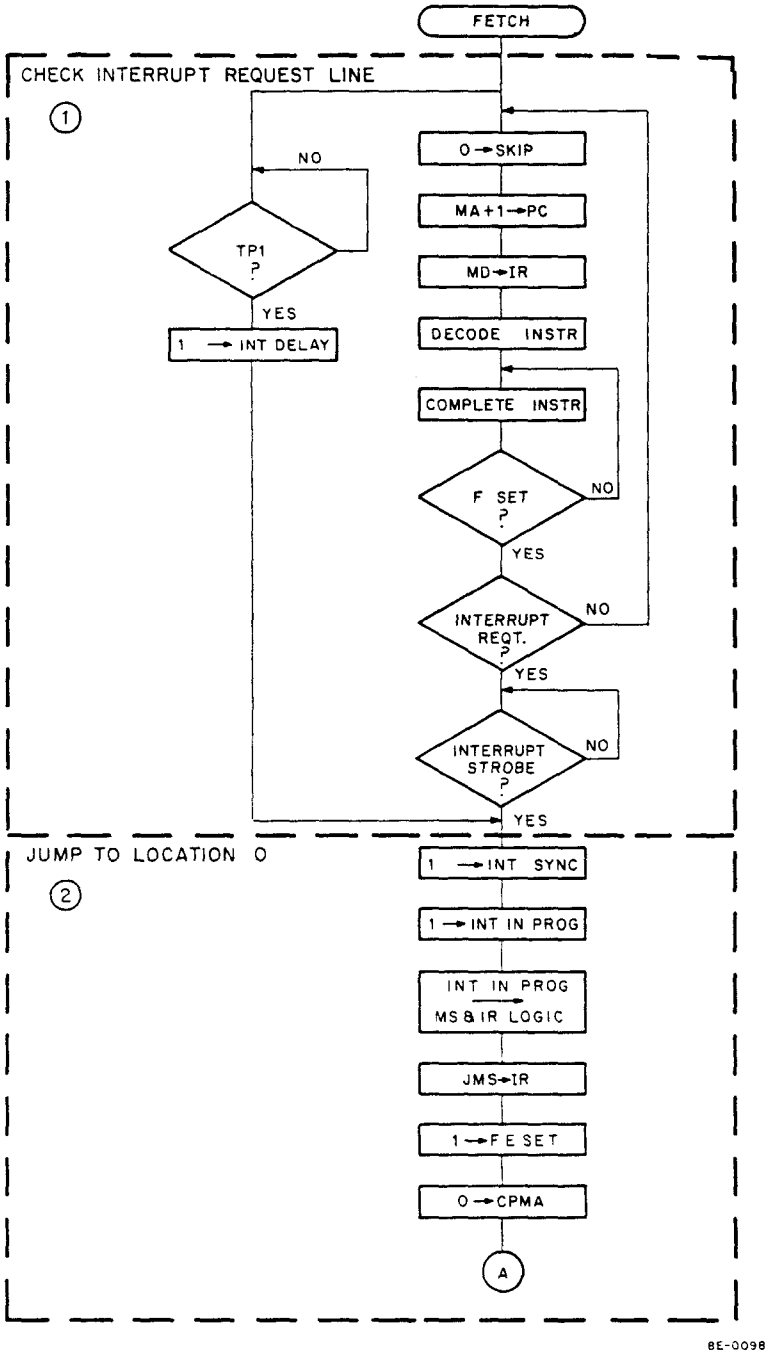


Figure 3-13 Programmed Interrupt System Flow Diagram (Sheet 1 of 2)

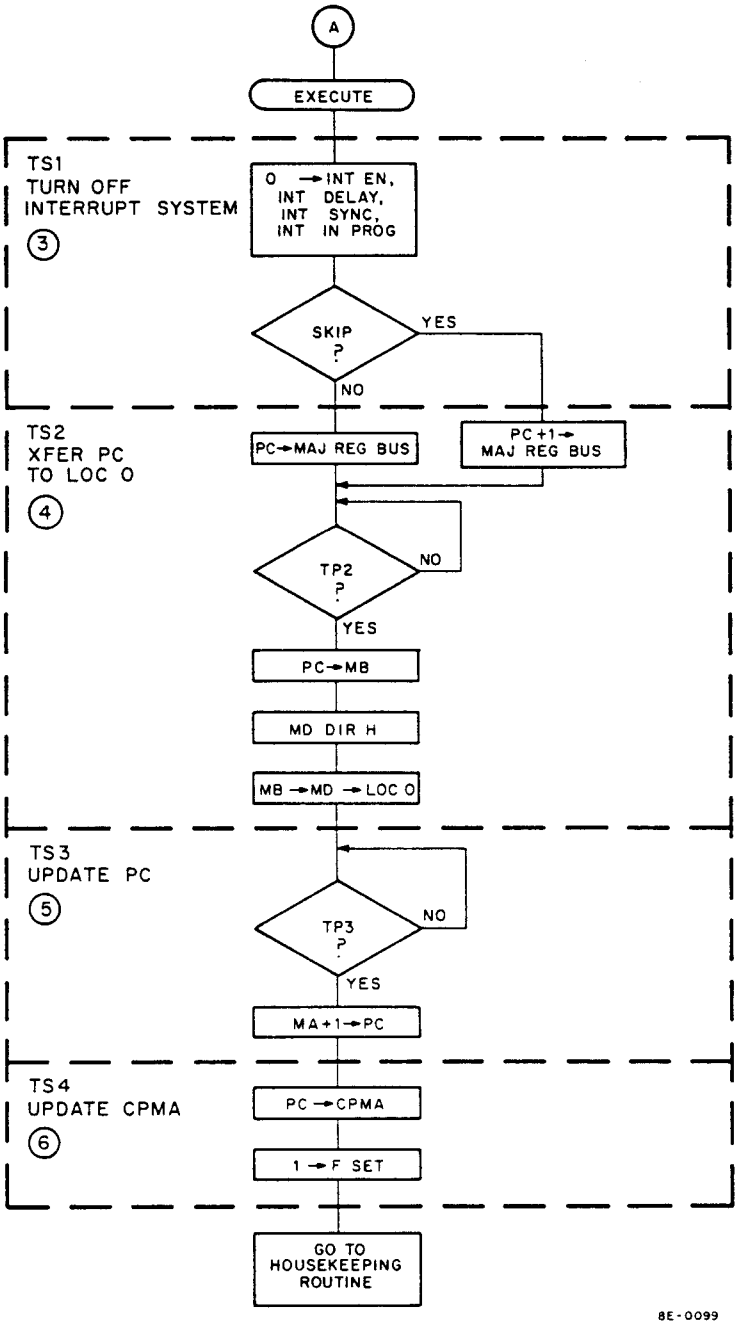


Figure 3-13 Programmed Interrupt System Flow Diagram (Sheet 2 of 2)

Flow Reference	Explanation
(4)	TRANSFER PC TO LOCATION 0 – The contents of the PC are transferred to location 0 during TS2. The Register Input Multiplexer is enabled to allow the contents of the PC to be applied to the MAJOR REGISTERS BUS (Figure 3-2). If the SKIP flip-flop is set, CAR IN is also asserted. At TP2, the content of the MAJOR REGISTERS BUS is loaded into the MB Register. Because MD DIR L is negated (H) at TP2, the content of the MB is immediately applied to the MD BUS, gated into the inhibit drivers, and routed to the addressed memory location (location 0).
(5)	UPDATE PC – During TS3, the content of the CPMA is gated through the Register Input Multiplexer and applied to the adders (Figure 3-2). A CAR IN L signal is developed that places a 1 on adder stage 11. The result is applied to the MAJOR REGISTERS BUS and loaded into the PC at TP3.
(6)	UPDATE CPMA – During TS4, the Register Input Multiplexer is enabled to allow the content of the PC to be applied to the MAJOR REGISTERS BUS and loaded into the CPMA at TP4. Because INT IN PROG is not active, F SET L will be asserted and the next processor cycle will be FETCH. In the event that any important data is in the AC and LINK, a housekeeping routine to store this data must be enacted.

3.9.6.1 Check Interrupt Request Line (SRQ) Instruction Flow Diagram – Refer to Figure 3-14 for the following discussion:

Flow Reference	Explanation
(1)	During TS1, the SKIP flip-flop is cleared. The content of the CPMA Register is gated through the Register Input Multiplexer (Figure 3-2) and placed on the adders. A 1 is developed by the Carry In logic and placed on the adder stage 11. The MA + 1 result is then loaded into the PC Register at TP1. The flow diagram assumes that the current addressed memory location contains instruction (6003) SRQ. READ memory begins during the latter portion of TS1.
(2)	During the second half of TS1 and the first half of TS2, the READ operation is active, and the content of the addressed memory location is read into the memory register (Figure 3-2). Because MD DIR L was asserted during TS1, the content of the memory register will be gated out to the MD BUS and ready for decoding. The Instruction Register looks at the first three bits (0–2) and decodes the IOT. I/O PAUSE L is generated earlier. I/O PAUSE L allows the IOT Decoder to decode the last three bits, providing the middle six bits are 0s. Because the last three bits contain 3_8 (for an SRQ instruction), the Interrupt Request line is now ready to be tested during TS3.
(3)	If an Interrupt Request has been made, signal SKIP L is asserted.
(4)	When SKIP L is asserted, CAR IN L is developed, and a 1 is placed on adder stage 11. The Register Input Multiplexer (Figure 3-2) is enabled so that the content of the PC is placed on the adders. The content of the PC + 1 is applied to the MAJOR REGISTERS BUS and loaded into the CPMA during TS4. If SKIP L was not asserted, only the PC is loaded into the CPMA, and the processor goes on to the next sequential instruction. Otherwise, a Flag Check subroutine is next performed.

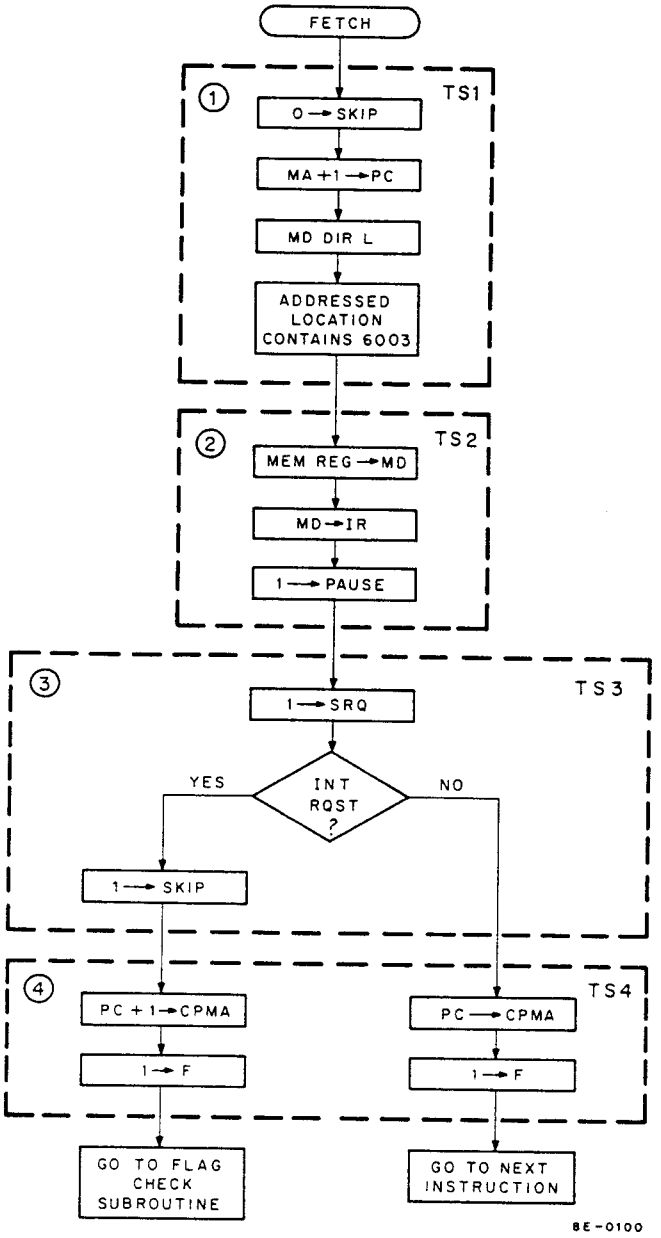


Figure 3-14 Check Interrupt Request Line Instruction Flow Diagram

3.9.6.2 **Turn On Interrupt (ION) System** – The Interrupt System is turned on during the restoration housekeeping routine (Figure 3-13). Refer to Figure 3-15 for the following discussion:

Flow Reference	Explanation
(1)	The SKIP flip-flop is cleared during TS1, and a 1 is added to the content of the CPMA and loaded into the PC.
(2)	With MD DIR L, the content of the addressed memory location is placed on the MD BUS during the READ operation. The instruction is applied to both the Instruction Register and the IOT Decoder.
(3)	The resulting ION instruction sets the INT EN flip-flop at TP3.
(4)	At TS4, the CPMA Register is updated and F SET L is enabled.

NOTE

During the cycle following TP1, INT DELAY is set; this ensures that the processor cannot honor an interrupt until the end of the next instruction.

3.9.7 JUMP Instruction

The JUMP instruction first modifies the PC and then modifies the CPMA so that both contain the new address at the start of the next instruction. A test is also made to determine if the instruction is direct addressed (the next processor cycle is FETCH), or if the instruction is indirectly addressed (the next processor cycle is DEFER). If the instruction is direct addressed, the content of the addressed memory location will be an instruction. If the address is indirect, the content of the addressed memory location will contain the address of the next instruction.

The JUMP instruction flow diagram is illustrated in Figure 3-16. This flow diagram is a subflow of Figure 3-8 and contains only the TS3 portion of the JUMP instruction.

If MD4 L = 1, PAGE Z L is not asserted (indicating that the new address will be on the current page). The first five CPMA output lines are routed through the Adder Output Multiplexer to the MAJOR REGISTERS BUS. Thus, the first five MA bits are gated through to the MAJOR REGISTERS BUS.

If MD4 L = 0, PAGE Z L is asserted; the first five MA bits are negated and cause 0s to be placed on the MAJOR REGISTERS BUS.

Because MD5 L – MD11 L output lines are routed directly to the Adder Output Multiplexer, these seven bits are applied to the MAJOR REGISTERS BUS. The content of the MAJOR REGISTERS BUS is then loaded into the PC at TP3, and a test for direct or indirect addressing is next accomplished. (Note that if JMP is indirect, the PC is loaded twice, once during FETCH, and the second time during DEFER. The first address is ignored.) The modification of the CPMA is accomplished in a similar manner (Figure 3-8).

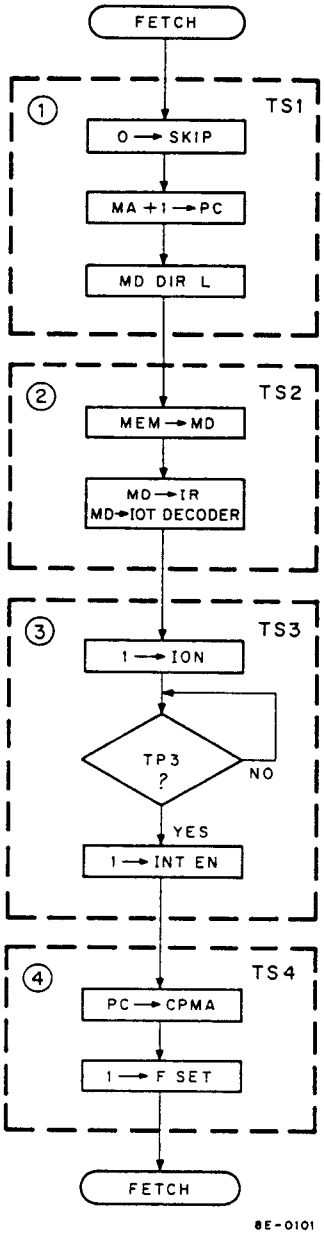


Figure 3-15 Turn On Interrupt (ION) System Flow Diagram

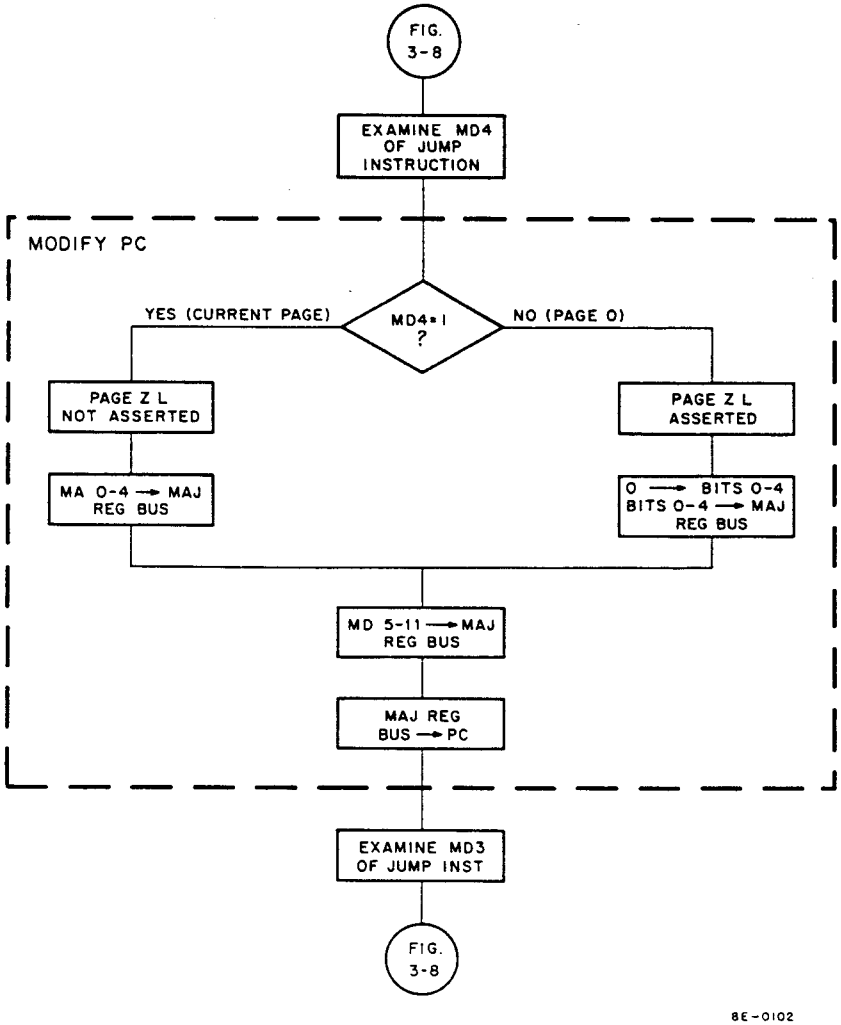


Figure 3-16 Direct JUMP Instruction Flow Diagram

3.10 DEFER STATE INSTRUCTION FLOW DIAGRAM

The DEFER state instruction flow diagram is illustrated in Figure 3-17. DEFER performs two types of functions. During any one processor cycle, DEFER provides an indirect address to the location containing the operand; if the addressed location is between 10_8 and 17_8, it provides the autoindex operation.

Flow Reference	Explanation
(1)	The DEFER state is always entered from the FETCH state, on indirect addressing. During the last half of TS1 and the first half of TS2, the content of the addressed memory location is read from memory and placed in the Memory Register (Figure 3-2). Because MD DIR L is asserted at this time, the content of the Memory Register is gated out to the MD BUS.
(2)	The content of the MD BUS is gated through the Register Input Multiplexer to the adders (Figure 3-2) using Register Input Enable Logic. At the same time, the Carry In logic places a 1 in the adders. The result is then placed on the MAJOR REGISTERS BUS and, at TP2, is loaded into the MB Register.

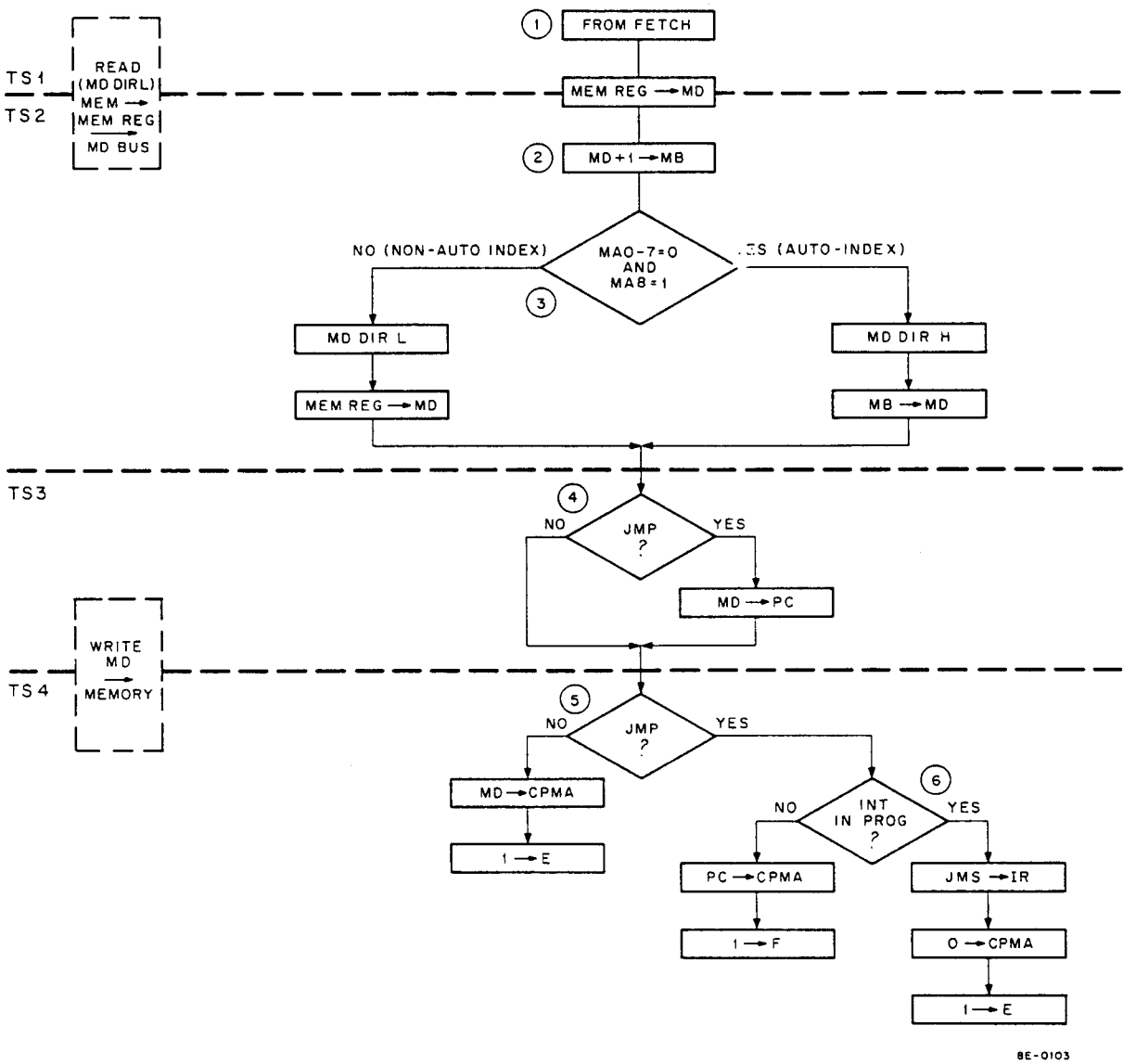


Figure 3-17 DEFER State Instruction Flow Diagram

Flow Reference	Explanation
(3)	The autoindex operation is determined by examining the content of the first nine Memory Address bits. If bits 0–7 contain 0s and bit 8 contains a 1, MD DIR L is allowed to go high and the content of the MB Register (which contains MD + 1) is gated onto the MD BUS. Otherwise, MD DIR L remains low and the content of the Memory Register is gated onto the MD BUS.
(4)	If the JMP instruction is in the IR, the content of the MD is gated through the Register Input Multiplexer, through the adders, onto the MAJOR REGISTERS BUS, and loaded into the PC at TP3. Remember the MD BUS carries either the previous memory contents (if the instruction is not autoindexed), or the incremented memory contents (if the instruction is autoindexed). If JUMP is not in the IR, then no action is taken during TS3, and JUMP is tested again in TS4.
(5)	If the JMP instruction is in the IR, the processor goes on to test the INT IN PROG line. Otherwise, the content of the MD BUS is again gated through the Register Input Multiplexer, through the adders, and onto the MAJOR REGISTERS BUS. At TP4, the CPMA is loaded containing the new address of the operand. The combination of DEFER and JMP does not necessarily cause the next processor state to be EXECUTE.
(6)	If the IR contains JMP, the INT IN PROG line is tested. If no interrupt has occurred, the content of the PC is gated through the Register Input Multiplexer, through the adders to the MAJOR REGISTERS BUS. At TP4, the CPMA is loaded. Because the current major state is DEFER and the instruction is JMP, the next major state must be FETCH. If there is an INT IN PROG, a JMS is forced into the Instruction Register, all 0s are forced into the CPMA, and the next major state is EXECUTE.

3.11 EXECUTE STATE INSTRUCTION FLOW DIAGRAM

The EXECUTE state instruction flow diagram is shown in Figure 3-18. EXECUTE can be entered from FETCH, DEFER, or EXECUTE. During the second half of TS1 and the first half of TS2, the READ operation is performed. MD DIR L is also asserted to allow the content of the addressed memory location to be gated out to the MD BUS (Figure 3-2).

Flow Reference	Explanation
(1)	The operation of the AND and TAD instructions is the same during TS2. The MD gate of the Register Input Multiplexer is enabled and the content of the MD BUS is placed on the MAJOR REGISTERS BUS. At TP2, MB LOAD L is developed and loads the content of the MAJOR REGISTERS BUS into the MB Register. Also at TP2, MD DIR L is allowed to go high and the content of the MB is automatically placed on the MD BUS. Although this operation does not change any register or bus during an AND or TAD instruction, it is automatic for both instructions during the EXECUTE state.

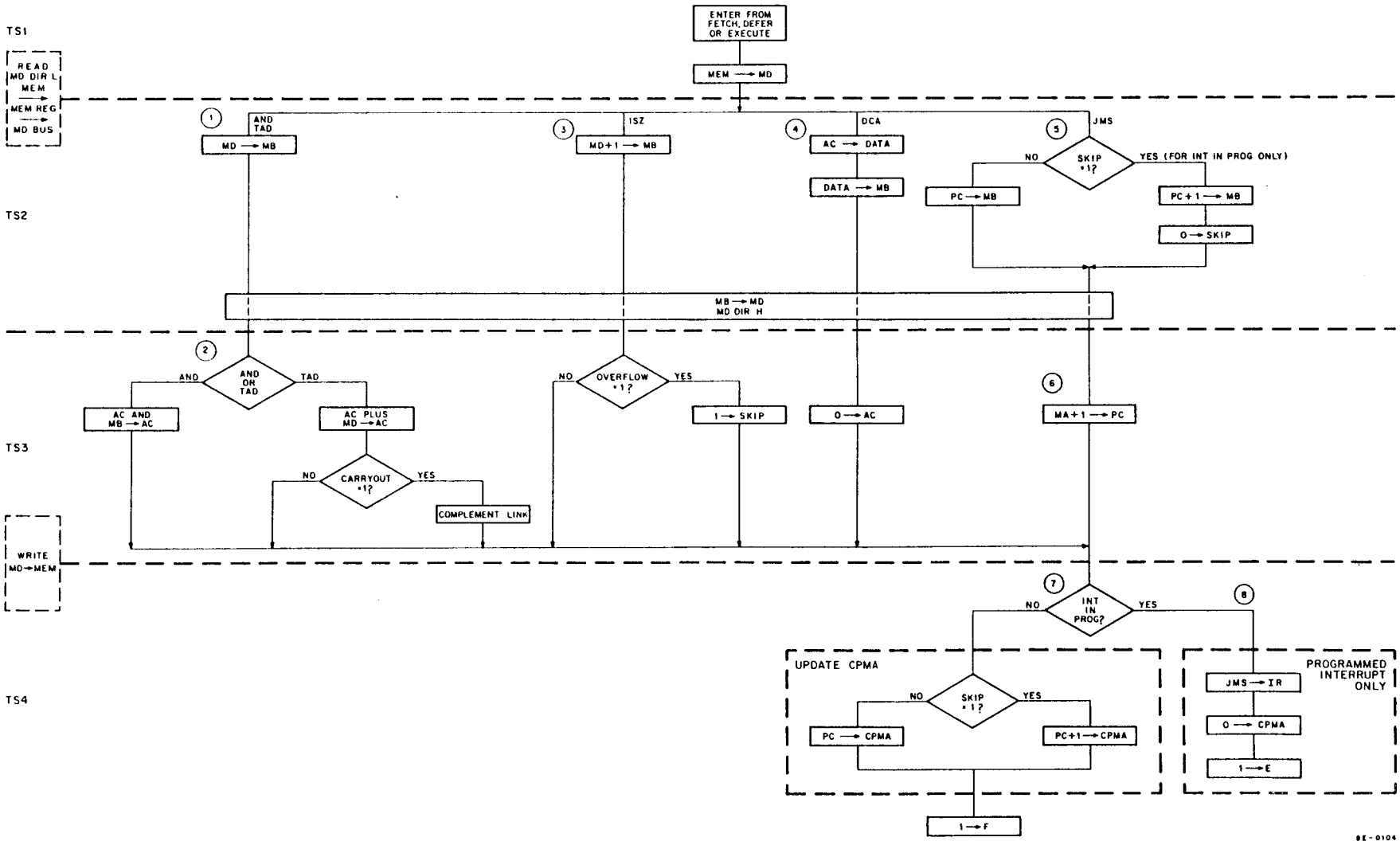


Figure 3-18 EXECUTE State Instruction Flow Diagram

Flow Reference	Explanation
(2)	If the instruction is AND, the AC/MB AND gate (Figure 3-2) receives the content of the AC and the MB. A logical AND function will be performed for each of the 12 bits; there is no carry from one stage to the next. The ANDed result is then applied to the Adder Output Multiplexer and placed on the MAJOR REGISTERS BUS. At TP3, the content of the MAJOR REGISTERS BUS is loaded into the AC. For a TAD instruction, the process differs. The Register Input Multiplexer is enabled to allow the content of the MD BUS to be applied to the adders. To bring the AC to the adders, enabling signal AC → BUS L is first developed. This places the content of the AC on the DATA BUS. To apply the content of the DATA BUS to the other side of the adders, the Data Control Gate (DATA T L) is enabled. The resulting addition is then applied to the MAJOR REGISTERS BUS and loaded into the AC at TP3. If CAR OUT L equals a 1, the result is applied to the Link Adder circuit, and the LINK is complemented.
(3)	If ISZ is in the Instruction Register, CAR IN L is asserted, which places a 1 in the adders at TS2. At the same time, the Register Input Multiplexer is enabled to allow the contents of the MD BUS to be placed onto the adders. If the OVERFLOW flip-flop is not set at TP2, no operation is performed during TS3. If the OVERFLOW flip-flop is set to 1, a 1 is developed on the SKIP line. (See Flow Reference (7) for CPMA Update.)
(4)	If instruction DCA is in the Instruction Register, signal AC → BUS L is developed, and the content of the AC Register is applied to the DATA BUS (Figure 3-2). The Data Control Gate is enabled next; thus, the content of the DATA BUS can be applied to the MAJOR REGISTERS BUS. At TP2, the content of the MAJOR REGISTERS BUS is then loaded into the MB Register and because MD DIR L goes high at TP2, the content of the MB Register is gated onto the MD BUS. To clear the AC, signal AC → BUS L is not asserted, and DATA T L is high. With DATA T L high, 0s are applied to the MAJOR REGISTERS BUS and loaded into the AC Register at TP3. The contents of the MD BUS are then applied to the inhibit drivers for the WRITE operation. WRITE begins during the second half of TS3 and continues through the first half of TS4.
(5)	If a JMS instruction is in the Instruction Register, the Register Input Multiplexer is enabled to allow the content to the PC to be applied through the adders to the MAJOR REGISTERS BUS and loaded into the MB Register at TP2. The SKIP L signal is also tested during TS2. If the Skip logic has produced a 1, SKIP L signal is applied to the Carry In logic, and signal CAR IN L becomes a 1*. This is applied to the adders and added to the content of the PC. The result is then applied to the MAJOR REGISTERS BUS and loaded into the MB at TP2. At TP2, the SKIP flip-flop is also cleared. (This condition can occur only when an interrupt is honored immediately after an OPR, IOT, or ISZ instruction.)
(6)	A CAR IN L signal is asserted and a 1 is placed in the adders. The content of the CPMA Register is gated through the Register Input Multiplexer to the adders. The result is applied to the MAJOR REGISTERS BUS and loaded into the PC Register at TP3.

*AC signal line is pulled low.

Flow Reference	Explanation
(7)	For all instructions, if there is no INTERRUPT IN PROGRESS, the SKIP L signal line is tested. If SKIP L does not equal 1, no CAR IN L signal is developed and the content of the PC Register is gated through the Register Input Multiplexer and then applied to the MAJOR REGISTERS BUS. At TP4, the content of the BUS is loaded into the CPMA Register. If the SKIP L signal equals 1 (because of ISZ and CARRY OUT), a CAR IN L signal is developed and applied to the adders. This signal is added to the PC and loaded into the CPMA at TP4. In both cases, F SET L is asserted and the next major state is FETCH.
(8)	If there is an INTERRUPT IN PROGRESS, a JMS instruction is forced into the Instruction Register and the Register Input Multiplexer is enabled so that 0s are applied to the MAJOR REGISTERS BUS. During TP4, the content of the BUS is loaded into the CPMA and EXECUTE is clocked into the Major States Register.

3.12 TIMING GENERATOR, GENERAL DESCRIPTION

The M8330 Timing Generator provides synchronizing signals for memory and processor operations. Eight basic processor timing signals and five basic memory timing signals are generated.

3.13 TIMING GENERATOR, FUNCTIONAL DESCRIPTION

Figure 3-19 shows the functional sections of the PDP-8/E Timing Generator. At the heart of the timing operation is a chain of 4-bit shift registers, designated the Timing Shift Register. A preset combination of logic 1s and 0s is repetitively cycled through the chain. Selected outputs of the Timing Shift Register are used to control flip-flops that produce the basic timing signals. Think of the chain of shift registers as a tapped delay line; in this way the concept of shift register timing might be more easily understood. A control signal is placed on the input of this delay line at time 0. This signal flows along the delay line and is sampled at selected taps, where it is used to set or reset flip-flops. Thus, consecutive timing signals can be produced. When the signal reaches the end of the delay line it can be returned to the beginning to start another timing cycle.

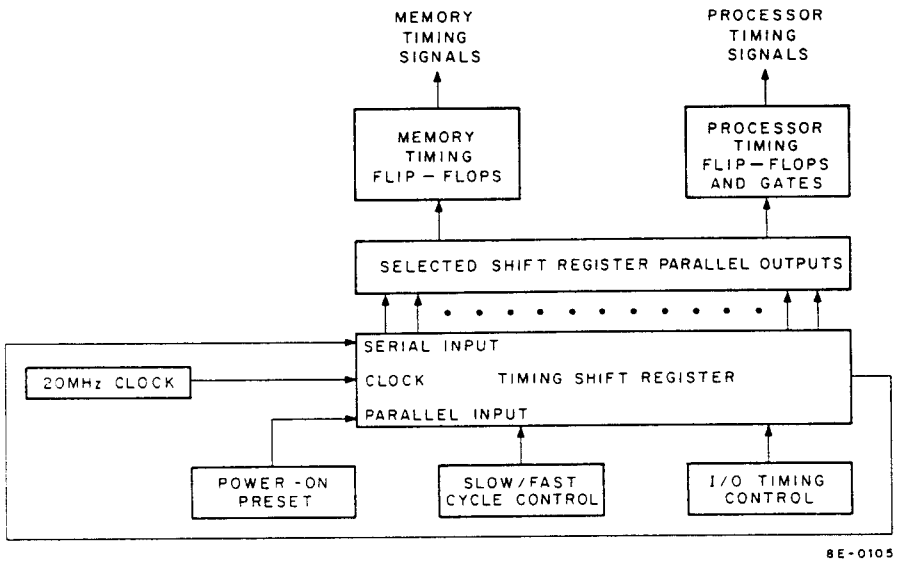


Figure 3-19 Timing Generator, Block Diagram

The delay line concept is easily understood; however, the PDP-8/E features a variable timing cycle. A delay line does not provide the necessary balance between flexibility and simplicity of design, nor does it provide a stable cycle time. Balance and stability are achieved by using a chain of shift registers to produce the timing signals. In its simplest form, the Timing Shift Register is a 28-bit shift register that is right-shifted by clock pulses derived from a 20 MHz, crystal-controlled transistor oscillator.

3.14 BASIC TIMING OPERATION

Figure 3-20 is a simplified representation of the Timing Shift Register; it illustrates the basic timing operation. Assume a method exists for presetting a 0 voltage level in the first stage of this register and also presetting positive voltage levels in every other stage. After this initial condition has been established, the clock is turned on. The first clock pulse shifts the 0 level to stage 2; simultaneously, the positive level from stage 28 is shifted into stage 1. Clock pulse 2 shifts the 0 level into stage 3 and simultaneously shifts a positive level into both stages 1 and 2. Each pulse moves the 0 level to the right by 1 bit, replacing it with a positive level. When the clock shifts the level into stage 5, the flip-flop is cleared by the negative-going edge of the pulse. The flip-flop remains in this reset state until clock pulse 8 shifts the level into stage 9, thereby setting the flip-flop. The signal produced at the 0 side of the flip-flop is a 200 ns gate. Pulses can also be generated, as shown by the AND gate connected to stage 12. When the level is shifted into the stage by clock pulse 11, the gate is enabled and the desired output is produced.

The actual operation is more detailed than the example given, although the basic shifting process remains the same. As the block diagram indicates, the shift register is preset by a circuit that operates the moment power is turned on. Each clock pulse shifts the preset control signal to the right; the register is recycled by connecting the last stage back to the first. In the simplest arrangement, a complete cycle requires 28 clock pulses, or 1.4 μs; this is the "slow" cycle. If a "fast" cycle is called for, the slow/fast cycle control decreases the cycle time by 200 ns. Another control network that modifies the basic shifting operation is shown as I/O timing control on Figure 3-19. This control is used to interrupt the timing cycle while certain I/O transfers are carried out. All of these control circuits are discussed in detail in the following sections.

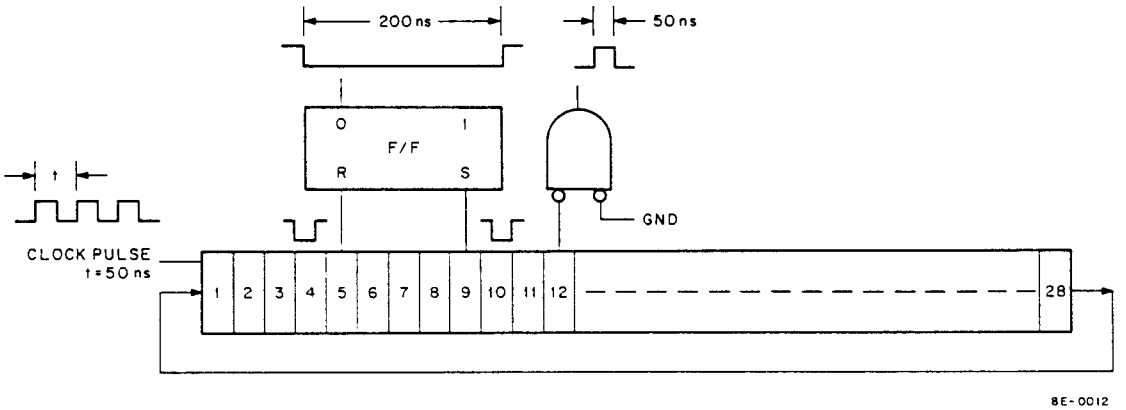


Figure 3-20 Simplified Timing Shift Register Operation

3.15 TIMING SHIFT REGISTER

As previously noted, the shift register is the key to the timing operation. The shift register comprises ten DEC 74194, 4-bit shift registers. A logic representation of the DEC 74194 integrated circuit (IC) is shown in Figure 3-21. The circles at the outputs of each bit (pins 15, 14, 13, and 12), at the corresponding parallel-entry inputs (pins 3, 4, 5, and 6, respectively), and at the serial-in (S) line, indicate that ground level signals represent logic 1s. If the mode (M) input is taken to a positive voltage, the DEC 74194 IC is programmed for parallel loading. Those signals present at the parallel-entry inputs are transferred to the corresponding outputs by a clock pulse at C. Thus, the logic 1 at pin 3 is transferred to output pin 15. The same clock pulse transfers a logic 1 from pin 4 to pin 14 and logic 0s from pins 5 and 6 to pins 13 and 12, respectively.

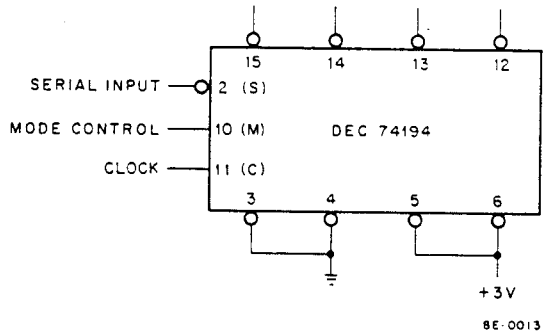


Figure 3-21 DEC 74194 Shift Register Logic

If the M input is taken to ground, rather than to a positive voltage, the DEC 74194 IC is programmed for shifting operation and the parallel-entry inputs are disabled. Information at the S input is shifted to the right one bit each time a clock pulse is applied at C. Thus, a logic 1 at S is shifted to pin 15 by the first clock pulse, to pin 14 by the second, etc. Refer to Appendix A for a detailed discussion of DEC 74194.

Ten shift register ICs are connected to form the Timing Shift Register referred to in Figure 3-19. This arrangement is presented in detail in Figure 3-22. For the moment, all ICs, with the exception of the first, E43, are shown programmed for serial-shift operation; i.e., the M inputs are grounded. Outputs that are used to produce the timing signals are identified according to function. Parallel-entry inputs are shown only on E43.

The discussion of the 28-stage shift register (Figure 3-20) assumed that the register could be preset so that stage 1 contained a 0-voltage level, while all other stages contained positive voltage levels. Essentially, this is accomplished by the power-on preset control. This control operates when the power is first turned on and ensures that, before a timing cycle is initiated, bits 1 and 2 of E43 (represented by output pins 15 and 14, respectively) contain logic 1s, while all other bits of the Timing Shift Register contain logic 0s. The control takes the M input of E43 to a positive voltage and maintains this voltage for a predetermined delay period. Thus, during this time period E43 is programmed for parallel-entry, while the remaining ICs of the register are programmed for serial shifting (the delay period is required to offset the indeterminate state of individual bits at power turn-on; because a bit can assume either a 0 or a 1 level at power-on, the delay period is used to shift out of the register any logic 1s that may be present). The first clock pulse that occurs transfers the logic levels at the parallel-entry inputs of E43 to the outputs. Pins 15 and 14 go to ground (logic 1), and pins 13 and 12 go to +3V (logic 0). The logic 0 at pin 12 is applied to the S input of E38. Thus, the next clock pulse shifts the logic 0 into E38. Each succeeding clock pulse does the same, while also right-shifting the register. During the shifting operation, a signal from the control holds the timing flip-flops in the reset state. This action ensures that the logic 1s being shifted through the register have no affect on the flip-flops. All logic 1s are shifted out of the register in approximately 1.2 μs (25 clock pulses). The register is then in the preset condition.

When the predetermined delay period has ended, E43 must be placed in the right-shift mode by activating a key on the operator's console, thereby asserting the OMNIBUS MEM START L signal. This signal causes the power-on preset control to bring the M input of E43 to ground, programming E43 for shifting operation. Clock pulses at C begin shifting the logic 1s of bits 1 and 2 to the right. A negative pulse moves through the shift register (see Figure 3-23 for a graphic representation of this pulse). The negative-going edge is used to set and reset flip-flops, thereby producing timing gates, while the entire pulse is used to produce timing pulses. Note that 28 clock pulses return the register to the initial condition; thus, a timing cycle of 1.4 μs results (28 clock pulses X 50 ns per clock pulse).

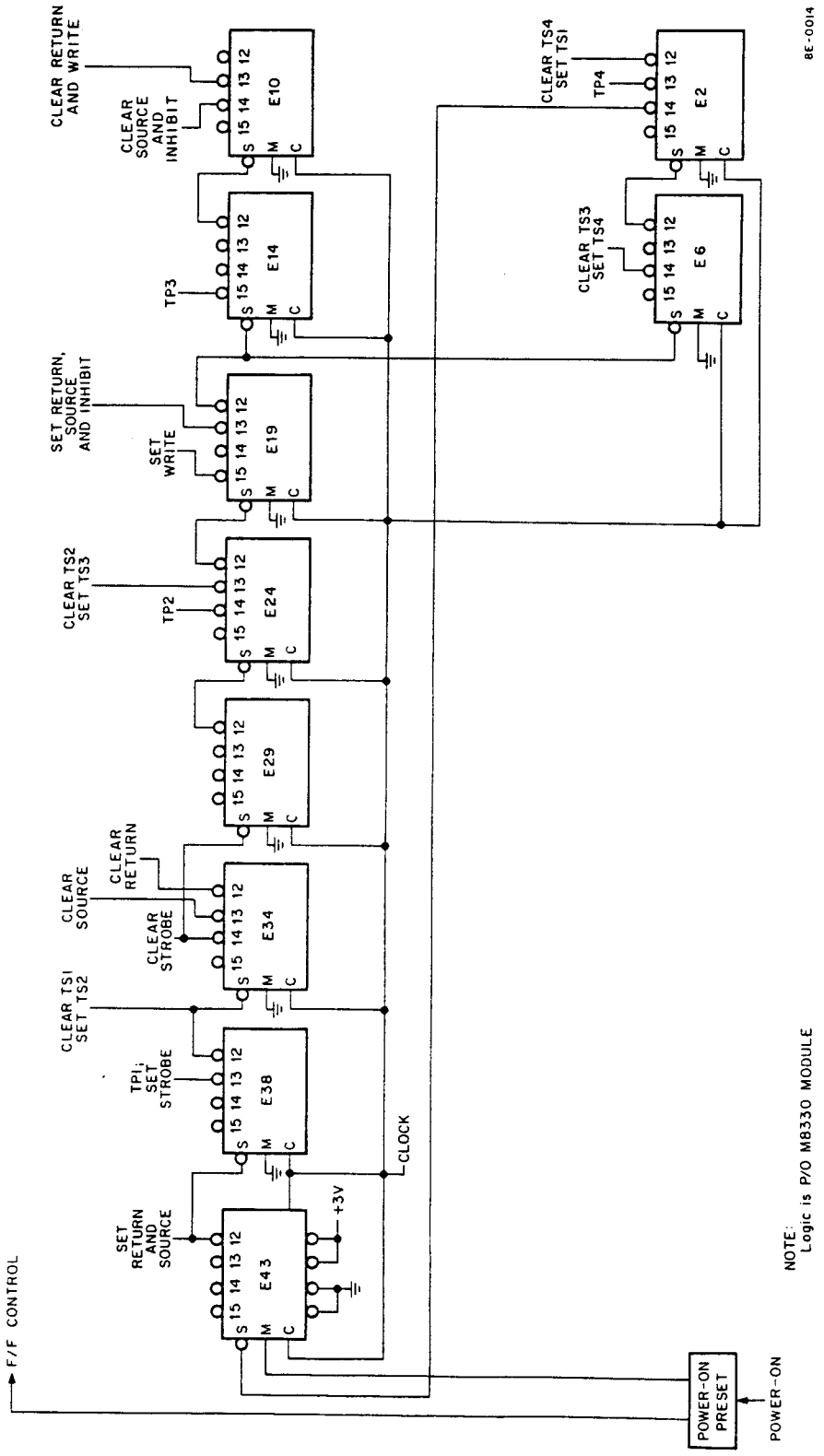


Figure 3-22 Timing Shift Register, Simplified Version

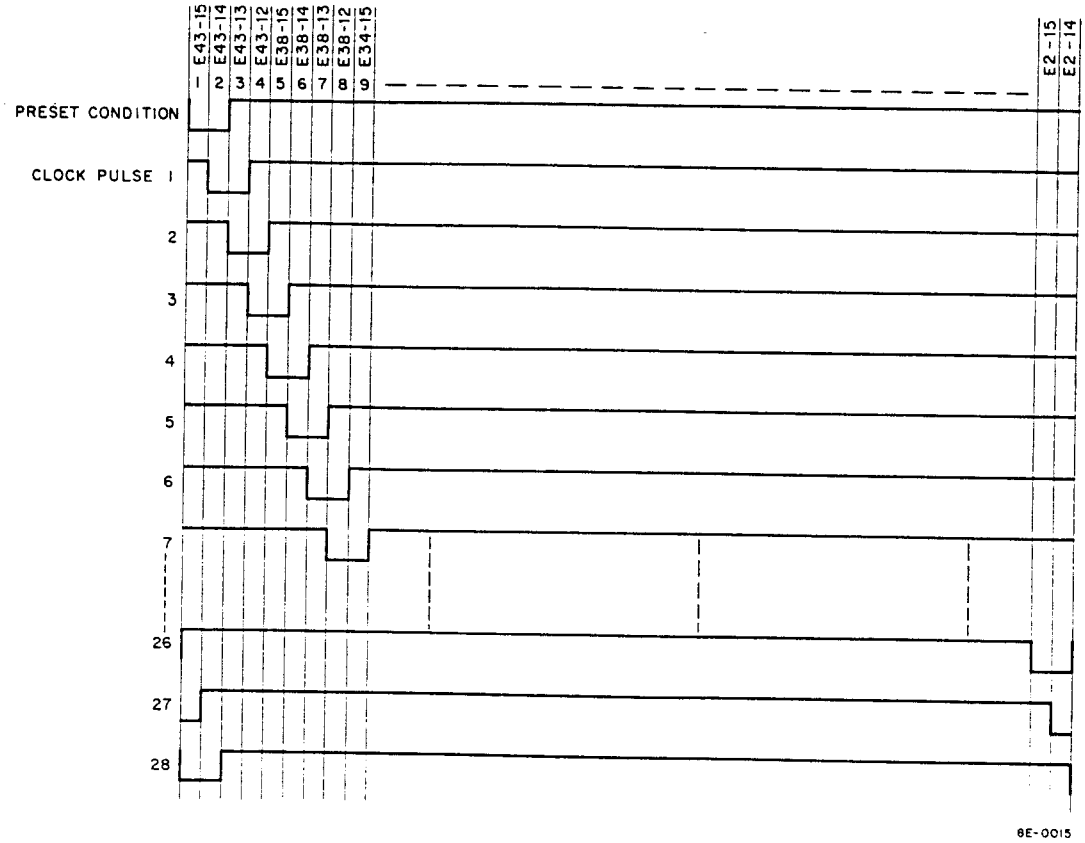


Figure 3-23 Register Composite Logic Signal Timing Diagram

3.16 POWER-ON PRESET CONTROL

The power-on preset control logic is shown in Figure 3-24. Remember that this logic determines the operating mode of IC E43 in the Timing Shift Register. At power-on, the control holds E43 in the parallel-entry mode while all logic 1s are shifted out of the remainder of the register. To carry out this function, the control logic monitors the OMNIBUS POWER OK signal that originates in the power supply (Paragraph 3.47.6).

When power is turned on, POWER OK is negated (grounded). This signal is negated when power supply voltages are below a predetermined level, which is the case at power-on. Power supply voltages do not reach this predetermined level instantaneously at power-on; rather, there is a delay of perhaps hundreds of microseconds before POWER OK is asserted. However, at some time during this delay, the voltages reach a level that is sufficient to start the clock and begin loading and/or shifting the Timing Shift Register. Note that when POWER OK is low, both flip-flop E39B and flip-flop E39A (RUN) are held in the clear state by the asserted POWER PRESET L signal. The 0 output of E39B is high; this signal keeps E43 in the parallel-entry mode. Thus, the conditions for presetting the register are met, viz., E43 is held in the parallel-entry mode, clock pulses shift out the remaining register bits, and the POWER PRESET L signal holds the timing flip-flops in the reset state.

Long after the register has been preset, POWER OK is asserted. After a delay introduced by the delay circuit shown in Figure 3-24, POWER PRESET L is negated (the delay circuit has major significance only at power-off; this is explained shortly). The operator can activate either the DEP, CONT, or EXAM key (Paragraph 3.32.2.1), causing MEM START L to be asserted. This signal sets the RUN flip-flop; the 1 output of the flip-flop causes RUN L to be asserted and provides a high level at the D-input of flip-flop E39B. The next clock pulse sets E39B; the 0-output of the flip-flop places IC E43 in the right-shift mode, and the timing cycle begins.

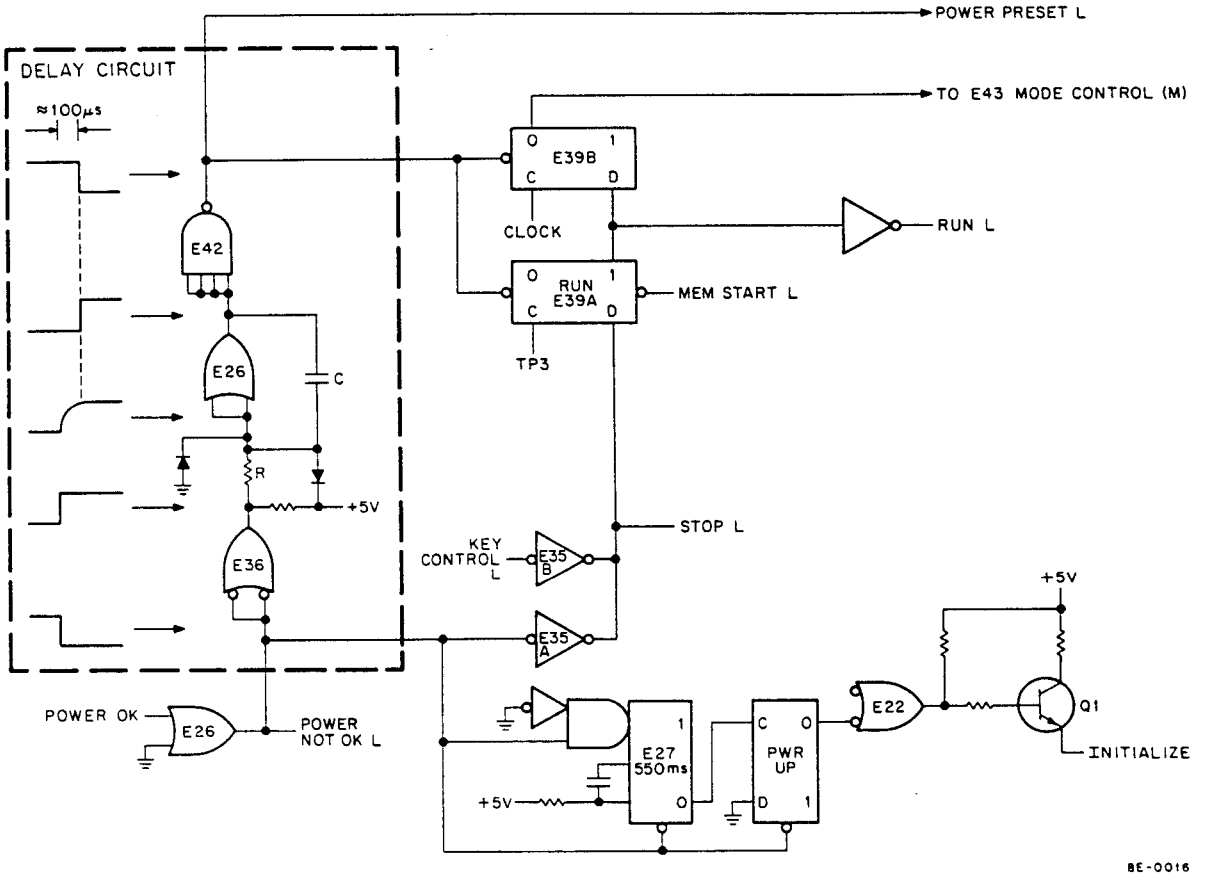


Figure 3-24 Power-On Preset Control Logic

The power-on preset control has an important function at power-off as well. If the operator turns off the power, or a low power supply voltage is detected, POWER OK is negated. To ensure that both processor and memory complete the current timing cycle, the assertion of POWER PRESET L is delayed by approximately 100 μs. This delay is accomplished by the circuit shown within the dashed line; the method is illustrated by the waveforms shown.

When POWER OK is negated, POWER NOT OK L is asserted. The next occurring TP3 pulse resets the RUN flip-flop, thereby negating the RUN L signal and enabling the clock to reset flip-flop E39B. The current timing cycle proceeds to its conclusion and, because IC E43 of the Timing Shift Register is in the parallel-entry mode, the register halts in the preset state. When the POWER PRESET L signal goes low after the delay, it holds E39A, E39B, and the timing flip-flops in the clear state. Timing can be restarted only if the operator activates one of the keys mentioned earlier.

Note that when POWER OK is negated, the STOP L signal is asserted by gate E35A. The STOP L signal can be asserted in a number of other ways as well:

a. A HLT instruction in the program can assert STOP L.

b. The HALT switch or the SING STEP switch on the operator's console can be closed, asserting STOP L.

c. The DEP key, the EXAM key, or the EXTD ADDR LOAD key can be activated, asserting KEY CONTROL L that causes STOP L to be asserted, if the processor is not in a running condition.

That part of the logic in the lower right portion of Figure 3-24 is used to generate the INITIALIZE signal at power-on. At some time before POWER OK goes high, the power supply voltages become sufficiently high for transistor Q1 to conduct, asserting the INITIALIZE signal (note that 1-shot E27 is held in the clear state and the PWR UP flip-flop is held in the set state, both by POWER NOT OK L). When POWER OK goes high, the 1-shot is triggered. 550 ms later, E27 times out; its 0-output clears the PWR UP flip-flop; this causes the INITIALIZE signal to be negated. The long-duration INITIALIZE signal allows all system equipment to complete the operations initiated by the leading edge of the signal.

3.17 SLOW/FAST CONTROL

Figure 3-22 shows only the intermodule connections required for a slow cycle of operation. Other connections, necessary for normal timing operation, are omitted for clarity. The PDP-8/E uses a fast timing cycle (1.2 μs) in normal operation; to produce this fast cycle, five additional connections are necessary (Figure 3-25). The connections are:

a. a connection between E34, pin 14 and E24, pin 3

b. three connections on E24 itself

c. a connection from the slow/fast control to the mode input of E24.

The key to the difference between a fast and slow cycle can be found in IC E24. The mode control signal of E24 is controlled by the 0 side of flip-flop E30. This flip-flop is reset each time either a FETCH state or a non-autoindex DEFER state, both requiring a fast cycle, is entered. Thus, a fast cycle puts E24 in the parallel-entry mode. The outputs of E24 are connected to the parallel-entry inputs; consequently, parallel loading of E24 accomplishes the same result as serial shifting, e.g., four clock pulses shift the signal in E24, pin 15 into E19, pin 15. The difference between fast and slow cycles occurs because of the number of clock pulses needed to shift a signal from E34, pin 14 into E24, pin 15. During a slow cycle, when the parallel-entry inputs of E24 are disabled, five clock pulses shift a signal from E34, pin 14, through E29 and into E24, pin 15. During the fast cycle, however, with the parallel-entry at E24, pin 3 enabled, E29 is bypassed and only one clock pulse is needed to shift the signal from E34, pin 14 into E24, pin 15. TP2 and all subsequent timing signals are generated four clock pulses earlier than during the slow cycle. Therefore, the fast cycle shortens both the memory and processor timing cycles by 200 ns.

NOTE

E30 can be held in the set state by connecting jumper W1 from the "dc set" input to ground. The SLOW CYCLE ONLY feature facilitates troubleshooting by keeping the timing cycle at a constant 1.4 μs.

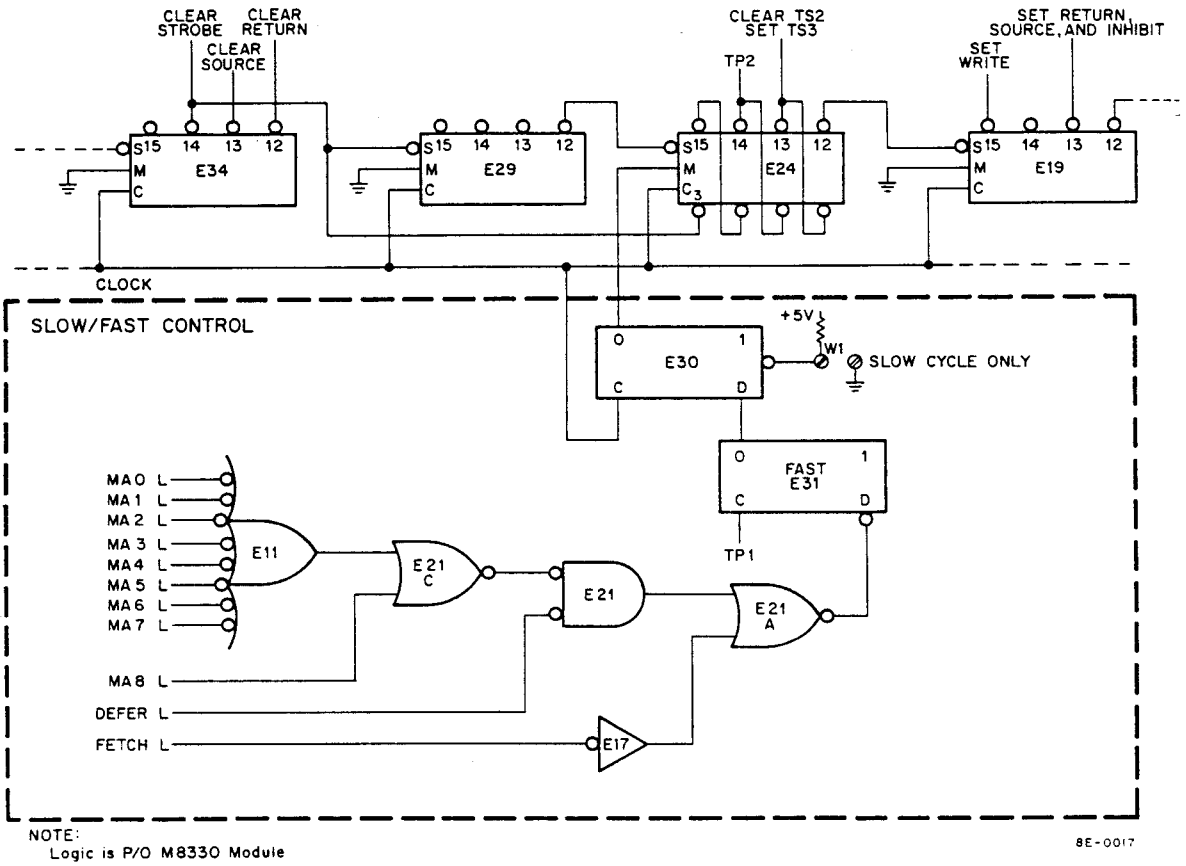


Figure 3-25 Slow/Fast Control Logic

3.18 TIMING DIAGRAM

Timing diagrams of the two cycles of operation are shown in Figure 3-26. The slow cycle is taken as the base and is shown for one timing cycle with TS1 as the initial signal. Processor time states (TS1, etc.) are entered successively, and the timing pulses (TP1, etc.) bracket the trailing edges of their corresponding time state signals.

Note that the time duration of each timing signal, except TS2, remains constant whether the cycle is slow or fast. The 200 ns difference between the slow and fast cycle is accomplished by varying the time duration of TS2 alone and, thus, the amount of time between the read and write portions of a memory cycle is variable. The slow cycle is used when data is read from memory, taken to the processor for modification, and returned to memory. If the data is to be read and then rewritten, as in a FETCH cycle, less cycle time is required; thus, the fast cycle is provided.

3.19 PROCESSOR TIMING

Figure 3-27 shows the logic that provides processor timing signals. Time state signals are provided by four R/S flip-flops; each flip-flop consists of two cross-coupled NOR gates and is controlled by selected pins of the Timing Shift Register. Timing pulse signals are provided by four NOR gates connected to the register. The POWER PRESET L signal from the power-on preset controls the flip-flops at both power-on and power-off (or at some condition of low power supply voltage). The signal clears the TS2, TS3, and TS4 flip-flops and sets the TS1 flip-flop. Thus, the processor is clamped in TS1 if a timing cycle is not in progress.

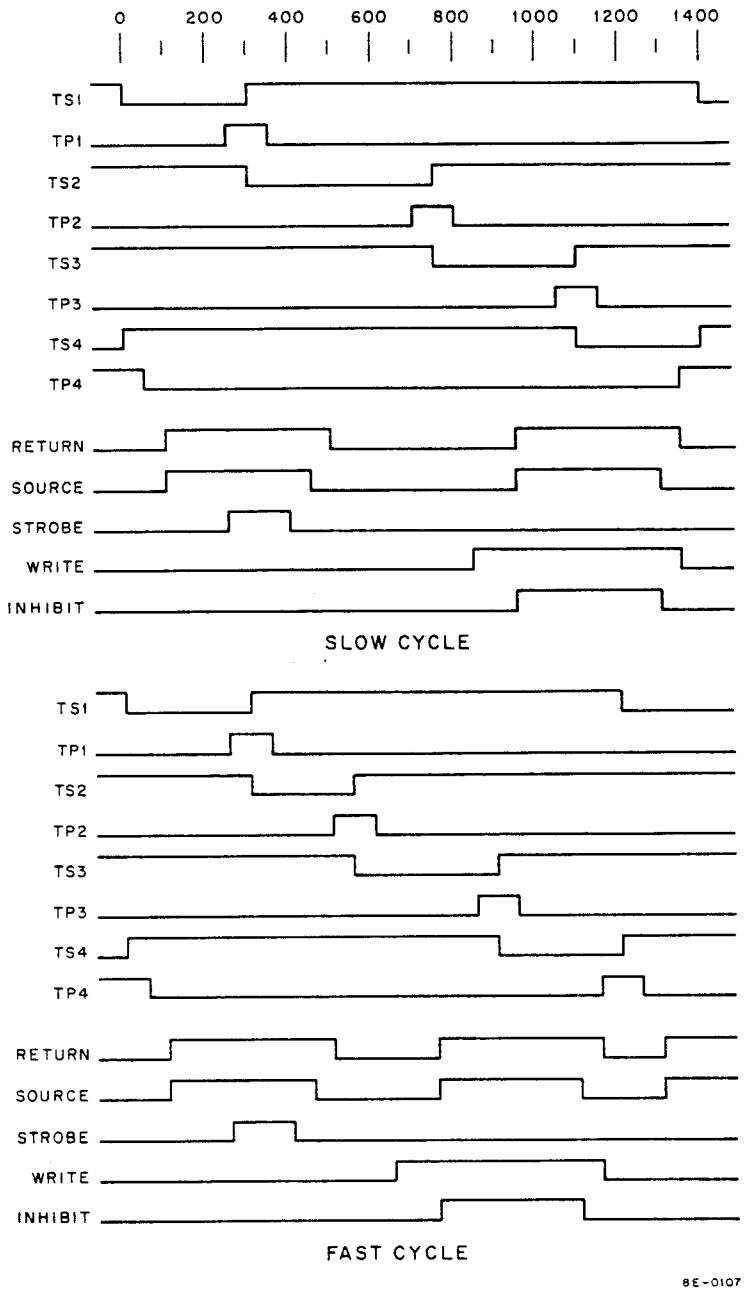


Figure 3-26 Memory and Processor Signals, Timing Diagram

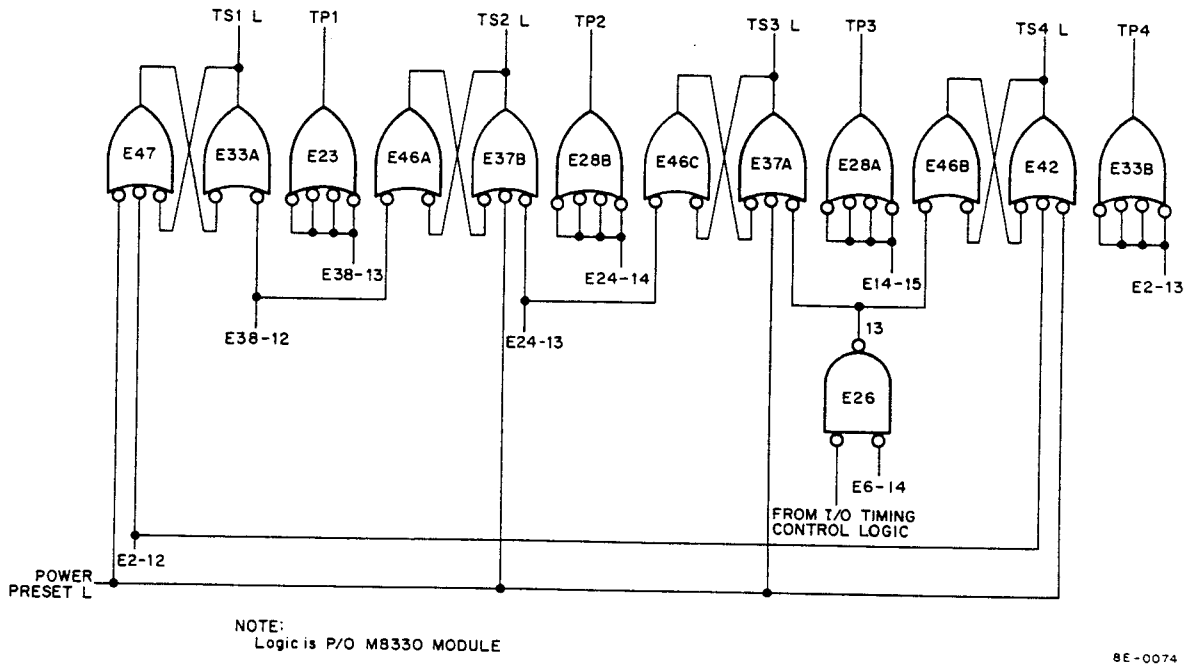


Figure 3-27 Processor Timing Signal Logic

The processor timing signals are used primarily in the CPU, where they generate signals for major register gating and control. Timing pulses have two major functions within the CPU: to sample processor control lines, and to generate "load" signals for the major registers. The time state signals generally provide enabling levels, during which major register outputs are processed.

3.20 MEMORY TIMING

Figure 3-28 shows the logic that provides the memory timing signals. Each signal is generated by an R/S flip-flop of two cross-coupled NOR gates and is controlled by the indicated shift register output pins. The POWER PRESET L signal resets all flip-flops at power-on and power-off.

These timing signals are used in the memory to control the read and write portions of the timing cycle. RETURN and SOURCE are generated during both halves of the cycle, thereby turning on memory current. The conjunction of these two signals determines the width of the current pulse. Note on the timing diagram that return and source are asserted at the same time, but that return is negated 50 ns later than source; this ensures that the memory stack does not remain capacitively charged. STROBE is generated only during the read half of the memory cycle and is used to provide a time reference from which the outputs of the sense amplifiers are sampled. WRITE and INHIBIT are generated only during the write half of the memory cycle. WRITE enables the proper Read/Write switches, thereby providing write currents to the memory stack. INHIBIT is asserted 100 ns later than WRITE and gates the Inhibit Drivers associated with memory control. Details regarding the function of these signals are presented in Section 4, Memory System.

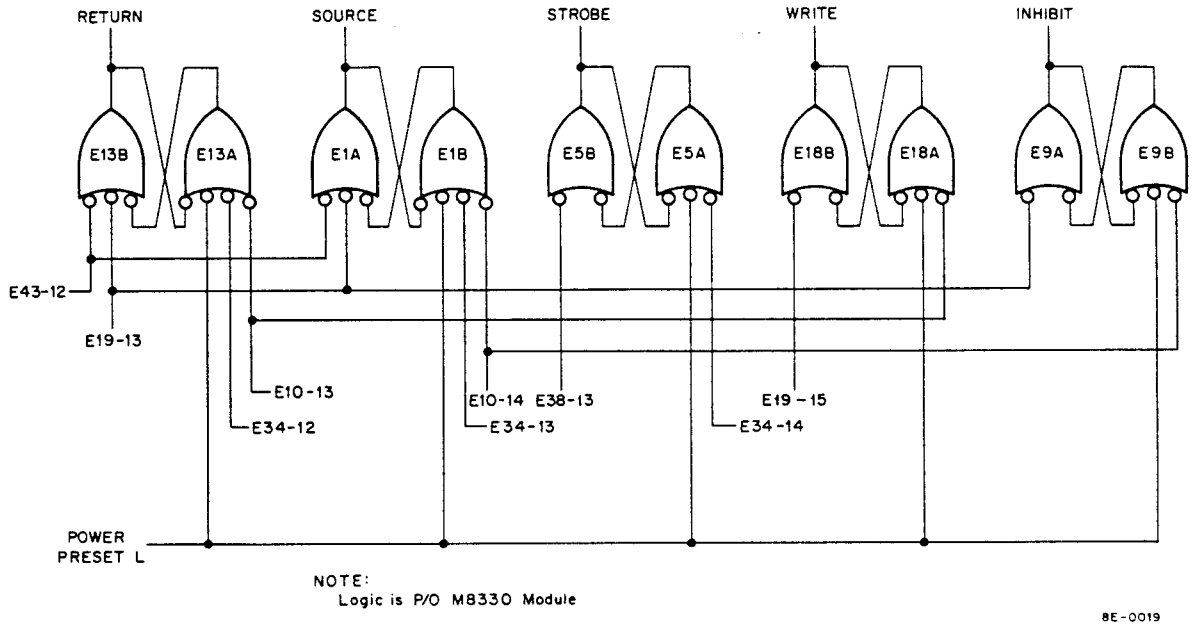


Figure 3-28 Memory Timing Signal Logic

3.21 I/O TIMING CONTROL

The connection between the I/O Timing Control and the mode input of IC E6, omitted from Figure 3-22, is illustrated in Figure 3-29. This control network is used when a peripheral is making more than one I/O transfer during a single IOT instruction and when, because of gating delays, the peripheral needs more time for a transfer than is allowed with normal timing. In either case, the peripheral takes the NOT LAST TRANSFER line to ground, and at the next TP3 time the timing cycle is interrupted and stalled in TS3. The peripheral transfers the information, issuing a BUS STROBE L signal with each transfer. Transfers continue until the peripheral negates the NOT LAST TRANSFER L signal, signifying that the next BUS STROBE L issued by the peripheral is the last of the I/O transfer. This last BUS STROBE L signal restarts the timing cycle, allowing TS3 to end and TS4 to begin.

The last five shift register ICs of the chain are shown in Figure 3-29. Note that all but E6 are programmed for serial shifting. The mode input of E6 is controlled by flip-flop E20B, which is, in turn, controlled by flip-flop E20A. This mode input is normally at a ground level, and the timing signals are generated in the normal way, i.e., the 100 ns negative pulse is shifted from E19 through E14 and E6 to E10 and E2, respectively (Figure 3-23). Note that when E6, pin 14 goes low NAND gate E26 is enabled, provided flip-flop E20A is set; the TS3 L signal is negated, and TS4 is entered.

However, if the peripheral has caused the NOT LAST TRANSFER L signal to be asserted, E20A is cleared at TP3 time, and NAND gate E26 cannot be enabled (the timing diagram in Figure 3-30 visualizes the process). This action prevents both the TS3 L signal from being negated and the TS4 L signal from being asserted. In order to complete the interruption of the timing cycle, the shifting process must be halted. This is done at the next clock pulse time, when flip-flop E20B is cleared. The 0 output of the flip-flop places E6 in the parallel-entry mode. The 100 ns negative pulse is stalled in E6, pins 15 and 14 staying low until the I/O transfer has ended (the state of the parallel-entry inputs of E6 ensures that the state of the outputs remains constant). Note that IC E14 is allowed to continue shifting the negative pulse down the line. This path of the shift register deals with the write half of the memory timing signals. Because I/O transfer data is not transferred directly to memory, the memory timing signals need not be altered in any way.

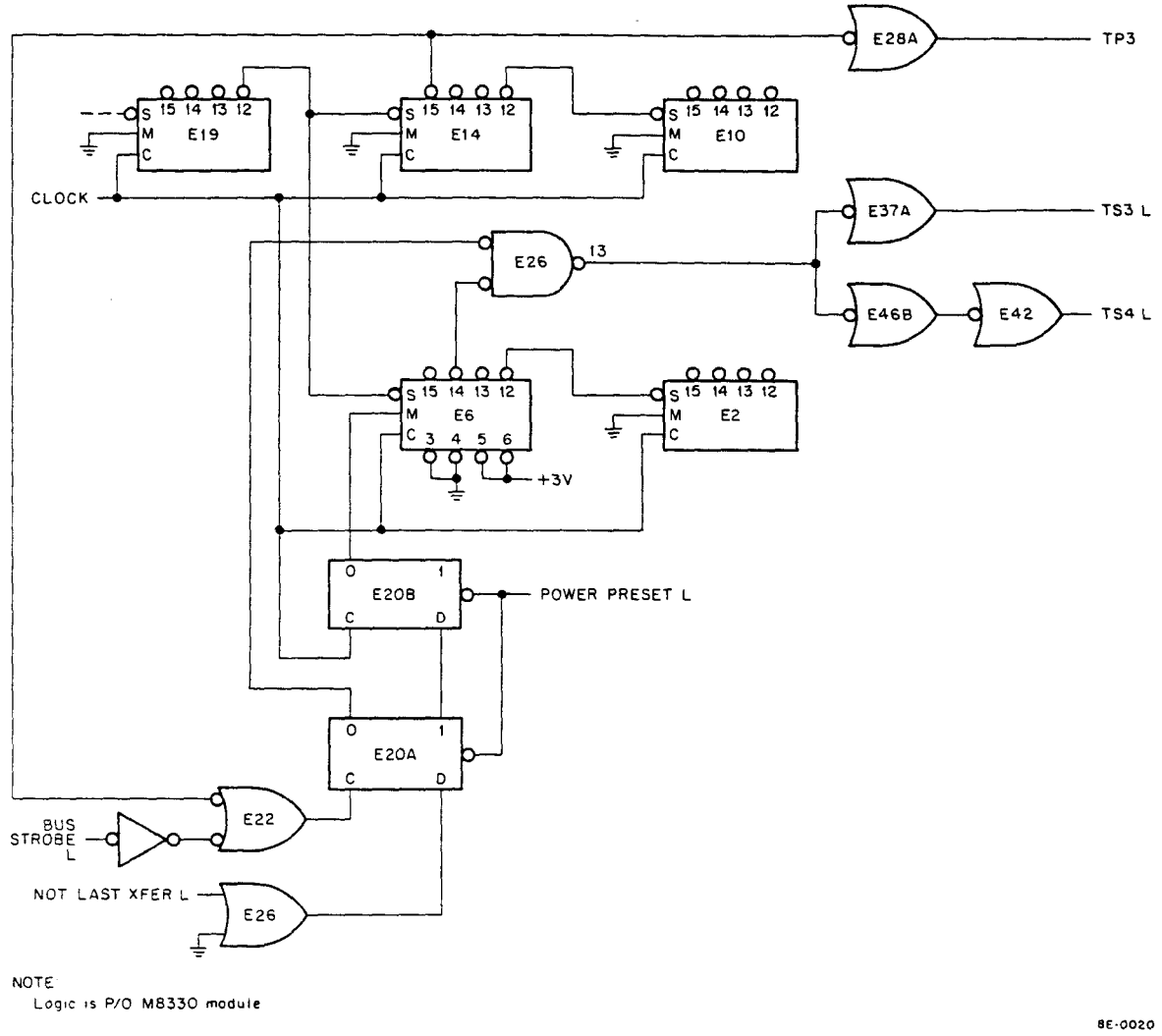


Figure 3-29 I/O Timing Control Logic

When the I/O transfer is complete, the NOT LAST TRANSFER L signal is negated and the peripheral generates a BUS STROBE L signal that sets E20A. NAND gate E26 is enabled, causing the TS3 L signal to be negated and the TS4 L signal to be asserted. The first clock pulse to occur after E20A is set, sets E20B, and E6 is returned to the right-shift mode. The next clock pulse begins shifting the negative pulse through E6 and the timing returns to normal.

Figure 3-30 illustrates an I/O timing interrupt. The cycle time is arbitrarily shown as 1550 ns. Note that the timing, before interruption, is that of a fast cycle. This is always true, because I/O transfers are accomplished while the processor is in the FETCH state, which uses a fast timing cycle.

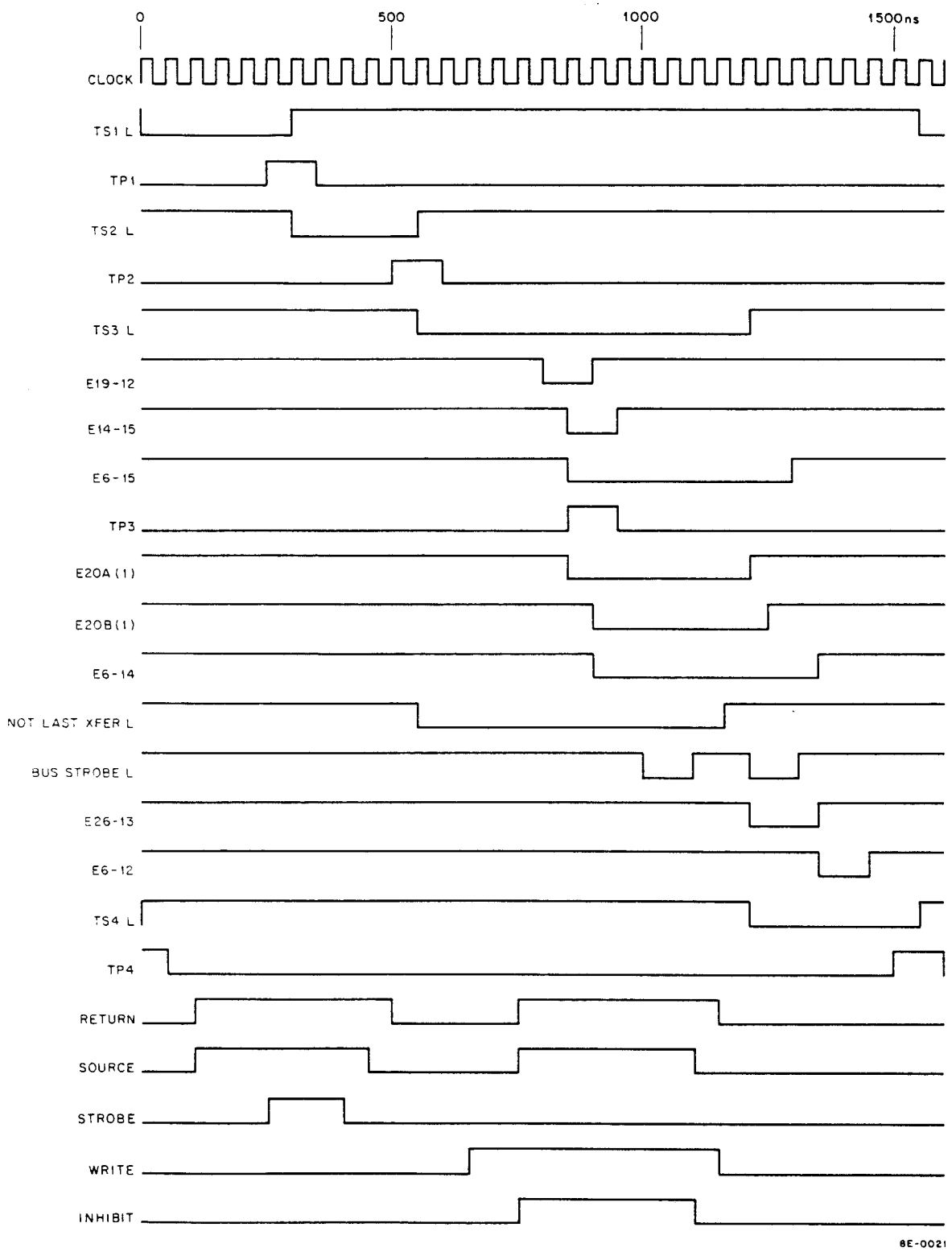


Figure 3-30 Memory and Processor Timing I/O Interrupt

3.22 MEMORY SYSTEM, GENERAL DESCRIPTION

The standard PDP-8/E core memory (designated MM8-E) is a random access, coincident-current, magnetic READ/WRITE core memory with cycle times of 1.2 μs and 1.4 μs. The memory comprises ferrite cores wired in a 3-D, 3-wire, planar configuration. The basic unit can store up to 4096 (4K) 12-bit words. The memory can be expanded to 32K words in 4K increments.

3.23 MEMORY SYSTEM, FUNCTIONAL DESCRIPTION

The memory system performs three basic functions for the PDP-8/E processor:

a. It decodes and selects the desired core location in which a 12-bit word is stored or will be stored.

b. It reads a 12-bit word from the selected location.

c. It writes a 12-bit word into the same selected location.

These functions are illustrated in Figures 3-31 and 3-32, for which one memory cycle is represented. The processor must first supply the address (refer to Chapter 4, Section 1, Memory Addressing, of the *PDP-8/E & PDP-8/M Small Computer Handbook)* before a read or write operation can be considered. The CPMA Register (Paragraph 3.34) is loaded at TP4; the content of the CPMA is placed on the MA lines. Memory address decoders receive the MA bits and turn the corresponding Read current switch on when control signals RETURN, SOURCE, and WRITE L (not) are present. The Memory Register is cleared when RETURN and NOT WRITE L become active (WRITE L is high and RETURN is high).

The outputs from the 12 selected cores are fed to their respective sense amplifiers. A strobe signal is used to gate the Sense Amplifier into the local Memory Register. If MD DIR L is low (as it always is during the READ portion of the memory cycle), the output of the Memory Register is placed on the MD lines. During the WRITE portion of the memory cycle, the memory selection system uses the same address inputs and control signals; however, control signal WRITE L will change states, causing the write current switches to be activated. To write the content of the Memory Register back into core, MD DIR L will be low (active). Otherwise, the content of the MB Register will be placed on the MD lines, and the word in the MB Register will be written into core. The INHIBIT L signal controls the gating circuits, and only when INHIBIT L is active will the Inhibit Drivers be activated. A 0 received from the MD lines and INHIBIT L causes the corresponding Inhibit Driver to produce inhibit current.

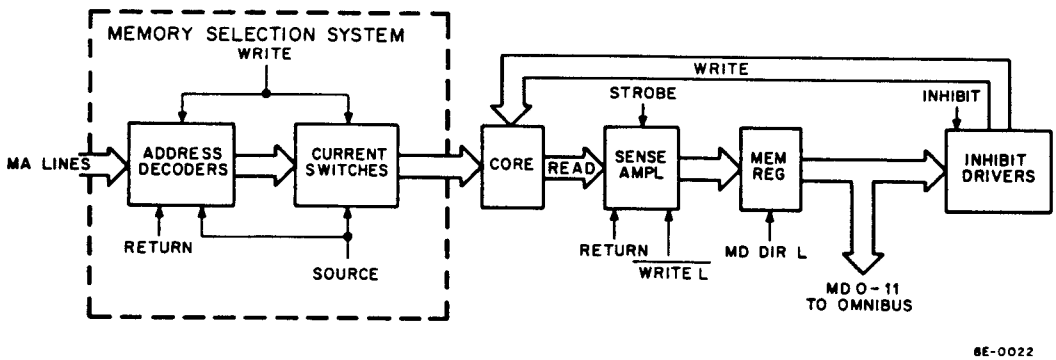


Figure 3-31 Memory System Functional Flow Diagram

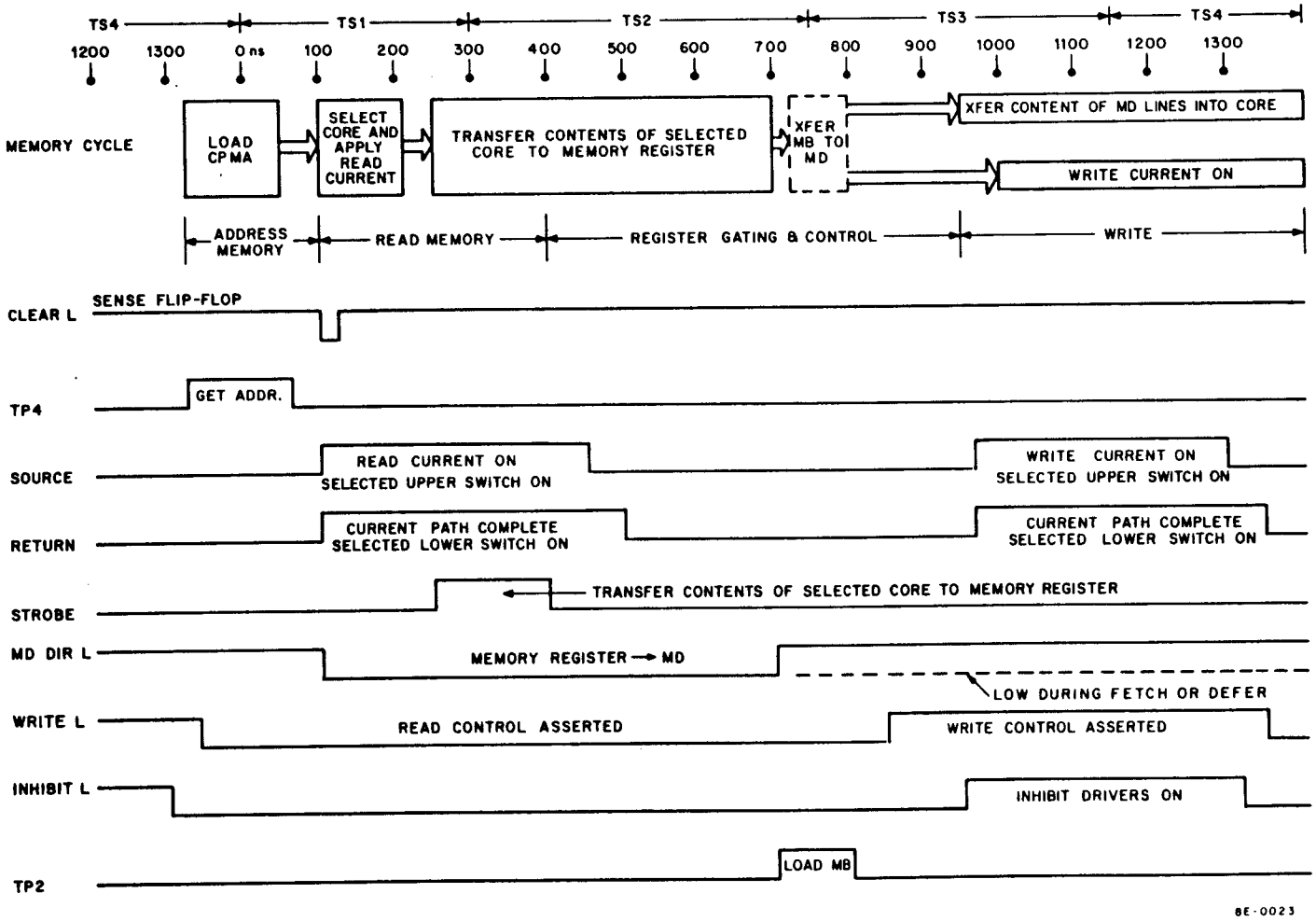


Figure 3-32 Memory Cycle Timing

3.24 MEMORY SYSTEM, DETAILED THEORY

The organization of the memory system is illustrated in Figure 3-33. Three quad-size boards are used to contain the memory system as follows:

a. G104 Sense/Inhibit contains 12 Sense Amplifiers, Memory Registers, and Inhibit Drivers with the corresponding control logic, slice control, -6V supply and current control;

b. G619 Memory Stack contains 12 mats of 4096 cores per mat, and X/Y diode selection matrix;

c. X/Y Driver and Current Source contains address decoding and selection switches, X-current source, Y-current source, and stack discharge switch-power ON/OFF protection circuit.

The detailed theory of core memory, memory selection system, and the memory sense/inhibit function is described in the following paragraphs.

3.25 CORE MEMORY

The basic storage element in the MM8-E Memory System is a small toroidal (ring-shaped) piece of magnetic material, called a magnetic core. A single core, mounted on a ground plane, is illustrated in Figure 3-34. Three wires pass through each core to accommodate the X- and Y-selection and the sense/inhibit function. A primary difference between the PDP-8/E and its predecessors is the combination of the SENSE line with the INHIBIT line to form a three-wire system instead of a four-wire system.

3.25.1 Hysteresis Loop

The characteristics of the magnetic core can be shown by a graph, plotting the current (the magnetizing force) versus flux-density (the resulting magnetism) hysteresis loop as illustrated in Figure 3-35. This hysteresis loop illustrates the magnetizing current, I, produced by the current contained in the three wires plotted along the horizontal axis, and the resulting flux density, B, through the core along the vertical axis. Two directions of current are shown. READ current, with respect to the graph, is directed from right to left. If a logic 1 is stored in the core, B will move from the remanent point ($+B_r$) down to saturation at $-B_m$ when the READ current is turned on. When the magnetizing current is removed, the flux density settles down to the remanent point at $-B_r$. WRITE current is directed from left to right with respect to the graph. If a 1 is to be written into core, the flux density will move the point $-B_r$ to point $+B_m$ on the graph and then settle down to $+B_r$ when the magnetizing current is removed. Thus, points $-B_m$ and $+B_m$ are the extreme saturation points, and points $-B_r$ and $+B_r$ are the extreme points in the normal logic states.

3.25.2 X/Y Select Lines

Core saturation occurs only when both the X- and Y-select lines each contain half the amount of current required to reach saturation. This is called the coincident current technique and results in a fully selected core. If either X- or Y-line contains no current, there is no significant change in flux density. For example, for a READ, if the core is in logic 1 state, the flux change is from point $+B_r$ to H on the graph and then reverts back to point $+B_r$. For a WRITE, the flux change is from point $-B_r$ to point J and then reverts back to $-B_r$.

3.25.3 READ Operation

READ occurs during the first half of the memory cycle. Its function is to sample either a logic 1 or logic 0 in a fully selected core. Thus, both the X- and Y-Read half-select currents must be applied for the Sense/Inhibit line to receive a pulse resulting from a change in flux density if the core is in the logic 1 state. If the core is in the logic 0 state, no change in flux density occurs and, therefore, no pulse appears on the Sense/Inhibit line.

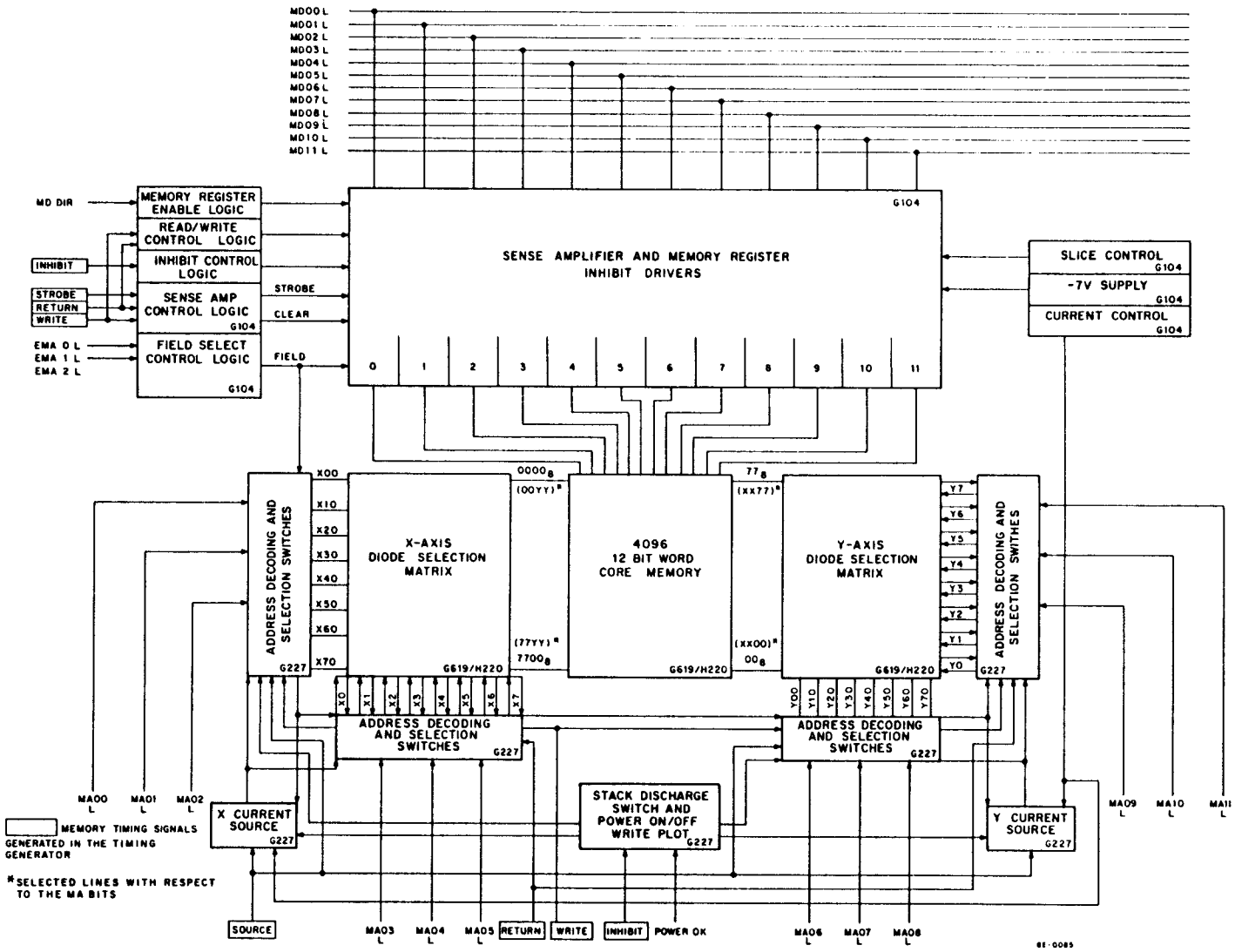


Figure 3-33 Memory System Block Diagram

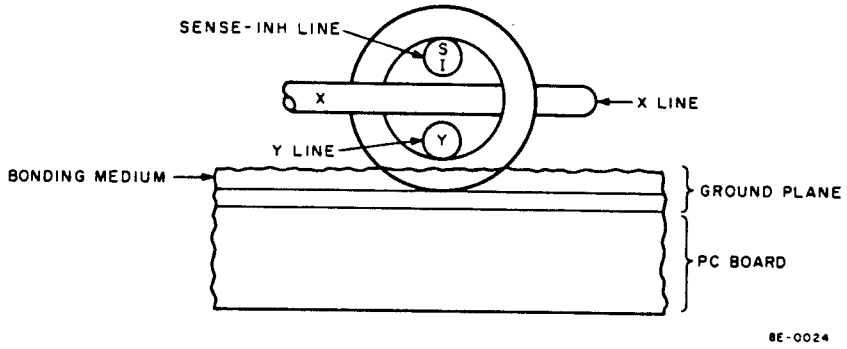


Figure 3-34 Magnetic Core

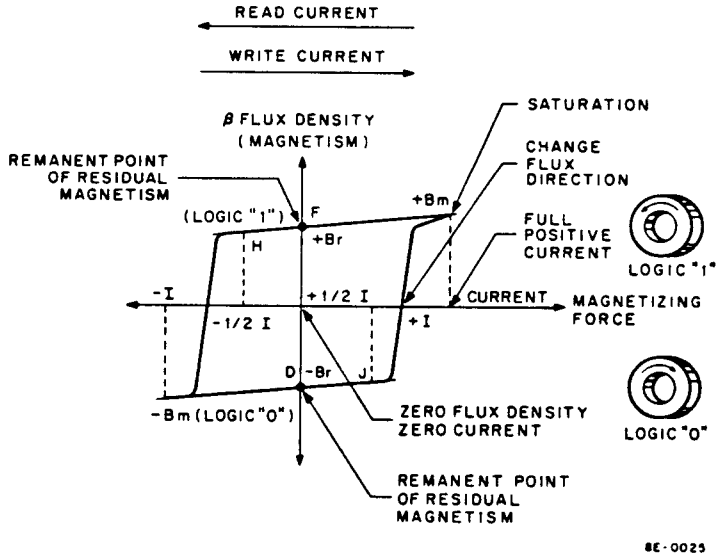


Figure 3-35 Magnetic Core Hysteresis Loop

3.25.4 WRITE Operation

WRITE occurs during the second half of the memory cycle. Because WRITE follows READ, the cores at the selected address have been cleared to a logic 0 state. If the fully selected core (X- and Y-currents) is not inhibited, the magnetic flux moves from point $-B_r$ to $+B_r$ on the graph, and a 1 is stored in core. However, to store a 0 in core, it is necessary to cause a less than fully selected condition. This can be achieved by generating an inhibit current and applying this current to the Sense/Inhibit line. If this inhibit current is in the opposite direction to the X- and Y-current, the net result of the change in flux will be from point $-B_r$ to point J on the graph. When all currents are removed, the flux density reverts back to $-B_r$ on the graph.

3.25.5 Magnetic Core In Two-Dimensional Array

A partial three-wire memory configuration is illustrated in Figure 3-36. Half-select currents are produced for one X-line and one Y-line. If, for example, the core at X3, Y2 is selected, the corresponding wires going through each row would contain half-select current. For the X3 row, X3, Y1 core would contain only half-select current, and X3, Y2 core would contain full-select current. All other cores in row Y2 would contain half-select current. The Sense/Inhibit line terminates at the Sense Amplifier and the Inhibit Driver in the manner shown in Figure 3-36. There are two termination points on the Sense Amplifier side, and one termination point at the Inhibit Drivers.

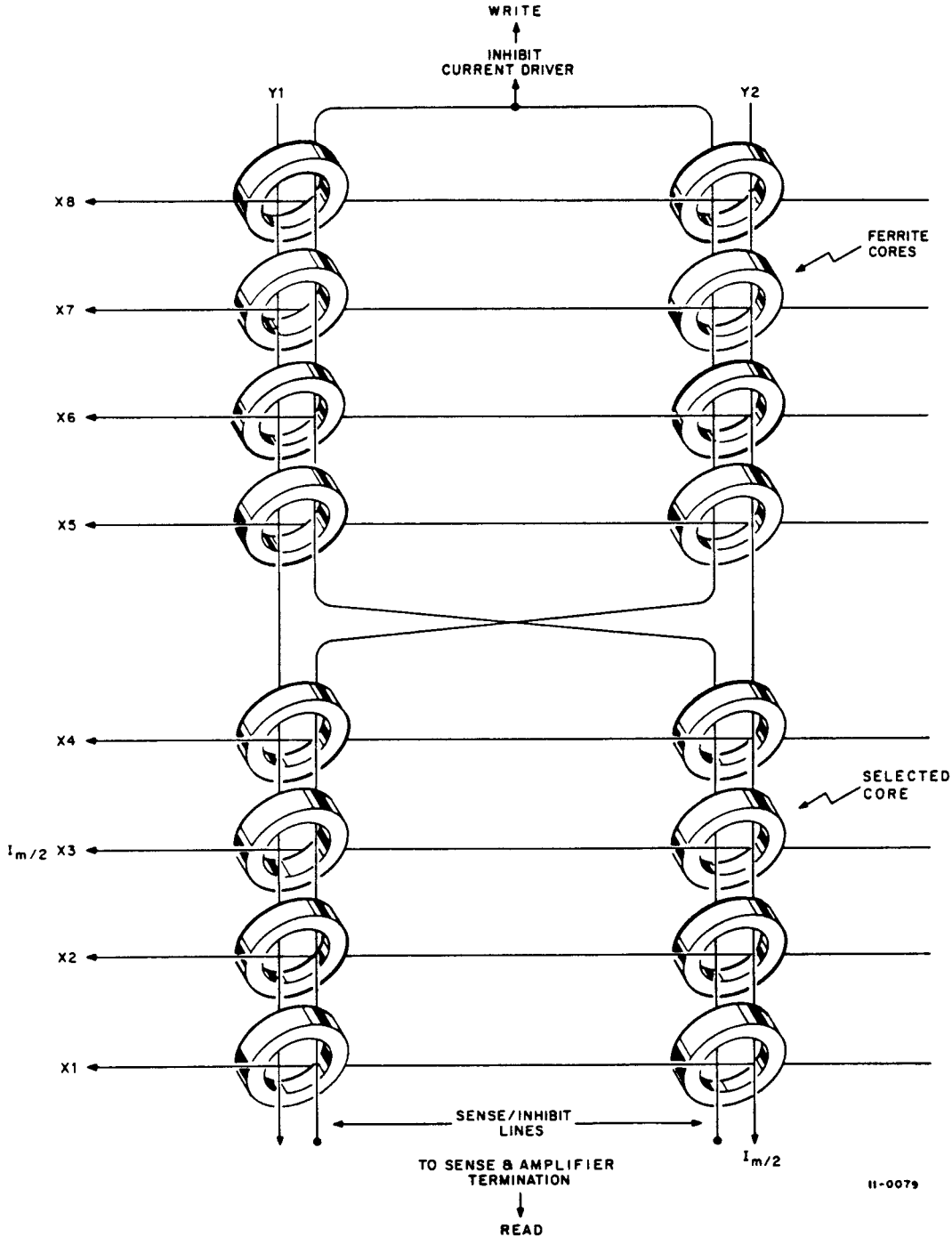


Figure 3-36 Three-Wire Memory Configuration

The third wire (the Sense/Inhibit line) receives the resulting signal at the coincident-current points during READ. Current direction is from the top of the illustration down to the Sense Amplifier. For WRITE, current direction is from the bottom of the illustration to the top to the Inhibit Current Driver. This direction opposes the current in the Y-selection line and, therefore, causes a half-select condition. This half-select procedure is only required where a 0 is to be written into core.

3.25.6 Assembly of 12-Stacked Core Mats

The MM8-E Memory is a 64 X 64 configuration (64 X-rows and 64 Y-rows). This configuration provides 4096 cores per mat, for which one core can be selected during any one memory cycle and, therefore, one bit of information per mat.

The MM8-E is a 12-bit word memory system; thus, 12 mats are used. Each mat stores one unique bit of information, which is deposited and sensed by one unique line called the Sense/Inhibit line. Thus, 12 Sense/Inhibit lines are used to deposit and sense 12 unique bits of information. The arrangement of the selection lines is quite different. All 12 mats contain 64 X-lines and 64 Y-lines. The threading of each of the X- and Y-lines continues from one mat to the next through all 12 mats. For example, row X31 of mat 0 is common to row X31 of mat 1, which is common to all subsequent mats at row X31. The common factor to each mat is the selection line that is threaded through 12 X 64 cores or 768 cores. The intersection of X31 and Y29, therefore, occurs 12 times in the 12 mats. Because each mat contains a unique Sense/Inhibit line, 12 unique bits of information can be stored to form a 12-bit word.

3.25.7 Physical Orientation of Core Memory

The memory stack layout is illustrated in Figure 3-37. Figure 3-38 illustrates the X- and Y-windings within the memory stacks.

3.26 CORE SELECTION SYSTEM

Core selection is accomplished by enabling the desired X-line and the desired Y-line and allowing current to pass through the selected lines. To accomplish the selection of the X- and Y-lines, a decoding network that receives the MA bits and decodes for line selection is required. An X- and Y-current source is also required so that each line is half-selected.

A selection system functional block diagram illustrating the parts of the memory system involved in core selection is given in Figure 3-39. The primary components involved are:

a. the memory address decoder, which receives memory address bits and control signals to select (enable) the corresponding switch and driver,

b. a current source to provide the necessary select current,

c. a driver and switch to apply current to the selected row and forward-bias the selection diode,

d. one read or write diode, which becomes forward-biased by the driver and switch while all other diodes are back-biased,

e. one selected row containing 768 cores.

The driver and switch shown in Figure 3-39 are one of 16 drivers and one of 16 switches. A WRITE operation for row X13 is illustrated to show the current path.

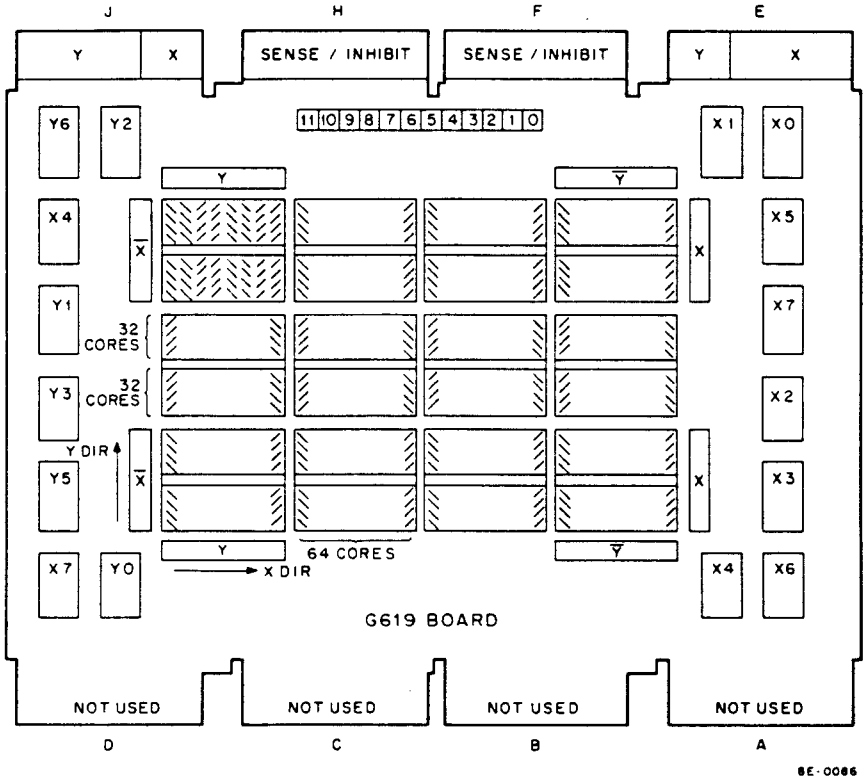


Figure 3-37 Memory Stack Layout (Core Orientation)

Both the READ and WRITE current paths are illustrated in Figure 3-40. Although not all of the circuitry is shown, the current path relationship between a READ and WRITE operation (Figures 3-40a and 3-40b) illustrates how the direction of current for WRITE is opposite to the direction for READ. The illustration also shows how the unselected components are interconnected but passive.

NOTE

Electron current flow is presented in this manual. The reader should consider current originating at a more negative voltage level and taking the path to a more positive voltage level. A forward-biased diode results when the current takes the direction opposite to the diode arrow.

3.26.1 Organization of X/Y Drivers and Current Source

Figure 3-41 illustrates the organization of the X/Y drivers and current source, and the primary signals required to make line selection and current switching possible. Eight decoders are used to select one of 64 X-lines and one of 64 Y-lines as determined by the content of bits MA0 through MA11 L. X-current and Y-current, provided by the X- and Y-current source, are applied to the drivers. The READ signal is applied to both the decoder control gates and the Bias Driver. When a READ operation is to be performed, the selected READ switches and drivers are enabled and the READ/WRITE current switch changes its output signal from ground to -15V. The negated READ signal acts to enable the WRITE function in a similar manner.

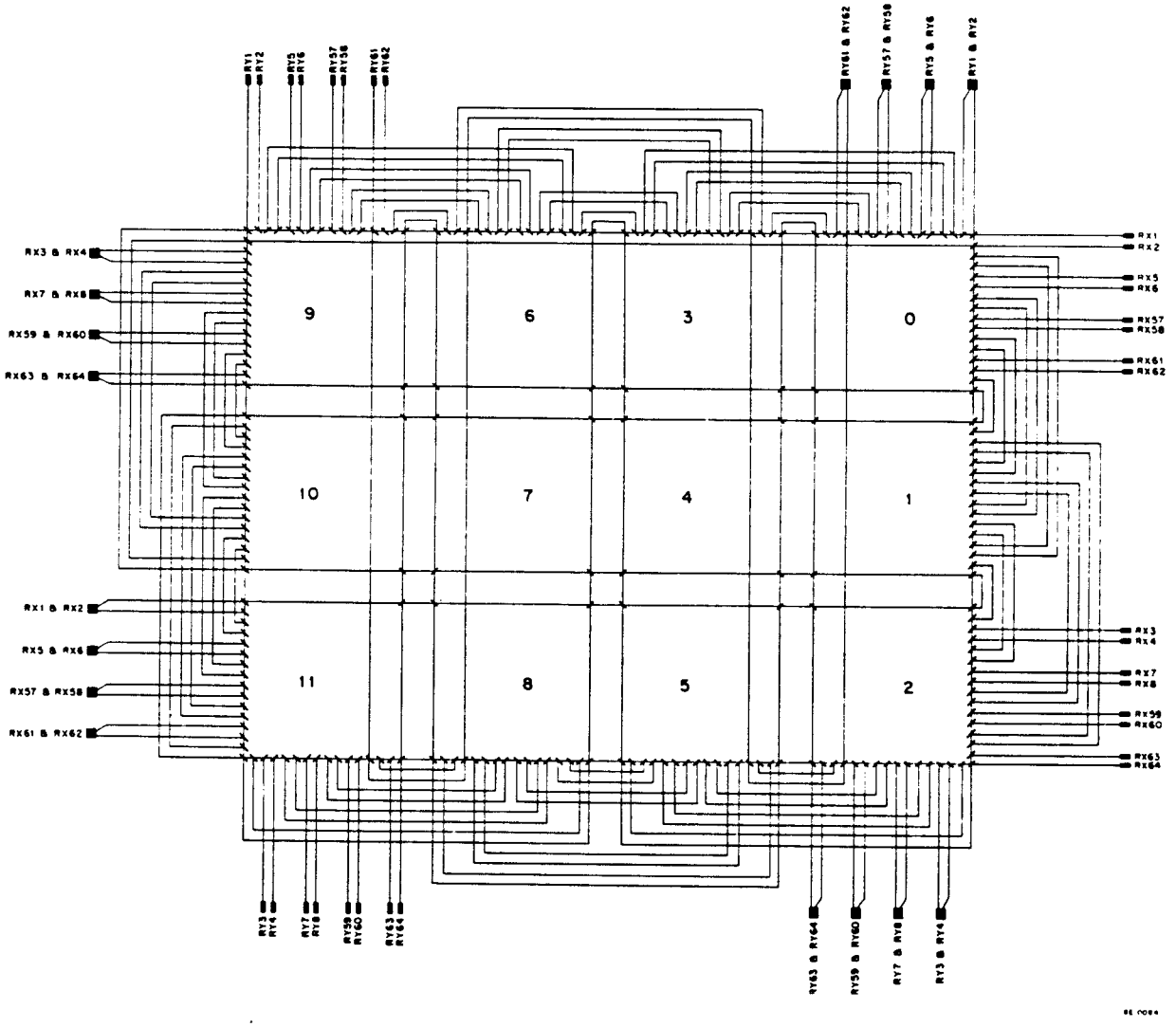


Figure 3-38 Memory Stack X, Y Windings

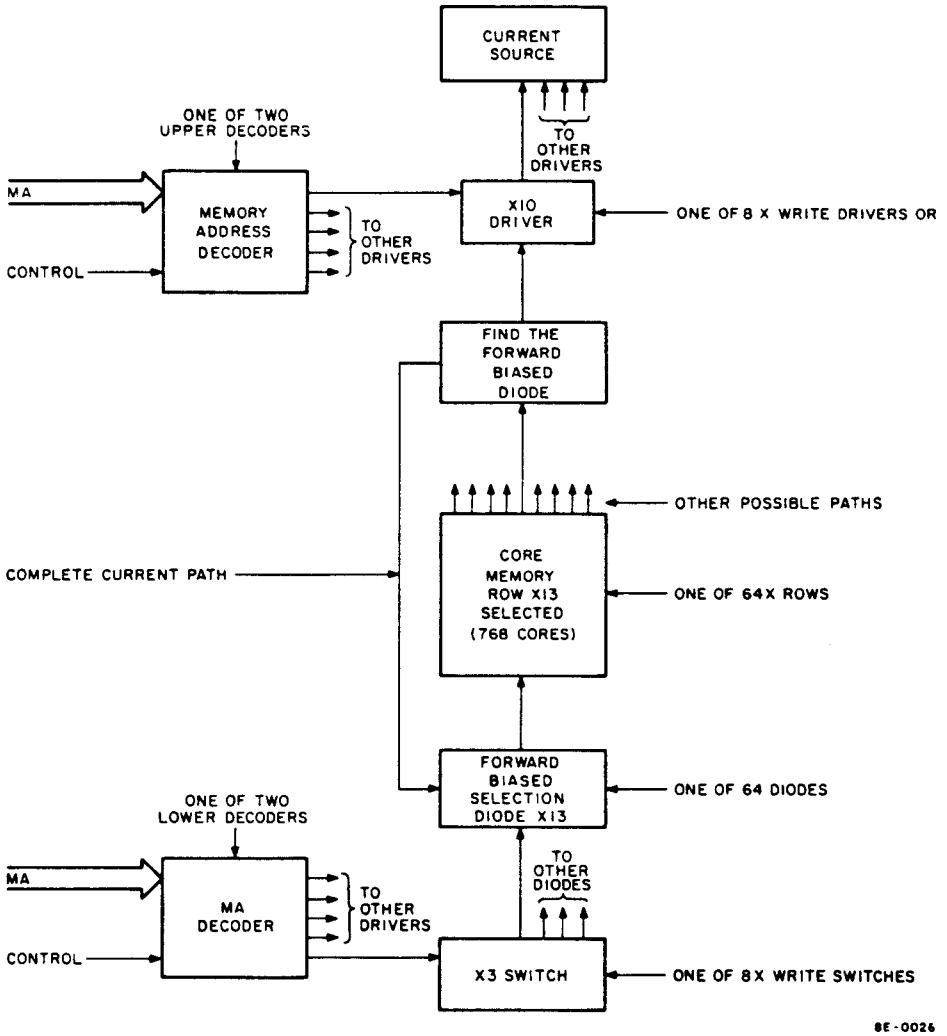
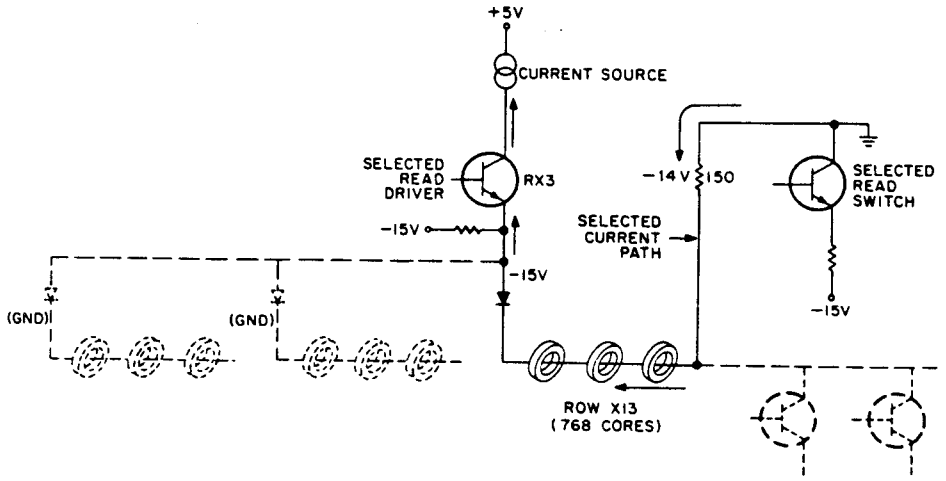
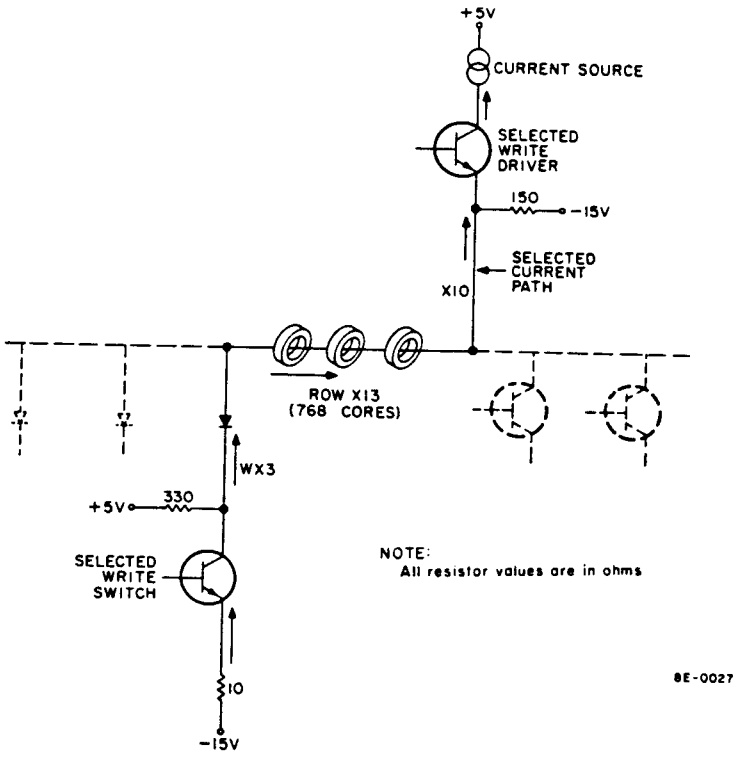


Figure 3-39 Selection System Functional Block Diagram for Write Current of X Rows



a. Current Path for Read Current



b. Current Path for Write Current

Figure 3-40 Read/Write Current Paths

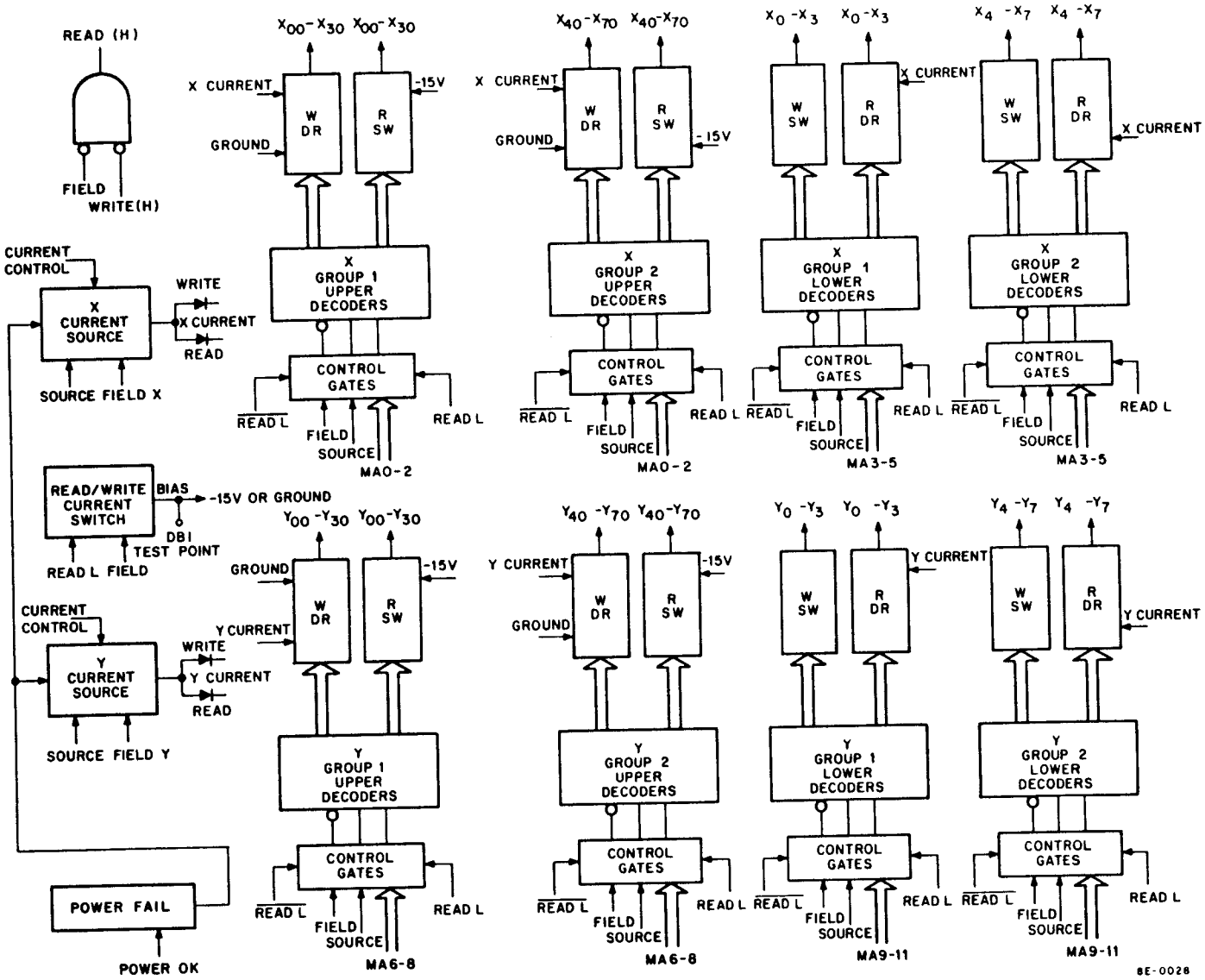


Figure 3-41 X- and Y-Drivers and Current Source
(Block Diagram Representation of G227 Circuit Schematic)

3.26.2 X- and Y-Current Sources

The X- and Y-current sources supply constant current to the READ and WRITE drivers (Figures 3-42 and 3-43). The READ and WRITE drivers receive bias voltage from the current control circuit located on the sense/inhibit board and are turned on when both FIELD and SOURCE are active. They have a slow turn-on rate and a fast turn-off characteristic due to the capacitor in the circuitry. A fast turn-off is achieved by the interaction between the capacitor and two transistors. When SOURCE is negated, one of the transistors is turned on, causing the capacitor to discharge, which causes the output transistor to be biased off. The slow turn-on time reduces the coupling effects within the core stack. Furthermore, the slow turn-on time also means that the READ current is completely controlled by the current source. Because the current source is controlled, the position of the sense output voltage relative to the drive currents is constant.

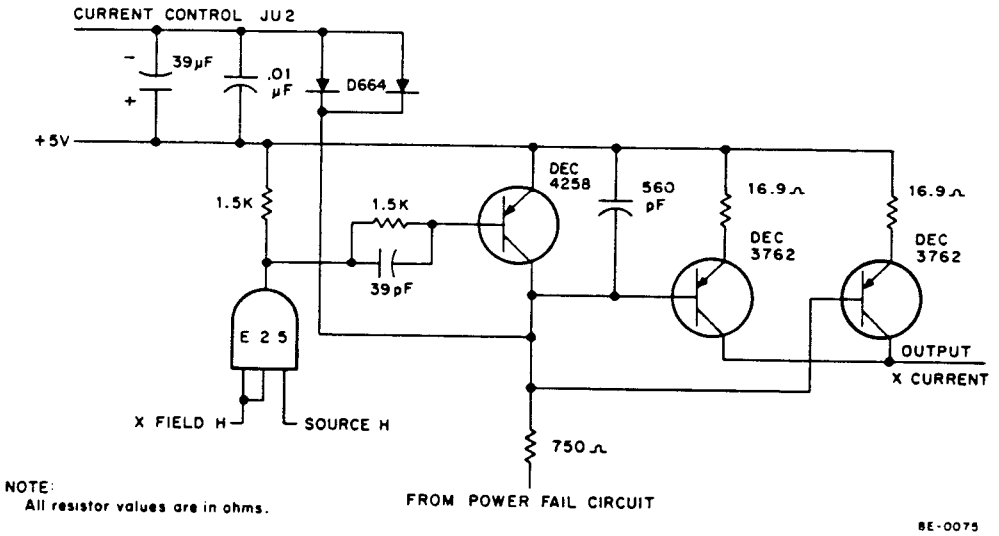


Figure 3-42 X-Current Source

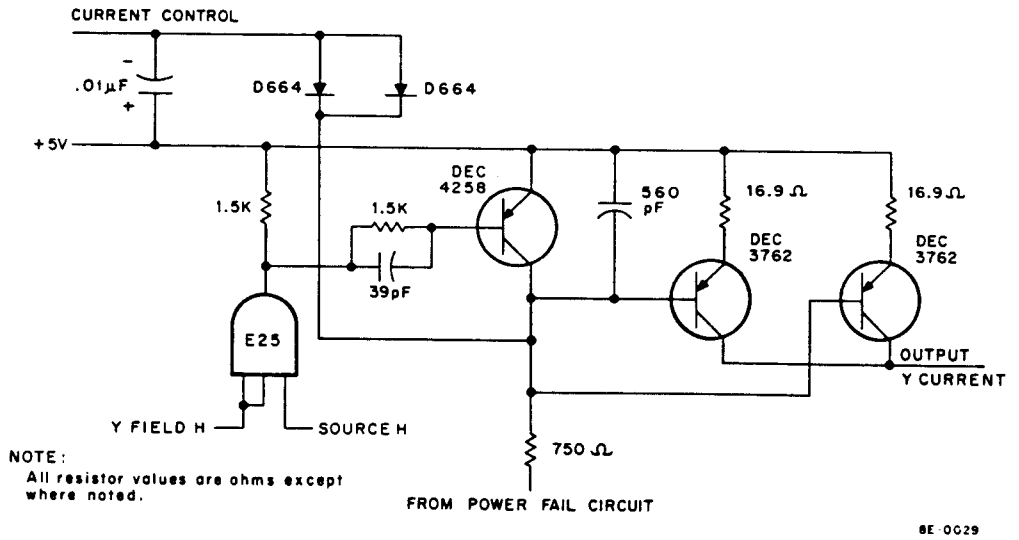


Figure 3-43 Y-Current Source

3.26.3 Bias Driver

The Bias Driver (Figure 3-44) switches the bias voltage from ground for a READ operation to -15V for a WRITE operation. When control signals READ and X FIELD are both active, level shifting circuits along with an output transistor switch the output to ground. When READ is not asserted, the output switches to -15V. The Bias Driver provides the reverse bias condition on the nonselected diodes in the memory stack. Reverse biasing the diodes reduces capacitance and, therefore, reduces "sneak currents" that might be on the line. Refer to Paragraph 3.26.7 for the organization of the planar stack diode matrix.

3.26.4 Power Fail Circuitry

The power fail circuitry (Figure 3-45) responds to the POWER OK signal from the power supply. Its primary function is to ensure that selected memory locations are not changed due to a power failure. The power supply senses a voltage change when the dc voltage drops and grounds the POWER OK line when the voltage is too low. This shuts off the timing chain but ensures that the memory cycle is completed. The memory power fail circuitry turns off the X- and Y-current source after a delay sufficient to complete the WRITE operation. When the machine is turned on initially and the POWER OK signal is asserted, the current source is activated immediately. Thus, the memory power fail circuit has a characteristic of a fast-on/slow-off switch.

3.26.5 Core Selection Decoders

Eight decoders (IC 8251) (Figure 3-41) are used to decode MA0 L through MA11 L from the Memory Address Register (refer to Appendix A for circuit description of 8251). These bits are combined with READ L, FIELD, SOURCE, and RETURN signals to enable the appropriate switch and driver. Signal READ L is generated when WRITE L is not asserted, or negated READ L results when WRITE L is active. The WRITE L signal is developed in the Timing Generator during the last half of the memory cycle. SOURCE is necessary to turn on the selected driver or switches corresponding to the upper X- and Y-select lines, and RETURN is necessary to turn on the selected drivers or switches corresponding to the lower X- and Y-select lines. Both RETURN and SOURCE are developed in the Timing Generator. RETURN remains on for 50 ns longer than SOURCE so that the lines completely discharge. FIELD is developed in the Sense Inhibit circuitry (Figure 3-47). If Extended Memory has not been addressed, this signal will be active.

3.26.6 Address Decoding Scheme

The block diagram in Figure 3-41 illustrates the method through which the MA bits are decoded; the results enable either a WRITE driver or READ switch and the corresponding driver or switch counterpart required to complete the current path. The decoder is arranged as follows: the upper select line decoders are on the left side and the lower select line decoders are on the right side of the illustration. The upper X-select line decoders decode bits MA0–2 L, while the lower X-select line decoders decode bits MA3–5 L. The upper Y-select line decoders decode bits MA6–8 L, while the lower Y-select line decoders decode bits MA9–11 L. There are a total of eight upper X-select lines, eight upper Y-select lines, eight lower X-select lines, and eight lower Y-select lines. The decoder outputs are applied to the selected switches. The outputs of the selected switches connect to the X-selection diodes (Paragraph 3.26.7) which, in turn, are connected to a line that is threaded through 768 memory cores. The arrangement of the illustration (Figure 3-41) is such that each component corresponds to the approximate location on the engineering drawing schematic (G227). This arrangement allows a quick reference to the circuits of interest.

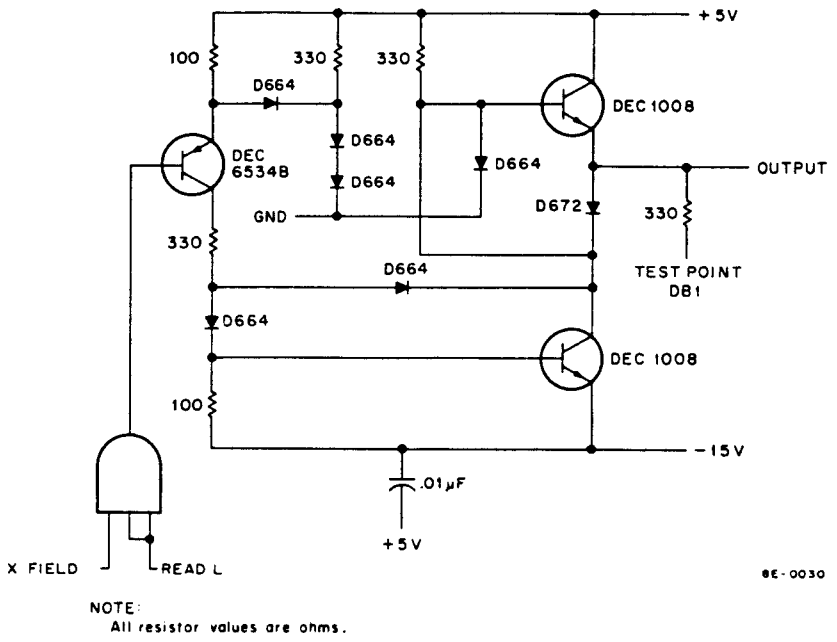


Figure 3-44 Bias Driver

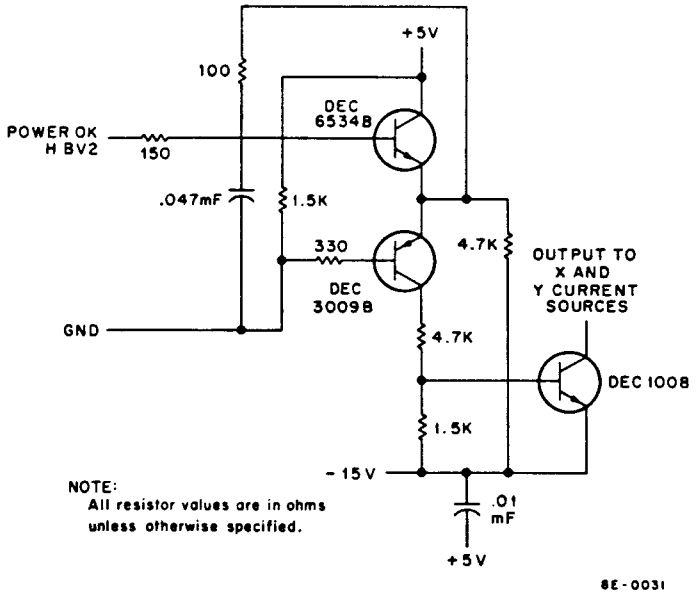


Figure 3-45 Power Fail Circuit

The decoding scheme of the MA bits is illustrated in Figure 3-46. The illustration shows the five parts of the memory address, what is decoded, and where in the field of the drawing the decoders are located. Table 3-3 lists the necessary input control signals, the content of the memory address, the input pins, the output pins, and the selected X- or Y-line. With this information, the user can easily trace through all of the components on any signal/current path to find the selected components.

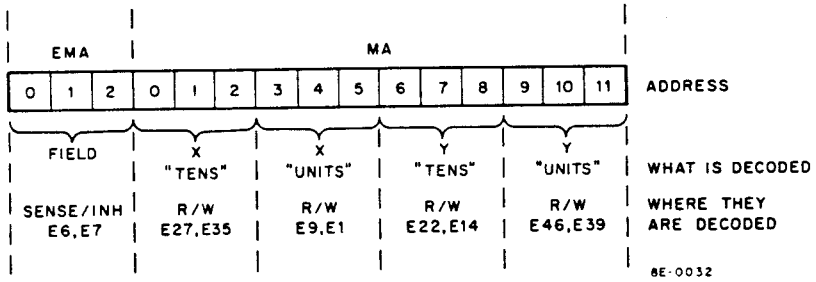


Figure 3-46 Decoding Relationships

3.26.7 Operation of Diodes

Each of the X- and Y-select lines are connected to a corresponding string of diodes (Figure 3-47). Selection is such that any one of the eight upper select lines will pass current in a path determined by whether it is a READ or WRITE operation. In the illustration given in Figure 3-47, for X-selection, the example illustrates line X_{12} being selected. The current passes through 768 cores and back through one of the diodes. The path the current takes from this point is determined by the diode that is forward-biased. The forward-biasing of a diode is accomplished by operating the switch and driver. If it is a WRITE operation, WX2 is forward-biased and the current takes the path from WX2 to X10. If it is a READ operation, RX2 is forward-biased and the current takes the path from RX10 to RX2.

NOTE

The READ and WRITE currents are opposite in direction. This is accomplished by READ L, which controls the Bias Driver circuit.

In both cases, the selection diodes are instrumental in determining the current path. All diodes except the selected diode are reverse-biased.

3.26.8 Operation of Selection Switches

Figure 3-48 illustrates the switching operation of the currents through X12 select line. On the upper side, a pair of transistors are used to either drive or switch current, depending on whether the operation is READ or WRITE. A complementary pair of transistors on the lower side are used to either drive or switch the current. Between the upper and lower side is a line that is threaded through 768 cores. The READ operation begins with the decoders. When an X-line such as X12 is to be selected, the READ driver and READ switch must first be turned on. To turn on the READ driver and READ switch, the base of each transistor must be positive with respect to the emitter. This occurs only when the output of the decoder is low (active). Otherwise, +5V is applied to the emitter side of the transformer as illustrated by S = open.

Table 3-3
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

READ (SOURCE-)

FUNCTION	FIELD	SOURCE	WRITE L	MA 0–2 (X) MA 6–8 (Y)	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Read Switch	L ↕ L	H ↕ H	L ↕ L		DBA				
				000	LLL	4L	– – – – – –		X or Y 00
				001	LLH	5L	– – – – – –		X or Y 10
				010	LHL	6L	– – – – – –		X or Y 20
				011	LHH	7L	– – – – – –		X or Y 30
							DBA		
				100	– – – – – –		LLL	4L	X or Y 40
				101	– – – – – –		LLH	5L	X or Y 50
				110	– – – – – –		LHL	6L	X or Y 60
				111	– – – – – –		LHH	7L	X or Y 70

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

WRITE (SOURCE-)

FUNCTION	FIELD	SOURCE	WRITE L	MA3–5 L MA9–11 L	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Write Switch	L ↕ L	H ↕ H	H ↕ H		DBA				
				000	LLL	0L	– – – – – –		WX0 or WY0
				001	LLH	1L	– – – – – –		WX1 or WY1
				010	LHL	2L	– – – – – –		WX2 or WY2
				011	LHH	3L	– – – – – –		WX3 or WY3
							DBA		
				100	– – – – – –		LLL	0L	WX4 or WY4
				101	– – – – – –		LLH	1L	WX5 or WY5
				110	– – – – – –		LHL	2L	WX6 or WY6
				111	– – – – – –		LHH	3L	WX7 or WY7

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

WRITE
(RETURN+)

FUNCTION	FIELD	SOURCE	WRITE L	MA0–2 L MA6–8 L	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Write Drivers	L ↕ L	H ↕ H	H ↕ H		DBA				
				000	LLL	0L	– – – – – –		X or Y 00
				001	LLH	1L	– – – – – –		X or Y 10
				010	LHL	2L	– – – – – –		X or Y 20
				011	LHH	3L	– – – – – –		X or Y 30
							DBA		
				100	– – – – – –		LLL	0L	X or Y 40
				101	– – – – – –		LLH	1L	X or Y 50
				110	– – – – – –		LHL	2L	X or Y 60
				111	– – – – – –		LHH	3L	X or Y 70

Table 3-3 (Cont)
Core Selection Decoding Scheme

Groups 1 and 2 – Upper X- and Y-Decoders

READ
(RETURN+)

FUNCTION	FIELD	SOURCE	WRITE L	MA3–5 L MA9–11 L	Group 1 Input Pins	Group 1 Output Pins	Group 2 Input Pins	Group 2 Output Pins	Selected Line
Turn on Read Drivers	L ↕ L	H ↕ H	L ↕ L		DBA				
				000	LLL	4L	– – – – – –		RX 0 or RY 0
				001	LLH	5L	– – – – – –		RX 1 or RY 1
				010	LHL	6L	– – – – – –		RX 2 or RY 2
				011	LHH	7L	– – – – – –		RX 3 or RY 3
							DBA		
				100	– – – – – –		LLL	4L	RX 4 or RY 4
				101	– – – – – –		LLH	5L	RX 5 or RY 5
				110	– – – – – –		LHL	6L	RX 6 or RY 6
				111	– – – – – –		LHL	7L	RX 7 or RY 7

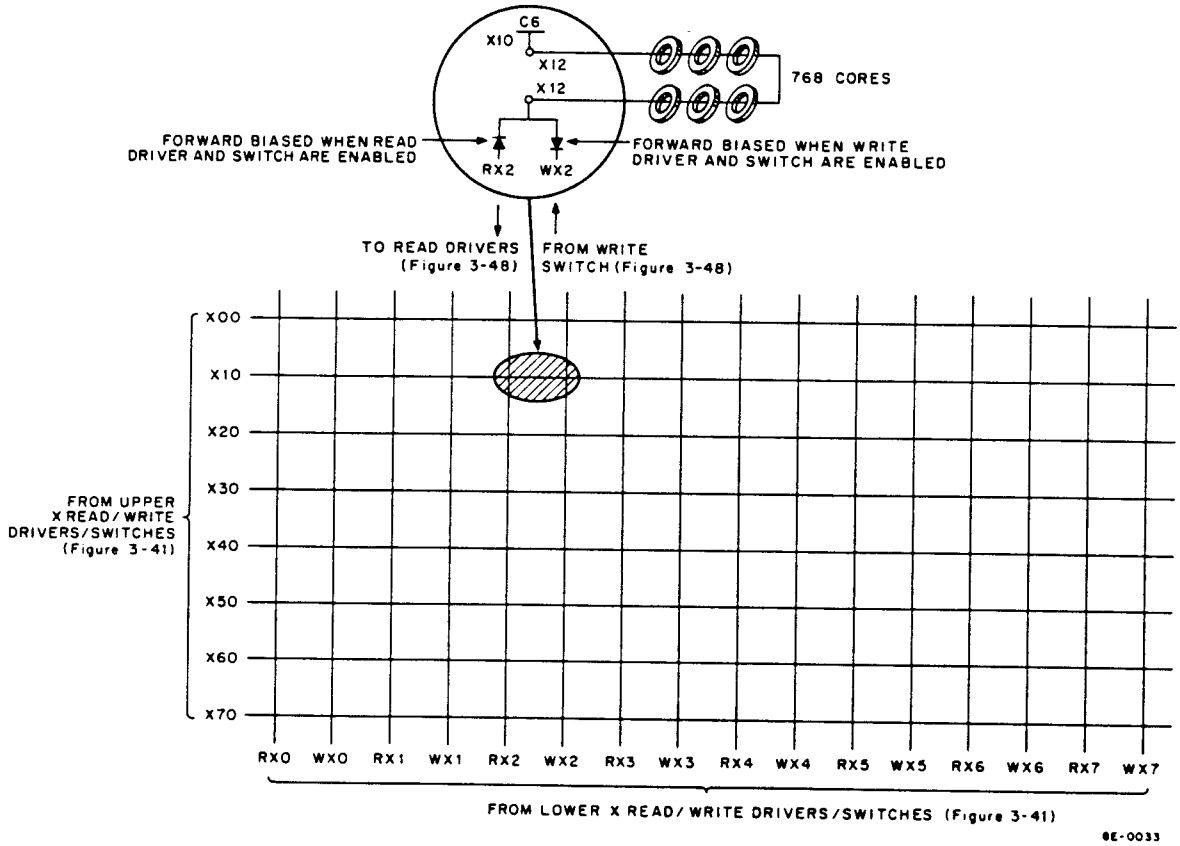


Figure 3-47 Organization of Planar Stack Diode Matrix for X Select Lines

When the READ driver is off, the +5V causes the READ diode at the current source to be reverse-biased. As soon as the READ driver is turned on, the READ diode immediately becomes forward-biased, allowing regulated current to be applied to the READ driver. The driver serves as a high-gain current amplifier, which supplies the required current to half-select any given core. A second requirement to pass READ current through core is to forward-bias the READ diode in the diode matrix. Current then passes through the READ driver, through the READ diode, through 768 cores, and back to the READ switch.

The WRITE operation is similar to READ and begins with the decoder. To select line X12, the decoder causes the WRITE driver transformer to reverse polarity, which then turns on the WRITE driver. The WRITE diode at the current source becomes forward-biased and current begins flowing through the diode, the WRITE diode of the matrix, and through 768 cores.

3.26.9 Operation of the Core Selection System

The cores that contain a selected X-line and selected Y-line define the location for which a 1 or 0 will be either written in or read out. Figure 3-49 illustrates a small portion of memory and the corresponding selection devices. Using Table 3-3, the selection of any given core can be traced from the Memory Address Register, through the decoders and switches, to the selected core.

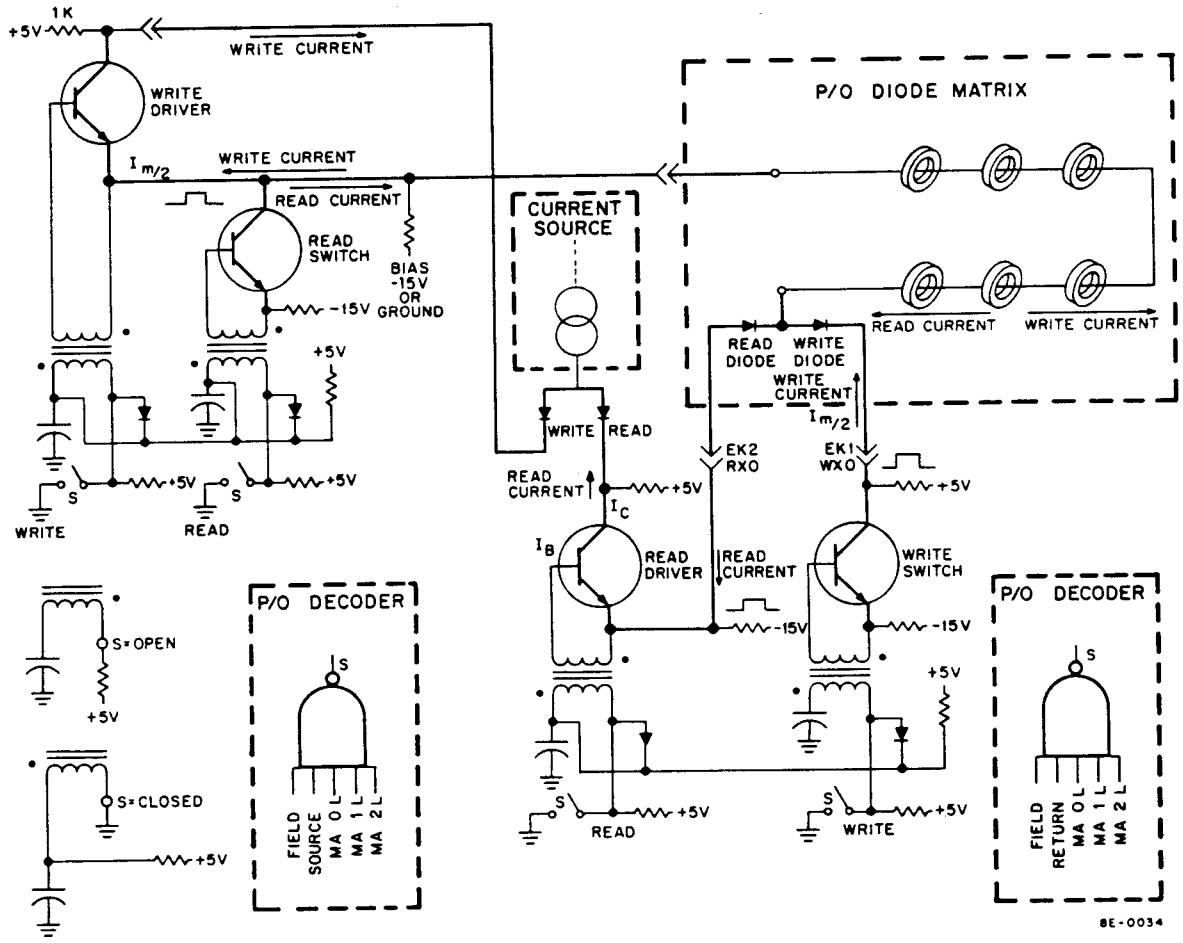


Figure 3-48 Operation of Selection Switches

3.27 SENSE/INHIBIT FUNCTION

The previous paragraphs have described the memory core, the selection of memory core, and the selection of memory core in terms of the READ/WRITE operation. However, to perform a READ or a WRITE operation, sense amplifiers are necessary to sense the state of the selected cores, and Inhibit Drivers are necessary to write 0s into core. Control logic and data registers are also required to control the data flow to and from memory. These necessary circuits are illustrated in a simplified diagram (Figure 3-50). The circuitry corresponding to the READ operation is shown on the lower portion of the illustration; the circuitry corresponding to the WRITE operation is illustrated in the upper portion of the illustration.

3.27.1 Sense/Inhibit Line

The line that is used to sense a 1 during READ is used to transmit current when a 0 is to be written during the WRITE portion of the memory cycle. The Sense/Inhibit line passes through 4096 cores of a corresponding mat. Both ends of this line are terminated at the input to the Sense Amplifier; a terminal connection is made so that the Inhibit Driver output joins this same line.

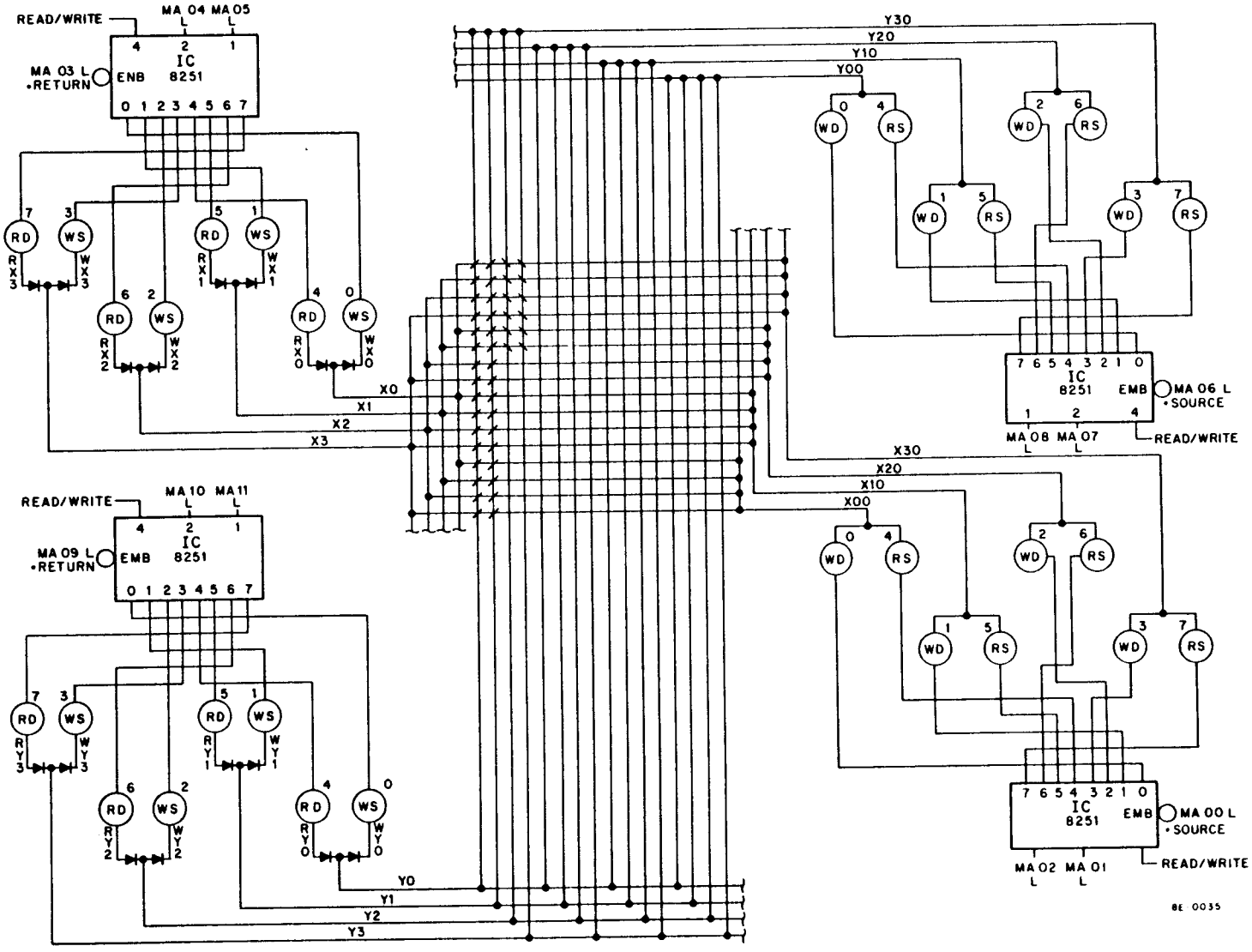


Figure 3-49 Operation of X/Y Selection Switches

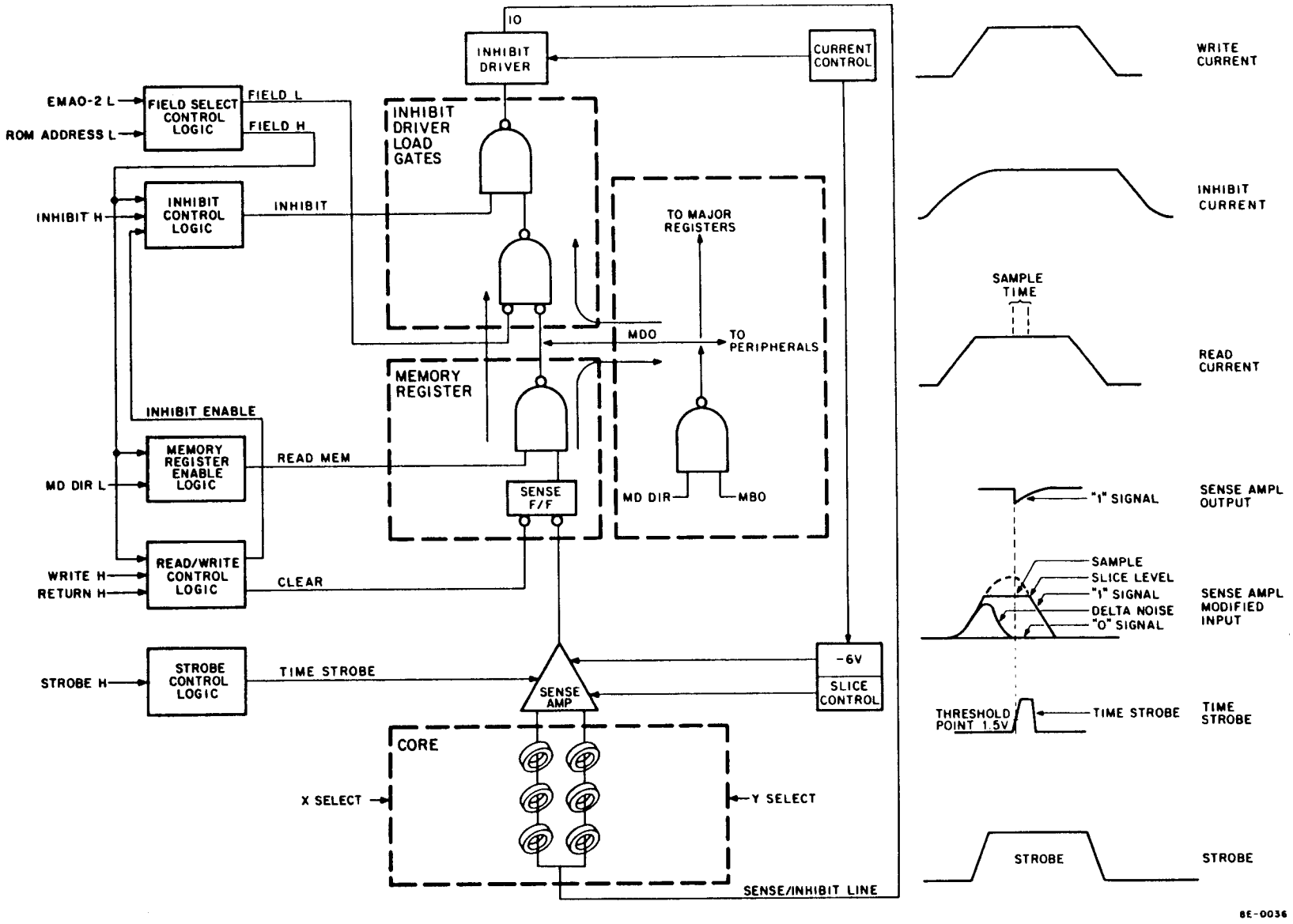


Figure 3-50 READ/WRITE Operation, Simplified Diagram (Bit 0)

3.27.2 READ Operation

The READ operation involves the Sense Amplifier, Memory Register, and the necessary control logic in conjunction with the selection system. During the READ portion of the memory cycle, the selected core develops a signal on the Sense/Inhibit line only if a 1 was previously stored in core. The SENSE flip-flops are cleared and TIME STROBE gates either a 1 or 0 out of the Sense Amplifiers and applies a corresponding pulse (if it is a 1) to the Memory Register. When a 1 is sensed, the Sense Amplifier applies a negative-going pulse to the SENSE flip-flop. The Memory Register output gate receives the SENSE flip-flop signal and gates the 1 or 0 out to the MD line. Note that the Memory Register outputs are gated onto the MD lines only when MD DIR L is low; consequently, the only requirement to write the contents of the Memory Register back into memory is to keep MD DIR L low during the WRITE portion of the memory cycle. The output of the Memory Register can be applied, therefore, to the inhibit circuits for a rewrite; or because the data is first applied to the MD BUS, the output of the Memory Register can be loaded into one of the major registers or a peripheral.

When the Memory Register applies data to the MD lines (Figure 3-2), the data can be loaded into any one of the Major Registers, as well as applied to the Inhibit Drivers for re-deposit into core. Conversely, the data contained in the Memory Buffer (MB) Register can be applied to the MD lines and to the Inhibit Drivers.

3.27.3 WRITE Operation

The WRITE operation involves the Inhibit Drivers, load gates, Memory Register, and the necessary control logic in conjunction with the selection system. The Inhibit Driver load gates receive 1s and 0s via the MD lines from either the MB Register in the processor or the Memory Register. Control gating signals for the Inhibit Driver load gates are:

a. FIELD, which indicates that field 0 has been selected,

b. INHIBIT from the Timing Generator. Inhibit current is generated by the Inhibit Drivers only when a 0 is to be written into core.

3.27.4 Field Select Control Logic

The field select control logic (Figure 3-51) determines if the basic memory has been selected. When field 0 is selected, the logic develops a signal, called FIELD, for gating other control logic and the Inhibit Driver load gates. The logic receives extended address memory bits EMA0 L through EMA2 L.

A comparison circuit compares the bits on the EMA lines with the EMA jumpers. If the two are equal and if ROM ADDRESS L is high, the field is selected. Bank 0 is always selected with all jumpers in. The Exclusive-OR gate provides a high output only when one input is high.

3.27.5 Inhibit Control Logic

The Inhibit Control logic (Figure 3-52) provides a gating control signal to the Inhibit Driver load gates during the WRITE portion of the memory cycle. The logic receives INHIBIT from timing, RETURN from the Timing Generator, FIELD from the Field Select Control logic, and WRITE ENABLE from the READ/WRITE control logic.

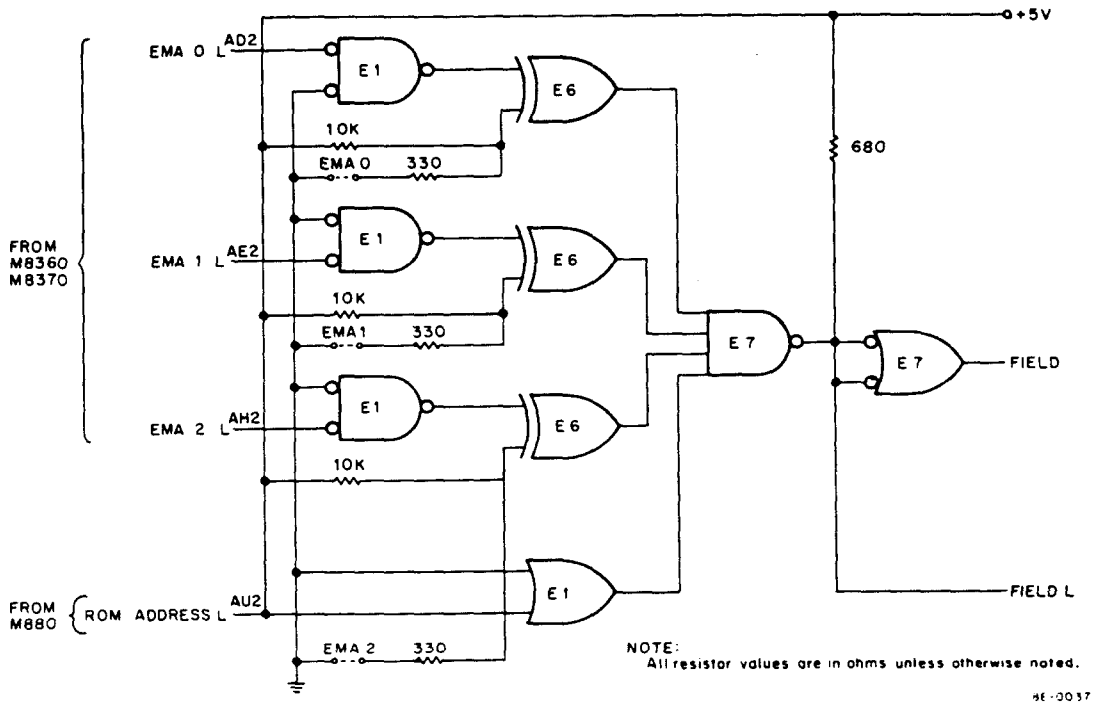


Figure 3-51 Field Select Control Logic

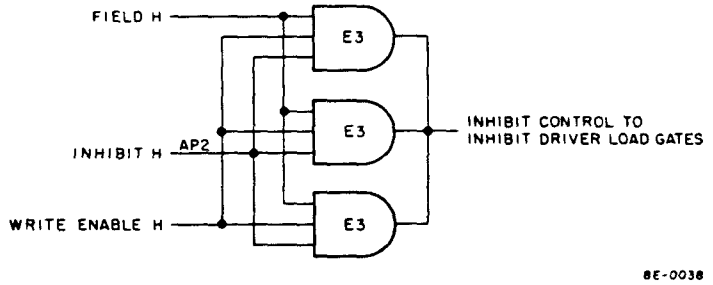


Figure 3-52 Inhibit Control Logic

3.27.6 Memory Register Enable Logic

The Memory Register Enable logic (Figure 3-53) functions when the contents of the Memory Register are to be gated onto the Inhibit Drivers and MD lines. When MD DIR L is low, the output of the control logic (READ) gates the content of the SENSE flip-flops to the MD BUS.

3.27.7 READ/WRITE Control Logic

The READ/WRITE Control logic (Figure 3-54) clears all SENSE flip-flops and enables the Inhibit Control logic.

The CLEAR L signal only becomes active when WRITE H is not active and RETURN H is asserted. This begins at the start of the READ portion of the memory cycle and continues for a period of approximately 50 ns. The CLEAR L signal becomes inactive when the E4 flip-flop is reset by the CLEAR L signal input.

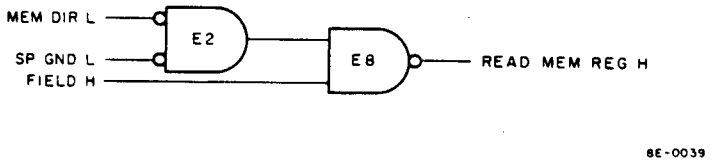


Figure 3-53 Memory Register Enable Logic

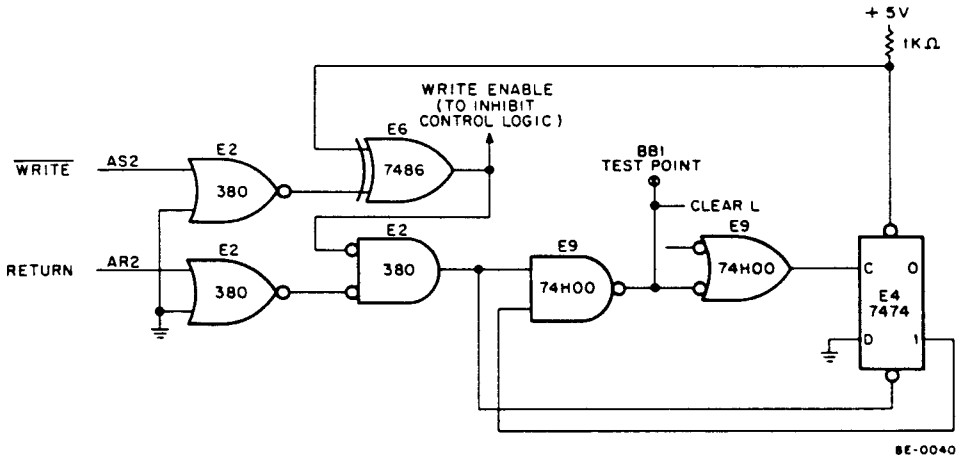


Figure 3-54 READ/WRITE Control Logic

3.27.8 Strobe Control Logic

The Strobe Control logic (Figure 3-55) is used to control the sample time of the Sense Amplifiers during the READ portion of the memory cycle. TIME STROBE occurs when WRITE L is not asserted, FIELD has been selected, and the STROBE timing signal from the Timing Generator has been received. STROBE is gated in and passed through an adjustable time-delay circuit. The flip-flop (7474) senses the rise and fall times of the strobe pulse and enables the output gate. The signal can be observed at test point CA1 (using a module extender).

3.27.9 Sense Amplifiers

Twelve Sense Amplifiers (Figure 3-56) are required to sense signals on the twelve sense lines. If the selected core in a given mat contains a 1, a pulse is received on the Sense/Inhibit winding. This pulse is amplified by the Sense Amplifier and then used to set a 1 into the Memory Register. If the selected core contains a 0, the signal received by the Sense Amplifier is small, and no pulse appears at the output of the Sense Amplifier; the Memory Register remains in the 0 state. The Sense Amplifier is "strobed" with a narrow pulse to ensure that the content of the sense lines is sampled at the proper time. This timing is necessary because the cores in the 0 state produce a small signal when "sensed" and because many of the cores in each mat receive half-selected pulses. The total sum of the noise can be considered a "delta noise", which appears at the early portion of the core selection time. The noise, generated by the half-selected cores, ceases shortly after the half-select pulses are started. Therefore, the Sense Amplifier is strobed during the latter part of the READ time, when the output resulting from a selected core-reversing state is highest in proportion to the noise from half-selected cores (maximum signal-to-noise ratio). Because the delta noise is confined to a smaller amplitude with respect to ground, the slice control ensures that any sampling of the 1 state occurs beyond the noise level amplitude. Thus, there are two methods of avoiding

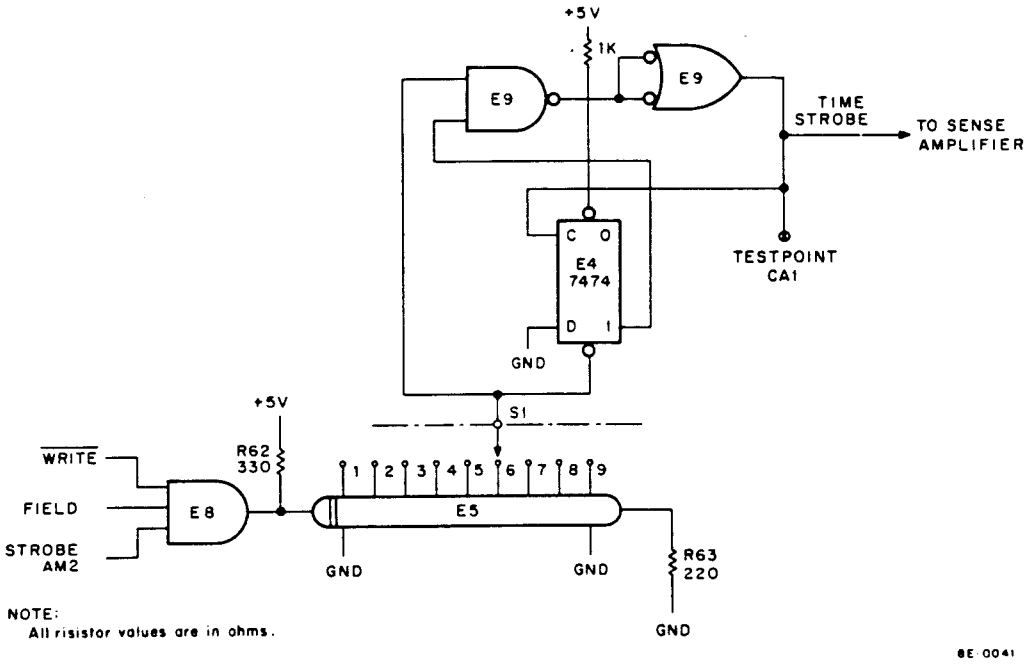


Figure 3-55 Strobe Control Circuit

the delta noise: (a) sample beyond the noise level amplitude, and (b) sample after the noise pulse. The delta noise is a direct function of the switching of the cores. For a 0, the Sense Amplifier senses a negligible change; a delta noise occurs but is not sensed, because STROBE is applied after the noise has settled down. STROBE is factory adjusted so that sampling clears the delta noise pulse, but does not clear it so far that the amplitude of a 1 is missed. This adjustment is in increments of 10 ns in a range of 30 to 40 ns. STROBE can be adjusted at the time-delay switch shown in Figure 3-55. However, the switch positions should not be changed until the diagnostic procedures indicate that STROBE timing is not properly synchronized. There are six distinct values on this switch in 10 ns increments. The switch is connected to a tapped delay line located on the Sense/Inhibit board. At CA1, a test point is available if any troubleshooting is necessary. The waveform is illustrated in Figure 3-56, corresponding to pin 9 of the Sense Amplifier; the sense line waveform at pin 10 is also shown. During the 1 state, the top portion is sliced off by the slice control input.

The balun transformer shown in Figure 3-56 performs an equalizing function for the inhibit currents during a WRITE operation. The Sense/Inhibit line is constructed so that one end of the wire is connected to one leg of the balun transformer, and the other end of the wire is connected to the other leg of the transformer. The inhibit output is tapped in the middle of this wire, thus forming a Y-type of connection. During the WRITE portion of the memory cycle, it is necessary to apply an equal amount of current through both legs of the Sense/Inhibit line. However, because the resistance on each leg is not exact (approximately 3Ω), it is possible to have 20 percent more current on one leg than the other. The balun transformer functions to make up the difference in current so that both legs are equalized. When the inhibit current is removed, a voltage backswing is prevented from entering the amplifier by the presence of the diodes. During the READ portion of the memory cycle, both ends of the diodes are at ground level and, therefore, back-biased. During the WRITE portion of the memory cycle, these diodes are forward-biased and, therefore, the transformer immediately begins balancing the currents.

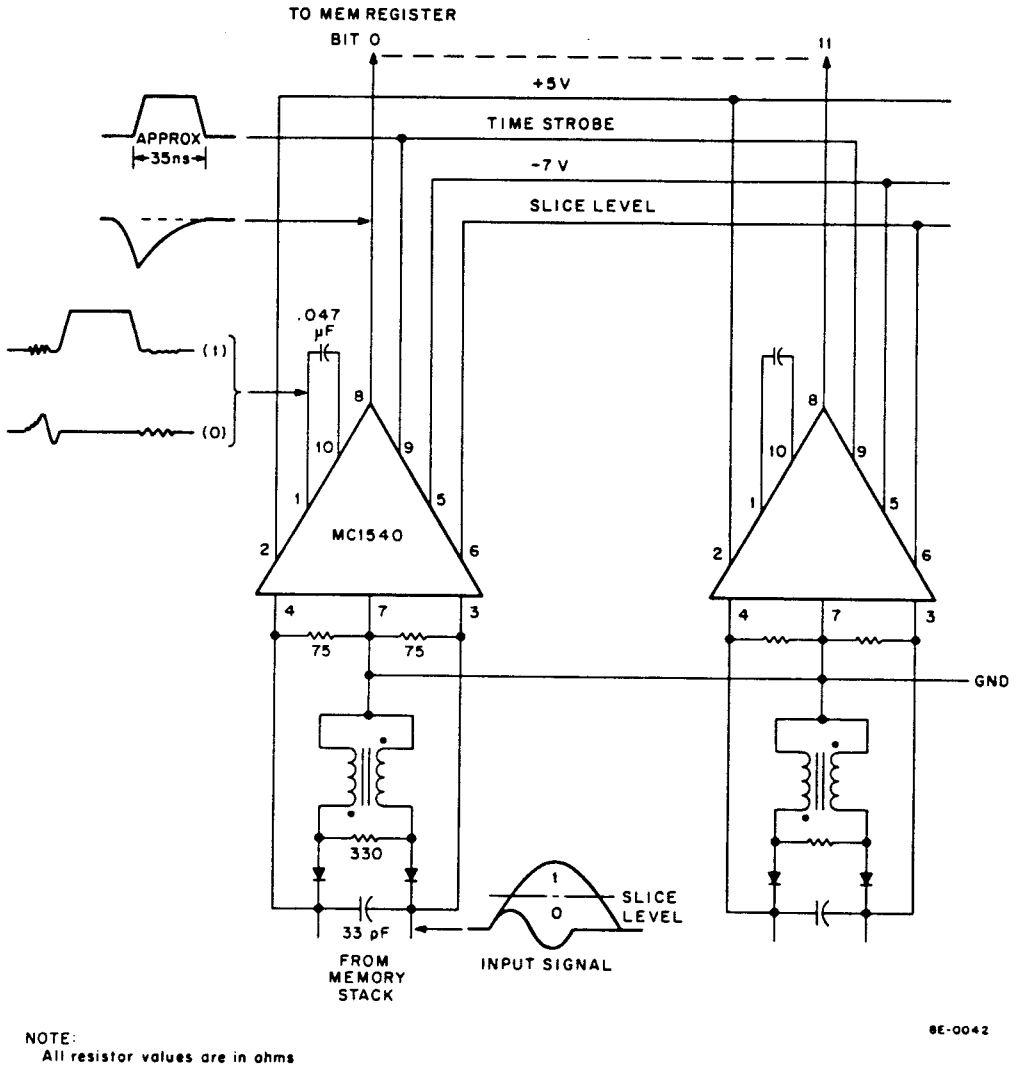


Figure 3-56 Sense Amplifiers

3.27.10 Memory Register

The Memory Registers (Figure 3-57) retain the information strobed out of the Sense Amplifiers until a CLEAR L signal is received during the first 50 ns of the next READ operation. The output gates, controlled by the READ MEM signal, drive 1s and 0s into the Inhibit Driver load gates. The flip-flops are termed "Sense flip-flops" and are set when there is a 1 (negative-going pulse) on the output of the corresponding Sense Amplifier. READ MEM is enabled only when MD DIR L is low.

3.27.11 Inhibit Driver Load Gates

The Inhibit Driver Load Gates (Figure 3-58) control the WRITE operation. During READ, the contents of the sense lines are placed on the MD lines. With FIELD (active) and INHIBIT (active), the contents of the MD lines are gated into the Inhibit Drivers. INHIBIT is generated in the Timing Generator only during the WRITE portion of the memory cycle.

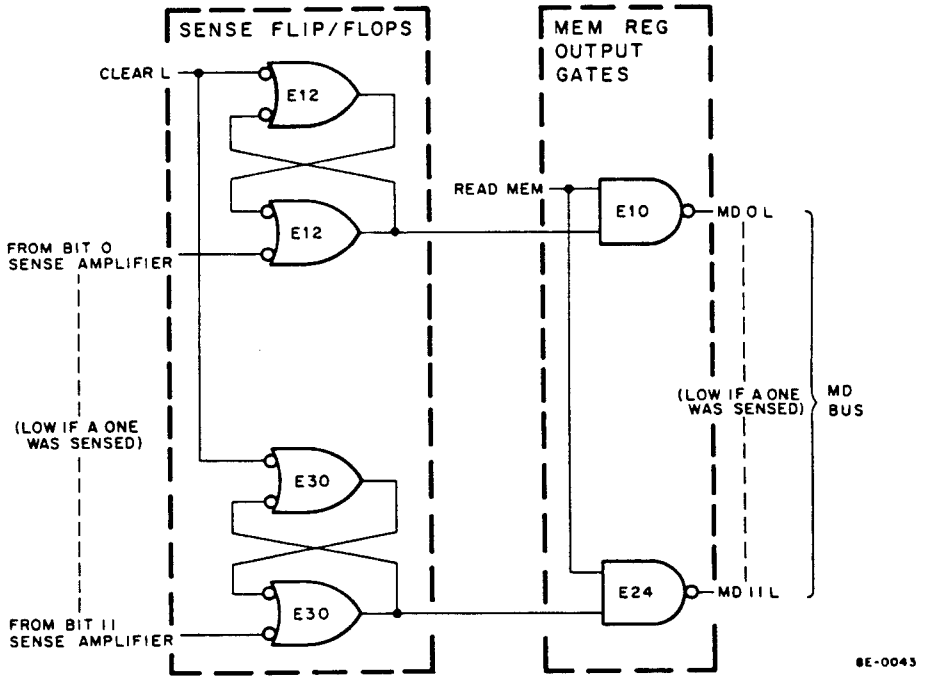


Figure 3-57 Memory Register

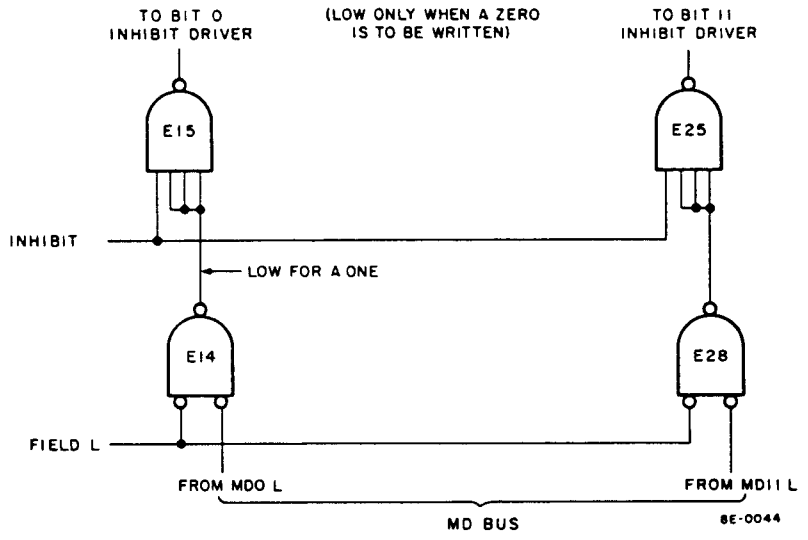


Figure 3-58 Inhibit Driver Load Gates

The MD lines receive data from the Sense flip-flops. When a FETCH or DEFER state is being processed, MD DIR L is made low and the memory cycle is a fast cycle (1.2 μs). This allows the content of the Sense flip-flops to be gated out to the Inhibit Driver load gates during WRITE and, subsequently, applied to the Inhibit Drivers. When data is to be written into memory from the MB Register, memory cycle timing is 1.4 μs and MD DIR L is high during the WRITE portion of the memory cycle. The Sense flip-flops are then made inactive, and the Inhibit Driver input gates look at only the MB Register. If data break is used, data is transferred immediately from a peripheral to the MB Register and gated into memory during the current memory cycle. During most other types of transfer operation, data must be transferred from the AC Register to the MB Register and applied to the Inhibit Driver input gates.

3.27.12 Inhibit Drivers

Inhibit Drivers (Figure 3-59) apply inhibit current to the selected core when a 0 is to be written. Each of the 12 drivers receives either a positive level (for a 1) or a ground input (for a 0) at the 1:1 input transformer. During a 0 output of any Inhibit Driver load gate, the transistor-base side of the transformer secondary is positive with respect to the emitter side. This forward bias turns the transistor on, allowing inhibit current to pass through and be applied to the selected core. Because the inhibit current direction is opposite to the write select current, a half-select condition results and the core remains in the 0 state. During a 1 output of any one Inhibit Driver input gate, the transistor-emitter at the same potential as the base and the transistor does not conduct. The full select current is then applied to the corresponding core, which results in a 1 state. The Inhibit Driver acts as a relay solenoid driver. It consists of an inductor, a resistor, and a switching transistor. When the transistor is turned on, the Inhibit line current is determined by the transistor emitter circuit. When the switch turns off, the energy stored in the inductor creates a back EMF that can damage the transistor circuit. The diode-to-ground at the collector output is used to protect the transistor from this unwanted backswing condition.

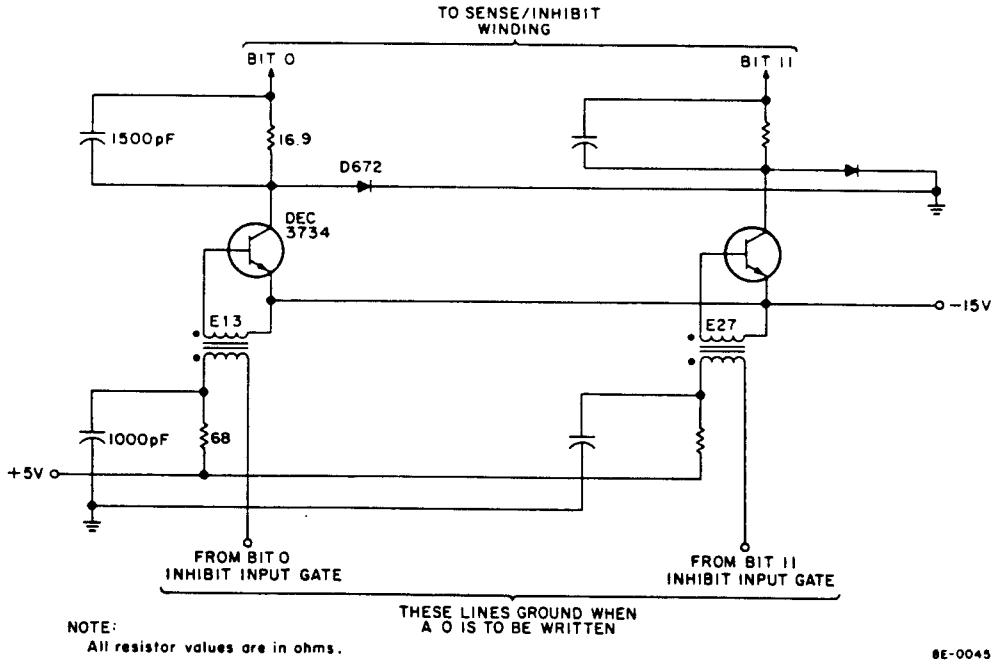


Figure 3-59 Inhibit Drivers

3.27.13 Current Control Circuit

The Current Control circuit (Figure 3-60) controls the current level in the X- and Y-select lines. The control circuit operates on a +5V and -15V supply. The output of the X- and Y-current sources (Figures 3-42 and 3-43) is a voltage-regulated supply that varies with temperature changes. The temperature sensing is accomplished by the thermistor, located on the memory stack board. The two jumpers are factory installed to control the preset X- and Y-current reference point.

3.27.14 -7V Supply and Slice Control Circuits

The -7V Supply and Slice Control circuits (Figure 3-61) provide a voltage slice level to the Sense Amplifier (Figure 3-56) and a regulated -5 Vdc output to the Sense Amplifier. The slice level is controlled by jumpers SLA and SLB, which are factory installed.

3.28 MEMORY TRANSFER CONTROL LOGIC

Memory transfer control is accomplished by signal MD DIR L. When MD DIR L is low, the content of the Memory Register, containing information from the READ operation, is gated out to the MD BUS. When MD DIR L is high, the content of the MB Register is gated out to the MD BUS for deposit in memory during the WRITE operation. When the processor directs memory to write back into memory the word retrieved during READ (manipulating signal MD DIR L), MD DIR L remains low during the WRITE operation. The content of the Memory Register is on the MD BUS; consequently, the same word is written back into memory. This procedure always applies during FETCH and DEFER (NON-AUTOINDEX).

3.28.1 Transfer Control During FETCH, DEFER, or EXECUTE States

The memory transfer control logic for FETCH, DEFER, or EXECUTE states is illustrated in Figure 3-62. A CLEAR L signal is generated by timing 100 ns after the start of TS1. This resets E19, which asserts MD DIR L. The flip-flop remains unchanged until TP2 is received as a clock input. If the major state is FETCH, a low will be clocked into the data input of the flip-flop, and E19 remains unchanged until TP2 of the next cycle. If the major state is DEFER (NON-AUTOINDEX), a low will be clocked into the data input of the flip-flop, and E19 remains unchanged. Thus, in both cases, the data from the Memory Register is re-deposited in memory.

If the major state is DEFER and AUTOINDEX (MA0—7 L equals 0 and MA8 L equals 1), a high is clocked into the flip-flop, and E19 is set. A low into E27 causes MD DIR L to go high, and memory receives the data from the MB Register.

If the major state is EXECUTE, a high is clocked into the data input of the flip-flop, and E19 is set; this condition, as in the previous case, causes MD DIR L to be high.

3.28.2 DMA State, Manual Operation Transfer Control

MD DIR L is high at TP2 unless pulled low by the Memory Transfer Control logic in the Programmer's Console (Figure 3-63).

Because FETCH or DEFER is not asserted, due to the DMA state, the Memory Transfer Control logic in the Timing Generator remains high, because no reset pulse is generated by timing. Either the LOAD ADDR or EXAM key, when depressed, will generate MD DIR L, which places the content of the Memory Register onto the MD BUS.

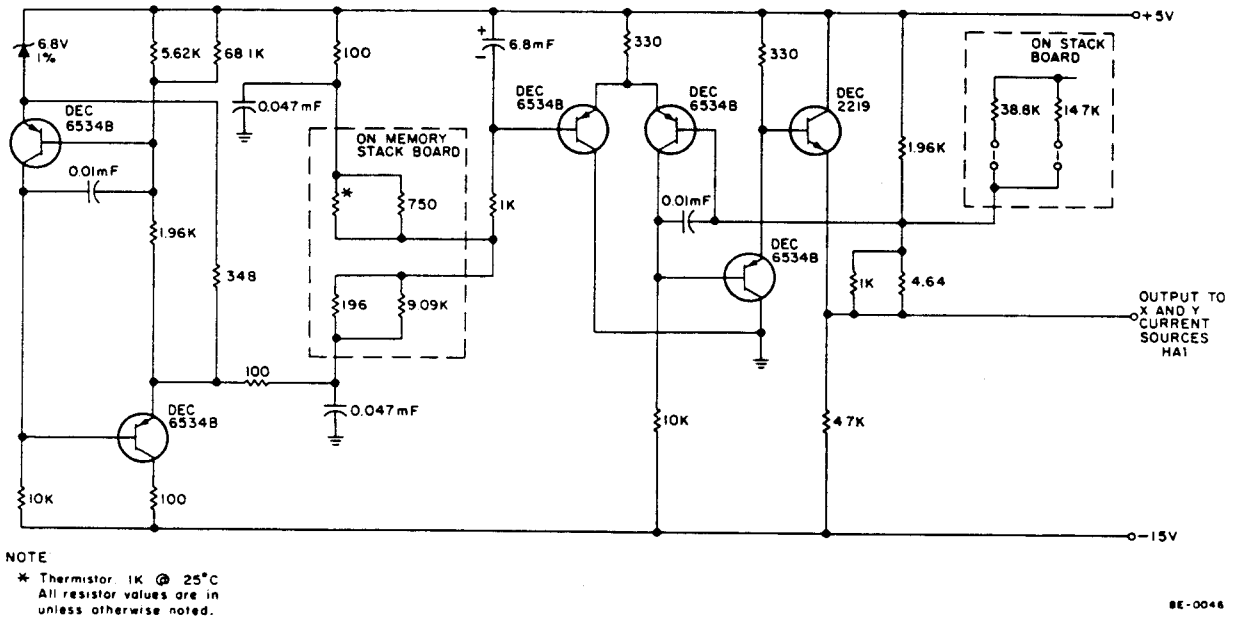


Figure 3-60 Current Control

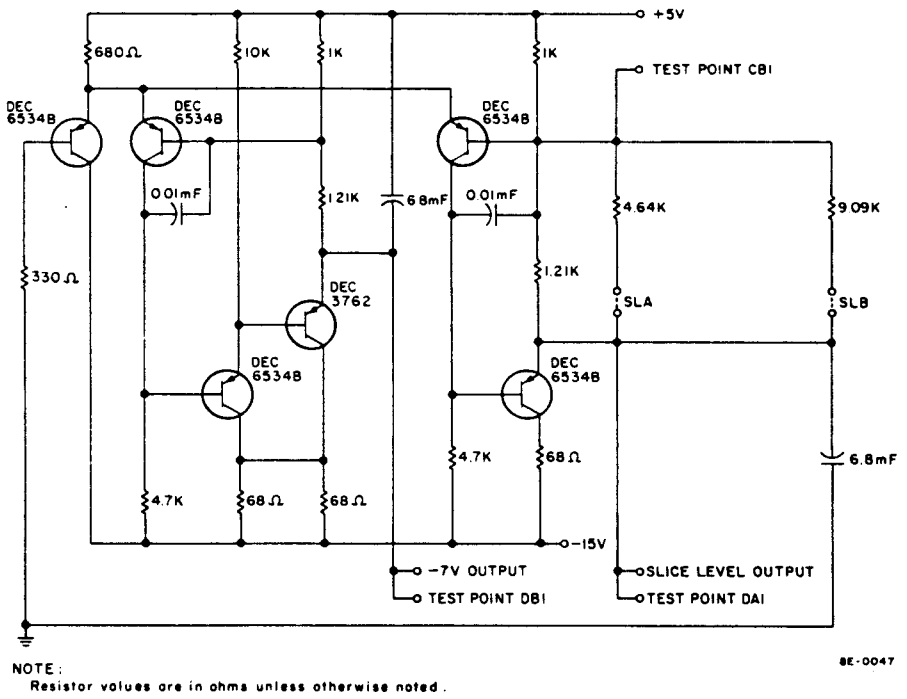


Figure 3-61 -7V Supply and Slice Control Circuits

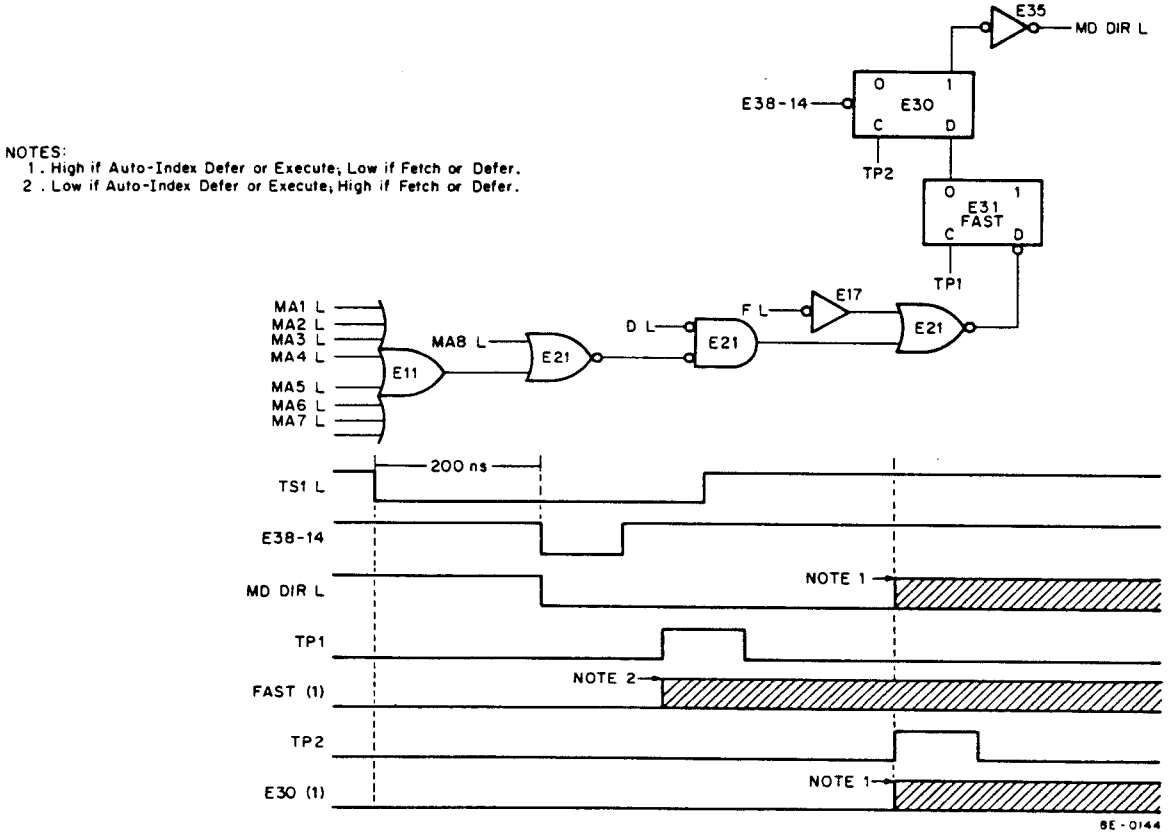


Figure 3-62 Memory Transfer Control Logic (FETCH, DEFER, or EXECUTE)

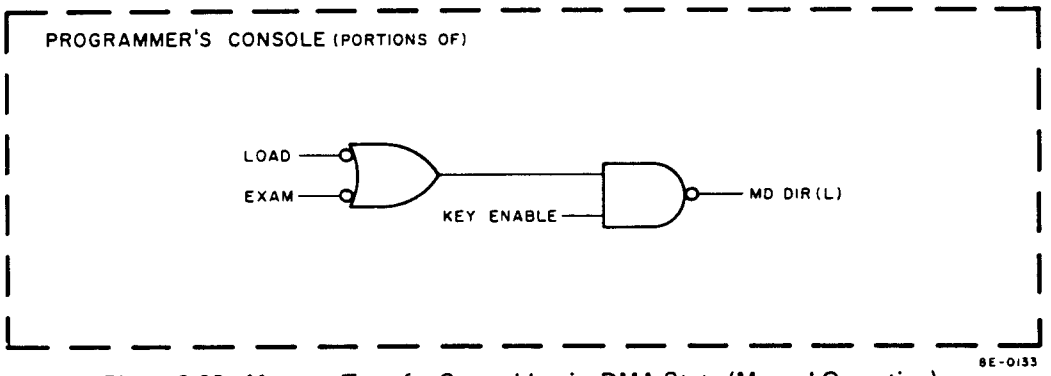


Figure 3-63 Memory Transfer Control Logic, DMA State (Manual Operation)

When data is deposited into memory, the data path is from the DATA BUS to the MB Register to memory. Thus, MD DIR L must go high so that the content of the MB Register can be gated out to the MD BUS.

3.28.3 DMA State, Data Break Operation

Each data break device contains Memory Transfer Control logic. MD DIR L will always be low except when:

a. Incrementing the word count (3-cycle data break device)

b. Incrementing the current address (3-cycle data break device)

c. Transferring data from the device to memory, or incrementing memory.

Refer to Volume 2, Chapter 10 of this manual for a detailed discussion of data break transfers.

3.29 CENTRAL PROCESSOR, GENERAL DESCRIPTION

The central processor unit (CPU) manipulates data in response to a predetermined sequence of instructions. In the PDP-8/E, both the data to be manipulated and the instructions are stored in memory. An instruction is brought from memory to the processor where it is decoded to determine, first, what to do to the data, and, second, what data is affected. When the data has been manipulated, the result is stored within the processor, transferred to a memory location, or transferred to some peripheral equipment. The CPU consists of the M8300 Major Registers module, and the M8310 Major Register Control module.

3.30 CENTRAL PROCESSOR, FUNCTIONAL DESCRIPTION

Figure 3-64 shows the functional breakdown of the CPU and should aid in understanding processor operation. To perform all the operations involved in retrieving, storing, and modifying information, the CPU utilizes the major registers, previously introduced. Data is transferred between registers, between registers and memory (via the OMNIBUS MD lines), between registers and peripherals (via the OMNIBUS DATA lines), and between registers and internal options. Transfers are accomplished by a major register gating network, which selects the particular register that takes part in the transfer and performs some operation on the data being transferred. The selection and operation performed are determined by control signals developed within the Major Register Control logic. This logic also provides control signals that determine the destination of the transferred data.

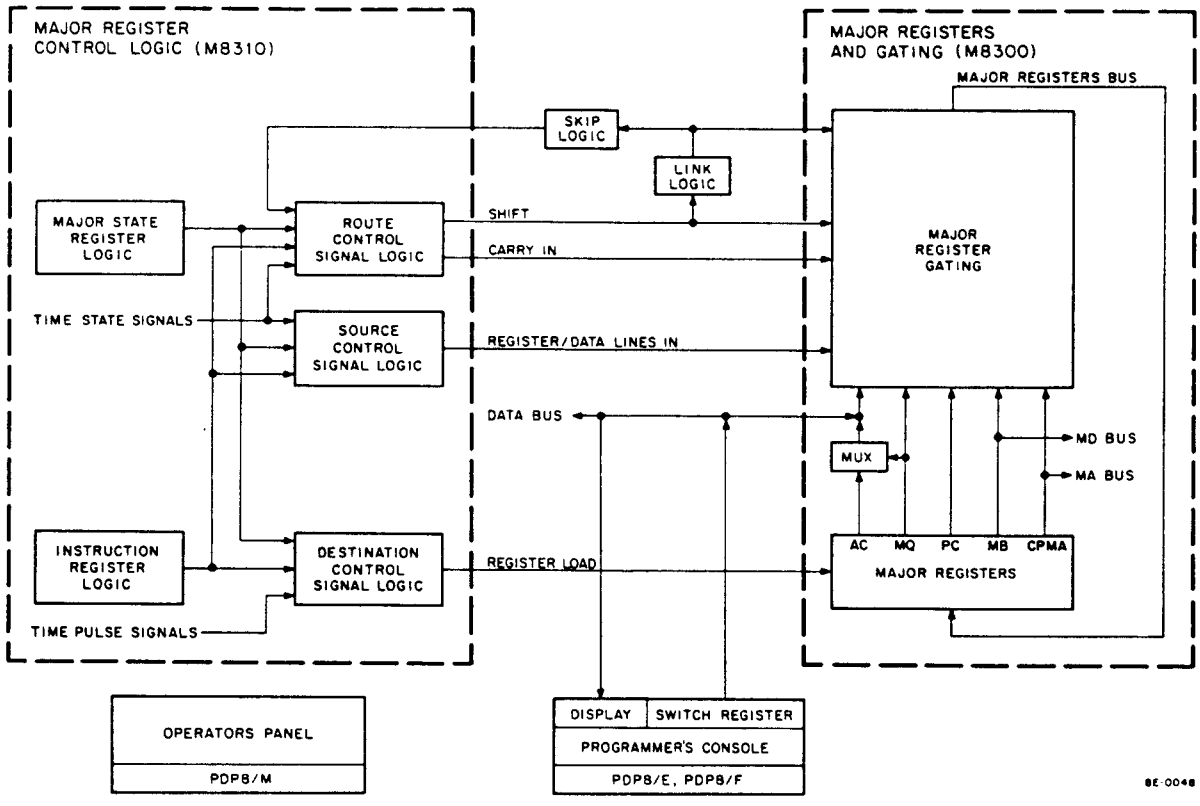


Figure 3-64 Block Diagram, Central Processor Unit

The signals that control the registers and their gating are developed within the Major Register Control logic. The signals are developed largely in response to three variables: (a) basic instructions (as decoded by the Instruction Register logic), (b) processor major states (as determined by the Major State Register logic), and (c) time states and time pulses. These variables are combined to produce control signals that make the major register gating network function. For convenience, these signals are grouped according to function. Thus, source control signals select the register that contains the data to be operated on; route control signals determine what is done to the data, and then place the result on the MAJOR REGISTERS BUS; finally, destination control signals load the result into the selected register.

Two other logic groupings are the Skip logic and the Link logic. Both logic blocks utilize timing signals, major state signals, and instruction signals, among others, to carry out operate microinstructions. The LINK, itself, is used to extend AC Register arithmetic capability. As shown, the LINK can be applied to the major register gating in response to shift signals. It is also used to initiate Skip logic in response to certain operate microinstructions. The Skip logic, in carrying out various microinstructions, is used primarily to generate the Carry In route control signals.

The Programmer's Console, although not physically part of the CPU, is functionally inseparable. The operator can communicate with the major registers and cause data transfers to occur by operating various front panel keys. Data is transferred between the console and the processor on the DATA lines, in response to control signals generated within the console logic (Figure 3-64). If an Operator's Panel is used instead of the Programmer's Console, the operator has no control over the processor. He can turn power on at the front panel, and he can cause memory and processor timing to begin, provided certain options are connected to the OMNIBUS.

Each functional group is discussed, in detail, in succeeding sections. Expressions of the form PC → MA were introduced earlier. The quantities to the left of the arrow represent the source data. This data is transferred to the destination indicated on the right of the arrow. Source data is produced during a time state, either by a time state signal itself (TS3) or by a composite that includes the time state signal (DCA·E·TS3). Source data is loaded into the destination by the time pulse that corresponds to this time state signal, or by a composite that includes the time pulse. Thus, source data produced during TS3 is loaded into its destination at TP3. This information will aid in understanding processor operation.

3.31 FRONT PANEL OPERATIONS

The front panel of the basic computer can incorporate a Programmer's Console or an Operator's Panel, the latter usually finding greater application with OEMs. In either case, the respective module contains keys and switches, indicating devices, and the logic that drives the controls and indicators. The controls protrude through slots in the silk-screened front panel; the indicators are visible at designated spots on the panel.

The PDP-8/M Operator's Panel, KC8-M, is described in Paragraph 3.32. The PDP-8/E and the PDP-8/F Programmer's Consoles, KC8-EA and KC8-FL, respectively, are described in Paragraph 3.33. Information concerning the types of front panels available with each system can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

3.32 KC8-M OPERATOR'S PANEL

The Operator's Panel is used with the PDP-8/M (Figure 1-4). Unlike the Programmer's Console, the Operator's Panel printed circuit board does not plug into the OMNIBUS. Instead, it is hardware-mounted to the front panel and connected to the OMNIBUS by a connector/harness assembly. Only the SW switch, an integrated circuit, two resistors, and a capacitor are mounted on the printed circuit board. The light-emitting diodes (LEDs) that indicate POWER and RUN are mounted directly on the front panel.

Figure 3-65 represents the Operator's Panel printed circuit board and the connections to the OMNIBUS. Part of the ON/OFF microswitch wiring is also shown. P1 of the OMNIBUS harness assembly connects to J1 of the printed circuit board. When the power is on, the POWER LED will glow. When the RUN L signal is low, indicating that the Timing Generator is producing memory and CPU timing signals, the RUN LED will glow. When a KC8-M Operator's Panel is used, the Timing Generator cannot be turned on at the front panel unless an MI8-E Bootstrap Loader option is included in the system. If such a module is plugged into the OMNIBUS, the operator can start the Timing Generator by depressing and lifting the SW switch. If a KP8-E Power Fail and Auto-Restart option is included in the system, the Timing Generator can be turned on merely by turning the microswitch to ON.

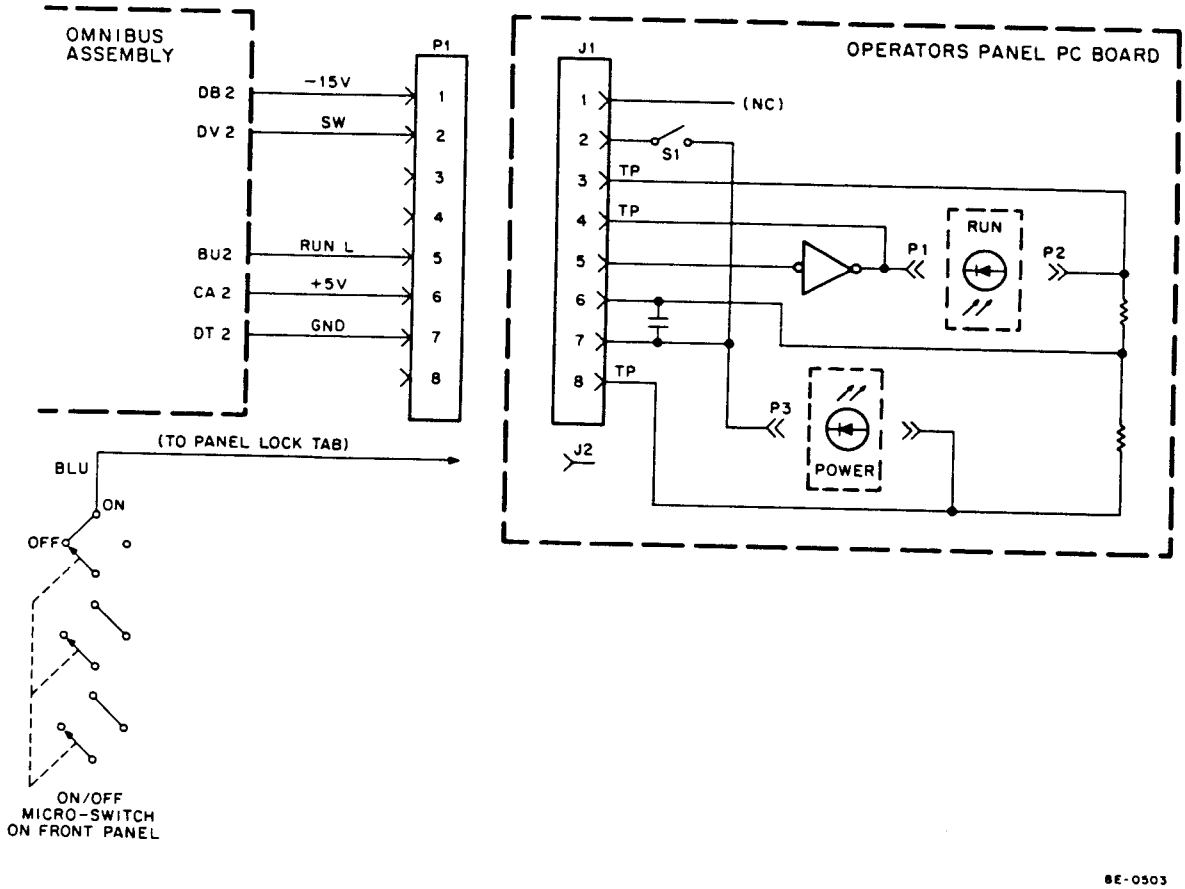


Figure 3-65 KC8-M Operator's Panel Logic

Note that a tab, labeled J2, is included on the Operator's Panel printed circuit board. This tab accommodates a spade lug that is connected by a wire to one section of the ON/OFF microswitch. This wire has no significance to a KC8-M and J2 is provided only in the interest of good housekeeping. However, a PDP-8/M can be equipped with a KC8–ML Programmer's Console (identical to the KC8-FL). In this case, the wire referred to is quite important. Figure 3-66 shows the OMNIBUS harness assembly and P1. When the KC8-ML is used, J1 of the microswitch harness assembly connects to P1. The spade lug on the end of the blue wire connects to the panel lock tab on the Programmer's Console. When the OFF/POWER/PANEL LOCK microswitch is in the POWER position, the -15V supply is connected to the console. In the PANEL LOCK position, the voltage is removed from the console, and switches, controls, and indicators (except the RUN indicator) are inoperative.

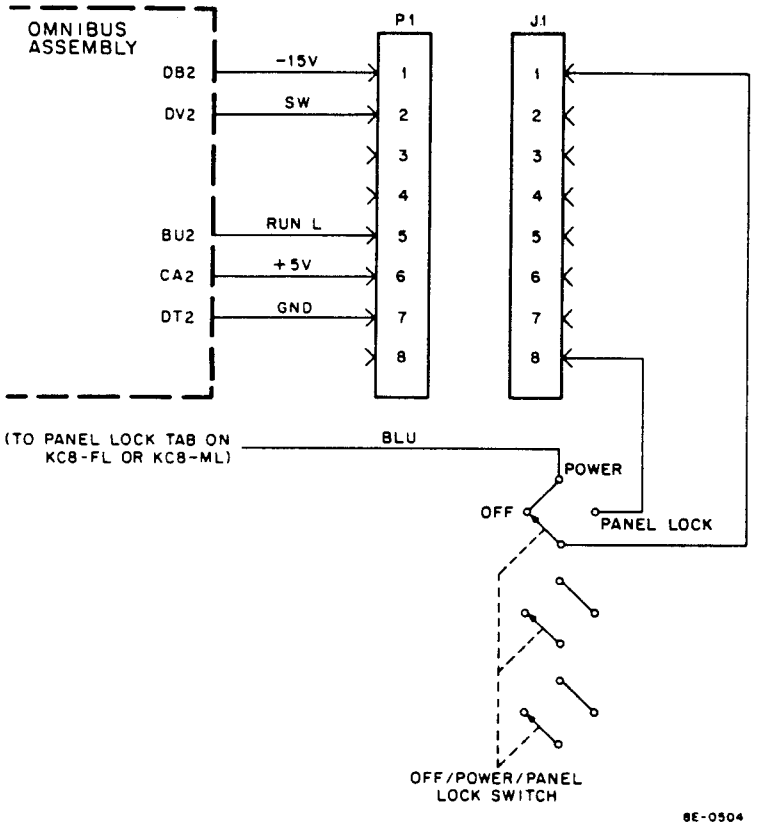


Figure 3-66 PDP-8/M Panel Lock Wiring

3.33 PROGRAMMER'S CONSOLE, GENERAL DESCRIPTION

Figure 3-67 is a block diagram of the two major functions of the KC8 Programmer's Console: manual operation and display. The display enables the operator to monitor the content of certain processor major registers, as well as the state of many of the OMNIBUS signal lines. Manual operation enables the operator to load programs into memory, initiate and halt automatic operation of the computer, and perform specialized tasks, which are discussed in subsequent sections.

As shown in Figure 3-67, the manual operations can be divided into a number of subordinate functions for convenience. Thus, several keys are grouped under the heading "manual start" to indicate that these keys initiate a timing cycle. Two switches, SING STEP and HALT, can be used to stop operation and are grouped under the heading "manual stop". The flow diagram, Figure 3-68, relates the manual functions to the processor time states.

The logic that makes manual operation and display possible is contained on the Programmer's Console module. The logic of the PDP-8/F Programmer's Console, KC8-FL, is simpler than that of the PDP-8/E Programmer's Console, KC8-EA (an earlier version of the KC8-FL uses logic that is similar to that of the KC8-EA; this version, which is not detailed in this manual, has been improved on the current model). The KC8-EA is described in Paragraph 3.33.1; the KC8-FL is described in Paragraph 3.33.2.

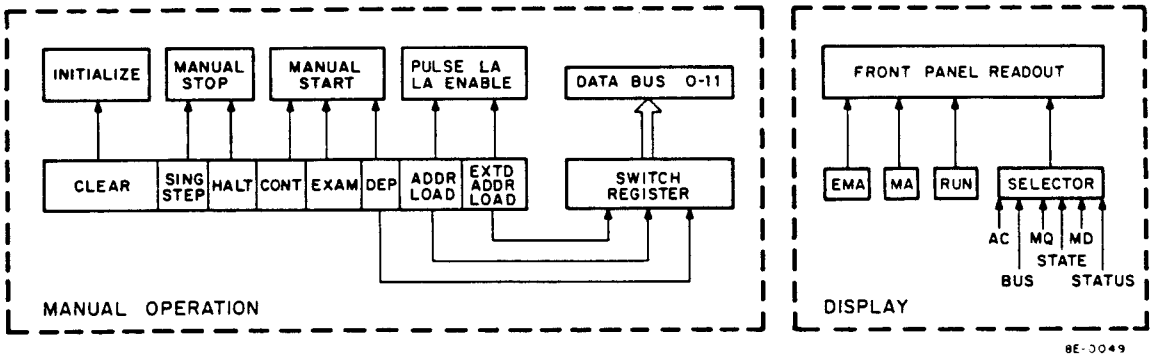


Figure 3-67 Programmer's Console, Block Diagram

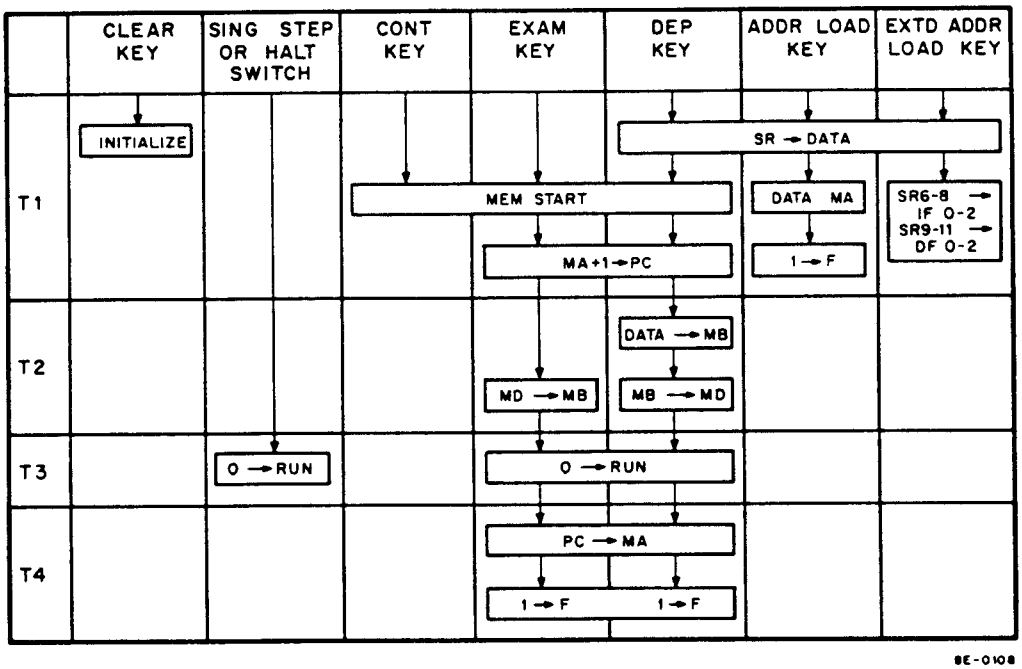


Figure 3-68 Manual Operation Function, Flow Diagram

3.33.1 KC8-EA Programmer's Console

3.33.1.1 Manual Operation

Switch Register — The switch register consists of 12 switches that enable the operator to load the processor CPMA Register with a 12-bit memory address, to deposit a 12-bit data word in a selected memory location, and to load the extended address bits, if more than 4K of memory is used. To carry out these functions, the switch register is operated in conjunction with the DEP, ADDR LOAD, and EXTD ADDR LOAD keys, as indicated on the block diagram.

Figure 3-69 illustrates the logic and circuits used to set data into the switch register and to place it on the DATA 0—11 lines; the circuit used with switch register bit 0 is shown in detail. If switch S11 is open (in the up position on the front panel), a positive voltage is applied to one input of NAND gate E25. If a positive enabling voltage is

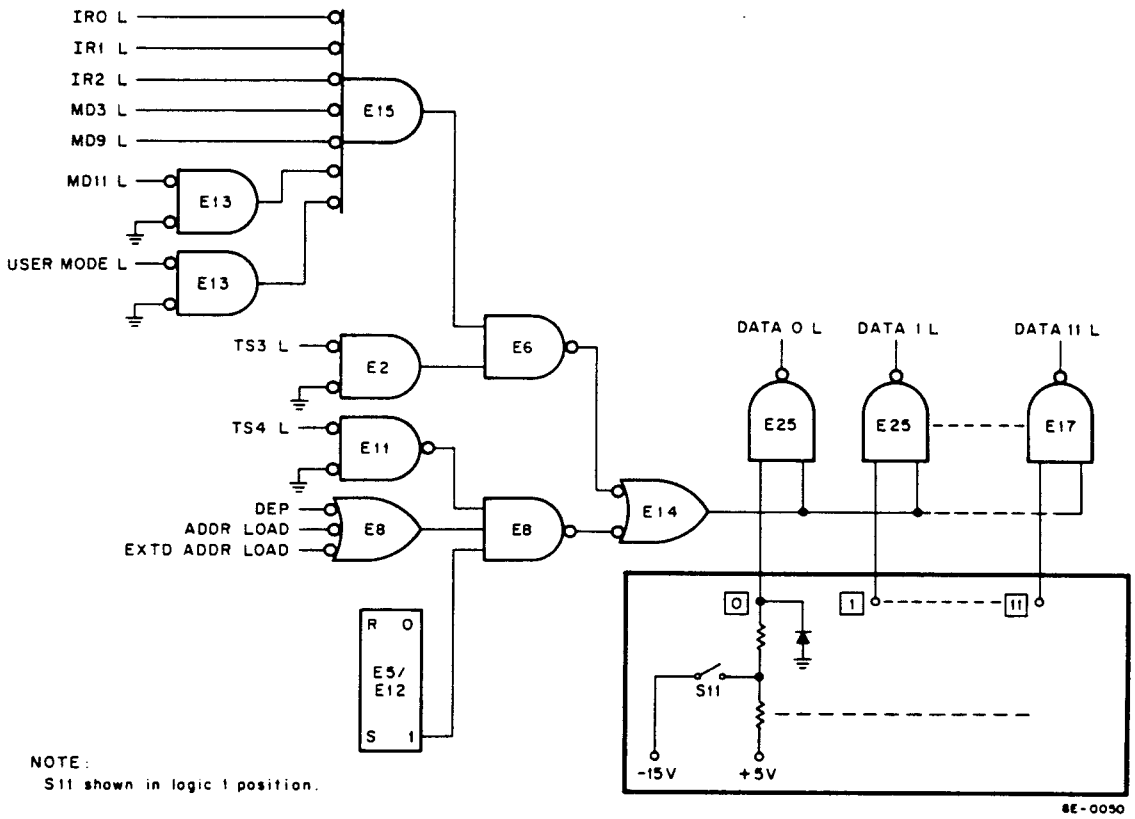


Figure 3-69 Switch Register Control Logic

applied at the other input, the DATA 0 line will go to ground, thereby indicating a logic 1. When the switch is closed, the diode in the circuit begins conducting. The resulting voltage drop across the diode takes the diode cathode below ground potential, inhibiting the NAND operation. The DATA 0 line remains at a positive voltage level, indicating a logic 0.

The NAND operation of E25 can be enabled by NOR gate E14 in either of two ways: (a) If the machine is stopped, the DEP, LOAD, or EXTD ADDR LOAD key can be activated. This action enables gate E25 and all of the other enable gates. (The DATA lines are reserved during TS4 for priority checking by peripherals; NANDing TS4 L ensures that no switch register information appears on the DATA lines during this time state.) (b) The OSR (inclusive OR, switch register with AC) instruction or the LAS (load AC with switch register) instruction can be issued, thereby enabling the gates at TS3, provided the USER MODE line has not been asserted by the KM8-E Memory Extension and Time Share option.

ADDR LOAD Key and EXTD ADDR LOAD Key – The ADDR LOAD key is used to load the CPMA Register with the memory address specified by the switch register. When the operator depresses this key, switch register information is placed on the DATA 0–11 lines. At the same time, LA ENABLE L and MS, IR DISABLE L are asserted. These two control signals enable a path for the DATA lines through the adder network to the MAJOR REGISTERS BUS. The PULSE LA signal is then asserted. This signal produces the CPMA LOAD L pulse, which loads the CPMA Register with the information on the DATA 0–11 lines. The memory location specified by the CPMA Register can then be operated on by the DEP key or the EXAM key.

Note, in Figure 3-68, that the ADDR LOAD key does not initiate a timing cycle. The purpose of this key is to establish a memory location at which some operation will take place. If a timing cycle is initiated, the CPMA address is incremented, and the operation takes place at the desired address plus 1. Thus, to avoid confusion, ADDR LOAD does not initiate a timing cycle.

The EXTD ADDR LOAD key, likewise, does not initiate a timing cycle. This key is used to load switch registers bits 6–11 into the Instruction Field (IF) and Data Field (DF) Registers of the KM8-E Memory Extension and Time Share option (bits 0–5 of the switch register are used for IOT designation and device selection code). When the operator depresses the EXTD ADDR LOAD key, the switch register information is placed on the DATA 0–11 lines. The LA ENABLE L and KEY CONTROL L signals are asserted, providing a path to the KM8-E option for the DATA 6–11 lines. The PULSE LA signal is then asserted, and the DF and IF Registers are loaded with the extended address information. The address specified by the CPMA Register and the DF and IF Registers can then be operated on by other keys.

Figure 3-70 shows the logic used by the ADDR LOAD and EXTD ADDR LOAD keys. When either key is depressed, NOR gate E14A is enabled. If the RUN L signal is negated, NAND E12A is also enabled (if RUN L is asserted, the computer is in automatic operation; E12A ensures that this operation is not inadvertently interrupted by key action). R/S flip-flop E5/E12, which is reset by INITIALIZE or by a previous TP4 pulse, is set when NAND E12B is enabled. The 1-side of the flip-flop is NANDed with positive voltage levels produced by key closure. Thus, LA ENABLE L, MS, IR DISABLE L, KEY CONTROL L, and SR → DATA are produced (note that LA ENABLE L asserts IND1 L and negates IND2 L, removing AC, MQ, or STATUS words from the DATA lines).

When NAND E12A is enabled, the block designated "pulse processor and delay network" also receives an initiating signal. This block, representing a noise filter, a differentiator, and a delay circuit, is discussed in detail in Paragraph 3.33.1.2. Essentially, the network generates a noise-free logic gate of 400 ns duration when activated. The start of the gate is delayed approximately 20 ms from the time the key is depressed, thus filtering out contact noise and allowing preliminary operations to be completed before PULSE LA is generated. The gate is NANDed with the positive voltage level that results from key closure. The amount of time that the key remains closed is indeterminate, being a result of operator action; however, it is much longer than the gate duration. Thus, PULSE LA is asserted for 400 ns.

DEP Key – If the operator wants to deposit data in a particular location of the basic 4K memory, he first loads the address into the CPMA, as described above. Then he sets the switch register switches to correspond to the data to be deposited, and lifts the DEP key. As the flow diagram in Figure 3-68 shows, the switch register data is placed on the DATA 0–11 lines. At the same time two control signals, MS, IR DISABLE L and KEY CONTROL L, are asserted. KEY CONTROL L selects the MA lines for gating into one leg of the adder network, while MS, IR DISABLE L provides an arithmetic 0 at the other adder input. KEY CONTROL L also asserts the CAR IN L signal, thus incrementing the CPMA Register. Some milliseconds later, MEM START L is asserted, the RUN flip-flop is set, and a timing cycle begins. At TP1 time the PC Register is loaded with the next consecutive memory address (note that the nonincremented address remains in the CPMA Register until TP4 of the cycle).

During TS2 of the timing cycle, the adder control signals enable a path through the adder network for the DATA 0–11 lines, adding an arithmetic 0 to each DATA bit. The switch register information is placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. This same TP2 pulse causes the MD DIR L signal to be negated, placing the MB Register data on the MD 0–11 lines. The data is then read into the memory location specified by the content of the CPMA.

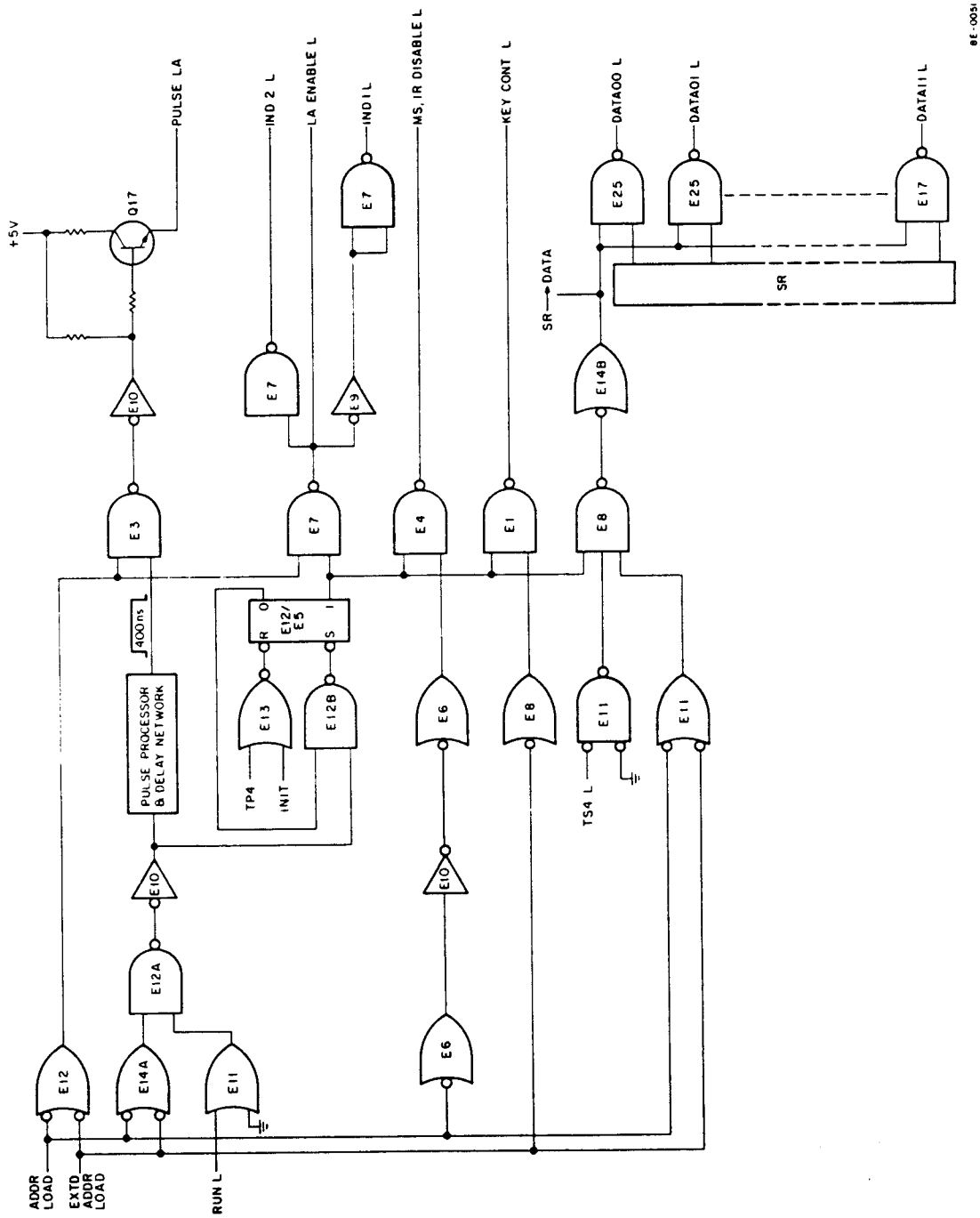


Figure 3-70 LOAD and EXTD LOAD Keys

At TP3 time, the KEY CONTROL L signal generates a STOP L signal, which resets the RUN flip-flop. The timing continues through TS4 and TP4 to halt in TS1 of some as yet unspecified cycle. Before completion of the cycle, one other operation is performed. The consecutive address must be transferred from the PC Register to the CPMA Register. Thus, the PC is gated to one leg of the adder, a 0 is added to each bit, and the new address is placed on the MAJOR REGISTERS BUS and loaded into the CPMA Register at TP4. The cycle then ends.

Figure 3-71 shows the logic used when a timing cycle is initiated by the DEP key. Again, flip-flop E5/E12 is set, provided that the RUN L signal is negated. The 1 side of E5/E12 is NANDed with positive voltage levels produced by the key closure, thereby asserting KEY CONTROL L, MS, IR DISABLE L, and SR → DATA. After the 20 ms delay, a 400 ns MEM START L signal is produced, which sets the RUN flip-flop. KEY CONTROL L enables TP3 to reset the RUN flip-flop; thus, only one cycle is produced.

EXAM Key – The EXAM key also initiates a timing cycle. By depressing this key, the operator can cause the contents of a selected memory location to be brought from memory and loaded into the MB Register. Except for the absence of SR → DATA, TS1 operations are identical to those of the DEP key. KEY CONTROL L and MS, IR DISABLE L are asserted. However, the EXAM key asserts two signals that are not needed by the DEP key and, therefore, TS2 operation is different. MD DIR L and BRK DATA CONT L are the additional signals. BRK DATA CONT L gates the MD lines to the adder network, where a 0 is added to the data being brought from the memory location. The MD bits are placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. The operator can monitor the contents of the MD lines by selecting the MD position with the front panel function selector switch. The data in the examined location can be modified by using the switch register and the DEP key. However, the EXAM cycle increments the PC Register to set up the next sequential memory address; therefore, to modify the data in an examined location, the switch register and ADDR LOAD key must be used to return to the correct address.

Figure 3-72 shows the EXAM key logic. This logic differs from the DEP logic only in the deletion of the SR → DATA enabling gate and the addition of enabling gates for MD DIR L and BRK DATA CONT L.

CONT Key – The CONT key also initiates a timing cycle by generating MEM START L. This is an important function because this is the only key that initiates repetitive timing cycles. Thus, the operator can begin automatic operation only by depressing the CONT key. Figure 3-73 shows the logic used to implement this function.

CLEAR Key – The last key on the Programmer's Console is the CLEAR key. As the flow diagram indicates, a timing cycle is not initiated. The logic diagram, Figure 3-74, shows that this key generates a 400 ns INITIALIZE signal. This signal clears the AC, LINK, and all peripheral flags.

SING STEP Switch and HALT Switch – The PDP-8/E can be stopped manually by either the SING STEP switch or the HALT switch. The logic is shown in Figure 3-75. Either switch enables TP3 to reset the RUN flip-flop, ending the generation of timing cycles. Both switches produce the STOP L signal, which is NANDed with TP3 in the timing logic. The resulting pulse resets the RUN flip-flop. If the SING STEP switch is used, the timing cycle halts at the beginning of the next TS1. However, the HALT switch produces the STOP L signal only when F SET L is asserted. Because F SET L is asserted only when the next machine cycle is to be a FETCH cycle, the processor completes an entire instruction before halting in TS1. The operator can use these switches, with the CONT key, to step a program one cycle or one instruction at a time.