part 2

PDP-8/E OPTIONS

CHAPTER 7

PDP-8/E OPTIONS

GENERAL

Chapter 7 contains descriptions of all the standard peripheral devices that are optionally available for the PDP-8/E computer. Section 1 deals with the mechanical expansion options. Section 2 covers the computer internal options. Section 3 describes the OMNIBUS input/output equipment options. Section 4 is concerned with the external bus input/output equipment options.

SECTION 1 MECHANICAL EXPANSION OPTIONS

Included in this section are those options which affect the external physical properties of the PDP-8/E computer, such as cabinets and panels. Further details regarding installation of these options appear in Chapter 11 of this handbook.

SYSTEM EXPANDER BOXES

Type BA8-AA System Expander Box

The BA8-AA includes a power chassis assembly and OMNIBUS assembly, capable of accommodating up to 20 PDP-8/E modules, and a BC08H-3F Cable Set (three and a half feet in length) with rack-mountable slides included, as well as a Type KC8-EB blank front panel.

Type BA8-AB System Expander Box

The BA8-AB includes a power chassis assembly and OMNIBUS assembly, capable of accommodating up to 20 PDP-8/E modules, and a BC08H-3F Cable set (three and a half feet in length) with table-top cover included, as well as a Type KC8-EB blank front panel.

Type BE8-A OMNIBUS Expander

The BE8-A includes an additional OMNIBUS assembly, capable of accommodating up to 20 PDP-8/E modules, together with M935 Bus Connectors for expanding either the PDP-8/E, the BA8-AA, or the BA8-AB to 38 slots.

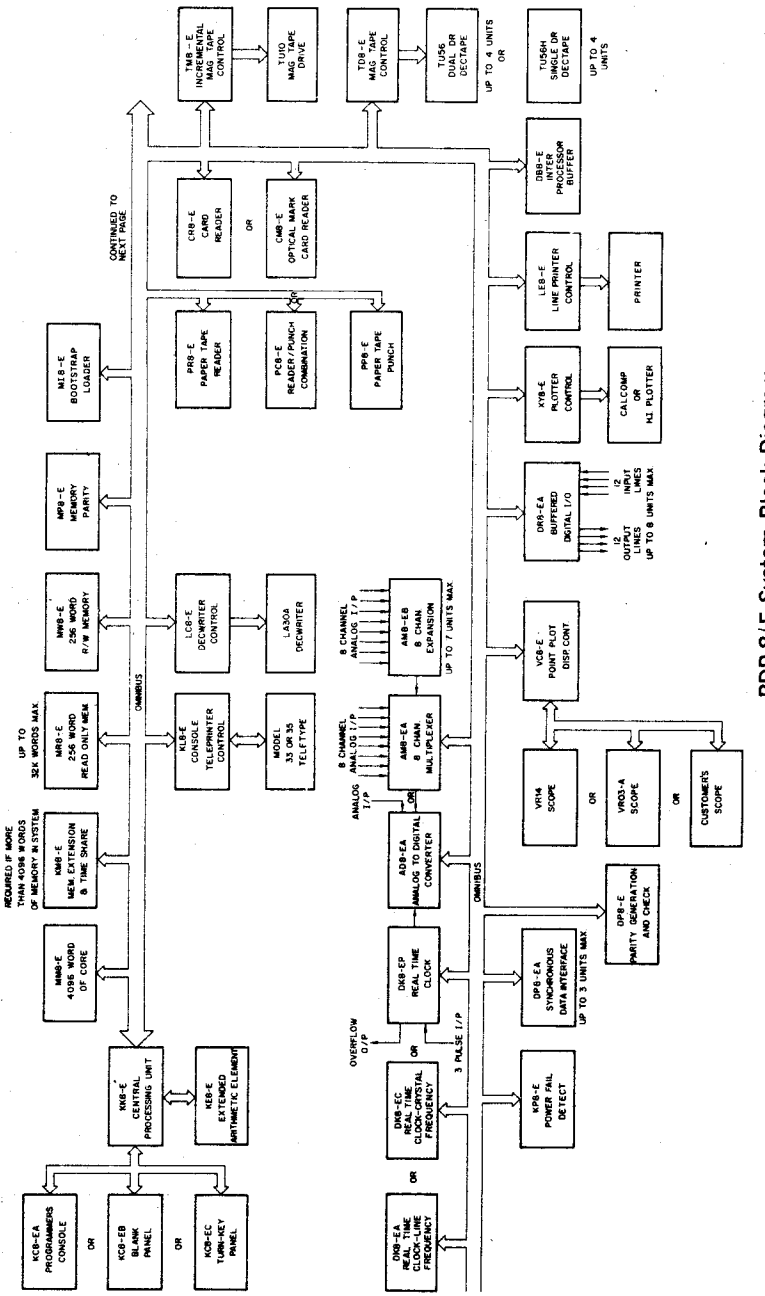
PANEL OPTIONS

Type KC8-EC Turn-Key Front Panel

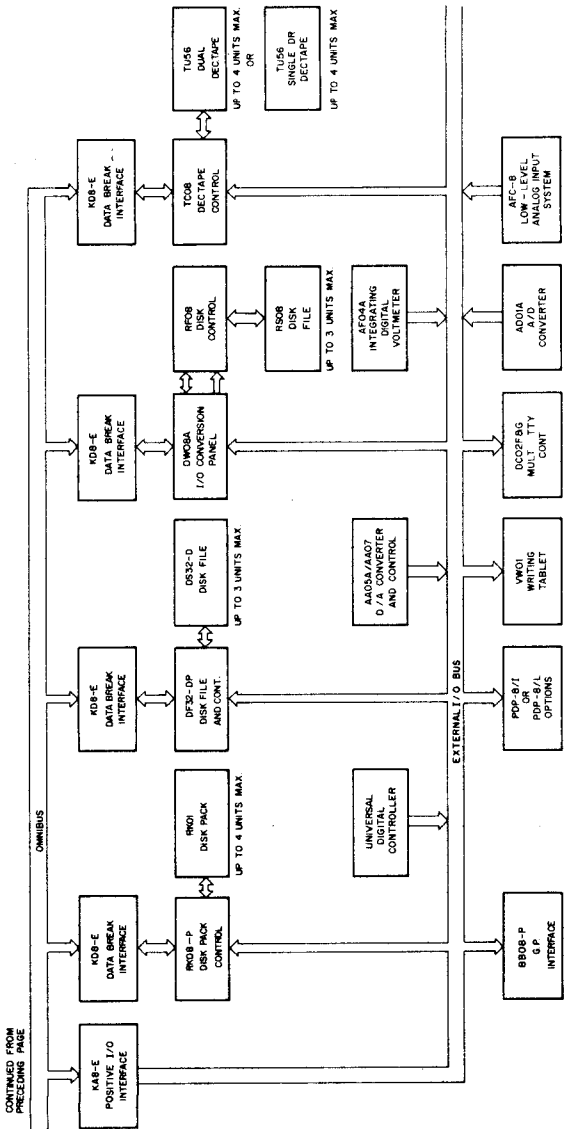
The KC8-EC panel contains a key-lock ON/OFF switch for controlling the application of power to the PDP-8/E system. The KP8-E Power Fail option is a prerequisite for using this panel. It is used as an alternate panel to the PDP-8/E.

Type KC8-EB Blank Front Panel

This panel can be used in place of the KC8-EA panel or the KC8-EC panel on the PDP-8/E, and is supplied with the BA8-AA or BA8-BA Expander Box option. It is used on the PDP-8/E when the system is equipped with a KP8-E, and the user wishes to switch power externally.



PDP-8/E System Block Diagram



PDP-8/E System Block Diagram (Continued)

SECTION 2 COMPUTER INTERNAL OPTIONS

This section deals with internal options for the PDP-8/E computer, including those concerned with the extended arithmetic facility, memory equipment, real-time measurement, and power fail detection and restart.

Many of these are covered in greater detail in Chapters 3 and 4 of this handbook.

The execution time for IOT instructions in this section is 1.2 μs, except where otherwise specified in the instructions for extended arithmetic.

TYPE KE8-E EXTENDED ARITHMETIC ELEMENT (EAE)

The KE8-E option plugs into the PDP8-E OMNIBUS to enable the central processor to perform arithmetic operations at high speeds by incorporating the EAE components with the existing central processor logic so that they operate asynchronously. This two-module option consists of circuits that perform parallel arithmetic operations on positive binary numbers, and includes:

a. A 5-bit Step Counter (SC) Register. This register is used to record the number of steps performed, and stops many EAE instructions after the correct number of operations. For these instructions, the SC is automatically loaded, and the instruction is terminated when the SC becomes a fixed number. There is one instance, the normalize (NMI) instruction, when the SC is of interest to the programmer. For this reason, instructions allow the programmer to load the SC from memory or the AC, depending upon the mode of operation; and to transfer the contents of the SC to the AC for storage upon interrupt or for program analysis.

b. A 4-bit instruction register (EAE IR)—This register consists of flip-flops set to MB (6,8-10) during the Fetch cycle of an EAE instruction.

c. The EAE timing and control logic—all EAE logic is contained in two modules which plug into the OMNIBUS. The KE8-E EAE logic circuits are used in conjunction with the accumulator (AC), link (L), multiplier quotient (MQ), and memory buffer (MB), though asynchronously with them to perform arithmetic operations. When this option is added to a PDP-8/E system, a class of instructions is added to the Group 3 Operate instruction list.

d. A mode flip-flop which controls the instruction set of the EAE. The mode flip-flop is set to mode A when power is applied to the machine, when the CLEAR key on the panel is operated, and when the CAF instruction is issued.

PROGRAMMING

The Extended Arithmetic Element (EAE) microinstructions are specified by an operate instruction (operation code 7) in which MB(3) and MB(11) always contain binary 1's. The instruction set is arranged so that programs written for the PDP-8/I EAE can be run on the PDP-8/E without modification. A greatly expanded instruction set is also available for new programming.

Two modes of operation, hereafter designated Mode A and Mode B, are available. Mode A, which is the mode in which the computer starts, is the PDP-8/I compatible mode.

COMMON OPERATIONS

Several EAE operations may be executed in either mode of operation. The common features of these operations are describd below.

Two-word instructions

Many EAE instructions require more than 12 bits. For these instructions, a second 12-bit word is obtained from the next location in memory. The second word is interpreted by the EAE hardware, and used either as an argument or the address of an argument. Program resumes at the location following the second word.

Multiplication

The Multiply instruction is a two-word instruction. The multiplier is either the second word or is located in the address specified by the second word, depending upon the mode. The contents of the MQ are multiplied by the multiplier and the 24-bit result is left in the AC (most significant bits), and MQ. The multiplication is an unsigned integer multiply, i.e. the multiplier and multiplicand are treated as 12-bit positive numbers with binary point at the right-hand end of the word. The binary point of the product is at the right-hand end of the MQ. If the AC is non-zero at the start of the multiply, its contents are added to the product. The Link is cleared. The SC is used in the execution of this instruction.

Division

The Divide Instruction is a two-word instruction. The division is either the second word or is located in the address specified by the second word. The contents of the AC (most significant bits) and MQ are divided by the divisor, and the quotient and remainder are left in the MQ and AC respectively. The division is an unsigned integer divide. The Link is cleared if the first subtraction produces a negative result, indicating that divide overflow has not taken place. If the first subtraction produces a positive result, the Link is set (indicating overflow) and the division is terminated. The contents of the AC and MQ are modified if divide overflow occurs. Ordinarily, the divide instruction is followed by a test of the Link to check for overflow before more computation occurs. The SC is used in the execution of this instruction.

Left Shift

The Link, AC and MQ are treated as one long register. The previous content of the Link is lost, AC0 is shifted into the Link, MQ0 is shifted into AC11, and zero enters the vacated MQ11 position. The second word of the two-word shift left instruction is loaded into the SC and thus defines the number of shifts to be performed.

Logical Right Shift

The Link is first cleared, then the AC and MQ, but not the Link are treated as one long register. MQ11 is either lost or shifted into the GT flag (depending on the mode). AC11 is shifted into MQ0, and the state of the Link is loaded into AC0. This instruction effectively divides the number of the AC and MQ by two for each place shifted. As in Left Shift, the number of positions shifted is defined by the last five bits of the second word of the two-word instruction.

Arithmetic Right Shift

This operation is identical to Logical Right Shift, except that the Link is initially loaded with the content of AC0, maintaining the sign of the number in the vacated bits. Because a right shift means shifting the contents of the AC and MQ one place to the right for each place shifted, the value of the 24 bits is effectively divided by two in signed arithmetic.

Normalization

The Normalize instruction is typically used to cast out and to account for leading zeroes when performing floating-point arithmetic. The Step Counter is initially cleared; then the contents of the L, AC and MQ are shifted left, as described above under Left Shift, until AC0 and AC1 are different or until the 24 bits contained in AC and MQ contains the number $(6000\ 0000)_8$. The Step Counter is incremented once for each shift. Normalize instruction must not be "ORed" with other EAE operations. At the conclusion of the Normalize instruction, the Step Counter contains a number equal to the number of shifts that were required to perform the normalization and is the EXPONENT (the binary power of 2) the 24-bit number. Thus the normalize instruction converts the number in the AC and MQ into the format. $M*2^n$; where M is the new result in AC and MQ and n is the contents of the step Counter. (The asterisk is a commonly-used symbol for multiplication)

MODE CHANGING INSTRUCTIONS (All instructions take place in 1.2 μsec.)

Switch from A to B (SWAB)

Octal Code: 7431

Operation: If the mode flip-flop is "A", it is changed to "B". If the mode flip-flop is already B, no operation occurs.

Switch from B to A (SWBA)

Octal Code: 7447

Operation: If the mode flip-flop is "B", it is changed to "A". If the mode is already A, no operation occurs.

Mode A Instructions

EAE instructions are augmented instructions, and can be combined to perform non-conflicting logical operations, as indicated in Figure 7-1.

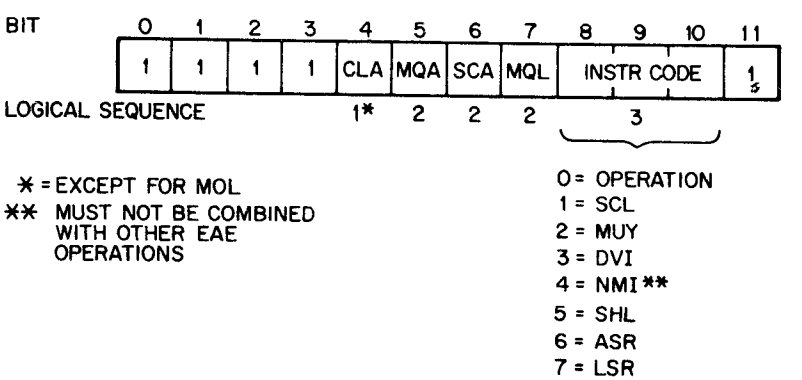


Figure 7-1 EAE Mode "A" Bit Assignments

The GT flag, explained in more detail under Mode B, is always zero for Mode A instructions. The instructions involving only bits 4, 5 and 7 have already been defined under Group 3 operate instructions in Chapter 3. For convenience, a summary of these instructions is given below. All execution times are 1.2 μs.

Mnemonic	Octal	Description
CAM	7621	0 → AC, O→MQ
MQA	7501	MQ "OR" ed with AC→AC
MQA CLA	7701	MQ→AC
MQL	7421	AC→MQ, O → AC
SWP	7521	AC→MQ, MQ→AC

The following Mode A instructions are added by the KE8-E hardware:

Step Counter "OR" with AC (SCA)
Octal Code: 7441
Execution time: 1.2 μs.
Operation: The contents of the Step Counter are "OR" ed with the five least-significant bits of the AC, and the result loaded into the AC.

Step Counter to AC (SCA CLA)
Octal Code: 7641
Execution time: 1.2 μs.
Operation: The contents of the Step Counter are loaded into AC 7-11. AC 0-6 are cleared.

Step Counter Load from Memory (SCL)
Octal Code: 7403
Execution time: 2.6 μs.
Operation: The next word in memory is treated as an operand. The one's complement of the last five bits of this operand are loaded into the Step Counter, and program resumes at the instruction word following the operand. The SCL instruction is most commonly used in interrupt servicing for restoration of the Step Counter.

Multiply (MUY)
Octal Code: 7405
Execution time: 7.4 μs.
Operation: The second word of this two-word instruction is the multiplier. Multiplication takes place as described above under "Common Operations"

Divide (DVI)
Octal Code: 7407
Execution time: 7.4 μs. if no divide overflow, 2.6 μs. if divide overflow.
Operation: The second word of this two-word instruction. Division takes place as described above under "Common Operations." Program resumes at the location following the divisor. If the Link = 1, at the conclusion of the division, divide overflow occurred; otherwise, the divide was legal.

Normalize (NMI)
Octal Code: 7411
Execution time: 1.5 + 0.3*N μs., where N is the number of shifts necessary to normalize.
Operation: The contents of AC and MQ are normalized, as described above under "Common Operations". This

command must not be combined with any other EAE commands. NMI "OR"ed with MQL is the SWAB instruction described under Mode Changing.

Shift Left (SHL)
Octal Code: 7413
Execution time: 2.6 + 0.3*N μs., where N is the number of shifts.
Operation: The number of shifts performed is equal to one more than the number in the last five bits of the second word. See "Common Operations" above for a description of Left Shift.

Arithmetic Shift Right (ASR)
Octal Code: 7415
Execution time: 2.6 + 0.3*N μs., where N is the number of shifts.
Operation: The number of shifts performed is equal to one more than the number in the last five bits of the second word. The old content of MQ11 is lost. See "Common Operations" above for a description of Arithmetic Right Shift.

Logical Shift Right (LSR)
Octal Code: 7417
Execution time: 2.6 + 0.3*N μs., where N is the number of shifts.
Operation: The number of shifts performed is equal to one more than the number in the last five bits of the second word. The old content of MQ11 is lost. See "Common Operations" above for a description of Logical Right Shift.

Mode B Instructions

Mode B differs from Mode A in the use of bit 6 of the instruction word, in the location of operands and in greatly increased double-precision arithmetic capability. As in Mode A instructions, these EAE instructions are able to be combined to form non-conflicting logical operations.
See Figure 7-2 for Mode B bit assignments.

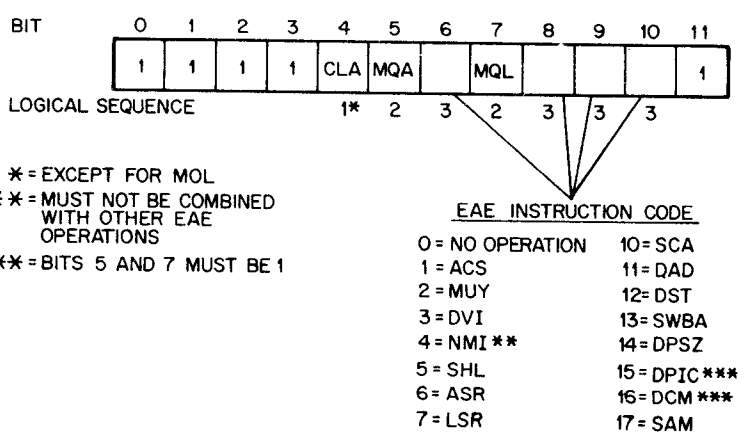


Figure 7-2 EAE Mode "B" Bit Assignments