IDENTIFICATION

Product Code:	MAINDEC-8/I-D5BB-D
Product Name:	DF32 DISCLESS Logic Test, MiniDisc
Date Created:	April 4, 1968
Maintainer:	Diagnostic Group
Author:	J. Hittell

1. ABSTRACT

Discless is a test of the DF32 disc logic and its computer interface. This program does not test the disc, nor associated analog interface circuits.

(The disc is not needed for these routines; if the disc is connected, the disc motor should be turned off. For a complete test of the disc system, use DF32 Disc Data Test.)

2. REQUIREMENTS

2.1 Equipment

Standard PDP-8/I Computer

DF32 Disc Logic
Light Card (for testing track selector)

2.2 Storage

The program occupies most of memory from address 100 to 3400 and locations 0, 1 and 2.

3. LOADING PROCEDURES

Procedures of normal binary tapes should be followed.

4. STARTING PROCEDURE

For normal operation all switches should be down.

4.1 Starting Address

The starting address for DF32 DISCLESS is 100.

Special Address	
76	Start for abnormal Print Out check
101	Start of Register Test
102	Start of shift, interrupt, error
103	DISC Memory Address Test SR=Address
104	DISC and Computer Extended Address Test SR=Address
105	DISC Data Memory Buffer SR=Data
106	Scope Loop SAD "FF"
107	Scope Loop SAP Pulse
110	Scope Loop ADC "FF"
111	Scope Loop SDP Pulse
112	Scope Loop DEP Pulse

113	Scope Loop TCR "FF"
114	Scope Loop IOT 66XX, SR=XX
115	Scope Loop Light Box AC 8, 9, 10 and 11=Track

4.2 Program and/or Operator Action

Turn disc motor off

Load Discless into memory

Select EM0 (DISC ZERO) (All other units to off)

Write Inhibit Switches off Set OPERATE/MAINT switch to MAINT

Connect Light Card if tracks are to be tested (not necessary for test)

Set the Switch Register to ~~37~~ 100

Load address

Set the SWITCH REGISTER to all zero (down)

Press START

Program will run; if the lightcard is used, lights will light from 0 to 17_8 in sequence and the program will loop upon completion.

5. OPERATING PROCEDURE

5.1 Operational Switch Settings

SW0	UP	Delete Print Out
SW1	UP	Halt After Error
SW2	UP	Sub Test Scope Loop
SW3	UP	Do not Exit Section
SW4	UP	Delete Light Box

There are three basic sections to loop on Interface test, Register test, Shift and Errors test.

When an error is detected and it is necessary to scope it, place SW1 UP to halt on the error, then SW2 UP to loop on it, then SW0 UP to delete printouts.

6. ERRORS

Logic hardware malfunctions detected by the program result in a type out, and a halt if SW2 is UP.

(If the light card is used, operator observance is necessary to detect an error.)

6.1 Error Halts and Description

Address Tag	Function Tested	Good (AC)	Bad (AC)	Corrective Action
603	START KEY CL(TRC)	0000	N/A	A15/B5/B19/B20
611	DSAC, 0 → AC	0000	7777	B18/D22
615	START KEY CL(ADC)	0000	N/A	B16/B5/B19/B18
622	START KEY CL(EMA)	0000	N/A	A21/B5/B19/see 1023
627	START KEY CL(EA)	0000	N/A	A21/B5/B19/see 1023
641	DOES WC BREAK	0000	7777	B29/A13/C15/C16/D22
641	DOES WC BREAK	0000	XXXX	B29/A13
645	DOES CA BREAK	0000	7777	C18 pin K
654	DMAW, 0 → AC	0000	7777	B18
663	DMAR, 0 → AC	0000	7777	B21/D10/D22
670	DMAC NOT SKIP	0000	N/A	B20/B19
676	DMAC, 0 → AC	0000	7777	B21
704	NO DRL STATUS	0000	0004	D20/A13
712	NO NED STATUS	0000	0002	B22/C20/B18/B20/ D18/D19
723	NO FLAG AFTER WRITE	0000	N/A	A19/B22/A15
726	NO FLAG AFTER WRITE	0000	N/A	A19/B22/A15
740	ADDRESS ACCEPT CL(DBR)	0000	0001	A13/B29
740	ADDRESS ACCEPT CL(DBR)	0000	XXXX	A13/B29
744	ADDRESS ACCEPT CL(DBR)	0000	XXXX	A13/B29
1010	NO FLAG AFTER READ	0000	N/A	A19
1013	NO FLAG AFTER READ	0000	N/A	A19
1023	DISC EXT. ADDRESS = 0	0000	XX00	B4/B1/B2/B3
1027	COMPUTER EXT. ADDRESS = 0	0000	0070	CD/23
1027	COMPUTER EXT. ADDRESS = 0	0000	00X0	B27/D20
1043	NO SYNC (PSM)	0000	400X	B18/D18/A30
1050	NO PARITY STATUS	0000	0001	A12/B15
1205	SEL ERROR STATUS	0000	N/A	B18/D19/D18/C20
1214	NO WLO (LOWER)	0000	N/A	A17/A12/C20/CHECK WLO SWITCHES
1225	NO WLO (UPPER)	0100	N/A	SAME AS ABOVE
1234	EM3 RAISE NEX	3000	N/A	D18/D19/B18/A30
1243	EM2 RAISE NEX	2000	N/A	D19/B2
1252	EM1 RAISE NEX	1000	N/A	D19/B1
1267	DISC EXT. ADDRESS = SEVEN	3700	0000	CD/23
1267	DISC EXT. ADDRESS = SEVEN	3700	XX00	B1/B2/B3/B4
1303	COMPUTER EXT. ADDRESS	0070	0000	CD/23
1303	COMPUTER EXT. ADDRESS	0070	00X0	D20/B27
1310	SKIP ON NO ERROR (READ)	0000	N/A	B20/C20/A20/B5/B26
** 1327	NO INTERRUPT	0000	N/A	D20/B22/A15
1405	SKIP ON DFSE (READ)	0000	N/A	B26/DIODE ON EM SELECT SWITCH
1413	SKIP ON DFSE (WRITE)	0402	N/A	B26/DIODE ON EM SELECT SWITCH
1420	SKIP ON DFSE (WRITE)	0000	N/A	B26/DIODE ON EM SELECT SWITCH
1504	RAISE (NED) STATUS	7002	7000	B22/B18/C20
1522	INTERRUPT ON (NED)	3000	N/A	D20/B22

*If light card is used (Sync) switch should be off.

*IF NO LIGHT CARD THEN THIS WILL ALWAYS FAIL

** ERROR IN PROGRAM CAUSES THIS TO ALWAYS FAIL

Address Tag	Function Tested	Good (AC)	Bad (AC)	Corrective Action
1534	CL PAR FF	3000	N/A	A20
1551	WILL (NED) SET (TRC)	7002	N/A	A19/A15/B19/B24
1616	DMA TEST	0000	XXXX	CD22/CD24/B5
1616	DMA BITS 0,1			B6/B12
1616	DMA BITS 2,3			B7/B12
1616	DMA BITS 4,5			B8/B12
1616	DMA BITS 6,7			B9/B13
1616	DMA BITS 8,9			B10/B13
1616	DMA BITS 10,11			B11/B13
1636	EMA TEST			
1636	EMA BIT 1	XX00	XX00	B1/B4
1636	EMA BITS 2,3	XX00	XX00	B2/B4
1636	EMA BITS 4,5	XX00	XX00	B3/B4
1636	EA BITS 6,7,8	XX00	XX00	B27/D20
1663	DMB TEST	XXXX	ALL	B19/A17/A22/B17/A21
		XXXX	0 to 5	B23
		XXXX	6 to 11	B24
1663	DMB BITS 0,1	XXXX	XXXX	A23/B23
1663	DMB BITS 2,3	XXXX	XXXX	A24/B23
1663	DMB BITS 4,5	XXXX	XXXX	A25/B23
1663	DMB BITS 6,7	XXXX	XXXX	A26/B24
1663	DMB BITS 8,9	XXXX	XXXX	A27/B24
1663	DMB BITS 10,11	XXXX	XXXX	A28/B24
2223	SHIFT DMA	1252	2525	A29/B5/B17/A16/A15/ B30
2223	SHIFT DMA	1252	XX52	B6/B7/B8
2223	SHIFT DMA	1252	12XX	B9/B10/B11
2244	SHIFT DMA	6525	XXXX	SAME AS 2223
2261	SHIFT DMA	7252	XXXX	SAME AS 2223
2301	SHIFT DMA	5525	XXXX	SAME AS 2223
2310	SKIP ON (ADC)	N/A	N/A	B16/A17/B15/B18
2341	SHIFT DMB	7777	ALI	A18/A21/A17
2341	SHIFT DMB	7777	XX77	A23/A24/A25/B23
2341	SHIFT DMB	7777	77XX	A26/A27/A28/B24
2430	SHIFT DMB	4000	XXXX	SAME AS 2341
2462	SHIFT DMB	5252	XXXX	SAME AS 2341
2515	SHIFT DMB	2525	XXXX	SAME AS 2341
2617	SHIFT DMA	5777	7777	B14/B15
2632	RAISE (DRL) STATUS	0004	0000	D20/A13
2635	SKIP ON DRL	0004	0004	C20
2641	WILL (DEP) SET (TRC)	N/A	N/A	A19
2653	INTERRUPT ON TRC	N/A	N/A	D20
2675	TRACK COUNTER (EMA)	3702	0000	B16/B19/B23
2675	TRACK COUNTER (EMA)	3702	XX00	B1/B2/B3
2705	TRACK COUNTER (EMA)	0000	XX00	