IDENTIFICATION

Product Code:	MAINDEC-08-D1B0-D
Product Name:	Memory Address Test
Date Created:	March 25, 1968
Maintainer:	Diagnostic Group
Author:	R. Green
Previous Code:	MAINDEC-08-D11A-D

PDP-8
LIBRARY

1. ABSTRACT

The Memory Address Test checks for proper memory address selection on the PDP-8.

2. REQUIREMENTS

2.1 Equipment

Standard PDP-8 Computer.

2.2 Storage

The low version occupies locations 0000-0222. The high version occupies locations 7400-7575, 0-3. The binary loader must be stored in the last memory page.

2.3 Preliminary Programs

It is assumed that the only malfunction is in the memory addressing circuits.

3. LOADING PROCEDURE

The program is supplied in RIM format.

4. STARTING PROCEDURE

4.1 Control Switch Settings

SR0 Halt after error printout.

4.2 Starting Addresses

0004
~~0000~~ Low Storage
7400 High Storage

4.3 Operator Action

a. Load the starting address into the program counter.
b. Set the SWITCH REGISTER to 4000, if halt on error is desired.
c. Push START.

5. OPERATING PROCEDURE

Same as section 4.

6. ERRORS

6.1 Error Printouts

Axxxx Cyyyy (Error printout format)

Axxxx. (Address). xxxx = Address containing the wrong data

Cyyyy. (Contents). yyyy = Contents of location xxxx.

The address should always equal the contents.

6.2 Error Recovery

Analysis of several error printouts should establish a meaningful pattern that will single out a particular address selector card.

If it is necessary to scope the problem, the following two instruction loop may be entered into memory by the operator.

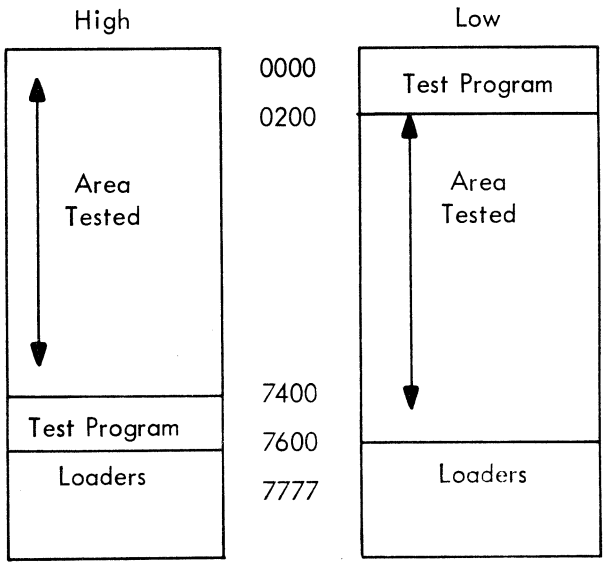
```
TAD [Bad Location]
JMP .-1
```

7. MISCELLANEOUS

7.1 Execution Time

An 11 is printed after every 96 complete program loops (every 28 seconds).

7.2 Memory Maps



8. PROGRAM DESCRIPTION

The program consists of four phases which occur in the following sequence.

Phase 1	Load memory sequentially in the forward direction, starting with the lowest address to be tested.
Phase 2	Read and check memory in the same manner as it was loaded in phase 1.
Phase 3	Load memory sequentially in the reverse direction, starting with the highest address to be tested.
Phase 4	Read and check memory in the same manner as it was loaded in phase 3.

In the load phases the contents of every location to be tested is set equal to its address. If the contents of an address are wrong, the contents specify the address which was in the MA register when the failure occurred. The address whose contents are wrong is the address that was selected in error.

Sample error printout:

A2560 C2760

Explanation - While attempting to write a 2760 into location 2760, the data was written into location 2560.