PROPERTY OF DIGITAL EQUIP

digital

KL8-J

Engineering Drawings

Digital Equipment Corporation

digital EQUIPMENT CORPORATION

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET ☐☐☐☐

SEQUENCE		SEQUENCE	
DRAWING DIRECTORY	B-DD-KL8-J		
TERMINAL CONTROL	D-CS-M8655-0-1		
ENGINEERING SPEC	A-SP-KL8-JA-1		
IN HOUSEFIELD SERV ACCEPT	A-SP-KL8-JA-2		
ACCESSORY LIST	A-AL-KL8-JA-4		

UNIT VARIATIONS

VAR	TITLE	PRINT SET 1	2	3	4
KL8-JA	TERM CONT/ASYNC DATA INT	X			

REVISIONS

REV	CHG. NO.	DATE

USED ON OPTION/MODEL	

SHEET 1 OF 2

DRW. L. Cook	DATE 1-9-74	TITLE TERM CONTROL/ ASYNC DATA INT
CHK'D L. Cook	DATE 1-4-74	
PROJ ENG. R. Regan	DATE 1/4/74	
PROG. D. DeRome	DATE 1/4/74	SIZE B · CODE DD · NUMBER KL8-J · REV
FIELD SERV. W Cook	DATE 1/4/74	DIST

DRB 106

CUSTOMER PRINT SET 1	2	3	4	SET MFG	FIRM NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
					1	A-PL-KL8-J-Ø	*	1	TERM CONT/ASYNC DATA INT	
X						A-SP-KL8-JA-1			ENGINEERING SPEC	
X						A-SP-KL8-JA-2			IN HOUSE AND FIELD SERV ACCEPT	
						A-SP-KL8-JA-3			PRODUCTION TEST PROCEDURE	
X						A-AL-KL8-JA-4			ACCESSORY LIST	
X					2	D-CS-M8655-Ø-1		4	TERMINAL CONTROL	
						K-CO-M8655-Ø-4		1	X-Y CO-ORDINATE HOLE LOC	
						D-AH-M8655-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
						B-MH-M8655-Ø-6		1	MODULE ECO HISTORY	

CUSTOMER PRINT SET				SET MFG	FIRM NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO / FILE DATE

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE		SIZE	CODE	NUMBER	REV
TERM CONT/ASYNC DATA INT	SHEET 2 OF 2	B	DD	KL8-J	

NOTES:

1. 19-11969 (8640) MAY BE USED IN PLACE OF 19-11113 (11380).
2. FOR YA,YB,YC,YD VARIATIONS SEE SHEET 5 OF 5 FOR CRYSTALS. (REFERENCE KL8-A OPTION ALSO)

DEVICE CODE & SPEED SELECTION

"TRANSMIT"		"RECEIVE"
← 0	B3 / B1	← 0
← 0	R= 150= B2	← 0
← 0	(MD03)	← 0
← 0	(MD04)	← 0
← 0	(MD05)	← 0
1 →	(MD06)	← 0
← 0	(MD07)	1 →
← 0	(MD08)	1 →

(ARROWS INDICATE DEPRESSED SWITCH, ON = 1, OFF = 0. FOR THE EXAMPLE SHOWN, RECEIVE DEVICE CODE = 03, TRANSMIT DEVICE CODE = 04, AND SPEED = 110 BAUD)

R = 150
OFF – TRANSMIT & RECEIVE SPEEDS ARE THE SAME.
ON – TRANSMIT SPEED SET BY B1, B2, & B3 RECEIVE SPEED IS 150 BAUD.

B1	B2	B3	BAUD RATE
0	0	0	110
0	0	1	150
0	1	0	300
0	1	1	600
1	0	0	1200
1	0	1	2400
1	1	0	4800
1	1	1	9600
1	1	1	10000

← 1 = ON
0 = OFF

W2 IN, W3 OUT NORMAL SETTING
W2 OUT, W3 IN, SPECIAL UART CHIP REQUIRED

JUMPER DEFINITIONS

S2/S1 STOP BITS OUT = 2 STOP BITS IN = ONE
NP – NO PARITY OUT = NO PARITY IN = PARITY
EVN – EVEN PARITY OUT = EVEN IN = ODD
NB1 & NB2 – NUMBER OF DATA BITS/CHAR

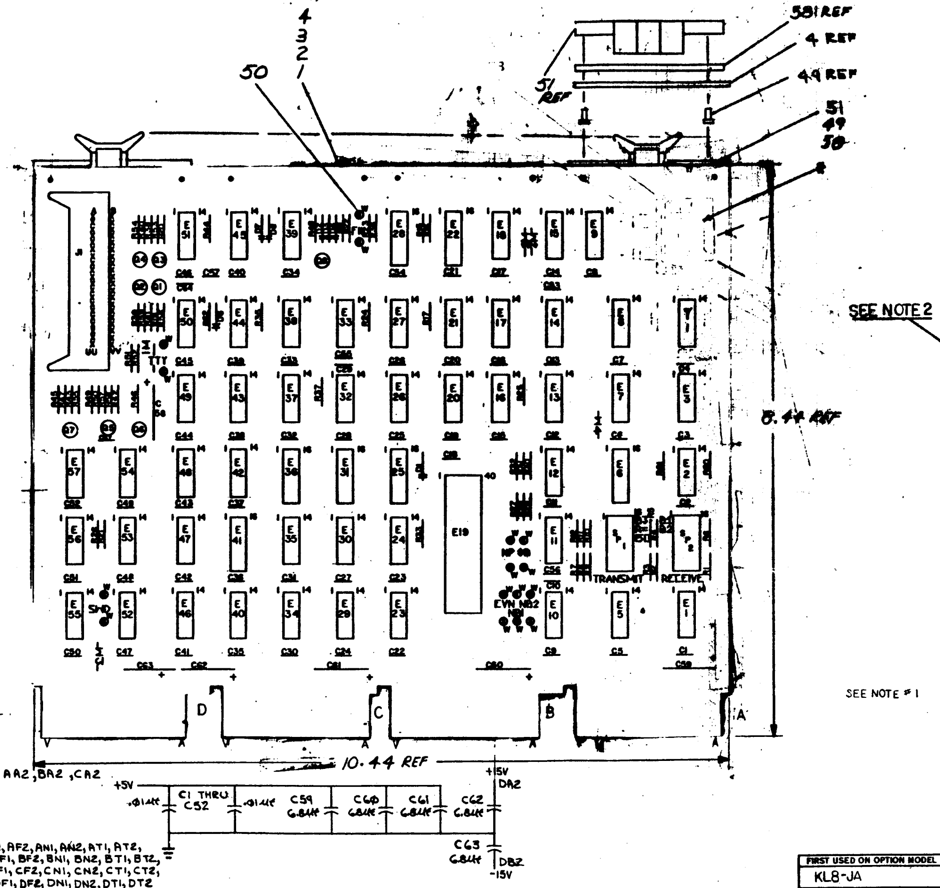
DATA BITS / CHAR	6	7	8	5
NB1	OUT	IN	OUT	IN
NB2	OUT	OUT	IN	IN

SWE/WD - STATUS WORD ENABLE OUT = DISABLE IN = ENABLE
FIL – FILLER CHARACTER ENABLE OUT = DISABLE IN = ENABLE (INSTALLED FOR VT05 OPERATION ABOVE 300 BAUD)
TTY/W1 - TELETYPE FILTER OUT = DISABLE IN = ENABLE (INSTALLED FOR 110 BAUD TELETYPE OPERATION ONLY)

IC TYPE	GND	+ 5V
IC 1808 UART -12V=2	3	1
IC 1488 -12V=1	7	42=14
IC 5380	1	8
IC 74175	8	16
IC 8266	8	16
IC 7442	8	16
IC 11380	1	8
IC 5384	1	8
IC 74151	8	16
IC 7493	10	5
IC 7492	10	5

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E6	I.C. DEC 7402	[illegible]	55
1	E30	I.C. DEC 1488L	[illegible]	56
1	E45	I.C. DEC 1489L	[illegible]	57
4		[illegible]	[illegible]	58
~~[illegible]~~		~~[illegible]~~	~~[illegible]~~	59

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-8655-Ø-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AM-8655-Ø-5	2
REF		MODULE ECO HISTORY	B-MH-8655-Ø-6	3
1		ETCHED CIRCUIT BOARD	5010614	4
3	C64, ~~[illegible]~~, C57, C67	CAP 330 PF 100V 5%	1000023	5
58	C1-C58	CAP .01 UF100V 20% AXIAL	1001610-00	6
1	C58	CAP 2.2 UF 35V 10%	1002431	7
5	C59 THRU C63	CAP 6.8 UF 35V 10%	1005306	8
8	D2 THRU D5, D7, D8	DIODE D664	1100114	9
2	D1, D6	DIODE ZENER 1N4742	1109502	10
~~2~~		~~CRYSTAL SOCKET [illegible]~~	~~[illegible]~~	11
2	E8, E20	I.C. SOCKET	1210025	12
1	J1	CONN 40 PIN	1209941	13
2	SP1, SP2	SWITCH (DIP 8 BIT)	1211164-04	14
2		SWITCH COVER	1211284-04	15
9	R48 THRU R52	RES 47 1/4W 5%	1300202	16
6	R44-R47, R53, R60	RES 68 1/4W 5%	1300219	17
1	R62	RES 150 1/4W 5%	1300250	18
2	R60, R61	RES 220 1/4W 5%	1300271	19
22	R23-R30, R18, R35-R43	RES 1K 1/4W 5%	1300365	20
3	R56-R58	RES 3.3K 1/4W 5%	1300430	21
19	R15-R17, R19-R22, R1-R12	RES 10K 1/4W 5%	1300479	22
2	R54, R55	RES 6.8K 1/4W 5%	1301423	23
3	Q1, Q2, Q7	TRANS MPS A05	1510705	24
5	Q3, Q4, Q5, Q6, Q8	TRANS MPS A55	1510706	25
1	Y1	OSCILLATOR 5.0688MHZ	1811660-02	26
7	E20, E27, E39, E42, E48, E56, E57	I.C. DEC 7474	1905547	27
5	E3, E21, E38, E40, E54	I.C. DEC 7400	1905575	28
1	E47	I.C. DEC 7410	1905576	29
1	E28	I.C. DEC 7430	1905578	30
1	E46	I.C. DEC 7440	1905579	31
2	E36, E37	I.C. DEC 7402	1909004	32
6	E8, E14, E15, E17, E18, E44	I.C. DEC 7493	1909054	33
3	E16, E32, E49	I.C. DEC 7404	1909006	34
2	E13, E53	I.C. DEC 8815	1900713	35
1	E38	I.C. DEC 8266	1909034	36
1	E22	I.C. DEC 74151	1909036	37
5	E11, E23, E29, E33, E34	I.C. DEC 97401	1909073	38
1	E7	I.C. DEC 7408	1910011	39
3	E1, E2, E5	I.C. DEC 8242	1909712	40
1	E41	I.C. DEC 7442	1910046	41
~~1~~	~~[illegible]~~	~~I.C. DEC 5380~~	~~[illegible]~~	42
3	E10, E12, E46	I.C. DEC 5384	1910394	43
1	E19	I.C. DEC 1800 (UART)	1910459-1	44
2	E25, E31	I.C. DEC 74175	1910651	45
5	E24, E30, E51, E52, E55	I.C. DEC 11380	1911113	46
~~2~~		~~PH SCREW #2-56 X 1/4 IN~~	~~[illegible]~~	47
~~2~~		~~HEX NUT #2-56~~	~~[illegible]~~	48
8		EYELET #GS4-11	9006750	49
16		SPLIT LUG	9006755	50
4		HANDLE FLIP CHIP (MAGENTA)	9008337-08	51
~~1~~		~~[illegible] REAR SUPPORT BRACKET~~	~~[illegible]~~	52
~~1~~		~~[illegible] CRYSTAL HOLDER BRACKET~~	~~[illegible]~~	53
A/R	W2, W3, W4	BUS WIRE #22GA	9107580-01	54

PARTS LIST

ETCH BOARD REV B

FIRST USED ON OPTION MODEL: KL8-JA

DEC NO.	EIA NO.	DEC NO.	EIA NO.
		A05	NONE
		A55	NONE
		1N4742	SAME
		D664	1N3606

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.			CHK
B	M8655-00001A	B. REGAN	H. Benemore 9-23-74	El Read 10-9-74
C	M8655-00002	B. REGAN	H. Benemore 5-21-76	R. Regan 6-4-76

REVISIONS

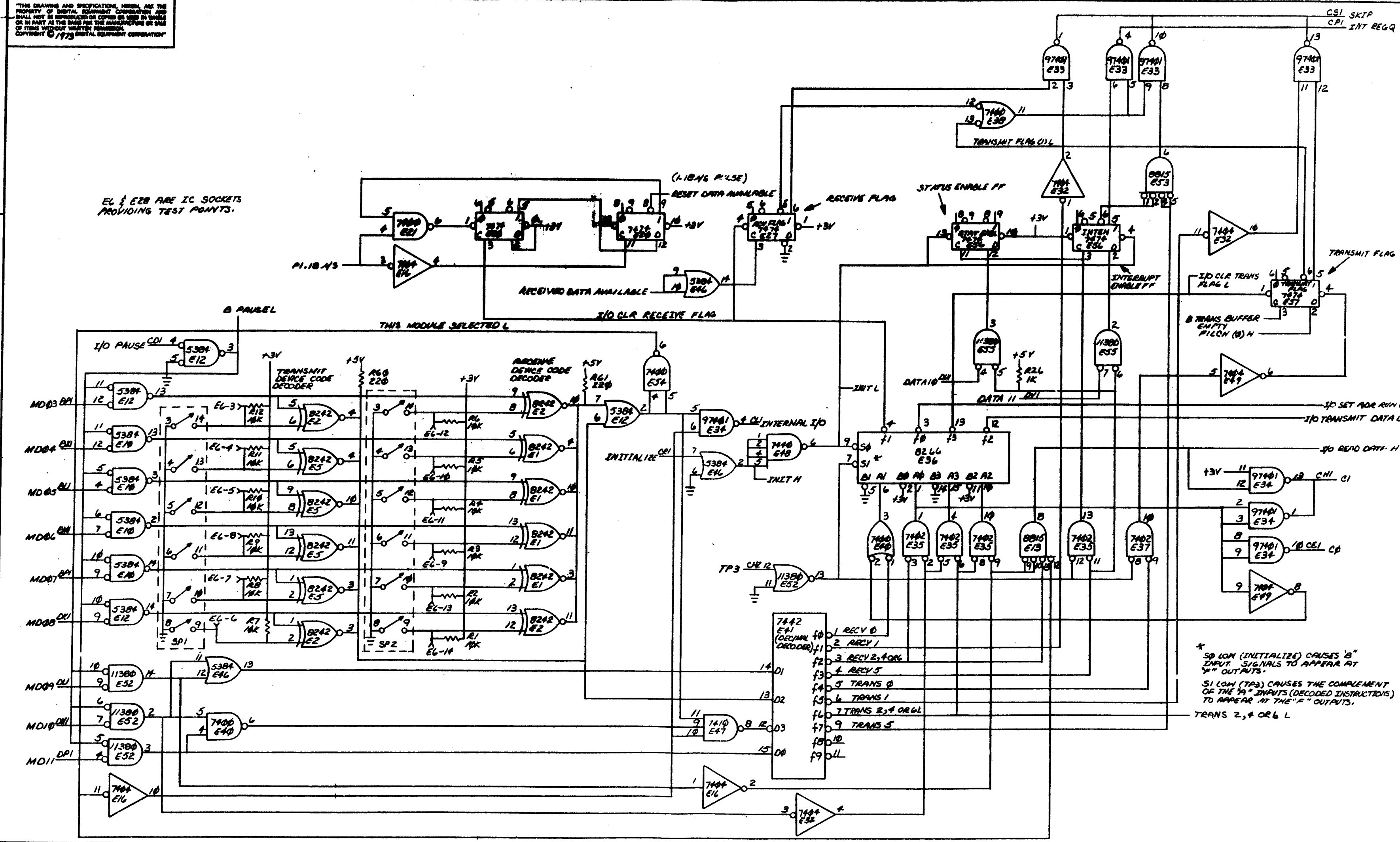
DRN. M. Pierce DATE 8-1-73
CHK'D. [illegible] DATE 9-26-73
ENG. R. Regan DATE 10-1-73
PROJ. ENG. R. Regan DATE 10-1-73
PROD. [illegible] DATE 10-1-73
NEXT HIGHER ASSY B-DD-KL8-JA-Ø
SCALE NONE
SHEET 1 OF 5

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TERMINAL CONTROL

SIZE D CODE CS NUMBER M8655-Ø-1 REV. C

DEC FORM NO. DRD-135A


EL & E28 ARE IC SOCKETS PROVIDING TEST POINTS.
* S0 LOW (INITIALIZE) CAUSES "B" INPUT SIGNALS TO APPEAR AT "F" OUTPUTS.
S1 LOW (TP3) CAUSES THE COMPLEMENT OF THE "A" INPUTS (DECODED INSTRUCTIONS) TO APPEAR AT THE "F" OUTPUTS.
TRANSMIT DEVICE CODE DECODER
RECEIVE DEVICE CODE DECODER
RECEIVE FLAG
TRANSMIT FLAG
STATUS ENABLE FF
INTERRUPT ENABLE FF
RESET DATA AVAILABLE
RECEIVED DATA AVAILABLE
I/O CLR RECEIVE FLAG
THIS MODULE SELECTED L
I/O PAUSE
B PAUSE L
INITIALIZE
INTERNAL I/O
INIT H
INT L
DATA 10
DATA 11
I/O SET ADR RUN L
I/O TRANSMIT DATA L
I/O READ DATA H
I/O CLR TRANS FLAG L
B TRANS BUFFER EMPTY FILCN (0) H
TRANSMIT FLAG (1) L
CSI SKIP
CPI INT REQ
TRANS 2,4 OR 6 L
RECV 0
RECV 1
RECV 2,4 OR 6
RECV 5
TRANS 0
TRANS 1
TRANS 2,4 OR 6 L
TRANS 5
7442 E41 (DECIMAL DECODER)
8266 E36
TP3
MD03
MD04
MD05
MD06
MD07
MD08
MD09
MD10
MD11
P1.18 A/3
(1.18 µS PULSE)

REVISIONS		
CHK	CHANGE NO.	REV.

(INSTRUCTION DECODING & FLAGS)

TITLE	TERMINAL CONTROL	SIZE	CODE	NUMBER	REV.
SCALE	SHEET 2 OF 5	D	CS	M8655-Ø-1	C

NOTE:
1. SIGNAL NAMES SUCH AS P1.08 µS ARE INTERPRETED AS FOLLOWS:
1.08 µS 1.08 µS

FF TO SYNC TIMING BETWEEN TWO MODULES ON B/E XOR TESTER

E6 & E28 ARE IC SOCKETS PROVIDING TEST POINTS.

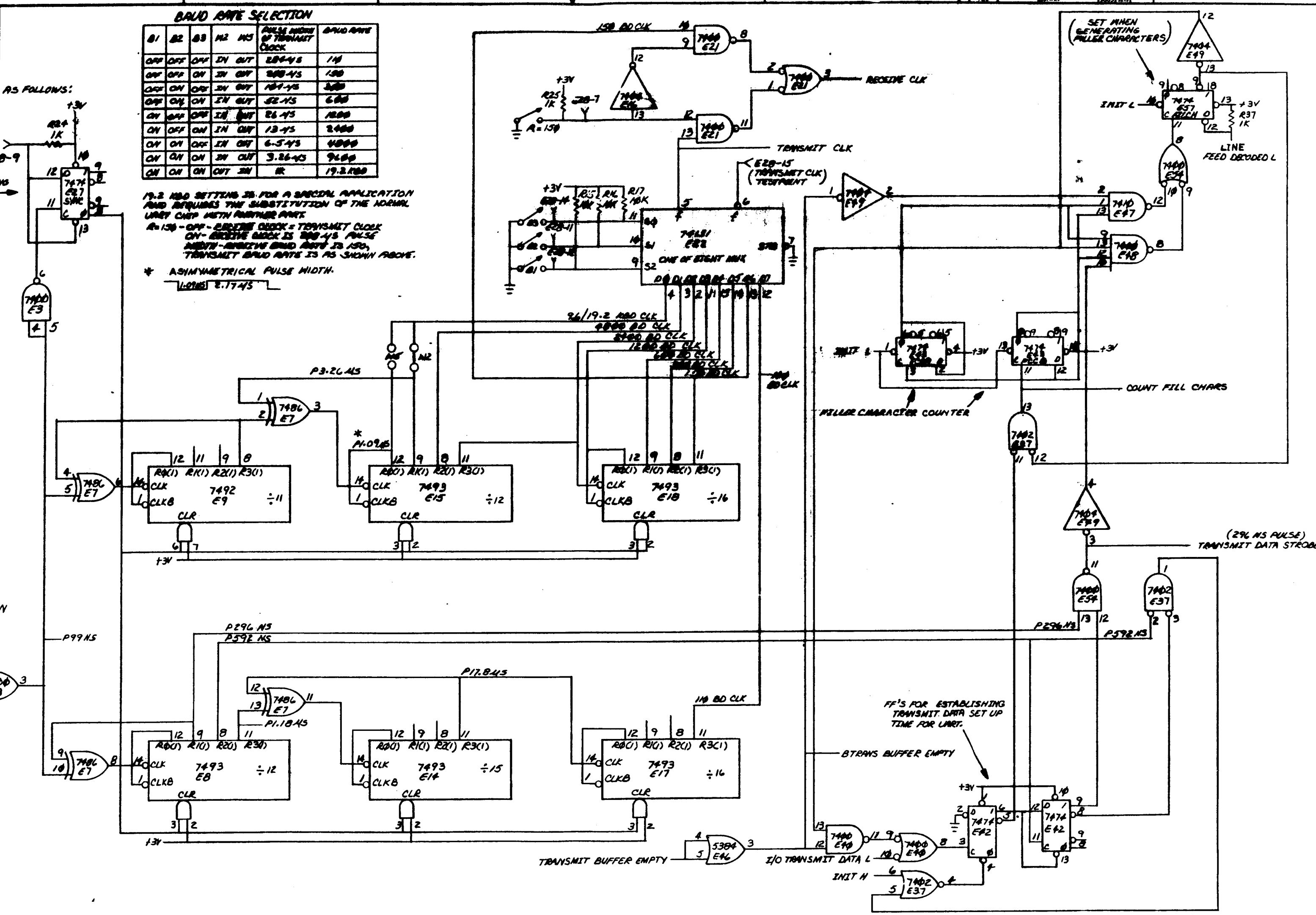
BAUD RATE SELECTION

B1	B2	B3	M2	M5	PULSE WIDTH OF TRANSMIT CLOCK	BAUD RATE
OFF	OFF	OFF	IN	OUT	284 µS	110
OFF	OFF	ON	IN	OUT	208 µS	150
OFF	ON	OFF	IN	OUT	104 µS	300
OFF	ON	ON	IN	OUT	52 µS	600
ON	OFF	OFF	IN	OUT	26 µS	1200
ON	OFF	ON	IN	OUT	13 µS	2400
ON	ON	OFF	IN	OUT	6.5 µS	4800
ON	ON	ON	IN	OUT	3.26 µS	9600
ON	ON	ON	OUT	IN	*	19.2 KBD

19.2 KBD SETTING IS FOR A SPECIAL APPLICATION AND REQUIRES THE SUBSTITUTION OF THE NORMAL UART CHIP WITH ANOTHER PART.

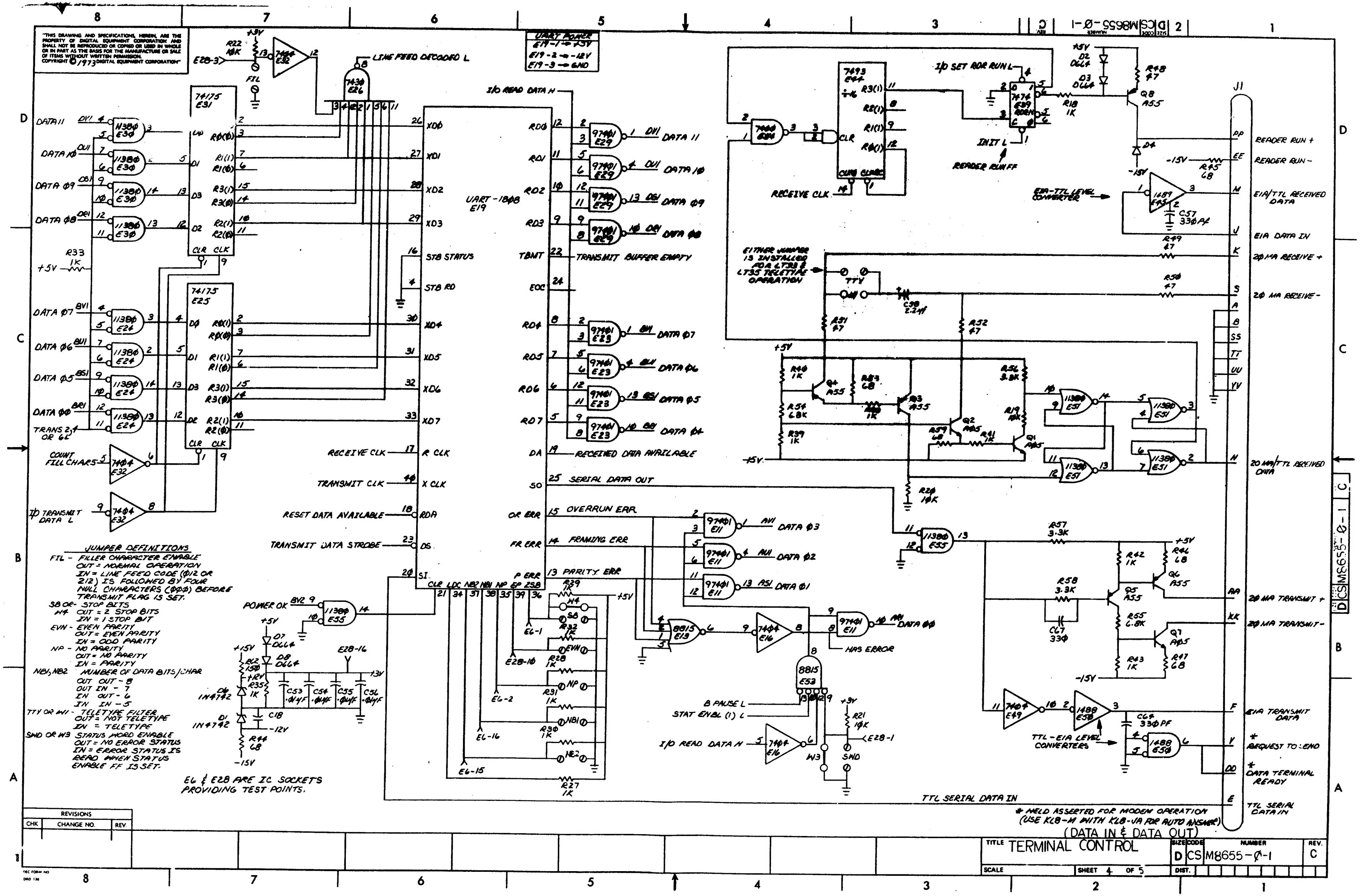
R=150 - OFF - RECEIVE CLOCK = TRANSMIT CLOCK
ON - RECEIVE CLOCK IS 208 µS PULSE WIDTH - RECEIVE BAUD RATE IS 150, TRANSMIT BAUD RATE IS AS SHOWN ABOVE.

* ASYMMETRICAL PULSE WIDTH.
1.09 µS 2.17 µS


150 BD CLK
7400 E21
RECEIVE CLK
TRANSMIT CLK
E28-15 (TRANSMIT CLK) TESTPOINT
74151 E82 ONE OF EIGHT MUX
96/19.2 KBD CLK
4800 BD CLK
2400 BD CLK
1200 BD CLK
600 BD CLK
300 BD CLK
110 BD CLK
P3.26 µS
P1.09 µS
7492 E9 ÷11
7493 E15 ÷12
7493 E18 ÷16
7493 E8 ÷12
7493 E14 ÷15
7493 E17 ÷16
P99 µS
P296 µS
P592 µS
P17.8 µS
P1.18 µS
Y1 5.0688 MHZ
CLK OUT ENABLE H E28-5
TEST CLK OUT E28-8
TEST CLK IN E28-4
TEST SYNC E28-9
SET WHEN GENERATING FILLER CHARACTERS
INIT L
LINE FEED DECODED L
COUNT FILL CHARS
FILLER CHARACTER COUNTER
(296 µS PULSE) TRANSMIT DATA STROBE
BTRANS BUFFER EMPTY
FF'S FOR ESTABLISHING TRANSMIT DATA SET UP TIME FOR UART.
TRANSMIT BUFFER EMPTY
I/O TRANSMIT DATA L
INIT H

REVISIONS		
CHK	CHANGE NO.	REV.

(TIMING & FILLER CHARACTER GENERATION)
TITLE TERMINAL CONTROL
SIZE D CODE CS NUMBER M8655-Ø-1 REV. C
SCALE SHEET 3 OF 5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UART POWER
E19-1 → +5V
E19-2 → -12V
E19-3 → GND
LINE FEED DECODED L
UART-1808 E19
I/O READ DATA H
DATA 11
DATA 10
DATA Ø9
DATA Ø8
DATA Ø7
DATA Ø6
DATA Ø5
DATA Ø4
DATA Ø3
DATA Ø2
DATA Ø1
DATA ØØ
TRANS 2,1 OR 6L
COUNT FILL CHARS
I/O TRANSMIT DATA L
TRANSMIT BUFFER EMPTY
RECEIVED DATA AVAILABLE
SERIAL DATA OUT
OVERRUN ERR
FRAMING ERR
PARITY ERR
RECEIVE CLK
TRANSMIT CLK
RESET DATA AVAILABLE
TRANSMIT DATA STROBE
STB STATUS
STB RD
POWER OK
HAS ERROR
B PAUSE L
STAT ENBL (1) L
I/O READ DATA H
I/O SET RDR RUN L
INIT L
READER RUN FF
EIA-TTL LEVEL CONVERTER
TTL-EIA LEVEL CONVERTERS
EITHER JUMPER IS INSTALLED FOR LT33 & LT35 TELETYPE OPERATION
TTL SERIAL DATA IN
READER RUN +
READER RUN -
EIA/TTL RECEIVED DATA
EIA DATA IN
20 MA RECEIVE +
20 MA RECEIVE -
20 MA/TTL RECEIVED DATA
20 MA TRANSMIT +
20 MA TRANSMIT -
EIA TRANSMIT DATA
* REQUEST TO SEND
* DATA TERMINAL READY
TTL SERIAL DATA IN
JUMPER DEFINITIONS
FIL - FILLER CHARACTER ENABLE
OUT = NORMAL OPERATION
IN = LINE FEED CODE (Ø12 OR 212) IS FOLLOWED BY FOUR NULL CHARACTERS (ØØØ) BEFORE TRANSMIT FLAG IS SET.
SB OR H4 - STOP BITS
OUT = 2 STOP BITS
IN = 1 STOP BIT
EVN - EVEN PARITY
OUT = EVEN PARITY
IN = ODD PARITY
NP - NO PARITY
OUT = NO PARITY
IN = PARITY
NB1, NB2 NUMBER OF DATA BITS/CHAR
OUT OUT - 8
OUT IN - 7
IN OUT - 6
IN IN - 5
TTY OR W1 - TELETYPE FILTER
OUT = NOT TELETYPE
IN = TELETYPE
SND OR W3 STATUS WORD ENABLE
OUT = NO ERROR STATUS
IN = ERROR STATUS IS READ WHEN STATUS ENABLE FF IS SET.
E6 & E28 ARE IC SOCKETS PROVIDING TEST POINTS.
* HELD ASSERTED FOR MODEM OPERATION (USE KL8-M WITH KL8-JA FOR AUTO ANSWER)
REVISIONS
CHK
CHANGE NO.
REV.
TITLE TERMINAL CONTROL
(DATA IN & DATA OUT)
SIZE D
CODE CS
NUMBER M8655-Ø-1
REV. C
SCALE
SHEET 4 OF 5
DIST.

M8655 VARIATION TRANSLATION TABLE

B1 B2 B3	M8655 OSCL 5.0688 MHz. DEC #18-11660-02 CLK PULSE WD/BAUD RATE	M8655-YA OSCL 4.433 MHz. DEC #18-11660-11 CLK PULSE WD/BAUD RATE	M8655-YB OSCL 3.0737 MHz. DEC #18-11660-09 CLK PULSE WD/BAUD RATE	M8655-YC OSCL 2.619 MHz. DEC #18-11660-08 CLK PULSE WD/BAUD RATE
OFF OFF OFF	284 USEC/110	326 USEC/N/A	488 USEC/88.7	538 USEC/58.8
OFF OFF ON	208 USEC/150	238 USEC/N/A	343 USEC/N/A	482 USEC/N/A
OFF ON OFF	104 USEC/300	119 USEC/N/A	171 USEC N/A	201 USEC/N/A
OFF ON ON	52 USEC/600	59.6 USEC/N/A	86 USEC/N/A	100 USEC/N/A
ON OFF OFF	26 USEC/1200	29.8 USEC/1050	43 USEC/N/A	50.5 USEC/N/A
ON OFF ON	13 USEC/2400	14.9 USEC/N/A	21.4 USEC/N/A	25.1 USEC/N/A
ON ON OFF	6.5 USEC/4800	7.45 USEC/N/A	10.7 USEC/N/A	12.6 USEC/N/A
ON ON ON	3.26 USEC/9600	3.62 USEC/N/A	5.37 USEC/N/A	6.35 USEC/N/A
ON ON ON	1.63 USEC/19.2 KBD *	1.87 USEC/N/A *	2.69 USEC/N/A *	3.17 USEC/N/A *

B1 B2 B3	M8655-YD OSCL 3.419 MHz DEC #18-11660-10 CLK PULSE WD/BAUD RATE
OFF OFF OFF	421 USEC/74.2
OFF OFF ON	408 USEC/N/A
OFF ON OFF	154 USEC/N/A
OFF ON ON	77 USEC/N/A
ON OFF OFF	38 USEC/N/A
ON OFF ON	19 USEC/N/A
ON ON OFF	9.6 USEC/N/A
ON ON ON	4.8 USEC/N/A

NOTE: DIFFERENTIATION BETWEEN M8655, YA, YB, YC AND YD MODULES IS THE XTAL SELECTION.

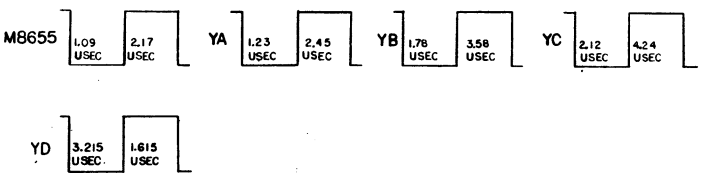
*W2 OUT, W5 IN FOR THESE CLOCK PULSES—W2 IN W5 OUT FOR ALL OTHER CASES.

PULSE NAME TRANSLATION TABLE

SIGNAL NAME (ORIGINATING PIN)	PULSE WIDTH FOR M8655	PULSE WIDTH FOR M8655 YA	PULSE WIDTH FOR M8655 YB	PULSE WIDTH FOR M8655 YC
P99 NSEC (E63-03)	99 NSEC	143 NSEC	163 NSEC	192 NSEC
P296 NSEC (E66-09)	296 NSEC	339 NSEC	489 NSEC	573 NSEC
P592 NSEC (E66-06)	592 NSEC	677 NSEC	976 NSEC	1.14 MICROSEC
P3.26 MICROSEC (E15-09)	3.26 MICROSEC	3.74 MICROSEC	5.39 MICROSEC	6.31 MICROSEC
P1.09 MICROSEC (E15-12)	*1.09 MICROSEC	*1.23 MICROSEC	*1.78 MICROSEC	* 2.12 MICROSEC
P17.8 MICROSEC (E14-11)	17.8 MICROSEC	20.2 MICROSEC	29.3 MICROSEC	33.4 MICROSEC

SIGNAL NAME (ORIGINATING PIN)	PULSE WIDTH FOR M8655-YD
P99 NSEC (E63-03)	146 NSEC
P296 NSEC (E66-09)	438 NSEC
P592 NSEC (E66-06)	877 NSEC
P3.26 MICROSEC (E15-09)	4.83 USEC
P1.09 MICROSEC (E15-12)	1.615 USEC
P17.8 MICROSEC (E14-11)	26.3 USEC

*ASYMMETRICAL PULSE WIDTH



NOTE: THIS TABLE IN REFERENCE TO SHEET 3 OF M8655 LOGIC DIAGRAM.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: TERMINAL CONTROL
SIZE: D | CODE: CS | NUMBER: M8655-0-1 | REV: C
SCALE | SHEET 5 OF 5 | DIST.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 9/25/73

TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
Bob Regan	R. Regan	A	SP	KL8-JA-1	

DEC 16-(393)-1079-N971
DRA 107

ENGINEERING SPECIFICATION CONTINUATION SHEET

TITLE KL8-JA TERMINAL CONTROL/ASYNCHRONOUS DATA INTERFACE

1.0 Scope

This document specifies the KL8-JA, its use a: operating characteristics.

2.0 Applications

The KL8-JA serves as data interface between an Omnibus type PDP8 computer (including PDP8's with DW8-E bus converters) and any asynchronous external device with electric lly compatible data leads and one of the many serial data for ats* available with the KL8-JA.

IOT instruction device codes for the KL8-JA are established at the time of system integration allowing up to seventeen (17) external devices to be interfaced, using KL8-JA's, to one PDP8. (Two device codes are used for each KL8-JA (Switch Selectable)).

The KL8-JA also provides reader control signals for use with LT33DC and LT33DD model teletypes and optionally generates filler characters for use with VT05 terminals.

*Serial Data Format - Transmit and receive speed of device and character configuration, i.e., number of data bits, control bits and parity bits.

3.0 Operation - Functional

The function of the KL8-JA in the simplest terms is to take parallel data presented to it by the CPU, convert it to a serial data format, transmit the character one bit at a time to an external device and vice-versa.

3.1 PDP8/M8655 Operation (Double Buffering)

Data transfers occur between the PDP8's Accumulator (AC) and registers within the M8655. In some earlier asynchronous data interfaces the shift registers which communicate with the external device also serve as communication links between the interface and CPU. When receiving a character, the receive flag would be set when a character had been assembled. The character, however, remained available only

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	

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DRA 109

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until the next character began to be assembled. The KL8-JA being double buffered, has an additional register between the receiver shift register and the AC. In this case, a character is assembled in the shift register and transferred to the "receive holding register" at which time the receive flag is set indicating that a character is available. The character remains available to the CPU in the holding register until the next character is completely assembled allowing the program roughly an order of magnitude more time to react to a receive flag and read a character.

In the transmission of data with earlier interfaces, time was lost between the transmission of characters since the shift register had to be completely empty before the transmit flag was set and the next character transmission wouldn't start until the CPU (program) got around to issuing another character. Double buffering in this case ("transmit holding register" between the AC and transmit shift register) eliminates this lost time since the transmit flag is set (indication to the CPU that another character may be issued to the interface) when the holding register to shift register transfer has been made. To maintain full speed transmission of characters, the CPU must only react to the transmit flag within one character time to refill the holding register.

3.2 M8655/External Device Operation & Serial Data Format

3.2.1 Data Leads

Section 2.0 referred to electrically compatible data leads. The KL8-JA provides two types of data leads for different applications: 20 mA and EIA leads (choice is made by cable selection).

The 20 mA circuits represent the binary information as a switch connected to a power source, i.e., switch open = "1", switch closed = "0". The 20 mA data circuits on the M8655 are active. The power source for both the transmit and receive circuits is on the M8655. For an external device to be electrically compatible, its transmit and receive

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	

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circuits must be passive (no power added to the 20mA lines). (More technical information in section 4.5 on cabling.)

The EIA data leads represent binary data as one of two voltage levels. When using these lines, EIA (Electronics Industry Association) specification RS232-C must be adhered to.

3.2.2 Serial Data Format

KL8-JA/external device operation is asynchronous (a character or string of characters may begin at any point in time) and full duplex (transfers may occur in both directions simultaneously).

Where data is transferred serially, all definitions concerning that data are made with respect to time. Baud rate is the rate at which these decisions may be made. (Baud rate is the total possible bits/second.)

A data line may be in one of two states - mark or space. In the idle state (no data being transferred), the line is in the mark state. To signify to the receiving unit that a character is coming, the line changes to the space state for 1/baud rate seconds (start bit). This is followed by the data (5 to 8 data bits, LSB first). If parity is used, it appears after the most significant bit. This is followed by a return to the idle state which lasts for 1, 1.5 or 2 bit times (stop bit(s)). The next character may occur at any time after that. Following are the character definitions applicable to the KL8-JA.

Transmit Baud Rate - 110, 150, 300, 600, 1200, 2400, 4800, 9600 (Switch Selectable).

Receive Baud Rate - May be set equal to the t ansmit baud rat or 150 baud (Switch Selectable).

SIZE	CODE	NUMBER	REV
A	SP	KL8-JA-1	

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Start Bit - Always 1 per character

Data Bits - 5, 6, 7 or 8 (Jumper Selectable)

Parity - Even, odd or none (Jumper Selectable)
(Parity is inserted after most significant data bit.)

Stop Bits - Choice of 1 or 2 for 6, 7 and 8 data bits.
Choice of 1 or 1.5 for 5 data bits.
(Jumper Selectable)

3.3 Additional Options

3.3.1 Error Status Word

The error status word may be enabled by the insertion of jumper "SWD". Detected are parity, framing and overrun errors (see Programming section).

3.3.2 Filler Characters - VT#5

To operate at speeds above 300 baud, the VT#5 requires that filler characters be transmitted to it following any line feed character. Insertion of the "FIL" jumper on the M8655 causes four all zero characters to be automatically transmitted to the VT#5 following every line feed. The transmit flag is not set until the KL8-JA is ready to accept other data.

3.3.3 Reader Run

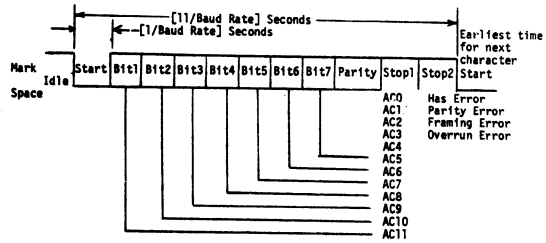
Reader control is provided for operating LT33 teletypes. See Programming section.

3.3.4 Teletype Filter

LT33 teletypes require a relatively large filter capacitor across the receiver lines. Installing the "TTY" jumper connects this capacitor.

SERIAL CHARACTER DEFINITION

Figure 1



The above example shows a character of one start bit, seven data bits, parity bit and two stop bits. Also shown is the relationship of the error status word to the AC bits.

4.0 Specifications

4.1 Physical

The M8655 meets the dimensional requirements for Omnibus type quad modules. Ref. D-MD-7605994 of the PDP8/E/F/M print set.

4.2 Power Requirements

From Omnibus - +5V at 1.1 Amps, -15V at 100 mA, +15V at 50 mA.
From external device - None

4.3 Environmental Requirements

Ambient temperature of M8655 - Operate between # and 55°C
Store between -15 and 65°C
Humidity - 10% to 90% non-condensing

4.4 System Configuration Restrictions

Maximum number of M8655's in one PDP8/E system - 17 or the power supply limit.

4.5 External Signals and Cabling Requirements

4.5.1 EIA signals

The EIA signals and their assigned pins on the 40 pin connector (Circuit Schematic Ref. J1) are as follows:

Signal Name	Pin at J1
Protective Ground	UU
Send Data	F
Receive Data	J
Request to Send	V (Held Asserted)
Signal Ground	VV
Data Terminal Ready	DD (Held Asserted)

(Received data after EIA to TTL level conversion is jumpered at cable, pins E and M). Since the "Request to Send" lead is held true, M8655's are suitable for

FULL DUPLEX operation only.

Modem Control may be accomplished when an M8655 is combined with a KL8-M (M8653).

Total cable length from KL8-JA to associated terminal or modem must not exceed 50 feet.

4.5.2 20mA Signals

The 20mA signals provided and their assigned pins at the 40-pin connector (Circuit Schmetic Ref. J1) and at the Mate-N-Lock end of a BC05-M cable are as follows:

Signal Name		Pin at J1	Pin at BC05-M
Transmit +		AA	5
Transmit -		KK	2
Receive +		K	7
Receive -		S	3
Reader Run +	For LT33	PP	6
Reader Run -	Operation Only	EE	4

(Received data after 20mA to TTL level conversion is jumpered at J1 pins E & H.)

The factors limiting the length of cable which may be attached to the 20mA circuits are: a) the total resistance which may be driven or, b) the total capacitance seen by the transmitter and receiver and the selected baud rate.

The following information will allow the user to calculate maximum cable distances:

Transmit + to Transmit - 700Ω
Receive + to Receive - 60 Ω
Reader Run + to Reader Run - 1220Ω

(LT33 reader circuit has 1KΩ resistance which leaves 220 for total cable resistance.)

Some Wire Resistances:

Wire Size	Ohms/1000 feet
26 AWG	40.81
24 AWG	25.67
22 AWG	16.14
18 AWG	8.05

Formula for calculating maximum distance due to cable capacitance and baud rate.

$$D_{max} = \frac{.3 \times 10^{-3}}{C_C \cdot Bd} - \left(\frac{C_T + C_R}{C_C}\right)$$

Where: D_{max} = maximum distance external device may be placed from KL8-JA.
C_C = capacitance of cable per foot.
Bd = baud rate.
C_R = Capacitance across the receiver circuit in question.
C_T = Capacitance across the transmitter circuit in question.

C_R for M8655 is 2.2 uf if TTY jumper is installed; ∅ if not.

C_T for M8655 is ∅.

C_R and C_T must be determined for external device.

Examples:

1. LT33 with reader.
The limiting factor in this case is the Reader Run circuit. Using 26 AWG cable, the maximum wire length is $\frac{220}{40.81\Omega}$/1000 feet or 5390 feet from Reader Run + to Reader-. Therefore the maximum cable length is 2695 feet.

2. High speed terminal (9600 bau with ∅ capacitance in either its transmitt or receiver. The limiting factor is cable apacitance. For this example cable capacitanc is 30 pf/ft.

$$D_{max} = \frac{.3 \times 10^{-3}}{30 \times 10^{-12} \; 9600} - \frac{\emptyset}{30 \times 10^{-12}} = \frac{.3 \times 10^{-3}}{.288 \times 10^{-6}} = 1040 \text{ ft.}$$

4.6 Module Setup - Jumpers and Switches

Refer to Dwg. D-CS-M8655-∅-1, Sheet 1.

5.0 Programming

5.1 Instruction Set

6XX∅ Clear keyboard flag (KCF)

Receiver flag is cleared without clearing the AC or enabling the reader.

6XX1 Skip if keyboard flag is set (KSF)
Increments the program counter to one location beyond the next sequential instruction if the receiver flag is set.

6XX2 Clear keyboard flag and set reader run (KCC)
Clear the receiver flag, and AC, and enable the reader.

6XX4 Read keyboard static (KRS)
Performs inclusive or of the receiver register and the AC leaving the result in the AC.

6XX5-AC11 Set/Clear Interrupt enable (KIE)
Loads AC bit 11 into the interrupt enable flip flop on the M8655. (1) = enable, (∅) = disable.

6XX5-AC10 Set/Clear status enable (KSE).
Loads AC bit 1∅ into status enable flip flop on M8655. (1) = enable, (∅) = disable. With SWD jumper installed, the status enable flop set causes the status word to be loaded into AC bits ∅-3 when a character is read (KRS or KRB inst.).

6XX6 Read keyboard buffer dynamic (KRB)
Performs the combined operations of KCC and KRS.

6YY∅ Set teleprinter flag (TFL)
Set the transmit flag.

6YY1 Skip on teleprinter flag (TSF)
Increments the contents of the program counter to one location beyond the next sequential instruction if the transmit flag is set.

6YY2 Clear teleprinter flag (TCF)
Clear the transmit flag.

6YY4 Load Teleprinter & Print (TPC)
The least significant bits of the AC are transferred to a data holding register on the M8655 and then transmitted. The transmit flag is not cleared by this instruction.

6YY5 Skip if teletype interrupt (SPI)
The next sequential instruction is skipped if the transmit or receive flag is set and the interrupt enable flip flop is set.

6YY6 Print character (TLS)
Combination of TCF and TPC performed.

5.2 Operation

5.2.1 Initialize

Initialize (key clear or CAF 6007 instruction) clears the receive flag, transmit flag and status word enable flip-flop, if applicable. It also sets the interrupt enable flip-flop.

Initialize does not reset the transmit or receive circuitry; i.e., if the M8655 were in the process of transmitting or receiving a character, the respective flag is set at the appropriate time despite the issuance of initialize. This circuitry is cleared only when power is first applied to the PDP8.

5.2.2 Status Word

This section applies only when the "SWD" jumper is installed on the M8655. (When this jumper is out, the read status logic is disabled.) Error status is read with the data bits when a read IOT is issued (KRS or KRB) if the status enable flip-flop was previously set.

AC∅ Inclusive or of the three error conditions. 1 = error.

AC1 Parity error (If PE jumper is not installed, this bit will always receive a zero.)

AC2 Framing Error = 1 if a legal stop bit was not detected (a space was detected half way through Stop Bit 1).

AC3 Overrun Error = 1 if the receive flag was not cleared prior to the character now being read (one character transmitted after another by the teletype without the first being read by the computer).

AC∅	AC1	AC2	AC3	AC4	AC5	AC6	AC7	AC8	AC9	AC10	AC11
Error	Parity Error	Framing Error	Overrun Error	MSB ← Data Bits →							LSB

AC After KRS or KRB Instruction With Status Enabled

5.2.3 Receive Flag

The receiver flag is cleared by key clear, or the CAF, KCF, KCC, and KRB instructions.

The receiver flag is set half way through the first stop bit of the characters being transmitted by the external device. This differs from the operation of earlier serial interfaces in that they did not look for framing errors and therefore could set the receiver flag half way through the most significant bit.

5.2.4 Reader Run

Reader Run is typically set when the previously read character is read into the AC. It is cleared when the start bit of the character to be read is detected. (Cleared half way through the start bit.)

5.2.5 Transmit Flag

The Transmit flag is cleared by initialize, or the TCF and TLS instructions.

The Transmit flag is set by the TFL instruction or anytime the Transmitter buffer is empty. (The transmission may or may not have occurred at this time.

When a character is to be transmitted to the external device, the character is received by the M8655, loaded into the transmit buffer, then loaded into the shift register from which the actual transmission occurs.

The first character being transmitted goes almost immediately from the transmit buffer to the shift register and the transmit flag is set. If another character is transferred from the computer at this time, the transmit flag is next set at the completion of the first transmission. (The transmit buffer is again empty.)

E. Set switches "RECEIVE"& "TRANSMIT" to the customer specified device codes as illustrated on sheet 1 of the circuit schematic.

F. Set baud rate as specified by customer as shown on sheet 1 of circuit schematic.

G. Install jumpers that are required by the customer. Parity, even parity, bits/character, fill characters TTY jumper and error status word. Ref. sheet 1 of circuit schematic.

H. Be sure power is off in PDP8 E/M/F and insert the M8655 into the omnibus according to PDP 8E maintenance manual Vol. 1 table 2-3.

III. Acceptance procedure

A. Load Maindec 08-DIKLA-A-PB (Loop Back Test) using normal binary loading procedures.

1. Run diagnostic according to the Maindec write-up Maindec 08-DIKLA-A-D.

2. Run at customers specified baud rate for 1 pass in 20 MA mode, and 1 pass in EIA mode. (See note 1) No errors are acceptable.

B. If the KL8-JA is shipped with a teletype, load Maindec #8-DIKLB-A-PB using normal loading procedures.

1. Run program 4 according to the maindec's write up, Maindec-#8-DIKLB-A-D.

2. No errors are acceptable.

C. If the KL8-JA is shipped with a VT05 load, Maindec 08-DGV5A-B-PB using normal binary loading procedures.

1. Run diagnostic for 1 complete pass according to the Maindec's writeup, Maindec 08-DGV5-B-D.

2. No errors are acceptable.

D. If the KL8-JA is shipped with a serial LA30, load Maindec-08-DHLAA-A-PB using normal binary loading procedure.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 9/24/73

TITLE KL8-JA FIELD SERVICE AND IN HOUSE ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG Bob Regan APPD Bill Cook SIZE A | CODE SP | NUMBER KL8-JA-2 | REV
DEC 16-COSD-1070-N0P1 DRA 107

1. Run diagnostic for 1 complete pass according to the Maindec's writeup, Maindec-08-DHLAA-A-D.

2. No errors are acceptable.

Note: 1 J1 connections for 20MA loop back test mode
E-H
K-KK
S-AA
J1 connections for EIA loop back test mode
E-M
F-J

I. Purpose

Define the procedure for installing and accepting the KL8-JA

II. Unpacking and Installation

A. Shipping Hardware

1. KL8-JA (M8655 Terminal Control/asynchronous interface)

B. Shipping Software

1. KL8-JA Print set

2. Maindec #8-DIKLA-A (KL8-JA LOOPBACK TEST)

3. Maindec #8-DIKLB-A (KL8-JA teletype test)

4. Maindec #8-DGV5A-B (VT05 terminal diagnostic)
Note: Shipped only if KL8-JA used as VT05 interface.

5. Maindec-#8-DHLAA-A (LA30 control/exerciser test)
Note: shipped only if KL8-JA used as LA30 interface.

C. Test hardware and software required.

1. PDP E/F/M with at least 4K R/W memory and a programmers console.

2. All applicable items listed under A and B above.

D. Unpack and inspect module for physical damage.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY R. Cook DATE 1-4-74	CHECKED R. Cook DATE 1-4-74	SECTION
ENG R. Ragan DATE 1/4/74	PROD D. Rowe DATE 1/4/74	ISSUED SECT.

LEGEND

- D DOCUMENT
- DN DOCUMENT CHANGE NOTICE
- PA PAPER TAPE ASCII
- PB PAPER TAPE BINARY
- PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION	KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	B-DD-KL8-JA	KL8-JA PRINT SET (LATEST REV)			
2	MAINDEC-08-DIKLB-A-D	KL8-JA TELETYPE TEST - DOCUMENT			
3	MAINDEC-08-DIKLB-A-PB	KL8-JA TELETYPE TEST/PAPER TAPE			
4	MAINDEC-08-DIKLA-A-D	KL8-JA LOOP BACK TEST DOCUMENT			
5	MAINDEC-08-DIKLA-A-PB	KL8-JA LOOP BACK TEST PAPER TAPE			

TITLE	ASSY. NO.	SIZE	CODE	NUMBER	REV.	ECO NO
TERMINAL CONTROL/ASYNC DATA INT	SHEET 1 OF 1	A	AL	KL8-JA-4		
		DIST.				