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DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		DATE 22 MARCH 78			
ENGINEERING SPECIFICATION					
TITLE KT8A FIELD INSTALLATION AND ACCEPTANCE PROCEDURE					
REVISIONS					
REV	DESCRIPTION	CHG NO	DATE	APPD BY	DATE
A	ECO CHANGE	00001	4-78	<i>R.B. Ryan</i>	5-3-78
B	ECO CHANGE	ML002	12-78	<i>R.B. Ryan</i>	12-78

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<p>I General</p> <p>This document will define the hardware requirements and tests to be performed to: #1) install, #2) configure and #3) accept a KT8-AA system or KT8-AB add-on to an existing system.</p> <p>Because the KT8-A Memory Management options has several possible hardware configurations, the Hardware Rules/Restrictions (appendix A), General Configuration Guide (appendix B) and Configuration Examples (appendix C) should be referenced before installing this option.</p> <p>A. If the KT8-AA was shipped as part of a system, refer only to the Acceptance procedure.</p> <p>B. If the KT8-AB is an add-on installation to upgrade an existing system, then refer to the Installation and Acceptance Procedures.</p>			
<p>II Hardware</p> <p>This section defines the required hardware to install and accept a KT8-A and also defines the three hardware designations of the KT8-A option.</p> <p>A. The KT can be installed and accepted on any 8A/420 or 620 machine.</p> <p>B. The K8A Programmer's Console is not required, as the KT diagnostics have a console package.</p> <p>C. Program loading media is via: Paper tape, Floppy, or RK85.</p> <p>D. The Three designations of the KT are as follows:</p> <ol style="list-style-type: none"> KT8A-A - the KT Memory Management option shipped as part of a system configured by a DEC Manufacturing facility. KT8A-B - the required hardware to upgrade an 8A/420 or 8A/620 system. The KT8-AC (M8317YB or YC) is part of this option. 			
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<p>III Installation</p> <p>Before proceeding with your installation refer to Appendix A and B to familiarize yourself with the rules and configurations. Also refer to the configuration example that most represents your particular installation.</p> <ol style="list-style-type: none"> Install all memory in the system, refer to Configuration guide (appendix B). Install the KT8-AB in any vacant OMNIBUS slot with an "E" connector. If the system is comprised of two (2) BA8C boxes and memory will be located in each box than install the M982B terminator module, in any available "E" connector of the box not containing the KT8-A (M8416). Now connect the cable (78-11411-1J) between the two berg connectors of the M8416 and M982B. 			
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<p>IV Acceptance</p> <p>The time to accept a KT8-A configuration depends upon the amount of memory installed.</p> <ol style="list-style-type: none"> Load and run the KT8-A Memory Management Test program. Maindec 88-DKTA-A, for five min. With NO errors. Load and run the Extended Address Test Maindec 88-DKMC-C, for one pass with NO errors. Load and run the Extended Memory Data and Checkerboard Test, Maindec 83-DKMA-D, for one pass with NO errors. To insure system integrity, load and build a DEC/X8 program using version 2, which will exercise up to 128K of memory. It is important that the program is build using the latest DEC/X8 modules. <p>NOTE: Reference should be made to the latest write-up for DEC/X8 (version 2) as further parameters must be inputted to support break devices.</p>			
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APPENDIX A	
HARDWARE RULES/RESTRICTIONS	
<ol style="list-style-type: none"> 1. Any OMNIBUS CPU (KK8A or KK8F) using a BA8C box (20 slot box) is acceptable. 2. The KT8-A system can only be configured using any combination of MM8AB (16K core) and MS8C (16K or 32K MOS) memories. NOTE: MM8AA, MR8A, MS8A, MM8E, MM8EJ and MR8F memories cannot be used to configure a KT8A system. 3. If the system is made up of MM8AB core memories (16K), then they must be modified per ECO MM8AB #7, refer to table 1 for instructions. 4. If the system is made up of MS8C type memories (16K or 32K MOS), then refer to table 2 for switch configuration. 5. The PDP/8E chassis cannot be used as part of a KT8-A system. 6. If Power Fail/Auto Restart and/or Bootstraps are required as part of the system, then a KM8-AC (M8317YB or YC) must be used with the Memory Extension and Timeshare option disabled via the jumper configuration in table 3. NOTE: The M8317 and M8317YA are incompatible with the KT8A system. 	
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TABLE 1 MM8-AB 16K CORE MEMORY CONNECTIONS	
MEMORY CONNECTIONS	
I BANK I	FIELD I WIRE I JUMPER I
0	0-3 (0-16K) AB1 to EB2 1-3, 3-4 in
	4-7 (16-32) AB1 to EB2 2-4, 3-4 in
1	0-3 (32-48) AB1 to ED2 1-3, 3-4 in
	4-7 (48-64) AB1 to ED2 2-4, 3-4 in
2	0-3 (64-80) AB1 to EL2 1-3, 3-4 in
	4-7 (80-96) AB1 to EL2 2-4, 3-4 in
3	0-3 (96-112) AB1 to ER2 1-3, 3-4 in
	4-7 (112-128) AB1 to ER2 2-4, 3-4 in
TABLE 2A MS8-CA 16K MOS MEMORY SWITCH SETTINGS	
MEMORY SWITCHES SET TO "OFF"	
I BANK I	FIELD I ALL OTHERS "ON"
0	0-3 (0-16K) S1-1
	4-7 (16-32K) S1-2
1	0-3 (32-48K) S1-3
	4-7 (48-64K) S1-4
2	0-3 (64-80K) S1-5
	4-7 (80-96K) S1-6
3	0-3 (96-112) S1-7
	4-7 (112-128) S1-8
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TABLE 2B MS8-CB 3:R MOS MEMORY SWITCH SETTING	
MEMORY SWITCHES SET TO "OFF"	
I BANK I	FIELD I ALL OTHERS "ON"
0	0-7 (0-32K) S1-1 and S1-2
1	0-7 (32-64K) S1-3 and S1-4
2	0-7 (64-96K) S1-5 and S1-6
3	0-7 (96-128) S1-7 and S1-8
TABLE 3 JUMPER CONFIGURATION TO DISABLE MEMORY EXTENSION AND TIMESHARE	
JUMPERS	
W1	OUT
W2	IN
W3	IN
W4	IN
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APPENDIX B	
General Configuration Files	
<ol style="list-style-type: none"> 1. All memories must be physically located in the OMNIBUS where an "E" connector is present. 2. Remembering the above rule, place the memories as far away as possible from the CPU. 3. Direct Memory Address interfaces can only be located between the CPU and the first memory element. With one exception, in a two box system (2 BA8C's) where memory is located in both boxes a DMA interface may be located in any vacant slot of the box containing the CPU. 4. Programmed I/O interfaces may be located in any vacant slot of the system. 5. When memories are located in two BA8C chassis then the KT8-EX option must be used to extend the memory management option bank bits. The M9020 terminator card must be located in an "E" connector of the BA8C not containing the M8416. The 70-11411-1J cable is then connected between the M9020 and the M8416. 	
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APPENDIX C		
Configuration Examples		
Because the KT8-A is limited to use in the B88C chassis (20 slot box) there are only four possible configurations.		
1. The entire system located in one B88C with a KR8A CPU as shown below.		
SLOT OPTION	DEFINITION	
1	KR8A CPU (#8315)	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTICN TWO (#8317YB or YC), IF REQUIRED	
4	KT8-A MEMORY MANAGEMENT OPTION (#8416)	
5	DMA DEVICES CONFIGURED FROM THIS POINT TOWARD MEMORY	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD THE CPU	
12	ONLY I/O INTERFACES	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	-----	
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2. The entire system located in one B88C with a KR8F CPU as shown below.		
SLOT OPTION	DEFINITION	
1	KR8F TERMINATOR, M8328	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTION TWO (#8317YB or YC), IF REQUIRED	
4	KT8-A MEMORY MANAGEMENT OPTION (#8416)	
5	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	KR8F CPU, M8318	
19	KR8F CPU, M8388	
20	KR8F CPU, M8338	
		DEC FORM NO EN-01022-16-0376-1(81) DRA 108
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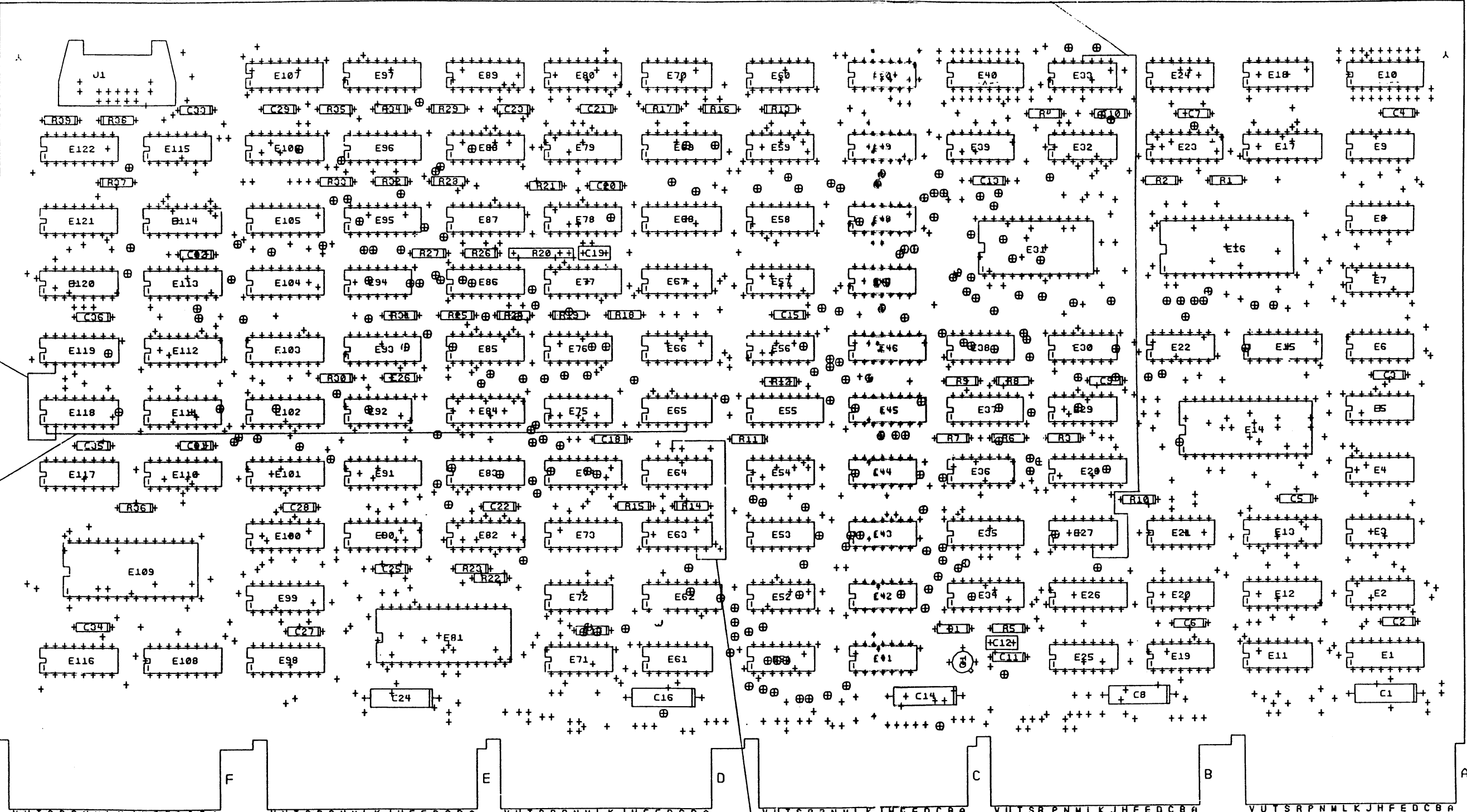
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3. The KT8-A system made up of two B88C boxes with the KR8F CPU in one box and all the memory located in the other box as shown below.		
(TOP B88C)		
SLOT OPTION	DEFINITION	
1	KR8F TERMINATOR, M8328	
2	ANY I/O INTERFACE	
3	ANY I/O INTERFACE	
4	KT8-A MEMORY MANAGEMENT OPTION (#8416)	
5	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD THE CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	BC08H-3 OMNIBUS EXPANDER CABLES (BOTTOM B88C)	
1	BC08H-3 OMNIBUS EXPANDER CABLES	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTION TWO (#8317YB or YC), IF REQUIRED	
4	-----	
5	-----	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	-----	
		DEC FORM NO EN-01022-16-0376-1(81) DRA 108
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4. The KT8-A system made up of two B88C boxes with a KR8F in one box and memories located in both boxes as shown below:		
SLOT OPTION	DEFINITION	
1	KR8F TERMINATOR, M8328	
2	ANY I/O INTERFACE	
3	ANY I/O INTERFACE	
4	M8828 KT8A TERMINATOR, LOCATE IN SLOT "E" OF OMNIBUS MEMORY	
5	MEMORY MEMORY CONFIGURED FROM THIS POINT TOWARD CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	MEMORY LAST MEMORY ELEMENT IN THIS B88C!	
12	ANY I/O INTERFACES	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	-----	
19	-----	
20	BC08H-3 OMNIBUS EXPANDER CABLES (BOTTOM B88C)	
1	BC08H-3 OMNIBUS EXPANDER CABLES	
2	DKC8A OPTION ONE (#8316), IF REQUIRED	
3	KM8-AC OPTION TWO (#8317YB or YC), IF REQUIRED	
4	KT8-A MEMORY MANAGEMENT OPTION, M8416	
5	MEMORY CONTINUE CONFIGURING MEMORY FROM THIS POINT TOWARD THE CPU	
6	-----	
7	-----	
8	-----	
9	-----	
10	-----	
11	-----	
12	-----	
13	-----	
14	-----	
15	-----	
16	-----	
17	-----	
18	KR8F CPU, M8318	
19	KR8F CPU, M8388	
20	KR8F CPU, M8338	
		DEC FORM NO EN-01022-16-0376-1(81) DRA 108
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COMPONENT SIDE VIEW

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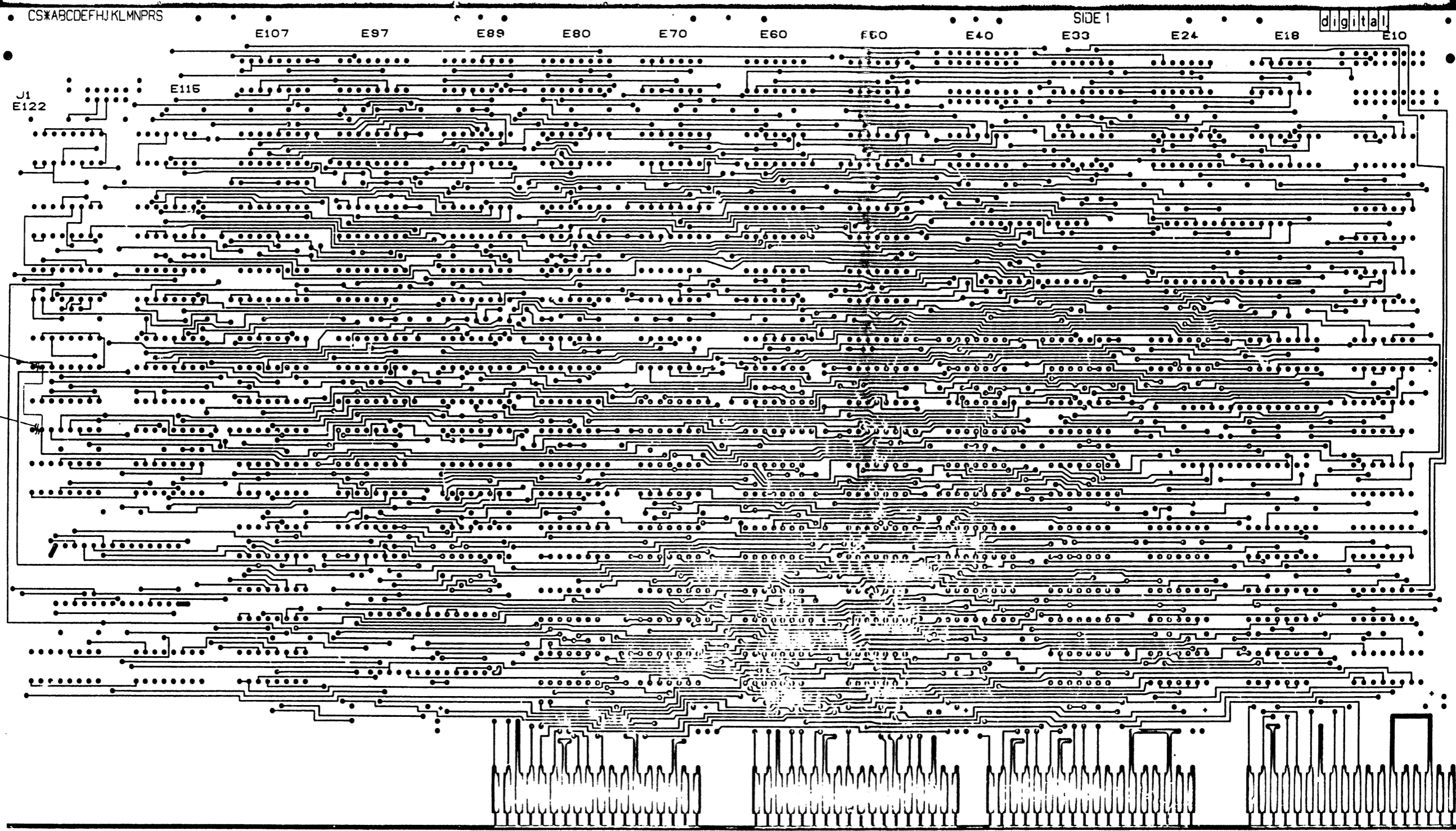
NOTES: MODULE REWORK AT RELEASE
ETCH CUT-SIDE 2 0-1 BETWEEN
BAZ 2 FEEDTHRU'S NEAR C6

CHANGE NO	REV	BY	DATE	DESCRIPTION
1A	MBIA/CCOOL	C		
	STEVEN			
	S. KLIEN			

ETCH REV.	C
P.C. DESIGN DATA BASE REV.	C

SIGNATURES	DATE	TITLE
DRN. <i>[Signature]</i>	10/1/77	digital TITLE PD178 MEMORY MANAGEMENT BOARD
CHK'D. <i>[Signature]</i>	11/1/77	
ENG. <i>[Signature]</i>	12/1/77	
PROJ. ENG. <i>[Signature]</i>	12/1/77	
PROD. <i>[Signature]</i>	12/1/77	
SCALE 2/1		SIZE CODE NUMBER
SHT. 1 OF 6		D UA MB 4,5-2-0
NEXT HIGHER ASSY. KM 8B		REV

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REV.	DATE	BY	CHKD

TITLE	PDP-8 MEMORY MANAGEMENT BOARD	SIZE CODE	D UA	NUMBER	M8416 -0-0	REV.	D
SCALE	3:1	SHEET	2	OF	6	DIST	