CHAPTER 5

INPUT/OUTPUT

Signals which pass between peripheral equipment and the PDP-8 are usually pulses supplied to a processor input bus, or static levels supplied as processor output signals which may be sampled or strobed by a selected I/O device. Exceptions to this rule are the address and data signals which arrive at the processor during data break operations as static levels, and the WC OVERFLOW, ADDRESS ACCEPTED, and IOP pulses, which are pulse outputs of the processor. The bussed nature of input/output signals of the processor requires that the peripheral equipment contain gating circuits to control the application of input pulses to the processor and timing control circuits to strobe processor output lines to transfer information into external device buffers. The design of circuits which perform these operations in input/output equipment depends upon the characteristics of the processor interface circuits as described in Chapter 6, the functional operation of the processor interface logic elements as explained in Chapter 3, and by the nature of the circuits in the peripheral equipment which receives or transmits signals. Gating circuits in peripheral equipment that supply input pulses to the processor are similar to those on the processor drawings for standard input/output devices.

Programmed information transfers (including initializing of equipment using the data break facility) between the processor and all other devices require that a preestablished select code in bits 3 through 8 of an IOT instruction enable each circuit (or group of circuits) transmitting or receiving information, and that transfers synchronize with the processor timing. A NAND gate and pulse amplifier circuits, serving as a device selector, perform these operations. Typical device selectors appear in engineering drawing 10 for the program interrupt synchronization element and on engineering drawing 11 for the Teletype control. An outline of a device selector suitable for peripheral equipment is at the end of this chapter.

The standard peripheral equipment supplied with a PDP-8 consists of a Teletype Model 33 Automatic Send Receive Set and a Teletype Control, which are described in this chapter. Except for the Type 189 Analog-to-Digital Converter, described in this chapter because it is intricately involved in the operations of the PDP-8 and wired into the system (adding this option to the computer requires little more than the insertion of the modules into the module connector blocks), other optional peripheral equipment is described in separate documents. The Type KR01 Automatic Restart, Type 182 Extended Arithmetic Element, and Type 681 Data Line Interface options described in Chapter 3 of this manual and the Type 183 Memory Extension Control, Type 184 Memory Module, and Type 188 Memory Parity options described in Chapter 4 of this manual are not peripheral equipment since these options are integral parts of the system and functionally inseparable from the processor.

TELETYPE MODEL 33 AUTOMATIC SEND RECEIVE SET

The Teletype unit supplied as standard equipment with a PDP-8 serves as a keyboard input and page printer output, and as a perforated-tape reader input and a tape-punch output device. This unit is a standard Model 33 Automatic Send and Receive Set (ASR) as described in Teletype Corporation bulletins 273B and 1184B. For operation with the PDP-8, this unit is modified as follows:

1. The WRU (who are you) pawl is removed. This pawl is used only when several Teletypes connect in a communication system so that a unit receiving a message sends a "who are you" message to the transmitting unit which automatically produces the "here is" identification code and supplies it to the receiving station. In the computer system this pawl is removed to prevent insertion of the "here is" code into data supplied to the computer from the Teletype unit.

2. Cables are connected between the Teletype unit and the control as appears in engineering drawing 11. Signal cables connect to a terminal block within the stand. A relay is added and connections are made to the tape reader advance magnet. These connections enable tape motion while the control assembles a character, and disable the magnet when the keyboard flag is a 1, indicating that the assembled character is ready for transfer to the computer.

This modification takes only a few minutes and does not permanently limit any normal use of the 33 ASR.

TELETYPE CONTROL (18)

The control assembles or disassembles serial information for the Teletype unit for parallel transfer to or from the accumulator of the processor. The control also provides the flags which cause a program interrupt or an instruction skip based upon the availability of the Teletype unit, thus controlling the rate of information transfer flow between the Teletype and the processor as a function of the program. Engineering drawing 11 shows the control and interface connections between the control and the Teletype unit. Table 5-1 indicates interface connections between the control and the processor.

In all programmed operation, the Teletype unit is considered two separate devices: a Teletype input device (TTI) from the keyboard or the perforated-tape reader; and a Teletype output device (TTO) for computer output information to be printed and/or punched on tape. Therefore, two device selectors are used, consisting of 6-input NAND gates at locations ME17 and ME18 (11, A2 and B1). One of these is assigned the select code of 03 to initiate operations associated with the keyboard/reader, and the other is assigned the select code of 04 to perform operations associated with the teleprinter/punch. Corresponding IOT

TABLE 5-1 TELETYPE CONTROL INTERFACE WITH PROCESSOR

Signal	Processor			Symbol and Direction*	Teletype Control Terminal
	Logic Element	Engineering Drawing	Terminal		
PWR CLR	Power Clear Generator	9	PD33U	⟶	MF36M
BAC4 (1)	AC	16	MF34M	⟷	ME22S
BAC5 (1)	AC	16	MF34P	⟷	ME23P
BAC6 (1)	AC	16	MF34S	⟷	ME23R
BAC7 (1)	AC	16	MF34T	⟷	ME23S
BAC8 (1)	AC	16	ME34V	⟷	ME24P
BAC9 (1)	AC	16	MF34D	⟷	ME24R
BAC10 (1)	AC	16	MF34E	⟷	ME24S
BAC11 (1)	AC	16		⟷	ME25H
INTERRUPT BUS IN	Interrupt Sync	10	PF1S	⟵	MF36S
COUNT PC	PC Control	11	PF1R	⟵	MF36R
TTI ⟶ AC	AC	2	PF1P	⟵	MF36P
KCC IOT 032	AC Control	3	PF1U	⟵	MF36U
IOP1	IOP Generator	10	PF1J	⟶	MF36J
IOP2	IOP Generator	10	PF1K	⟶	MF36K
IOP4	IOP Generator	10	PF1L	⟶	MF36L
MB3-4 (0)	MB	5	PD1R,T	⟶	MD36R,T
MB5-8 (0)	MB	5	PE1D,F,J,L	⟶	ME36D,F,J,L
MB7-8 (1)	MB	5	PE1K,M	⟶	ME36K,M
TTI0 (0)	AC	2	PB1A	⟷	MB36A
TTI1 (0)	AC	2	PB1B	⟷	MB36B
TTI2 (0)	AC	2	PC1A	⟷	MC36A
TTI3 (0)	AC	2	PC1B	⟷	MC36B
TTI4 (0)	AC	2	PD1A	⟷	MD36A
TTI5 (0)	AC	2	PD1B	⟷	MD36B
TTI6 (0)	AC	2	PE1A	⟷	ME36A
TTI7 (0)	AC	2	PE1B	⟷	MF36B

*Arrows pointing right designate processor output; arrows pointing left designate processor inputs.

pulses from the two device selectors perform parallel input and output functions. Pulses from the IOP1 pulse trigger the skip control element; pulses from the IOP2 pulse clear the control flags and/or the accumulator; and pulses produced by the IOP4 pulse initiate data transfers to or from the control.

Signals used by the Teletype unit are standard 11-unit-code serial current pulses consisting of marks (bias current) and spaces (no current). Each 11-unit Teletype character consists of a 1-unit start space, eight 1-unit character bits, and a 2-unit stop mark. The 8-bit flip-flop TTI shift register at locations MF22 through MF24 receive the Teletype characters from the keyboard/reader. The character code of a Teletype character loads into the TTI so that spaces correspond with binary 1's and marks correspond to binary 0's. Upon program command the complement of the contents of the TTI transfers in parallel to the accumulator. Eight-bit computer characters from the accumulator load in parallel into the 8-bit flip-flop shift register TTO at locations ME22 through ME25 for transmission to the Teletype unit. The TTO clock generates the start space, then shifts the eight character bits into a flip-flop which controls the printer selector magnets of the Teletype unit, and then produces the stop mark. This transfer of information from the TTO into the Teletype unit occurs in serial manner at the normal Teletype rate.

A ground IN ACTIVE signal flows from the control circuit of the Teletype incoming line unit module when a Teletype character starts to enter the TTI. This signal clears the READER RUN flip-flop, which in turn energizes a relay in the Teletype unit to release the tape feed latch. When released, the latch mechanism stops tape motion only when a complete character has been sensed and before sensing of the next character begins. The KEYBOARD FLAG flip-flop sets and causes a program interrupt when an 8-bit computer character has been assembled in the TTI from a Teletype character. The program senses the condition of this flag with a KSF microinstruction (skip if keyboard flag is a 1, IOT 6031) and issues a KRB microinstruction (IOT 6036) which clears the AC, clears the keyboard flag, transfers the contents of the TTI into the AC, and sets the READER RUN flip-flop to enable advance of the tape feed mechanism.

A TELEPRINTER FLG flip-flop sets when the last bit of the Teletype code has been sent to the teleprinter/punch, indicating that the TTO is ready to receive a new character from the AC. This flag connects to both the program interrupt synchronization element and the skip control element. Upon detecting the set set condition of the flag by the TSF microinstruction (skip if teleprinter flag is a 1, IOT 6041), the program issues a TLS microinstruction (IOT 6046) which clears the flag and loads a new computer character into the TTO.

Operation of the Teletype incoming line unit TTI requires an input clock signal which is eight times the baud frequency of the Teletype unit. This signal controls the strobing of Teletype information into the TTI during the center of each baud (which is the most reliable time for sensing) and controls the shifting of information through the flip-flops of the TTI. The Teletype transmitter requires an input clock frequency

which is the same as the baud frequency of the Teletype unit. This signal controls the shifting of the TTO and thus determines the timing of the 11-unit-code Teletype character it generates. The three Type S202 Dual Flip-Flops at locations MF14 through MF16 produce the TTI CLOCK and TTO CLOCK signals. These six flip-flops form a binary counter which provides frequency division of the output from the Type R405 Crystal Clock module at location ME15. This frequency division method is used since electronic clocks are not reliable at the low frequency required for Teletype operation. The 7.04-kc frequency of the clock is 64 times the baud frequency of the Teletype unit. Division of the clock frequency by 8 (three binary flip-flops) yields the TTI CLOCK signal, which is eight times the baud frequency, and division by 64 (six binary flip-flops) yields the TTO CLOCK signal, which corresponds with the baud frequency.

TYPE 189 ANALOG-TO-DIGITAL CONVERTER (189-0-2)

The Type 189 Converter operates in the conventional successive-approximation manner, using the memory buffer register as a distributor shift register and using the accumulator as the digital buffer register. The converter logic consists of some timing and control circuits, a 12-bit digital-to-analog converter, and a comparator. An ADC instruction, which produces a pause and clears the accumulator, initiates converter operation. The conversion process starts by assuming that the value of the analog input signal is at mid-scale. A binary 1 is therefore set into the most significant bit of the MB and transfers to accumulator bit AC0. This causes the digital-to-analog converter, whose output is a function of the number contained in the AC, to produce a voltage equal to the center of the converter range (ground to −10v). The output of the D/A converter, representing the first approximation of the input signal, is then compared with the actual analog input signal. If the approximated voltage is greater than the analog signal voltage, the AC bit clears. The binary 1 in bit MB0 then shifts one place to the right and transfers into the corresponding bit of the AC. The number in the AC is 4000 if the approximated voltage was less than the analog input signal or is 6000 if the approximated voltage was greater than the analog input during the previous step. The new number in the AC causes the D/A converter to generate a new approximated voltage. If this voltage is still too large, the clear and shift right process repeats, and the binary 1 now appears in bit AC2. The approximated voltage is again compared with the analog input signal. Each successive approximation reduces by one half the difference (error) between the value of the analog input signal and the value of its digital representation in the AC.

The location of the binary 1 in the MB controls the number of approximations made, and hence the accuracy of the conversion. Since the conversion starts when the binary 1 shifts right, one conversion takes place after sensing of the MB bit which discontinues the conversion process. At the conclusion of the conversion, the unsigned binary number in the accumulator is accurate to one half of the digital value