CHAPTER 2

LOGICAL FUNCTIONS

Both manual and stored-program operations of the PDP-8 are necessary to perform any complete task. The data break is the only fully automatic operation. Manual operation is normally limited to storing a Readin Mode or Binary Loader program, modifying or examining data or addresses in a prestored program, or establishing the starting conditions and initiating programmed operation of the system. Stored program operation is used in the performance of all user programs. However, for maintenance purposes and to facilitate the debugging of a new program, provision is made for manually advancing the program one cycle at a time or one instruction at a time.

The sequence in which operations occur during manual operation or during each machine cycle for stored program and automatic operation appears on the flow diagram, engineering drawing FD-D-8P-0-7.

FLOW DIAGRAM INTERPRETATION

The flow diagram illustrates the sequence of events that take place during each of the possible manual, stored program, or automatic operations. Sheet 1 of the flow diagram, containing all functions except manual operations, consists of six vertical columns. The first three columns correspond to one of the three major states in programmed operation: fetch (F), defer (D), and execute (E). The last three columns correspond to automatic operations during a data break and are represented by the word count (WC), current address (CA), and break (B) major states. Sheet 2 of the flow diagram contains the events that take place during manual operation. Horizontal rows on the flow diagram represent time states. Time proceeds from top to bottom on this diagram. The upper row represents the memory strobe during programmed and automatic operation, and represents time state SP0 during manual operation.

Events appear on the diagram as rectangular boxes joined by vertical flow lines. Operations in a sequence not specifically designated by a key name or instruction mnemonic are assumed to be common to all sequences (e.g., memory strobe in the F and D cycles, and 0 ⟶ RUN in time SP0). Branching of a common sequence into several operation chains, each associated with a specific instruction or key operation, appears as a vertical line terminated by an arrowhead on a horizontal line. Thus, in the fetch cycle, MEMORY STROBE is common to all operations, after which a branch occurs, and the next event is a JMS ⟶ IR if an INT ACK condition exists, or is MB TRANSITIONS ⟶ IR if an $\overline{\text{INT ACK}}$ condition exists. Confluence of several sequences into a further common sequence appears as several vertical lines with arrowheads that all meet a common horizontal line. A single vertical line descending from the

horizontal line to the rectangle specifies the next common event. Thus, the separate sequences associated with manual deposit and examine operations each conclude with the sequence 1 ⟶ MEM START, 1 ⟶ RUN, and 1 ⟶ RUN STOP.

Note that some events specified in the rectangles of the flow chart are conditional, others unconditional. Unconditional events appear as information transfer statements with no indication of register content. For example, key operations begin with the event 0 ⟶ RUN which occurs in time state SP0, and during a load address operation the PC clears in time state SP1. Conditional events appear as information transfer statements accompanied by one or more indications of the contents of a register. For example, during a group 1 OPR instruction, several conditional events may occur, and these appear in the leftmost sequence in time T1. The first event, +1 ⟶ PC, is unconditional. The second event, 0 ⟶ AC, occurs only if MB bit 4 contains a 1 and MB bit 6 contains a 0. When following the sequence of events in any given instruction, conditional events for which the required conditions are not met should be ignored.

To find the exact mechanism by which the processor executes an event specified in the flow diagram refer to the appropriate engineering logic diagram and the corresponding circuit description. When tracing a transfer operation, first examine the input and control gating of the register to which the transfer is being made. Thus, to trace the operation +1 ⟶ PC, first examine the logic diagram of the PC register: a command pulse designated +1 ⟶ PC strobes a set of input gates. To find how this pulse generates, examine the logic drawing of the PC control. When there is doubt where a pulse or level generates, consult Appendix 1. This appendix lists all command and control signals in alphanumerical order of designation, as well as the number of the engineering drawing on which the circuits which generate any given signal appear.

> NOTE: It is very important that maintenance personnel familiarize themselves with the flow diagram of the PDP-8. This flow diagram is the key to understanding system operation, and provides much information valuable in troubleshooting.

PREFATORY OPERATIONS

POWER and PANEL LOCK Switches

Primary power flows to the computer from the POWER and PANEL LOCK switches. With the PANEL LOCK switch in the unlocked (counterclockwise) position, turning the POWER switch to the clockwise position applies primary power to the computer. When a stored program is running, placing the PANEL LOCK

switch in the locked (clockwise) position disables the POWER switch to prevent primary power from being accidentally turned off. The PANEL LOCK switch also disables all manual keys except the SWITCH REGISTER, to prevent accidental distrubance of the program.

Power Clearing

When primary power is first applied, the capacitors of the power supply take an appreciable time to charge to the +10v and −15v levels. The processor logic circuits become operative before the supplies stabilize, but the +40v memory supplies are inhibited until the OK LEVEL relay driver in the power supply generates a negative OK level, usually when the potential on the −15v line reaches −14v. During the rise period, the $\overline{OK}$ ground level enables a 100-kc clock generating PWR CLR pulses to clear the RUN flip-flop, all the memory control flip-flops, and the Teletype control and register flip-flops. A PWR CLR pulse also generates when the START key is pressed. These PWR CLR pulses are also available at the interface to clear the registers of I/O devices. When the negative OK level appears, the 100-kc clock disables and the computer and I/O devices clear for operation.

MANUAL OPERATIONS

Keys and switches on the operator console have three functions: they permit information to be stored in core memory; they permit the contents of a specified core memory cell to be displayed for visual examination; and they permit a program to be started and stopped. Operation of the START, LOAD ADD (load address), DEP (deposit), EXAM (examine), or CONT (continue) keys causes the special pulse generator to generate four special pulse (SP) time states during which all manual operations occur. These five keys clear the RUN flip-flop during time state SP0, preventing or interrupting programmed or automatic operation. Operation of the START or CONT keys sets the RUN flip-flop to 1 during time state SP3 so that the processor begins programmed operation at the conclusion of the time state.

LOAD ADD Key

Before any program can be loaded or executed, the operator must set the starting address into the program counter (PC). Pressing the LOAD ADD (load address) key generates a KEY LOAD ADDRESS signal which starts the special pulse generator and prevents the RUN flip-flop from being set to 1 at the end of the special pulse cycle. During time state SP0, the RUN flip-flop clears. During time state SP1, the PC clears. During time state SP2, the contents of the switch register (SR) are set into the PC. If the memory extension control is in use, the contents of the INST FIELD (instruction field) switches are also set into the instruction field register (IF) and the contents of the DATA FIELD switches are set into the data field register (DF).

START Key

The START key initiates execution of a program which has been loaded into core memory. Pressing the key generates the KEY ST+EX+DP (key start OR examine OR deposit) level which starts the special pulse generator. During the cycle of the special pulse generator, the following sequence of events takes place:

1. During time state SP0, the RUN flip-flop clears, ensuring that the program does not start prematurely.

2. During time state SP1, the accumulator (AC), link (L), memory buffer register (MB), instruction register (IR), and interrupt control flip-flops clear. During this time state, the major state generator is set to fetch, and the contents of the PC jam-transfer into the memory address register (MA). At the end of this time state, the processor is ready to execute the first instruction and the PC contains the starting address.

3. During time state SP2, a MEM START pulse generates, setting the MEM ENABLE flip-flop and starting the memory timing circuits.

4. During time state SP3, the RUN flip-flop is set to 1. Programmed operation now initiated, the processor executes successive instructions until it encounters a halt command.

CONT Key

The CONT (continue) key permits a program which has temporarily halted to be restarted. Pressing this key clears the RUN flip-flop during time state SP0, generates T2B and MEM START signals during time state SP2, and sets the RUN flip-flop to 1 during time state SP3. Since operation of this key does not clear or in any way change the contents of any register, it initiates execution of the program from the conditions that currently exist.

DEP Key

Lifting the DEP (deposit) key causes the contents of the SR to deposit in memory at the address specified by the current program count. The contents of the PC then increment to permit repeated operation of the DEP key to store information at consecutive memory addresses. Note that a load address operation that sets the starting address into the PC must always precede the initial deposit operation. If the addresses at which information is to be deposited are not consecutive, a load address operation must precede each deposit operation. Pressing the DEP key initiates the following sequence of events:

1. During time SP0, the RUN flip-flop clears.

2. During time SP1, the AC, MB, and IR clear. The major state generator is set to the execute state, the contents of the PC transfer into the MA, and the contents of the PC then increment.

3. During time state SP2, the operation code for the DCA instruction (3_8) is set into the IR, the contents of the SWITCH REGISTER (SR) transfer into the AC, and a MEM START signal generates.

4. During time state SP3, the RUN flip-flop is set to 1, but is immediately reset to 0 by a T1 pulse, starting the execute cycle of the DCA instruction but ensuring that the CP halts at the end of the cycle.

5. The memory strobe is disabled so that the contents of the MB remain 0 until time state T1 of the execute cycle, when the contents of the AC transfer to the MB and the AC then clears.

6. During time state T2, the 0 state of the RUN flip-flop inhibits generation of the T2B pulse.

EXAM Key

Pressing the EXAM (examine) key causes the contents of the memory cell specified by the contents of the PC to transfer into the MB and AC for visual examination. The contents of the PC then increment so that repeated operation of the EXAM key permits examination of the contents of consecutive memory locations. Note that a load address operation must precede the first examine operation. To examine several non-consecutive memory cells, separately specify each location by a load address operation. When the EXAM key is pressed, the following sequence occurs:

1. In time states SP0 and SP1, the sequence is the same as that initiated by the DEP key.

2. In time state SP2, the operation code for TAD (1_8) is set into the IR, and a MEM START signal generates.

3. When the memory strobe pulse occurs, the contents of the specified memory cell read into the MB. During time state T1 of the execute cycle, a HALF ADD command pulse generates to transfer binary 1's from the MB into the corresponding bits of the AC.