

## CHAPTER 10

# ENGINEERING DRAWINGS

This chapter contains reduced copies of DEC block schematics, circuit schematics, and other engineering drawings necessary for understanding and maintaining this equipment. Only those drawings which are essential and are not available in the referenced pertinent documents are included. Should any discrepancy exist between the drawings in this chapter and those supplied with the equipment, assume that the latter drawings are correct. The Table of Contents contains a complete listing of the drawings in this chapter.

### DRAWING NUMBERS

DEC engineering drawing numbers contain five groups of information, separated by hyphens. A drawing number such as BS-D-9999-1-5 consists of the following information reading from left to right: a 2- or 3-letter code specifying the type of drawing (BS); a 1-letter code specifying the size of the original drawing (D); the type number of the equipment (9999); the manufacturing series of the equipment (1); and the drawing number within a particular series (5). The drawing type codes are:

BS, block schematic or logic diagram	PW, power wiring
CD, cable diagram	RS, replacement schematic
CL, cable list	UML, utilization module list
CS, circuit schematic	WD, wiring diagram
FD, flow diagram	WL, wiring list

### CIRCUIT SYMBOLS

Block schematic engineering drawings of DEC equipment indicate signal flow, logical functions, circuit type and physical location, wiring, and other pertinent information. Individual circuits are shown in block or semiblock form, using symbols that define the circuit operation. These symbols are similar to those appearing in both the FLIP CHIP Modules Catalog and the System Modules Catalog but are often simplified. Figure 10-1 illustrates some of the symbols used in DEC engineering drawings.

### LOGIC SIGNAL SYMBOLS

DEC standard logic signal symbols are shown at the input of most circuits to specify the enabling conditions required to produce a desired output. These symbols represent either standard DEC logic levels, standard DEC pulses, standard FLIP CHIP pulses, or level transitions.

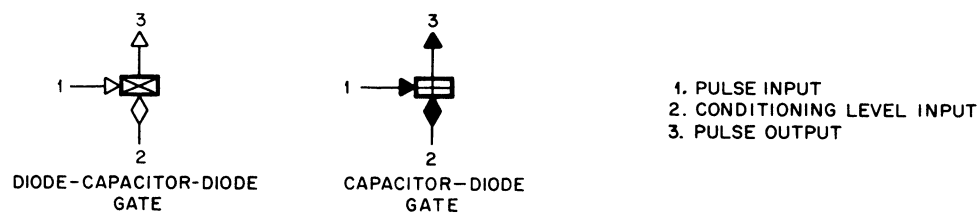
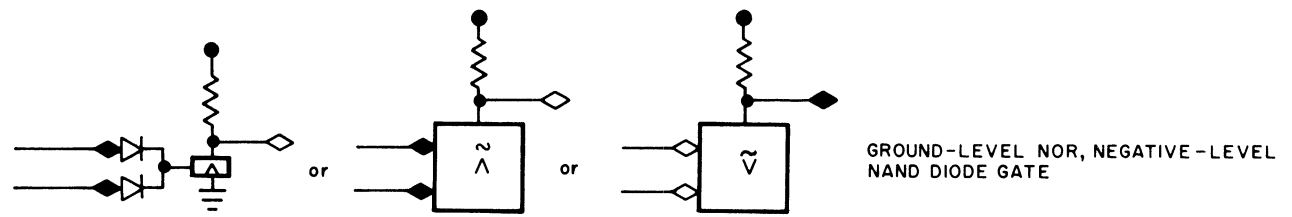
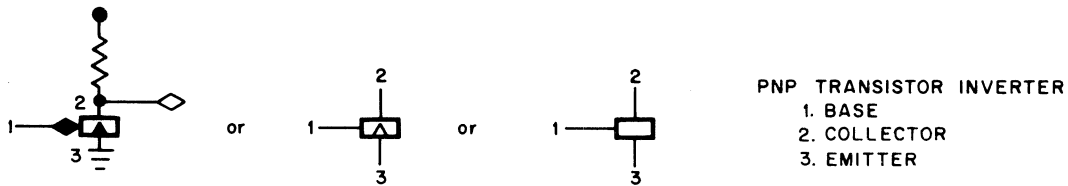
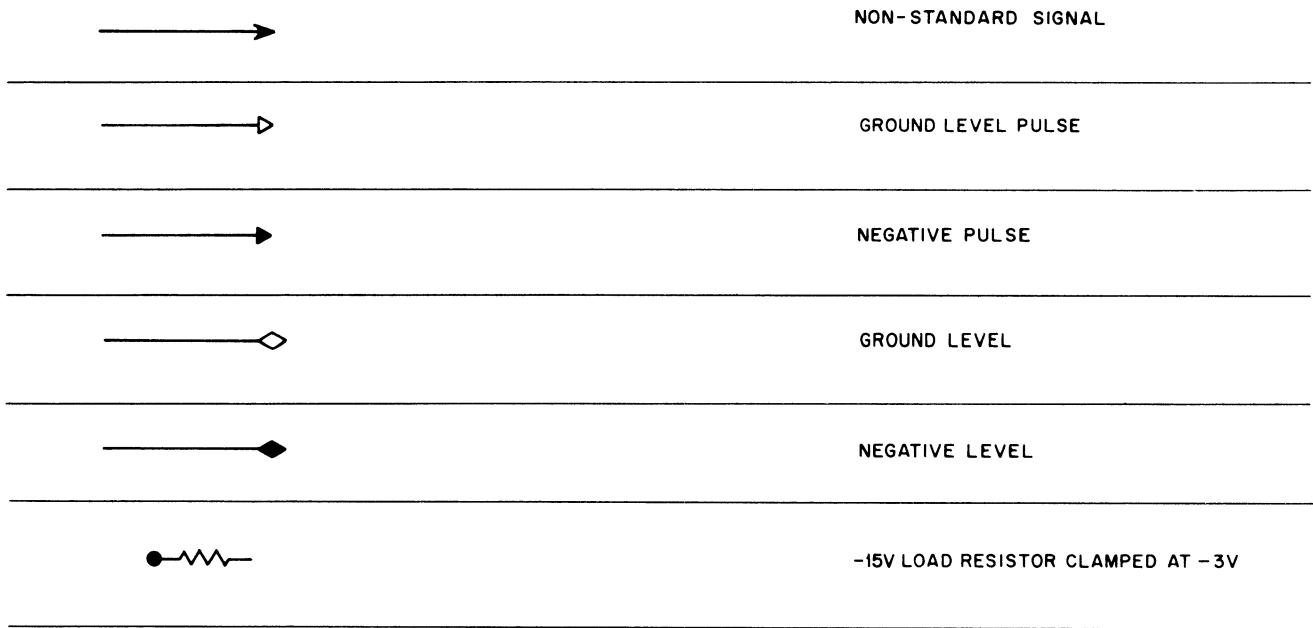
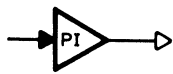
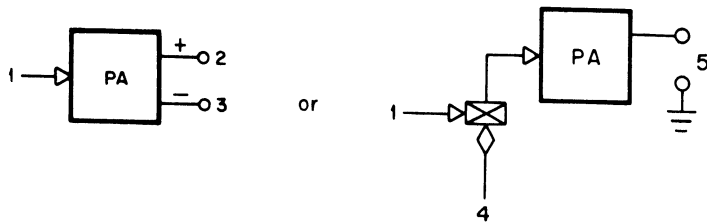


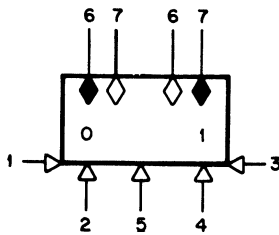
Figure 10-1 DEC Symbols



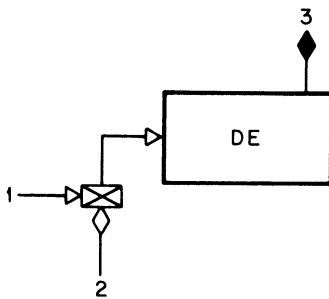
PULSE INVERTER



PULSE AMPLIFIER  
 1. PULSE INPUT, POLARITY INDICATED BY INPUT SIGNAL  
 2,3. TRANSFORMER-COUPLED PULSE OUTPUT. EITHER TERMINAL MAY BE GROUNDED  
 4. CONDITIONING LEVEL INPUT  
 5. DIRECT-COUPLED OUTPUT PULSE



FLIP-FLOP (MOST FLIP-FLOPS HAVE ONLY SOME OF THE FOLLOWING):  
 1. DIRECT-CLEAR INPUT  
 2. GATED-CLEAR INPUT  
 3. DIRECT-SET INPUT  
 4. GATED-SET INPUT  
 5. COMPLEMENT INPUT  
 6. OUTPUT LEVEL, -3 V IF 0, 0 V IF 1  
 7. OUTPUT LEVEL, 0 V IF 0, -3 V IF 1



DELAY (ONE-SHOT MULTIVIBRATOR)  
 1. INPUT TRIGGER PULSE  
 2. INPUT CONDITIONING LEVEL  
 3. OUTPUT LEVEL, -3V DURING DELAY

Figure 10-1 DEC Symbols (continued)

### Logic Levels

The standard DEC logic level is either at ground (0 to -0.3v) or at -3v (-2.5 to -3.5v). Logic signals generally have mnemonic names which indicate the assertion condition of the signal. An open diamond (—◇) indicates that the signal is a DEC logic level and that ground represents assertion; a solid diamond (—◆) indicates that the signal is also a DEC logic level and that -3v represents assertion. All logic signals at the conditioning level inputs of diode-capacitor-diode gates must be present for a specified length of time (depending on the module used) before an input pulse will trigger operation of the gate.

### Standard Pulses

DEC standard pulses are 2.5v in amplitude with reference to either ground or  $-3v$ , depending upon the type of module used. The width of standard pulses is either 40, 70, or 400 nsec as required for specific circuit configurations. The standard 2.5v negative pulse ( $-2.3$  to  $-3.5v$ ) is indicated by a solid triangle ( $\blacktriangleright$ ) and is always referenced with respect to ground, as shown in Figure 10-2.

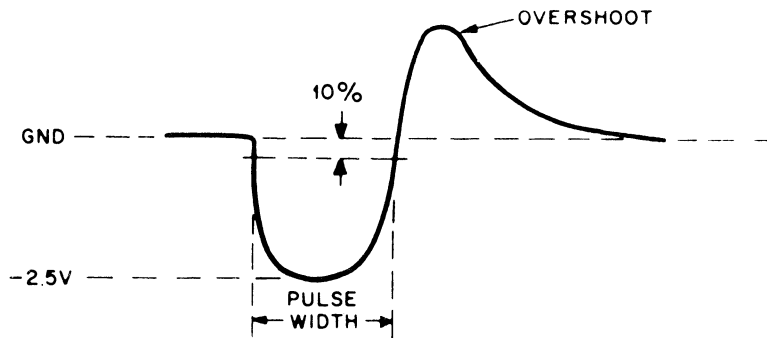


Figure 10-2 Standard Negative Pulse

The standard positive pulse is the inverse of the negative pulse and is indicated by an open triangle ( $\blacktriangleleft$ ). The positive pulse goes either from  $-3v$  to ground or goes from ground to  $+2.5v$  ( $+2.3$  to  $+3.0v$ ).

### FLIP CHIP Standard Pulses

FLIP CHIP circuit operation utilizes two types of pulses, R- and S-series and B-series. The pulse produced by R- and S-series modules starts at  $-3v$ , goes to ground ( $-0.2v$ ) for 100 nsec, then returns to  $-3v$ . This pulse is shown in Figure 10-3.

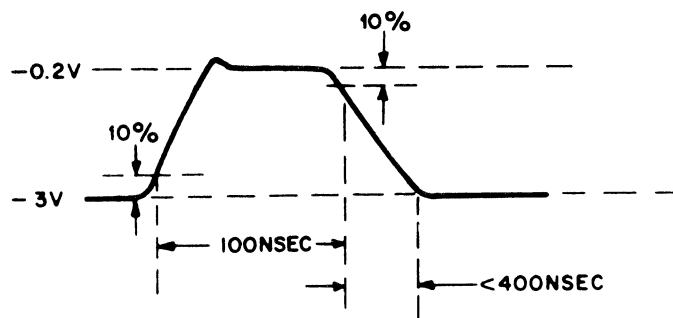


Figure 10-3 FLIP CHIP R- and S-Series Pulses

The B-series negative pulse is 2.5v in amplitude and 40 nsec in duration and is similar to the one shown in Figure 10-2. If this pulse arrives at the base of an inverter, the inverter output will be a narrow pulse, similar in shape to the R-series standard pulse. The B-series positive pulse, which goes from ground to + 2.5v, is the inverse of the B-series negative pulse.

### Level Transitions

Occasionally, the transition of a level is used at an input where a standard pulse is otherwise expected and a composite symbol (—◆▷) indicates this fact. The triangle is drawn open or solid depending, respectively, on whether the positive (-3v to ground) or the negative (ground to -3v) transition triggers circuit action. The shading of the diamond either is the same as that of the triangle to indicate triggering on the leading edge of a level or is opposite that of the triangle to indicate triggering on the trailing edge. An arrowhead (—▶) pointing in the direction of signal flow indicates nonstandard signals (power supply outputs, analog signals, etc.).

### SEMICONDUCTOR SUBSTITUTION

Standard EIA components as specified in Table 10-1 can replace most DEC semiconductors used in modules of the PDP-8. Exact replacement is recommended for semiconductors not listed.

TABLE 10-1 SEMICONDUCTOR SUBSTITUTION

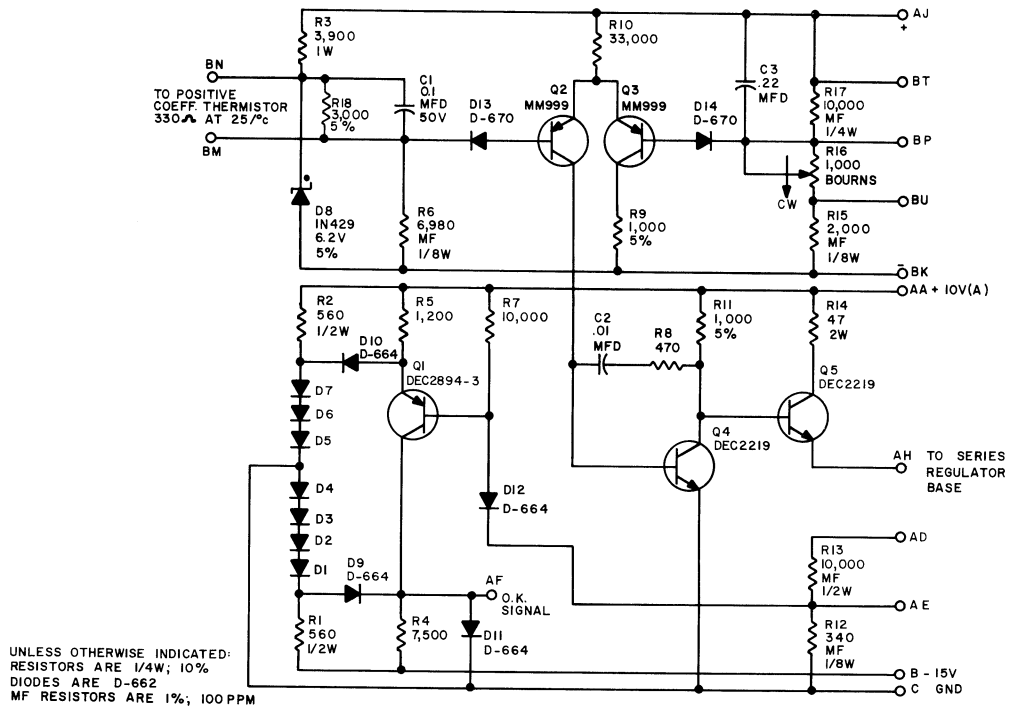
DEC	EIA	DEC	EIA
D-662	1N645	DEC 3639	2N3639
D-664	1N3606	DEC 3639-2	2N3639-2
D-670	1N3653	SDA-6	2N2060
D-668	two 1N3606 in series	1N429	1N429 6.2v 5%
DEC 1008	MM1008	1N449	1N449 6.2v 5%
DEC 2904	2N1132	1N762	1N762 5.5v 250 ohms 5%
DEC 3009	2N3009		

### S SERIES MODULES

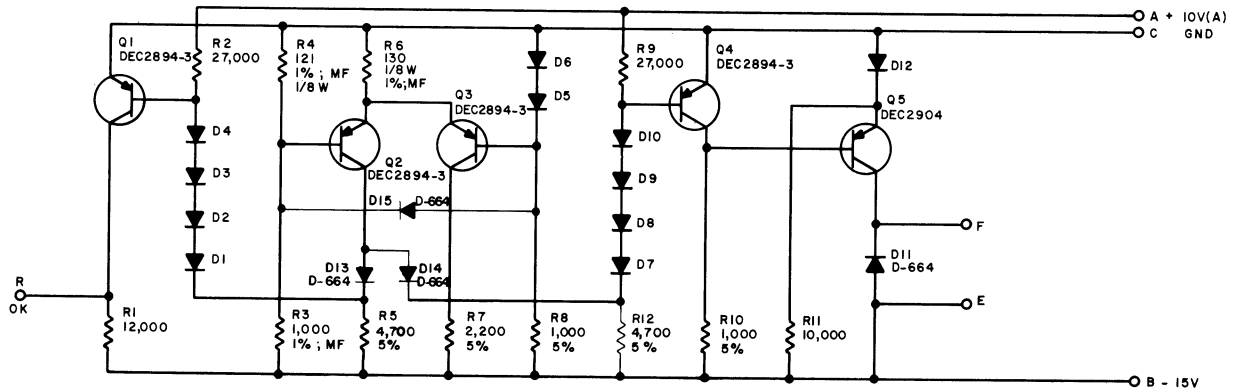
Ten R-series modules have been especially adapted for use in the PDP-8. The type numbers are the same, except that the prefix letter is S instead of R. They are:

S107	Inverter	S203	Triple Flip-Flop
S111	Diode Gate	S205	Dual Flip-Flop
S151	Binary-to-Octal Decoder	S284	Quadraflop
S181	DC Carry Chain	S602	Pulse Amplifier
S202	Dual Flip-Flop	S603	Pulse Amplifier

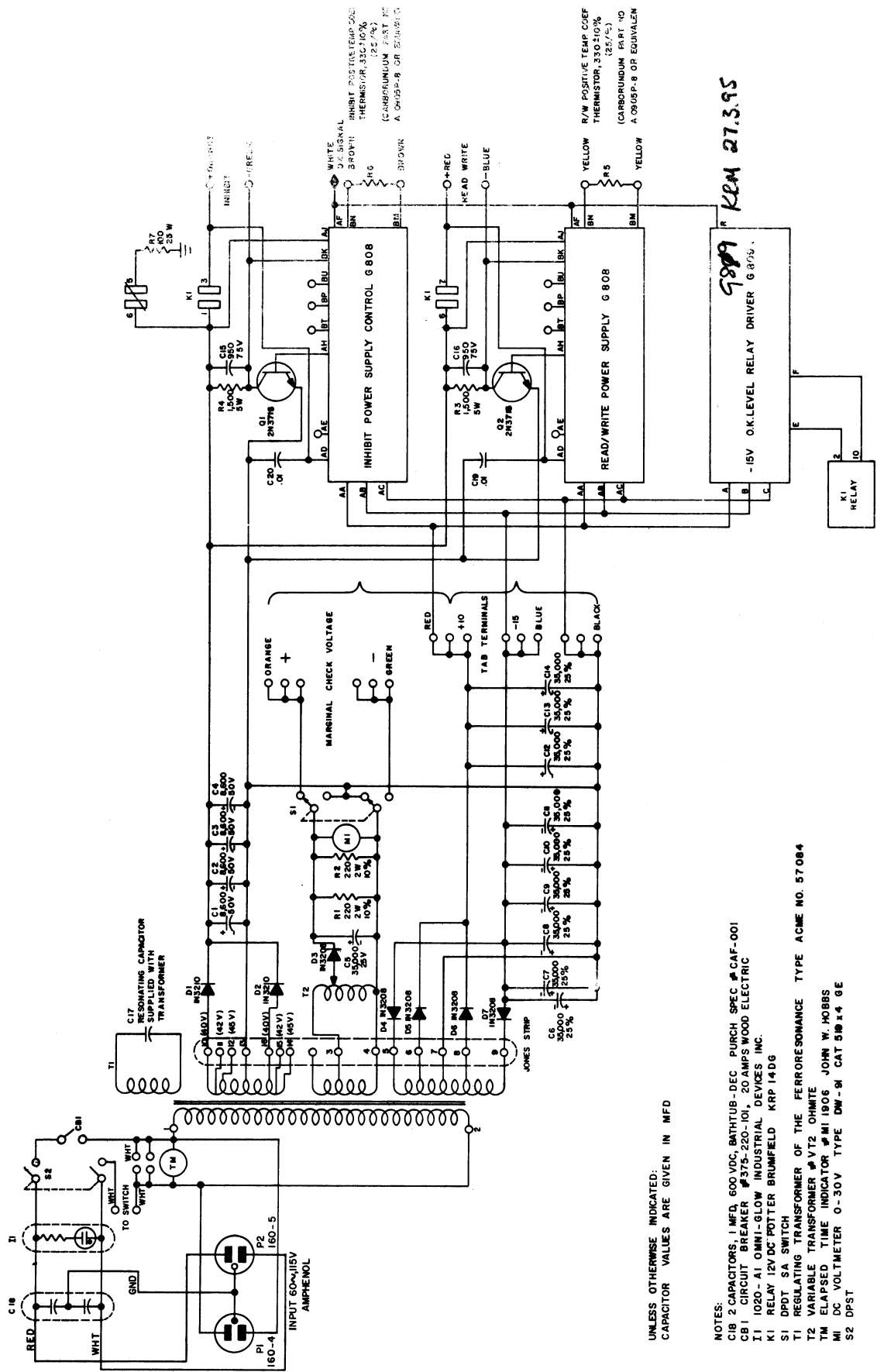
The S-series modules have 5-ma clamped loads instead of 2 ma. Their R-series counterparts may be modified by changing the load resistors to 3K ohms, but beware of decreased output drive.



RS-B-G808 Control for 708 Power Supply



RS-B-G809 -15v Sense and Relay Driver

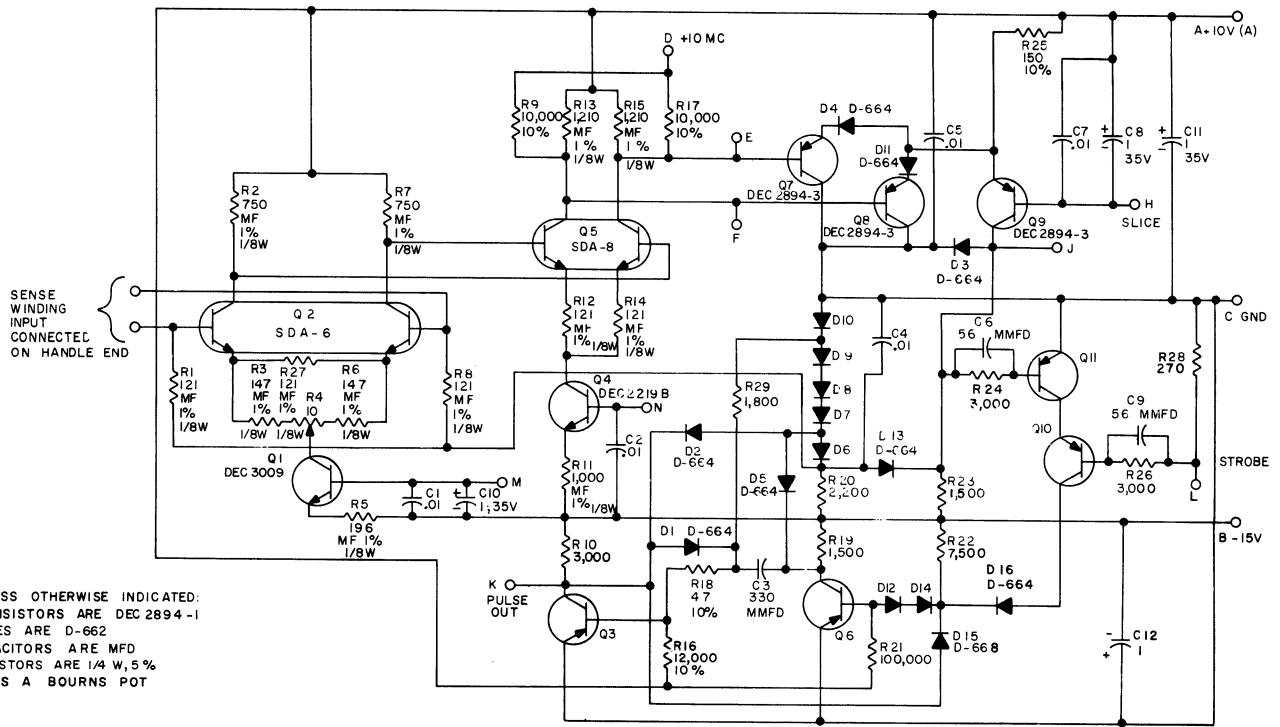


R/KEM 27.3.95

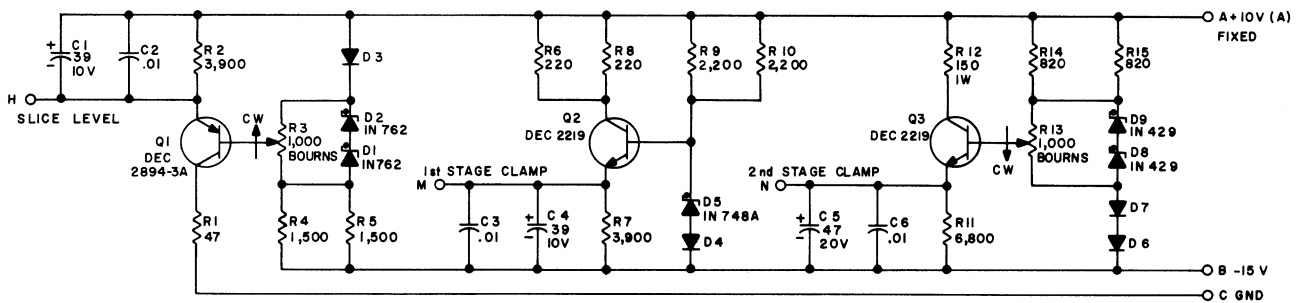
UNLESS OTHERWISE INDICATED:  
CAPACITOR VALUES ARE GIVEN IN MFD

- NOTES:
- C18 2 CAPACITORS, 1 MFD, 600 VDC, BATHTUB-DEC PURCH SPEC #CAF-001
  - C81 CIRCUIT BREAKER #375-220-10L, 20 AMPS WOOD ELECTRIC
  - I1 1020-A1 OMNI-GLOW INDUSTRIAL DEVICES INC.
  - K1 RELAY 12V DC POTTER BRUMFIELD KRP 14DG
  - S1 DPDT SA SWITCH
  - T1 REGULATING TRANSFORMER OF THE FERRORESONANCE TYPE ACME NO. 57084
  - T2 VARIABLE TRANSFORMER #VT2 OHMITE
  - TM TIME ELAPSED INDICATOR #MI 1906 JOHN W. HOBBS
  - MI DC VOLTMETER 0-30V TYPE DW-9I CAT 510 K 4 GE
  - S2 DPST

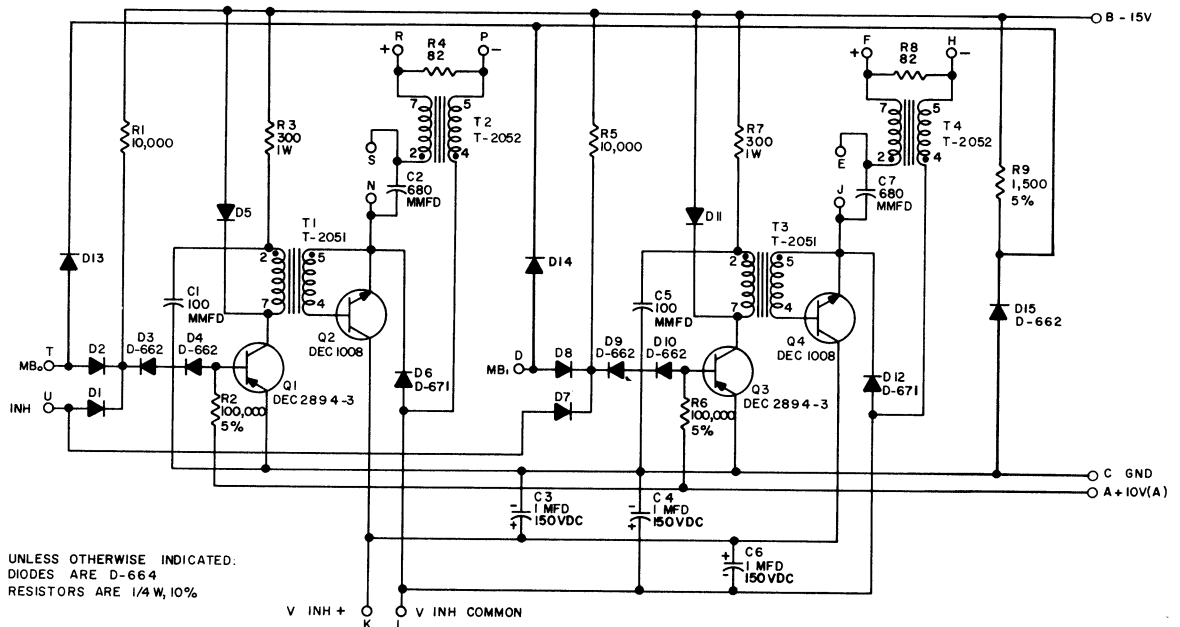
RS-C-708 Power Supply 708



RS-B-G007 Sense Amplifier

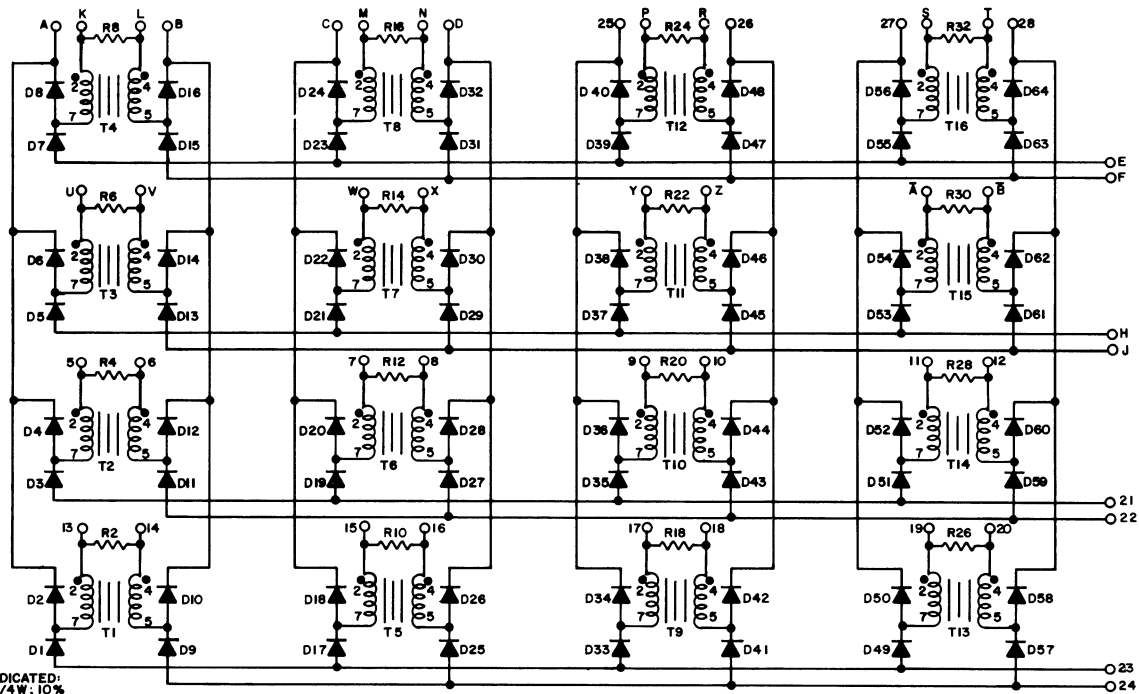


RS-B-G008 Master Slice Control

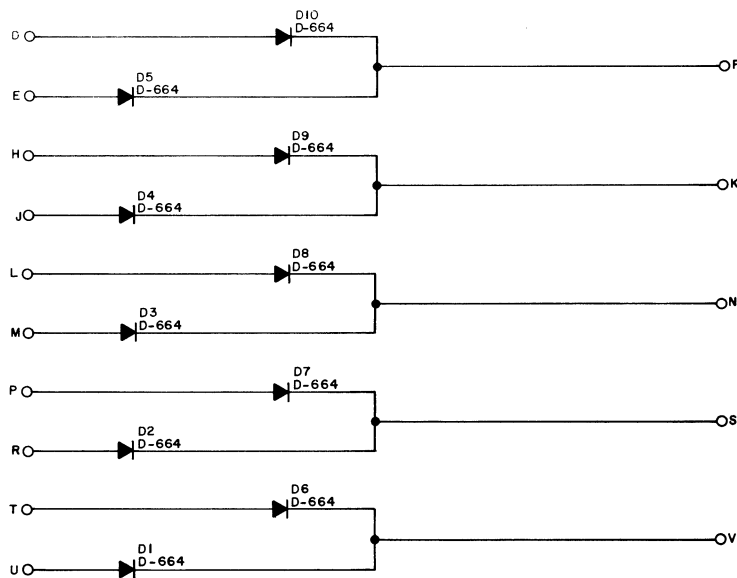


RS-B-G208 Inhibit Driver.

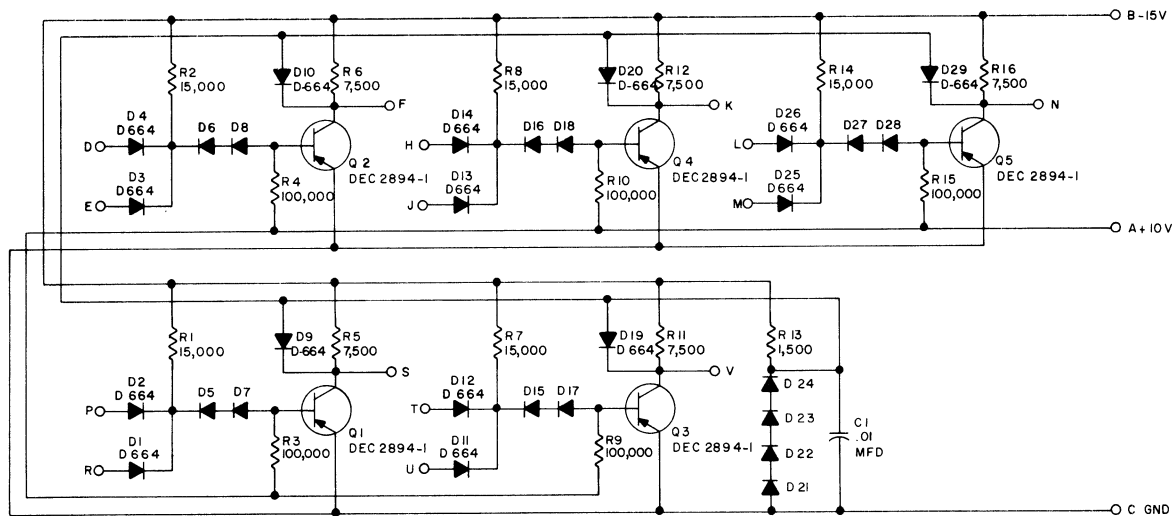




RS-B-G603 Memory Selector Matrix

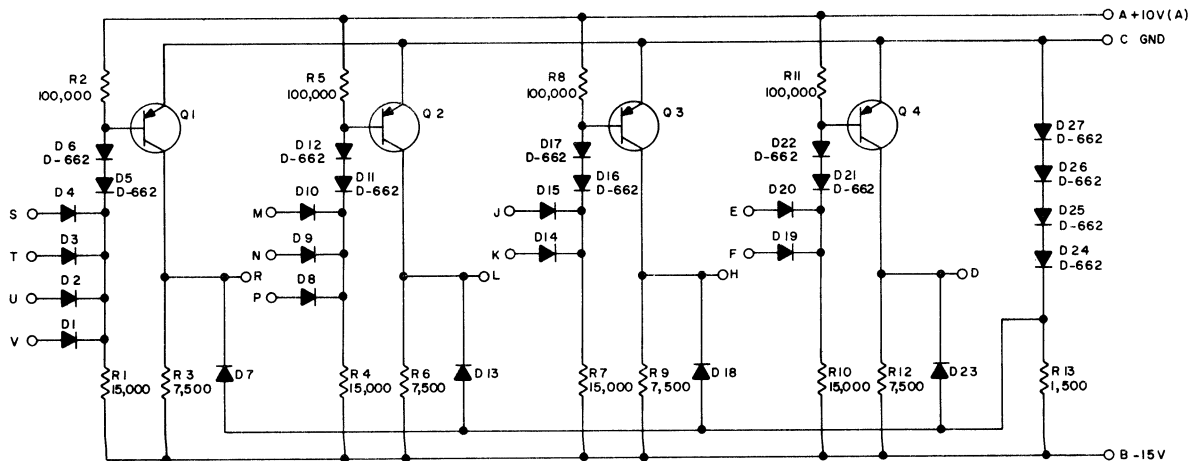


RS-B-R002 Diode Cluster



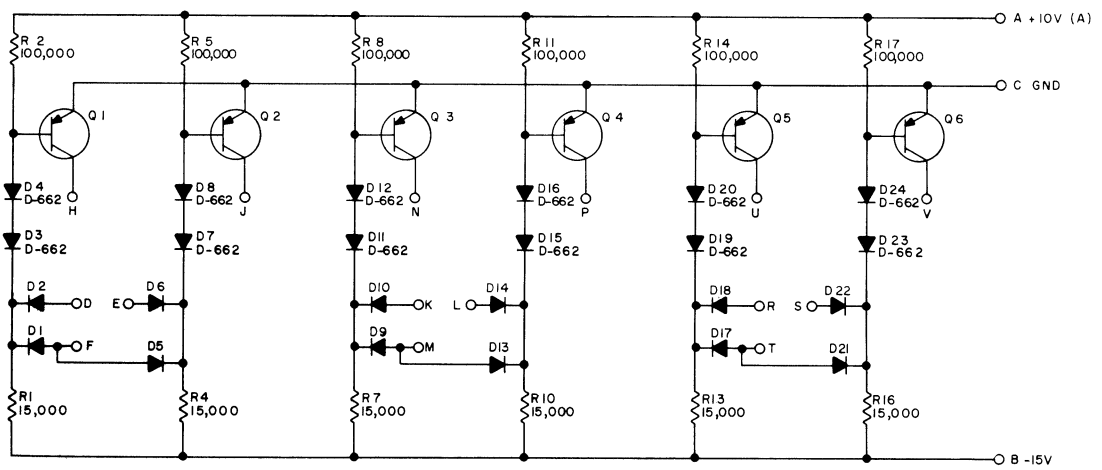
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4 W, 5%  
 DIODES ARE D 662

### RS-B-R113 Diode Gate



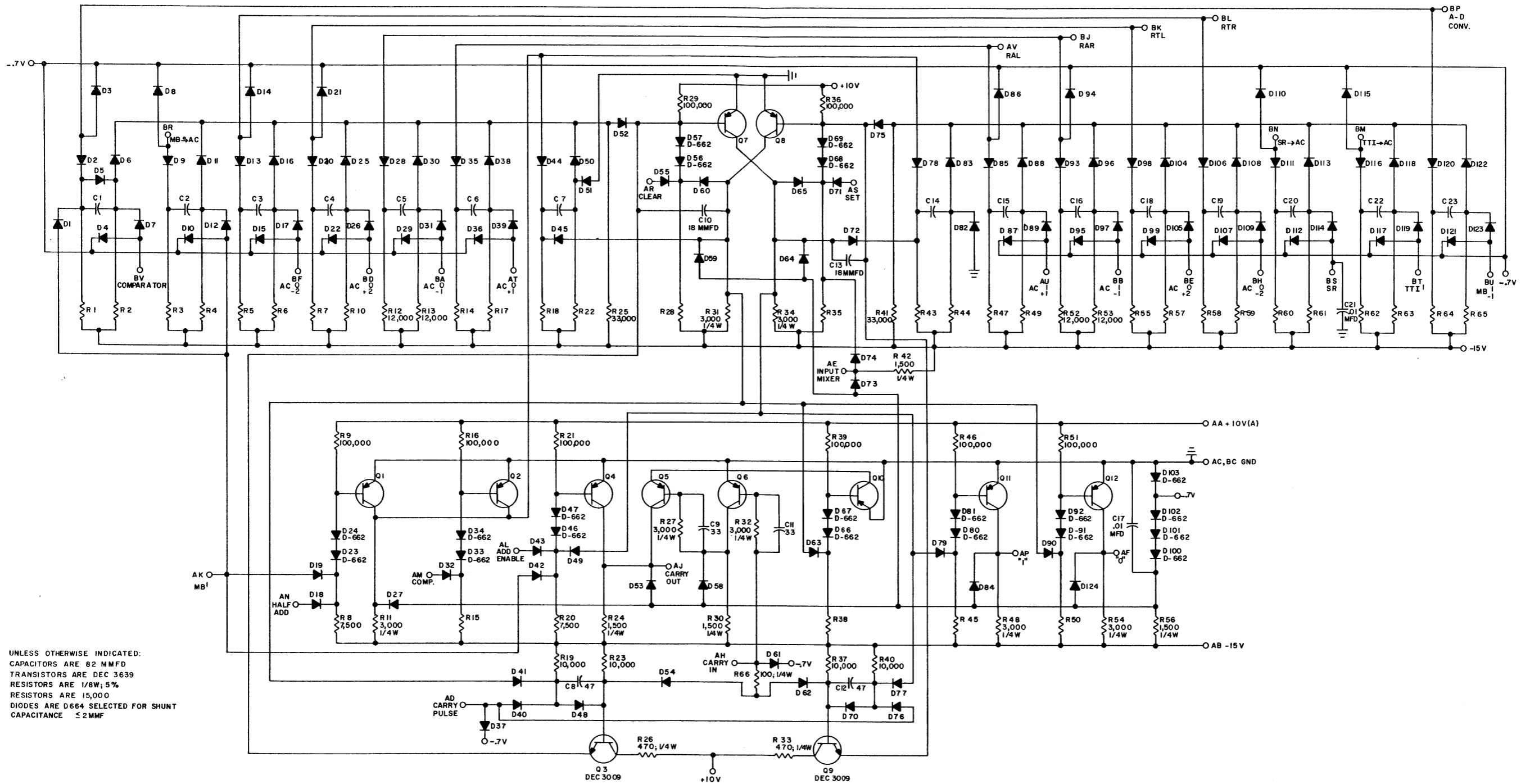
UNLESS OTHERWISE INDICATED:  
 TRANSISTORS ARE DEC 3639  
 DIODES ARE D-664  
 RESISTORS ARE 1/4 W, 5%

### RS-B-R121 NAND Gate



UNLESS OTHERWISE INDICATED:  
 TRANSISTORS ARE DEC 3639-0  
 RESISTORS ARE 1/4 W, 5%  
 DIODES ARE D-664

RS-B-R123 Diode Gate



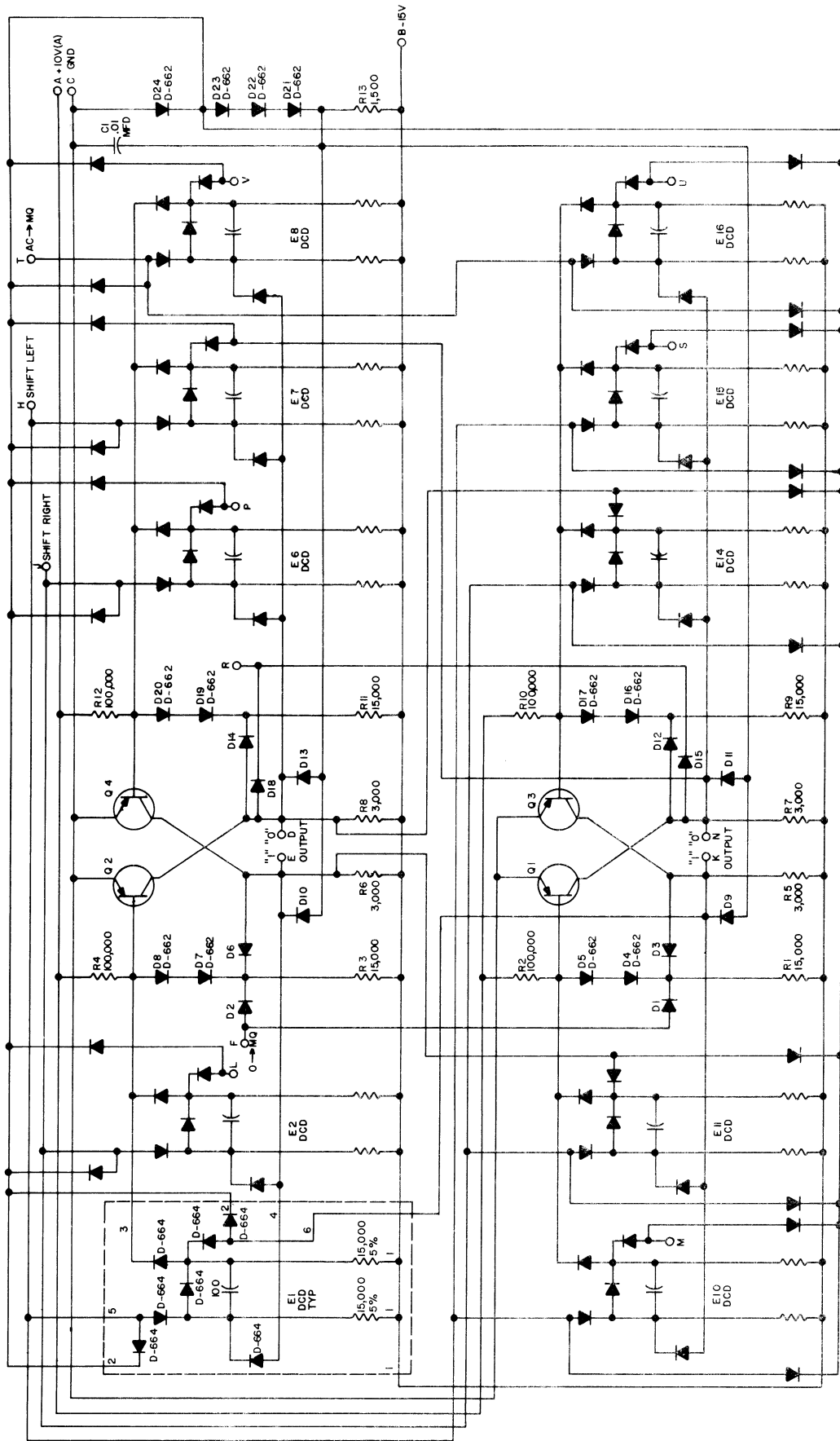
UNLESS OTHERWISE INDICATED:  
 CAPACITORS ARE 82 MMFD  
 TRANSISTORS ARE DEC 3639  
 RESISTORS ARE 1/8W; 5%  
 RESISTORS ARE 15,000  
 DIODES ARE D664 SELECTED FOR SHUNT  
 CAPACITANCE  $\leq 2$ MMF

RS-D-R210 PDP-8 Accumulator



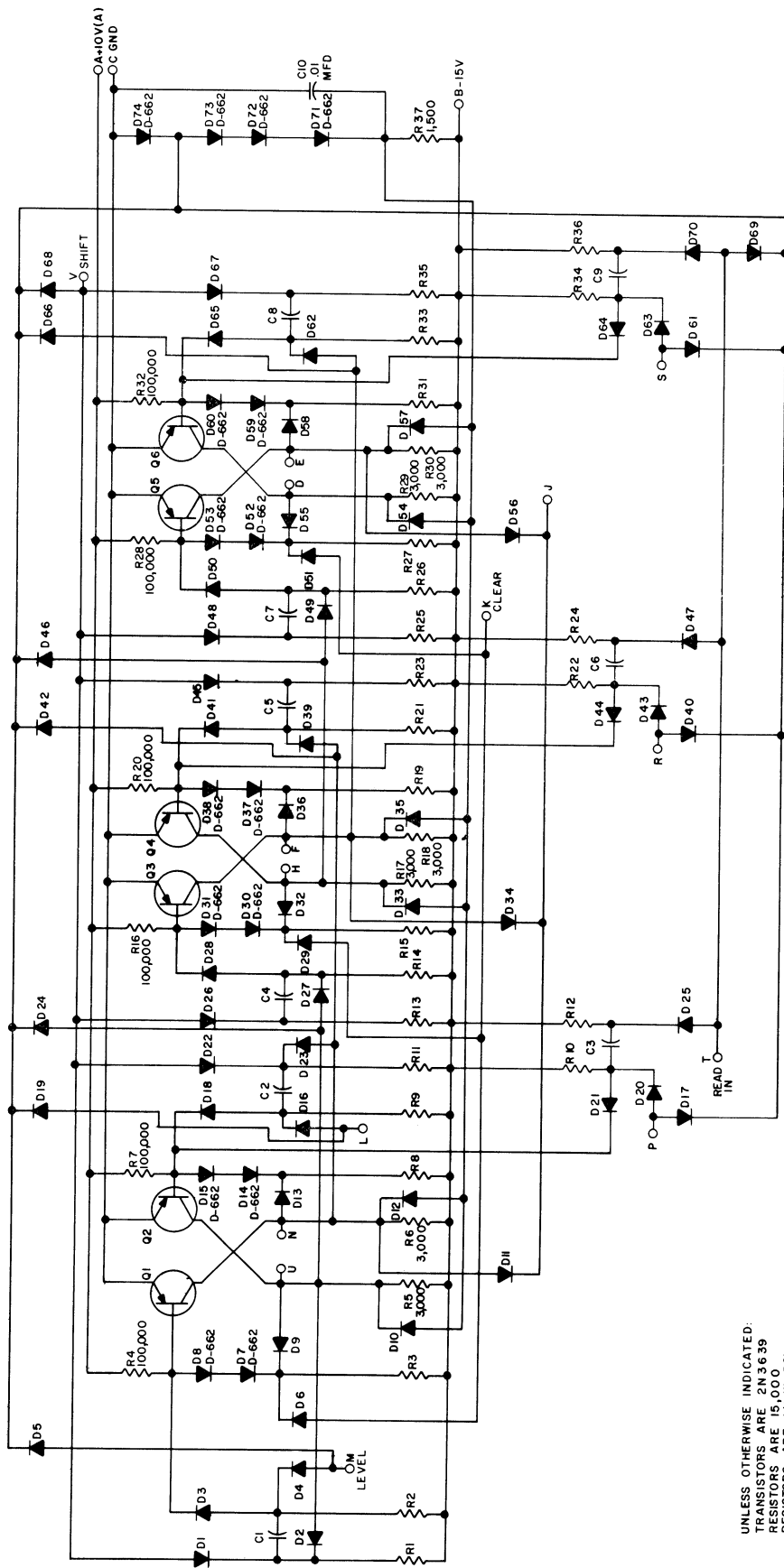


RS-D-R211 MA, MB, PC



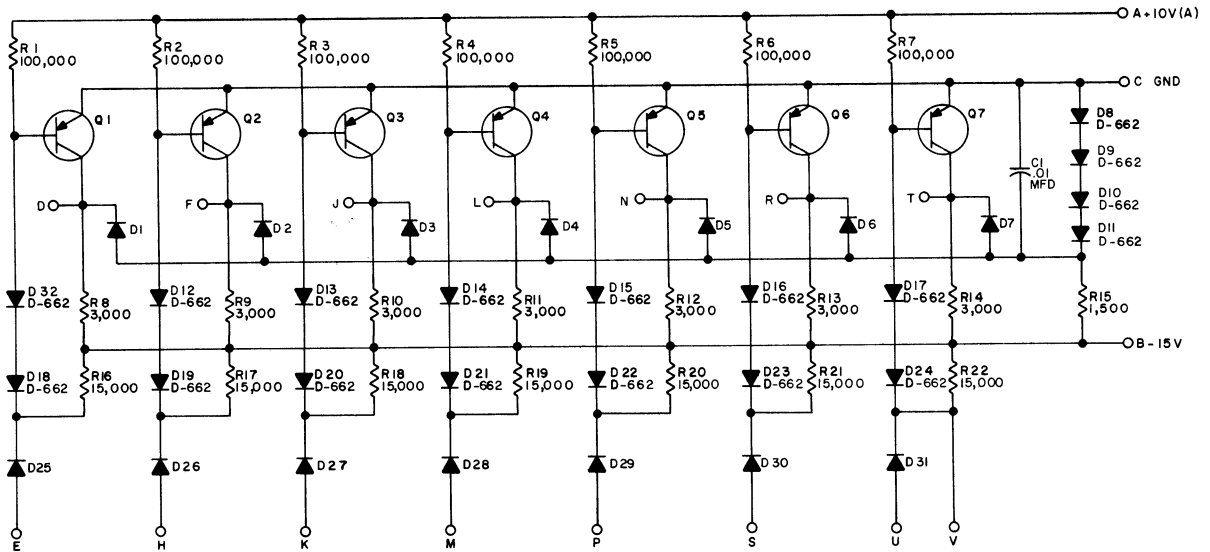
UNLESS OTHERWISE INDICATED:  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639  
 RESISTORS ARE 1/4W, 5%

RS-C-R212 MQ Register



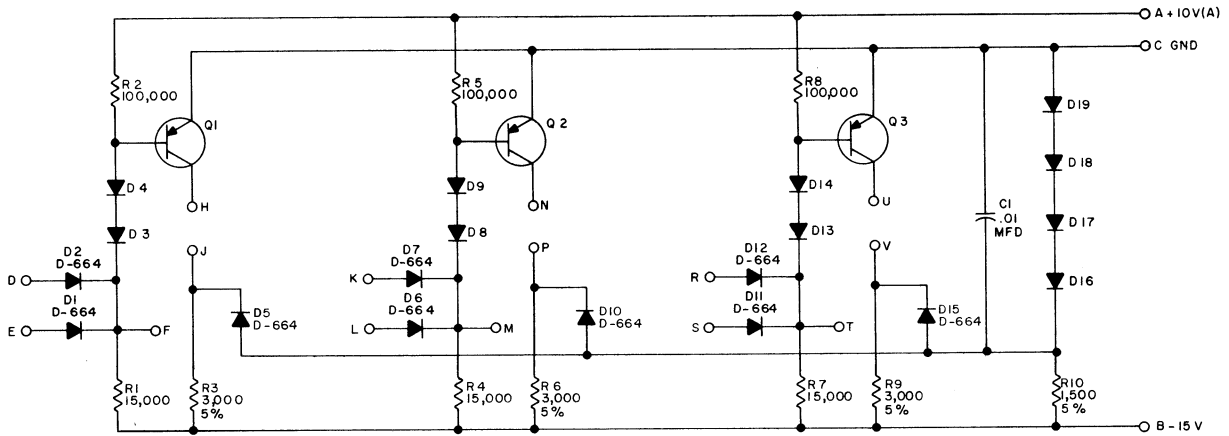
UNLESS OTHERWISE INDICATED:  
 TRANSISTORS ARE 2N3639  
 RESISTORS ARE 1/4 W 5%  
 CAPACITORS ARE 82MMFD  
 DIODES ARE D-664

RS-C-R220 3-Bit Shift Register



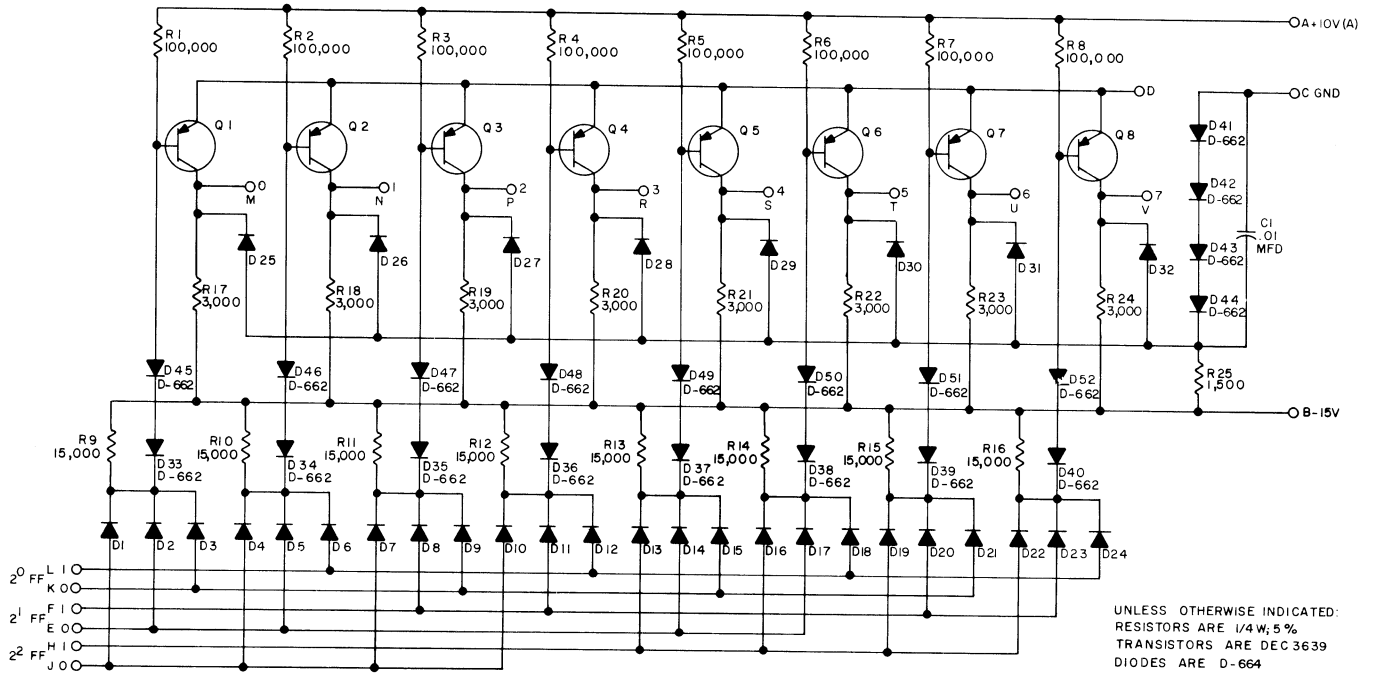
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4 W; 5%  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639

RS-B-S107 Inverter

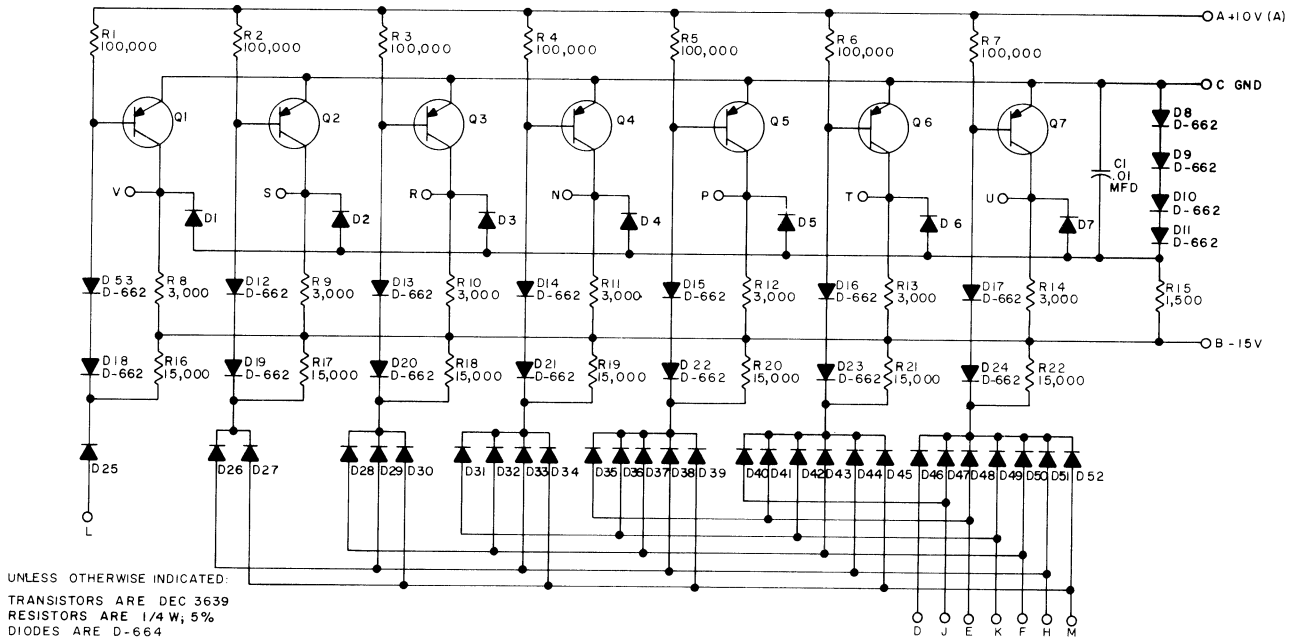


UNLESS OTHERWISE INDICATED:  
 TRANSISTORS ARE DEC 3639  
 RESISTORS ARE 1/4 W; 10%  
 DIODES ARE D-662

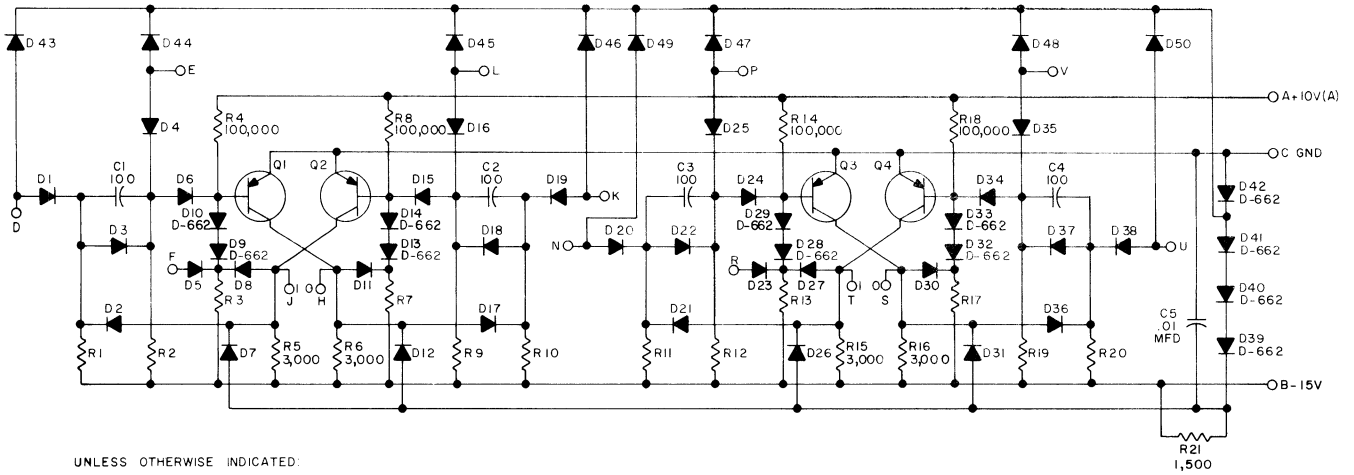
RS-B-S111 Diode Gate



RS-B-S151 Binary-to-Octal Decoder

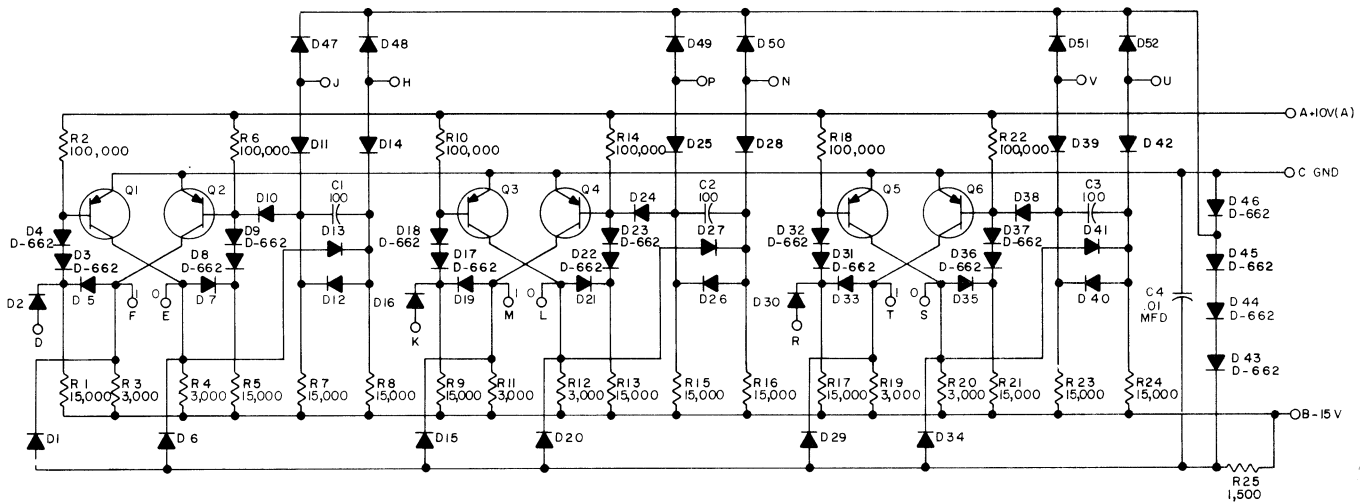


RS-B-S181 DC Carry Chain



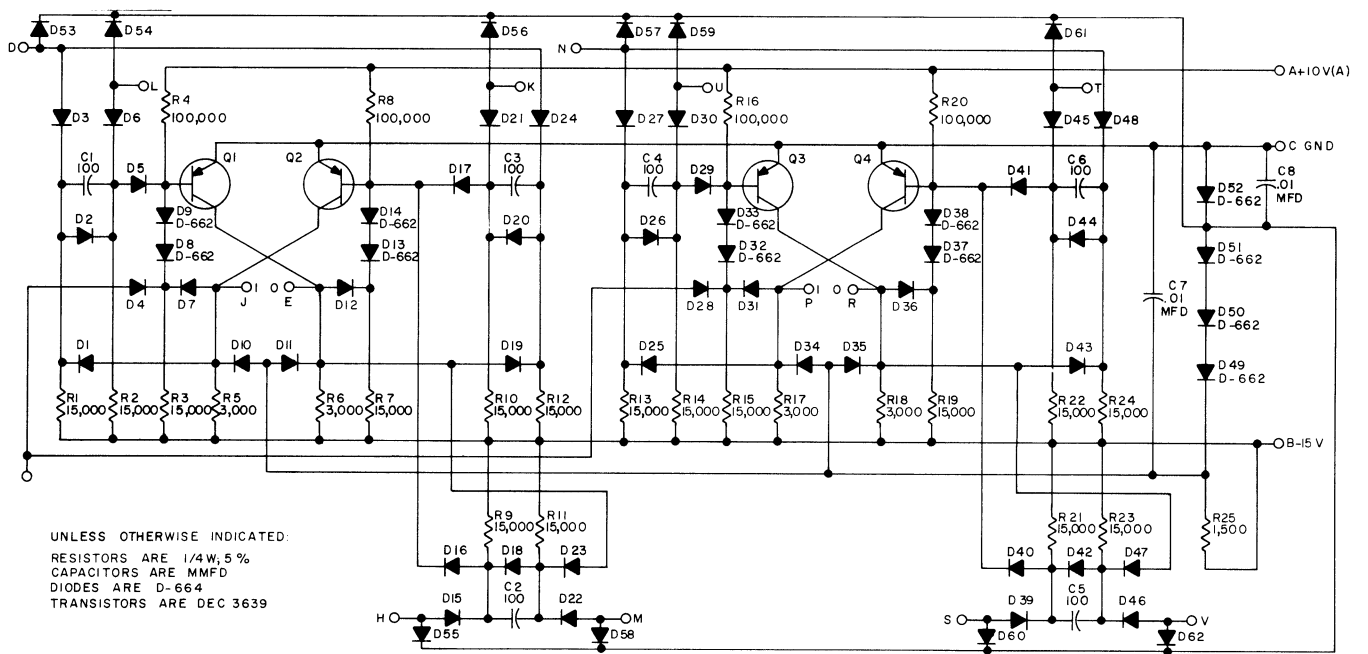
UNLESS OTHERWISE INDICATED:  
 TRANSISTORS ARE DEC 3639  
 RESISTORS ARE 15,000  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664

### RS-B-S202 Dual Flip-Flop

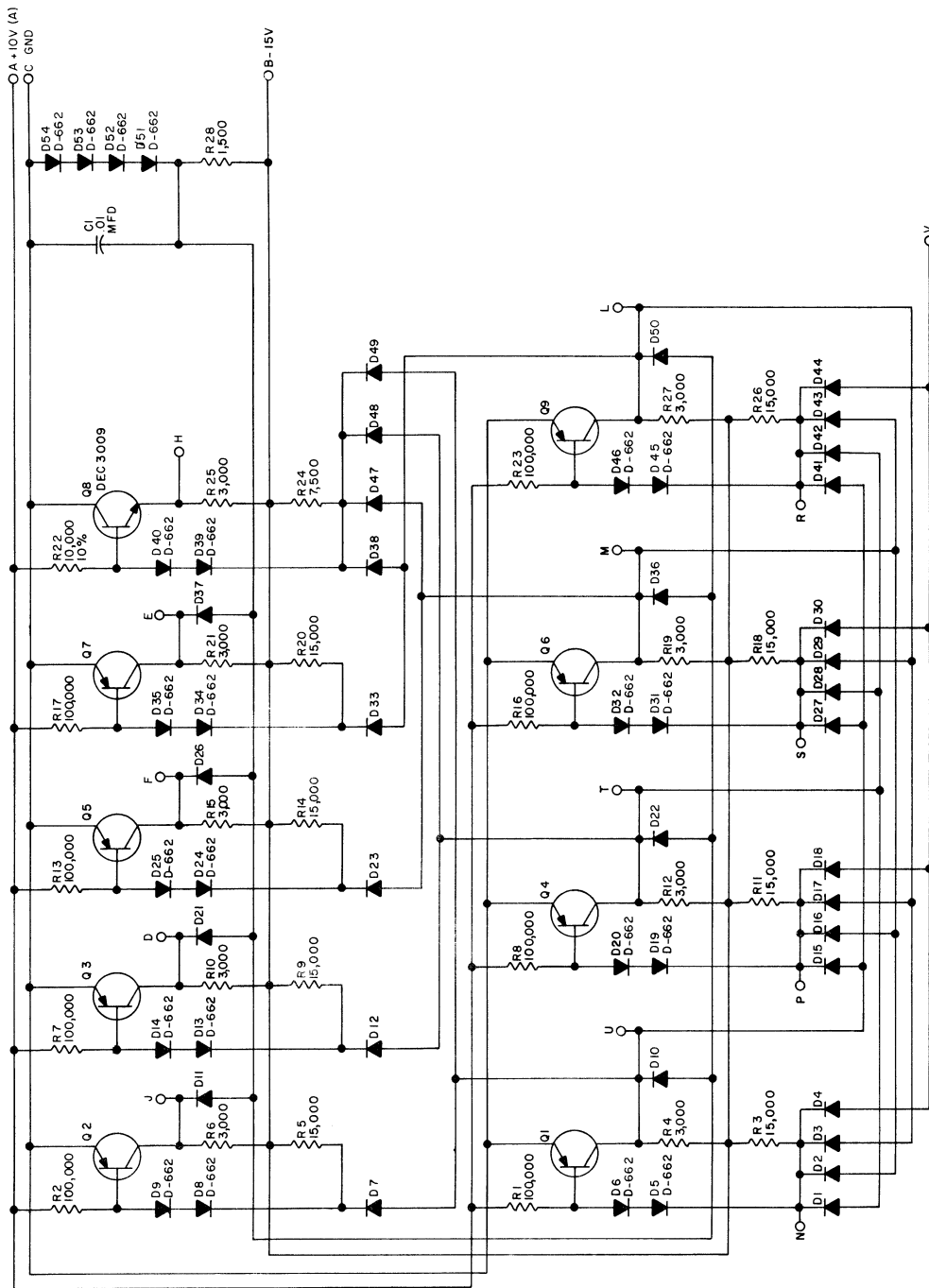


UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639

### RS-B-S203 Triple Flip-Flop

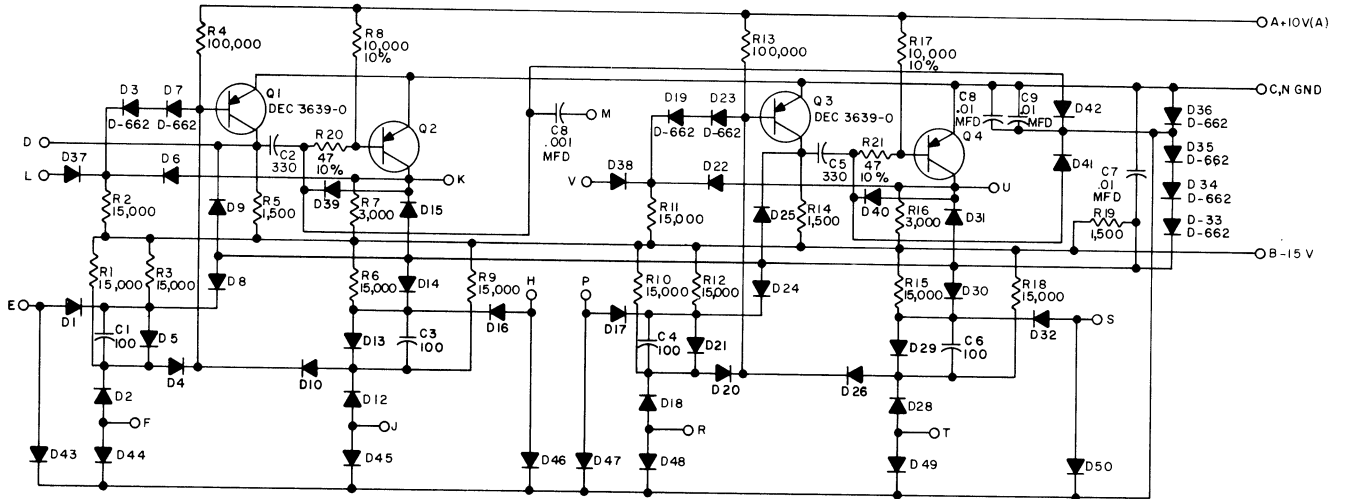


RS-B-S205 Dual Flip-Flop



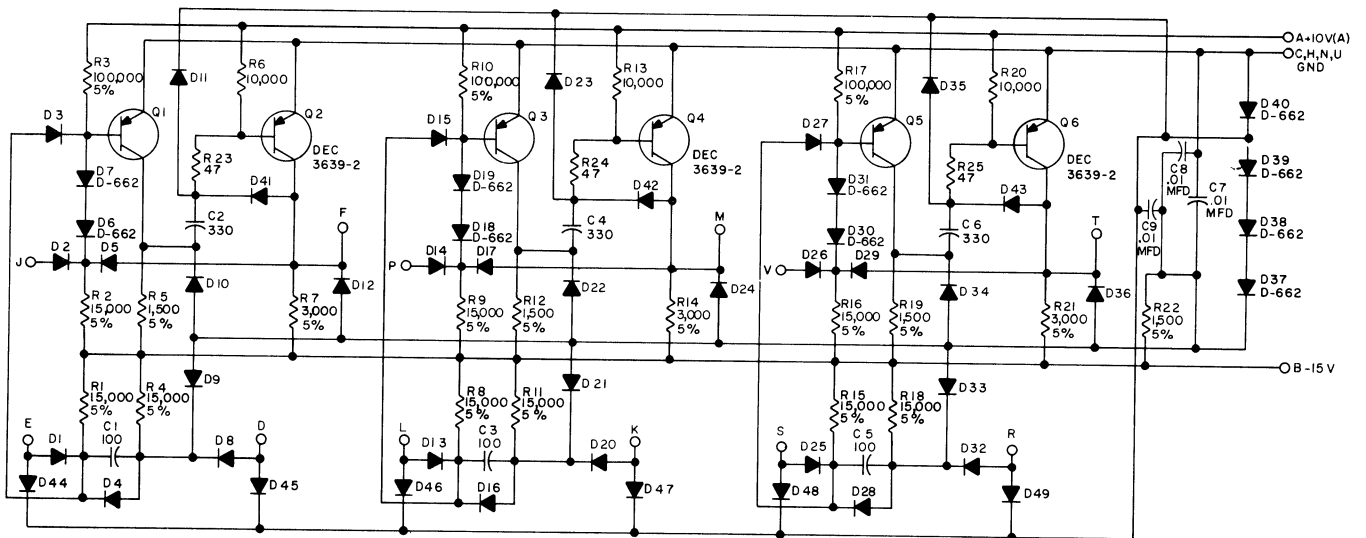
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4 W 15%  
 TRANSISTORS ARE DEC 3639  
 DIODES ARE D-664

RS-C-S284 Quadraflop



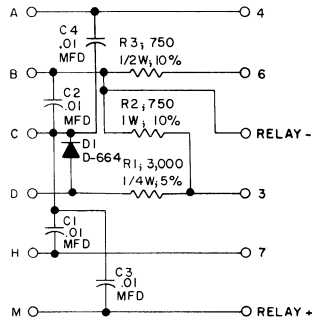
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4 W, 5%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639-2

### RS-B-S602 Pulse Amplifier

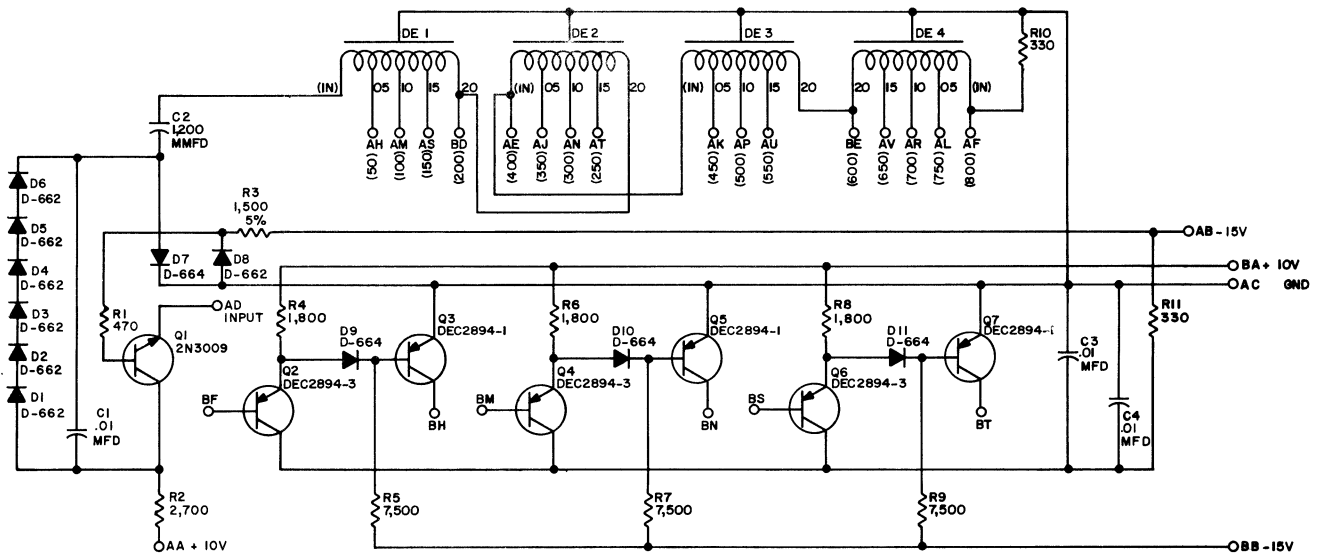


UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4 W, 10%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639-0

### RS-B-S603 Pulse Amplifier



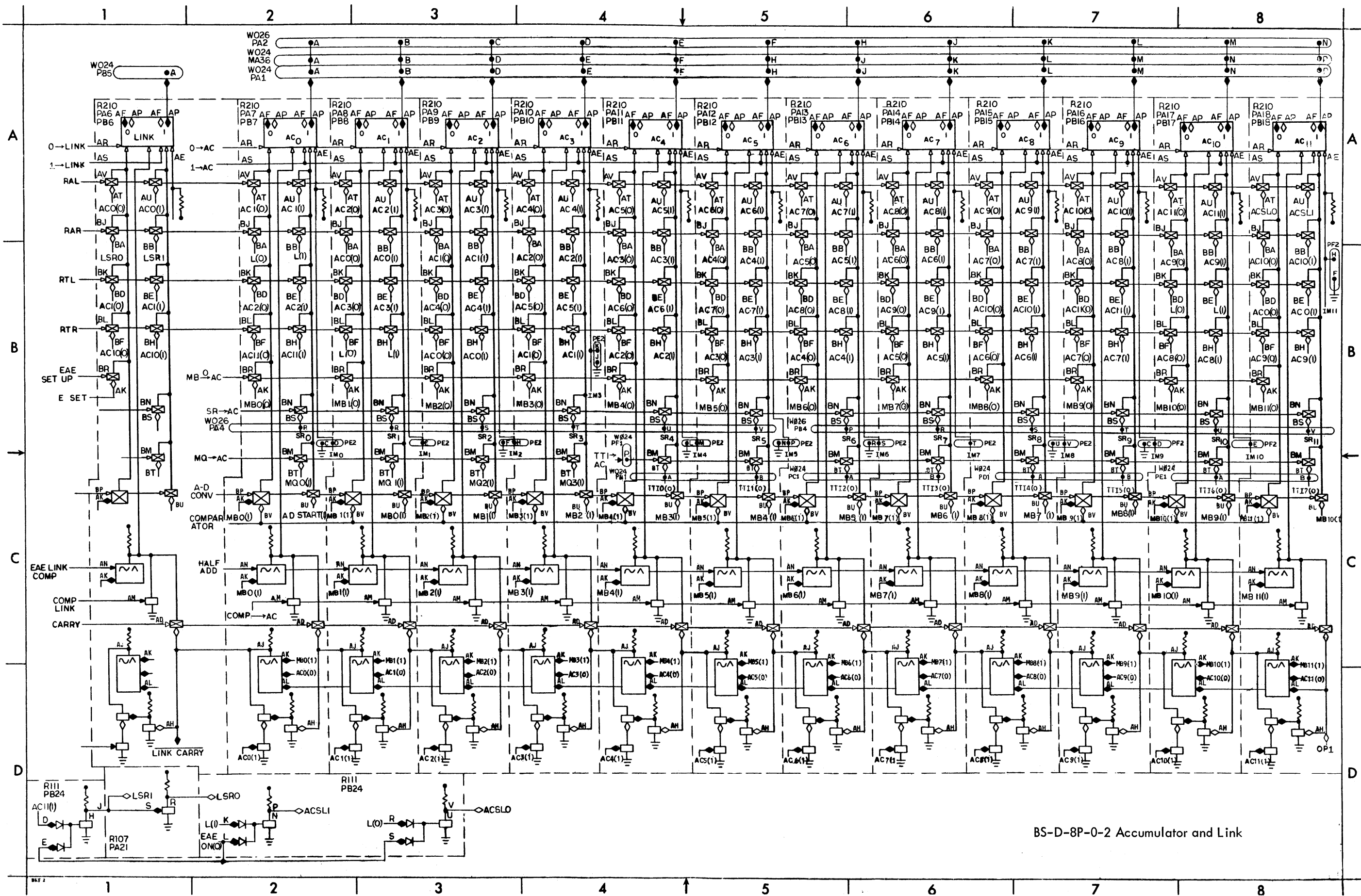
RS-B-W070 Teletype Connector



UNLESS OTHERWISE INDICATED:  
RESISTORS ARE 1/4W, 10%  
DE 1 - DE 4 ARE DEC NO. 330-25E-6

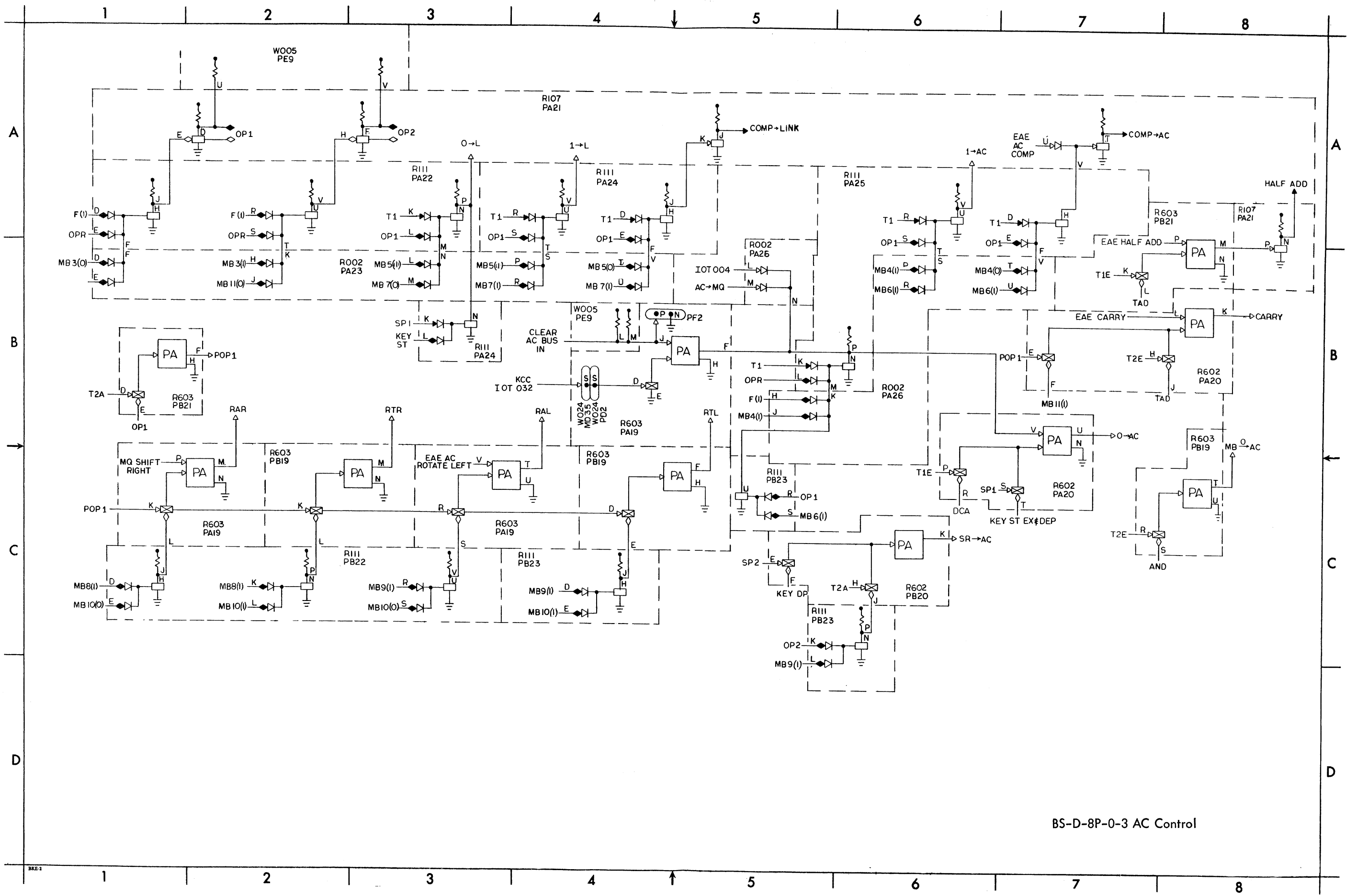
RS-B-W300 Delay Line





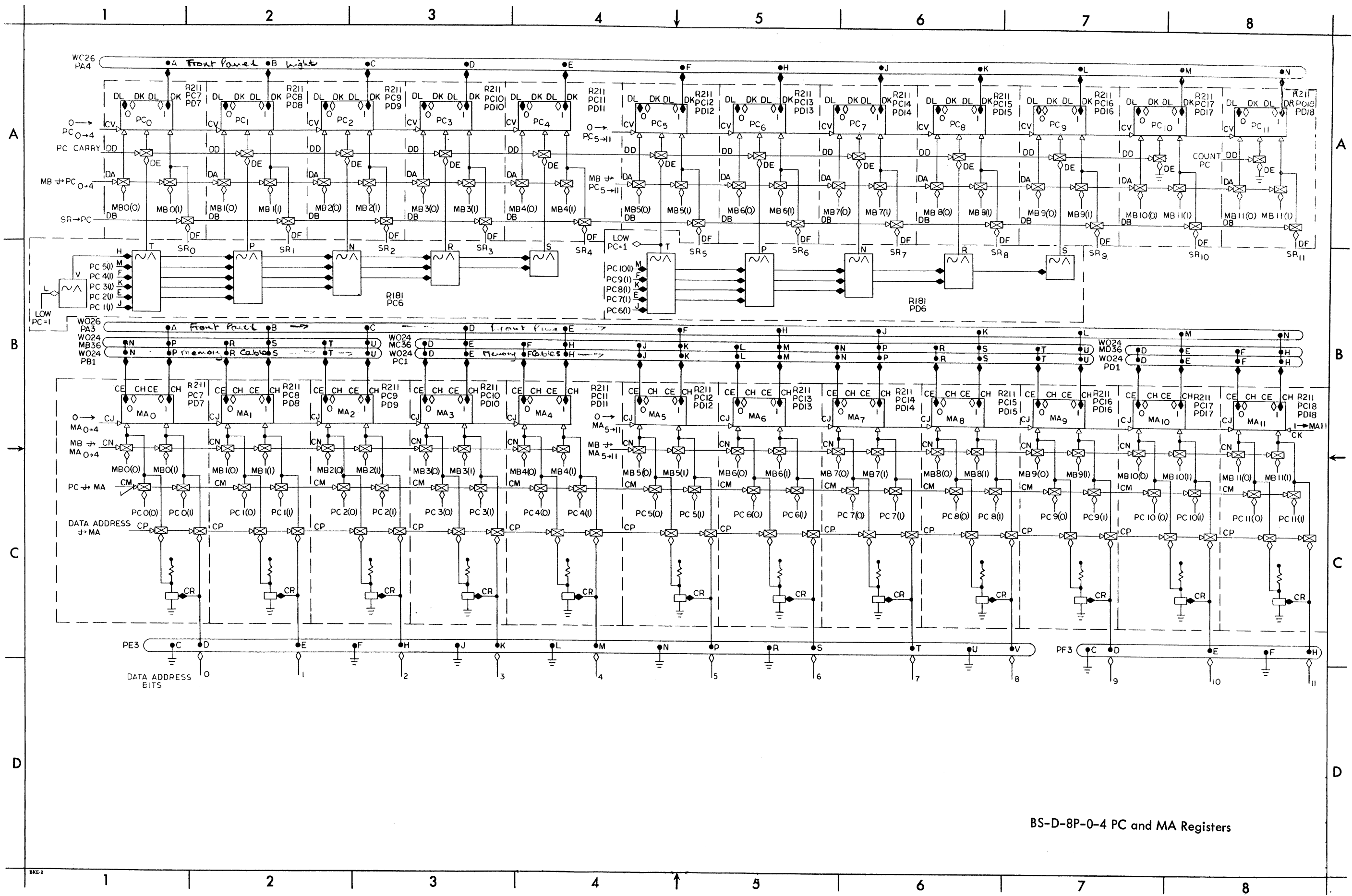
BS-D-8P-0-2 Accumulator and Link





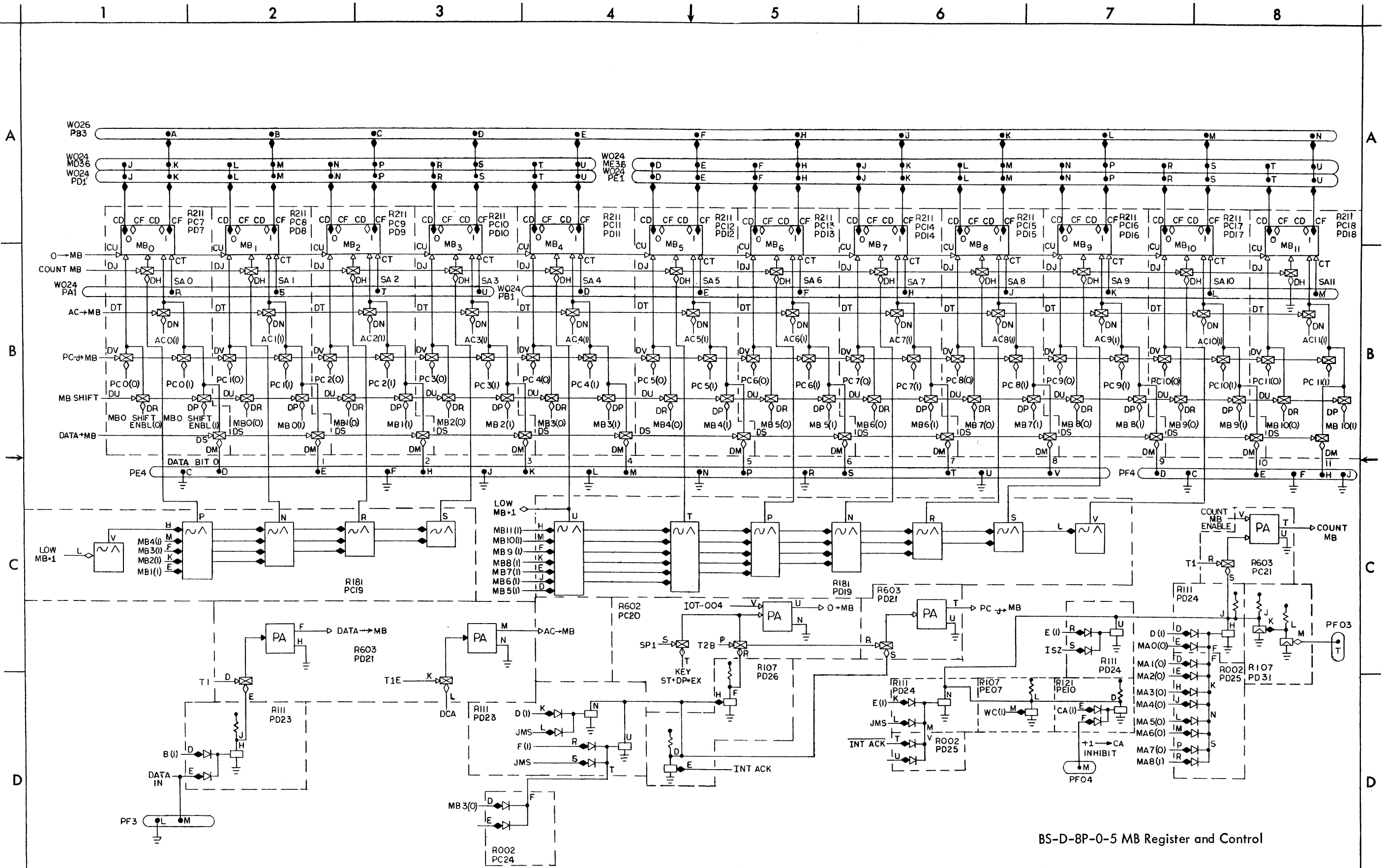
BS-D-8P-0-3 AC Control





BS-D-8P-0-4 PC and MA Registers





BS-D-8P-0-5 MB Register and Control

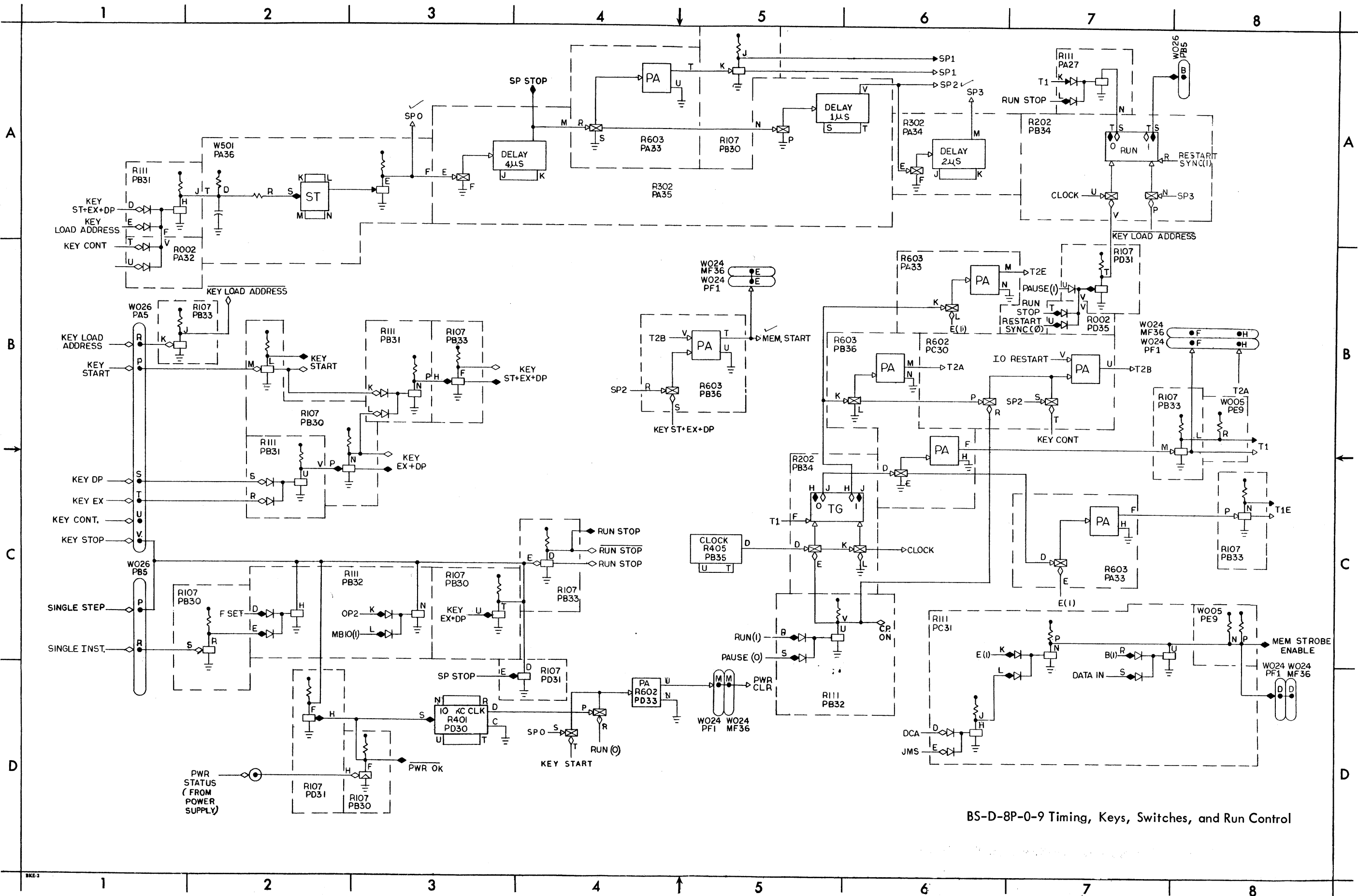






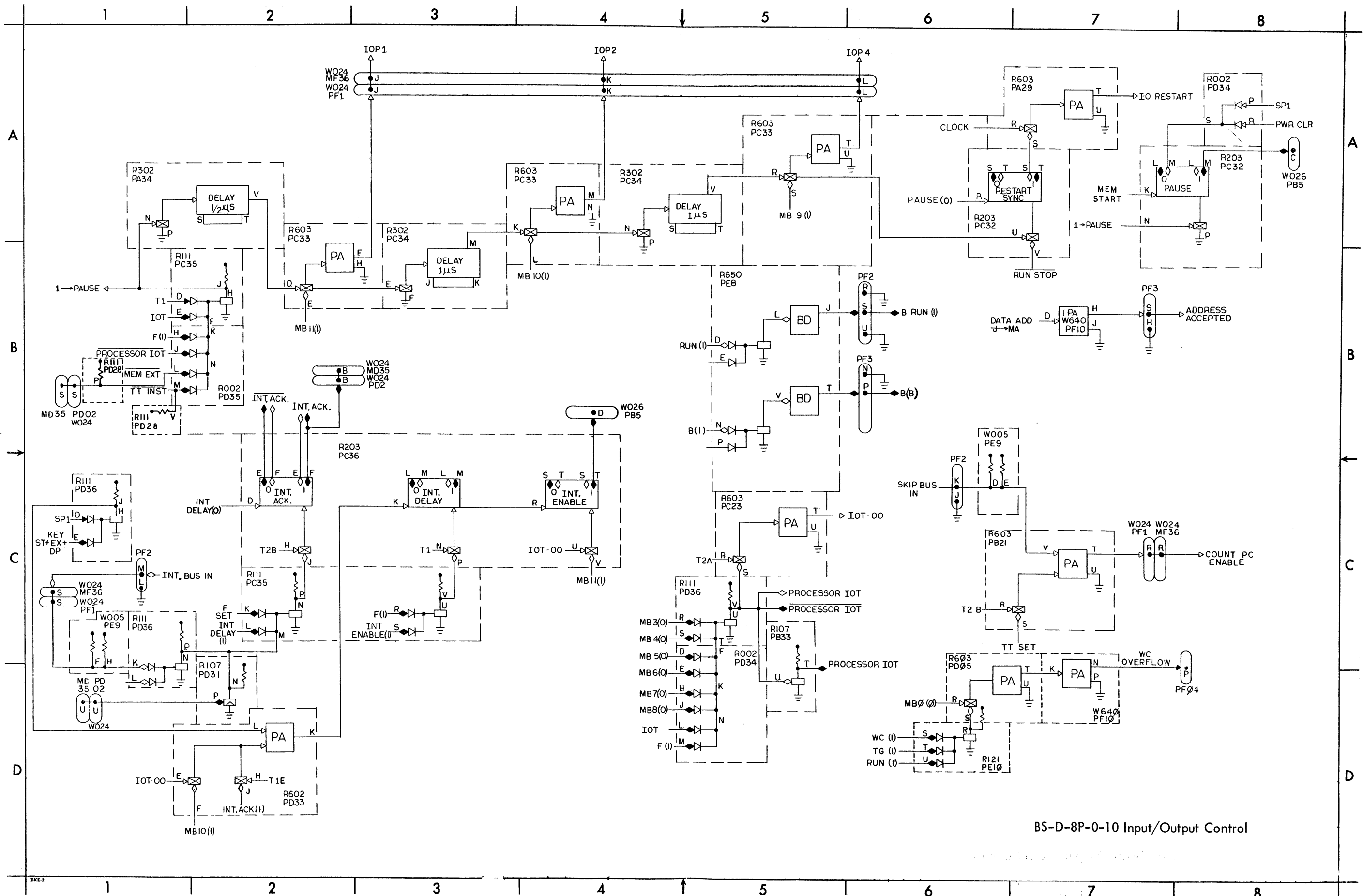






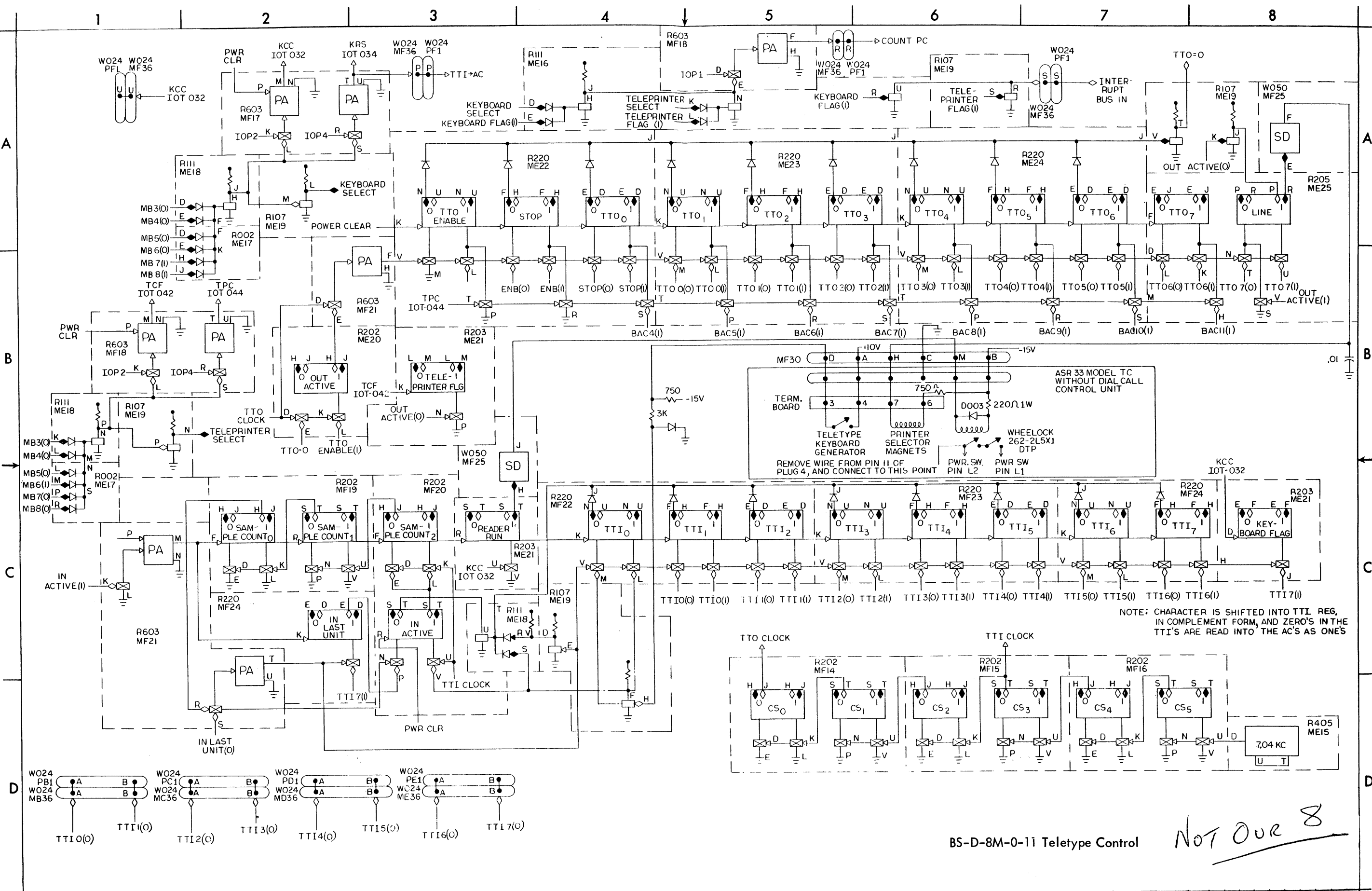
BS-D-8P-0-9 Timing, Keys, Switches, and Run Control





BS-D-8P-0-10 Input/Output Control

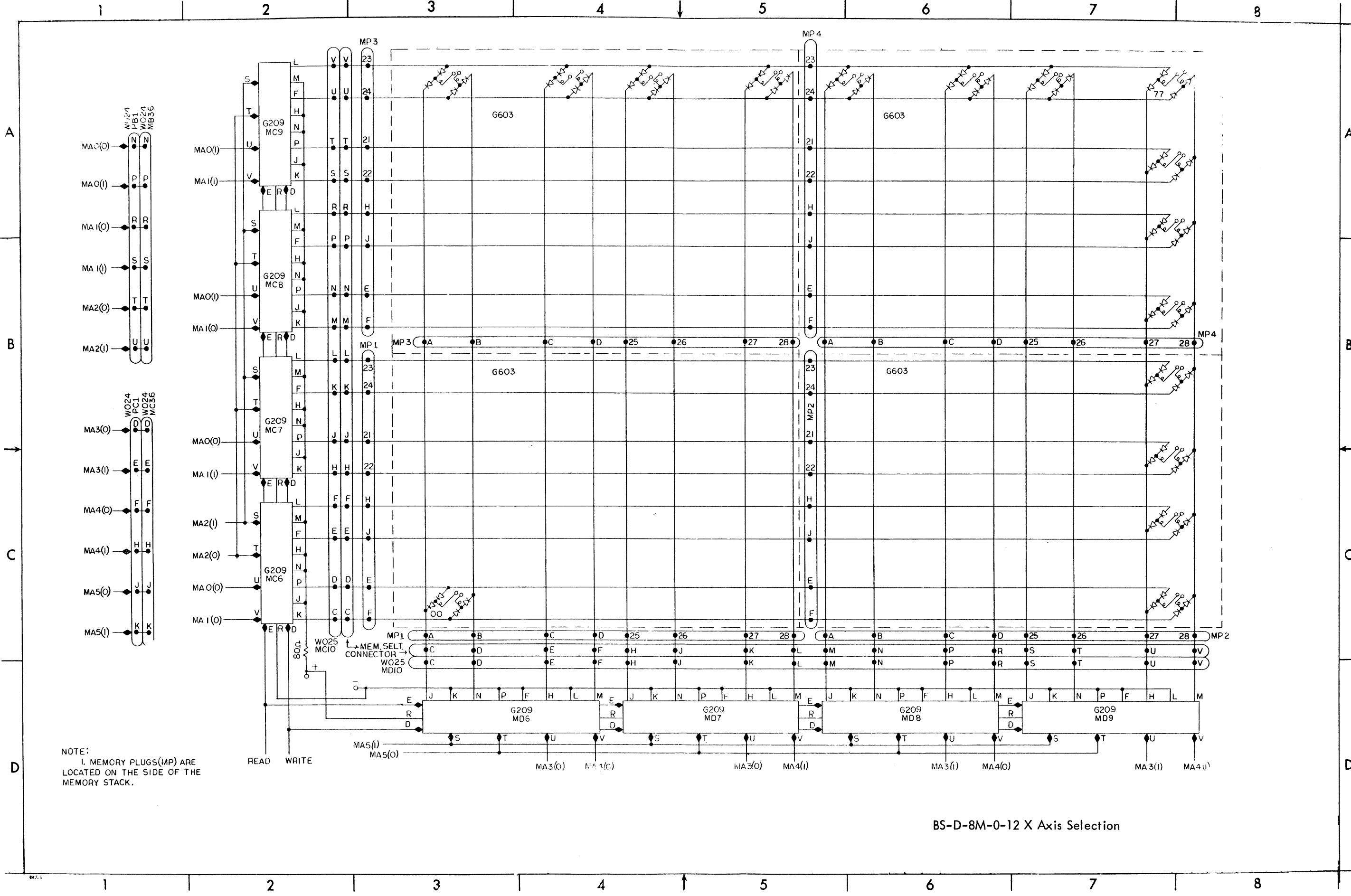




BS-D-8M-0-11 Teletype Control

NOT OUR 8

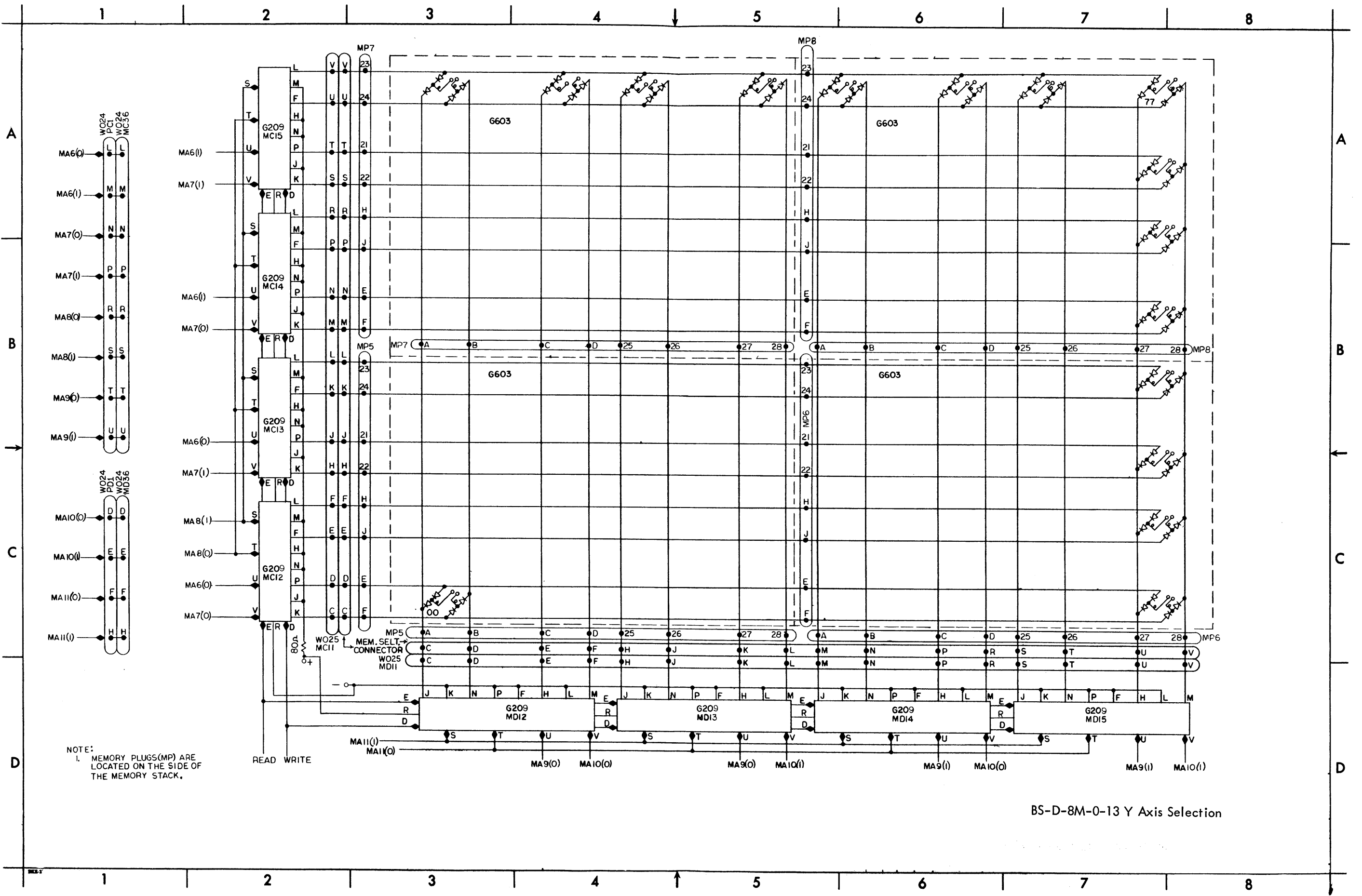
BS-D-8M-0-11 Teletype Control



NOTE:  
1. MEMORY PLUGS(MP) ARE  
LOCATED ON THE SIDE OF THE  
MEMORY STACK.

BS-D-8M-0-12 X Axis Selection

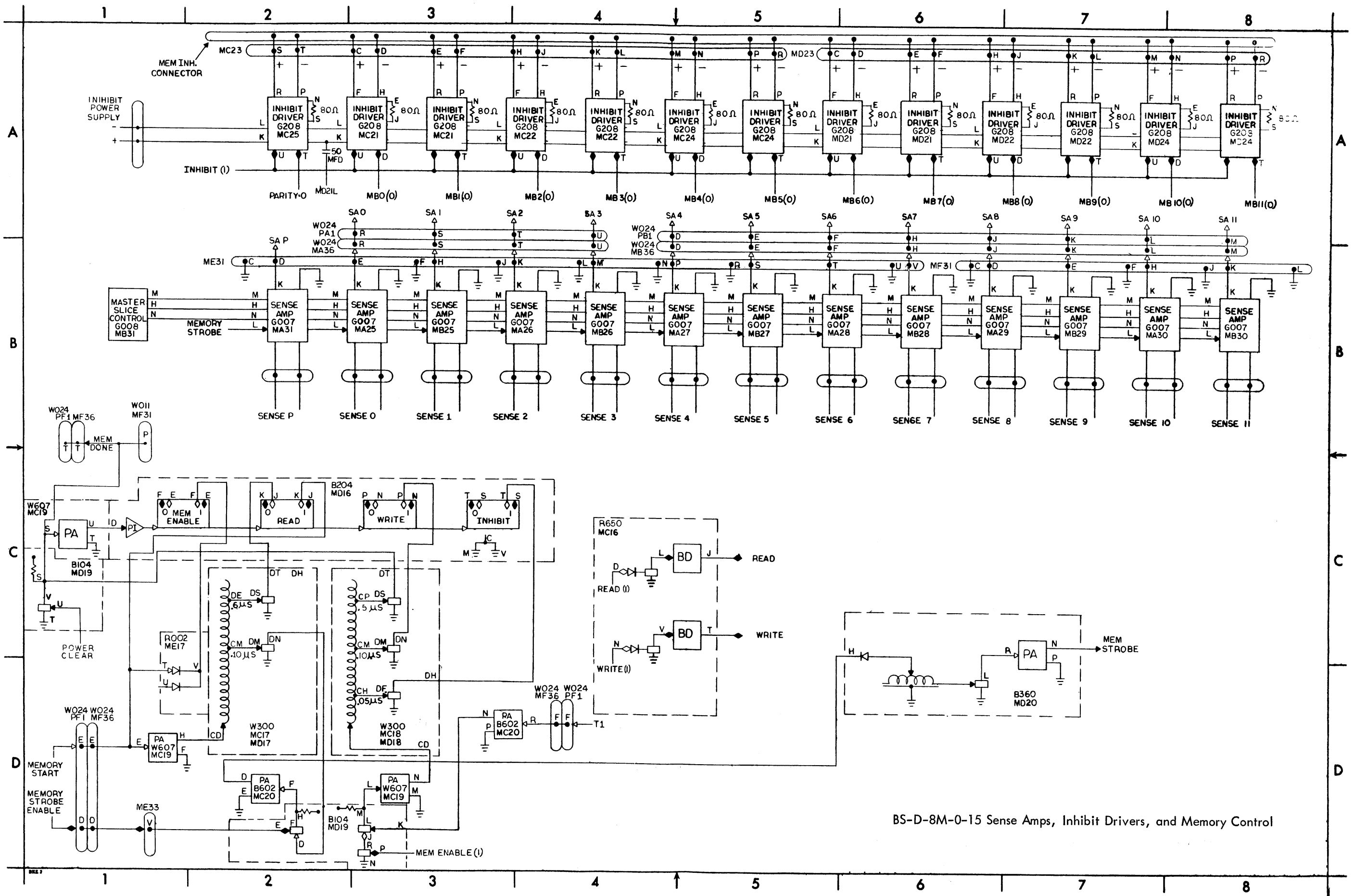
BS-D-8M-0-12 X Axis Selection



NOTE:  
1. MEMORY PLUGS(MP) ARE LOCATED ON THE SIDE OF THE MEMORY STACK.

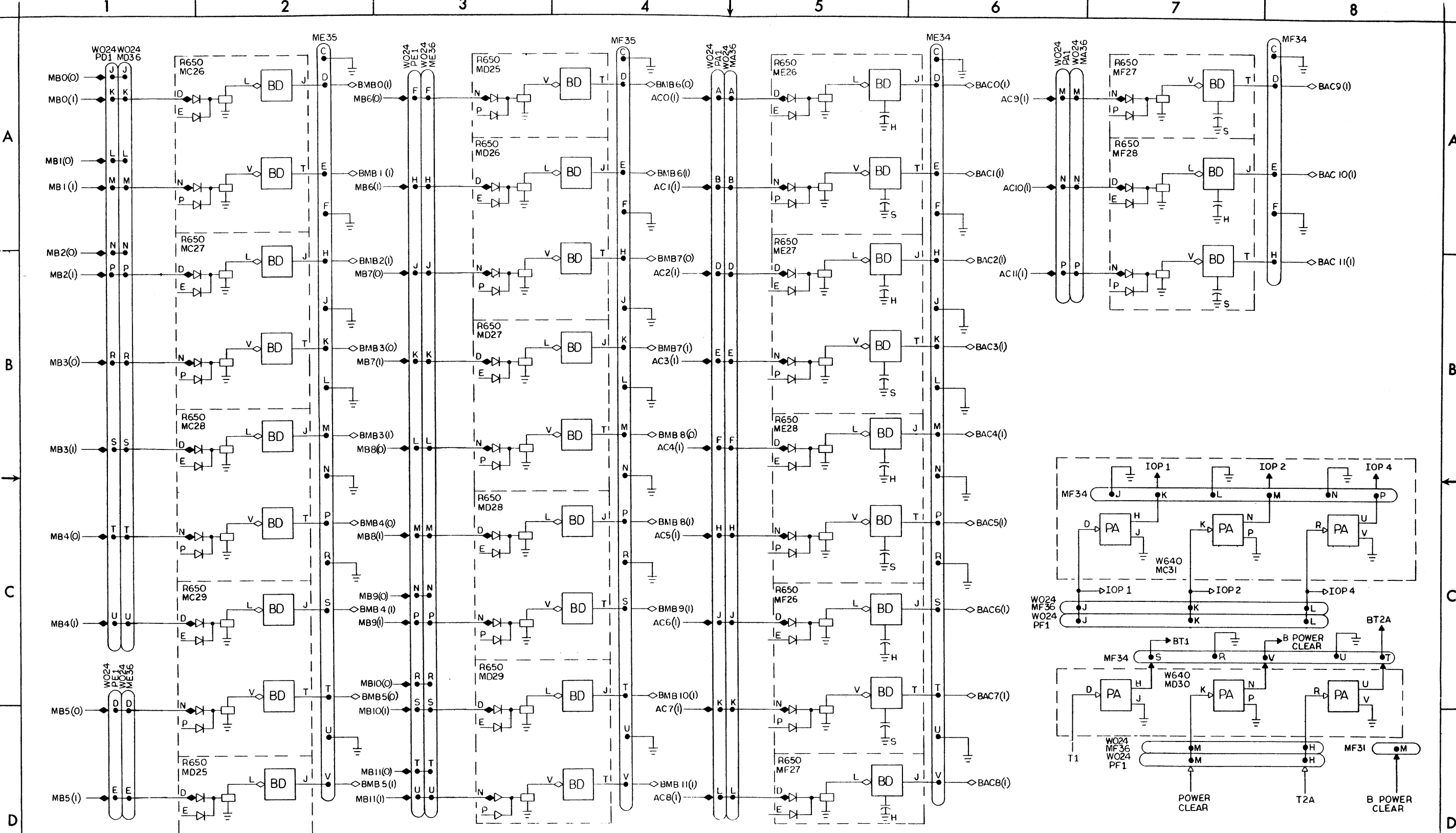
BS-D-8M-0-13 Y Axis Selection

BS-D-8M-0-13 Y Axis Selection



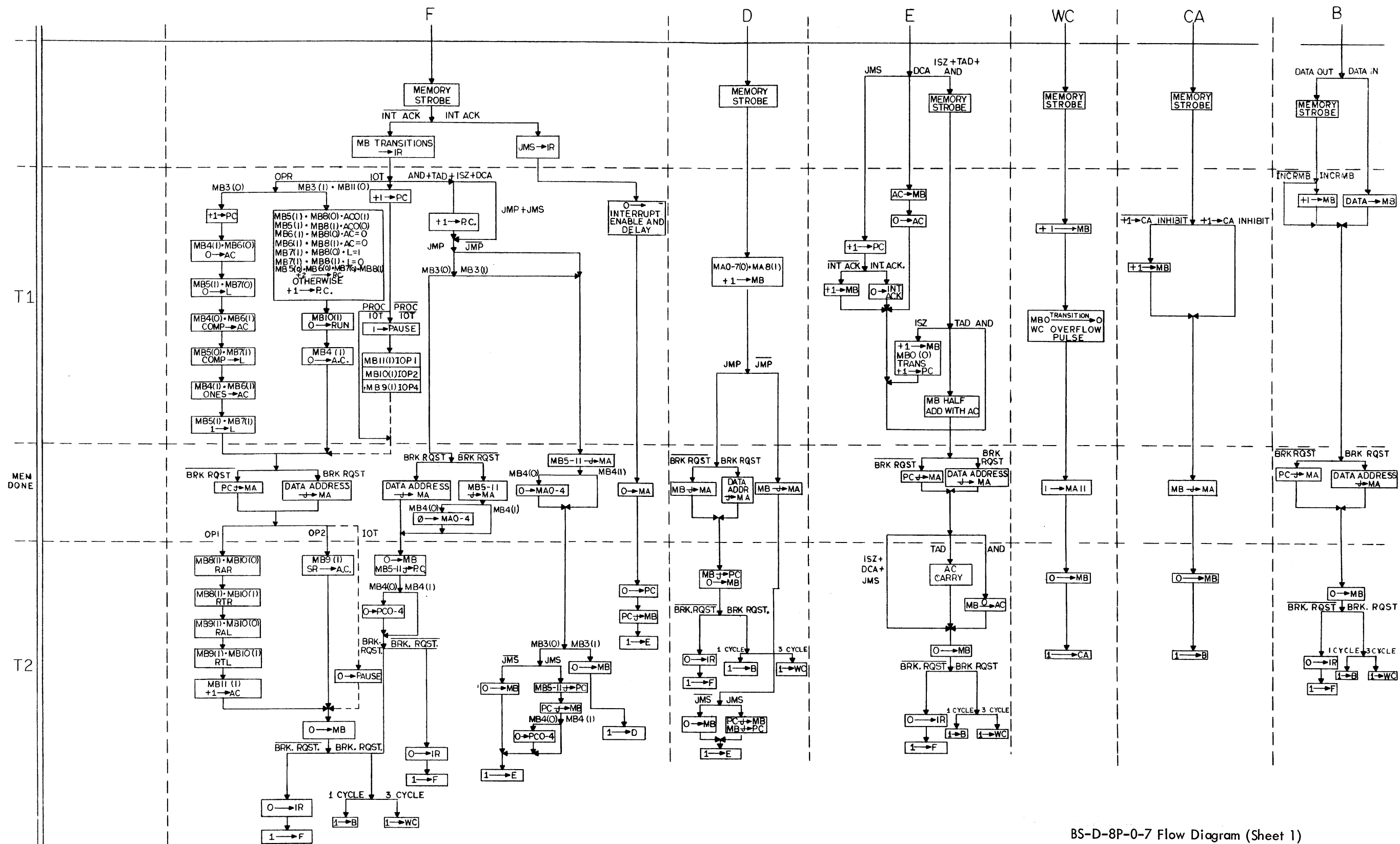
BS-D-8M-0-15 Sense Amps, Inhibit Drivers, and Memory Control





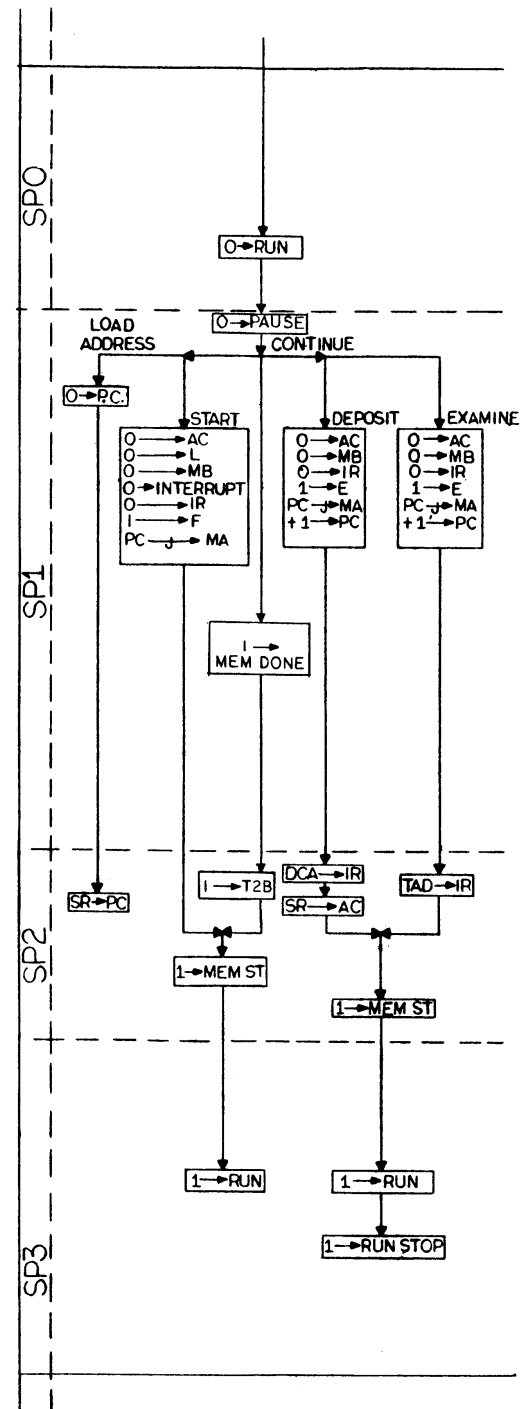
BS-D-8M-0-16 In/Out Buffers



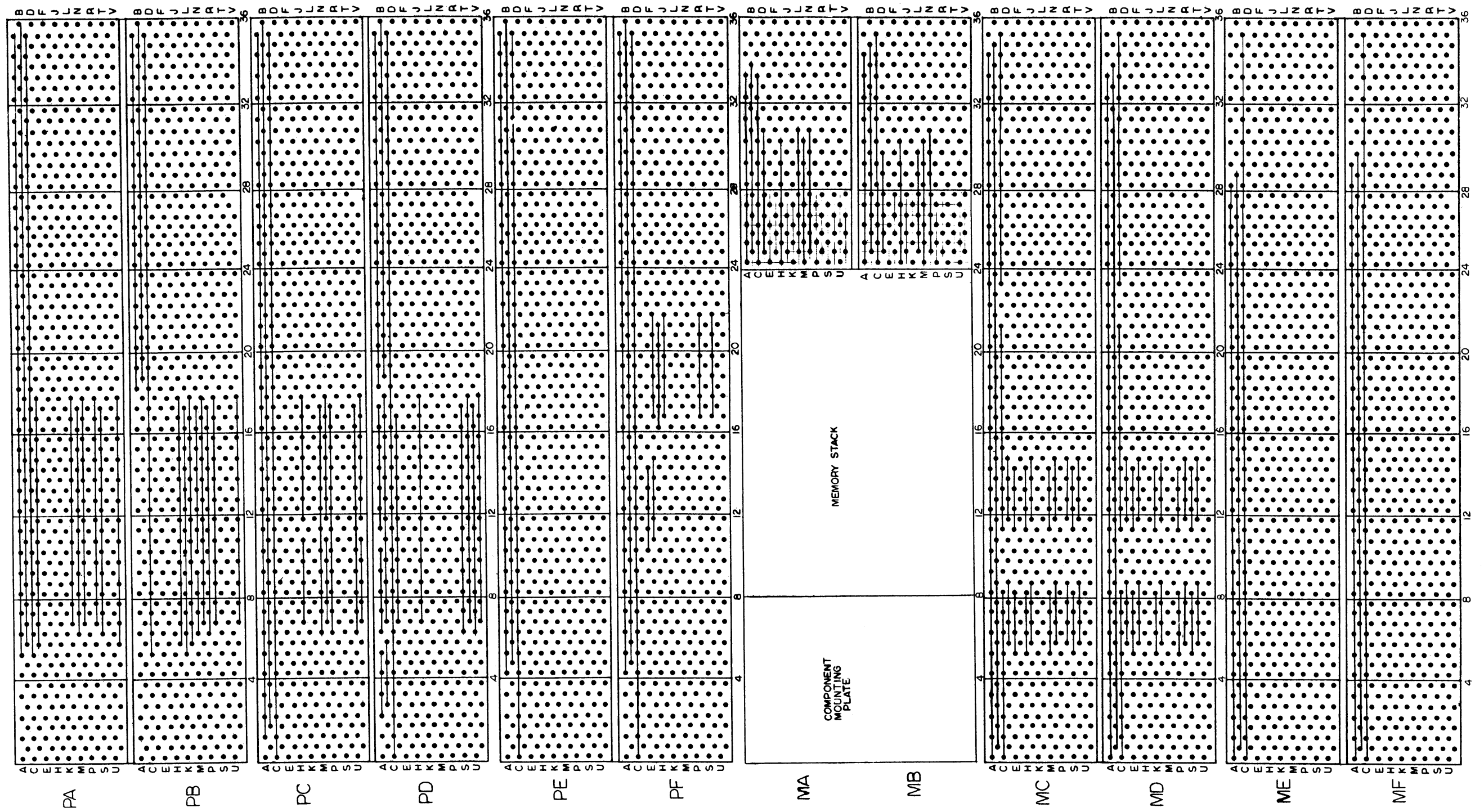


BS-D-8P-0-7 Flow Diagram (Sheet 1)









WD-D-8-0-14 Bus Bar for Power and Logic Wiring

WD-D-8-0-14 Bus Bar for Power and Logic Wiring

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
PA	W824	W826	W826	W826	W826	R210	R210	R210	R210	R210	R210	R210	R210	R210	R210	R210	R210	R210	5603	5602	5107	5111	R002	5111	5111	R002	5111	5602	5603	5111	5111	R002	5603	R302	R302	W501
	MEMORY CHASSIS CONNECTOR	INDICATOR CONNECTOR AC 9-11	INDICATOR CONNECTOR MA 9-11	INDICATOR CONNECTOR PC 9-11	INDICATOR CONNECTOR INSTR. STATES KEYS SR 9-5	LINC	AC 0	AC 1	AC 2	AC 3	AC 4	AC 5	AC 6	AC 7	AC 8	AC 9	AC 10	AC 11	CL AC BUS	CARRY	OP 1	OP 1	OP 1	COMP L	COMP AC	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2	0 → IR 2
PB	W824	5603	W826	W826	W826														5603	5602	5603	5111	5111	5111	5204	5107	5151	5203	5111	5107	5111	5111	5107	5202	R405	5603
	MEMORY CHASSIS CONNECTOR	T1B	INDICATOR CONNECTOR MB 9-11	INDICATOR CONNECTOR MQ 9-11	INDICATOR CONNECTOR LINK RUN P2055 ION SING STEP SING INST	LINC	AC 0	AC 1	AC 2	AC 3	AC 4	AC 5	AC 6	AC 7	AC 8	AC 9	AC 10	AC 11	RTL	SR → AC	POP 1	RAR	RTL	LSR 1	MAJOR STATES	TAD	IR DECODER	IR 1	KEY DP	KEY ST	KEY ST + EX + DP	KEY ST + EX + DP	KEY ST + EX + DP	KEY ST + EX + DP	KEY ST + EX + DP	KEY ST + EX + DP
PC	W824	5204	5603	R121	5111	5101	R211	R211	R211	R211	R211	R211	R211	R211	R211	R211	R211	R211	5101	5602	5603	5603	5603	R002	5111	5111	5111	5111	R002	5602	5111	5203	5603	R302	5111	5203
	MEMORY CHASSIS CONNECTOR	S	+	PC	SHIFT MB	HIGH PC CARRY	MB 0 MA 0 PC 0	MB 1 MA 1 PC 1	MB 2 MA 2 PC 2	MB 3 MA 3 PC 3	MB 4 MA 4 PC 4	MB 5 MA 5 PC 5	MB 6 MA 6 PC 6	MB 7 MA 7 PC 7	MB 8 MA 8 PC 8	MB 9 MA 9 PC 9	MB 10 MA 10 PC 10	MB 11 MA 11 PC 11	HIGH MB CARRY	PC → MA	0 → MA5-11	MB → MA5-11	SR → PC	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4	0 → MA8-4
PD	W824	W824	R113	R002	5603	5101													5101	5603	5603	5602	5111	5111	R002	5107	5111	5111	R002	R401	5107	5602	5602	R002	R002	5111
	MEMORY CHASSIS CONNECTOR	MEMORY CHASSIS CONNECTOR	T1S	TT INST	CA SET	LOW PC CARRY	MB 0 MA 0 PC 0	MB 1 MA 1 PC 1	MB 2 MA 2 PC 2	MB 3 MA 3 PC 3	MB 4 MA 4 PC 4	MB 5 MA 5 PC 5	MB 6 MA 6 PC 6	MB 7 MA 7 PC 7	MB 8 MA 8 PC 8	MB 9 MA 9 PC 9	MB 10 MA 10 PC 10	MB 11 MA 11 PC 11	LOW MB CARRY	PC CARRY	DATA MB	0 → PC5-11	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB	0 → MB
PE	W824	W811	W811	W811	R123	5107	5107	R050	W805	R121	A502	5203	R401	R302	5603	A704	5111	R123	R123	5111	R002	5107	5603	R002	5205	5111	5111	R002	5603	5107	5603	5203	5203	5111	5111	5111
	MEMORY CHASSIS CONNECTOR	IN-OUT CONNECTOR IM 9-8	IN-OUT CONNECTOR DATA ADDRESS 9-8	IN-OUT CONNECTOR DATA BITS 9-8	INTERRUPT	MB 0	C SET + S SET	SPEC. CYCLE	B RUN	LOADS THROUGH R	B SET	COMPARATOR	AD ENABLE	AD CONV.	AD CONV.	SHIFT MB	ACSL 0	IM 4	IM 5	IM 6	IM 7	IM 8	IM 9	IM 10	IM 11	IM 4	IM 8	IM 10	IM 4	IM 8	IM 10	IM 4	IM 8	IM 10	IM 4	IM 8
PF	W824	W811	W811	W811	5107	R002	R302	W501	5602	W600	A604	A604	A604	A601	A601		R212	R212	R212	R212	R212	R212	5602	5111	5205	5205	5205	5603	5111	5602	5111	5111	R002	5111	R002	R405
	MEMORY CHASSIS CONNECTOR	IN-OUT CONNECTOR IM 9-11	IN-OUT CONNECTOR DATA ADDRESS 9-11	IN-OUT CONNECTOR DATA BITS 9-11	INTERRUPT	PWR OK	RESTART	RESTART	POWER STATUS	PWR RESTART	WC OVERFLOW	D-A CONV. 2 BITS	D-A CONV. 2 BITS	D-A CONV. 2 BITS	D-A CONV. 3 BITS	D-A CONV. 3 BITS	REF. SUPPLY	MQ 0	MQ 1	MQ 2	MQ 3	MQ 4	MQ 5	MQ 6	MQ 7	MQ 8	MQ 9	MQ 10	MQ 11	MQ SHIFT RIGHT	MQ SHIFT LEFT	MQ SHIFT LEFT SWITCH	ATG 2	SC 1	SC 3	SC 0

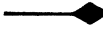







\* USED ONLY WITH #182 EAE. *Not fitted*  
 △ USED ONLY WITH #189 A-D CONVERTER *Not fitted*  
 □ USED ONLY WITH KRO1 POWER INTERRUPT *Not fitted*  
 ☆ USED ONLY WITH 681 DATA LINE INTERFACE *Not fitted*















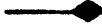























JACK <input type="checkbox"/>	PLUG <input checked="" type="checkbox"/>	LOCATION, LENGTH, ROUTE
FEMALE <input type="checkbox"/>	MALE <input checked="" type="checkbox"/>	PB 03

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PB 03	A	MB 0 (1) 	
W/BRN (Z)		B	 1 (1) 	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	 10 (1) 	
W/BRN (Z)	PB 03	N	MB 11 (1) 	
W/RED (R)		P		
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

JACK <input type="checkbox"/> PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE		
FEMALE <input type="checkbox"/> MALE <input checked="" type="checkbox"/>		PA 02		
COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PA 02	A	AC 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)	PA 02	N	AC 11 (1)	
W/RED (R)		P		
W/ORN (O)		R		
W/YEL (Y)		S		
W/GRN (N)		T		
W/BLU (B)		U		
W/VIO (V)		V		
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

CL-A-8P-0-26 Indicator Connectors for AC Bits

JACK <input type="checkbox"/> PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE		
FEMALE <input type="checkbox"/> MALE <input checked="" type="checkbox"/>		PA03		
COLOR	LOCATION	PIN	NAME	REMARKS
W/ BLK (X)	PA 03	A	MA 0 (1) 	
W/ BRN (Z)		B	 1 (1) 	
W/ RED (R)		C	2 (1)	
W/ ORN (O)		D	3 (1)	
W/ YEL (Y)		E	4 (1)	
W/ GRN (N)		F	5 (1)	
W/ BLU (B)		H	6 (1)	
W/ VIO (V)		J	7 (1)	
W/ GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/ BLK (X)		M	 10 (1) 	
W/ BRN (Z)	PA 03	N	MA11 (1) 	
W/ RED (R)		P		
W/ ORN (O)		R		
W/ YEL (Y)		S		
W/ GRN (N)		T		
W/ BLU (B)		U		
W/ VIO (V)		V		
W/ GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

JACK <input type="checkbox"/> PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE		
FEMALE <input type="checkbox"/> MALE <input checked="" type="checkbox"/>		PA 04		
COLOR	LOCATION	PIN	NAME	REMARKS
W/ BLK (X)	PA 04	A	PC 0 (1) 	
W/ BRN (Z)		B	 1 (1) 	
W/ RED (R)		C	2 (1)	
W/ ORN (O)		D	3 (1)	
W/ YEL (Y)		E	4 (1)	
W/ GRN (N)		F	5 (1)	
W/ BLU (B)		H	6 (1)	
W/ VIO (V)		J	7 (1)	
W/ GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/ BLK (X)		M	 10 (1) 	
W/ BRN (Z)		N	PC 11 (1) 	
W/ RED (R)		P	SR 0	
W/ ORN (O)		R	 1	
W/ YEL (Y)		S	2	
W/ GRN (N)		T	3	
W/ BLU (B)		U	 4	
W/ VIO (V)	PA 04	V	SR 5	
W/ GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

JACK <input type="checkbox"/>		PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE PA 05	
FEMALE <input type="checkbox"/>		MALE <input checked="" type="checkbox"/>			
COLOR	LOCATION	PIN	NAME	REMARKS	
W/BLK (X)	PA 05	A	AND (0)		
W/BRN (Z)	↑	B	TAD (1)		
W/RED (R)		C	ISZ (2)		
W/ORN (O)		D	DCA (3)		
W/YEL (Y)		E	JMS (4)		
W/GRN (N)		F	JMP (5)		
W/BLU (B)		H	IOT (6)		
W/VIO (V)		J	OPR (7)		
W/GRY (G)		K	FETCH (F)		
WHT (W)		L	EXECUTE (E)		
W/BLK (X)		M	DEFER (D)		
W/BRN (Z)		N	BREAK (B)		
W/RED (R)		P	KEY START		
W/ORN (O)		R	KEY LOAD ADDRESS		
W/YEL (Y)		S	KEY DP		
W/GRN (N)		T	KEY EX		
W/BLU (B)	↓	U	KEY CONT		
W/VIO (V)	PA 05	V	KEY STOP		
W/GRY (G)		W			
WHT (W)		X			
		Y			
		Z			

JACK <input type="checkbox"/>		PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE	
FEMALE <input type="checkbox"/>		MALE <input checked="" type="checkbox"/>		PAØ1 & MA36	
COLOR	PIN	PIN	NAME	REMARKS	
W/BLK (X)	PAØ1A	MA36A	AC0(1)		
W/BRN (Z)	PAØ1B	MA36B	AC1(1)		
W/RED (R)	↑ C	↑ C	GND		
W/ORN (O)	D	D	AC2(1)		
W/YEL (Y)	E	E	3(1)		
W/GRN (N)	F	F	4(1)		
W/BLU (B)	H	H	5(1)		
W/VIO (V)	J	J	6(1)		
W/GRY (G)	K	K	7(1)		
WHT (W)	L	L	8(1)		
W/BLK (X)	M	M	9(1)		
W/BRN (Z)	N	N	10(1)		
W/RED (R)	P	P	AC11(1)		
W/ORN (O)	R	R	SA 0		
W/YEL (Y)	S	S	↑ 1		
W/GRN (N)	T	T	↓ 2		
W/BLU (B)	↓ U	↓ U	SA 3		
W/VIO (V)	PAØ1V	MA36V	GND		

JACK <input type="checkbox"/> PLUG <input checked="" type="checkbox"/> FEMALE <input type="checkbox"/> MALE <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE PBØ1 & MB36		
COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PBØ1A	MB36A	TTI 0(1)	
W/BRN (Z)	↑ B	↑ B	TTI 1(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	SA 4	
W/YEL (Y)	E	E	↑ 5	
W/GRN (N)	F	F	6	
W/BLU (B)	H	H	7	
W/VIO (V)	J	J	8	
W/GRY (G)	K	K	9	
WHT (W)	L	L	↓ 10	
W/BLK (X)	M	M	SA 11	
W/BRN (Z)	N	N	MA 0(0)	
W/RED (R)	P	P	MA 0(1)	
W/ORN (O)	R	R	MA 1(0)	
W/YEL (Y)	S	S	MA 1(1)	
W/GRN (N)	T	T	MA 2(0)	
W/BLU (B)	↓ U	↓ U	MA 2(1)	
W/VIO (V)	PBØ1V	MB36V	GND	

JACK <input type="checkbox"/>		PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE	
FEMALE <input type="checkbox"/>		MALE <input checked="" type="checkbox"/>		PCØ1 & MC36	
COLOR	PIN	PIN	NAME	REMARKS	
W/BLK (X)	PCØ1A	MC36A	TTI2(1)		
W/BRN (Z)	↑ B	↑ B	TTI3(1)		
W/RED (R)	C	C	GND		
W/ORN (O)	D	D	MA 3(0)		
W/YEL (Y)	E	E	↑ 3(1)		
W/GRN (N)	F	F	4(0)		
W/BLU (B)	H	H	4(1)		
W/VIO (V)	J	J	5(0)		
W/GRY (G)	K	K	5(1)		
WHT (W)	L	L	6(0)		
W/BLK (X)	M	M	6(1)		
W/BRN (Z)	N	N	7(0)		
W/RED (R)	P	P	7(1)		
W/ORN (O)	R	R	8(0)		
W/YEL (Y)	S	S	8(1)		
W/GRN (N)	T	T	↓ 9(0)		
W/BLU (B)	↓ U	↓ U	MA 9(1)		
W/VIO (V)	PCØ1V	MC36V	GND		

JACK <input type="checkbox"/>	PLUG <input checked="" type="checkbox"/>	LOCATION, LENGTH, ROUTE PDØ1 & MD36
FEMALE <input type="checkbox"/>	MALE <input checked="" type="checkbox"/>	

COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PDØ1A	MD36A	TTI 4(1)	
W/BRN (Z)	↑ B	↑ B	TTI 5(1)	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	MA 10(0)	
W/YEL (Y)	E	E	↑ 10(1)	
W/GRN (N)	F	F	↓ 11(0)	
W/BLU (B)	H	H	MA 11(1)	
W/VIO (V)	J	J	MB 0(0)	
W/GRY (G)	K	K	↑ 0(1)	
WHT (W)	L	L	1(0)	
W/BLK (X)	M	M	1(1)	
W/BRN (Z)	N	N	2(0)	
W/RED (R)	P	P	2(1)	
W/ORN (O)	R	R	3(0)	
W/YEL (Y)	S	S	3(1)	
W/GRN (N)	T	T	↓ 4(0)	
W/BLU (B)	↓ U	↓ U	MB 4(1)	
W/VIO (V)	PDØ1V	MD36V	GND	

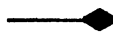
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FEMALE <input type="checkbox"/>		MALE <input checked="" type="checkbox"/>		PEØ1 & ME36	
COLOR	PIN	PIN	NAME	REMARKS	
W/BLK (X)	PEØ1A	ME36A	TTI 6(1)		
W/BRN (Z)	↑ B	↑ B	TTI 7(1)		
W/RED (R)	C	C	GND		
W/ORN (O)	D	D	MB 5(0)		
W/YEL (Y)	E	E	↑ 5(1)		
W/GRN (N)	F	F	6(0)		
W/BLU (B)	H	H	6(1)		
W/VIO (V)	J	J	7(0)		
W/GRY (G)	K	K	7(1)		
WHT (W)	L	L	8(0)		
W/BLK (X)	M	M	8(1)		
W/BRN (Z)	N	N	9(0)		
W/RED (R)	P	P	9(1)		
W/ORN (O)	R	R	10(0)		
W/YEL (Y)	S	R	10(1)		
W/GRN (N)	T	T	↓ 11(0)		
W/BLU (B)	↓ U	↓ U	MB 11(1)		
W/VIO (V)	PEØ1V	ME36V	GND		

JACK <input type="checkbox"/>		PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE	
FEMALE <input type="checkbox"/>		MALE <input checked="" type="checkbox"/>		PF01 & MF36	
COLOR	PIN	PIN	NAME	REMARKS	
W/BLK (X)	PF01A	MF36A	FETCH (F)		
W/BRN (Z)	↑ B	↑ B	B SET		
W/RED (R)	C	C	MEMORY STROBE ENB		
W/ORN (O)	E	E	MEM START		
W/YEL (Y)	F	F	T 1		
W/GRN (N)	H	H	T 2A		
W/BLU (B)	J	J	IOP 1		
W/VIO (V)	K	K	IOP 2		
W/GRY (G)	L	L	IOP 4		
WHT (W)	M	M	PWR CLR		
W/BLK (X)	N	N	E SET		
W/BRN (Z)	P	P	TTI AC		
W/RED (R)	R	R	SKIP		
W/ORN (O)	S	S	INTERRUPT		
W/YEL (Y)	T	T	<del>MEM</del> DONE		
W/GRN (N)	↓ U	↓ U	IOT 032		
W/BLU (B)	PF01V	MF36V	GND		
W/VIO (V)					

JACK <input type="checkbox"/> PLUG <input checked="" type="checkbox"/> FEMALE <input type="checkbox"/> MALE <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE PDØ2 & MD35		
COLOR	PIN	PIN	NAME	REMARKS
W/BLK (X)	PDØ2A	MD35A	JMS	
W/BRN (Z)	↑ B	↑ B	INT ACK	
W/RED (R)	C	C	GND	
W/ORN (O)	D	D	SR → PC	
W/YEL (Y)	E	E	MB → PC 0-4 ENABLE	
W/GRN (N)	F	F	0 → PC <sub>5-11</sub>	
W/BLU (B)	H	H	OPR	
W/VIO (V)	J	J	IM 6	
W/GRY (G)	K	K	↑ 9	
WHT (W)	L	L	↓ 7	
W/BLK (X)	M	M	10	
W/BRN (Z)	N	N	↓ 8	
W/RED (R)	P	P	IM 11	
W/ORN (O)	R	R	MB → PC 0-4 ENABLE	
W/YEL (Y)	S	S	MEM. EXT.	
W/GRN (N)	T	T	IOT	
W/BLU (B)	↓ U	↓ U	INT. INHIBIT	
W/VIO (V)	PDØ2V	MD35V	GND	

JACK <input type="checkbox"/>	PLUG <input checked="" type="checkbox"/>	LOCATION, LENGTH, ROUTE PB 04
FEMALE <input type="checkbox"/>	MALE <input checked="" type="checkbox"/>	

COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	PB 04	A	MQ 0 (1)	
W/BRN (Z)		B	1 (1)	
W/RED (R)		C	2 (1)	
W/ORN (O)		D	3 (1)	
W/YEL (Y)		E	4 (1)	
W/GRN (N)		F	5 (1)	
W/BLU (B)		H	6 (1)	
W/VIO (V)		J	7 (1)	
W/GRY (G)		K	8 (1)	
WHT (W)		L	9 (1)	
W/BLK (X)		M	10 (1)	
W/BRN (Z)		N	MQ 11 (1)	
W/RED (R)		P	SR 6	
W/ORN (O)		R	7	
W/YEL (Y)		S	8	
W/GRN (N)		T	9	
W/BLU (B)		U	10	
W/VIO (V)	PB 04	V	SR 11	
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

JACK <input type="checkbox"/>		PLUG <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE	
FEMALE <input type="checkbox"/>		MALE <input checked="" type="checkbox"/>			
COLOR	LOCATION	PIN	NAME	REMARKS	
W/ BLK (X)	PB 05	A	LINK		
W/ BRN (Z)	PB 05	B	RUN (1)		
W/ RED (R)	PB 05	C	PAUSE		
W/ ORN (O)	PB 05	D	ION		
W/ YEL (Y)		E			
W/ GRN (N)		F			
W/ BLU (B)		H			
W/ VIO (V)		J			
W/ GRY (G)		K			
WHT (W)		L			
W/ BLK (X)		M			
W/ BRN (Z)		N			
W/ RED (R)	PB 05	P	SINGLE STEP		
W/ ORN (O)	PB 05	R	SINGLE INST.		
W/ YEL (Y)		S			
W/ GRN (N)		T			
W/ BLU (B)		U			
W/ VIO (V)		V			
W/ GRY (G)		W			
WHT (W)		X			
		Y			
		Z			

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PE 02		
W/BRN	IM 0	D	↑		
W/RED	GND	<del>X</del>			
W/ORN	IM 1	E			
W/YEL	GND	F			
W/GRN	IM 2	H			
W/BLU	GND	J			
W/VIO	IM 3	K			
W/GRY	GND	L			
WHT	IM 4	M			
W/BLK	GND	N			
W/BRN	IM 5	P			
W/RED	GND	R			
W/ORN	IM 6	S			
W/YEL	GND	<del>X</del>			
W/GRN	IM 7	T			
W/BLU	GND	U			
W/VIO	IM 8	V	↓		
W/GRY	GND	<del>X</del>	PE 02		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/ BLK	G N D	C	PF 02		
W/ BRN	IM 9	D	↑ ↓		
W/ RED	G N D	<del>X</del>			
W/ ORN	IM 10	E			
W/ YEL	G N D	F			
W/ GRN	IM 11	H			
W/ BLU	G N D	J			
W/ VIO	SKIP	K			
W/ GRY	G N D	L			
WHT	INTERRUPT	M			
W/ BLK	G N D	N			
W/ BRN	AC CLEAR	P			
W/ RED	G N D	R			
W/ ORN	RUN (1)	S			
W/ YEL	G N D	<del>X</del>			
W/ GRN		T			
W/ BLU	G N D	U			
W/ VIO		V			
W/ GRY	G N D	<del>X</del>		PF 02	

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	ME34		
W/BRN	BAC 0 (1)	D	↑		
W/RED	GND	✕			
W/ORN	BAC 1 (1)	E			
W/YEL	GND	F			
W/GRN	BAC 2 (1)	H			
W/BLU	GND	J			
W/VIO	BAC 3 (1)	K			
W/GRY	GND	L			
WHT	BAC 4 (1)	M			
W/BLK	GND	N			
W/BRN	BAC 5 (1)	P			
W/RED	GND	R			
W/ORN	BAC 6 (1)	S			
W/YEL	GND	✕			
W/GRN	BAC 7 (1)	T			
W/BLU	GND	U			
W/VIO	BAC 8 (1)	V	↓		
W/GRY	GND	✕	ME34		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/ BLK	G N D	C	MF34		
W/ BRN	BAC 9 (1)	D	↑		
W/ RED	G N D	×			
W/ ORN	BAC 10 (1)	E			
W/ YEL	G N D	F			
W/ GRN	BAC 11 (1)	H			
W/ BLU	G N D	J			
W/ VIO	IOP 1	K			
W/ GRY	G N D	L			
WHT	IOP 2	M			
W/ BLK	G N D	N			
W/ BRN	IOP 4	P			
W/ RED	G N D	R			
W/ ORN	T 1	S			
W/ YEL	G N D	×			
W/ GRN	T 2	T			
W/ BLU	G N D	U			
W/ VIO	PWR CLR	V	↓		
W/ GRY	G N D	×	MF 34		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PE 03		
W/BRN	DATA ADD 0	D	▲		
W/RED	GND	✕			
W/ORN	DATA ADD 1	E			
W/YEL	GND	F			
W/GRN	DATA ADD 2	H			
W/BLU	GND	J			
W/VIO	DATA ADD 3	K			
W/GRY	GND	L			
WHT	DATA ADD 4	M			
W/BLK	GND	N			
W/BRN	DATA ADD 5	P			
W/RED	GND	R			
W/ORN	DATA ADD 6	S			
W/YEL	GND	✕			
W/GRN	DATA ADD 7	T			
W/BLU	GND	U			
W/VIO	DATA ADD 8	V	▼		
W/GRY	GND	✕	PE 03		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PF 03		
W/BRN	DATA ADD 9	D	▲		
W/RED	GND	×			
W/ORN	DATA ADD 10	E			
W/YEL	GND	F			
W/GRN	DATA ADD 11	H			
W/BLU	GND	J			
W/VIO	BRK. REQUEST	K			
W/GRY	GND	L			
WHT	DATA DIRCT.	M			
W/BLK	GND	N			
W/BRN	BREAK (B)	P			
W/RED	GND	R			
W/ORN	ADD ACCEPTED	S			
W/YEL	GND	×			
W/GRN	MB INCREMENT	T			
W/BLU	GND	U			
W/VIO		V	▼		
W/GRY	GND	×	PF 03		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PE 04		
W/BRN	MB 0 IN	D	▲		
W/RED	GND	✕			
W/ORN	MB 1 IN	E			
W/YEL	GND	F			
W/GRN	MB 2 IN	H			
W/BLU	GND	J			
W/VIO	MB 3 IN	K			
W/GRY	GND	L			
WHT	MB 4 IN	M			
W/BLK	GND	N			
W/BRN	MB 5 IN	P			
W/RED	GND	R			
W/ORN	MB 6 IN	S			
W/YEL	GND	✕			
W/GRN	MB 7 IN	T			
W/BLU	GND	U			
W/VIO	MB 8 IN	V	▼		
W/GRY	GND	✕	PE 04		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	PF 04		
W/BRN	MB 9 IN	D	↑		
W/RED	GND	×	↓		
W/ORN	MB 10 IN	E			
W/YEL	GND	F			
W/GRN	MB 11 IN	H	PF 04		
W/BLU	GND	J			
W/VIO	CYCLE SELECT	K	PF 04		
W/GRY	GND	L			
WHT	+I → CA INH.	M	PF 04		
W/BLK	GND	N			
W/BRN	WC OVERFLOW	P	PF 04		
W/RED	GND	R			
W/ORN		S			
W/YEL	GND	×			
W/GRN		T			
W/BLU	GND	U			
W/VIO		V			
W/GRY	GND	×			

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/ BLK	G N D	C	ME 35		
W/ BRN	BMB 0 (1)	D	↑		
W/ RED	G N D	✕			
W/ ORN	BMB 1 (1)	E			
W/ YEL	G N D	F			
W/ GRN	BMB 2 (1)	H			
W/ BLU	G N D	J			
W/ VIO	BMB 3 (0)	K			
W/ GRY	G N D	L			
WHT	BMB 3 (1)	M			
W/ BLK	G N D	N			
W/ BRN	BMB 4 (0)	P			
W/ RED	G N D	R			
W/ ORN	BMB 4 (1)	S			
W/ YEL	G N D	✕			
W/ GRN	BMB 5 (0)	T			
W/ BLU	G N D	U			
W/ VIO	BMB 5 (1)	V	↓		
W/ GRY	G N D	✕	ME 35		

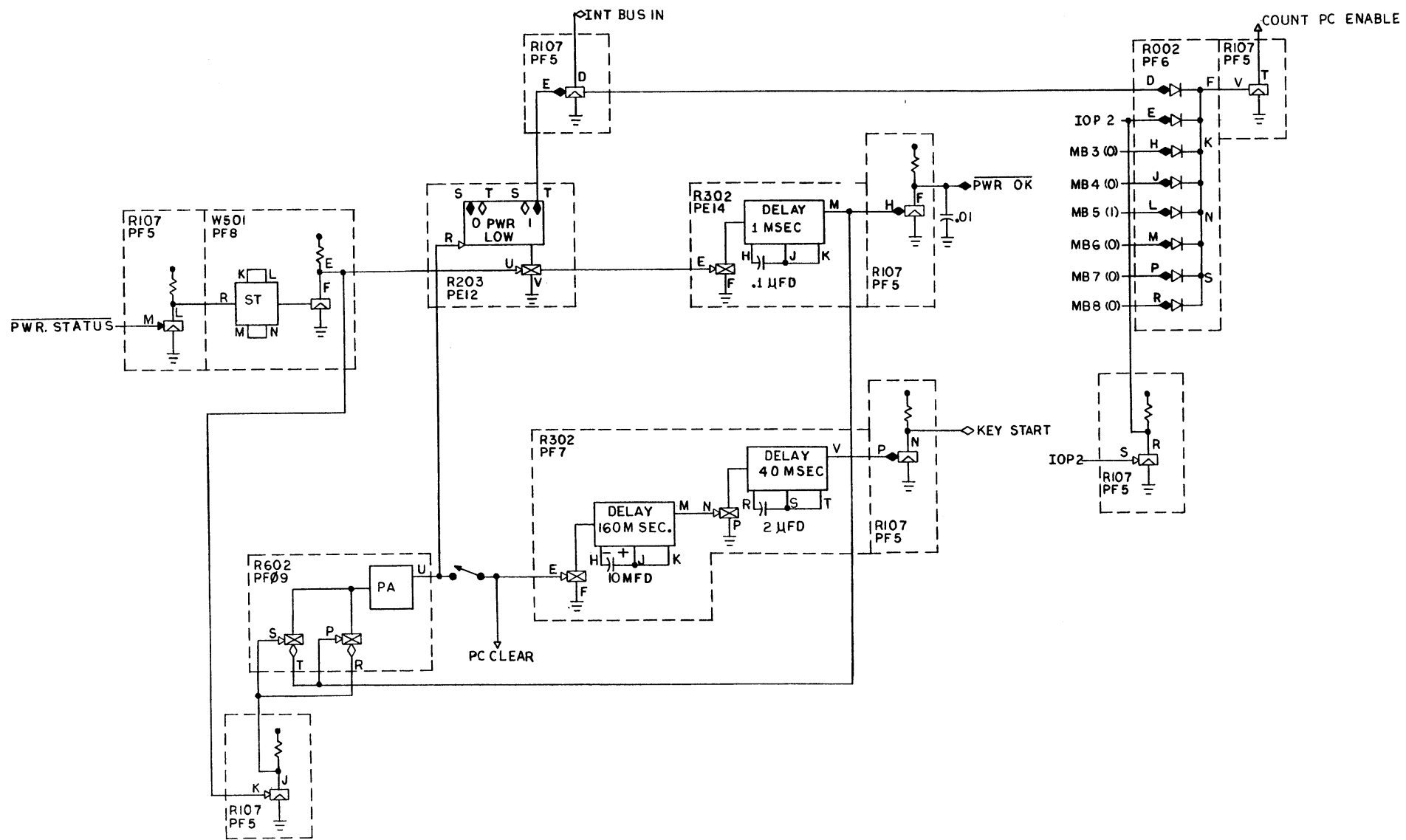
COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	MF35		
W/BRN	BMB 6 (0)	D	↑		
W/RED	GND	⊗			
W/ORN	BMB 6 (1)	E			
W/YEL	GND	F			
W/GRN	BMB 7 (0)	H			
W/BLU	GND	J			
W/VIO	BMB 7 (1)	K			
W/GRY	GND	L			
WHT	BMB 8 (0)	M			
W/BLK	GND	N			
W/BRN	BMB 8 (1)	P			
W/RED	GND	R			
W/ORN	BMB 9 (1)	S			
W/YEL	GND	⊗			
W/GRN	BMB 10 (1)	T			
W/BLU	GND	U			
W/VIO	BMB 11 (1)	V	↓		
W/GRY	GND	⊗	MF35		

JACK <input type="checkbox"/> PLUG <input checked="" type="checkbox"/> FEMALE <input type="checkbox"/> MALE <input checked="" type="checkbox"/>		LOCATION, LENGTH, ROUTE MA 35		
COLOR	LOCATION	PIN	NAME	REMARKS
W/BLK (X)	MA 35	A	DATA FIELD 0	
W/BRN (Z)	↑	B	DATA FIELD 1	
W/RED (R)		C	DATA FIELD 2	
W/ORN (O)		D	INST FIELD 0	
W/YEL (Y)		E	INST FIELD 1	
W/GRN (N)		F	INST FIELD 2	
W/BLU (B)		H		
W/VIO (V)		J		
W/GRY (G)		K		
WHT (W)		L		
W/BLK (X)		M		
W/BRN (Z)		N		
W/RED (R)		P	DATA FIELD SR 0	
W/ORN (O)		R	DATA FIELD SR 1	
W/YEL (Y)		S	DATA FIELD SR 2	
W/GRN (N)		T	INST FIELD SR 0	
W/BLU (B)	↓	U	INST FIELD SR 1	
W/VIO (V)	MA 35	V	INST FIELD SR 2	
W/GRY (G)		W		
WHT (W)		X		
		Y		
		Z		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS	
		A			BLANK	
		B			BLANK	
W/BLK	GND	C	ME 31			
W/BRN	SA P	D	↑ ↓			
W/RED	GND	<del>X</del>				
W/ORN	SA 0	E				
W/YEL	GND	F				
W/GRN	SA 1	H				
W/BLU	GND	J				
W/VIO	SA 2	K				
W/GRY	GND	L				
WHT	SA 3	M				
W/BLK	GND	N				
W/BRN	SA 4	P				
W/RED	GND	R				
W/ORN	SA 5	S				
W/YEL	GND	<del>X</del>				
W/GRN	SA 6	T				
W/BLU	GND	U				
W/VIO	SA 7	V				
W/GRY	GND	<del>X</del>		ME 31		

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
		A			BLANK
		B			BLANK
W/BLK	GND	C	MF 31		
W/BRN	SA 8	D			
W/RED	GND	<del>X</del>			
W/ORN	SA 9	E			
W/YEL	GND	F			
W/GRN	SA 10	H			
W/BLU	GND	J			
W/VIO	SA 11	K			
W/GRY	GND	L			
WHT	PWR CLR	M			
W/BLK	GND	N			
W/BRN		P			
W/RED	GND	R			
W/ORN		S			
W/YEL	GND	<del>X</del>			
W/GRN		T			
W/BLU	GND	U			
W/VIO		V			
W/GRY	GND	<del>X</del>		MF 31	

COLOR	NAME	PIN	LOCATION	LOCATION	REMARKS
	+10V	A	MF30		BLANK
	-15V	B	↑		BLANK
W/BLK	GND	C			
W/BRN	KEY BOARD GENERATOR	D			
W/RED	GND	×			
W/ORN		E			
W/YEL	GND	F			
W/GRN	SELECTOR MAGNETS	H			
W/BLU	GND	J			
W/VIO		K			
W/GRY	GND	L			
WHT	POWER SWITCHES	M			
W/BLK	GND	N			
W/BRN		P			
W/RED	GND	R			
W/ORN		S			
W/YEL	GND	×			
W/GRN		T			
W/BLU	GND	U			
W/VIO		V	↓		
W/GRY	GND	×	MF30		

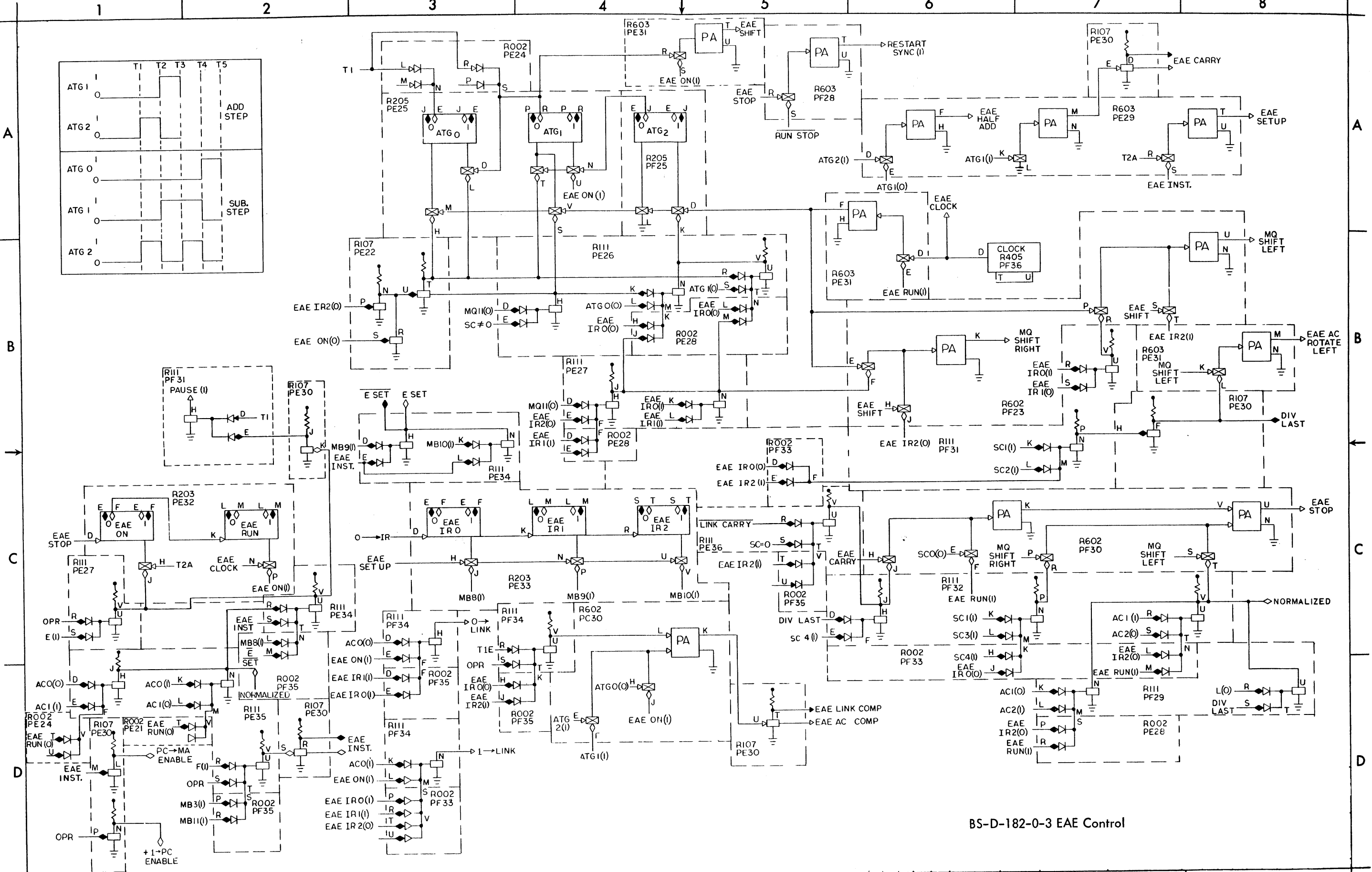


BS-D-KR01-0-2 Power Interrupt



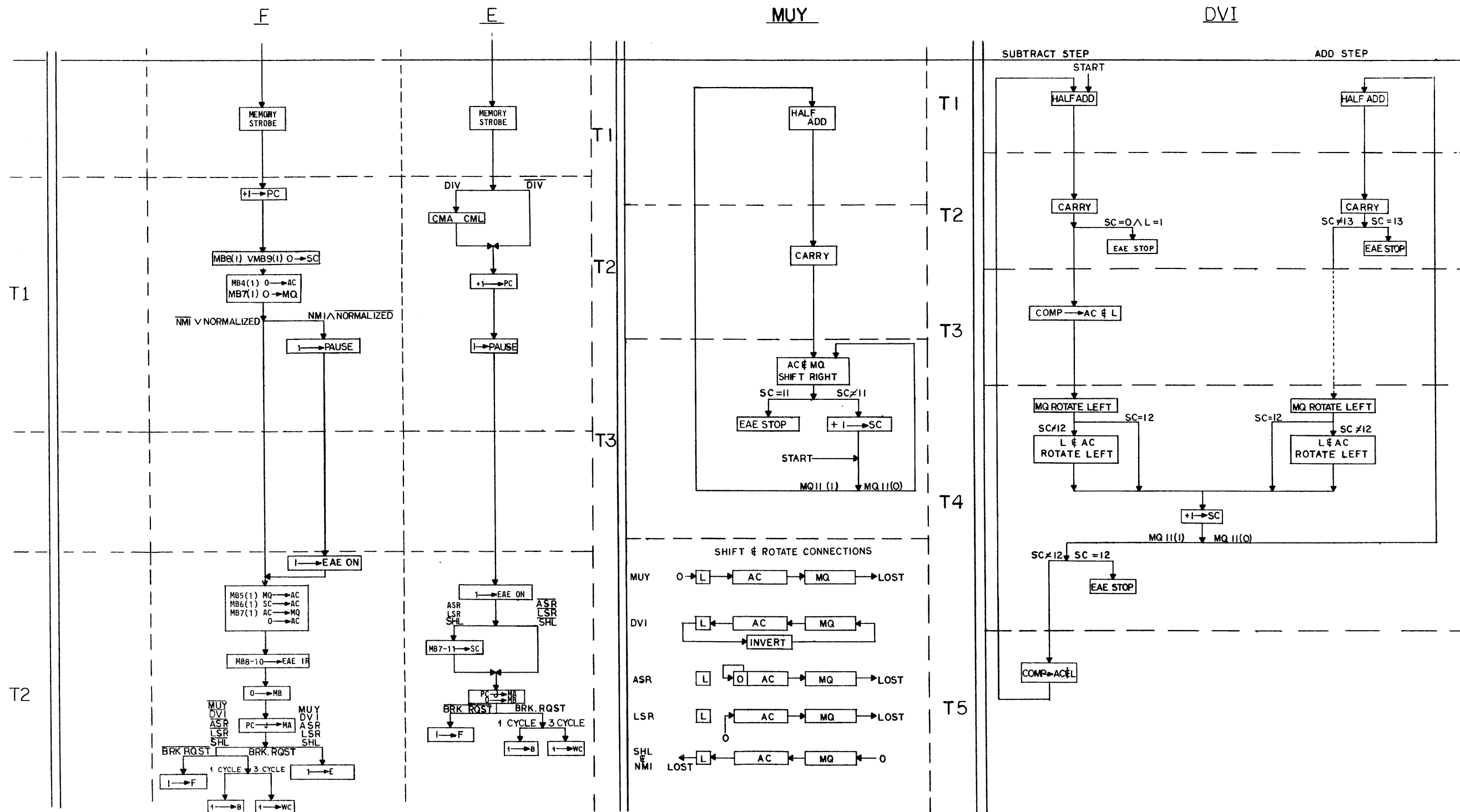




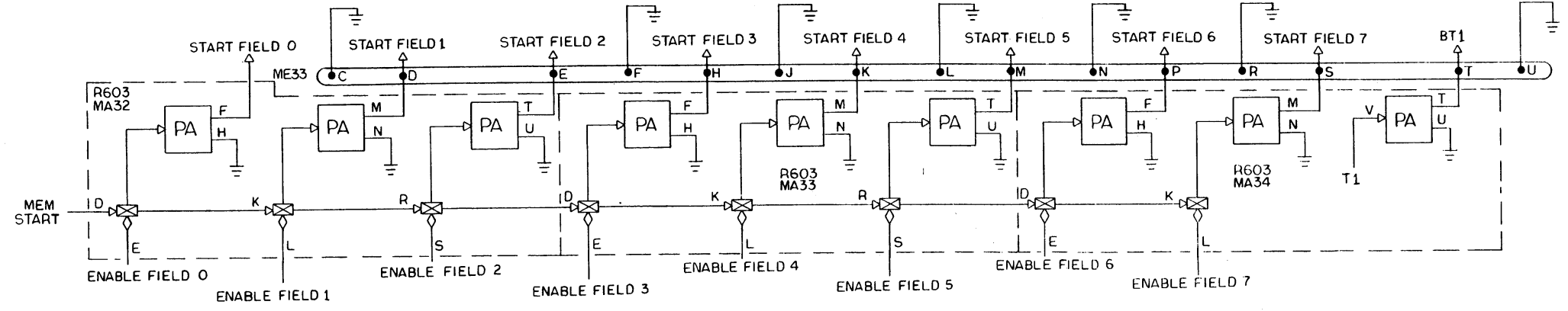
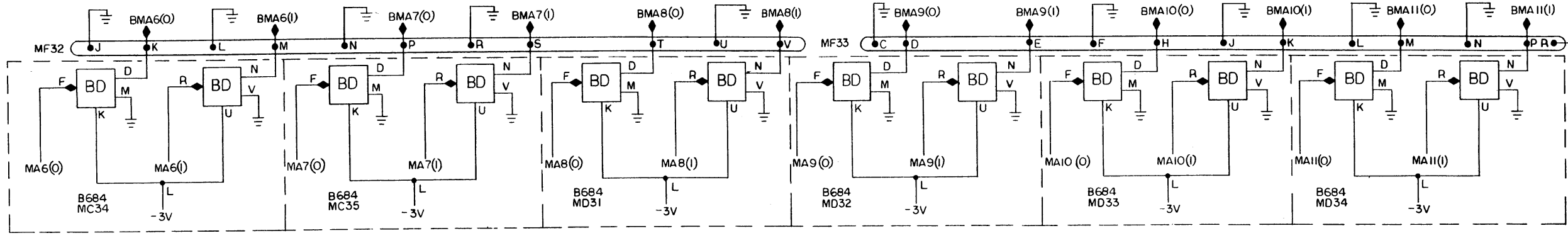
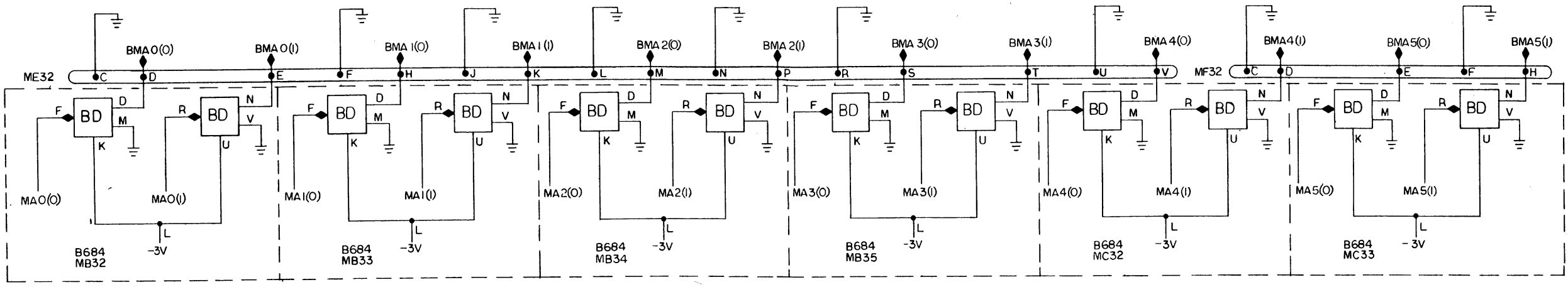


BS-D-182-0-3 EAE Control



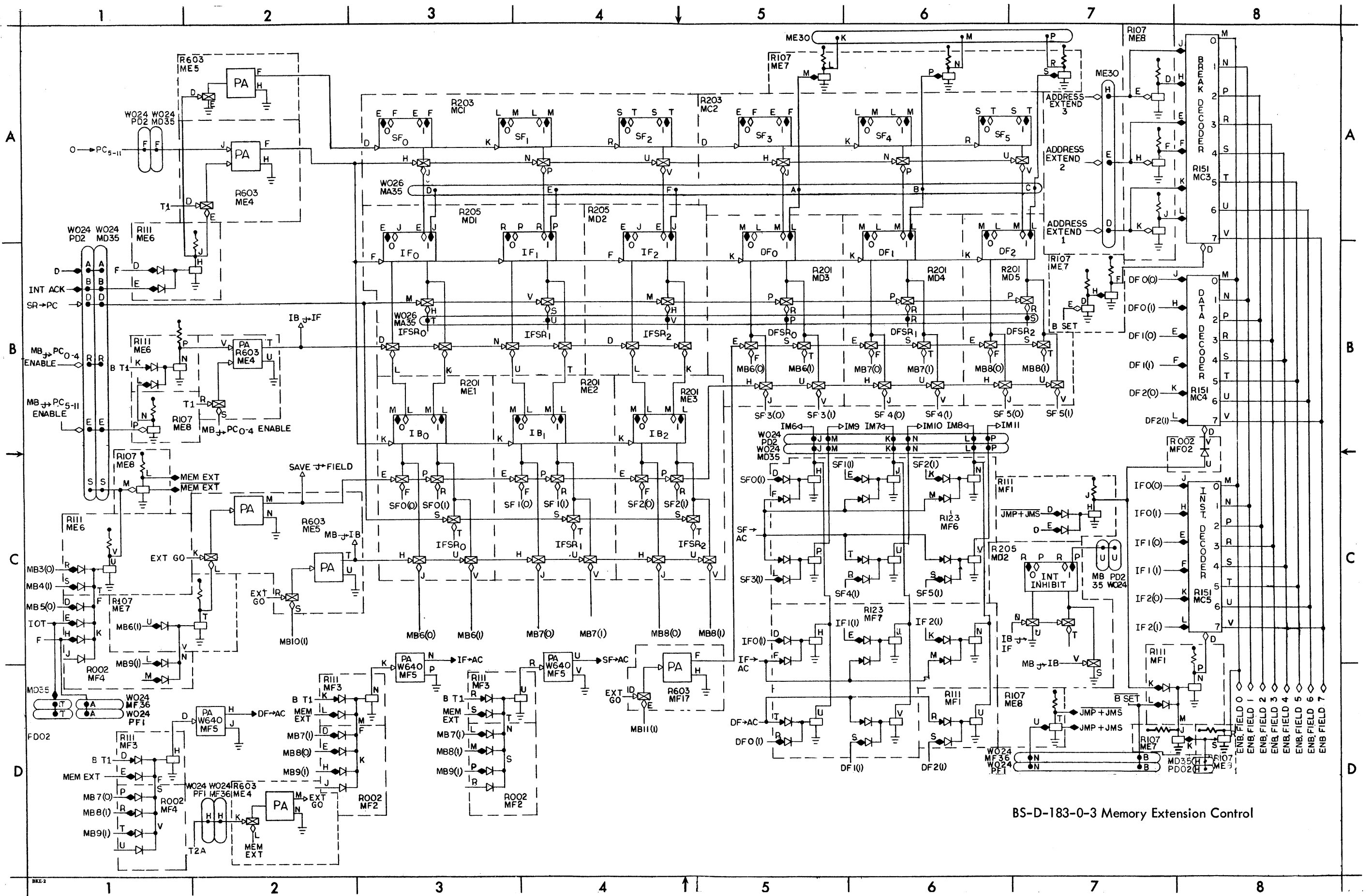






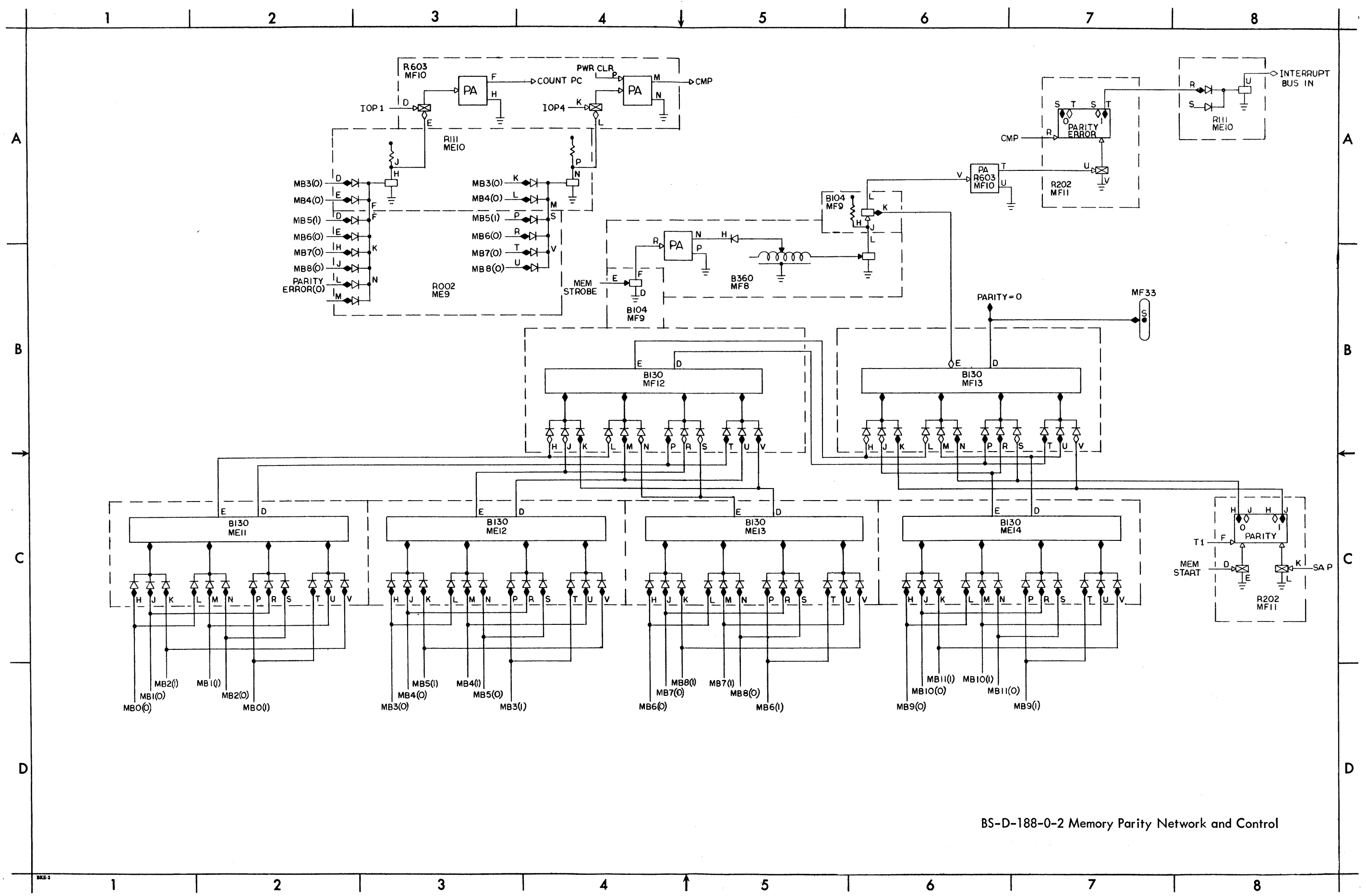
BS-D-183-0-2 MA Buffers and Start Field





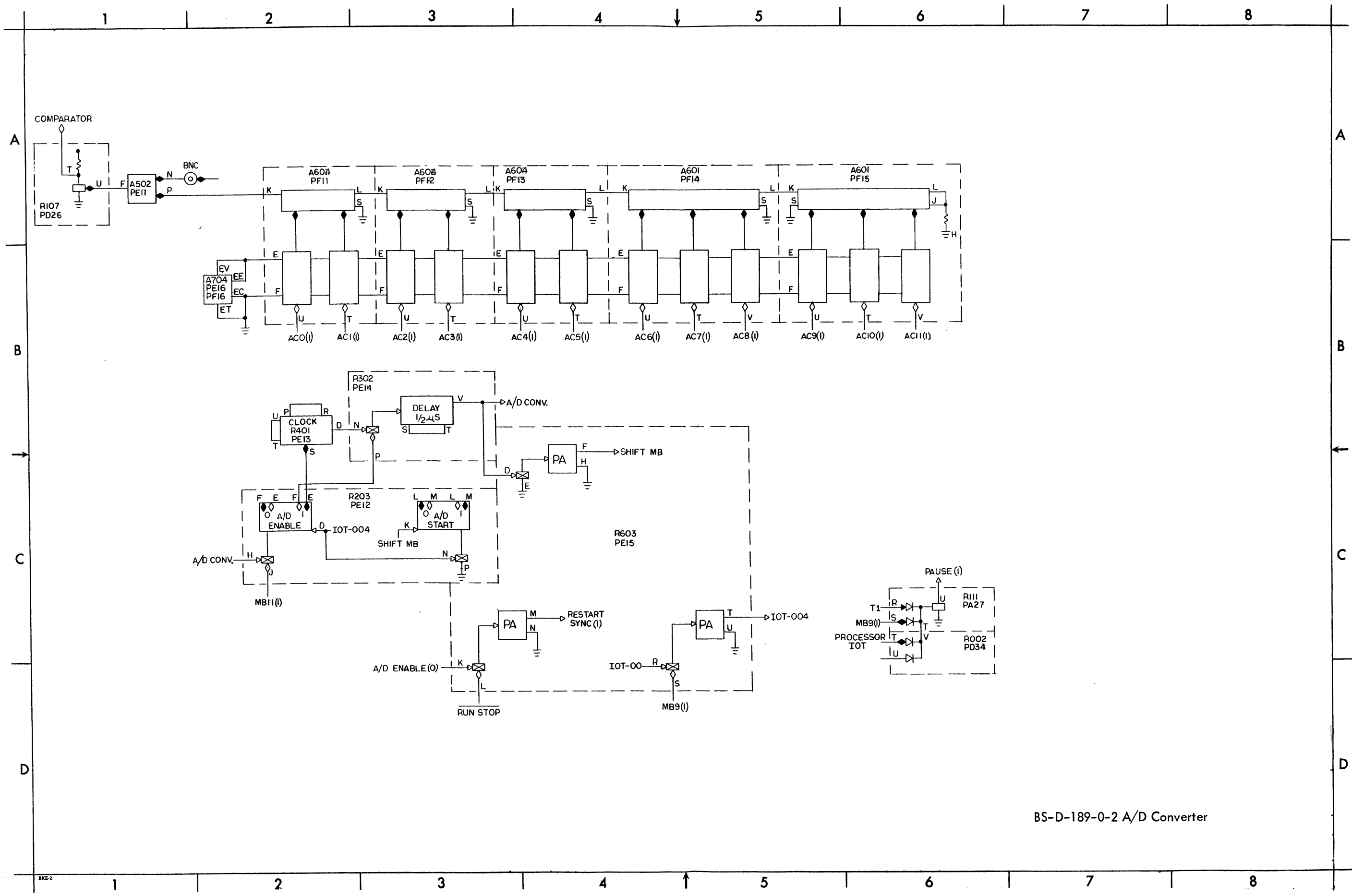
BS-D-183-0-3 Memory Extension Control





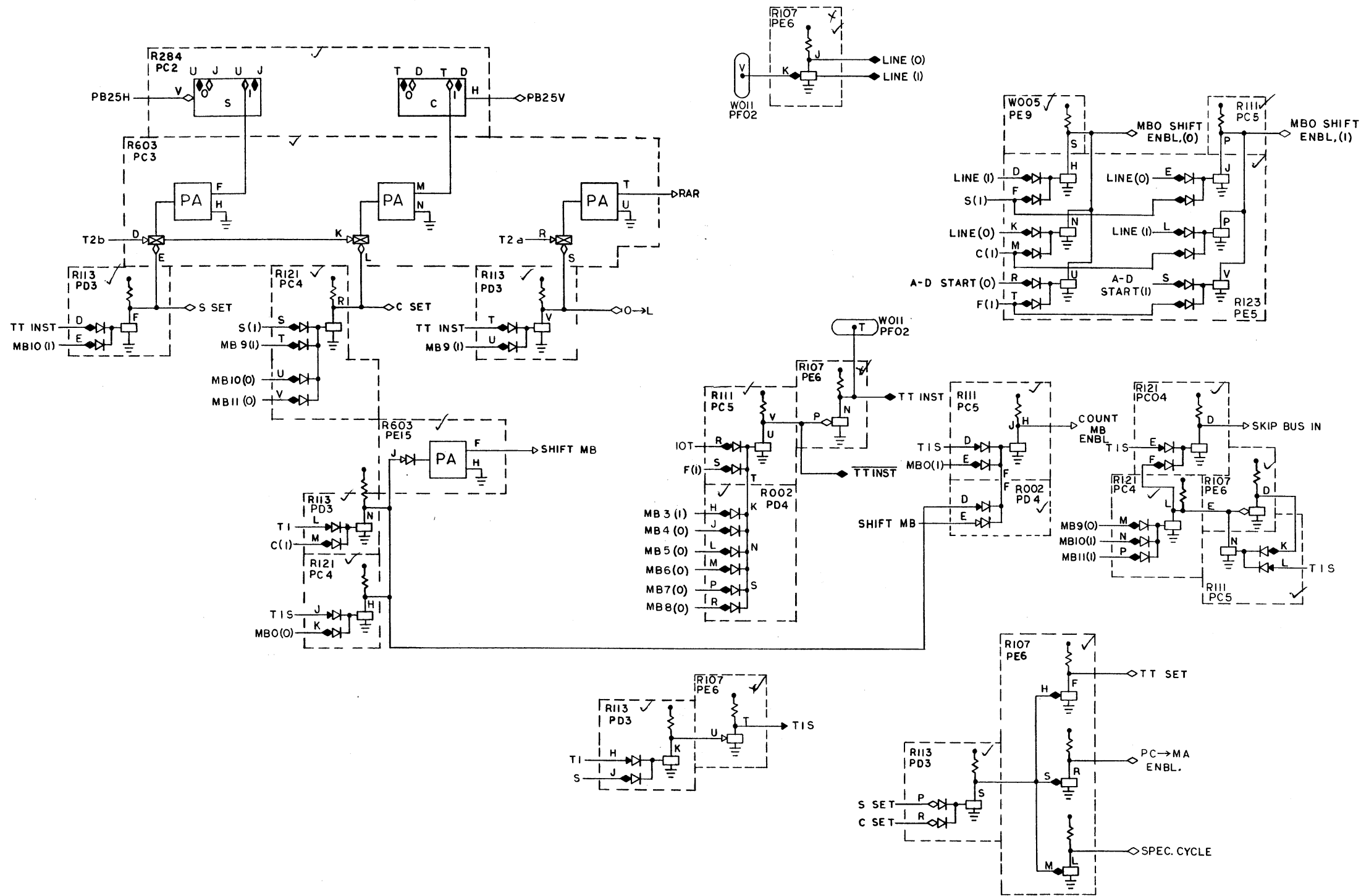
BS-D-188-0-2 Memory Parity Network and Control





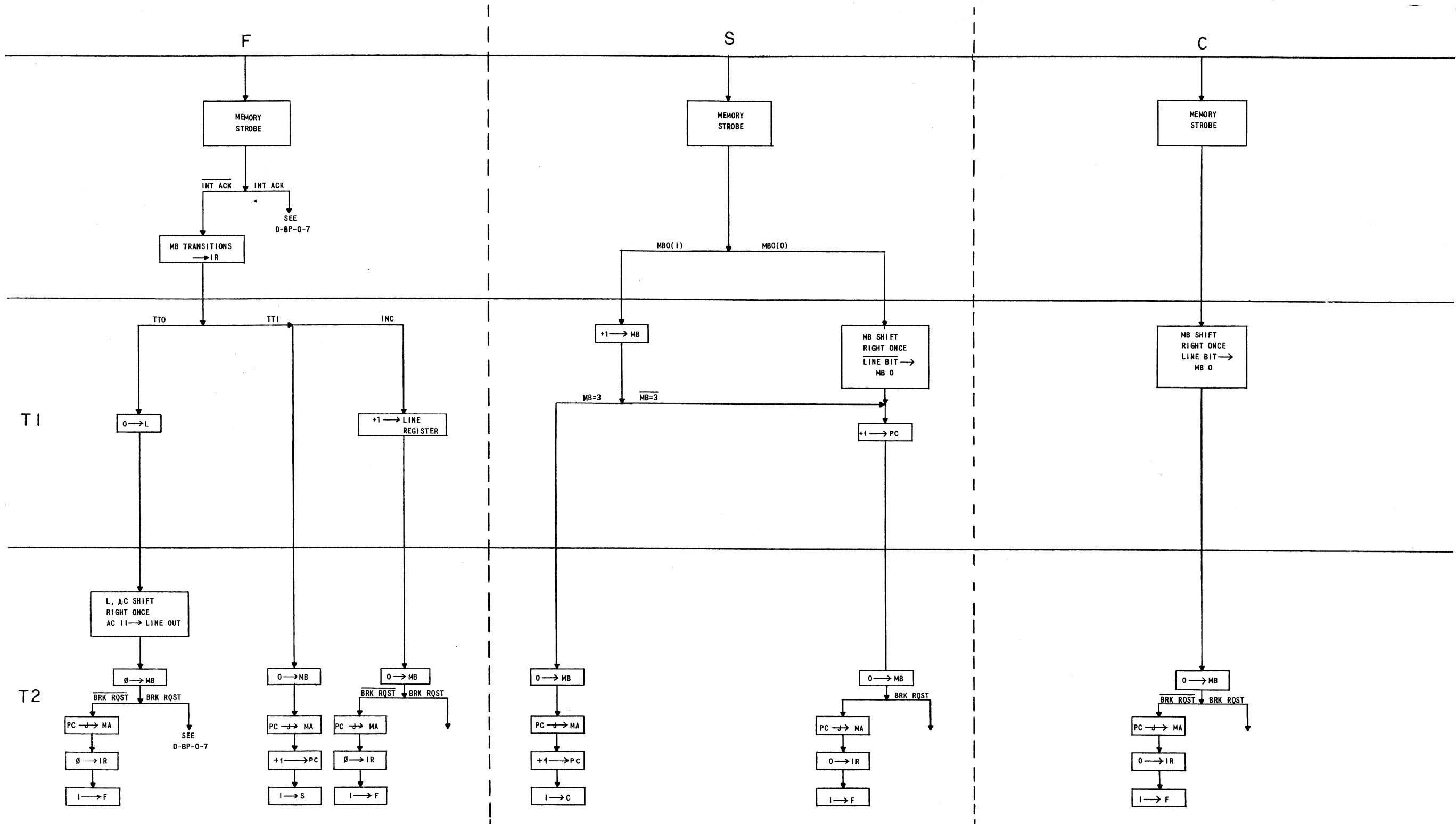
BS-D-189-0-2 A/D Converter





BS-D-681-0-2 Data Line Interface





FD-D-681-0-3 Data Line Interface Flow Diagram



# APPENDIX 1

## SIGNAL ORIGINS

A list of the signals in the PDP-8 and the engineering drawings on which they can be found appear in Table A1-1. This information should simplify and accelerate any detailed study of the machine logic on the engineering drawings.

TABLE A1-1 SIGNAL ORIGINS

Signal Name	Engineering Drawing	Signal Name	Engineering Drawing
AC → MB	D-8P-0-5	COMP → LINK	D-8P-0-3
ACSL0, ASCL1	D-8P-0-2	COUNT MB	D-8P-0-5
AC0(0) through AC11(1)	D-8P-0-2	COUNT MB ENABLE	D-681-0-2
A/D CONV.	D-189-0-2	COUNT PC	D-8P-0-8 D-8P-0-10 D-8M-0-11
ADDRESS ACCEPTED	D-8P-0-10	COUNT PC ENABLE	D-KR01-0-2
A/D START(0), A/D START(1)	D-189-0-2	D	D-8P-0-6
AND, $\overline{\text{AND}}$	D-8P-0-6	DATA → MB	D-8P-0-5
B	D-8P-0-6	DATA ADD → MA	D-8P-0-8
BAC0(1) through BAC11(1)	D-8M-0-16	DCA, $\overline{\text{DCA}}$	D-8P-0-6
B(B)	D-8P-0-10	$\overline{\text{D SET}}$	D-8P-0-6
BMB0(1) through BMB11(1)	D-8M-0-16	E(1)	D-8P-0-6
B POWER CLEAR	D-8M-0-16	EAE AC ROTATE LEFT	D-182-0-3
B RUN(1)	D-8P-0-10	EAE AC COMP	D-182-0-3
B SET, $\overline{\text{B SET}}$	D-8P-0-6	EAE LINK COMP	D-182-0-3
BT1	D-8M-0-16	ENB(0), ENB(1)	D-8M-0-11
BT2A	D-8M-0-16	$\overline{\text{E SET}}$	D-8P-0-6
CA	D-8P-0-6	F	D-8P-0-6
CARRY	D-8P-0-3	F SET, $\overline{\text{F SET}}$	D-8P-0-6
CLOCK	D-8P-0-9	HALF ADD	D-8P-0-3
COMPARATOR	D-189-0-2	INHIBIT(1)	D-8M-0-15
COMP → AC	D-8P-0-3	INT. ACK., $\overline{\text{INT. ACK.}}$	D-8P-0-10
		INT. DELAY (1)	D-8P-0-19

TABLE A1-1 SIGNAL ORIGINS (continued)

Signal Name	Engineering Drawing	Signal Name	Engineering Drawing
INT. ENABLE(1)	D-8P-0-10	MB0(0) through MB11(1)	D-8P-0-5
INTERRUPT BUS IN	D-8M-0-11	MB0 SHIFT ENBL	D-681-0-2
INTERRUPT INHIBIT	D-183-0-3	MB <sub>5-11</sub> $\rightarrow$ PC	D-8P-0-8
IOP1, IOP2, IOP4	D-8P-0-10 D-8M-0-16	MB SHIFT	D-189-0-2, D-681-0-2
IO RESTART	D-8P-0-10	MEM DONE	D-8M-0-15
IOT, $\overline{\text{IOT}}$	D-8P-0-6	MEM ENABLE(1)	D-8M-0-15
$\overline{\text{IOT}} + \overline{\text{OPR}}$	D-8P-0-6	MEM START	D-8P-0-9
IOT 00	D-8P-0-10	MEM STROBE	D-8M-0-15
IOT 004	D-189-0-2	MEM STROBE ENABLE	D-8P-0-9
IR0(0) through IR2(1)	D-8P-0-6	MQ SHIFT RIGHT	D-182-0-3
IS2, $\overline{\text{IS2}}$	D-8P-0-6	OPR, $\overline{\text{OPR}}$	D-8P-0-6
JMP, $\overline{\text{JMP}}$	D-8P-0-6	OP SKIP, $\overline{\text{OP SKIP}}$	D-8P-0-8
JMP + JMS	D-8P-0-8	OP1, OP2	D-8P-0-3
JMS, $\overline{\text{JMS}}$	D-8P-0-6	PARITY = 0	D-188-0-2
KCC IOT 032	D-8M-0-11	PAUSE(0), PAUSE(1)	D-8P-0-10 D-189-0-2
KEYBOARD FLAG(1)	D-8M-0-11	PB25H, PB25V	D-8P-0-6
KEYBOARD SELECT	D-8M-0-11	PC2H, PC2V	D-681-0-2
KEY EX + DP	D-8P-0-9	PC CARRY	D-8P-0-8
$\overline{\text{KEY LOAD ADDRESS}}$	D-8P-0-9	PC CLEAR	D-KR01-0-2
KEY START	D-8P-0-9	PC $\rightarrow$ MA	D-8P-0-8
KEY ST + EX + DP	D-8P-0-9	PC $\rightarrow$ MA ENABLE	D-681-0-2
KRS IOT 034	D-8M-0-11	PC $\rightarrow$ MB	D-8P-0-5
L(0), L(1)	D-8P-0-2	PC(0) through PC11(1)	D-8P-0-4
LSR0, LSR1	D-8P-0-2	POP1	D-8P-0-3
MA0(0) through MA11(1)	D-8P-0-4	PROCESSOR IOT, $\overline{\text{PROCESSOR IOT}}$	D-8P-0-10
MB $\xrightarrow{0}$ AC	D-8P-0-3	PWR CLR	D-8P-0-9
MB $\rightarrow$ MA <sub>0-4</sub>	D-8P-0-8	$\overline{\text{PWR OK}}$	D-8P-0-9
MB $\rightarrow$ MA <sub>5-11</sub>	D-8P-0-8	RAL	D-8P-0-3
MB $\rightarrow$ PC <sub>0-4</sub>	D-8P-0-8	RAR	D-8P-0-3
MB $\rightarrow$ PC <sub>0-4</sub> ENABLE	D-8P-0-8	READ(1)	D-8M-0-15
MB $\rightarrow$ PC <sub>5-11</sub> ENABLE	D-8P-0-8		

TABLE A1-1 SIGNAL ORIGINS (continued)

Signal Name	Engineering Drawing	Signal Name	Engineering Drawing
RESTART SYNC(1)	D-189-0-2	$\overline{TT\ INST}$	D-681-0-2
RTR	D-8P-0-3	TTI0(0) through TTI7(1)	D-8M-0-11
RUN STOP, $\overline{RUN\ STOP}$	D-8P-0-9	TT0 CLOCK	D-8M-0-11
RUN(0), RUN(1)	D-8P-0-9	TT0(0) through TT07(1)	D-8M-0-11
SA P	D-8M-0-15	TT0=0	D-8M-0-11
SA0 through SA11	D-8M-0-15	T1, T1E	D-8P-0-9
SHIFT MB	D-189-0-2	T2A, T2B, T2E	D-8P-0-9
SP STOP	D-8P-0-9	WC(1)	D-8P-0-6
SP0, SP1, SP2, SP3	D-8P-0-9	WC + WC SET	D-8P-0-6
SR $\longrightarrow$ AC	D-8P-0-3	WRITE(1)	D-8M-0-15
SR $\longrightarrow$ PC	D-8P-0-8	0 $\longrightarrow$ AC	D-8P-0-3
STOP(0), STOP(1)	D-8M-0-11	0 $\longrightarrow$ L	D-8P-0-3
TAD, $\overline{TAD}$	D-8P-0-6	0 $\longrightarrow$ MA <sub>0-4</sub>	D-8P-0-8
TCF IOT 042	D-8M-0-11	0 $\longrightarrow$ MA <sub>5-11</sub>	D-8P-0-8
TELEPRINTER FLAG(1)	D-8M-0-11	0 $\longrightarrow$ MB	D-8P-0-5
TELEPRINTER SELECT	D-8M-0-11	0 $\longrightarrow$ PC <sub>0-4</sub>	D-8P-0-8
TPC IOT 044	D-8M-0-11	0 $\longrightarrow$ PC <sub>5-11</sub>	D-8P-0-8
TTI $\longrightarrow$ AC	D-8M-0-11	1 $\longrightarrow$ L	D-8P-0-3, D-182-0-3
TTI CLOCK	D-8M-0-11	+1 $\longrightarrow$ PC ENABLE	D-8P-0-8



## APPENDIX 2

### DIGITAL PROGRAM LIBRARY

The following is a current list of program tapes and descriptive material for programs applicable to the PDP-8. DEC constantly develops, field tests, and documents into the Digital Program Library new techniques, routines, and programs for incorporation into users' systems.

#### SYSTEM PROGRAMS

Digital	8-1-S	Symbolic Editor
Digital	8-1-SL	Symbolic Editor Listing
Digital	8-2-S	FORTRAN System
Digital	8-2-SL	FORTRAN Operating System Listing
Digital	8-3-S	PAL III (Program Assembler Language)
Digital	8-3-SL	PAL III Listing
Digital	8-4-S	DDT-8
Digital	8-5-S	Floating-Point System
Digital	8-6-S	Symbol Print
Digital	8-7-S	DECtape Library System
Digital	8-8-S	MACRO 8
Digital	8-9-S	DECtape FORTRAN
Digital	8-10-S	CALCULATOR System
Digital	8-11-S	DĀTAK System (Data Acquisition Program)
Digital	8-12-S	ODT-8
Digital	8-13/14-S	Multianalyzer Programs
Digital	8-15-S	Oceanographic Analysis
Digital	8-16-S	Master Tape Duplicator
Digital	8-35-S-A	TTY 680 5-Bit Character Assembly Subroutines
Digital	8-35-S-B	TTY 680 8-Bit Character Assembly Subroutines

#### ELEMENTARY FUNCTION ROUTINES

Digital	8-9-F	Square Root Subroutine - Single Precision
Digital	8-11-F	Signed Multiply Subroutine - Single Precision
Digital	8-12-F	Signed Divide Subroutine - Single Precision
Digital	8-13-F	Double-Precision Multiply Subroutine - Signed
Digital	8-14-F	Double-Precision Divide Subroutine - Signed
Digital	8-15-F	Sine Routine - Single Precision
Digital	8-16-F	Sine Routine - Double Precision
Digital	8-17-F	Cosine Routine - Single Precision
Digital	8-18-F	Sine Routine - Double Precision
Digital	8-20-F	Four Word Floating Point Package
Digital	8-21-F	Signed Multiply Single Precision Using EAE Type 182
Digital	8-22-F	Signed Divide Single Precision Using EAE Type 182
Digital	8-23-F	Signed Multiply Double Precision Using EAE Type 182
Digital	8-25-F	Floating Point Package EAE

## UTILITY PROGRAMS

Digital	8-0	Format for PDP-8 Program Documentation
Digital	8-1-U	Read-In-Mode Loader
Digital	8-2-U-Rim	Binary Loader (ASR-33 or 750C)
Digital	8-2A-U-Rim	Binary Loader (Extended Memory, ASR-33)
Digital	8-2B-U-Rim	Binary Loader (Extended Memory, 750C)
Digital	8-3-U	DECTape Library System Loader
Digital	8-4-U-Rim	Read-In-Mode Punch ASR-33
Digital	8-5-U-Sym	Binary Punch 33/75E
Digital	8-6-U-Sym	Octal Memory Dump
Digital	8-7-U-Sym	Logical Subroutines
Digital	8-8-U-Sym	Arithmetic Shift Subroutines
Digital	8-9-U-Sym	Logical Shift Subroutines
Digital	8-12-U	Incremental Plotter Subroutines
Digital	8-14-U-Sym	Binary to Binary-Coded-Decimal Conversion
Digital	8-15-U	Binary to Binary-Coded-Decimal Conversion (Four Digit)
Digital	8-16-U-Sym	Binary to Binary-Coded-Decimal Conversion (Compatible with IBM BCD Mode Mag-Tape Format)
Digital	8-17-U	EAE Instruction Set Simulator
Digital	8-18-U-Sym	Subroutine for Alphanumeric Message Typeout
Digital	8-19-U-Sym	Teletype Output Subroutines
Digital	8-20-U	Character String Typeout
Digital	8-21-U-Sym	Symbolic Tape Format Generator
Digital	8-22-U	Unsigned Decimal Print
Digital	8-26-U-Bin	DECTOG
Digital	8-27-U-Bin	DECTape Subroutines
Digital	8-28-U	580 Tape Control Subroutines
Digital	8-32-U	Binary Punch (6 Channel)
Digital	8-33-U	5/8 TOG
Digital	8-34-U	DECEX DECTape Exerciser

## APPLICATION PROGRAMS

Application Note 801	Scaling for Fixed-Point, 2's Complement Arithmetic
Application Note 802	Matrix Inversion
Application Note 803	Performance Capability Program (Edit Subprogram)
Application Note 804	Throughput to IBM-Compatible Magnetic Tape
Application Note 805	Linearization Subprogram

## MAINTENANCE PROGRAMS

A complete collection of maintenance and diagnostic programs is available for the basic computer and many of its options. Table 9-1 lists these Maindec programs for the basic PDP-8.

## DECUS LIBRARY

DECUS No. 5-1	Binary Package
DECUS No. 5-2	Octal Package and Symbolic Dump
DECUS No. 5-3	BRL - A Binary Relocatable Loader with Transfer Vector Options for the PDP-5 Computer
DECUS No. 5-4	Octal Typeout of Memory Area with Format Option
DECUS No. 5-5	Expanded Adding Machine
DECUS No. 5-6	BCD-to-Binary Conversion of 3-Digit Numbers
DECUS No. 5/8-7	Decimal-to-Binary Conversion by Radix Deflation on PDP-8
DECUS No. 5-8	PDP-5 Floating Point Routines
DECUS No. 5/8-9	Analysis of Variance PDP-5/8
DECUS No. 5-10	Paper Tape Reader Tester
DECUS No. 5-11	PDP-5 Debug System
DECUS No. 5-12	Pack-Punch Processor and Reader for the PDP-5
DECUS No. 5-13	PDP-5 Assembler
DECUS No. 5-14	Dice Game for the PDP-5
DECUS No. 5-15	ATEPO (Auto Test in Elementary Programming and Operation of a PDP-5 Computer)
DECUS No. 5-16	Tape Duplicator for PDP-5/8
DECUS No. 5-17	Type 250 Drum Transfer Routine for Use on PDP-5/8

