

IDENTIFICATION  
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PRODUCT CODE: MAINDEC-08-DHKMC-B-D

PRODUCT NAME: PDP-8E EXTENDED MEMORY ADDRESS TEST (EABE)

DATE RELEASED: MAY 1976

MAINTAINER: DIAGNOSTIC GROUP

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1. ABSTRACT  
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MODIFIED TO RUN ON APT 8A SYSTEMS, APRIL 1975.  
SEE NOTES AT END OF DOCUMENT.  
MODIFIED TO RUN WITH A NEW CONSOLE PACKAGE MAY 1976.  
SEE SECTION 10 FOR CONSOLE ADDENDUM.  
MODIFIED TO RUN WITH NO CONSOLE TERMINAL MAY 1976.  
SEE SECTION 11 FOR OPERATING PROCEDURES ON A NON CONSOLE SYSTEM.

THE PDP-8E EXTENDED MEMORY ADDRESS TEST IS DESIGNED TO DETECT ANY LOCATION THAT CANNOT BE UNIQUELY ADDRESSED. THIS IS PERFORMED BY A SERIES OF FOUR TEST ROUTINES WHICH WILL TEST SYSTEMS EQUIPPED WITH FROM 8K TO 32K WORDS OF CORE MEMORY. AUTOMATIC PROGRAM RELOCATION IS PROVIDED IN ORDER TO TEST ALL MEMORY FIELDS FROM EACH MEMORY FIELD. TELETYPE PRINT-OUTS ARE PROVIDED FOR ERROR IDENTIFICATION, AND THE OPERATOR IS GIVEN A DEGREE OF CONTROL OVER THE PROGRAM BY VARIOUS SR SETTINGS.

2. REQUIREMENTS  
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2.1 EQUIPMENT  
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A PDP-8E OR A PDP-8A COMPUTER EQUIPPED WITH A MINIMUM OF 8K WORDS OF CORE MEMORY.

2.2 STORAGE  
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THE PROGRAM OCCUPIES CORE LOCATIONS 0000 TO 4777, WITH LOCATIONS 5000 TO 5177 USED AS A BUFFER AREA.

2.3 PRELIMINARY PROGRAMS  
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THE BINARY LOADER MUST BE IN MEMORY. ALSO, ALL DIAGNOSTICS FOR A BASIC 4K PDP-8E OR PDP-8A MUST HAVE BEEN PREVIOUSLY RUN SUCCESSFULLY.

3. LOADING PROCEDURE  
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LOAD THE PROGRAM WITH THE BINARY LOADER (BIN). THE PROGRAM MAY BE LOADED INTO ANY DESIRED CORE STACK BY HAVING BIN IN THAT CORE STACK.

4. OPERATING PROCEDURE

4.1 PROGRAM AND OPERATOR ACTION

- A. SET THE SR TO THE INSTRUCTION FIELD AND DATA FIELD OF THE STACK WHICH CONTAINS THE PROGRAM.
- B. PRESS KEY EXT0 ADDR LOAD.
- C. SET THE SR FOR DESIRED STARTING ADDRESS ACCORDING TO THE FOLLOWING TABLE.

ADDRESS	TEST EXECUTION
0200	RUN ALL TESTS
0201	RUN ONLY TEST 1
0202	RUN ONLY TEST 2
0203	RUN ONLY TEST 3
0204	RUN ONLY TEST 4

D. PRESS KEYS ADDR LOAD, CLEAR, AND CONT. A SETUP SR MESSAGE WILL BE PRINTED.

E. SET THE SR FOR DESIRED OPERATION ACCORDING TO THE FOLLOWING TABLE.

SWITCH	0 (DOWN)	1 (UP)
SR00	CONTINUE AFTER ERROR	HALT AFTER ERROR
SR01	TYPEOUT ERRORS	INHIBIT ERROR TYPEOUTS
SR02	NORMAL	TTY BELL ON ERROR
SR03	RELOCATE PROGRAM	INHIBIT PROGRAM RELOCATION
SR04	NORMAL	CHANGE STACK LIMITS
SR05	NORMAL	HALT AFTER CURRENT TEST
SR06-08	STARTING STACK LIMIT (0-7)	
SR09-11	ENDING STACK LIMIT (0-7)	

F. PRESS KEY CONT.

4.2

DETAILED SR EXPLANATION  
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 SR00-02 SR02, WILL RING THE TTY BELL ONCE FOR EACH ERROR.  
 SR00 AND SR01 HAVE NO EFFECT WITH SR02 SET.  
 SR03 SR03 MAY BE SET OR RESET AT ANY TIME AND THE PROGRAM  
 WILL ACT ACCORDINGLY  
 SR04 SR04 ALLOWS THE OPERATOR TO CHANGE THE STACK LIMITS AS  
 DEFINED BY SR06-11.  
 SR05 SR05 IS NORMAL HALT FOR PROGRAM  
 SR06-08 THESE SWITCHES DEFINE THE STARTING STACK LIMIT  
 (NORMALLY 0).  
 SR09-11 THESE SWITCHES DEFINE THE ENDING STACK LIMIT  
 (NORMALLY 7)

4.3

EXAMPLE OF SELECTING STACKS FOR TEST  
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 EXAMPLE 1: SR = 0007, 28K SYSTEM  
 STACKS SELECTED FOR TESTING ARE 6,5,4,3,2,1,0  
 EXAMPLE 2: SR = 0004, 28K SYSTEM  
 STACKS SELECTED FOR TESTING ARE 4,3,2,1,0  
 EXAMPLE 3: SR = 0022 28K SYSTEM  
 STACKS SELECTED FOR TESTING ARE 2  
 (NO RELOCATION WILL OCCUR)

EXAMPLE 4: SR = 0041 28K SYSTEM  
 STACKS SELECTED FOR TESTING ARE 6,5,4,1,0

NOTE 1: STACKS NOT IN THE SYSTEM ARE AUTOMATICALLY DE-SELECTED  
 AS IS EXAMPLE 1. STACK 7 IS NOT PRESENT THEREFORE NOT  
 SELECTED.

NOTE 2: A SINGLE STACK CAN BE SELECTED FOR TESTING PROVIDING  
 THE PROGRAM IS NOT IN THAT STACK AS IN EXAMPLE 3.

NOTE 3: ANY STACK OR GROUP OF STACKS CAN BE BY-PASSED AS IN  
 EXAMPLE 4. STACKS 2 AND 3 ARE NOT SELECTED, STACK 7  
 IS NOT PRESENT.

ERRORS  
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5.

THE CONTENTS OF A GIVEN MEMORY TEST LOCATION SHOULD ALWAYS BE  
 EQUAL TO ITS ADDRESS OR THE COMPLEMENT OF ITS ADDRESS. IF IT  
 IS NOT, A TEST ERROR WILL RESULT. A RELOCATION ERROR WILL  
 OCCUR IF THE RELOCATION COMPARISON CHECK FAILS.