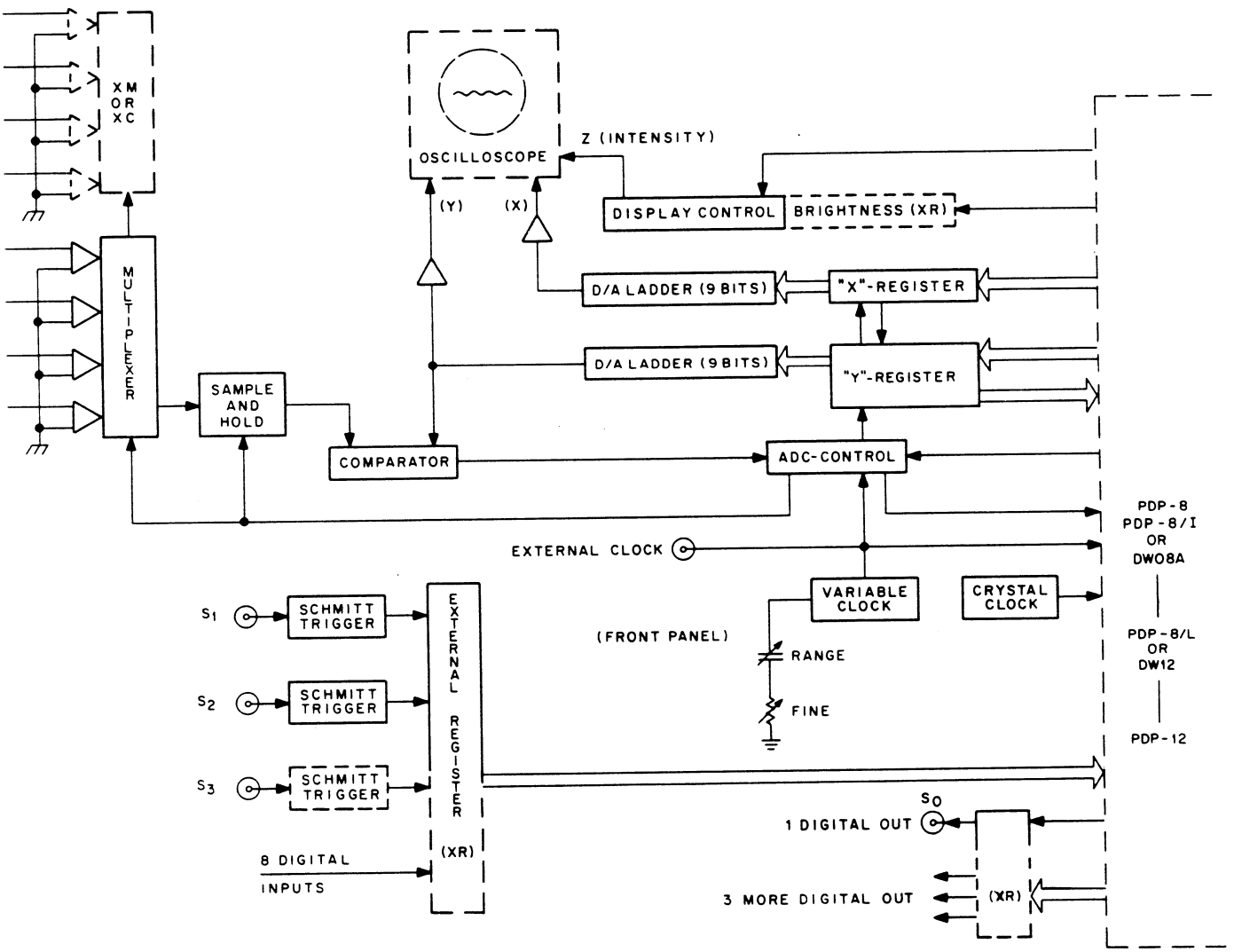

Diagram 1 AX08 Operational Flow Diagram

AX08 - LABORATORY PERIPHERAL

The AX08 was developed to integrate into one piece of electronics hardware all the accessories (A/D, multiplexer, Schmitt triggers, clocks, display, etc.) commonly required with the PDP-8/L or PDP-8/I to assemble a compact, inexpensive, yet versatile computer system especially tailored to the laboratory environment. Further advantages are convenience and efficiency in programming and protection from analog-input overloads. By eliminating the duplication of modules required with separate A/D converters and displays, cost was decreased without loss of capacity. The DW08A, IO Bus Converter Panel is required when using the AX08 on the PDP-8/L.

As shown in Diagram 1, the basic elements of the AX08 are as follows:

I. Analog-to-Digital Converter Section
   - A. Preamplifiers
   - B. Multiplexer
   - C. Sample-and-Hold
   - D. Converter
   - E. Timing Error Flag

II. Schmitt Triggers

III. Crystal-controlled and RC Clocks

IV. "Enable" register

V. "External" register

VI. Display Control

VII. Power Supply

The following options may be added:

Option XR - Expands the registers to include three levels of brightness control on the scope; adds eight digital inputs, three digital outputs, and one additional pulse input.

Option XM - Expands the analog section for eight inputs - includes extra multiplexer and preamplifiers.

Option XC - For expansion of the analog section beyond eight inputs - an additional four channels including preamplified multiplexed analog input (4XC's and one XM are required for expansion of basic AX08 to 24 inputs).

I. Analog-to-Digital Converter (ADC) Section

The ADC Section, including preamplifiers, multiplexer, sample-and-hold, and 9-bit successive approximation converter was designed to perform as a system with an accuracy of ±0.2%, ±1/2 LSB (Least Significant Bit).

Basic elements of the ADC have the following specifications:

A. Preamplifiers - Two A202 modules (in basic configuration) each containing two preamplifiers for two input channels. As special systems and at additional cost, 3-wire (balanced) low-level differential preamplifiers are available with gains up to 1000.

Input

Amplitude:	±1V
Impedance:	50K ohms, ±10%
Configuration:	Single-ended, resistive to ground
Leakage current:	Negligible at 50K ohms input impedance
Overload Protection:	Input clamped at 1.7V; protected to 1000% overload

Amplifier

Recovery:	2 μs or faster after 1000% overload
Response:	3 db down at or above 50 KHz.
Gain:	Factor of 5 (suitable for driving A130 Multiplexer); variable ±10%.

Output

Amplitude: ±5V nominal

Impedance: 10K ohms nominal

Zero level offset: Adjustable, ±10%

B. Multiplexer - In basic configuration one A130 module containing 4 diode-selection multiplexers.

Switching time: Less than or equal to 1 μs (full scale)

Slew rate: Less than or equal to 1 μs, as used in the system.

Input

Amplitude: ±5V

Impedance: 10K ohms nominal

Configuration: Emitter-follower circuit

Output

Amplitude: -0.5 to -5.5V from multiplexer

Gain and offset accurate to ±4% (adjustable)

C. Sample-and-Hold - One A401 module - for up to 24 channels.

Tracking: Any signal with a slew rate of less than 2 μs for full analog input scale; accuracy better than 0.2%

"Hold" Time - Approximately 2 μs after sampling pulse.

"Held" Value - Value of input signal at "hold" time.

Input (amplitude) - Nominal -0.5V to -5.5V (from A130 module).

Duration of Hold - At least 17 μs

Output

Amplitude: 0 to -10V nominal

Impedance: Nominal 5K ohms (non-linear)

D. Converter (Successive Approximation Type)

Precision: 9 bits, including sign (1 part in 512)

Maximum sampling rate: 17 μs per point with resultant digital value held in ADC buffer.

E. Timing Error Flag

This flag is set whenever two conversions are initiated without the result of the first conversion being read (by the instruction RADC).

It is sensed with instruction SKER and will cause an interrupt if Bit 4 of Enable Register has been set. The second conversion will be inhibited.

The instruction CLER will clear the ADC error and ADC done flags. The next ADCV will not cause a timing error.

G. Front panel knobs are connected to analog channels 34-37 implemented in all AX08's.

II. Schmitt Triggers

Two W501 modules, each containing a Schmitt trigger, connected to potentiometers and input BNC connectors on the front panel. Option XR adds one additional pulse input (BNC connector) and a W501 module connected to a third front-panel potentiometer.

The Schmitt triggers are threshold detectors and can accept pulse or continuously (and slowly) varying analog inputs. In either case, the circuit will fire when the trigger threshold has been exceeded in the negative direction after having been 0.7V above trigger threshold.

Trigger level: Variable from -0.5 to -2.5V

Input: ±10V maximum

Output level: Switches from -3V to 0 on triggering.

III. Crystal-controlled and RC Clocks

A. Crystal Clock - The crystal clock runs at the rate of 10 kHz (100 μs between pulses). Each pulse "sets" the crystal clock flag. The crystal clock can be used to supply timing information to the computer in two ways:

(1) Executing instruction SKXK (Skip on crystal clock flag). Will cause a program branch if the crystal clock flag is up ("set").

(2) A program Interrupt - If Bit 3 of the Enable Register is in the "one" state, a Program Interrupt will occur when clock flag goes up.

In order for the state of the crystal clock flag to convey meaningful timing information it must be cleared after it is read or "sensed". This can be done with instruction CLXK (clear crystal clock flag).

B. RC Clock - A variable frequency (16 Hz to 200 kHz) oscillator controlled by a multiple position switch (coarse) and potentiometer (fine) on the front panel of the AC08 is used to generate RC clock pulses (if Bit 10 of the Enable Register is set).

Relationship between RC or External Oscillator and RC Clock Pulse Rate:

(1) An RC Clock Pulse is generated every 4 oscillator pulses if Bit 0 of Enable Register is in the "zero" state and bit 10 is in "one" state.

(2) An RC Clock Pulse is generated every 32 oscillator pulses if Bit 0 of Enable Register is in the "one" state and bit 10 is in "one" state.

(3) An RC Clock Pulse is generated every time an external clock pulse is received at EXTERNAL connector (on front panel of AX08), if Bit 9 of Enable Register is in the "one" state.

RC Clock pulses set the RC clock flag and can be used to supply timing information to the computer in the following ways:

(1) Executing instruction SKRK (Skip on RC Clock Flag) causes a program branch if the RC Clock Flag is set.

(2) A program interrupt will be caused if Bit 2 of Enable Register is in "one" state and RC Clock Flag is set.

(3) A/D conversions will be automatically initiated at the RC Clock rate if Bit 1 of Enable Register is set.

Instruction CLRK clears the RC Clock Flag.

IV. ENABLE REGISTER (See Diagram 2)

This register is primarily used to set up conditions to make possible or "enable", actions by other elements of the AX-08. Certain bits of the Enable Register must be in a given condition (usually set) before some action can cause some other action to occur - such as a clock or A/D flag causing a program interrupt.

A. Conditions can be set up for program interrupts actuated by the following elements with the indicated bits of the Enable Register:

1. Analog-to-Digital Converter - Bit 5 set (Interrupt initiated when A/D Done flag goes up).

2. ADC Timing Error Indicator - Bit 4 set (Interrupt initiated when ADC Timing Error flag goes up).

3. Crystal-controlled Clock - Bit 3 set (Interrupt initiated when Crystal Clock flag goes up).

4. RC Clock - Bit 2 set (Interrupt initiated when RC Clock flag goes up).

B. The RC Clock is started as soon as Bit 10 of the Enable Register is set. If Bit 0 of the Enable Register is in the "zero" state, "cleared", the RC Clock flag will go up 2 oscillator pulses later and every 4 thereafter (or every 32 oscillator pulses, if Bit 0 is set).

C. When Bit 9 is set, each pulse arriving at the EXTERNAL connector on the front panel generates an RC Clock pulse.

D. When Bit 1 is set, A/D conversions are initiated by RC Clock pulses.

E. With Option XR the condition (state) of 3 external relays can be controlled by bits 6, 7, and 8 of the Enable Register.

F. The level on Sync channel 0 will change as soon as Bit 11 is set and will remain at the new level as long as Bit 11 remains set.

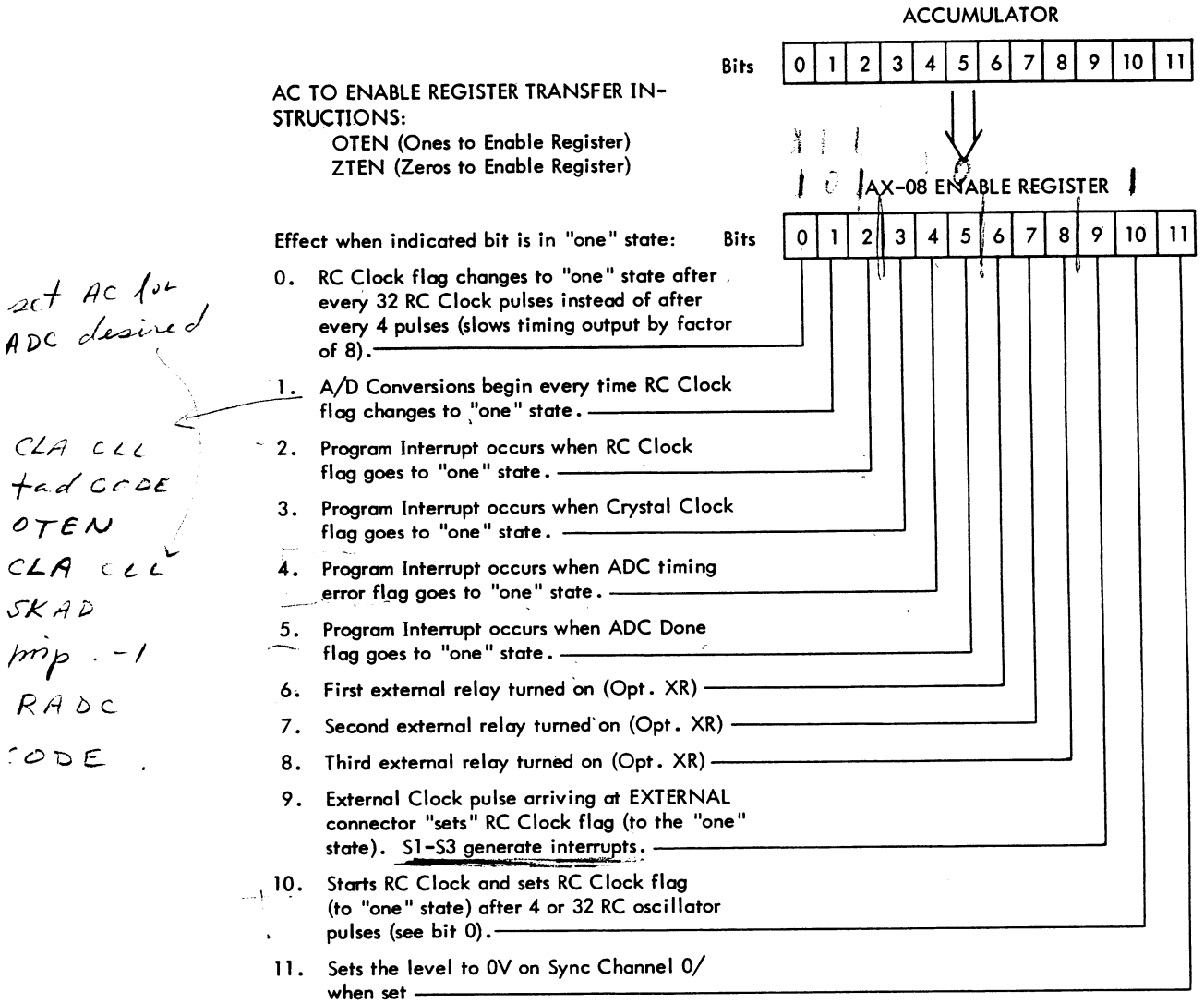

Diagram 2 A Summary of the Function of the Various Bits of the Enable Register

Any or all bits of the Enable Register can be set by having the corresponding bit number(s) of the accumulator set to a "one" and executing the instruction OTEN (Ones to Enable Register). All bits in the Enable Register (except Bit 11) may be cleared by having corresponding AC bits in the "zero" state and executing the instruction ZTEN (zeros to Enable Register). Bit 11 must be cleared with the instruction XRCL (External Register Clear). Bit 11 of the Enable Register is the same flip-flop as Bit 0 of External Register.

G. When Bit 9 of the Enable Register is set, inputs firing Schmitt triggers will cause interrupts.

V. External Register

The External Register is a set of flip-flops, which is used as a buffer between external devices and the computer system. The inputs connected to the External Register can be divided into the following three categories:

A. Eight "Contingency" Inputs located on the front panel "blue-ribbon" connector. A 0V input (C0-C7) will set the corresponding flip-flop in the External Register if option XR is implemented. (See Diagram 3.)