

New Module News

6206 MA, PC, IR FLIP-FLOPS

6/17/64

Non-Catalog (\$440.00) Avail. Now.
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The 6206 is used in the control section of the PDP-6. It contains one bit each of the Program Counter, Instruction Register, and Memory Address registers and gating circuits for each bit. The module contains 3 buffered 10 mc. flip-flops and associated gating circuitry. Two of the flops can generate a carry pulse. Each flop has a direct clear input, and also a gated set input or a normal set input or both. Double length board. Two connectors: front 22 pins, back 18 pins. Frequency Limit: 10 mc.

Maximum delay for output fall: 70 nanoseconds.

Maximum delay for output rise: 50 nanoseconds.

INPUTS

Program Counter: Direct Clear- Pin RE - Pos. pulse from P.A.

Gated Set- Pin RC - Neg. pulse from P.A.

Gated with MA (1).

Increment input- Pin E - Neg. pulse.

Instruction Register: Direct Clear- Pin RS or RR - Pos. pulse from P.A.

Normal Set- Pin X - Pos. pulse from collector of inver.

Gated Set- Pin Y - Neg. level input.

Pin RU or RT - Neg. Pulse from P.A.

Memory Address: Direct Clear- Pin RH - Pos. pulse from P.A.

Normal Set- Pin L - Pos. pulse from inverter.

Increment input- Pin P = Neg. pulse.

Gated Set- Pin RM - Neg. pulse from P.A.

Pin R - Neg. level.

Pin RP - Neg. pulse from P.A.

Gated with PC(0)

Pin RK - Neg. pulse from PAA.

Gated with MAS(1).

Level input- Pin J - input to MA gated set & MAS;=MA; gat

OUTPUTS

Program Counter: PC(1) - Pin H

Carry pulse- Pin F.

Instruction Register: IR(1) - Pin W - Bus driver output.

IR(0) - Pin U - Bus driver output.

Indicator Driver:- Pin V

Memory Address: MA(1) - Pin T

MA(0) - Pin M

Carry Pulse - Pin N

MA;= MAS; - Pin K.

POWER -15 volts/300 ma. +10 volts(A)/3.0 ma. +10 volts(B)/140 ma

