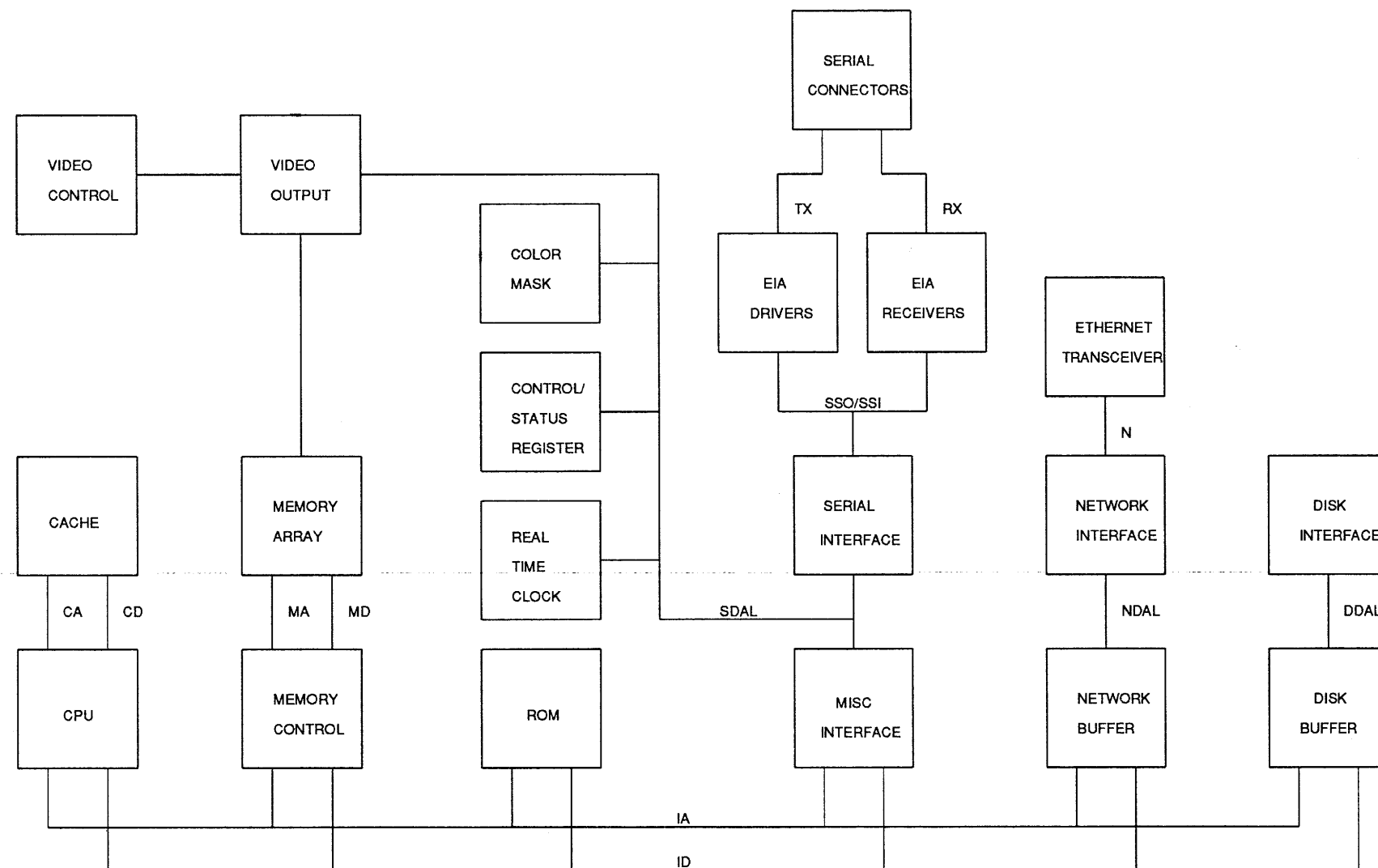


Include
decis



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CHK	CHANGE NO.	REV.

digital

USRA:
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DRN.

CHK'D.

DATE

DATE

ENG.

M. NIELSEN

BOARD LOCATION:

SHEET

TOP DOCUMENT NUMBER:

DATE
31 OCT 88

1 OF 21

TITLE:

PMAX System Module

SIZE

B

CODE

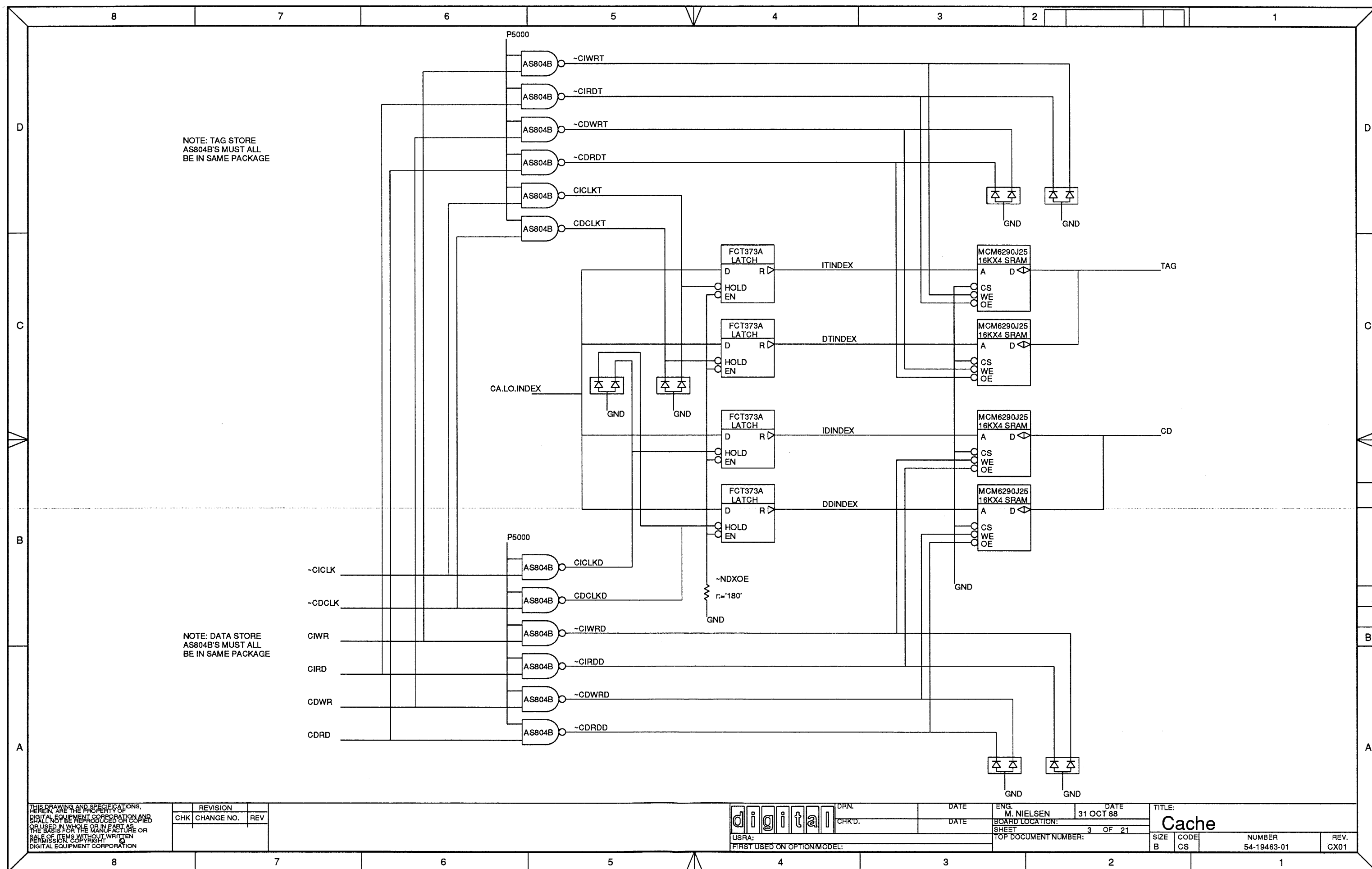
CS

NUMBER

54-19463-01

REV.

CX01



Declarations

```

type
  memAdr = record
    reserved: bits(7);
    bank: bits(3);
    row, col: bits(10);
    byte: bits(2);
  end;
var
  mra, mwa: memAdr;
  mc: bits(10);
  i, j: cardinal;
  vrr, vwr, vc, vs: bits(2);

```

```

f:= 'PAL:MUXCTL';
tpd:= '15ns';
r1class:= inputPin;
PAL22V10
D10 R10
D9 R9
D8 R8
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
CLK
IA[28]
MEMCLK
~MEMRD
CA.HI[12]
~IWR
VCYC
~SYSRESET
MONO

```

```

Code
for i := 0 to 9 do begin
  if i = 7 then
    j := i+1
  else if i = 8 then
    j := i-1
  else
    j := i;
  mcj;
end;
for i := 0 to 1 do begin
  vrr;
  vwr;
  vcj;
  vsj;
end;

```

```

f:= 'PAL:VROW';
tpd:= '25ns';
PAL22V10
D10 R10
D9 R9
D8 R8
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
CLK
~VROWTS
VREQD
VREQS
~SYSRESET
MEMCLK

```

```

CA MRA
IA MWA

```

```

f:= 'PAL:SCANMUX';
tpd:= '15ns';
r1class:= inputPin;
PAL22V10
D10 R10
D9 R9
D8 R8
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
CLK
VROW

```

```

f:= 'PAL:MEMSEQ';
tpd:= '15ns';
PAL22V10
D10 R10
D9 R9
D8 R8
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
CLK
~MEMTS
VREQD
CONFLICT
IA[28]
~SYSRESET
VREQS
CA.HI[12]
~IWR
~MEMRD

```

```

f:= 'PAL:MEMSEQ';
tpd:= '15ns';
PAL22V10
D10 R10
D9 R9
D8 R8
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
CLK
~MEMTS
VREQD
CONFLICT
IA[28]
~SYSRESET
VREQS
CA.HI[12]
~IWR
~MEMRD

```

```

FCT374A
REGISTER
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
EN
CLK
~ID2MDERLY
~MASKOERLY
~ID2MD
~MASKOE

```

```

FCT138A
DECODER
4S 7F
2S 6F
1S 5F
4F 3F
3F 2F
1F 0F
E3
E2
E1

```

```

F374
REGISTER
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
EN
CLK
VREQD
VREQS
VREQR
VREQR2

```

```

f:= 'PAL:RASCAS';
tpd:= '15ns';
r1class:= inputPin;
r8class:= inputPin;
r9class:= inputPin;
r10class:= inputPin;
PAL22V10
D10 R10
D9 R9
D8 R8
D7 R7
D6 R6
D5 R5
D4 R4
D3 R3
D2 R2
D1 R1
D0 R0
CLK
WACCTYP[1]
WACCTYP[0]
IA[1]
IA[0]
CA.HI[12]
~MEMRD
MEMCLK
DCOK
~IWR
VCYC
CONFLICT

```

```

P5000
r:= '3K'
r:= '3K'
~REFEN
~ICAS
r:= '27'
~CAS
RASEN
~CRAS
AS08
~IRAS
r:= '27'
~RAS
r:= '27'
MA
r:= '27'
VA

```

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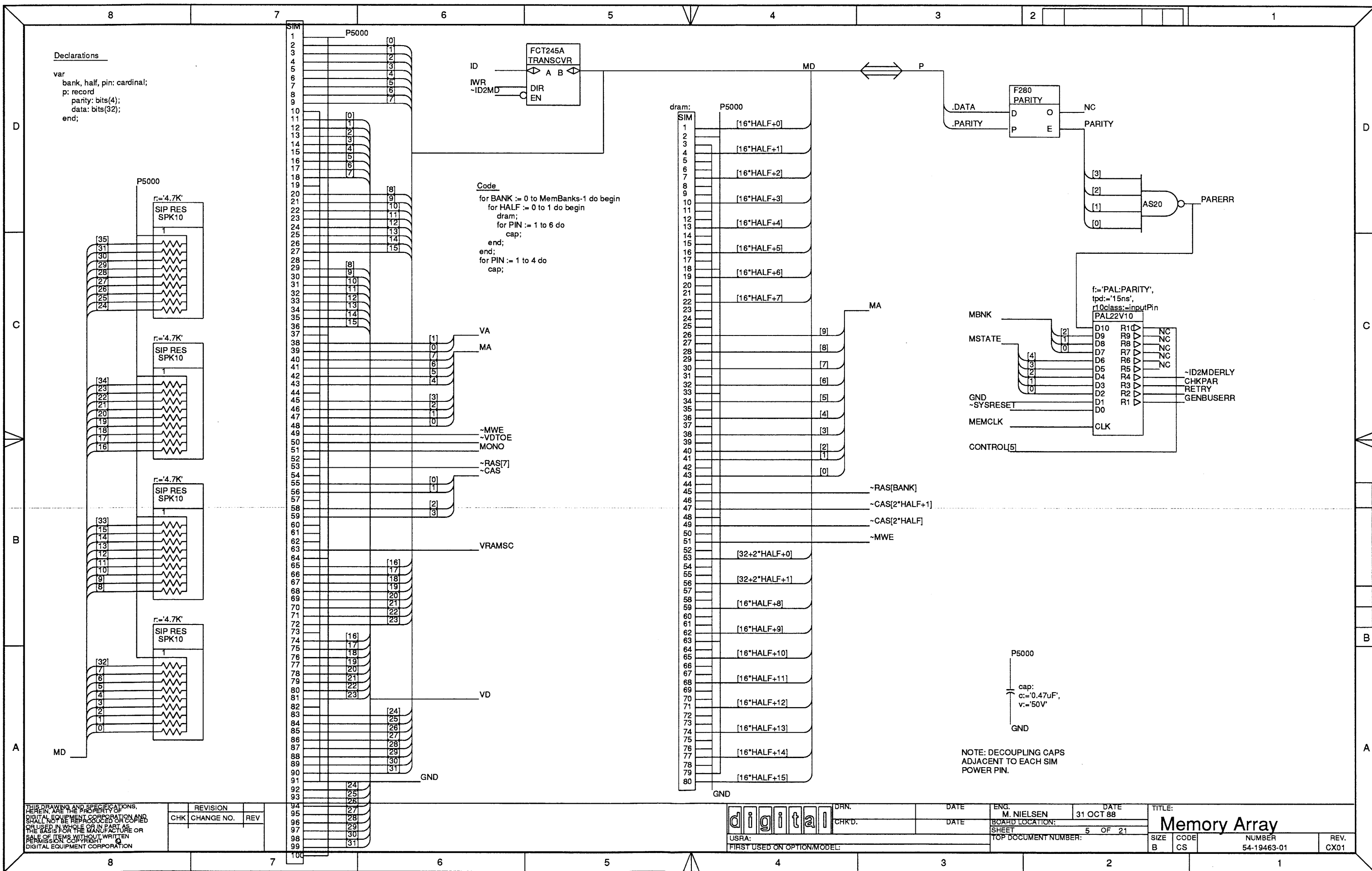
REVISION	CHK	CHANGE NO.	REV

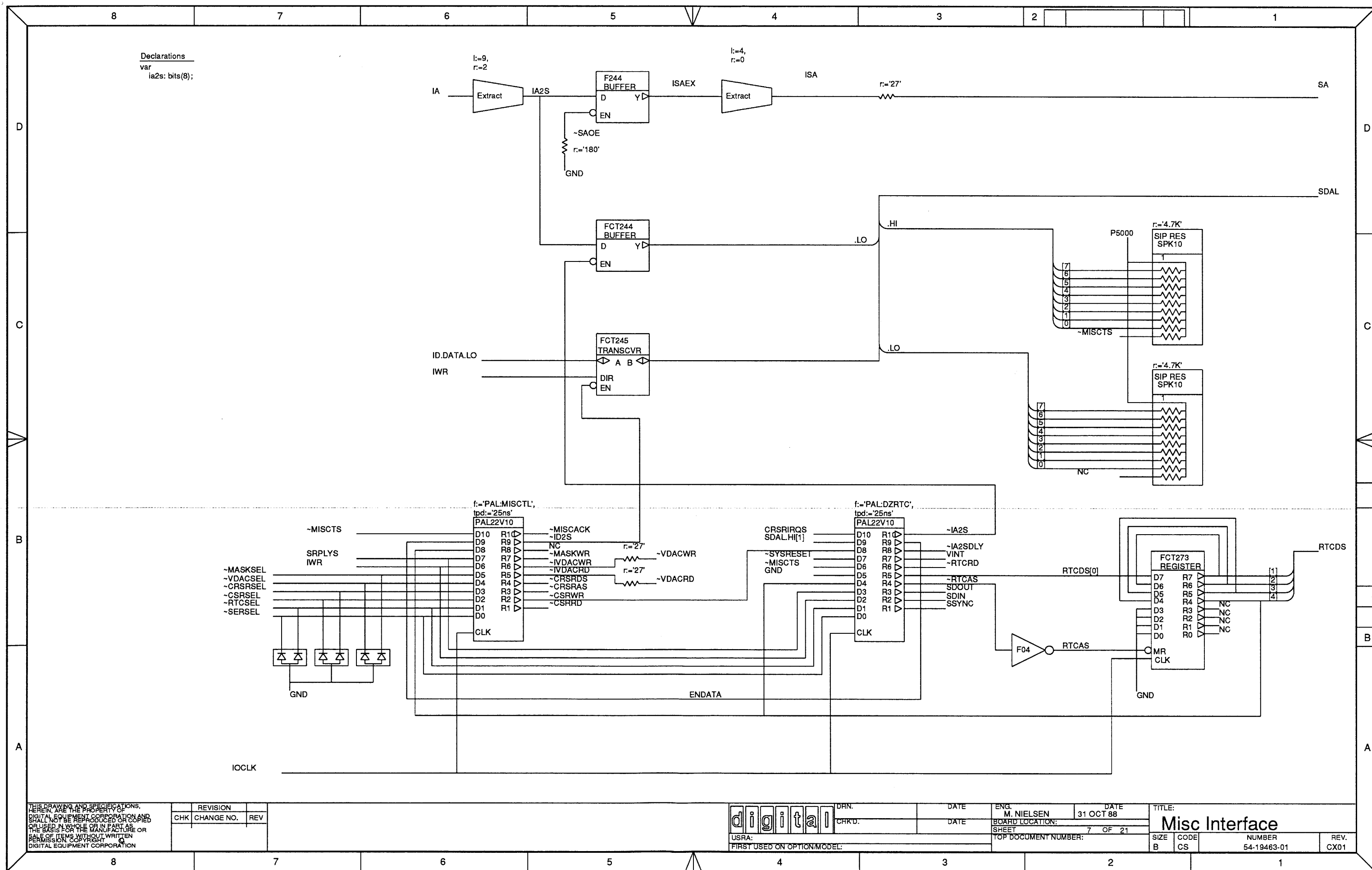
digital
USRA:
FIRST USED ON OPTION/MODEL:

DATE
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ENG.
M. NIELSEN
BOARD LOCATION:
SHEET
TOP DOCUMENT NUMBER:

DATE
31 OCT 88
TITLE:
Memory Control
SIZE
CODE
NUMBER
54-19463-01
REV.
CX01





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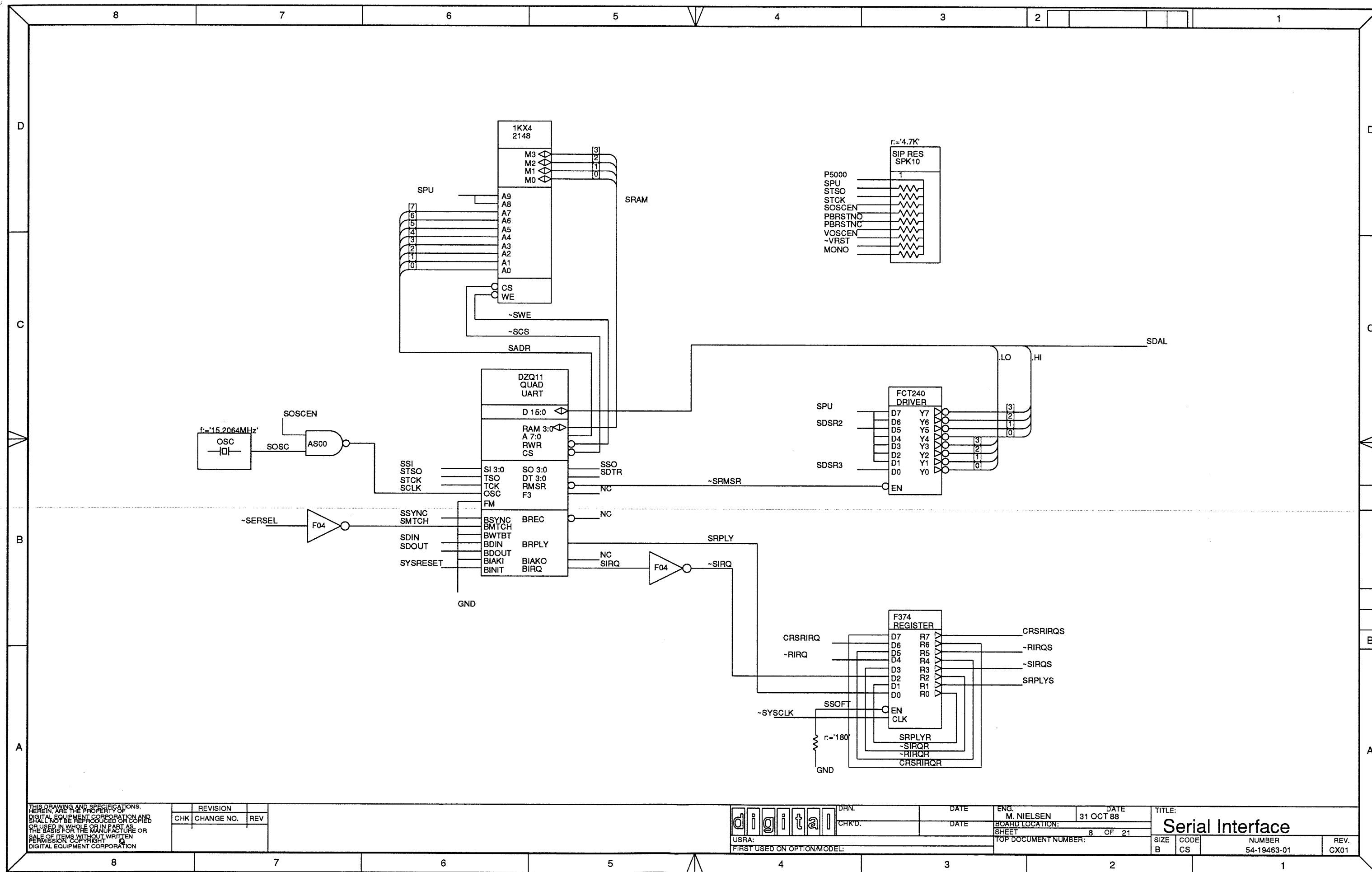
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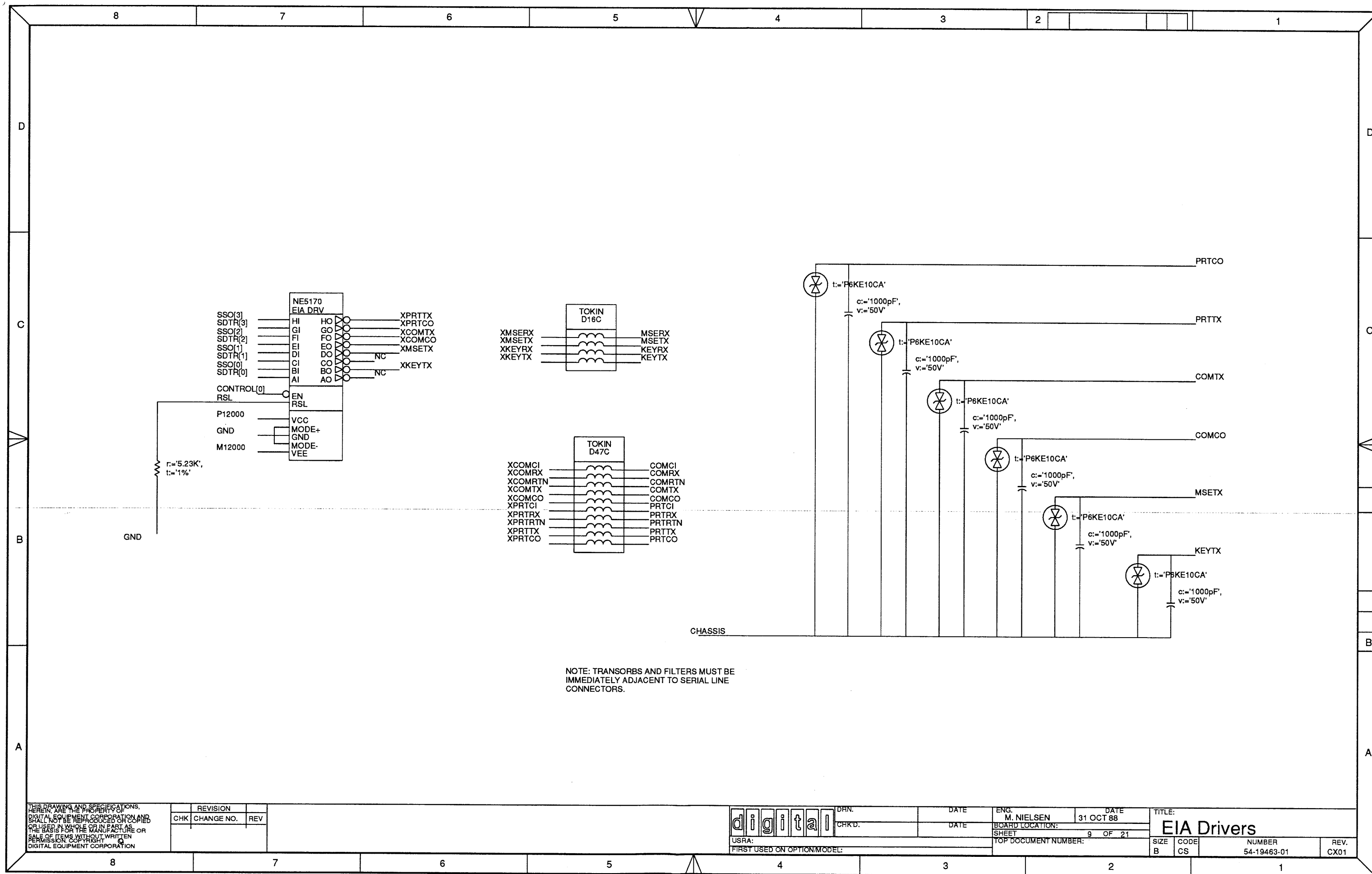
ENG.
M. NIELSEN
BOARD LOCATION:
SHEET 7 OF 21
TOP DOCUMENT NUMBER:

DATE
31 OCT 88

TITLE:
Misc Interface

SIZE B	CODE CS	NUMBER 54-19463-01	REV. CX01
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M. NIELSEN

DATE
31 OCT 88

BOARD LOCATION:
SHEET 9 OF 21
TOP DOCUMENT NUMBER:

TITLE:

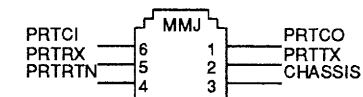
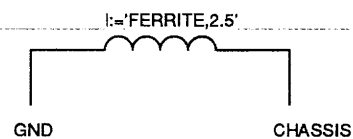
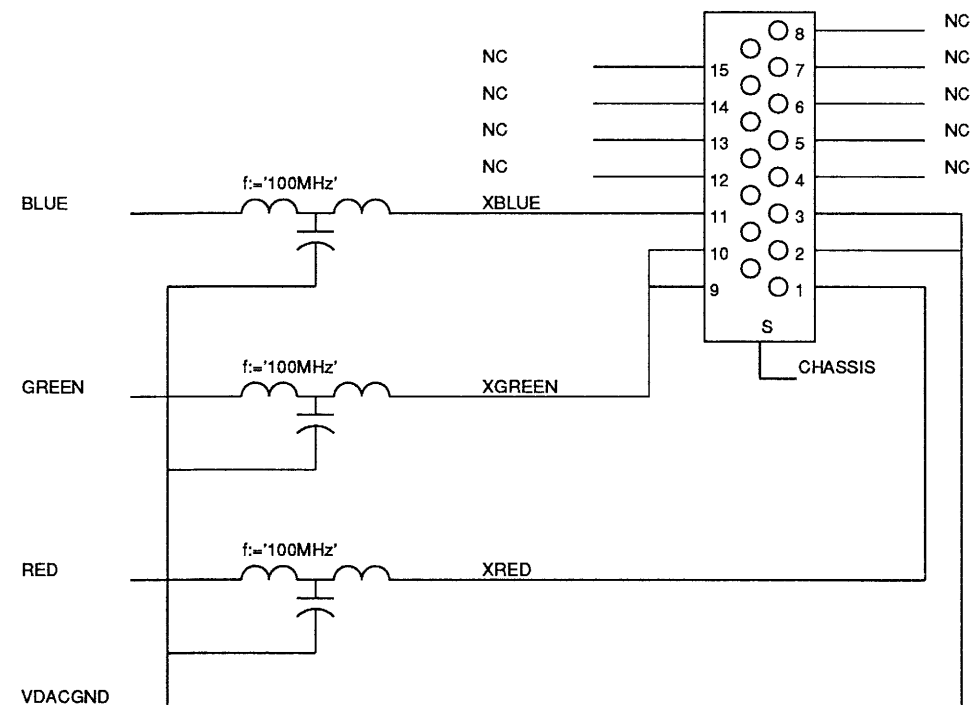
EIA Drivers

SIZE
B CS

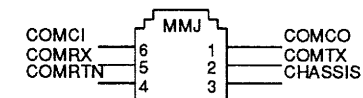
NUMBER
54-19463-01

REV.
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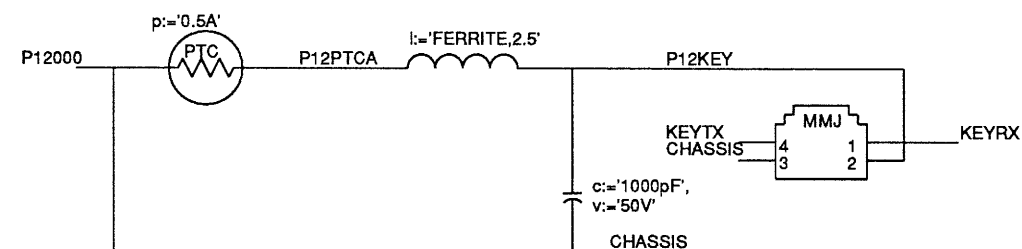
Video Connector



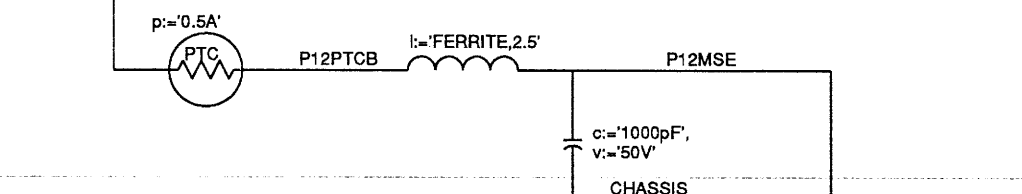
Printer Connector



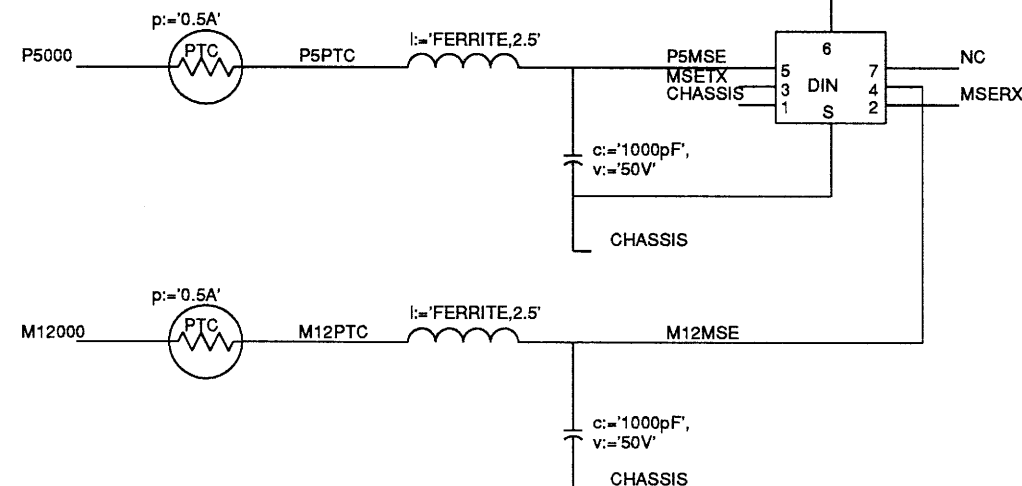
Comm Connector



Keyboard Connector



Mouse Connector



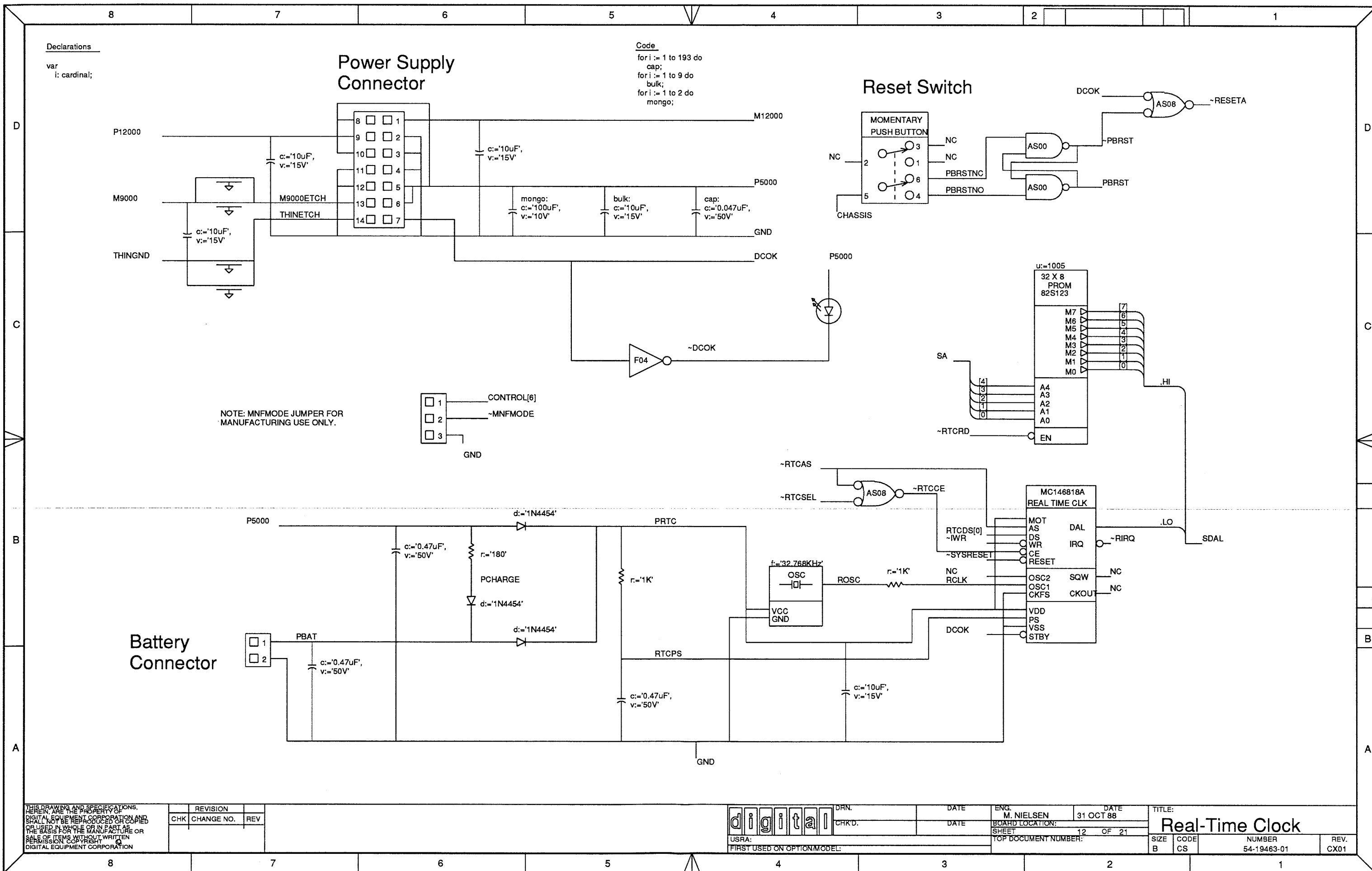
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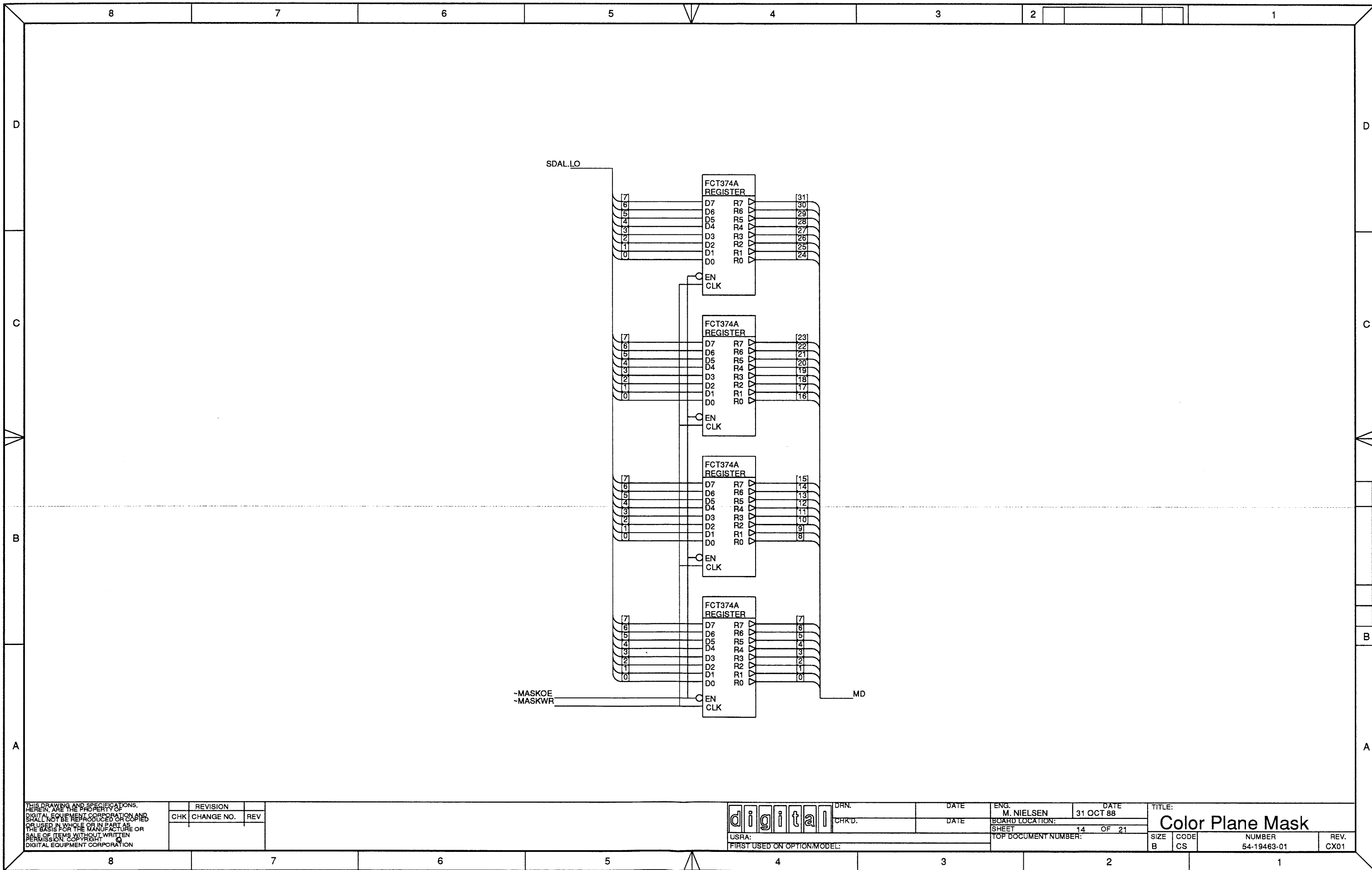
REVISION	CHK	CHANGE NO.	REV

digital
USRA:
FIRST USED ON OPTION/MODEL:

DRN.	DATE	ENG.	DATE
CHK'D.	DATE	M. NIELSEN	31 OCT 88
		BOARD LOCATION:	
		SHEET	11 OF 21
		TOP DOCUMENT NUMBER:	

TITLE:			
Serial Connectors			
SIZE	CODE	NUMBER	REV.
A	CS	54-19463-01	CX01





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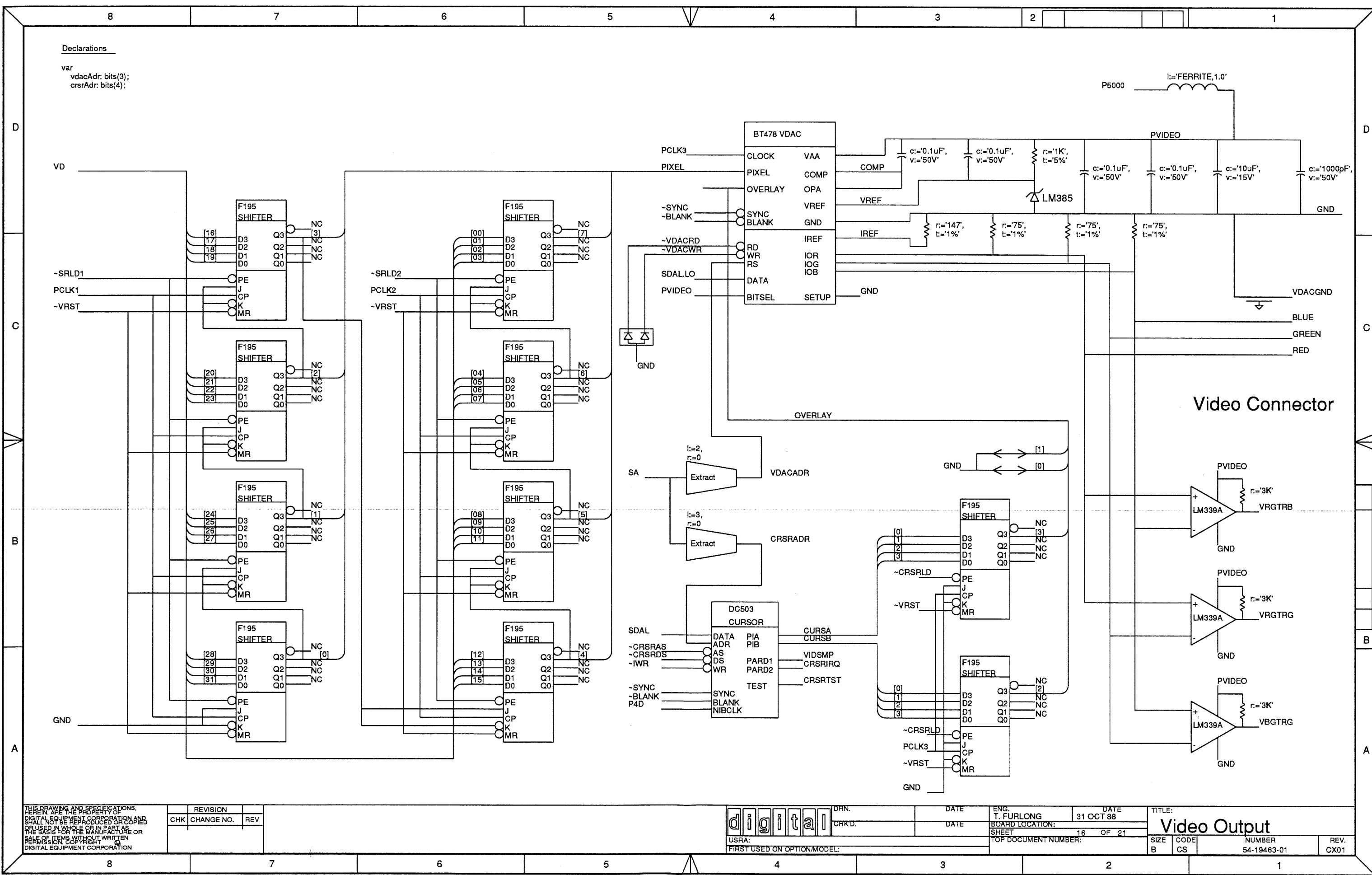
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M. NIELSEN
BOARD LOCATION:
SHEET 14 OF 21
TOP DOCUMENT NUMBER:

DATE
31 OCT 88

TITLE:
Color Plane Mask

SIZE B	CODE CS	NUMBER 54-19463-01	REV. CX01
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REVISION		
CHK	CHANGE NO.	REV

digital DRN.
CR'D.
USRA:
FIRST USED ON OPTION/MODEL:

DATE	ENG.	DATE	TITLE:
	T. FURLONG	31 OCT 88	Video Output
	BOARD LOCATION:		
	SHEET	16 OF 21	
	TOP DOCUMENT NUMBER:		

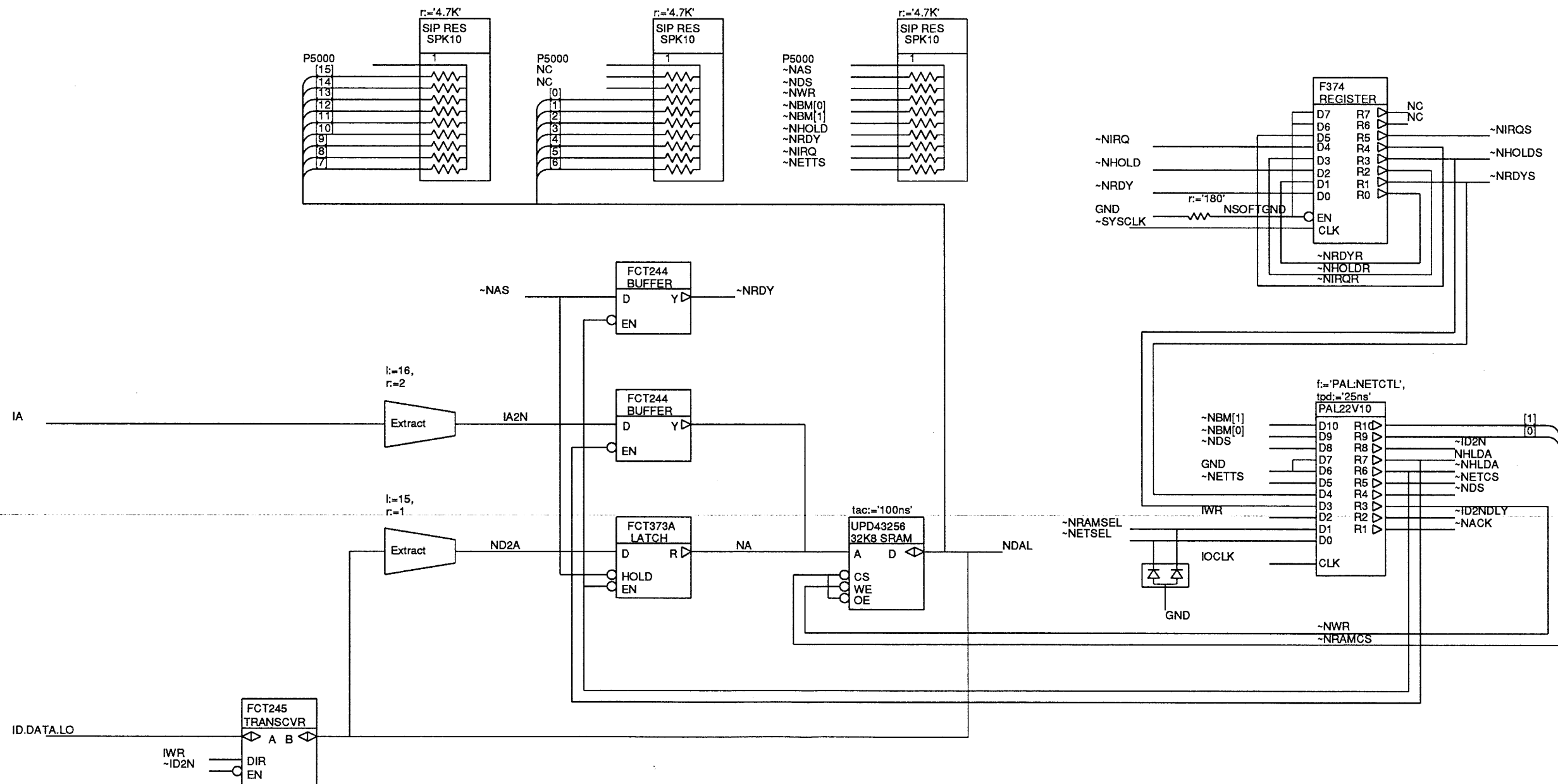
SIZE	CODE	NUMBER	REV.
B	CS	54-19463-01	CX01

Declarations

```

var
  ia2n: bits(15);
  nd2a: bits(15);

```



NOTE: NET BUFFER IS 32K 16-BIT WORDS. BUFFER IS 16-BIT-ALIGNED TO LANCE, 32-BIT-ALIGNED TO CPU. BUFFER HAS 8-BIT ACCESS TO LANCE, 16-BIT ACCESS TO CPU. CPU IS DEFAULT MASTER OF NDAL, AND IS STALLED FOR LANCE-CSR OR BUFFER ACCESS IF LANCE DMA IS IN PROGRESS.

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CHK'D.

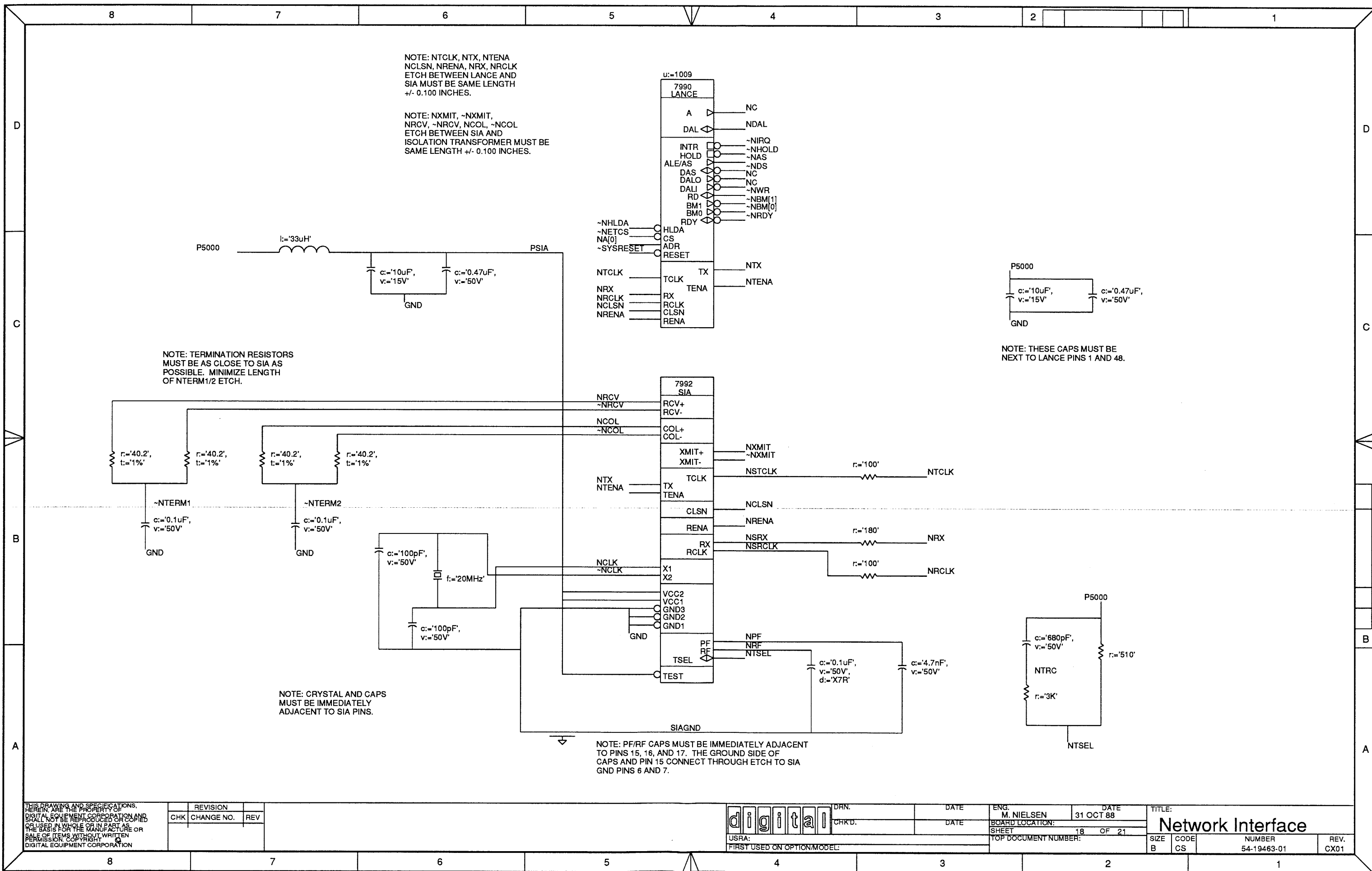
DATE
DATE

ENG.
M. NIELSEN
BOARD LOCATION:
SHEET 17 OF 21
TOP DOCUMENT NUMBER:

DATE
31 OCT 88

TITLE:
Network Buffer

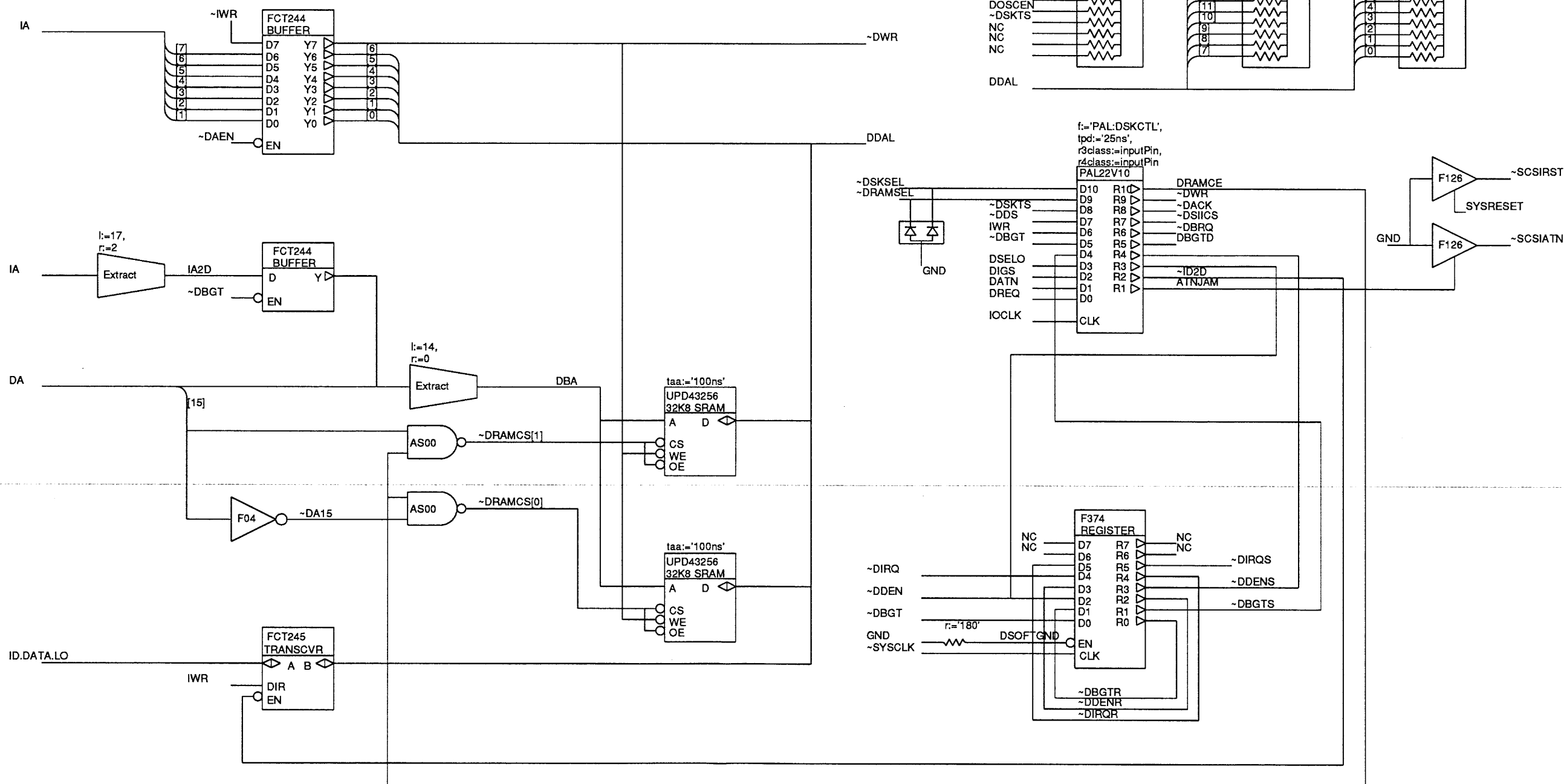
SIZE CODE NUMBER REV.
B CS 54-19463-01 CX01



Declarations

```
var
  ia2d: bits(16);
  dba: bits(15);
```

NOTE: DISK BUFFER IS 64K 16-BIT WORDS. BUFFER IS 16-BIT-ALIGNED TO SII, 32-BIT-ALIGNED TO CPU. BUFFER HAD 16-BIT ACCESS TO SII AND CPU. SII IS DEFAULT MASTER OF DDAL. CPU IS STALLED FOR SII-CSR OR BUFFER ACCESS IF SII DMA IS IN PROGRESS.



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CHK	REVISION	REV
	CHANGE NO.	

digital
USRA:
FIRST USED ON OPTION/MODEL:

DRN.

CHK'D.

DATE

DATE

ENG.

M. NIELSEN

DATE

31 OCT 88

TITLE:

Disk Buffer

BOARD LOCATION:

SHEET

TOP DOCUMENT NUMBER:

20

OF 21

SIZE

B

CODE

CS

NUMBER

54-19463-01

REV.

CX01

