M242
J-K Flip-Flops

The M242 module contains three J-K flip-flops augmented by multiple-input AND gates for general use as gated control flip-flops or buffers. A truth table for the clocked set and reset conditions appears below. The J or K inputs are HIGH when the three inputs to their corresponding AND gate are HIGH; otherwise, they are LOW. Note that when the J and K inputs are both HIGH, the flip-flop complements on each CLOCK pulse.

Starting Condition (Output)		Input Condition		Result at End of Standard CLOCK Pulse (Output)	
1	0	J	K	1	0
L	H	L	L	No Change	
		L	H	No Change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No Change	
		L	H	L	H
		H	L	No Change	
		H	H	L	H

The J and K inputs must be stable during the leading edge threshold of a standard CLOCK input and must remain stable during the positive state of the CLOCK. The J and K inputs do not have to remain stable after the CLOCK pulse reaches its trailing edge threshold (negative-going voltage). The minimum width of the CLOCK pulse should be 12 ns.

Application of a LOW level to the R input for at least 16 ns resets the flip-flop unconditionally. Application of a LOW level to the 5 input for at least 16 ns sets the flip-flop unconditionally. Propagation delay time to logical 1 level (HIGH) from trailing edge of the CLOCK pulse to output is 21 ns (maximum). Propagation delay time to logical level (LOW) from trailing edge of the CLOCK pulse to output is 27 ns (maximum).

Propagation delay time to logical 1 level (HIGH) from S and R input to output is 12 ns (maximum). Propagation delay time to logical 0 level (LOW) from S and R input to output is 24 ns. Maximum clock frequency is 24 MHz.

The following are the input, output, and power characteristics of the M242 module.

INPUTS: All inputs but the S and R input present 1.25 TTL unit loads. The S and R input presents 2.5 unit loads.

OUTPUTS: Each output is capable of driving 12 unit loads.

POWER: Power dissipation of the M242 module is 5V at 90 mA (maximum).