M240
R-S Flip-Flops

The M240 module contains six R-S-type flip-flops. Each flip-flop consists of two NAND gates with cross-coupled outputs. Two inputs are provided for setting the flip-flops, and one input is provided for resetting the flip-flops. The following truth table defines the operation of the flip-flops. When the SET output (F1) is HIGH, both of the SET inputs (C1 and B1) are HIGH. When the SET output is LOW, either one or both SET inputs are LOW.

Previous State		Input Condition		Result	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	No Change	
H	L	H	H	No Change	
H	L	L	H	No Change	
L	H	H	L	No Change	
L	H	L	L	H	H*
H	L	L	L	H	H*

*Ambiguous state: In practice, the input that stays low longest assumes control.

Propagation delay time from SET or RESET to logical 1 (HIGH) level output is 10 ns (maximum). Propagation delay time from SET or RESET to logical 0 (LOW) level output is 20 ns (maximum).

The following are the input, output, and power characteristics of the M240 module.

INPUTS: Each input presents 1.25 TTL unit loads.

OUTPUTS: Each output is capable of driving 34 TTL unit loads.

POWER: Power dissipated in the M240 module is 5V at 185 mA.