M223
MA and MB Registers

The M223 module contains two 4-bit registers with input gating logic. Five of these modules are used to form the 18-bit memory buffer (MB) register and the 13-bit memory address (MA) register that are used in each memory bank of the PDP-15. (Refer to Engineering Drawings D-BS-MM15-0-3 through D-BS-MM15-0-5.) The MA register receives the memory cell address from the central processor or the I/O processor and selects a specific core location. The data or instruction word to be read from or written into the specified core location travels through the MB register to or from the central processor and the I/O processor.

The following are the input, output, and power characteristics of the M223 module.

INPUTS: All input connections and the TTL unit loading they present are shown below.

Name	Pin	Loading
MDL	D2, E2, F2, H2	1 each
MB LOAD	J1	8
MB CLEAR	J2	12
MA LOAD	P1	4
MA HOLD	P2	4
SA (MB D SET)	K2, L2, M2, N2	2 each

OUTPUTS: Each MB output (pins K1, L1, M1, and N1) is capable of driving 9 unit loads. Each MA output (pins R1, R2, S1, S2, U1, U2, V1, and V2) is capable of driving 10 unit loads.

POWER: Power dissipation of the M223 module is 5V at 175 mA (maximum).