M214
Data Storage Register

The M214 module contains a 6-bit adder and a 6-bit storage register with input gating logic. Three of these modules are connected in tandem to form the 18-bit data storage register (DSR) used in the I/O processor of the PDP-15. (Refer to Engineering Drawings D-BS-KD15-0-1 through D-BS-KD15-0-3.) The register is used for exchanging data between memory and I/O devices. Input gating logic is included in the module for strobing the memory data lines (MDL), I/O buffer (IOB), and the I/O address (IOA) into the register.

The following are the input, output, and power characteristics of the M214 module.

INPUTS: The following list shows all input connections and the TTL unit loading they present:

Name	Pin	Loading
CARRY-IN	U1	4
IOA to DSR	R2	6
IOB to DSR	R1	6
MDL to DSR	H1	6
DSR to DSR	M2	6
IOA	B2, C1, K2, J1, P2, P1	1 each
IOB	H2, F2, L2, L1, S2, T2	1 each
MDL	A1, D2, J2, F1, N2, N1	1 each
STROBE	V2	6

OUTPUTS: Each DSR output (pins E2, E1, K1, M1, U2, and V1) is capable of driving 9 unit loads, and the CARRY OUTPUT (pin D1) is capable of driving 5 unit loads. The STROBE pulse should occur at least 100 ns after the CARRY-IN and the input data have stabilized. DSR outputs should occur 50 ns (maximum) after the module is strobed.

POWER: Power dissipation of the M214 module is 5V at 280 mA (maximum).