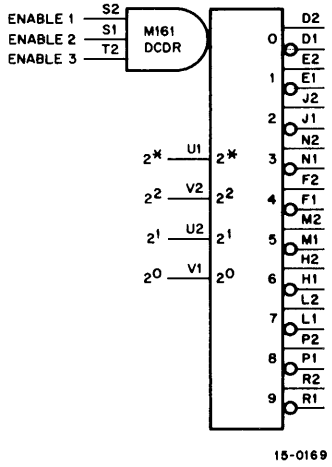
M161
Binary to Octal/Decimal Decoder

The M161 is a functional decoding module that can be used as a binary-to-octal or binary-coded decimal-(8421 or 2421 codes)-to-decimal decoder. In the binary-to-octal configuration, up to eight M161s can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown in DEC's **Digital Logic Handbook**, 1970 edition. The figure assumes that the inputs to the decoder are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.



M161 Simplified Diagram

The propagation delay through the decoder is typically 55 ns in the binary-to-octal mode and 75 ns in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 ns, thereby frequency-limiting this module to 8 MHz when used in this fashion. The ENABLE inputs can be used to strobe output data, if inputs 2° - 2* have settled at least 50 ns prior to the input pulse.

*The 2-bit input may be of decimal value 2, 4, 6, or 8 if illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The following are the input, output, and power characteristics of the M161 module.

INPUTS: The inputs to the M161 are: 2^0 through 2*, 1 unit load each; ENABLE 1 through ENABLE 3, 2 unit loads each.

OUTPUTS: Each positive output is capable of driving 10 unit loads, and each negative output is capable of driving 9 unit loads.

POWER: Power dissipation of the M161 module is 5V at 120 mA (maximum).

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