M104
I/O Bus Multiplexer

The M104 module has been designed specifically for controllers of PDP-15 peripherals. It is used in all controllers that make use of the API or data channel facilities in the I/O processor. It accepts a request from the controller logic at its FLAG (1) H input and synchronizes this request to the I/O SYNC H pulses issued from the I/O processor. These pulses are fed into SYNC of the M104 and immediately set the REQ flip-flop. The REQ flip-flop can be monitored through pins J2 and U2. The I/O processor responds to a request with a GRANT, and ENA is set. This flip-flop is generally used to gate any address information onto the bus; e.g., the API trap address or the word count address of the multicycle data break. The next SYNC pulse sets ENB.

The REQ flag can be reset through pin F2 (CLR RQ) by the controller logic. Pin N1 should be tied to power clear or its equivalent.

The Enabling level ENABLE IN holds REQ off if ENABLE IN arrives as a negative level. When REQ is set (if ENABLE IN is positive), ENABLE OUT goes negative; and the next peripheral on the bus receives this level as a negative ENABLE IN. In this way, the M104 establishes priorities among devices on the same API level or among devices that use the data channel. See the timing diagram for additional information.

The following are the input, output, and power characteristics of the M104 module.

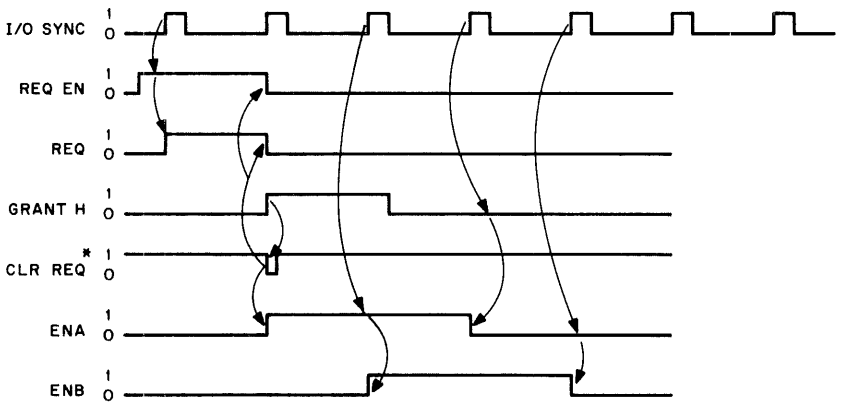
INPUTS: The inputs are standard TTL voltages and have the following input pins and loads:

Input Pin	Load (Units)
H2	2.5
S2	1
H1	6
E2	3
N1	1
F2	1-1/4
K2	68Ω Termination
S2	1

OUTPUTS: The output gates can drive as follows:

Output Pin	Number of Loads Pin Can Drive
U2	5
J2	8
P1	9
S1	10
E1	10
F1	10
M2	PDP-15 I/O Bus Compatible (30 units)
J1	7

POWER: The power dissipation of the M104 module is 1W at 5V.



M104 Timing Diagram