MAINDEC-11-D2QA-PB NEW NUMBER = DZQKA

T15 Instruction Exerciser

ABSTRACT =

This program is designed to be a comprehensive check of all 11 family processor instructions. The program executed each instruction in all address modes and includes tests for traps and the teletype interrupt sequence. The program relocates the test code throughout memory 0-28K.

REQUIREMENTS =

PDP-11 family central processor
Optional = KL11-L (line clock)

STORAGE = Program uses all the first 4K of memory (excluding that area of memory reserved for the loaders.)

LOADING = Absolute Loader

EXECUTION TIME = For 4K = 1 min. For 28K = 5 min.

STARTING PROCEDURE = 200

PRINTOUTS = Yes

SWITCH REGISTER OPTIONS = Yes

SW15 = ,,,, HALT ON ERROR
SW14 = ,,,, LOOP SUBTEST
SW13 = ,,,, INHIBIT ERROR PRINTOUT
SW12 = ,,,, INHIBIT TRACE TRAPPING
SW11 = ,,,, INHIBIT SUBTEST ITERATION
SW10 = ,,,, RING BELL ON ERROR
SW 8 = ,,,, LOAD PDP-11/45 MICRO BREAK REGISTER
SW 7-0 = ,,,, WHEN SET LOADS THE MICRO BREAK REGISTER WITH THE VALUE SET INTO SW7-0 AT THE BEGINNING OF EACH SUBTEST, WITH THE VALUE SET INTO SW7-0 AT THE BEGINNING OF EACH SUBTEST.

NOTE

WHEN ALL SWITCHES ARE DOWN NO TYPEOUTS WILL OCCUR AT THE END OF A PASS (errors will be typed), SETTING SW7 WILL CAUSE END OF PASS MESSAGE TO BE TYPED.