LOGIC SYMBOLOGY MANUAL

DOCUMENT IDENTIFIER: A-MN-ELSM056-00-0 Rev D, 04-Apr-1989

ABSTRACT: This manual is a compilation of internal and external standards for symbology used in engineering documentation.

APPLICABILITY: Mandatory for all organizations within Digital that develop engineering documentation.

STATUS: APPROVED 04-Apr-1989; see EL-INDEX-00 for expiration date.

This manual is not to be supplied to customers, although specific documents can be provided to qualified vendors with appropriate Non-Disclosure agreement.

TITLE: LOGIC SYMBOLOGY MANUAL

DOCUMENT IDENTIFIER: A-MN-ELSM056-00-0 Rev D, 04-Apr-1989

REVISION HISTORY:

Rev A,	27-Aug-1985
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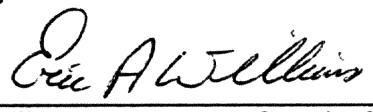
Responsible Department:	Standards and Methods (SMC)
Responsible Person:	Eric Williams

APPROVAL: This manual has been approved for use throughout Digital by the Manager of Standards and Methods Control.



Eric Williams, Manager - Standards and Methods Control

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DATE : 11-APR-1989
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Subject: Updates to A-MN-ELSM056-00-0

Enclosed you will find updates for A-MN-ELSM056-00-0, Logic Symbology Manual. Please update your manual as follows:
Remove the Title Page and Table of Contents and replace with new Revision D.
Also, please:

Remove:	Add:
A-DS-EL00056-01-0 Rev D	This document has been inactivated.
A-DS-EL00056-02-0 Rev D	This document has been inactivated.
A-DS-EL00056-04-0 Rev D	This document has been inactivated.
A-DS-EL00056-06-0 Rev D	This document has been inactivated.
A-DS-EL00056-07-0 Rev D	This document has been inactivated.

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Orig: Georgia Ireland
Phone: 287-3720
Loc.: CTS1-2
Cost Center No.: 3VQ

Sheet: 1 of 2
Date Received: 07-Apr-1989
MS: D4
Final Issue: 07-Apr-1989

Unit(s) to be changed: A-DS-EL-00056-00-0

Prod. Families Affected: N/A

ECO Type Code: 5 Category: Manual FCC Req.: No
F/S Affected: No FCO Req.: No LOU Code: N/A
Where Used: ELSM056

Documentation Affected: A-MN-ELSM056-00-0

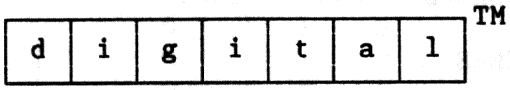
PROBLEM Documents contained in this manual have been updated.

CORRECTION Replace with new updated revisions

BREAK-IN/ EFFECTIVITY Immediately upon release of this ECO

APPROVAL NAMES		C/C	Phone No. DTN-Ext.	Date dd-mmm-yyyy
Standards Process Manager:	Eric A. Williams Eric Williams	396	287-3696	07-Apr-1989
Standards and Methods Supv:	Maureen Bishop-Elffing Maureen Bishop-Elffing	3VQ	287-3725	07-Apr-1989
Coordinator:	Barbara Bowers Barbara Bowers	3VQ	287-3674	07-Apr-1989

Charge Number: 3VQ W.O. No: 192715

EEEEEE CCCC 0000 E C C 0 0 EEEE C 0 0 E C C 0 0 EEEEEE CCCC 0000	ECO No: ELSM056-CTS03  TM ENGINEERING CHANGE ORDER

CONTINUATION SHEET Sheet: 2 of 2

ITEM NO.	PART NUMBER	DOCUMENT NUMBER	OLD REV	NEW REV
1	EL-SM056-00	A-MN-ELSM056-00	C	D

DESCRIPTION: Update the Title Page and Table of Contents per this ECO.

ITEM NO.	PART NUMBER	DOCUMENT NUMBER	OLD REV	NEW REV
2	EL-00056-01-0	A-DS-EL00056-01-0	D	INA

DESCRIPTION:Do not replace any document.

ITEM NO.	PART NUMBER	DOCUMENT NUMBER	OLD REV	NEW REV
3	EL-00056-02-0	A-DS-EL00056-02-0	D	INA

DESCRIPTION:Do not replace any document.

ITEM NO.	PART NUMBER	DOCUMENT NUMBER	OLD REV	NEW REV
4	EL-00056-04-0	A-DS-EL00056-04-0	D	INA

DESCRIPTION:Do not replace any document.

ITEM NO.	PART NUMBER	DOCUMENT NUMBER	OLD REV	NEW REV
5	EL-00056-06-0	A-DS-EL00056-06-0	D	INA

DESCRIPTION:Do not replace any document.

ITEM NO.	PART NUMBER	DOCUMENT NUMBER	OLD REV	NEW REV
6	EL-00056-07-0	A-DS-EL00056-07-0	D	INA

DESCRIPTION:Do not replace any document.

LOGIC SYMBOLOGY MANUAL

DOCUMENT IDENTIFIER: A-MN-ELSM056-00-0 Rev C, 20-Mar-1987

ABSTRACT: This manual is a compilation of internal and external standards for symbology used in engineering documentation.

APPLICABILITY: Mandatory for all organizations within Digital that develop engineering documentation.

STATUS: APPROVED 20-Mar-1987; see EL-INDEX-00 for expiration date.

This manual is not to be supplied to customers, although specific documents can be provided to qualified vendors with appropriate Non-Disclosure Agreements.

digital™ EN-01047-16-REVB(396)

TITLE: LOGIC SYMBOLOGY MANUAL

DOCUMENT IDENTIFIER: A-MN-ELSM056-00-0 Rev C, 20-Mar-1987

REVISION HISTORY: Rev A, 27-Aug-1985
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Document Management Group: Standards and Methods Admin. (TDA)
Responsible Department: Standards and Methods (SMC)
Responsible Person: Joe Kurta

APPROVAL: This manual has been approved for use throughout Digital by the Manager of Standards and Methods Control.

Joseph M Kurta

Joe Kurta, Manager - Standards and Methods Control

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Table of Contents/Revision Status

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DEC STD 056-0 SYMBOLOGY - CIRCUIT SCHEMATIC REQUIREMENTS

DOCUMENT IDENTIFIER: A-DS-EL00056-00-0 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 defines the requirements for graphic symbols to be used on circuit schematics in the Engineering Documentation System for use by Manufacturing, Field Service and customers. The standard also describes circuit schematic labeling and interconnection requirements.

APPLICABILITY: This section is mandatory for anyone involved in the use and/or design of circuit schematics. This section describes symbols to be used universally so that symbology can be interpreted consistently and correctly. Each integrated circuit that is either brought into or designed by Digital shall have a schematic symbol for the users of the integrated circuit included in the purchase specification.

STATUS: APPROVED 15-Jan-1985; see EL-INDEX-00 for expiration date.

FOR INTERNAL USE ONLY

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TITLE: DEC STD 056-0 SYMBOLOGY - CIRCUIT SCHEMATIC REQUIREMENTS

DOCUMENT IDENTIFIER: A-DS-EL00056-00-0 Rev D, 15-Jan-1985

REVISION HISTORY: Rev C 29-Sep-1980
Rev D 15-Jan-1985 ECO #AP001

Document Management Group: Engineering Design/Documentation Methods (TDD)
Responsible Department: ADS Comittee (list of current members can be obtained from Standards and Methods Control)
Responsible Individual: Thomas Smith

APPROVAL:

Secretary, Engineering Committee

Direct requests for further information to:

Tom Smith
APO-1/C3, DTN: 289-1046, NONAME::SMITH

Copies of this document can be ordered from:

Standards and Methods Control,
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

TABLE OF CONTENTS/REVISION STATUS

1 INTRODUCTION

1.1 PURPOSE

This section of DEC STD 056 defines the requirements for graphic symbols to be used on circuit schematics and describes circuit schematic labeling and interconnection requirements. The purpose of standardizing these requirements is to provide accurate and consistent circuit schematics that can be interpreted easily by the users.

1.2 SCOPE

Graphic symbols are used on circuit schematics to represent discrete electronic and electromechanical components, and integrated circuit logic elements. Distinctive shape logic symbols are used to uniquely identify specific logic functions. This standard applies to all these graphic symbols used on circuit schematics producted by Digital.

This section of DEC STD 056 provides the general requirements for circuit schematics. Sections 1 through 5 provide specific requirements for the following:

a. Distinctive shape logic symbols (DEC STD 056-1)

b. Complex (uniform shape) logic symbols (DEC STD 056-2)

c. Discrete electronic and electromechanical component symbols (DEC STD 056-3)

d. Interconnections between graphic symbols (DEC STD 056-4)

e. Industry standard logic symbols and diagrams (DEC STD 056-5)

Also included at the end of this section are the following:

a. A glossary of terms (DEC STD 056-6)

b. Logic function labels (DEC STD 056-7)

c. Pin label definitions (DEC STD 056-7)

Note

This section does not include the graphic symbols for every discrete electrical component and logic element used by Digital.

1.3 RESPONSIBILITIES

1.3.1 Engineering Services Design/Drafting Groups

Design/Drafting groups are responsible for ensuring that circuit schematics use graphic symbols conforming to the requirements of this standard.

1.3.2 Project Engineers and Product Managers

Project engineers and product managers are responsible for ensuring that documentation submitted by a vendor under contract to Digital complies with the requirements of this standard.

1.3.3 Automated Drafting Systems Committee

The Automated Drafting Systems (ADS) Committee is responsible for this standard. The ADS Committee chairman is Allan Kent, LM04/D2, DTN: 279-6726.

2 CIRCUIT SCHEMATICS

A circuit schematic is the basic drawing or set of drawings used to diagnose and service an interconnection of electronic and/or electromechanical elements.

The following general requirements apply to circuit schematics produced by Digital Equipment Corporation.

2.1 LAYOUT

A circuit schematic shall use a layout that follows the circuit signal or transmission path from input to output, source to load, or in order of functional sequence. Circuit schematics shall be as symmetrical as possible, and well spaced. Where possible, the primary signal path shall flow left-to-right, bottom-to-top. Unnecessary crossovers and bends shall be eliminated. However, the clarity of the drawing, shall not be sacrificed for the sake of symmetry or compactness. (See also DEC STD 056-5).

2.2 DRAWING SIZE

A drawing shall consist of one page, or two or more like-sized pages. A circuit schematic may consist of multiple drawings (for example, drawing numbers). In all cases, the original page size shall not exceed 22 by 34 inches (D size) or 594 by 841 mm (A1 size).

See DEC STD 013-1 Standard Engineering Drawing Formats and Forms - General Purpose Drawing Sizes and Formats.

2.3 TITLE BLOCK CODE

All circuit schematic drawings shall have a Title Block Code of "CS", and a title not exceeding 32 characters and spaces.

2.4 LETTERING

Lettering on circuit schematics shall conform to the requirements of DEC STD 182-0 Engineering Documentation Acceptance Criteria and Units of Measurement.

2.5 ABBREVIATIONS

Abbreviations used on circuit schematics shall conform to the requirements of DEC STD 015-0 Abbreviations and Units of Measurement.

Note

Signal names are not abbreviations. They are strings of characters with mnemonic significance (see sections 4 and 5 of this standard).

2.6 NOTES

Notes are recommended for use on circuit schematics to help clarify circuit functioning. Notes may be sample waveforms, truth tables, logic equations, or simple descriptions of operations. They may be placed in the "Notes" area or adjacent to the function described. (See also DEC STD 056-5).

2.7 FUNCTIONAL BLOCKS

When necessary, areas of a circuit schematic may be separated into functional blocks. Functional blocks shall be labeled accordingly. (See also DEC STD 056-5).

2.8 NUMERIC VALUES

Numeric values on circuit schematics shall be indicated, using conventional unit factors, in the numeric form requiring the fewest zeros. (See DEC STD 015-0 Abbreviations and Units of Measurement.)

REFERENCED DOCUMENTS

EL-CLASS DOCUMENTS

EL-00056-01	DEC STD 056-1 Symbology - Distinctive Shape Logic
EL-00056-02	DEC STD 056-2 Symbology - Complex (Uniform Shape) Logic Symbols
EL-00056-03	DEC STD 056-3 Symbology - Discrete Electronic and Electromechanical Component Symbols
EL-00056-04	DEC STD 056-4 Symbology - Electrical Interconnections Between Graphic Symbols
EL-00056-05	DEC STD 056-5 Symbology - Industry Standard Logic Symbols And Diagrams
EL-00056-06	DEC STD 056-6 Symbology - Glossary Of Terms
EL-00013-01	DEC STD 013-1 Standard Engineering Drawing Formats and Forms - General Purpose Drawing Sizes and Formats
EL-00015-00	DEC STD 015-0 Abbreviations and Units of Measurement
EL-00182-00	DEC STD 182-0 Engineering Documentation Acceptance Criteria

Copies of the referenced documents can be obtained from:

Standards And Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

DEC STD 056-1 SYMBOLOGY - DISTINCTIVE SHAPE LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-01-0 Rev INA, 15-Mar-1989

ABSTRACT: This document has been inactivated and replaced by *DEC STD 056-5 Symbology - Industry Standard Logic Symbols and Diagrams.*

STATUS: INACTIVATED 15-Mar-1989.

TITLE: DEC STD 056-1 SYMBOLOGY - DISTINCTIVE SHAPE LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-01-0 Rev INA, 15-Mar-1989

REVISION HISTORY:

Rev A,	29-Mar-1971	
Rev B,	06-Jan-1977	
Rev C,	19-Jun-1980	
Rev D,	15-Jan-1985	ECO# AP001
Rev INA,	15-Mar-1989	ECO# CTS02

CHANGE AUTHORIZED BY:

Eric A Williams

Eric Williams, Standards Process Manager

DEC STD 056-1 SYMBOLOGY - DISTINCTIVE SHAPE LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-01-0 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides detailed requirements for the accurate and consistent use of distinctive shape logic symbols.

APPLICABILITY: This section is mandatory for anyone involved in the use or design of Digital Equipment Corporation circuit schematics. This document describes distinctive shape logic symbols to be used universally so that these symbols can be interpreted consistently and correctly.

STATUS: This section of DEC STD 056 will no longer be applicable for new projects starting July 1, 1985.

FOR INTERNAL USE ONLY

TITLE: DEC STD 056-1 SYMBOLOGY - DISTINCTIVE SHAPE LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-01-0 Rev D, 15-Jan-1985

REVISION HISTORY:

Rev A	29-Mar-1971	
Rev B	06-Jan-1977	
Rev C	19-Jun-1980	
Rev D	15-Jan-1985	ECO# AP001

Document Management Group: Engineering Design/Documentation Methods (TDD)

Responsible Department: ADS Committee (list of current members can be obtained from Standards and Methods Control)

Responsible Individual: Thomas Smith

APPROVAL:

Secretary, Engineering Committee

Direct requests for further information to:

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APO-1/C3, DTN: 289-1046, NONAME::SMITH

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APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

TABLE OF CONTENTS/REVISION STATUS

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1 INTRODUCTION

This section of DEC STD 056 will no longer be applicable for new projects starting July 1, 1985. Until that time, either section 1 or section 5 may be applied.

1.1 PURPOSE

This section of DEC STD 056 provides detailed requirements for the accurate and consistent use of distinctive shape logic symbols on circuit schematics produced by Digital.

1.2 SCOPE

Distinctive shape logic symbols are used to uniquely identify specific logic functions. This section of the standard describes the symbol outlines, labels, and indicators necessary for proper use of distinctive shape logic symbols.

1.3 RESPONSIBILITIES

See DEC STD 056-0 Symbology - Circuit Schematic Requirements, subheads 1.3.1 through 1.3.3.

2 REQUIREMENTS

A distinctive shape logic symbol is a symbol whose form uniquely identifies the logic function it represents. Distinctive shape logic symbols must have a symbol outline, function labels, and physical pin labels. Logical pin labels and special indicators are used as required.

2.1 SYMBOL OUTLINE

The symbol outlines of distinctive shape logic symbols are completely fixed in terms of shape, size, and pin location. The size of the symbols is 3/4 MIL-STD-806B size, which is the size of symbols on the Digital Engineering Template, part number 76-06117. (See Figure 1.) Templates are available from any office supplies stockroom.

The orientation of a symbol is preferred to be 0 degrees as shown on the template with the Digital logo reading correctly at the bottom. When necessary, 90, 180, and 270 degree orientations are acceptable.

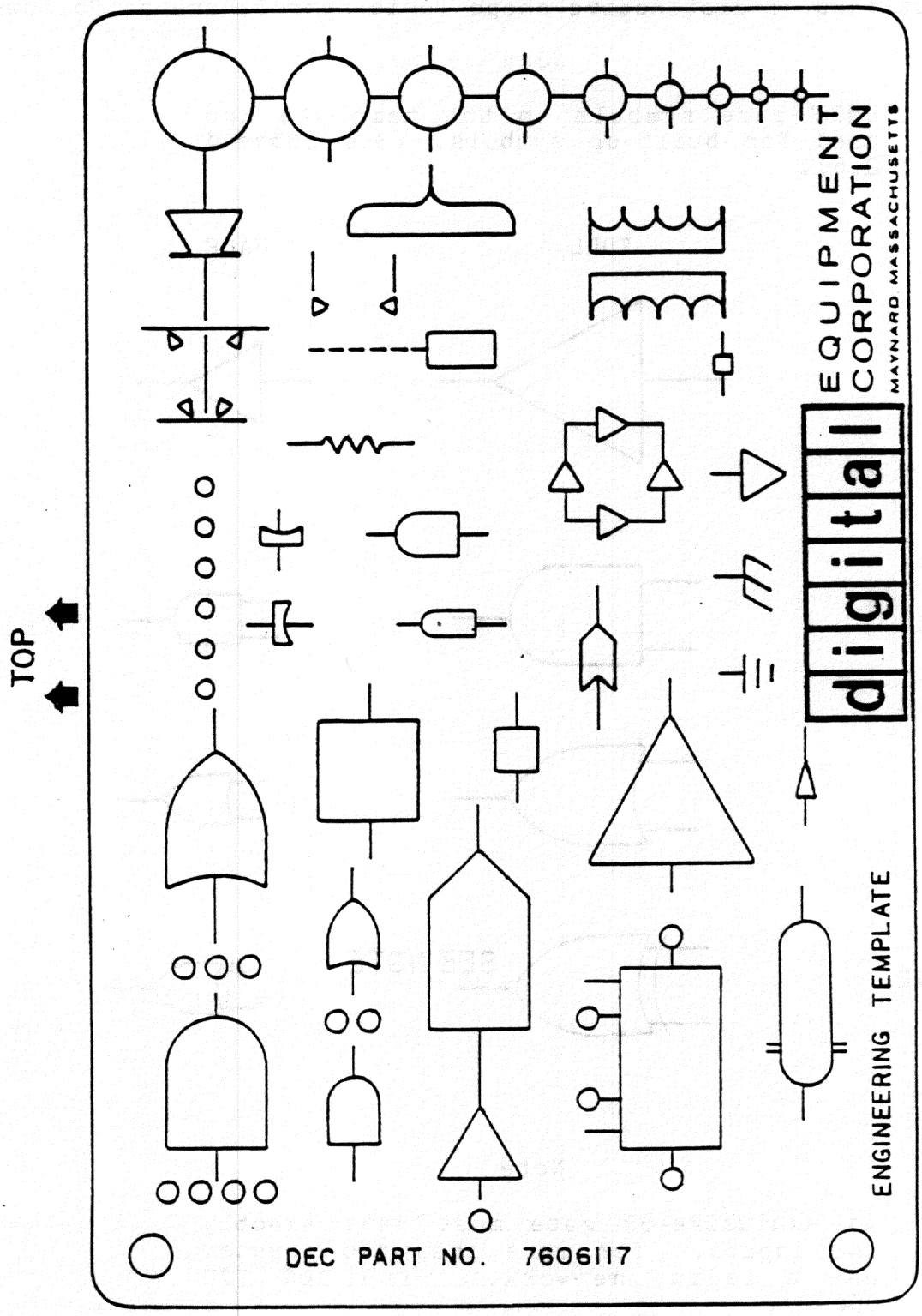
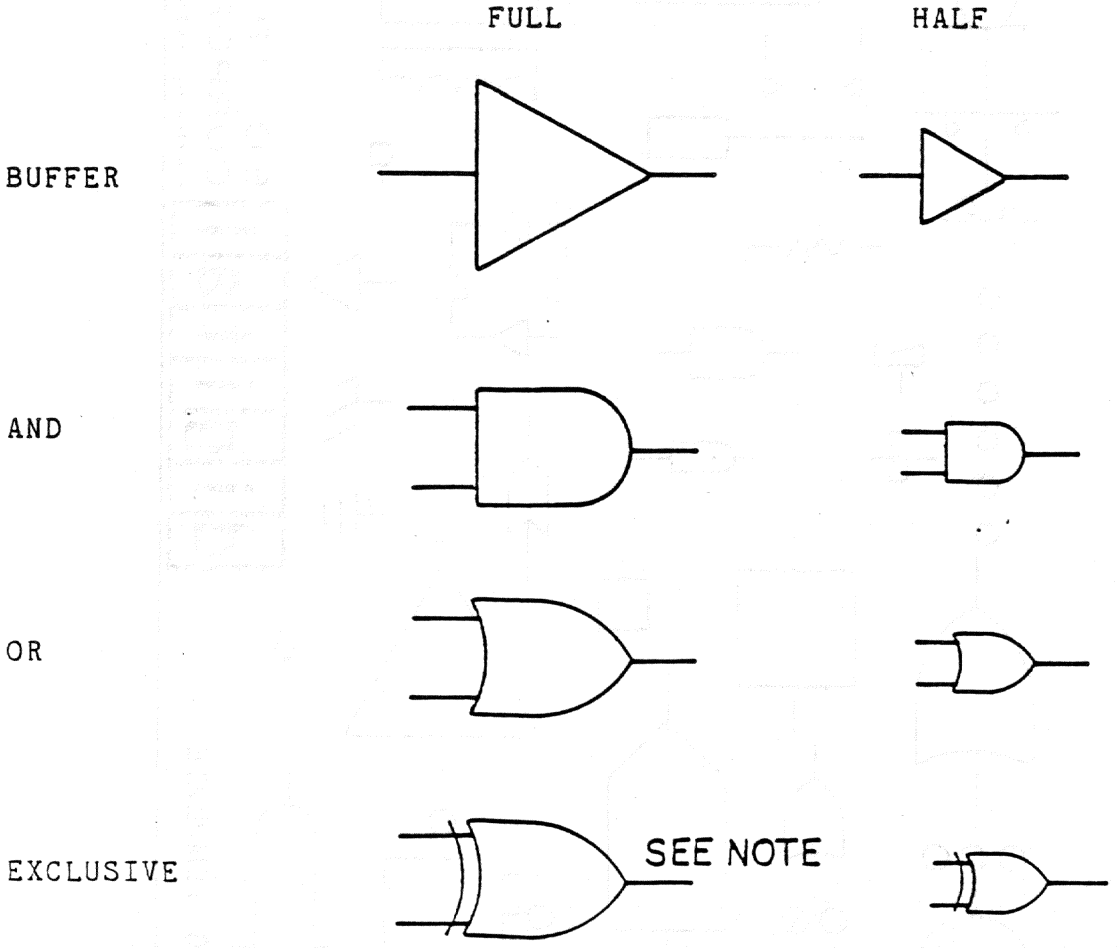


Figure 1. Engineering Template

The basic outlines of distinctive shape logic symbols are as follows.

Note

Half size symbols on the template are used for built-up symbols. (See subhead 2.6).



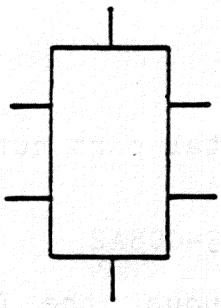
Note

An exclusive-OR gate must have exactly two inputs. For more than two inputs, use a parity network. (See DEC STD 056-2).

FLIP-FLOP

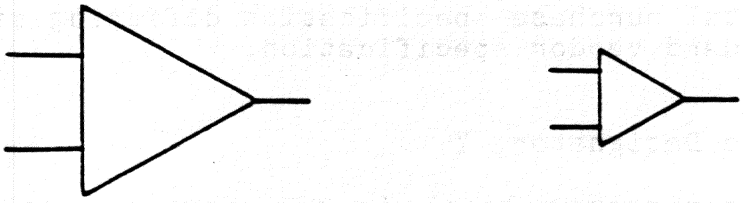
OR

MONOSTABLE

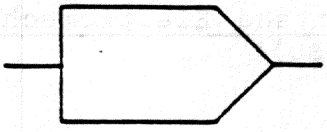


FULL HALF

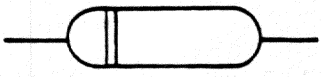
ANALOG AMPLIFIER, COMPARATOR, ETC.



PULSE AMP



DELAY



2.2 FUNCTION LABELS

Three categories of function labels exist for logic symbols. The forms are as follows.

W - Logic function
X - Part type
Y - Reference designator

A part type label and a reference designator are required for every distinctive shape logic symbol. Logic function labels are optional except on flip-flops and monostable multivibrators (one-shots).

2.2.1 Part Type, X

A part type label is the Digital part number or vendor number as shown on the appropriate parts list.

Examples: 7400, 7474, 301, 23-C08A2

If a vendor number is ambiguous, the Digital part number shall be used. Following are examples of ambiguous vendor numbers.

a. PROMS and ROMS having a pattern label.

b. Multiple vendor numbers used for the same part.

c. A Digital purchase specification differing significantly from a standard vendor specification.

2.2.2 Reference Designator, Y

The reference designator label is the physical position designator indicating the location of the part on the module. (See DEC STD 056-3 Symbology - Discrete Electronic and Electromechanical Component Symbols for proper designation formats.)

Example: E21

2.2.3 Logic Function, W

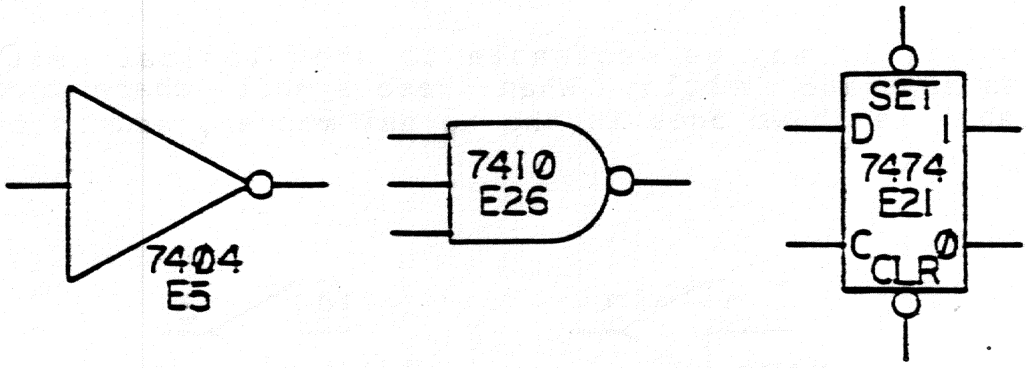
The logic function label is an optional logic function description for distinctive shape logic symbols. When used, the label must conform to the "Label" column of Table 1, DEC STD 056-7 Symbology - Logic Function Labels and Pin Label Definitions.

Example: FF, MONO, COMP

2.2.4 Label Locations

The logic function label must be placed inside the symbol, while the other labels may be placed outside as dictated by legibility.

Examples:



Part type
reference designator

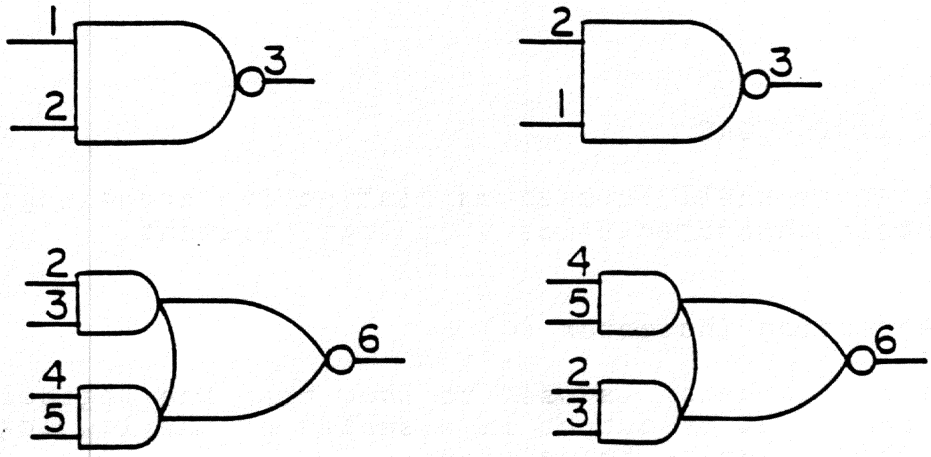
2.3 PHYSICAL PIN LABELS

All pins must be labeled with their physical pin numbers. Physical pin labels are placed adjacent to the pin, outside the symbol outline. Placement of the label above or to the right of the pin is preferred.

It is recommended that all power pins and ground pins, standard or non standard, be listed in tabular form on the circuit schematics. Power pins or ground pins that connect to other components instead of a power bus may be shown.

Pin numbers for logically equivalent inputs may be shown in any order.

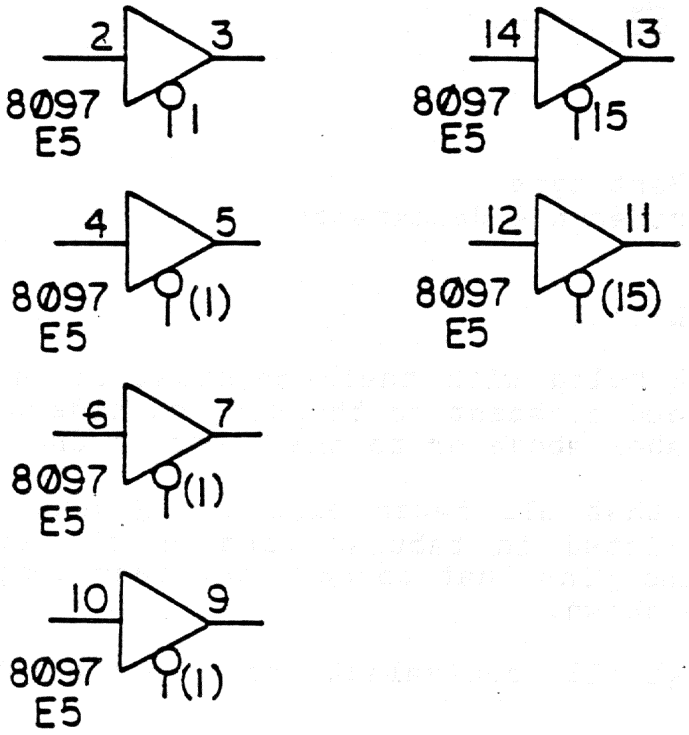
Examples:



2.3.1 Redundant Pin Labels

In some cases, it may be desirable to show logical sections of a function as separate symbols. When these symbols share a common pin, the pin label is shown once in the normal manner, and in parentheses elsewhere.

Examples:



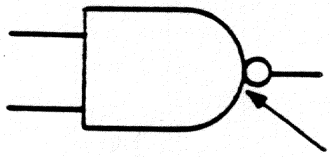
2.4 SPECIAL INDICATORS

Special indicators shall be used on distinctive shape logic symbols to describe certain characteristics of a logic element.

2.4.1 Low Assertion Indicator (0)

A low assertion indicator is used to show that the logical function or variable at the input or output is asserted by the low logic level, or asserted by the low-going transition.

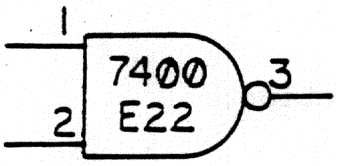
Example:



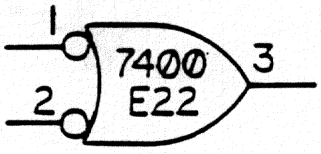
Low Assertion Indicator

2.4.1.1 Multiple representations - because many of these symbols have more than one representation, the correct version must be used to follow the correct logical requirement of the application.

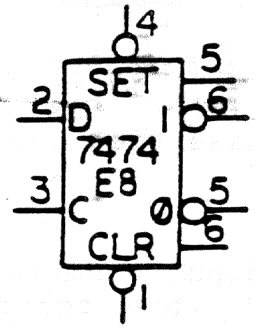
Example: AND, with output asserted when low:



OR, with inputs asserted when low:



FF high data assertion:



FF low data assertion:

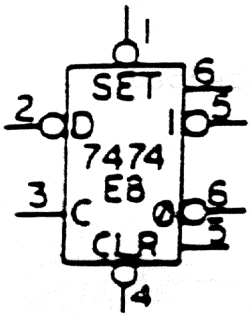
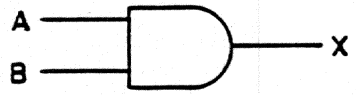
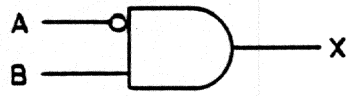
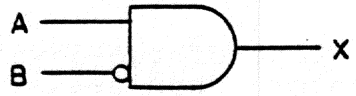
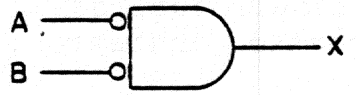
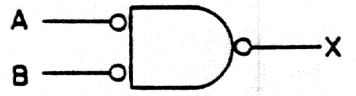
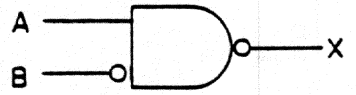
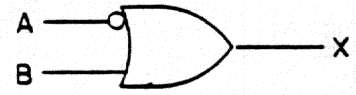
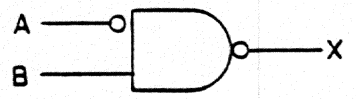
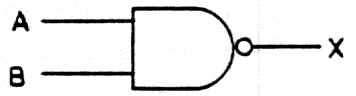


Table 1 shows the applications and functions of two variables and equivalents.

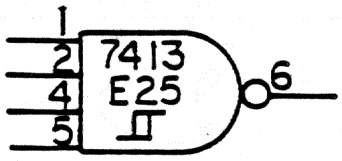
Table 1. AND and OR combinations

AND	OR	A	B	X
		H H L L	H L H L	H L L L
		H H L L	H L H L	L L H L
		H H L L	H L H L	L H L L
		H H L L	H L H L	L L L H
		H H L L	H L H L	H H H L
		H H L L	H L H L	H L H H
		H H L L	H L H L	H H L H
		H H L L	H L H L	L H H H

2.4.2 Hysteresis Input Indicator (⊓)

This symbol indicates that an input is a hysteresis input. It is an optional indicator and is placed at the input pin if associated with only some inputs. It is placed with the function label if it applies to all inputs.

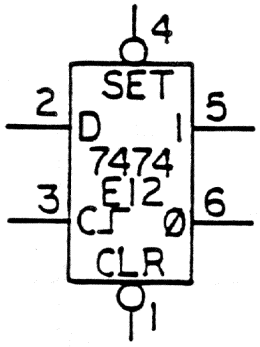
Example:

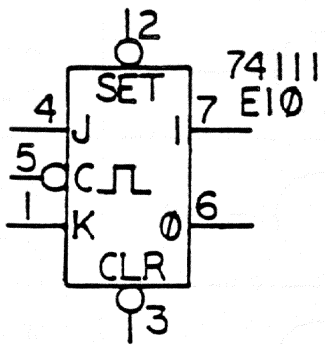


2.4.3 Clock Assertion Indicators

These symbols represent the electrical characteristics of the physical element. The last transition of the indicator represents the completion of the clocking function. Clock assertion indicators are optional and are placed at the input inside the symbol outline. They may supply redundant information with the low assertion indicator.

Examples:





Clock (CLK): ⌐¬

Latch (LCH): ⊓⊔

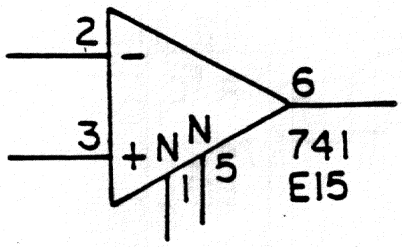
Latch clock (LCK): ⊓⌐

(See DEC STD 056-2 Symbology - Complex (Uniform Shape) Logic Symbols for further definition of clocks.)

2.4.4 Differential Analog Input Indicators (+, -)

These indicators designate the polarity of analog signal inputs. They are placed at the inputs, inside the symbol outline. They are required. When the inputs are in the indicated polarity, they are true.

Example:



2.4.5 Open Collector Output and Tristate Output Indicators

These symbols are allowed but not required, per the design engineer. See DEC STD 056-2, subheads 2.4.1 and 2.4.2.

2.5 LOGICAL PIN LABELS

Logical pin labels are required on flip-flop and monostable symbols to designate pin functions. They are also required on some analog symbols. Logical pin labels are placed inside the symbol outline, adjacent to the appropriate pin.

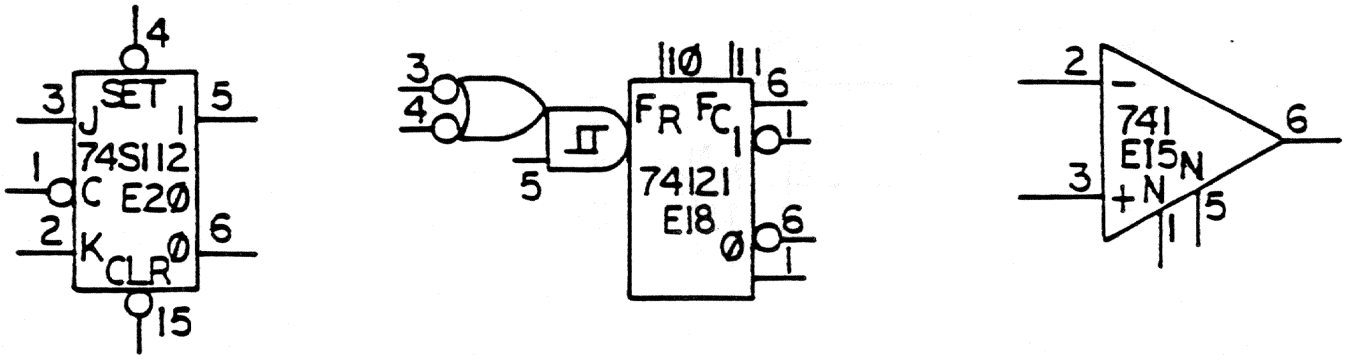
Examples:

C - Clock
J,K - Data inputs in J-K type flip-flop
SET - Set
CLR - Clear
1 - Asserted output when in 1 state
0 - Asserted output when in 0 state

FC - Monostable external capacitor connection
FR - Monostable external resistor connection
N - Analog circuit null or offset control

A complete list of all labels is provided in DEC STD 056-7, Table 7-2.

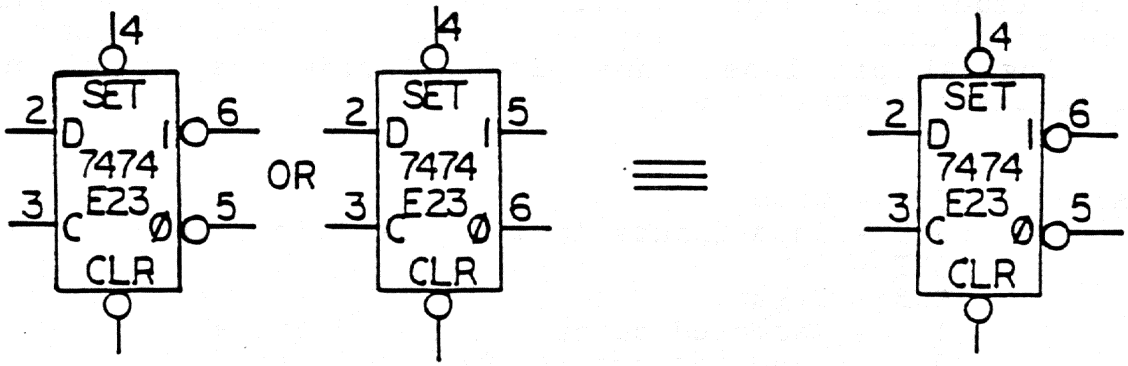
Examples:



2.5.1 Flip-flop/Monostable Symbols

In addition to the required use of logical pin labels on flip-flop and monostable symbols, the outputs of the symbols may be shown in either "2" or "4" output forms.

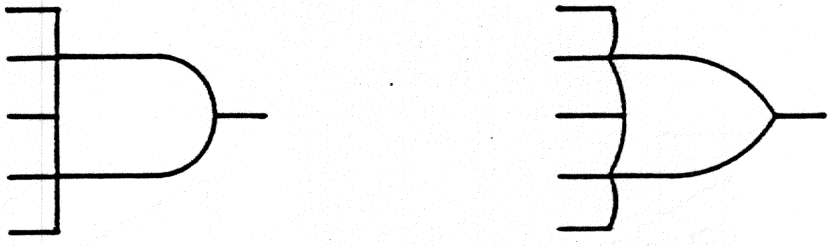
Example:



"2" output forms "4" output form

Flip-flop and monostable symbols may also be built-up. See subhead 2.6.

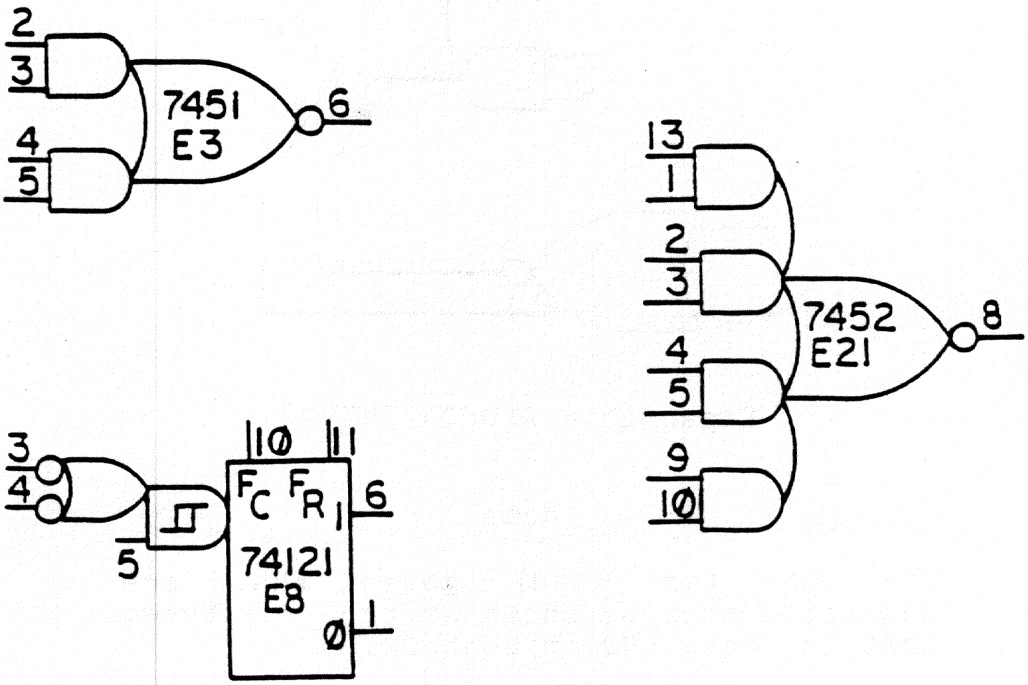
2.5.2 Symbol Input "Wings"



2.6 BUILT-UP SYMBOLS

Some logic functions may be represented by combining distinctive shape logic symbols. These combinations may be used only if the resultant symbol is clear and unambiguous. The symbols combined must be drawn touching, and consist of a full-size basic symbol with half-size attachments.

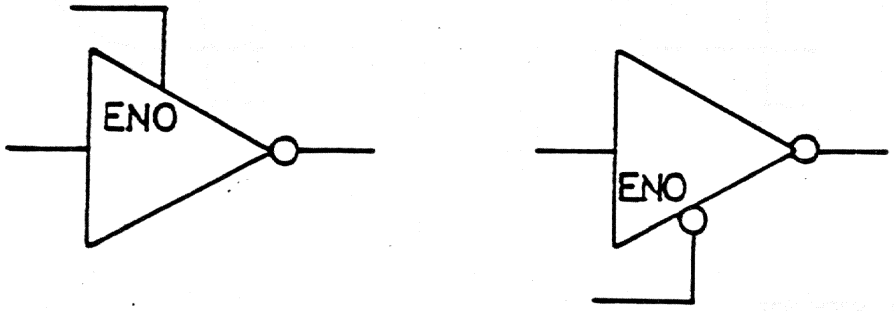
Examples:



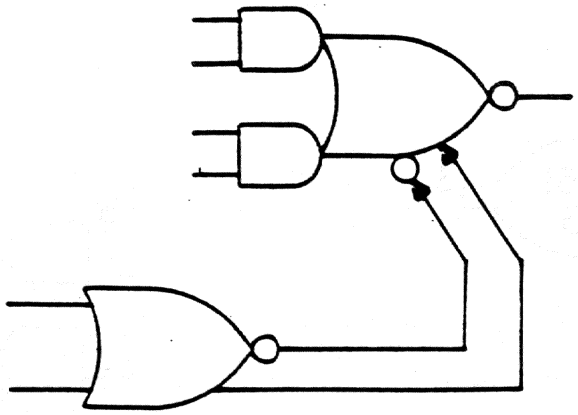
2.7 CONTROL AND EXPANSION INPUTS

Some simple functions, drawn as distinctive shape logic symbols, have control or expansion inputs. These inputs are shown on a different edge of the symbol than the standard logical inputs. Expansion inputs require arrow heads.

Examples:



Inverter with tristate output control



Expandable AND/OR/INVERT

Note

The two (or more) gates that are connected must be shown as the same type, that is, both AND or both OR.

REFERENCED DOCUMENTS

EL-CLASS DOCUMENTS

EL-00056-00	DEC STD 056-0 Symbology - Circuit Schematic Requirements
EL-00056-02	DEC STD 056-2 Symbology - Complex (Uniform Shape) Logic Symbols
EL-00056-03	DEC STD 056-3 Symbology - Discrete Electronic and Electromechanical Component Symbols
EL-00056-07	DEC STD 056-7 Symbology - Logic Function Labels and Pin Label Definitions

Copies of the referenced documents can be obtained from:

Standards and Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

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EN-01047-16-REVB(396)

DEC STD 056-2 SYMBOLOGY - COMPLEX (UNIFORM SHAPE) LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-02 Rev INA, 15-Mar-1989

ABSTRACT: This document has been inactived and replaced by *DEC STD 056-5 Symbology - Industry Standard Logic Symbols and Diagrams.*

STATUS: INACTIVATED 15-Mar-1989.

digital

TITLE: DEC STD 056-2 SYMBOLOGY - COMPLEX (UNIFORM SHAPE) LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-02-0 Rev INA, 15-Mar-1989

REVISION HISTORY:

Rev C,	29-Sep-1980	
Rev D,	15-Jan-1985	ECO# AP002
Rev INA,	15-Mar-1989	ECO# CTS03

CHANGE AUTHORIZED BY:

Eric A Williams

Eric Williams, Standards Process Manager

DEC STD 056-2 SYMBOLOGY - COMPLEX (UNIFORM SHAPE) LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-02-0 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides detailed requirements for the accurate and consistent use of complex, uniform shape logic symbols.

APPLICABILITY: This section is mandatory for anyone involved in the use or design of Digital Equipment Corporation circuit schematics. This document describes complex (uniform shape) logic symbols to be used universally so that these symbols can be interpreted consistently and correctly.

STATUS: This section of DEC STD 056 will no longer be applicable for new projects starting July 1, 1985.

TITLE: DEC STD 056-2 COMPLEX (UNIFORM SHAPE) LOGIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-02 Rev D, 15-Jan-1985

REVISION HISTORY: Rev C 29-Sep-1980
Rev D 15-Jan-1985 ECO #AP002

Document Management Group: Engineering Design/Documentation Methods (TDD)
Responsible Department: ADS Committee (list of current members can be obtained from Standards and Methods Control)
Responsible Indivual: Thomas Smith

APPROVAL:

Secretary, Engineering Committee

Direct requests for further information to:

Thomas Smith
APO-1/C3, DTN: 289-1046, NONAME::SMITH

Copies of this document can be ordered from:

Standards and Methods Control,
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

TABLE OF CONTENTS/REVISION STATUS

1 INTRODUCTION

This section of DEC STD 056 will no longer be applicable for new projects as of 01-Jul-1985. Until that date either this section or section 5 may be applied.

1.1 PURPOSE

This section of DEC STD 056 provides the detailed requirements for the accurate and consistent use of complex (uniform shape) logic symbols on Digital produced circuit schematics.

1.2 SCOPE

A complex (uniform shape) logic symbol is used when a logic function is too intricate to be completely described by the shape of a symbol. This section of this standard describes the symbol outline, labels, and indicators necessary for proper use of uniform shape logic symbols.

1.3 RESPONSIBILITIES

See DEC STD 056-0 Symbology - Circuit Schematic Requirements, subheads 1.3.1 through 1.3.3.

2 REQUIREMENTS

Complex (uniform shape) logic symbols identify logic functions too intricate to be completely described by the shape of a symbol. The symbol outline used is a rectangle. Pertinent functional information is provided by function labels, physical and logical pin labels, and, when applicable, special indicators.

2.1 SYMBOL OUTLINE

The symbol outline of uniform shape logic symbols is a rectangle of sufficient size to legibly contain the required labels. The following rules apply:

a. Detailed logic may be drawn within the symbol as long as minimum symbol content (a rectangle with labels) is preserved.

b. The complete symbol must be detailed at least once on a drawing set, and for other occurences the "minimum" symbol may be used.

c. A particular complex (uniform shape) logic symbol must remain the same size throughout a drawing set.

d. The interior of a symbol may be divided with lines to denote logical sections.

e. Inputs should be on the left and/or bottom edges of a symbol, and outputs on the right and/or top edges.

f. The part type (DEC STD 056-1 Symbology - Distinctive Shape Logic Symbols, subhead 2.2.1), reference designator (DEC STD 056-1, subhead 2.2.2), and logic function (DEC STD 056-1, subhead 2.2.3) shall be at the top of the symbol. The preferred arrangement is logic function on the first line, part type on the next line, and reference designator on the last line.

2.2 FUNCTION LABELS

Because the shape of a uniform shape logic symbol does not describe a logic function, a logic function label is required. The logic function label must conform to the "Label" column of DEC STD 056-7 Symbology - Logic Function Labels and Pin Label Definitions, Table 7-1.

Uniform shape logic symbols must also have a part type label and a reference designator. See DEC STD 056-1, subheads 2.2.1, 2.2.2, and 2.2.4, for requirements.

2.3 PHYSICAL PIN LABELS

See DEC STD 056-1, subhead 2.3.

2.3.1 Redundant Pin Labels

See DEC STD 056-1, subhead 2.3.1.

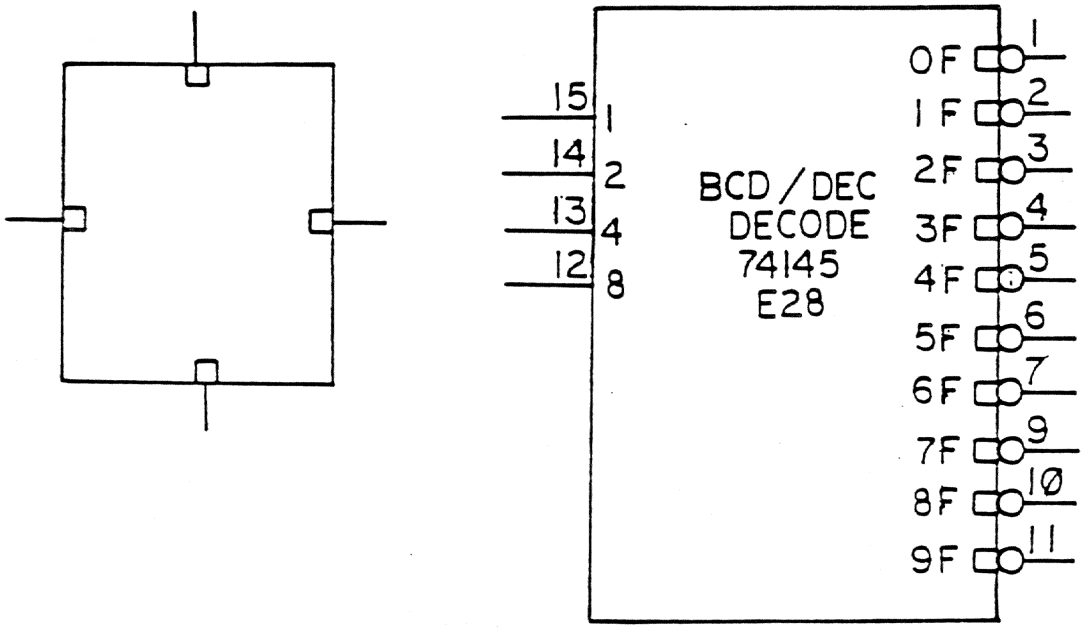
2.4 SPECIAL INDICATORS

Special indicators shall be used on complex (uniform shape) logic symbols to clarify logical functions or describe certain characteristics of a logic element. The low assertion, hysteresis input, clock assertion, and differential analog input indicators described in DEC STD 056-1, subheads 2.4.1 through 2.4.4, shall be used on uniform shape logic symbols. In addition to these indicators, the following indicators may also be used on uniform shape logic symbols.

2.4.1 Open Collector Output Indicator (□)

This symbol indicates an open collector output. It is placed inside the symbol outline, touching at the signal output. The open collector output indicator is optional on hand-drawn schematics.

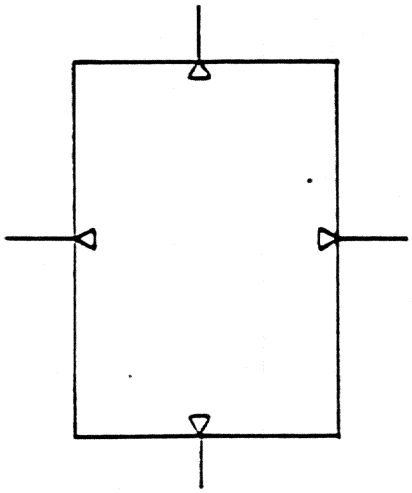
Example:

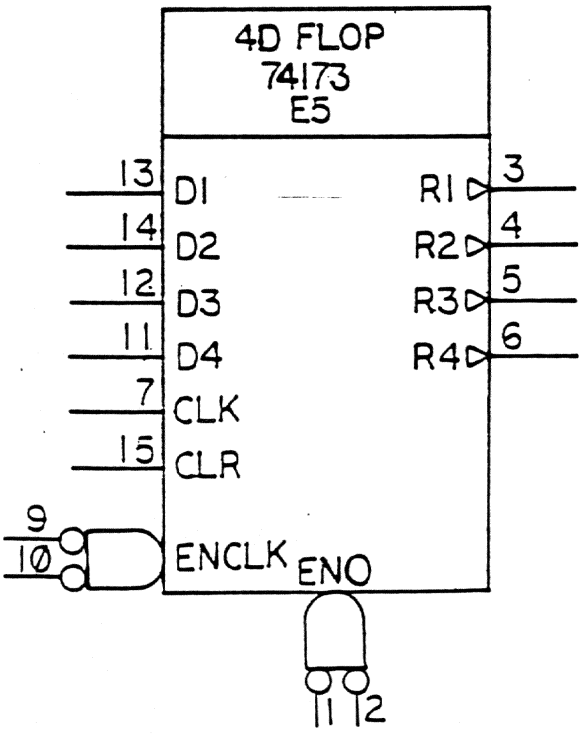


2.4.2 Tristate Output Indicator (▷)

This symbol indicates a tristate output. It is placed inside the symbol outline, touching at the output and pointing outward. This symbol is optional on hand-drawn schematics.

Example:

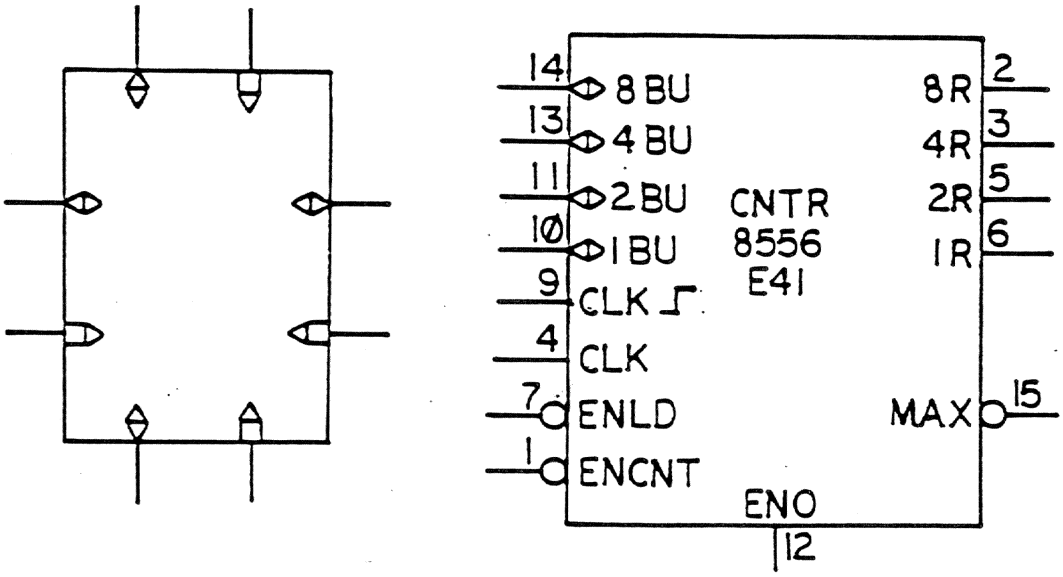




2.4.3 Bidirectional Input/Output Indicator (◁)

This symbol, drawn pointing inward, is used in conjunction with either the open collector or tristate output indicator to show bidirectional input/output pins. The resulting symbols are drawn as follows:

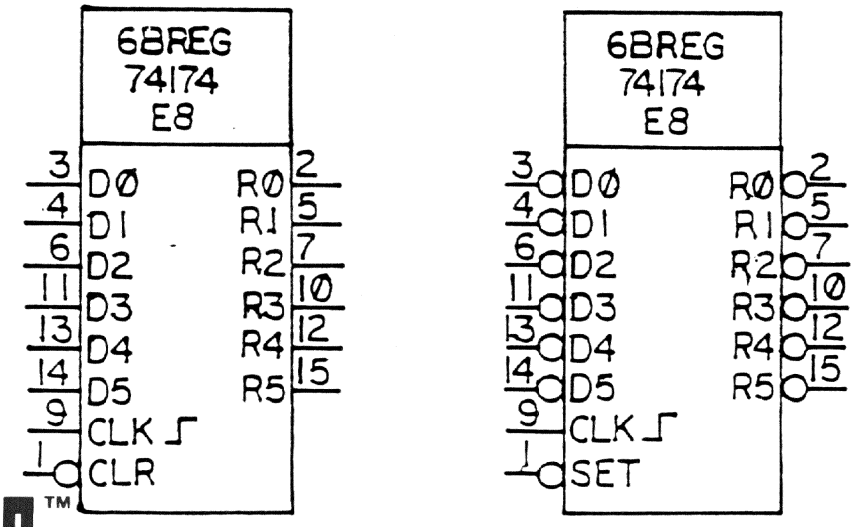
Examples:



2.4.4 Multiple Representations

Because some logic functions have more than one representation, the version to be used should follow the logical requirement of the application. In the case of read-only memory, this may mean that some outputs have low assertion indicators and some do not on the same integrated circuit. Also note that certain signals, like sets and clears, will be interchanged.

Examples:



2.5 LOGICAL PIN LABELS

A logical pin label is required for each input and output pin of a complex (uniform shape) logic symbol. Each label is placed within the symbol outline, adjacent to the pin it describes. The primary purpose of the label is to identify the particular logical function being performed within the context of the overall logic function.

Logical pin labels have the form "WFFFS."

W	-	Weighting factor
FFF	-	Function mnemonic
S	-	Suffix, indicating either pin uniqueness or grouping

The function mnemonic is required. Weighting factors and suffixes are used only as needed.

2.5.1 Function Mnemonics

Function mnemonics are used to describe the functions of pins. They fall into two general categories: general mnemonics and unique mnemonics. Mnemonics must be used as shown in DEC STD 056-07, Table 7-2.

2.5.1.1 General Mnemonics

Clocking Inputs

CLK - Used for general edge triggered clocks. Where multiple clocks exist, it is shortened to CK and followed by a modifying mnemonic such as CKLD (load clock), CKSF (shift clock), CKUP (up clock), and CKDN (down clock).

LCH - Used for level sampling clocks where the outputs follow the inputs during one level, and are latched during the other.

LCK - Latch clock used in master slave configuration. Where master operates in latch mode and slave follows on the trailing edge.

Note

The plotter quality and character set design should be such that LCH and LCK can be easily distinguished.

Initializing Inputs

CLR - Presets (sets) device to the logical zero or minimum state.

LD - Presets (sets) device to a state determined by the D (data) inputs.

SET - Presets (sets) device to the logical one or maximum state.

Data Inputs

D - Used for general data inputs. Where multiple types of data may exist, a modifying mnemonic may be added, such as DX for data to be transmitted.

Enabling Inputs

EN - Used for device enabling inputs. It implies that the device function is valid when EN is asserted and does not define output state when EN is not asserted. Modifying mnemonics may be added for clarity, such as ENCNT (count enable), ENCRY (carry enable), ENX (transmit enable), ENM (memory enable), and ENO (output enable).

Note

"Disable" inputs shall not be used. Instead, use an enable input with the opposite polarity.

Selecting Inputs

S - Used for inputs which select among functions or data paths within a device. They normally will be weighted.

A - Used as a special form of select for address selection on memories.

Register Outputs

R - Register (bistable) output, that is, shift register, counter, and so forth.

M - Memory outputs (special case of R for RAMS and ROMS).

Combinational Logic Outputs

F - Functional output of a combinational logic circuit (that is, non-register or memory) such as multiplexers, decoders, and so on.

Y - Special case of F, where the output is combinational but the function is not obvious from the symbol or its labels.

Miscellaneous But Common Inputs and Outputs

CRY - Designates carries to or from counters, and must be modified CRYI (carry in) and CRYO (carry out).

MAX - Output indicating counters have reached maximum count.

MIN - Output indicating counters have reached minimum count.

BU - Bus transceiver input or output.

SOn - Serial shift register output from stage "n."

SINn - Serial shift register input to stage "n."

ODD EVEN - Parity generator inputs or outputs modified as FODD and FEVEN for outputs, and DODD and DEVEN for inputs.

A<B A=B A>B - Comparative inputs or outputs modified with D for inputs and F for outputs such as: DA<B, DA=B, FA=B, FA>B, and so on.

2.5.1.2 Unique Mnemonics - Some complex symbols have unique functional pins that require special mnemonics.

Examples:
BI - Blanking input for digital displays
RD - Read select
WR - Write select
F(A) - F(G) - Outputs for 7 segment displays
EOC - UART end of character

These mnemonics must be carefully selected to avoid confusion with the general set.

2.5.2 Suffixes

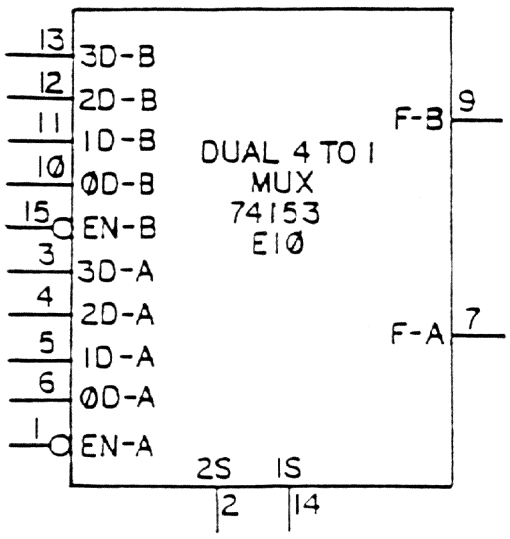
Suffixes are used to indicate uniqueness or grouping of pins.

2.5.2.1 Uniqueness Suffixes - Uniqueness suffixes are used to differentiate between identical functional pins, or to show order when no weighting label is used. See subhead 2.5.3. A uniqueness suffix is always a numeric character.

Examples: See subhead 2.4.4

2.5.2.2 Grouping Suffixes - Pins that act together as a separate function or subfunction of a device may be denoted as such by the use of a grouping suffix. A grouping suffix is always alphabetical, and, if no uniqueness suffix exists, it is separated from the function mnemonic by a "-". Grouping suffix letters need not be sequentially chosen if other letter combinations are of greater mnemonic significance.

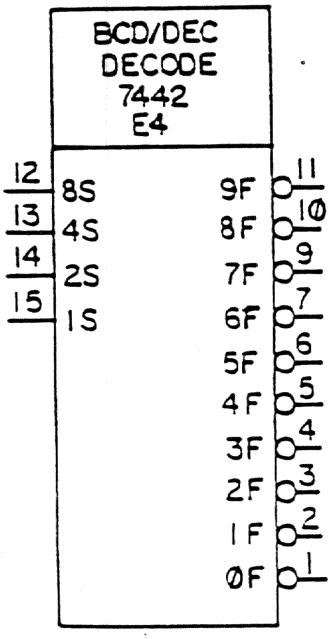
Examples:

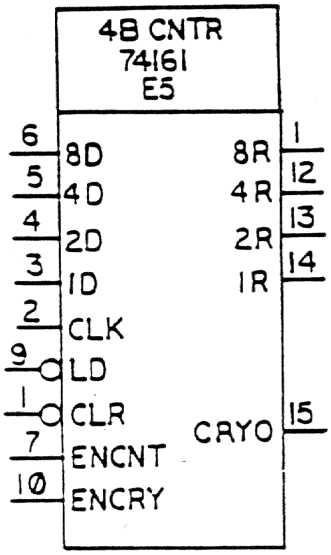


2.5.3 Weighting Factors

If a group of pins has identical function mnemonics and grouping indicators, and there is significance to the ordering of the pins, then each pin must have a weighting factor. For example, input pins on decoders, or output pins on counters have weighted significance in their order and thus require weighting factors in their logical pin labels. Devices such as shift registers, where the stages are ordered but not intrinsically weighted, shall not have weighting factors.

Examples:

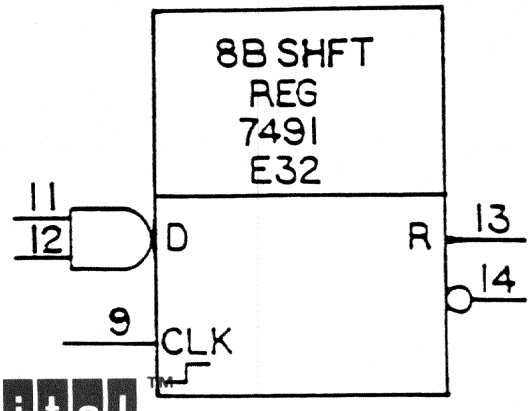


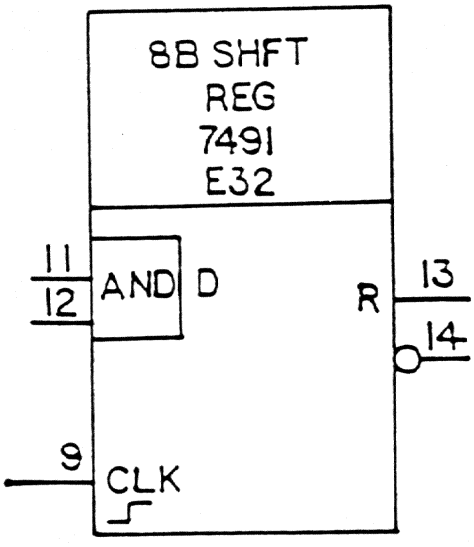


2.6 BUILT-UP SYMBOLS

For some complex (uniform shape) logic symbols, it may be desirable to add half-size distinctive gate shapes to the rectangle to clarify simple gating of inputs. To do this, the gate outline must touch the rectangle outline.

Example:





REFERENCED DOCUMENTS

EL-CLASS DOCUMENTS

EL-00056-00	DEC STD 056-0 Symbology - Circuit Schematic Requirements
EL-00056-01	DEC STD 056-1 Symbology - Distinctive Shape Logic Symbols
EL-00056-07	DEC STD 056-7 Symbology - Logic Function Labels and Pin Label Definitions

Copies of the referenced documents can be obtained from:

Standards and Methods Control
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DEC STD 056-3
SYMBOLOGY - DISCRETE ELECTRONIC AND ELECTROMECHANICAL COMPONENT SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-03 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides detailed requirements for using discrete electronic and electromechanical component symbols on circuit schematics.

APPLICABILITY: This section is mandatory for anyone involved in the use and/or design of circuit schematics. This section describe discrete electronic and electromechanical component symbols to be used universally so that symbology can be interpreted consistently and correctly.

STATUS: APPROVED 15-Jan-1985; see EL-INDEX-00 for expiration date.

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TITLE: DEC STD 056-3 SYMBOLOGY - DISCRETE ELECTRONIC AND ELECTROMECHANICAL COMPONENT SYMBOLS

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Responsible Individual: Tom Smith

APPROVAL:

Sue Camber

Secretary, Engineering Committee

Direct requests for further information to:

Tom Smith
APO-1/C3, DTN: 289-1046, NONAME::SMITH

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1 INTRODUCTION

1.1 PURPOSE

This section of DEC STD 056 provides the detailed requirements for the accurate and consistent use of discrete electronic and electromechanical component symbols on Digital produced circuit schematics.

1.2 SCOPE

This section of the standard identifies the symbol outlines, reference designators, and descriptive information necessary for the proper use of discrete electronic and electromechanical component symbols.

1.3 RESPONSIBILITIES

See DEC STD 056-0 Symbology - Circuit Schematic Requirements, subheads 1.3.1 through 1.3.3.

2 REQUIREMENTS

A discrete electronic or electromechanical component symbol consists of a unique symbol outline and a label. The label contains a reference designator and, as necessary, descriptive information. Discrete component labels should be placed above or to the right of their respective symbols.

2.1 REFERENCE DESIGNATORS

Discrete component reference designators consist of up to six alphanumeric characters. All alphabetic characters must precede all numeric characters, and no special characters are allowed.

The maximum number of characters equals six minus the number of digits in the pin count. For example: up to six characters may be used if a component has no pins; up to five characters may be used if a component has between one and nine pins.

Single in line packages (SIPs), dual in line packages (DIPs), quad in line packages, and packages with pins around four edges have a reference designator of "E." All other components should carry their appropriate reference designators as defined in this standard. Miscellaneous integrated circuits not in the packages described above are labeled "Z."

2.2 DESCRIPTION

The description portion of a discrete component symbol label is used for some components. It usually describes the value or characteristic of component.

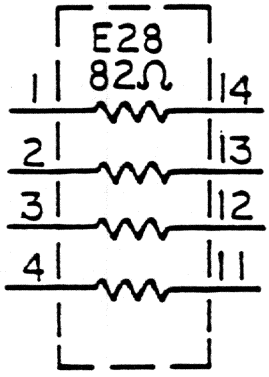
Space must exist between any value and its unit factor.

Example: 10 nF

2.3 PIN NUMBERS

Some components require pin numbers or lead labels to differentiate between connections. All pins or taps that exist must be shown and labeled with the pin numbers or lead labels adjacent to their respective pins.

Examples:



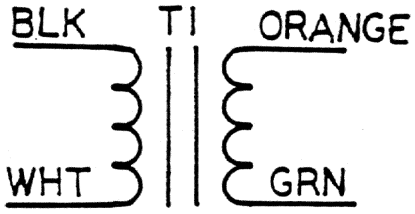


Table 3-1. Discrete Component Symbols and Labeling

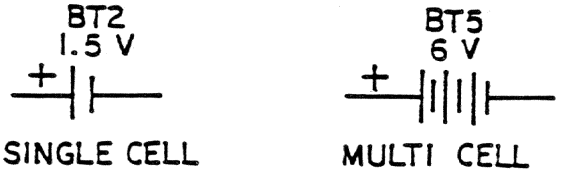
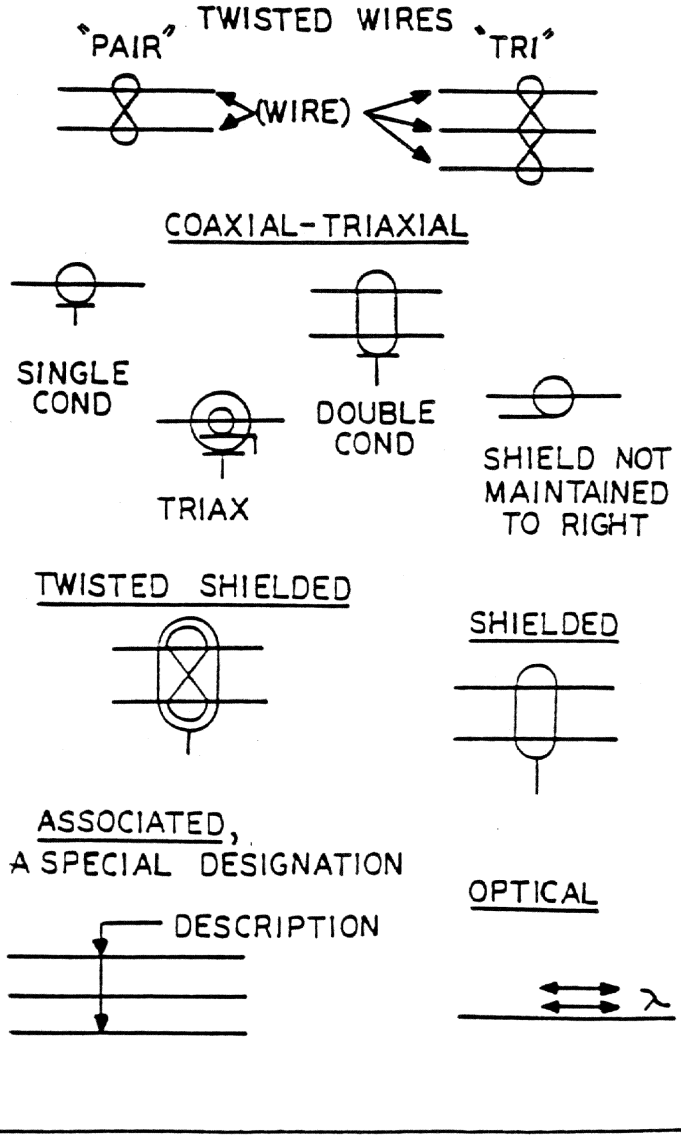
DESCRIPTION	SYMBOL
Battery Reference designator: BT Value in volts (V).	
Cables Reference designator: none Color code, if any; Wire size, if appropriate (AWG, or mm, or other measure); add conductors to basic symbol as required.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

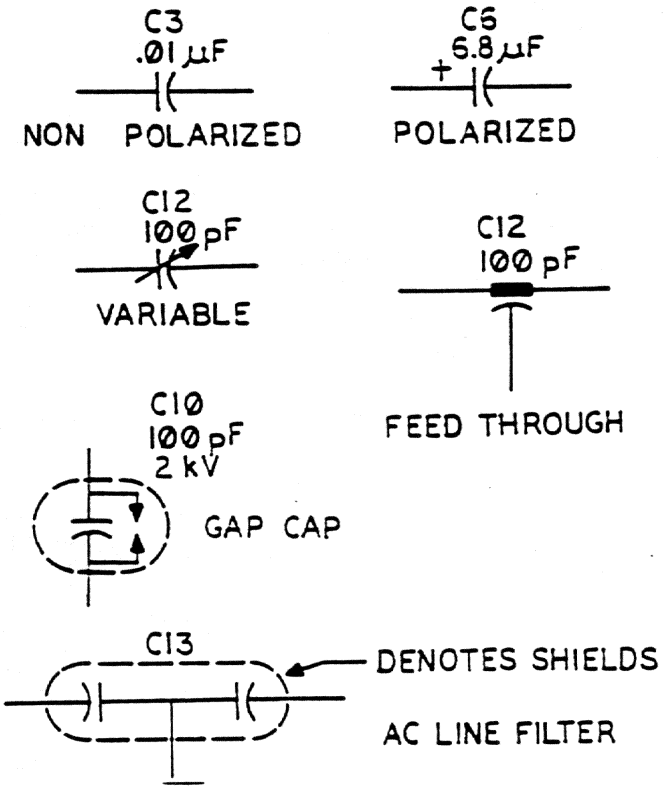
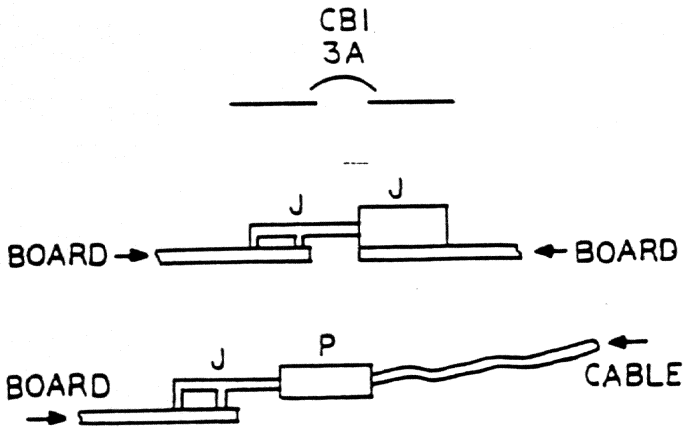
DESCRIPTION	SYMBOL
Capacitor Reference designator: c value in farads (f) with appropriate unit factor. Voltage and tolerance are optional.	
Circuit Breaker Reference designator: CB value in amperes (A) with appropriate unit factor.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

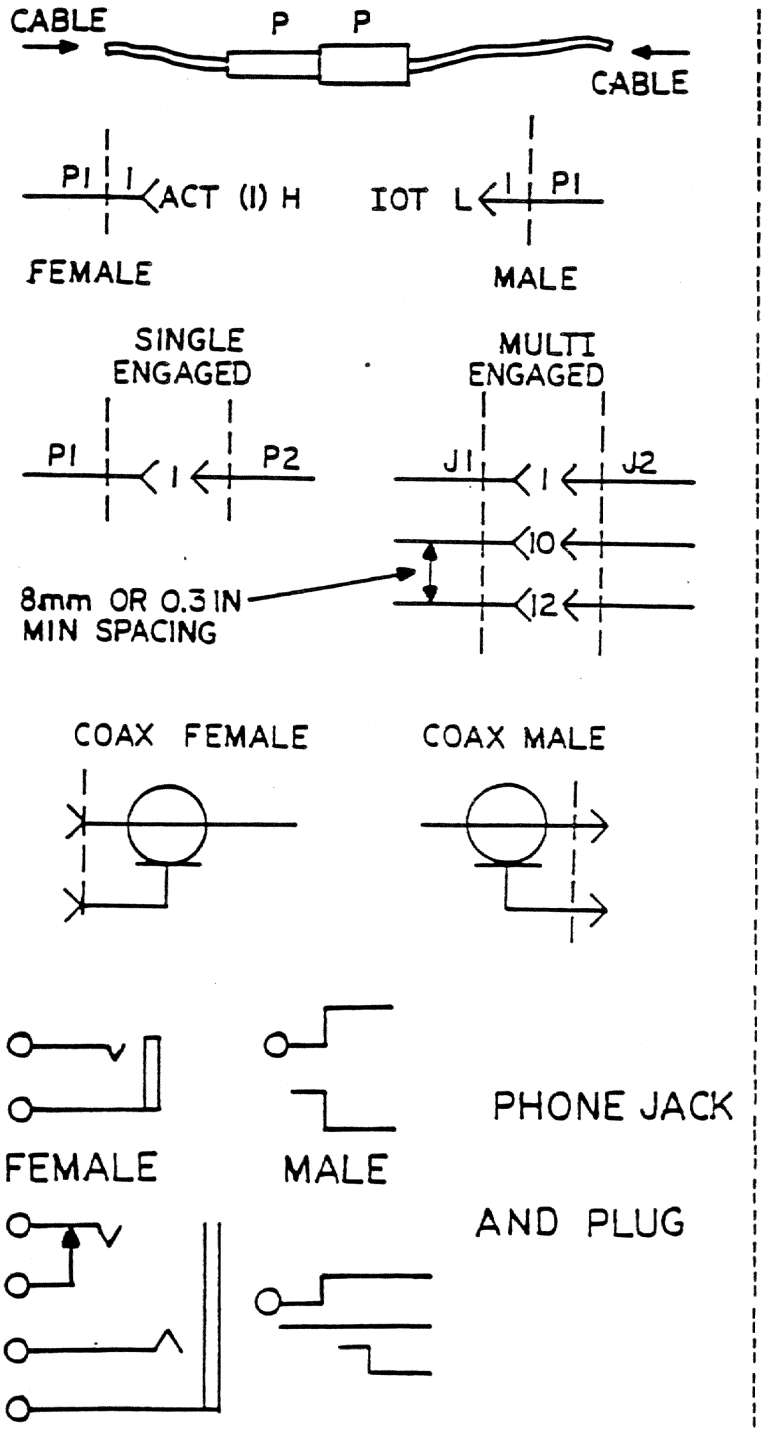
DESCRIPTION	SYMBOL
Connectors and Contacts Reference designators: Connectors are labeled either J (jack) or P (plug); contacts attached directly to a circuit board or sheet metal panel are labeled J (jacks). Connectors attached to the ends of cables are labeled P (plugs). Description is not necessary for connectors and cables, but may be added for clarity.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

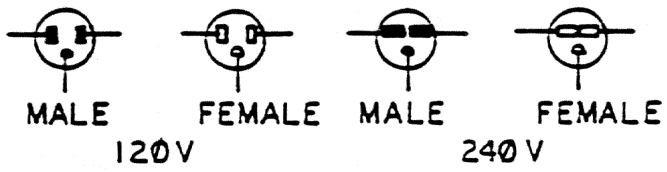
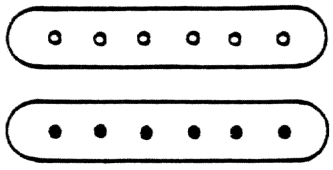
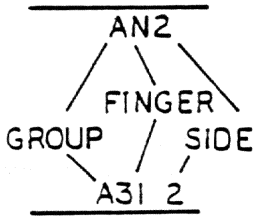
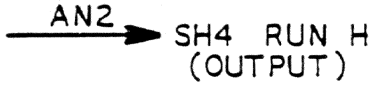
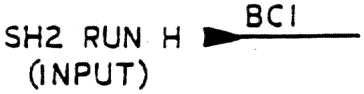
DESCRIPTION	SYMBOL
Line plug and socket symbols should either look similar to the actual plug or socket used, or include a common plug/socket designation together with pin names (see DEC STD 002-0). Note Pin identification is required and keyways should be shown schematically if they exist.	AC LINE PLUG & SOCKET  CABLE CONNECTORS & CONNECTOR BLOCKS  OPEN CIRCLE (FEMALE) CLOSED CIRCLE (MALE)
Module Connector Fingers A special type of connector that does not carry P or J designations, but does carry the pin number and signal name. Arrows are optional, but may be used to emphasize pins. When pin labeling is not specified by DEC STD 030, or physically labeled on the module, then it is suggested that an isometric view of connector and pin labels be shown.	  

Table 3-1. Discrete Component Symbols and Labeling (continued)

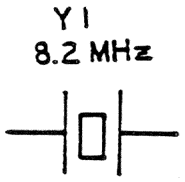
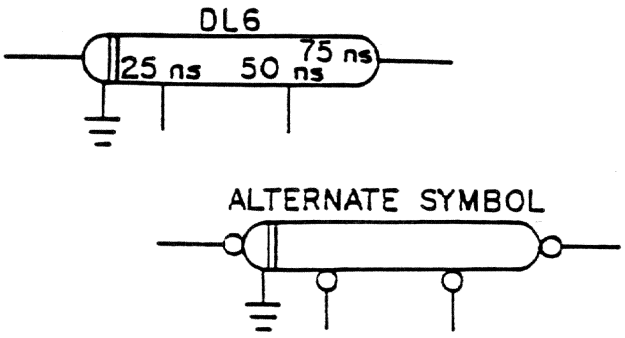
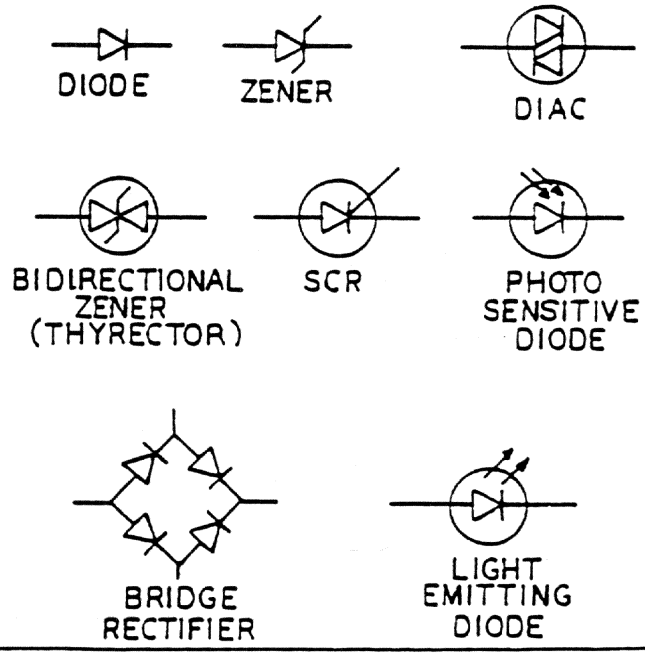
DESCRIPTION	SYMBOL
Crystal Reference designator: Y frequency in hertz (Hz) with an appropriate unit factor.	
Delay Line Reference designator: DL Delay value(s) within symbol with appropriate unit factor. All taps that exist must be shown.	
Diode Reference designator: D if discrete, E if part of a DIP. Component type (for example, 1N5444); for some types of diode, other pertinent information must be added (for example, voltage of zener must be shown).	

Table 3-1. Discrete Component Symbols and Labeling (continued)

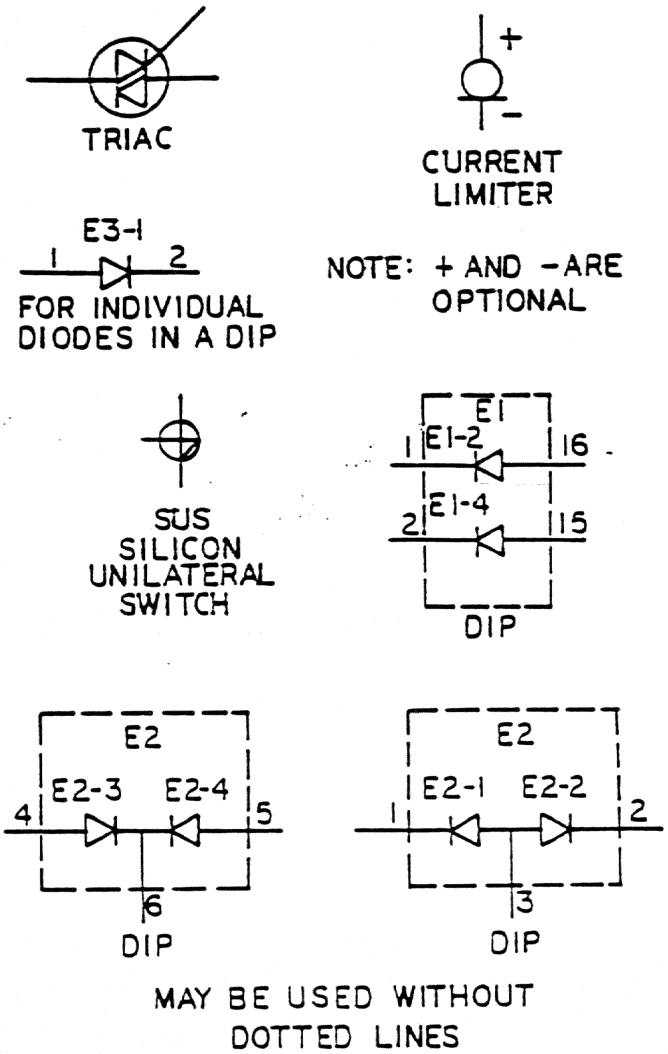
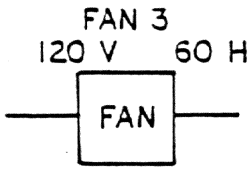
DESCRIPTION	SYMBOL
Diode (continued)	
Fans, Blowers Reference designator: FAN Voltage (V), frequency (Hz), and polarity if appropriate.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

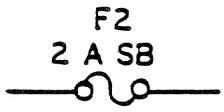
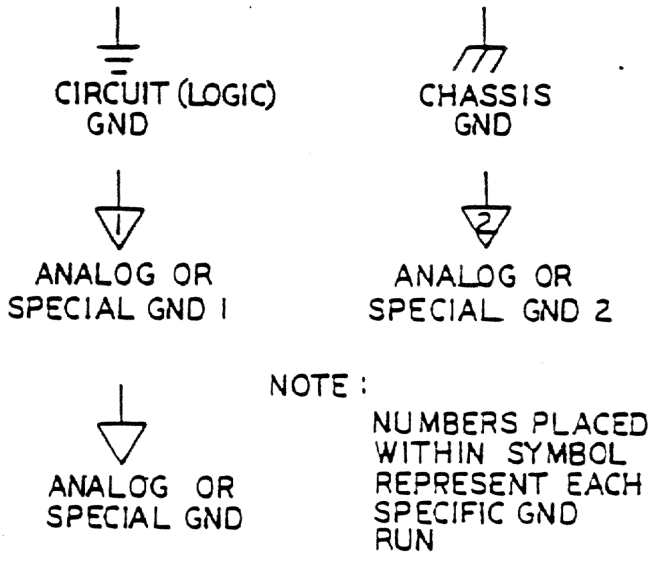
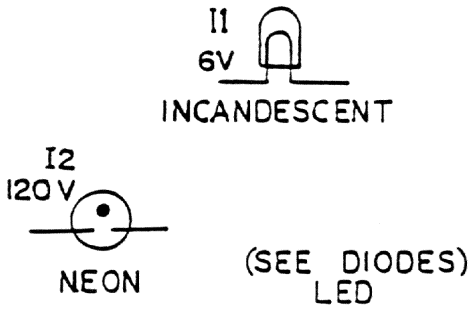
DESCRIPTION	SYMBOL
Fuse Reference designator: F Current value (A) and, if applicable: SB (Slo Blo) FF (Super Fast) F (Fast M (Medium) T (Slow) TT (Super Slow) Add any other information required for the application.	
Ground Reference designator: None Type of ground or specific run indication. Numbers placed within symbol represent each specific ground, run.	
Indicators (Lamps) Reference designator: I Voltage (V) and/or current (I).	

Table 3-1. Discrete Component Symbols and Labeling (continued)

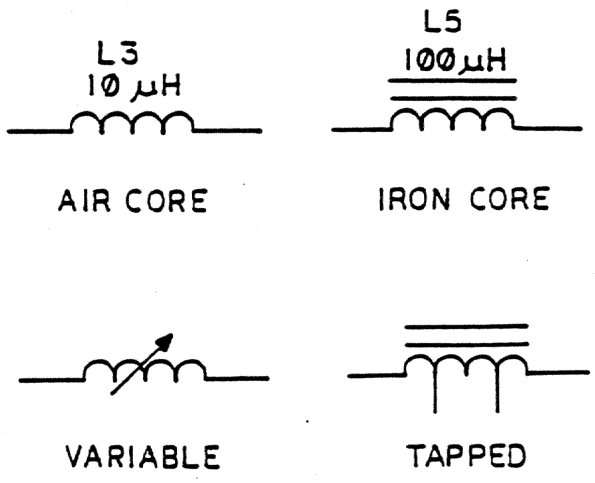
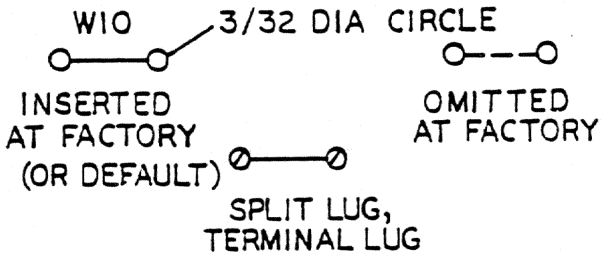
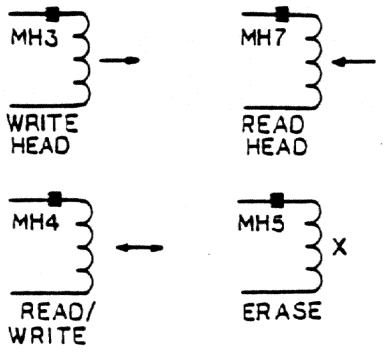
DESCRIPTION	SYMBOL
Inductors Reference designator: L Value in henrys (H) with an appropriate unit factor.	
Jumper Reference designator: W Function jumper performs.	
Magnetic Head, Inductive Pickup Reference designator: MH Inductance; resistance if appropriate; polarity if appropriate.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

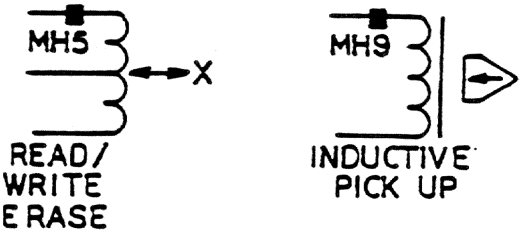
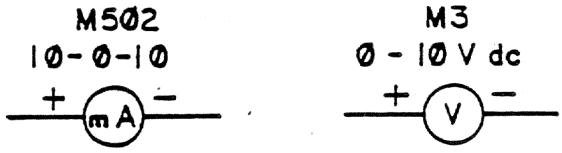
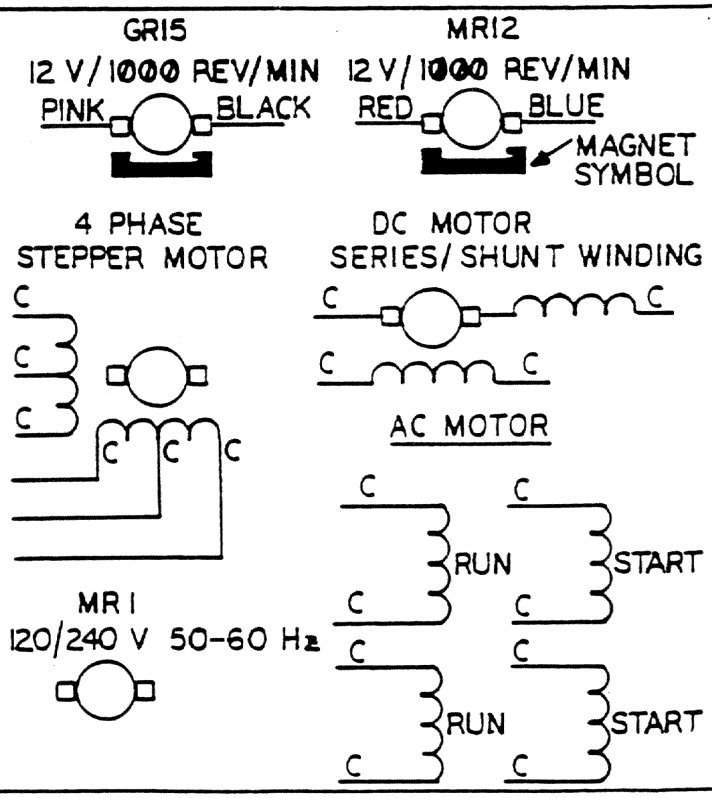
DESCRIPTION	SYMBOL
Magnetic heads (continued)	
Meters Reference designator: M Units measured and placed within symbol or adjacent to symbol.	
Motor, Generator Reference designator: MR, GR Fixed speed; voltage, frequency, variable speed, voltage at speed, (for example, 12 V/1000 rev./min). Multiple windings/taps shown if accessible. Color or other lead designation shown. If appropriate, purpose of windings shown with windings drawn adjacent to the motor symbol.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

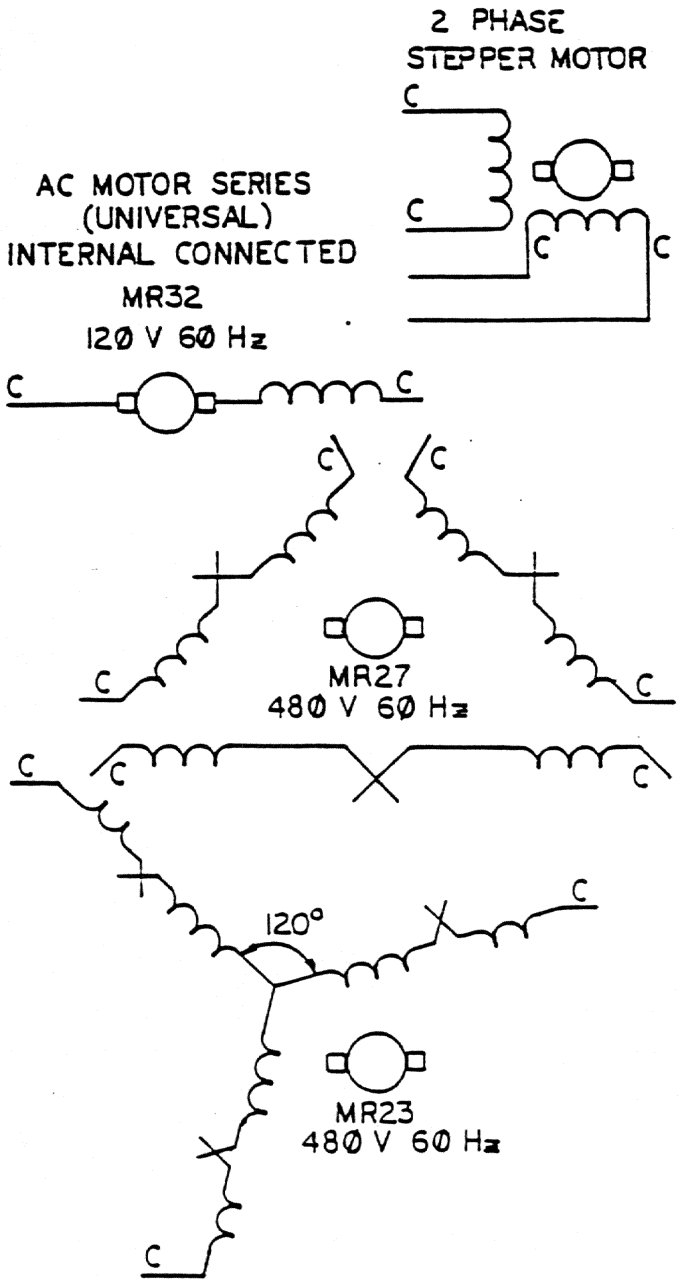
DESCRIPTION	SYMBOL
Motor, Generator (continued)	
Thermal cutout, add to motor windings as appropriate	

Table 3-1. Discrete Component Symbols and Labeling (continued)

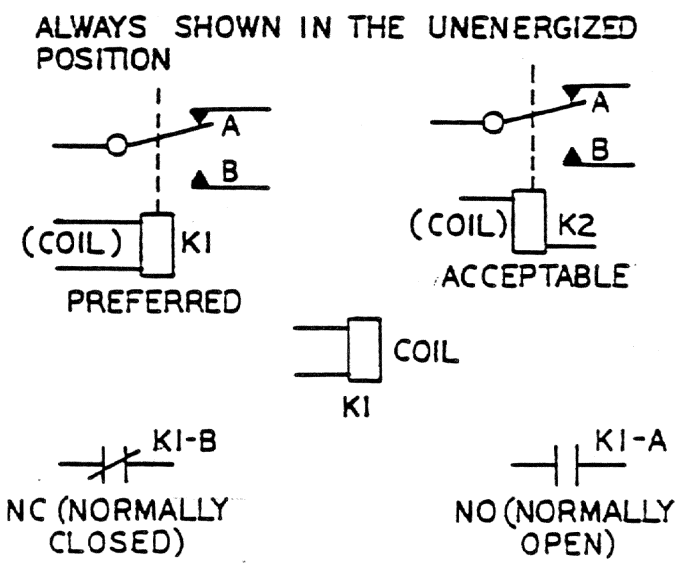
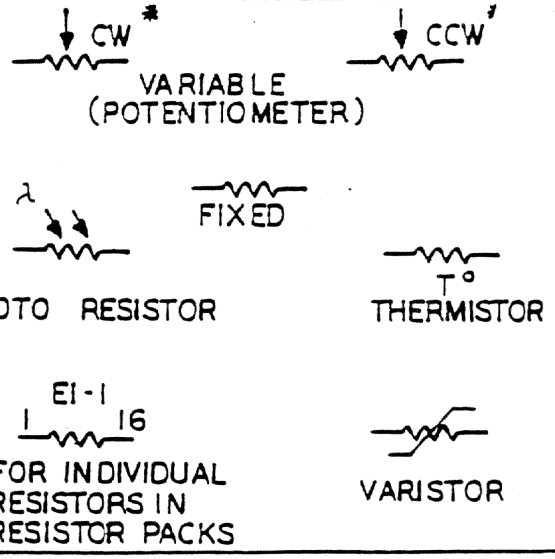
DESCRIPTION	SYMBOL
Relay Reference designator: K Voltage (V), current (I), ac or dc or any other special characteristics.	
Resistor Reference designator: R if discrete, E if part of a DIP. Resistance (Ω), with appropriate unit factor. Power and tolerance are optional. * Viewed from shaft or knob end.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

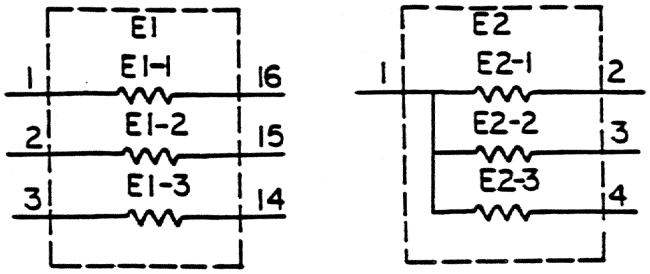
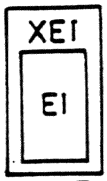
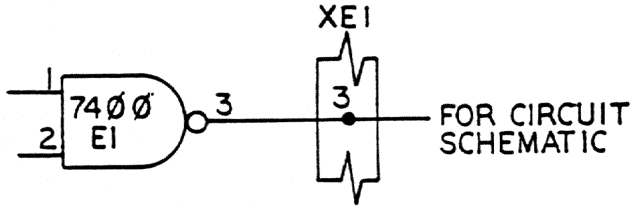
DESCRIPTION	SYMBOL
Resistor (continued)	 RESISTOR PACKS
Socket Reference designator: X Remainder of reference designator is the reference designator of component held in socket. Sockets may be shown on circuit schematics at discretion of the engineer.	 EXAMPLE OF COMPONENT SOCKET SHOWN TOGETHER ON ASSEMBLY DRAWINGS 
Speaker Reference designator: LS Impedance; voltage if appropriate; "Sonalert."	

Table 3-1. Discrete Component Symbols and Labeling (continued)

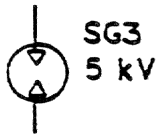
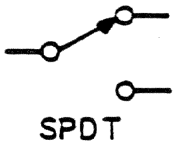
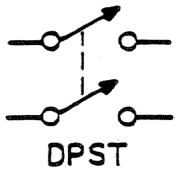
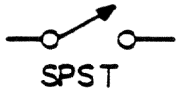
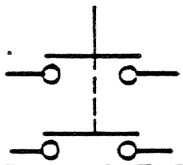
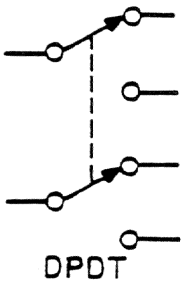
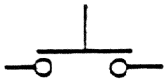
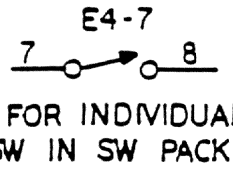
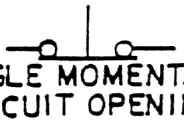
DESCRIPTION	SYMBOL
Spark Gap Reference designator: SG Voltage.	
Switch Reference designator: S, unless contained in a DIP, then E. If required to clarify the function, use the description.	       

Table 3-1. Discrete Component Symbols and Labeling (continued)

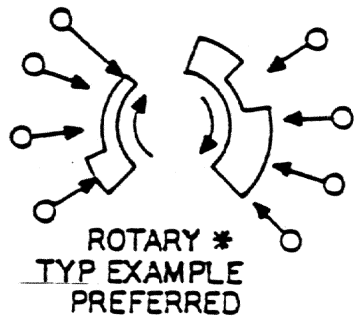
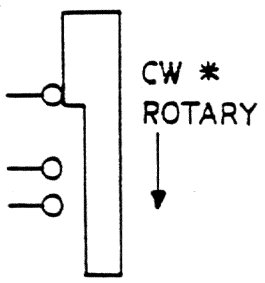
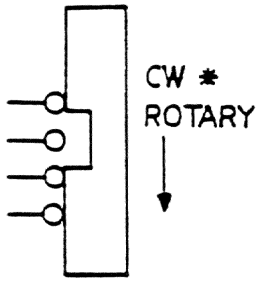
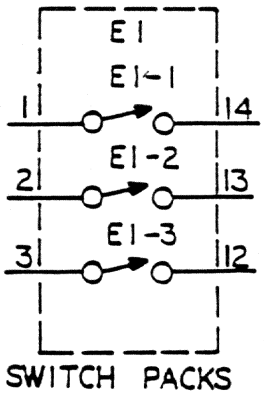
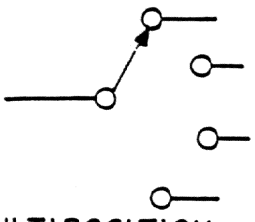
DESCRIPTION	SYMBOL
Switch (continued) * Viewed from the same end as the knob or actuator.	    SWITCH PACKS  MULTIPOSITION STRAIGHT OR ROUND

Table 3-1. Discrete Component Symbols and Labeling (continued)

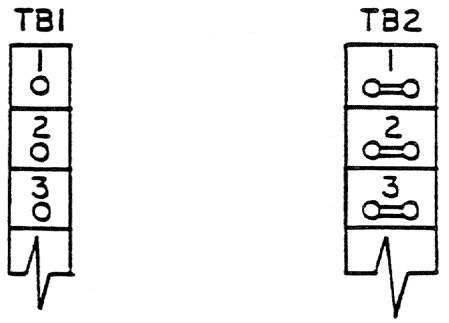
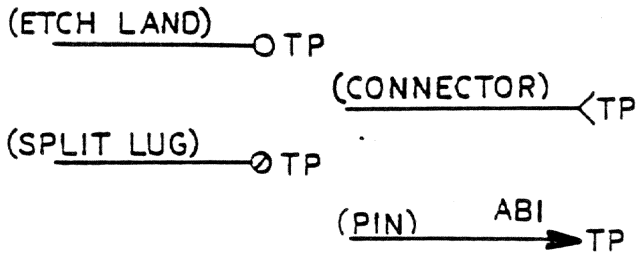
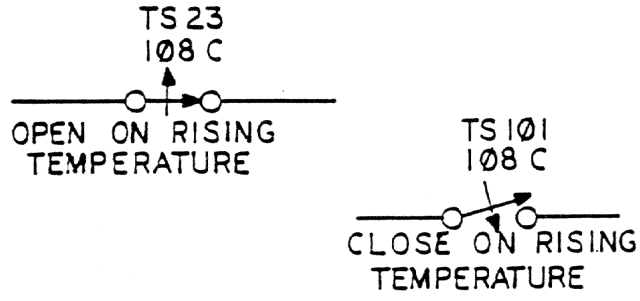
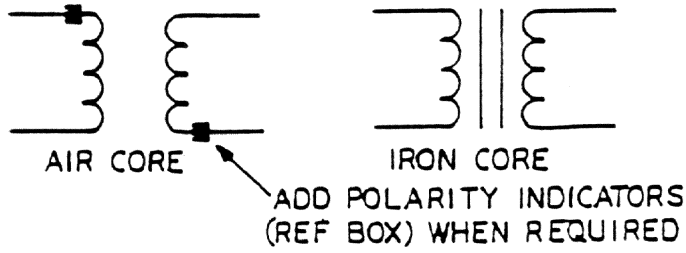
DESCRIPTION	SYMBOL
Thermal Boards and Terminal Strips Reference designator: TB signal or function, if desired. Order of terminals shown on circuit schematic need not be the same as on the physical terminal strip.	
Test Points Reference designator: TP signal or function, if desired.	
Thermostat Reference designator: TS Temperature of actuation; close/open on rising temperature.	
Transformer Reference designator: T Voltage (V), Amperes (A) impedance, frequency, or turns ratio as applicable.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

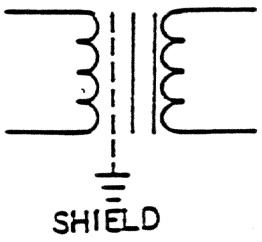
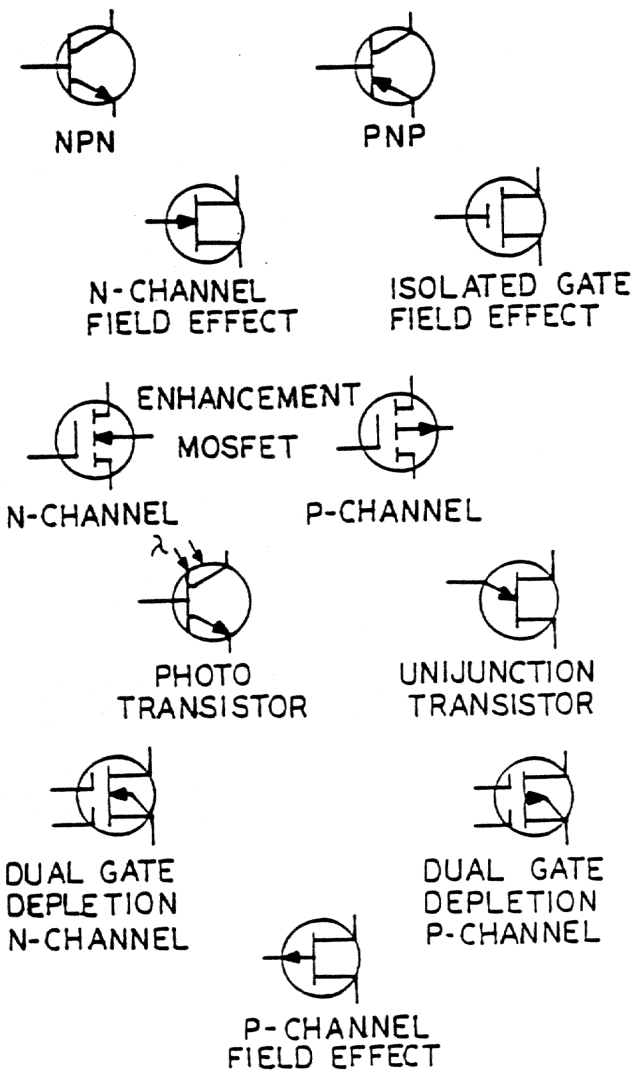
DESCRIPTION	SYMBOL
Transformer (continued)	
Transistor Reference designator: Q, unless part of a DIP, then E. Type number.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

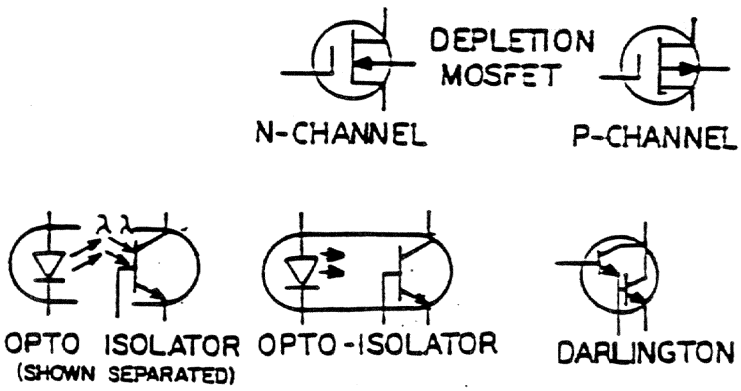
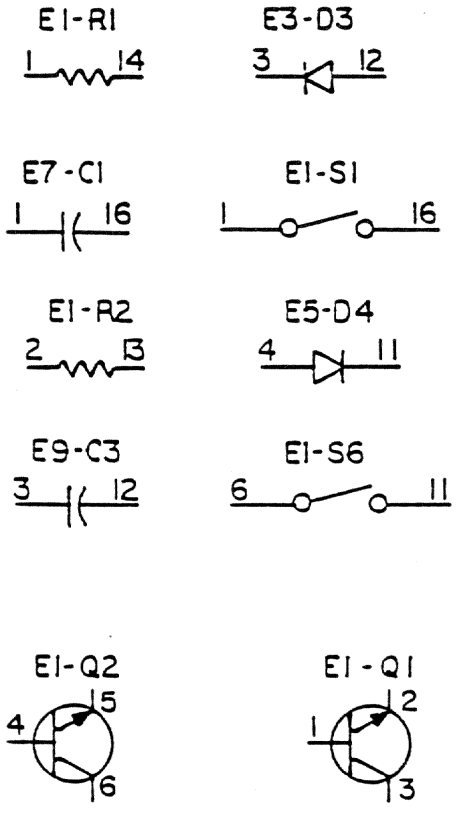
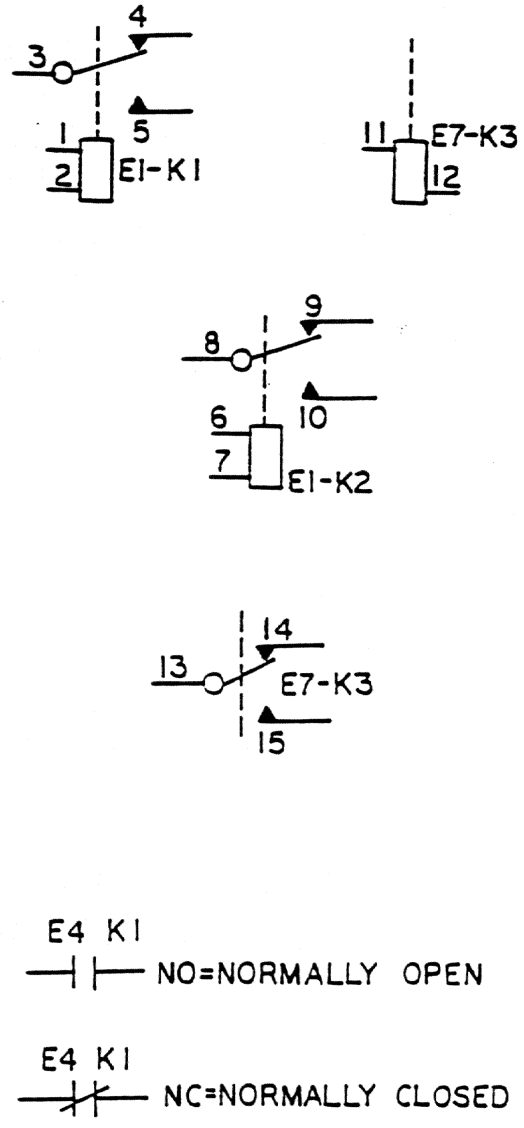
DESCRIPTION	SYMBOL
Transistor (continued)	
Optional Labeling for DIPs Note These optional methods are acceptable for labeling sections of a package on a schematic. Only the inital portion of the label, however, is the true package reference designator used on parts lists and in automated systems.	

Table 3-1. Discrete Component Symbols and Labeling (continued)

DESCRIPTION	SYMBOL
DIPs (continued)	

REFERENCED DOCUMENTS

EL-CLASS DOCUMENTS

EL-00002-00	DEC STD 002-0 AC Power Wiring, Grounding, Receptacle, and Name Plate Requirement
EL-00030-00	DEC STD 030-0 Module Manufacturing Standard
EL-00056-00	DEC STD 056-0 Symbology - Circuit Schematic Requirements
EL-00056-02	DEC STD 056-2 Symbology - Complex (Uniform Shape) Logic Symbols
EL-00056-04	DEC STD 056-4 Symbology - Electrical Interconnections Between Grapic Symbols
EL-00056-05	DEC STD 056-5 Symbology - Industry Standard Logic Symbols and Diagrams
EL-00056-06	DEC STD 056-6 Symbology - Glossary Of Terms
EL-00056-07	DEC STD 056-7 Symbology - Logic Function Labels and Pin Label Definitions

Copies of the referenced documents can be obtained from:

Standards and Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

DEC STD 056-4 SYMBOLOGY - ELECTRICAL INTERCONNECTIONS BETWEEN GRAPHIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-04-0 Rev INA, 15-Mar-1989

ABSTRACT: This document has been inactivated and replaced by *DEC STD 056-5 Symbology - Industry Standard Logic Symbols and Diagrams.*

STATUS: INACTIVATED 15-Mar-1989.

TITLE: DEC STD 056-4 SYMBOLOGY - ELECTRICAL INTERCONNECTIONS BETWEEN GRAPHIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-04-0 Rev INA, 15-Mar-1989

REVISION HISTORY:

Rev A,	18-Feb-1970	
Rev B,	28-Mar-1971	
Rev C,	19-Jun-1980	
Rev D,	15-Jan-1985	ECO# AP002
Rev INA,	15-Mar-1989	ECO# CTS03

CHANGE AUTHORIZED BY:

Eric A Williams

Eric Williams, Standards Process Manager

DEC STD 056-4
SYMBOLOGY - ELECTRICAL INTERCONNECTIONS BETWEEN GRAPHIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-04-0 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides the requirements for representing electrical interconnections between graphic symbols on circuit schematics produced by Digital Equipment Corporation.

APPLICABILITY: This section is mandatory for anyone involved in the use or design of Digital-produced circuit schematics. This section describes electrical interconnections between graphic symbols to be used universally so that symbology can be interpreted consistently and correctly.

STATUS: This section of DEC STD 056 will no longer be applicable for new projects starting 01-Jul-1985.

FOR INTERNAL USE ONLY

TITLE: DEC STD 056-4 SYMBOLOGY - ELECTRICAL INTERCONNECTIONS BETWEEN GRAPHIC SYMBOLS

DOCUMENT IDENTIFIER: A-DS-EL00056-04-0 Rev D, 15-Jan-1985

REVISION HISTORY:

Rev A	18-Feb-1970	
Rev B	28-Mar-1971	
Rev C	19-Jun-1980	
Rev D	15-Jan-1985	ECO #AP002

Document Management Group: Engineering Design/Documentation Methods (TDD)

Responsible Department: ADS Committee (list of current members can be obtained from Standards and Methods Control)

Responsible Individual: Thomas Smith

APPROVED:

Sue Cambier

Secretary, Engineering Committee

Direct requests for further information to:

Thomas Smith
APO-1/C13, DTN: 289-1046, NONAME::SMITH

Copies of this document can be ordered from:

Standards and Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

TABLE OF CONTENTS/REVISION STATUS

List of Table

1 INTRODUCTION

This section will be obsolete for new projects as of July 1, 1985. Until that time, either this section or section 5 may be applied.

1.1 PURPOSE

This section of DEC STD 056 provides the requirements for representing electrical interconnections between graphic symbols on Digital-produced circuit schematics.

1.2 SCOPE

This section includes the requirements for the spacing, grouping, and junctions of connecting lines, and defines proper use of signal names, power signal names, signal busing, and connectors.

1.3 RESPONSIBILITIES

See DEC STD 056-0, subhead 1.3.1 through 1.3.3.

2 REQUIREMENTS

The interconnections of the elements of a circuit may be represented by connecting lines, signal names, signal busing, and connectors. The following requirements apply.

2.1. CONNECTING LINES

Connecting lines on a circuit schematic should be drawn with as few crossovers and bends as possible. Except for components such as diode bridges, connecting lines and the symbols they join should be drawn horizontally and vertically. Long connecting lines between symbols should be avoided.

Connecting lines continued on another page must be terminated with a signal name and resumed with the identical signal name. See subhead 2.2.

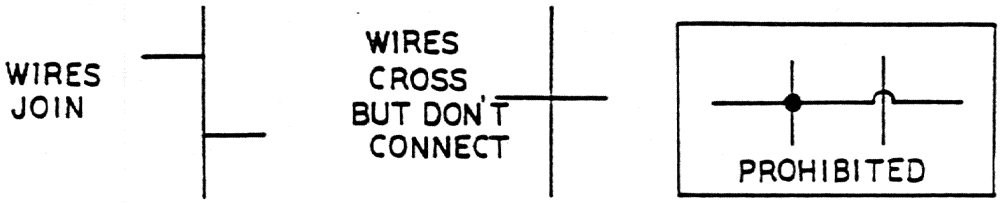
2.1.1 Spacing

Long parallel lines on a circuit schematic should be arranged in groups, preferably in groups of three, with double spacing between each group. A space of at least 5 mm (0.2 inch) must exist between parallel lines and between lines and components.

2.1.2 Junctions

All junctions must be drawn as single junctions. Solid dots to show connections, and "wickets" to show crossovers are prohibited.

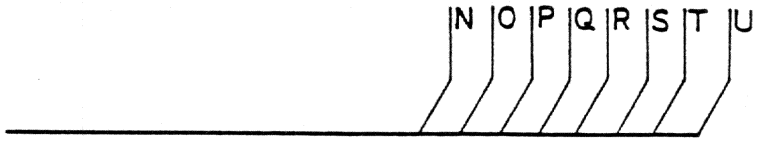
Examples:

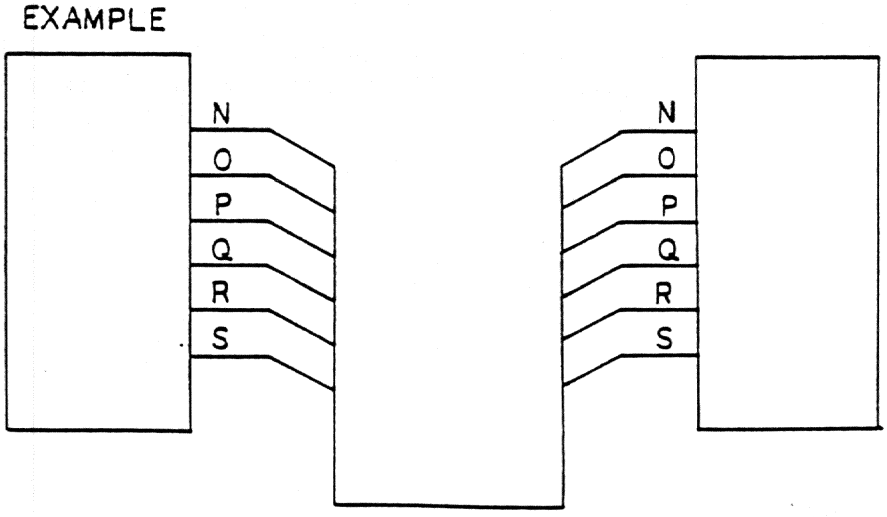


2.1.3 Grouping of Leads

Leads may be grouped using the following symbol convention. Labels, however, must be included on both ends of the leads.

Examples:

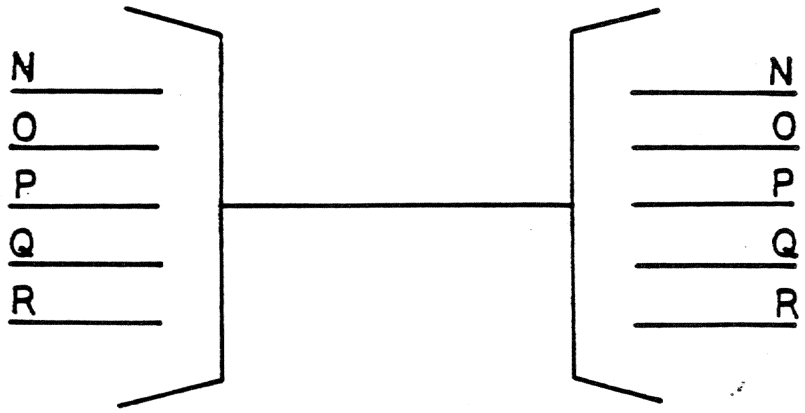




2.1.4 Interrupted Cables

Cables may be interrupted by using the following symbol convention. Labels, however, must be included on both ends of the leads.

Example:



2.2 SIGNAL NAMES

Signals either leaving a page or not directly interconnected by lines on the page must have signal names. Signal names take the form "An NAME X," where

An - Source designator

NAME - Description of signal function

X - Assertion level of signal if digital

When possible, input signal names should be grouped and brought in from the left or bottom. Output signal names should be grouped and brought to the right or top.

Table 4-1 lists the character set allowed for each of the associated CAD tools.

Table 4-1. CAD Tool Character Sets

Program	Number of Characters	Alphanumerics	Quote (Escape) Characters
TLE	25	Embedded spaces, no specific assn/pol. All SIXBIT except : ; . , / = * [ ] " '	"xx" 'xx'
WRL	22	All printable except . and , Fixed field format	None
TUMS (ISPS)	>100	Begin with alpha. Period for hierarchy. No special characters	None
SAGE 2	25	Embedded spaces plus the following: % ( ) + - .	? x ? x
SAGE 3	25	Embedded spaces plus the following: _ % , $ assn and pol	"xx"
SUDS	25	Embedded spaces plus _ % .	

2.2.1 Assertion Level (X)

Assertion levels are required on all digital signal names. They indicate the physical level, usually a voltage level, in which the signal is asserted.

The assertion level may appear as "H" for high or "L" for low, but must always agree with the output from which it emanates. For example, if the output has low assertion indicators (o), the signal assertion level will be "L" or low.

It is preferred that the signal assertion level should agree with the input assertion level. For example, FOO H should go into an input without a low assertion indicator, whereas FOO L should go into an input with a low assertion indicator. The assertion level may be inverted (that is, "L" replaced by "H" or vice versa) and the signal name preceded by a "not" indicator " ~ " or "-". In these cases, the " ~ " symbol is preferred, and an overbar is not acceptable.

For flip-flops, registers, and monostables, the indicator (0) or (1) is changed when the assertion level is inverted.

2.2.2 Source Designator (An)

This portion of the signal name is required on all drawing sets with more than two pages. The source designator carries the following information.

A - An upper case alpha code of undefined length for the circuit schematic on which the signal appears.

n - A page number with enough leading zeros to make the total number of characters equivalent throughout the drawing set.

Bused signals appearing on multiple pages should carry a unique source designator. See subhead 2.3 for more information on bused signals.

Examples:		
	Read/Write CS	RWn
	Bus Interface CS	BIn
	Power supply regulator	RGn

2.2.3 Description of Signal Function (NAME)

This portion of the signal name is required. The signal function name, the source designator, and the space between each shall not exceed 22 characters, including imbedded spaces. The name is supplied by the engineer, and should describe the function of the signal.

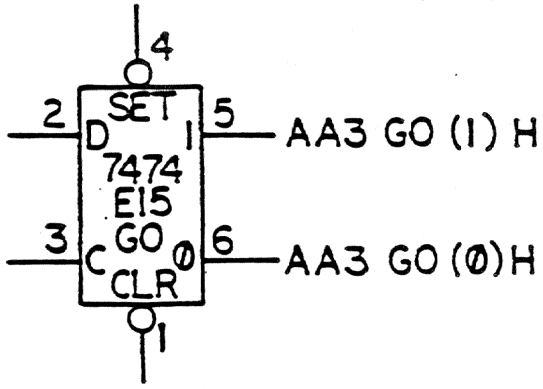
Signals that are the outputs of flip-flops or one-shot monostables have names ending with (1) or (0). This indicates the logic output from which the signal emanates. Both outputs of a flip-flop must carry the same name except for the (1) or (0) designator. Where only one side of a flop-flop is used or exists, the (0) or (1) may be omitted.

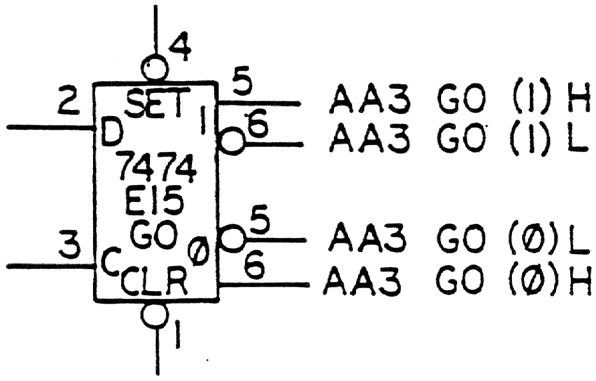
Example:	GO (1) H	Says GO flip-flop in the (1) state asserted high.
	GO (0) H	When in the (1) state, not asserted.

Note

The designators (1) and (0) a leading "not" sign (~ or -),the single spaces immediately preceding and following them and the "H" or "L" are not included in the 22-character limit.

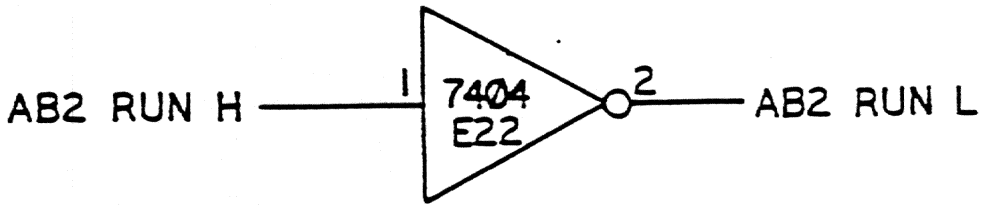
Examples:


4
2
SET
D
1
5
AA3 GO (1) H
7474
E15
3
C
GO
Ø
6
AA3 GO (Ø)H
CLR
1


4
2
SET
5
AA3 GO (1) H
D
1
6
AA3 GO (1) L
7474
E15
3
C
GO
Ø
5
AA3 GO (Ø) L
CLR
6
AA3 GO (Ø) H
1

If two signals emanating from the same source have opposite polarities, they should have the same name.

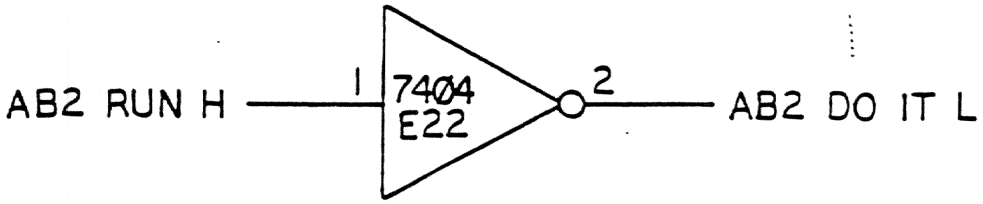
Examples:



Note

If the inverter is on a different page than the source of its input, then the signal name of the output of the inverter shall have the prefix of the page that the inverter was on. This practice should be avoided if possible.

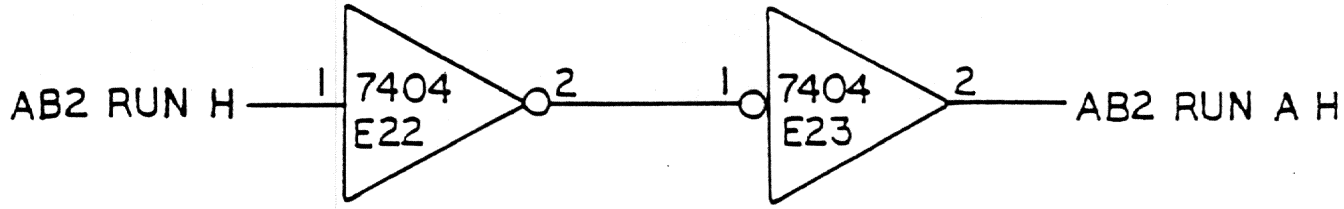
Example: UNACCEPTABLE USE



NOT RECOMMENDED

When two signals exist that are identical except for different sources, they must carry the same name except for a letter modifier.

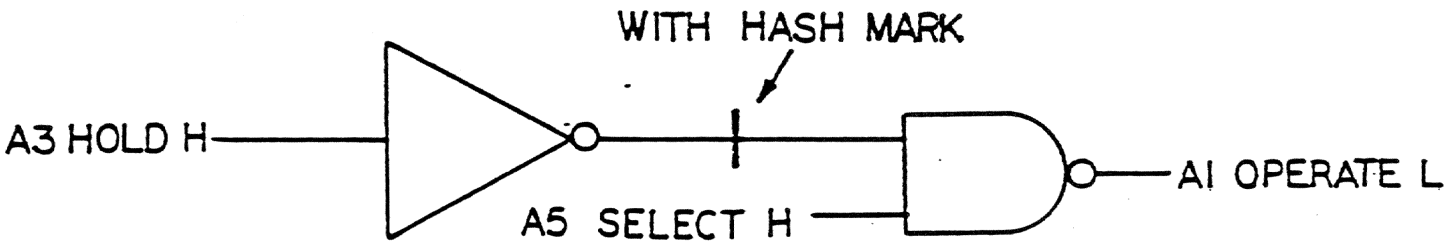
Example:

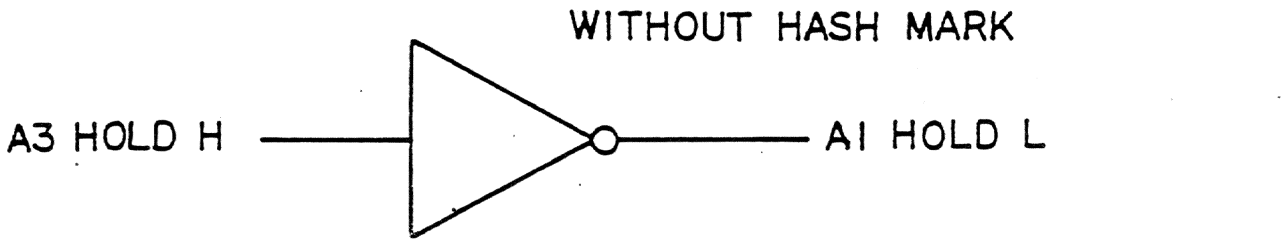


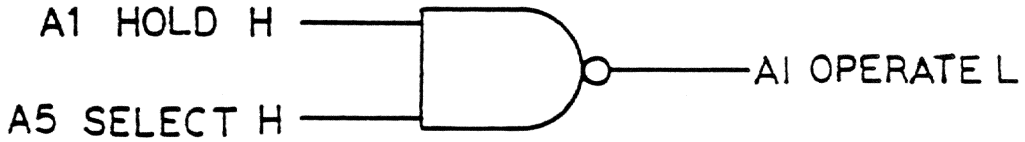
2.2.4 Polarity Mismatches

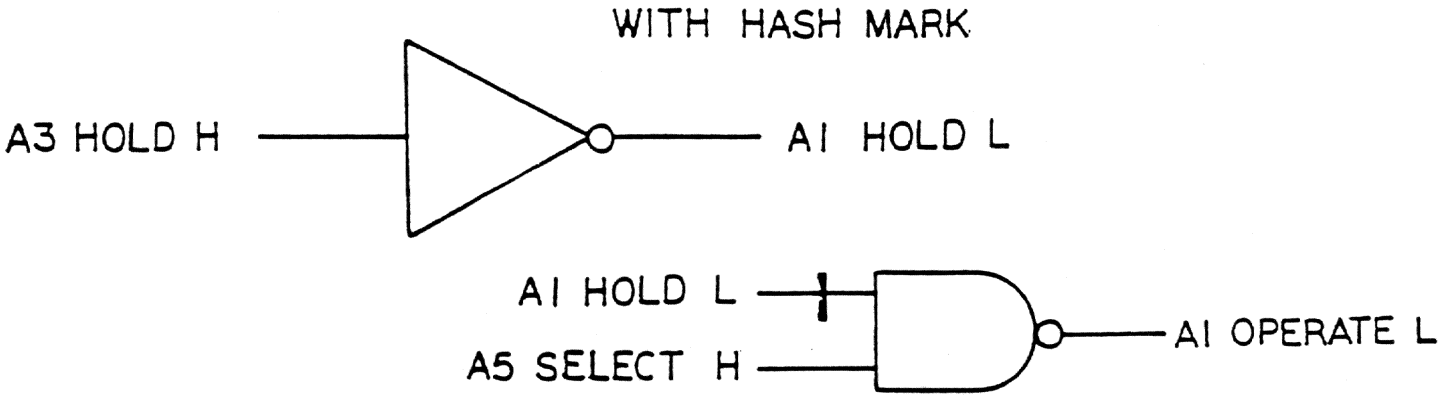
Hash marks are shown to correct polarity mismatches only. The mark is a heavy perpendicular line that intersects a signal run.

Example:





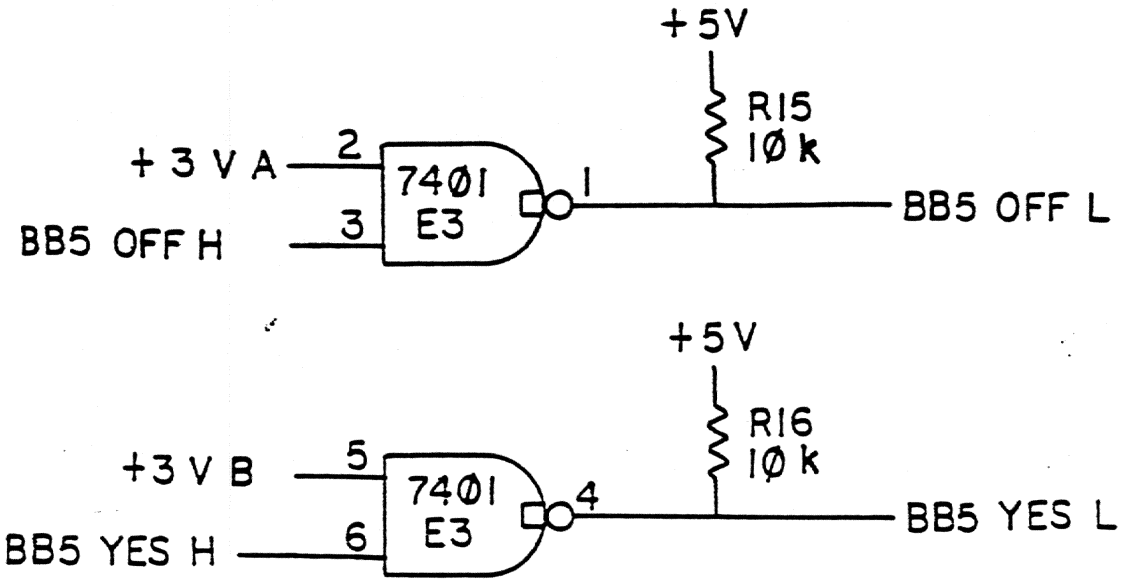




2.2.5 Power Signal Names

Connections to power buses should be labeled instead of connected by lines. For multiple buses of the same voltage, a uniqueness suffix must be added.

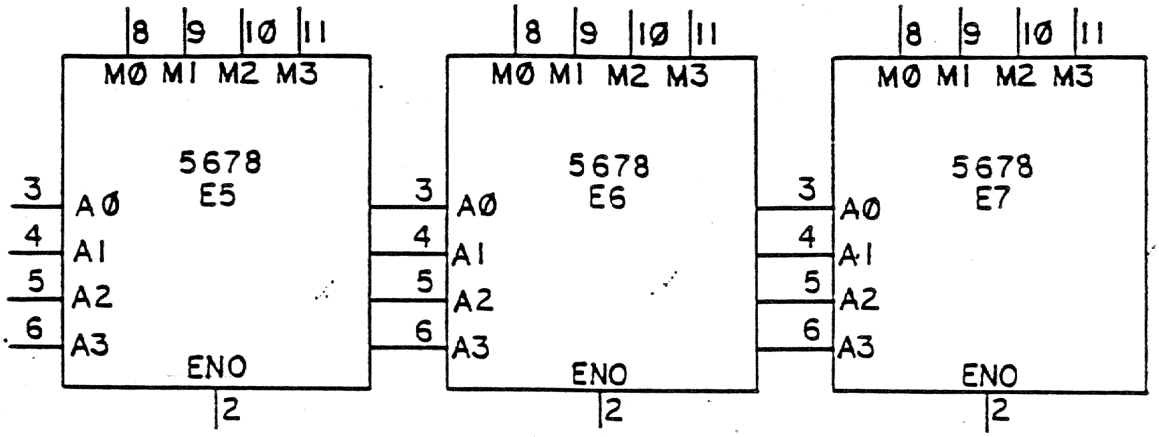
Example: Single +5 V bus and two +3 V buses on the module:

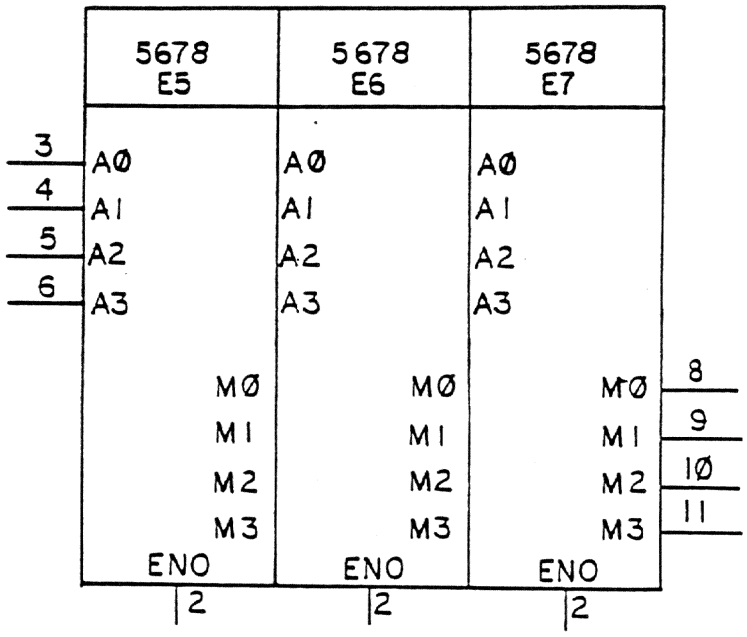


2.3 SIGNAL BUSING

Signal buses common to identical symbols may be shown by placing the identical symbols side by side or touching. The common signals are shown entering the first symbol or leaving the last symbol. Signal buses must have identical symbols with the pin locations shown in the same positions.

Examples:

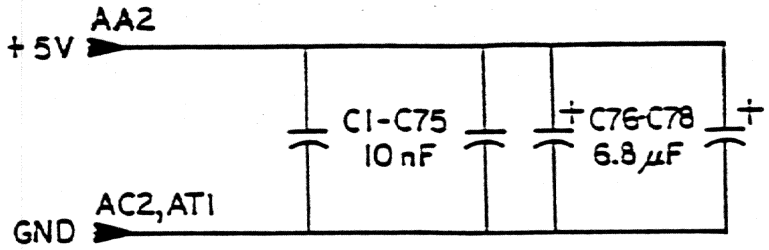




2.4 FILTER CAPACITORS

When appropriate, filter capacitors may be shown in the following way.

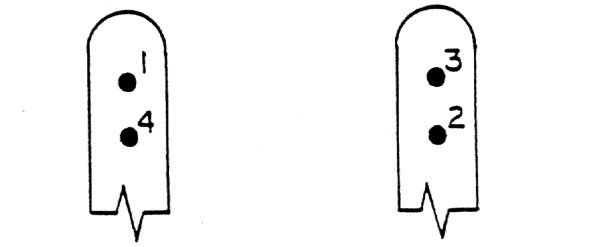
Examples:



2.5 CONNECTORS

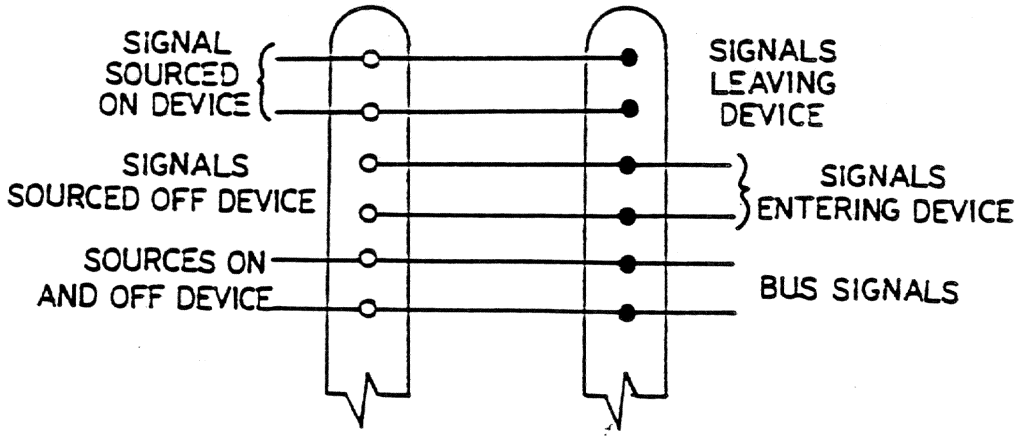
When logic flow dictates, separate portions of connectors may be shown in different locations on a drawing set. Pins do not have to be in alphabetic or numeric order.

Example:



It is recommended that connectors be drawn so that signals leaving the device are drawn to the left of the connector symbol, and signals entering the device are drawn to the right of the connector symbol.

Example:



REFERENCED DOCUMENTS

EL-CLASS DOCUMENTS

EL-00056-00 DEC STD 056-0 Symbology - Circuit Schematic Requirements

Copies of the referenced document can be obtained from:

Standards and Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

digital™

EN-01047-16-REVB(396)

DEC STD 056-5
SYMBOLOGY - INDUSTRY STANDARD LOGIC SYMBOLS AND DIAGRAMS

DOCUMENT IDENTIFIER: A-DS-EL00056-05 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides detailed requirements for the accurate and consistent use of industry standard logic symbols and diagrams.

APPLICABILITY: This section is mandatory for anyone involved in the use and/or design of circuit schematics. This section describes industry standard logic symbols and diagrams to be used universally so that symbology can be interpreted consistently and correctly.

STATUS: APPROVED 15-Jan-1985; see EL-INDEX-00 for expiration date.

TITLE: DEC STD 056-5 SYMBOLOGY - INDUSTRY STANDARD LOGIC SYMBOLS AND DIAGRAMS

DOCUMENT IDENTIFIER: A-DS-EL00056-05 Rev D, 15-Jan-1985

REVISION HISTORY: Rev C 19-Jun-1980
Rev D 15-Jan-1985 ECO# AP002

Document Management Group: Engineering Design/Documentation Methods (TDD)
Responsible Department: ADS Committee (list of current members can be obtained from Standards and Methods Control)
Responsible Individual: Tom Smith

APPROVAL:

Secretary, Engineering Committe

Direct requests for further information to:

Tom Smith
APO-1/C3, DTN: 289-1046, NONAME::SMITH

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APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

TABLE OF CONTENTS/REVISION STATUS

1 INTRODUCTION

1.1 PURPOSE

The purpose of this standard is to provide rules and guidelines by which circuit schematics produced by Digital can also be made to be in accordance with applicable U.S. industry and international standards.

1.2 SCOPE

This standard is mandatory for all circuit schematics produced by Digital that document products started after July 1, 1985. The standard is optional for all other circuit schematics.

This standard also describes the preferred form of circuit schematic documentation for products purchased by Digital from outside vendors. However, any documentation conforming to the referenced industry and international standards shall be considered acceptable.

1.3 RESPONSIBILITIES

See DEC STD 056-0 Symbology - Circuit Schematic Requirements, subhead 1.3.

2 REQUIREMENTS

2.1 SYMBOLS

2.1.1 Logic Symbols

Logic symbols shall be in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617, part 12 (1984). Conformance to the ANSI/IEEE standard shall be considered necessary and sufficient conformance to the IEC publication.

In some cases, the ANSI/IEEE standard permits alternative approaches to symbols. The following list outlines all selected options and exceptions to the referenced sections of ANSI/IEEE Std 91.

a. ANSI/IEEE STD 91, subhead 2.1.2-Nonstandardized Information
Additional information that assists in the interpretation of a logic symbol may be included inside a symbol, enclosed in square brackets, and is encouraged. Signal names or input/output labels supplied by a vendor may be included in this way.

b. ANSI/IEEE STD 91, subhead 2.3.2 - Common Control Block and ANSI/IEEE STD 91, subhead 2.3.2.1 - Weighted Arrays

The common control block may be placed at either the top or bottom of the symbol. In any array in which the individual bits have weighted significance (for example a counter), the individual array elements should be ordered by weight, with the smallest weighted element next to the common control block. To date, all published sources of IEEE symbols show the control block, and therefore the least significant bit, at the top. Using this convention will make it easier to copy symbols from other sources without special expertise in the symbology "language." If the alternative arrangement is used, caution should be exercised in translating a symbol shown with the control block at the top to a form showing it at the bottom. In some cases, a simple top-to-bottom mirror image of the symbol will suffice, keeping the lettering and other qualifying symbols right-side-up. In other cases, for example where a shift function is involved, certain changes may be necessary in one or more of the qualifying symbols.

To avoid confusion, weighted arrays that have an inherent weighting to the individual elements (such as counters) should include within each element the decimal weight enclosed in square brackets. (See symbol 5.13-13.) Arrays such as shift registers and memories that do not have an inherent arithmetic weight need not be labeled in that fashion.

c. ANSI/IEEE STD 91, subhead 3.1 - Negation And Polarity Symbols

All diagrams produced by Digital shall employ direct polarity indication. The symbol indicating inversion is the polarity symbol (symbols 3.1-4 through 3.1-8, and 3.1-11). The negation symbol (symbols 3.1-1 through 3.1-3 and 3.1-10) may be used instead, but must be accompanied by the following note on the diagram.

Note

"DIRECT POLARITY INDICATION APPLIES.
NEGATION SYMBOL IS USED IN LIEU OF
POLARITY SYMBOL."

The negation symbol shall have no line through it.

d. ANSI/IEEE STD 91, symbol 3.3-3 - Open Circuit Output

The symbol for open-circuit output shall not be used. The appropriate symbol for the particular type of open-circuit output (symbols 3.3-4 through 3.3-7) shall be used instead.

e. ANSI/IEEE STD 91, symbols 3.4-4 and 3.4-5 - Signal Flow Arrow

The arrow indicating direction of signal flow shall not be filled.

f. ANSI/IEEE STD 91, subheads 4.3.1 and 6.1.3 - Negated Signal Names and Identifying Numbers

The negation bar over signal names and identifying numbers shall be replaced by a preceding NOT sign (¬) or a preceding tilde (~). If confusion is likely to occur regarding the portion of a label to which an in-line negation character applies, the affected portion may be enclosed in parentheses. See ANSI/IEEE STD 991, section 8.2.2.1.

g. ANSI/IEEE STD 91, symbols 5.1 - 1,2,3,4,11,12,13,14,17,18,20 Distinctive Shape Symbols

Distinctive shape representation is preferred for elementary, nonembedded logic functions with a small number of inputs and a single output. Inputs and outputs shall not be shown on the top or bottom edges of a distinctive shape symbol.

h. ANSI/IEEE STD 91, symbols 5.1-15 and 5.1-16 - Distributed-AND and -OR Functions

Distributed-AND and -OR functions shall not be shown using the simple junction technique. Either the distinctive-shape or rectangular shape "phantom function" shall be shown, and all inputs and outputs shall carry the same polarity or negation symbol. See also ANSI/IEEE Std 991 section 6.1.2.

i. ANSI/IEEE STD 91, subhead 5.13 - Ripple Counters

Counters shall be shown using the qualifying symbol RCTR or RCTRDIVm not as in symbol 5.13-11.

j. ANSI/IEEE STD 91, subhead 6 - Complex Function Elements

The techniques of complex function elements may be used to construct symbols representing a lower level in a hierarchical design.

k. ANSI/IEEE STD 91, subhead 6.1.2 Input and Output Designation (for Complex Function Elements)

Input or output labels shall be selected from the data sheet of the manufacturer who controls the type number shown on the symbol. For example, if the type number is 74xxx, then the input/output labels shall be those found on the Texas Instruments data sheet, regardless of which vendor or vendors supply the part to Digital. If the number shown is a Digital part number (2-5-2), then the input/output labels shall be those found on the Digital purchase specification. If the part is an assembly manufactured by Digital, then the input/output labels shall be the signal names found on the circuit schematic for that assembly.

If the symbol represents a lower level of a hierarchical design, then the input/output labels shall correspond to the input/output labels or signal names found on the lower-level diagram.

2.1.2 Nonlogic Symbols

Symbols for nonlogic devices shall be in accordance with DEC STD 056-3, ANSI Y32.2/IEEE STD 315-1975, and IEC Pub 617, parts 1 through 11 and 13. It should be noted that many conflicts presently exist among the three standards. However, future IEEE work will most likely go in the direction of IEC 617.

2.2 CIRCUIT SCHEMATICS (LOGIC DIAGRAMS)

Circuit schematics shall conform to ANSI/IEEE Std 991 (when issued), IEC Publication 113 (several parts), and ANSI Y14.15-1966, Y14.15a-1970, and Y14.15b-1973. Where conflicts exist, the precedence of standards shall be as listed above. Until published, IEEE STD 991, draft 10 or a later edition may be provisionally used.

Reference designations shall be in accordance with DEC STD 056-3 and ANSI Y32.16/IEEE STD 200-1975. Where conflicts exist, DEC STD 056-3 shall take precedence.

2.3 SOURCES OF INDUSTRY STANDARD LOGIC SYMBOLS

The following is a partial list of publications that contain summaries of ANSI/IEEE STD 91 "Graphic Symbols for Logic Functions," and/or contain catalogs of symbols conforming to the standard.

2.3.1 Vendor Publications

2.3.1.1 Texas Instruments

1. Overview of IEEE STD 91-1984

   This is a condensation of the IEEE standard. It is not complete, but is commendable in its breadth and brevity.

2. TTL Data Book Volume 1 - 1984

   This contains symbols and packaging data for the entire TI TTL line. Other volumes in the series provide more detailed device data. A version of the above overview is also included.

2.3.1.2 Signetics

1. TTL Logic Data Manual 1982 (newer edition available)

   This contains data sheets for most of the Signetics TTL logic devices, each including both "black box" style symbols and new IEEE symbols. 54/74, 54/74S, 54/74LS, and 8T families are covered. No explanation of the symbology is given.

2.3.1.3 Motorola

1. Schottky TTL Data Book (1984)

   This book contains copies of the corresponding TI symbols.

2.3.2 Standards Organizations

2.3.2.1 Nederlands Normalisatie-Instituut

1. Publication NPR 5157, Logic Symbols for Integrated Circuits, 1985.

   This publication is a comprehensive catalog of symbols for 54/74 series through 74699, CMOS 4000 series through 4737, and ECL 10000 series. This document provides some less detailed alternative symbols that may be more useful in an actual application than those found in the TI catalog.

2.3.3 Textbooks

2.3.3.1 McGraw Hill Publications

1. Digital Hardware Design, by John B. Peatman (1980)

   This textbook, by Professor Peatman at Georgia Tech, includes an earlier version of the TI summary of the IEEE standard as well as some tutorial sections on particular aspects of the symbology. These tutorial sections are woven into the other text, but are relatively easily found.

2. Digital Circuits and Microprocessors, by Herbert Taub (1982)

   The new symbology is introduced at various points in the text, but it is somewhat harder to find these sections, and the material is not as completely explained as in Peatman's text. Professor Taub is at CUNY.

REFERENCED DOCUMENTS

EL-CLASS DOCUMENTS

EL-00056-00	DEC STD 056-0 Symbology - Circuit Schematic Requirements

Copies of the referenced documents can be obtained from:

Standards and Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

USA AND INTERNATIONAL STANDARDS

ANSI/IEEE STD 91-1984	Graphic Symbols for Logic Functions
ANSI Y32.2/IEEE STD 315-1975	Graphic Symbols for Electrical and Electronics Diagrams
ANSI/IEEE STD 991 (when issued)	Logic Circuit Diagrams
ANSI Y32.16/IEEE STD 200-1975	Reference Designations for Electrical and Electronic Parts and Equipments

Copies of the referenced IEEE and ANSI/IEEE standards are included in the Logic Symbology Handbook EL-SM056-00 and can be obtained from:

Standards and Methods Control
APO-1/F7, DTN: 289-1414, JOKUR::SIMONETTI

ANSI Y14.15-1966,Y14.15a-1970, Y14.15b-1973	Electrical and Electronics Diagrams
IEC Publication 617 (several parts)	Graphical Symbols for Diagrams
IEC Publication 617, part 12-1984	Recommended Graphical Symbols, Binary Logic Elemens
IEC Publication 113 (several parts)	Diagrams, Charts and Tables

Copies of the referenced ANSI and IEC documents can be obtained from:

Sales Department of American National Standards Institute
1430 Broadway
New York, NY 10018

DEC STD 056-6 SYMBOLOGY - GLOSSARY OF TERMS

DOCUMENT IDENTIFIER: A-DS-EL00056-06-0 Rev INA, 15-Mar-1989

ABSTRACT: This document has been inactivated. There is no replacement.

STATUS: INACTIVATED 15-Mar-1989.

TITLE: DEC STD 056-6 SYMBOLOGY - GLOSSARY OF TERMS

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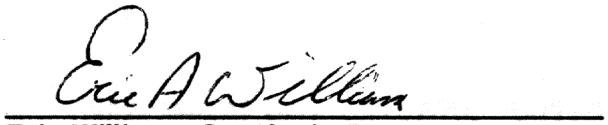

Eric Williams, Standards Process Manager

DEC STD 056-6 SYMBOLOGY - GLOSSARY OF TERMS

DOCUMENT IDENTIFIER: A-DS-EL00056-06-0 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides definitions for certain terms used throughout DEC STD 056.

APPLICABILITY: This section is mandatory for anyone involved in the use and/or design of circuit schematics. This section defines terms used throughout DEC STD 056, with the intention of making a correct and consistent interpretation of these terms possible.

STATUS: APPROVED 15-Jan-1985; see EL-INDEX-00 for expiration date.

FOR INTERNAL USE ONLY

TITLE: DEC STD 056-6 SYMBOLOGY - GLOSSARY OF TERMS

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APPROVAL:

Sue Camber
Secretary, Engineering Committee

Direct requests for further information to:

Tom Smith
APO-1/C3, DTN: 289-1046, NONAME::SMITH

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1 GLOSSARY OF TERMS

Built-Up Symbol - A symbol created by combining one or more distinctive shape symbols with a distinctive or uniform shape base symbol.

Combinational Logic - Logical function whose output is a function of its present inputs only (no memory).

Distinctive Shape - A symbol outline whose shape defines a logical function.

Expandable Gates - Function such that the attachment of additional physical circuits can increase the number of logical inputs.

Flip-Flop - Logical function whose output reflects the history of the sequence of its inputs and may not reflect the state of the present input, thus providing storage.

Function Label - Label required on each symbol designating its logical function, physical part type, and physical location.

Hysteresis - An input with two distinct switching thresholds such that the upper threshold must be crossed for the input to have been considered high, and the lower threshold be crossed to consider the input low. Schmitt Trigger is an example.

Logical Function - An electronic circuit that transforms all combinations of inputs to defined outputs.

Logical Level - One of two levels into or out of a logical function, described as the "1" (asserted) and "0" (negated) levels. It should be noted that these need not correspond to the "high" and "low" physical (voltage) levels.

Monostable - Logical function (one shot) whose output is asserted for a prescribed period of time upon "triggering" and then returns to the unasserted state.

Open Collector - An output consisting of only a pull down transistor. These may be physically attached to other open collector outputs to perform additional logical functions and require external "pull-ups" (current sources).

Physical Circuits - A physical package (integrated circuit) housing one or more logical functions.

Pin - An input or output attachment to a physical circuit.

Pin Label (logical) - A label associated with input or output pin describing the logical function of that input or output with respect to the entire function.

Pin Label (physical) - A label describing the physical position (location) of the pin on the physical circuit.

Recommended - These are optional, not required, items. In general, recommendations should be followed for the sake of uniformity. The recommendations are indicated by the phrase "may be" or "should be."

Required - These are items that must be included unless waivered. They are indicated by the phrases "must be," or "shall be."

Special Indicators - These are attachments to logic symbols that carry specific functional meaning and clarify the overall function of the symbol.

Transition - The change of an input or output from one logical level to the other.

Tristate Output - An output that has, in addition to the two usual logical levels, a third "off" (high impedance) state.

Uniform Shape - A symbol representing a function too complex to be readily expressed by a distinctive shape. The symbol will be a rectangle and the logical function will be conveyed by the function label.

Weighting - The assigning of relative powers to an input or output to show the relative magnitude of the input with respect to the function being performed. For example, a two decade decimal counter may have weights of 1, 2, 4, 8, 10, 20, 40, and 80.

Note

"Address" and "Select" are covered in Table 7-2.

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DEC STD 056-7 SYMBOLOGY - LOGIC FUNCTION LABELS AND PIN LABEL DEFINITIONS

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ABSTRACT: This document has been inactivated. There is no replacement.

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TITLE: DEC STD 056-7 SYMBOLOGY - LOGIC FUNCTION LABELS AND PIN LABEL DEFINITION

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Eric A Williams

Eric Williams, Standards Process Manager

DEC STD 056-7
SYMBOLOGY - LOGIC FUNCTION LABELS AND PIN LABEL DEFINITIONS

DOCUMENT IDENTIFIER: A-DS-EL00056-07-0 Rev D, 15-Jan-1985

ABSTRACT: This section of DEC STD 056 provides authorized logic function labels and pin label definitions.

APPLICABILITY: This section is mandatory for anyone involved in the use of logic function labels or pin labels. This section provides authorized definitions for consistent and accurate use and interpretation.

STATUS: This section of DEC STD 056 will no longer be applicable for new projects starting July 1, 1985.

FOR INTERNAL USE ONLY

TITLE: DEC STD 056-7 SYMBOLOGY - LOGIC FUNCTION LABELS AND PIN LABEL DEFINITIONS

DOCUMENT IDENTIFIER: A-DS-EL00056-07-0 Rev D, 15-Jan-1985

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Responsible Individual: Thomas Smith

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Secretary, Engineering Committee

Direct requests for further information to:

Tom Smith
APO-1/C3, DTN: 289-1046, NONAME::SMITH

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1 INTRODUCTION

The following tables list all currently defined labels to be used in constructing logic symbols according to DEC STD 056-2, and DEC STD 056-3.

Table 7-1 is a list of all currently defined logic function labels compiled according to the principal portion of the label. Each description contains the minimum set of modifiers for that class of logic function labels. Modifiers enclosed in brackets [ ] are required where appropriate. All other modifiers are mandatory. Variable portions of a modifier are shown in lower-case letters.

Table 7-2 lists the definitions of all authorized pin labels.

This section of DEC STD 056 is obsolete for new projects as of 01-Jul-1985. Until that time, either this section or section 5 may be applied.

Table 7-1. Logic Function Labels

CLASS	LABEL	DESCRIPTION
ADD	ADD	1-bit adder
	nB ADD	n-bit adder
ALU	ALU	Arithmetic logic unit
AMP	AMP	Amplifier
	SENSE AMP	Sense amplifier
CNTR	[/n] [/m] [U/D] CNTR	Counter
	CNTR	Binary counter (noncascading)
	/n CNTR	Modulo n counter
	/n/m CNTR	Modulo n modulo m cascade counter. "m" is most significant
	/n U/D CNTR	Modulo n up/down counter.
COMP		Comparator
	nB COMP	n-bit comparator
DECODE	from/to DECODE	Decoder, n to n+m lines To convert data from one number system to another. For example, an octal-to-decimal decoder. From/to: BCD - Bcd code DEC - 1 of n lines 7SEG- 7-segment XS3G- XS-3 Gray
DSPLY	[7 SEG] [LED] DSPLY	Display
DRIVER	DRIVER	Logic to non-standard level converter. It may also be used as a modifier to other labels.
	label/DRIVER	
ENCODE	From/to ENCODE	Encoder, n+m to n lines (see DECODE for codes)
FIFO		First in, first out memory
	n X m FIFO	n words of m bits FIFO

Table 7-1. Logic Function Labels (continued)

CLASS	LABEL	DESCRIPTION
GEN		Generator
	LA CRY GEN	Look ahead carry generator
	PAR CHK/GEN	Parity checker and generator
LCH		Latch
	nB LCH	n-bit latch
MEMORY	none (see FIFO, ROM, RAM, PROM)	
MULT		Multiplier
	type RATE MULT	Rate multiplier type - BIN binary or DEC-decimal
MUX		Multiplexer
	[DATA] [CONTROL] MUX	
	QUAD / DUAL n TO 1 MUX	n lines to 1 line multiplexer
MIX		Alternate label for digital MUX
OSC		(Also see VCO)
	OSC	Oscillator
PROM	n x m [MULTI-PORT] [CHAR GEN] PROM	Programmable read-only-memory n words of m bits
RAM	n X m [MULTI-PORT] RAM	Random access (R/W) memory n words of m bits RAM
RCVR	RCVR	Receiver only when not representable by a simple gate.
	DRIVER/RCVR	Driver/receiver
REG		Register
	nB REG	n bit register
	nB SHFT REG	n bit shift register

Table 7-1. Logic Function Labels (continued)

CLASS	LABEL	DESCRIPTION
ROM	n x m [MULTI-PORT] [CHAR GEN] ROM	Read-only memory (see PROM)
SYNC	SYNC	Synchronizer
TIMER	TIMER	Timer
UART	UART	Universal Asynchronous Receiver/Transmitter
USART	USART	Universal Synchronous/ Asynchronous/Receiver/ Transmitter
USRT	USRT	Universal synchronous Receiver/Transmitter
VCO	VCO	Voltage controlled oscillator

Table 7-2. Pin Label Definitions

Inhibit inputs shall not be used. Use the corresponding (inverted, complemented) enable input instead.

Mnemonic	Definition
A	Address Selector (special case of S for Memories)
AGND	Analog ground
AVCC	Analog Vcc.
BI	Blanking In (Digital Displays)
BO	Blanking Out (nonactive portion of Horizontal and Vertical scans)
BRWI	Borrow IN
BRWO	Borrow OUT
BU	Transceiver I/O Pin (BUS)
BUSY	Busy
C	Clock on simple flip-flops (implied edge trigger)
CG	Carry Generate Output
CKDN	Count Down Clock (implied edge trigger)
CKLD	Load Clock (clock preset inputs, implied edge trigger)
CKSF	Shift Clock. Clocks shifting function (implied edge trigger)
CKUP	Count Up Clock (implied edge trigger)
CLK	Clock on complex symbols (implied edge trigger)
CLR	Clear (set to logical zero) bistable element or array (asynchronous)
COMP	Complement Outputs (input)
CP	Carry Propagate Output
CRYI	Carry Input
CRYO	Carry Output (count has exceeded maximum)
CT	Count
D	Data In
DEC EN	Decimal Enable
DEVEN	Even Parity In
DIN	Data In (on complex functions)
DODD	Odd Parity In
DOUT	Data Out
DVLD	Data Valid
DWN	Down
DX	Data to Transmit Input
DX=Y	Comparator input for X=Y
DX>Y	Comparator input for X greater than Y
DX<Y	Comparator input for X less than Y
EN	Enable
ENCLR	Clear Enable. Synchronous version of CLR
ENLD	Synchronous form of LD. Loads from preset inputs only when clocked

Table 7-2. Pin label Definitions (continued)

Mnemonic	Definition
ENM	Memory Enable. Enables data transfers into and out of memory. Does not enable or disable outputs or inputs.
ENO	Outputs enable on tri-state or open collector outputs
ENRD	Read (synchronous)
ENSET	Synchronous form of Set. Sets only when clocked
ENSFn->m	Enable shift into element whose relative value or uniqueness I.D. is "n," shifting toward element "m." Shifts when clocked
ENWR	Write Enable (synchronous)
EOC	End of character
F	Output of non-bistable function. Function is apparent from symbol. Output is undefined when inputs are undefined.
F(A) - F(G)	7-segment display outputs
FC	Frequency controlling external capacitor pin
FEVEN	Even parity generator output
FODD	Odd Parity Generator Output
FR	Frequency controlling external resistor pin
FSEL	Function Select
FX=Y	Comparator output for X=Y
FX>Y	Comparator output for X greater than Y
FX<Y	Comparator output for X less than Y
GND	Ground
J	J-input to J-K flop
K	K input to J-K Flop
LCH	Latch (hold output values when true)
LCK	Latch, then clock, on edge going false, if true data input occurred while LCK was true, controlled element ->true, otherwise controlled element-> false. Controlled element latched while LCK is true.
LD	Load, synonymous with WR but for devices other than memories (asynchronous)
LSB	Least significant BIT
M	Memory output on ROMS and RAMS (same as R)
MAX	Counter has hit maximum count.
MIN	Counter has hit minimum count.
MSB	Most significant BIT

Table 7-2. Pin label Definitions (continued)

Menmonic	Definition
PARIN	Parity In
PAROUT	Parity Out
PE	Parity error
R	Register (bistable element) output on complex functions. Output retains its last well-defined value.
RB	Ripple blanking input on digital displays
RCV	Receive
RD	Read (Asyncronous)
RDY	Ready output
S	Select (on complex functions)
SET	Set bistable element or array to value (implied value is element or array maximum) (asynchronous)
SINn	Shift input. Input at this pin shifts into the element whose relative value or uniqueness ID is "n."
SOn	Shift output. Output at this pin shifts out of the element whose relative value or uniqueness ID is "n."
SYNC	Synchronization
T	Toggle. Complement state of bistable element
VCC	Constant voltage supplied to collector circuit (see Note 1)
VDD	Constant voltage supplied to drain (see Note 1)
VEE	Constant voltage supplied to emitter (see Note 1)
VSS	Constant voltage supplied to source (see Note 1)
WR	Write (Asyncnronous)
XMIT	Transmit
[Xn]	Left and right brackets. Xn is not defined in this table. Refer to DEC In-House Specification
Y	Output of non-bistable complex function. Function is not apparent from symbol. Output is undefined when inputs are undefined.

Note

These labels are commonly used to tag voltages.