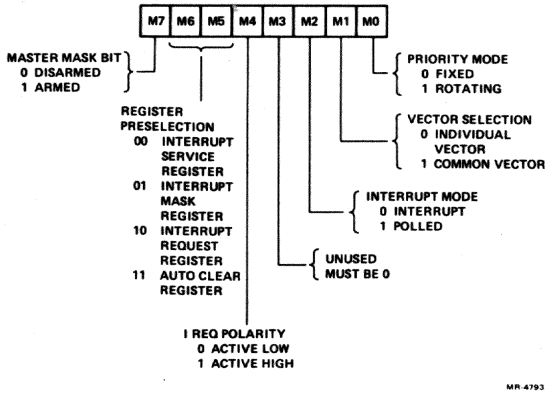
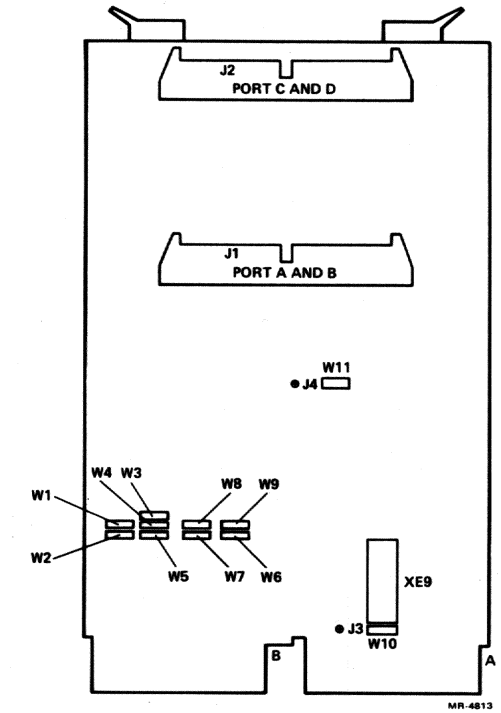
MODE REGISTER BIT ASSIGNMENTS



JUMPER LOCATIONS



COMMAND CODE SUMMARY

Command Code								Command Description
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and IMR bits
0	0	0	1	1	B2	B1	B0	Clear IRR and IMR bit specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR bits
0	0	1	0	1	B2	B1	B0	Clear IMR bit specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bit specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load mode register bits 00:04 with specified pattern
1	0	1	0	M6	M5	0	0	Load mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselect IMR for subsequent writing through CSRB or CSRD
1	1	0	0	X	X	X	X	Preselect ACR for subsequent writing through CSRB or CSRD
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect vector address memory request level specified by L2, L1, L0 for subsequent writing through CSRB or CSRD

NOTE: X = "Don't care" condition

EH-DRV1J-PC-002

DRV11-J Programming Card

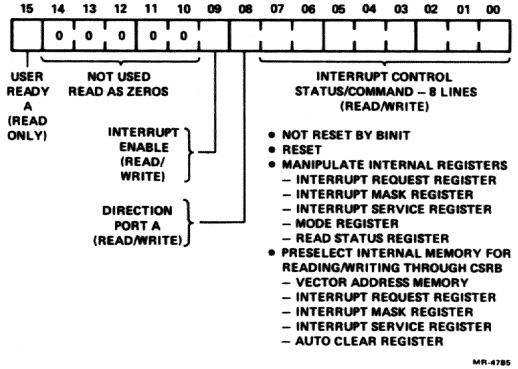
NOVEMBER, 1980

digital

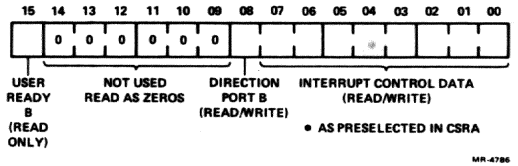
DIGITAL EQUIPMENT CORPORATION

FORMAT OF DIRECT ADDRESSABLE REGISTERS

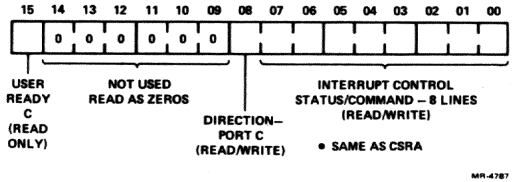
CSRA
LOCATION = DEVICE ADDRESS



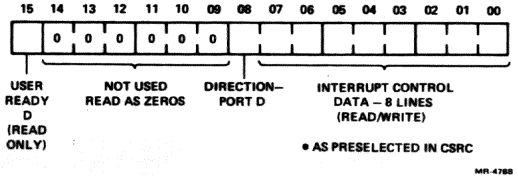
CSRB
LOCATION = DEVICE ADDRESS + 4_8



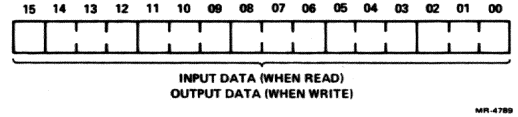
CSRC
LOCATION = DEVICE ADDRESS + 10_8



CSRD
LOCATION = DEVICE REGISTER + 14_8



DBRA, DBRB, DBRC, DBRD
LOCATION = DEVICE ADDRESS = $+2_8$, $+6_8$, $+12_8$, $+16_8$ RESPECTIVELY



DRV11-J REGISTER ADDRESSES

Mnemonic	Description	Address (octal)*
CSRA	Control Status Register A	7XXXX0
DBRA	Data Buffer Register A	7XXXX2
CSRB	Control Status Register B	7XXXX4
DBRB	Data Buffer Register B	7XXXX6
CSRC	Control Status Register C	7XXX10
DBRC	Data Buffer Register C	7XXX12
CSRD	Control Status Register D	7XXX14
DBRD	Data Buffer Register D	7XXX16

*XXXX is jumper selectable between 6000_8 and 7776_8 to select a group of addresses in a modulus of 20 octal. Factory set to 6416_8 (CSRA = 764160_8, DBRD = 764176)

FIXED PRIORITY MODE

Group	Connection	Level	IRR, ISR, IMR, ACR Bit Assignments		Priority
1	A I/O 0	0	D0		Highest
1	A I/O 1	1	D1		
1	A I/O 2	2	D2		
1	A I/O 3	3	D3	CSRB	
1	A I/O 4	4	D4		
1	A I/O 5	5	D5		
1	A I/O 6	6	D6		
1	A I/O 7	7	D7		
2	A I/O 8	0	D0		
2	A I/O 9	1	D1		
2	A I/O 10	2	D2		
2	A I/O 11	3	D3	CSRD	
2	USER RPLY A	4*	D4		
2	USER RPLY B	5*	D5		
2	USER RPLY C	6*	D6		
2	USER RPLY D	7*	D7		Lowest

*Jumper (W11) selects either USER RPLY (A:D) or A I/O <15:12> signals.

VECTOR ADDRESS MEMORY FIELD CODING

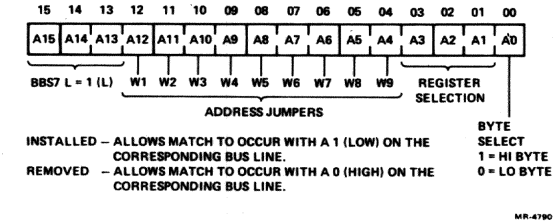
Byte Count Register		
BY1	BY0	Count
0	0	1
0	1	2
1	0	3
1	1	4

IRQ Level			
L2	L1	L0	Level
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

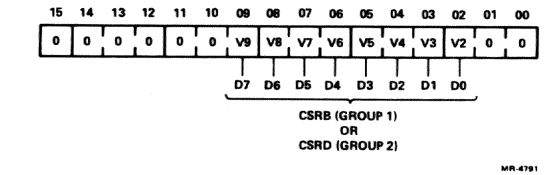
COMMAND REGISTER B2, B1, B0 FIELD CODING

COMMAND REGISTER FIELD			
B2	B1	B0	Bit Specified
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

DEVICE ADDRESS FORMAT



VECTOR ADDRESS FORMAT



CSRA, CSRC STATUS REGISTER BIT ASSIGNMENTS