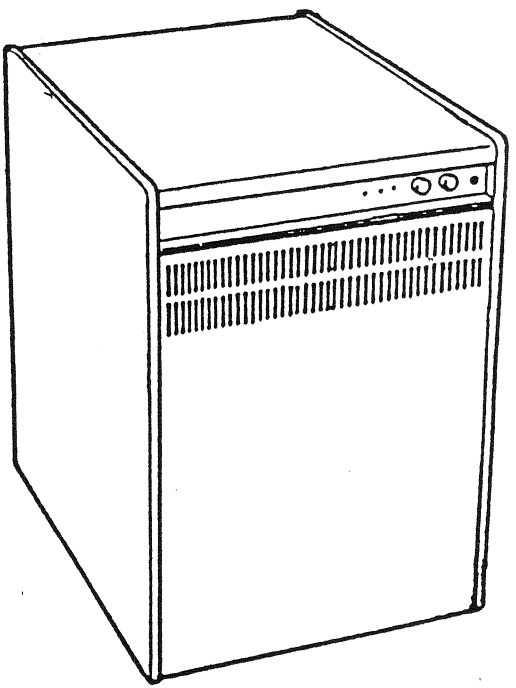
SYSTIME

750 CPU



REFERENCE MANUAL

VAX 11/750 PROCESSOR INFORMATION

Hardware Training cannot accept any responsibility for inaccurate or incorrect data presented in this document.

VAX 11/750 INFORMATION

CONTENTS PAGE

VAX 11/750 INFORMATION

CONTENTS PAGE

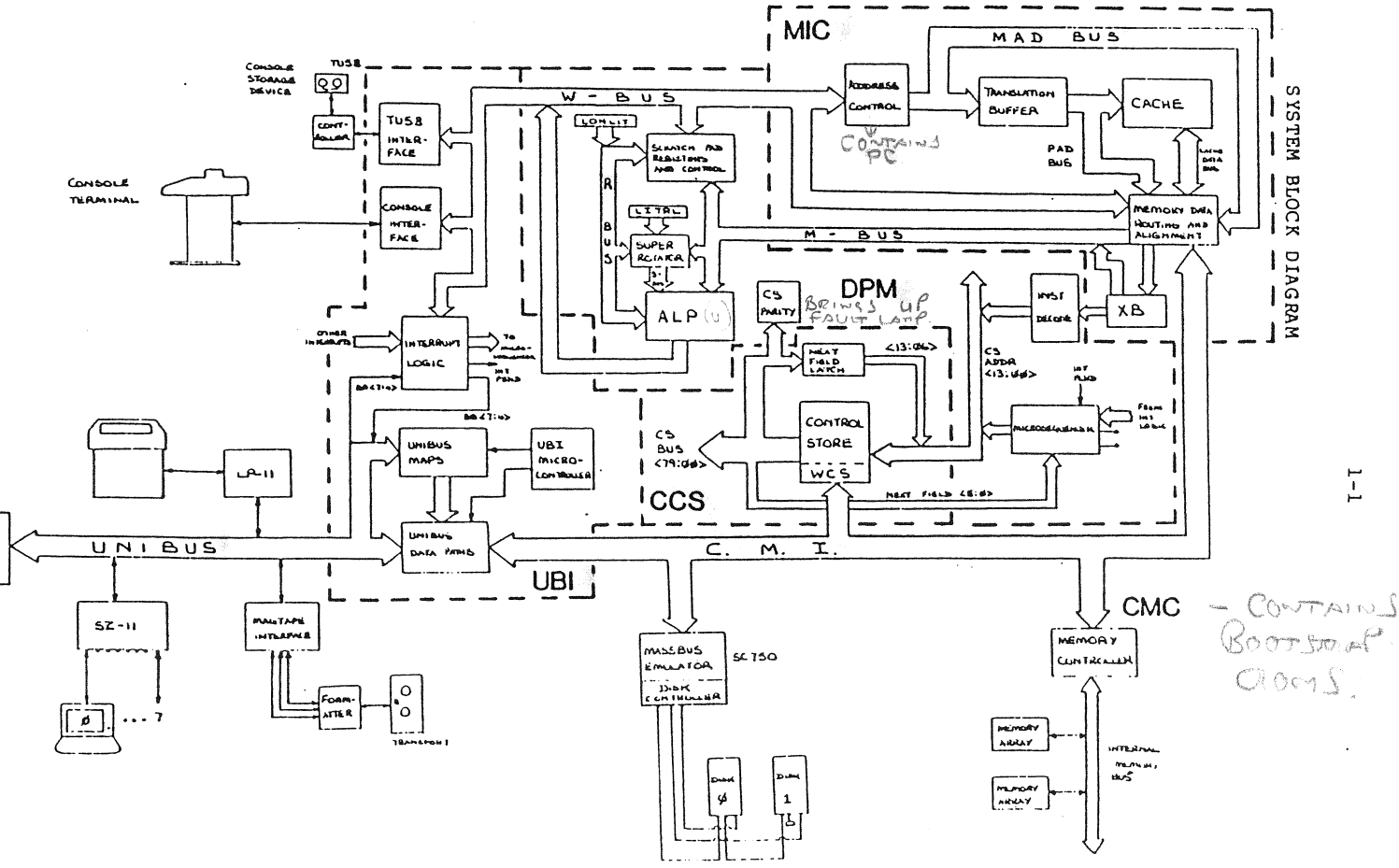
VAX 11/750 INFORMATION

CONTENTS PAGE

APPENDIX A - Product Bulletins

1 - GENERAL INFORMATION

W BUS = WRITE BUS



SUMMARY OF SPECIFICATIONS

CPU

TYPE:	KA750 (VAX 11/750)
CPU CYCLE TIME:	320ns
INTERNAL DATA PATHS:	32-bit
INSTRUCTION BUFFER:	8-byte
TRANSLATION BUFFER:	512 entries
TRANSLATION BUFFER TYPICAL HIT RATIO:	98-99%
PERFORMANCE FACTOR:	0.6
CONTROL STORE:	6KW ROM Standard, 1KW RAM OPTION or, 6KW ROM and 1KW RAM Standard (W=80 bits)

CACHE MEMORY

TYPE:	DIRECT MAPPING
SIZE:	4KB
TYPICAL CYCLE TIME:	320ns
TYPICAL HIT RATIO:	90%

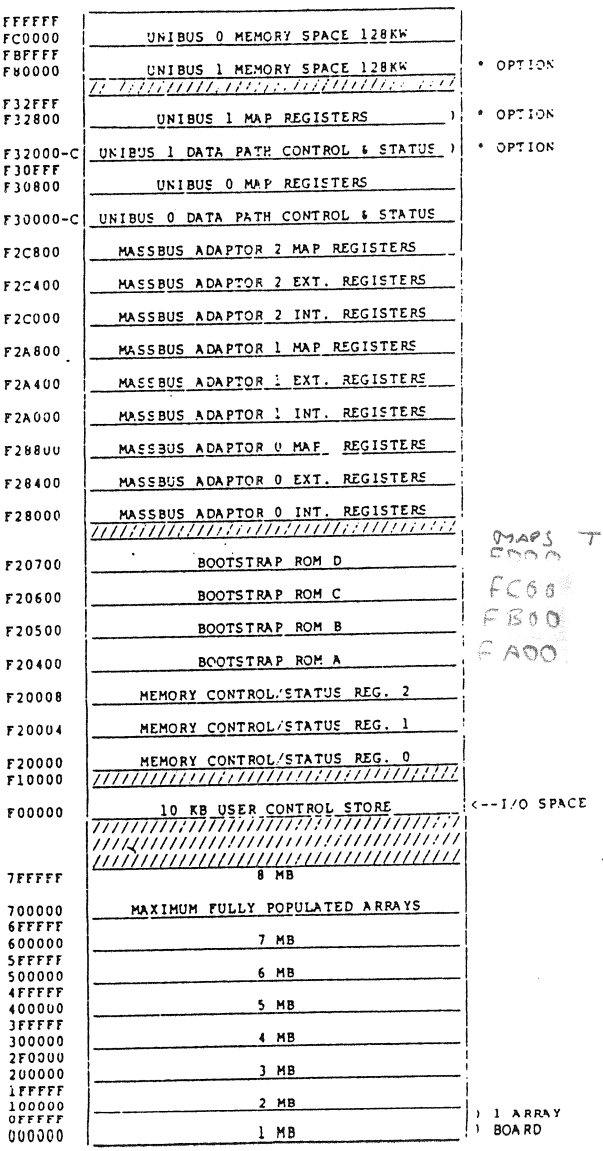
MAIN MEMORY

PHYSICAL ADDRESS SIZE:	24-bits (16MB)
MAXIMUM PHYSICAL MEMORY EXPANSION:	8MB
PARITY:	7-bit ECC
CYCLE TIME:	READ - 800ns WRITE - 640ns

POWER REQUIREMENTS

MAINS SUPPLY:	SINGLE PHASE 240V AC
MAXIMUM POWER CONSUMPTION:	1700watts

PHYSICAL ADDRESS SPACE



INTERNAL PROCESSOR REGISTERS

IPR No.	Mnemonic	RW*	Name
00	KSP	RW	Kernel Stack Pointer
01	ESP	RW	Executive Stack Pointer
02	SSP	RW	Supervisor Stack Pointer
03	USP	RW	User Stack Pointer
04	ISP	RW	Interrupt Stack Pointer
05	Reserved		
06	Reserved		
07	Reserved		
08	P0BR	RW	P0 Base Register
09	P0LR	RW	P0 Length Register
0A	P1BR	RW	P1 Base Register
0B	P1LR	RW	P1 Length Register
0C	SBR	RW	System Base Register
0D	SLR	RW	System Length Register
0E	Reserved		
0F	Reserved		
10	PCBB	RW	Process Control Block Base
11	SCBB	RW	System Control Block Base
12	IPL	RW	Interrupt Priority Level
13	ASTR	RW	AST Level Register
14	SIRR	WO	Software Interrupt Request Register.
15	SIR	RW	Software Interrupt Summary Register.
16	Reserved		
17	CMIERR	RO	CMI Error Register
18	ICCS	RW	Interval Clock Control/Status
19	NICR	WO	Next Interval Count Register
1A	ICR	RO	Interval Count Register
1B	TODR	RW	Time of Day Register
1C	CSRS	RW	Console Storage Receiver Status
1D	CSRD	RO	Console Storage Receiver Data
1E	CSTS	RW	Console Storage Transmit Status
1F	CSTD	WO	Console Storage Transmit Data

INTERNAL PROCESSOR REGISTERS continued

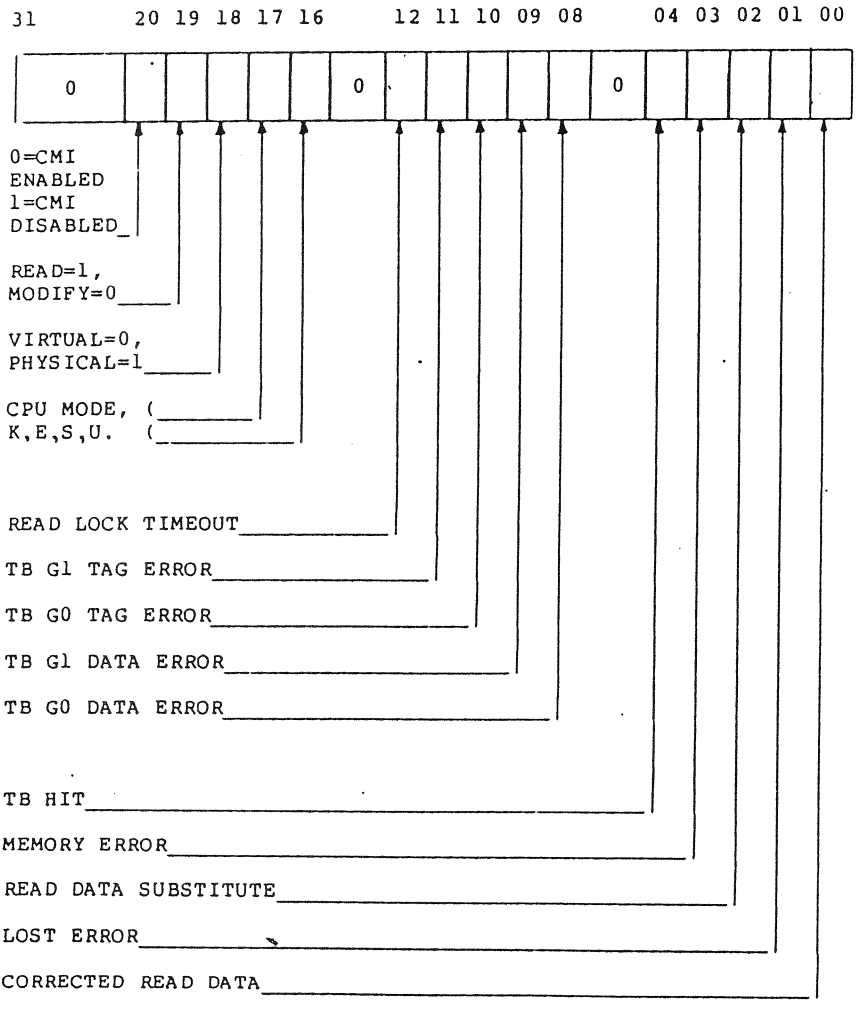
IPR No.	Mnemonic	RW*	Name
20	RXCS	RW	Console Receive Control/Status
21	RXDB	RO	Console Receive Data Buffer
22	TXCS	RW	Console Transmit Control/Status
23	TXDB	WO	Console Transmit Data Buffer
24	TBDR	RW	Translation Buffer Disable Register.
25	CADR	RW	Cache Disable Register
26	MCESR	RW	Machine Check Error Summary Register.
27	CAER	RW	Cache Error Register
28	ACCS	RO	Accelerator Control/Status Register.
29	Reserved		
2A	Reserved		
2B	Reserved		
2C	Reserved		
2D	Reserved		
2E	Reserved		
2F	Reserved		
30	Reserved		
31	Reserved		
32	Reserved		
33	Reserved		
34	Reserved		
35	Reserved		
36	Reserved		
37	IO RESET	WO	Initialize Unibus
38	MME	RW	Memory Management Enable
39	TBIA	WO	Translation Buffer Invalidate All.
3A	TBIS	WO	Translation Buffer Invalidate Single.
3B	TB Data	RW	Translation Buffer Data
3C	Reserved		
3D	PMR	RW	Performance Monitor Register
3E	SID	RO	System Identification
3F	Reserved		

*RO means read-only; WO means write-only. RW means both read and write.

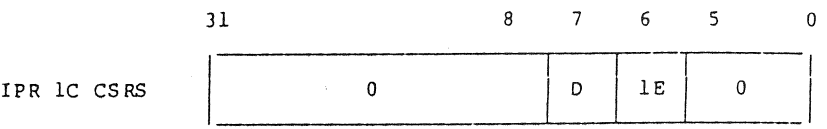
INTERNAL PROCESSOR REGISTERS, BIT DEFINITIONS

The following diagrams illustrate the format of the 8750 specific internal processor registers.

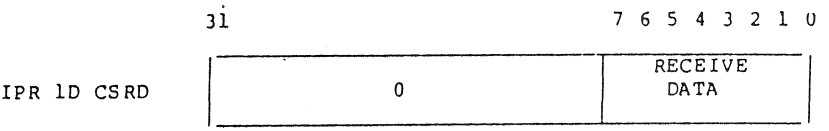
IPR 17 CMI ERROR REGISTER



Console Storage Receiver Status

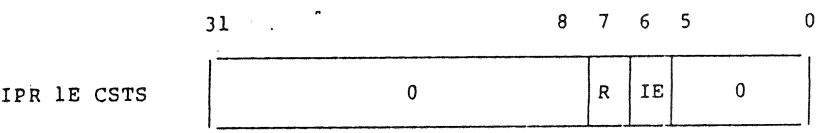


Console Storage Receiver Data

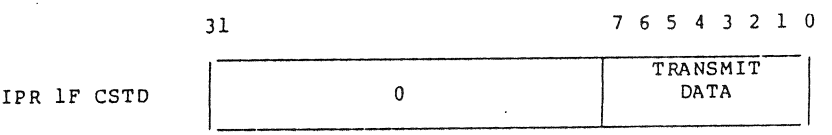


RECEIVE FROM TU58

Console Storage Transmit Status

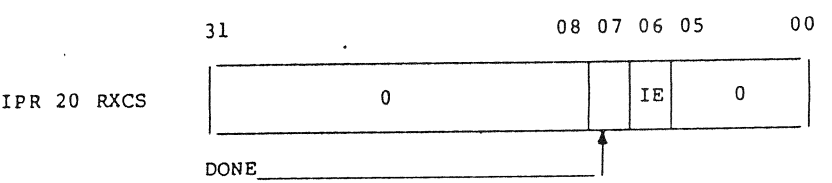


Console Storage Transmit Data

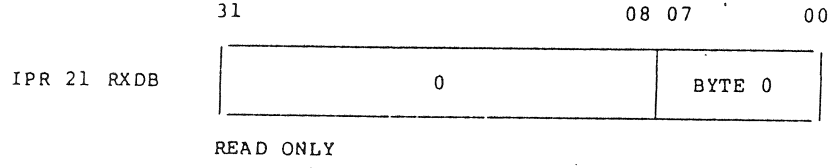


TRANSMIT FROM TU58

Console Receive Control/Status

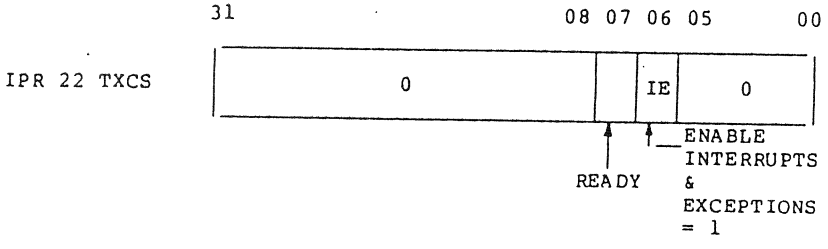


Console Receive Data Buffer

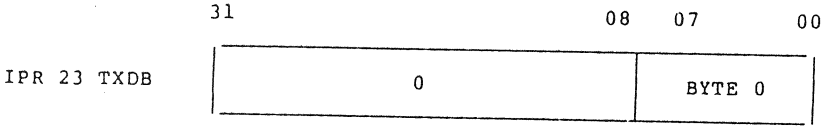


READ ONLY

Console Transmit Control/Status

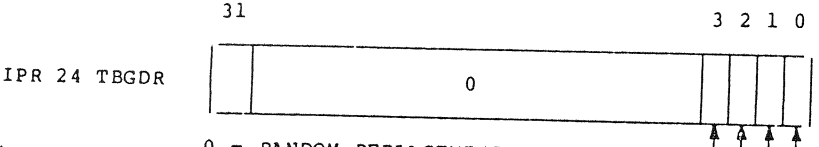


Console Transmit Buffer



WRITE ONLY

Translation Buffer Group Disable Register



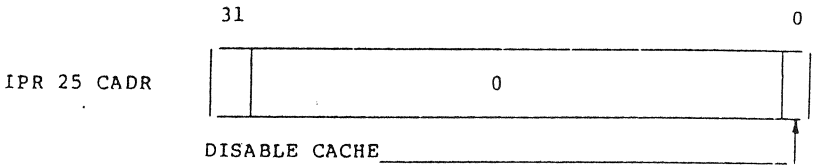
0 = RANDOM REPLACEMENT
1 = FORCE REPLACEMENT

0 = REPLACE GROUP 0
1 = REPLACE GROUP 1

FORCE MISS GROUP 1
FORCE MISS GROUP 0

This IPR is read/write to all bits

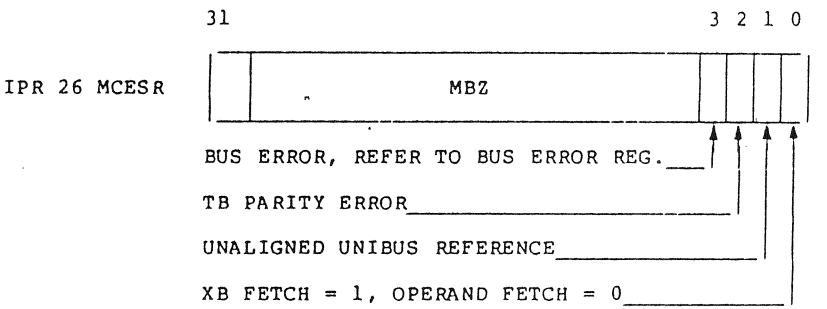
Cache Disable Register



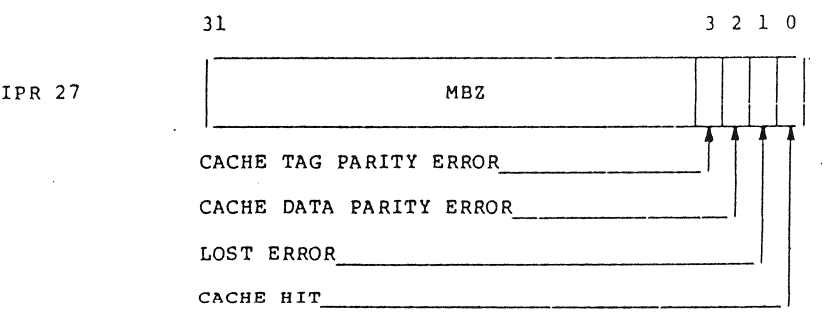
This IPR is read/write

Machine Check Error Summary Register

This IPR is read/write to all bits. Writing a 1 to bit 3 clears the bus error register. Writing a 1 to bit 2 clears the TB Group Parity Register.

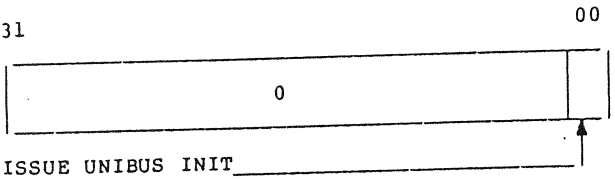


Cache Error Register

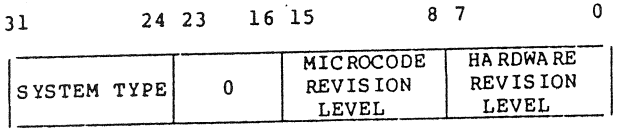


This IPR is read/write

Reset Initialize Unibus



System Identification (Read Only)

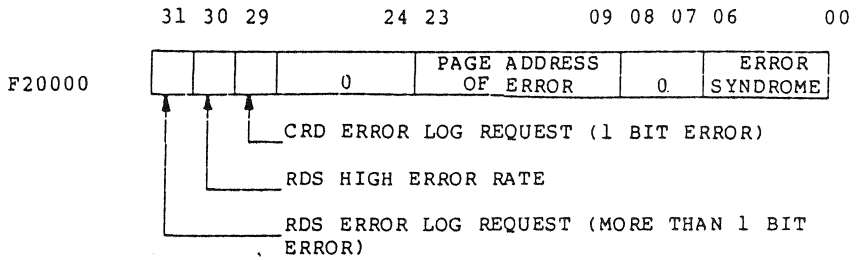


00 UNDEFINED	FROM MICRO WORD LITERAL FIELD	FROM SWITCHES LOCATED ON THE BACKPLANE
01 8780		
02 8750		
03 8730		

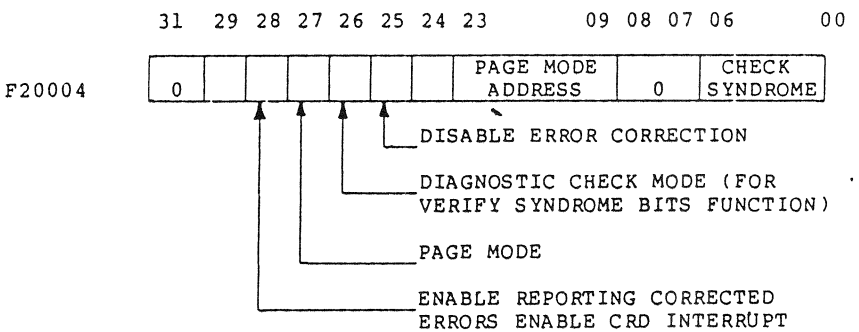
Reserved Operand Fault if Write

MEMORY REGISTERS

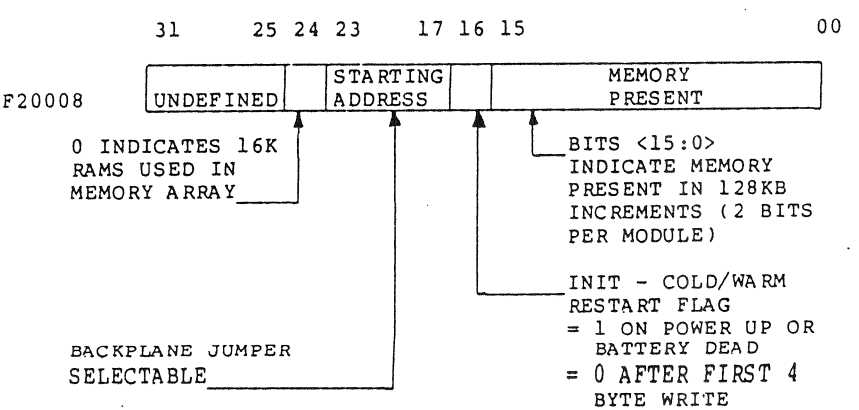
CSR0 Bit Allocations



CSR1 Bit Allocations

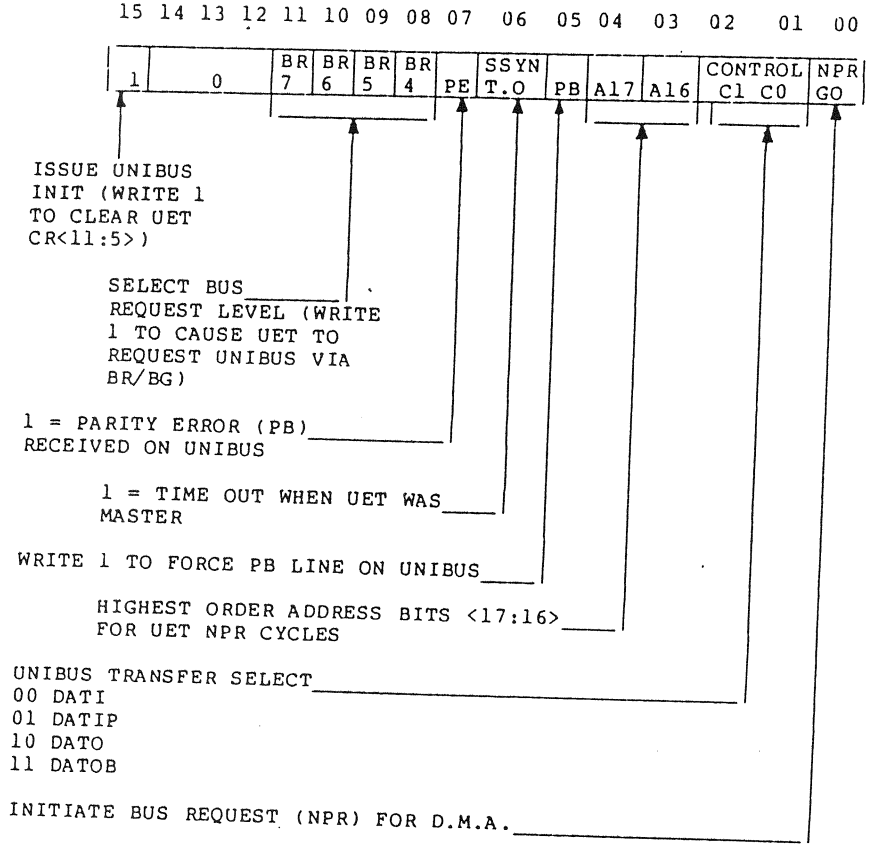


Control/Status Register 2 (RO)

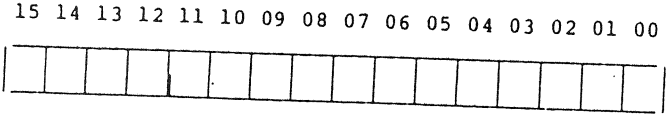


UET REGISTERS

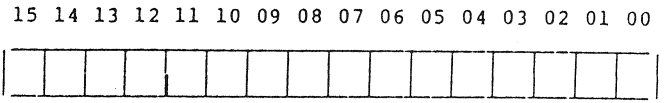
FFF464 UET Control Register



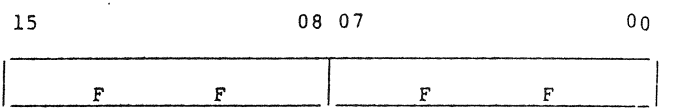
FFF460 UET Bus Address Register (BAR)



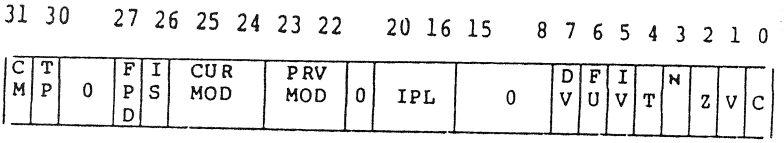
FFF462 UET Data Register (DR)



FFF466 PROM Register (RO)



PROCESSOR STATUS LONGWORD

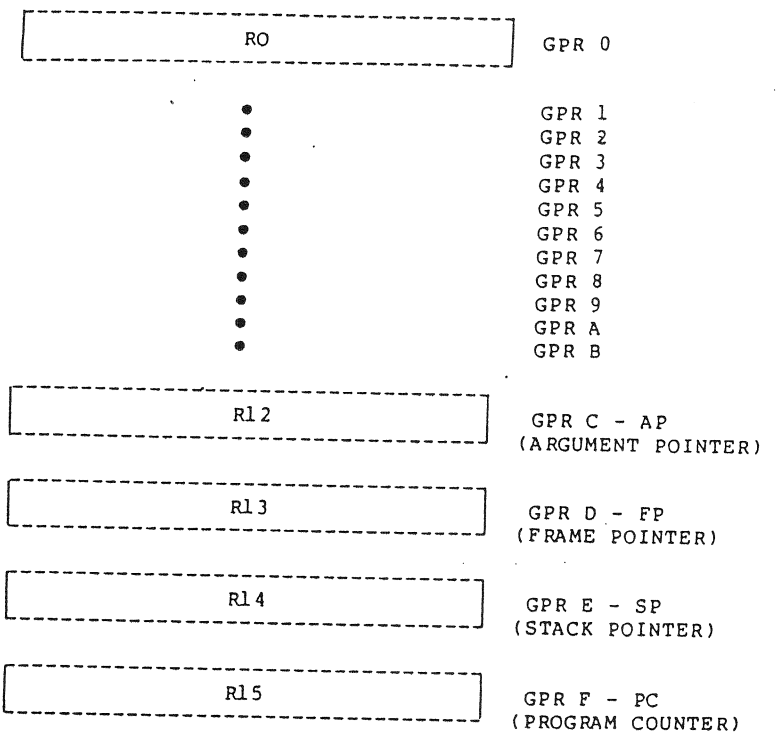


BITS	DESCRIPTION
0-C	Bit 0 is the carry condition code.
1-V	Bit 1 is the overflow condition code.
2-Z	Bit 2 is the zero condition code.
3-N	Bit 3 is the negative condition code.
4-T	Bit 4 is the Trace enable.
5-IV	Bit 5 is the Integer Overflow trap enable.
6-FU	Bit 6 is the Floating Underflow trap enable.
7-DV	Bit 7 is the Decimal Overflow trap enable.
15:8-MBZ	These eight bits are reserved and Must Be Zero.
20:16-IPL	Bits 10 through 16 make up the Interrupt Priority Level or IPL field.
21-MBZ	Bit 21 is reserved and Must Be Zero.
23:22-PRVMOD	Bits 22 and 23 are the Previous Mode Field.
25:24-CURMOD	Bits 24 and 25 are the Current Mode Field.
26-IS	Bit 26 is the Interrupt Stack active bit.
27-FPD	Bit 27 is the First Part Done Bit.
29:28-MBZ	These two bits are reserved and Must Be Zero.
30-TP	Bit 30 is the Trace Pending Bit.
31-CM	Bit 31 is the Compatibility Mode Bit.

NOTE: There are other trap conditions which are always enabled - division by zero and floating overflow.

GENERAL PURPOSE REGISTERS

The VAX architecture defines 16, 32-bit General Purpose Registers shown below.



11/750 INTERRUPT PRIORITY LEVELS

IPL	CONDITION	VECTOR
1F	MACHINE CHECK - CS PARITY - TB PARITY - BAD IRD - MEMORY ERROR - CACHE PARITY	4
	KERNEL STACK NOT VALID INTERRUPT STACK NOT VALID	8
1E	POWER FAIL	C
1D	WRITE BUS ERROR	60
1C	-	
1B	-	
1A	CORRECTED READ DATA	54
19	-	
18	INTERVAL TIMER	CO
17	TU58 RECEIVE TU58 TRANSMIT UNIBUS BR7	F0 F4 200 + VEC
16	CONSOLE RECEIVE CONSOLE TRANSMIT UNIBUS BR6	F8 FC 200 + VEC
15	MBA0 MBA1 MBA2 UNIBUS BR5	150 154 158 200 + VEC
14	UNIBUS BR4	200 + VEC
13	-	
12	-	
11	-	
10	-	
F) e) d) c) b) a) 9) 1)	SOFTWARE INTERRUPTS	BC 84
0	NORMAL PROCESS PRIORITY	-

OPERATOR CONTROL PANEL

INDICATORS (meaning when on)

POWER:	DC Power OK
RUN:	VAX CPU is Running
ERROR:	Control Store Parity Error (Lit Brightly)

KEYSWITCH

OFF:	DC Power Off
SECURE:	DC Power On, Console I/O Mode Disabled
LOCAL:	DC Power On, Console I/O Mode and Program I/O mode enabled.

POWER-ON ACTION SWITCH

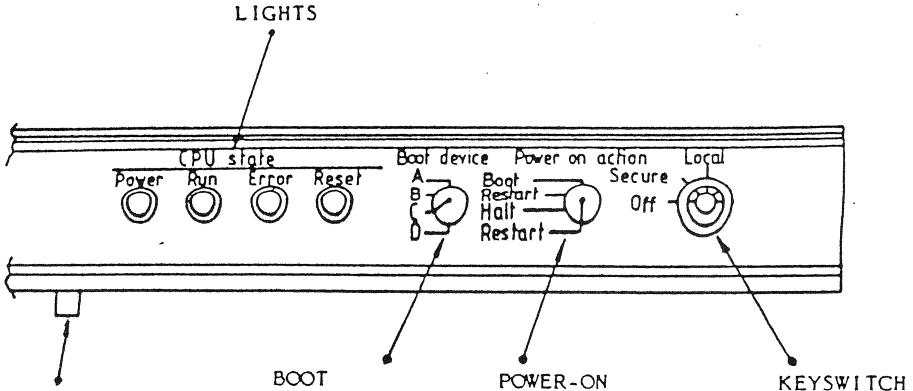
BOOT:	Will boot device selected by the boot device switch on power-up or if RESET switch activated.
RESTART:	On power-up or RESET will attempt to RESTART VMS, if fails will reboot VMS.
HALT:	CPU will halt in console I/O mode after power-up or RESET.
RESTART:	On power-up or RESET will attempt to restart VMS, if fails will HALT.

BOOT DEVICE SWITCH

A - D:	Will select one of four possible boot proms.

RESET

(PUSHBUTTON)	Initiates a power-up/down sequence to reset the CPU.



PROCESSOR MODULES

L0002 DATA PATHS MODULE - DPM

- Arithmetic Logic
- Rotator Logic
- Scratch Pad Register and Control
- Main Microsequencer Logic

L0003 MEMORY INTERCONNECT MODULE - MIC

- Address Logic
- Translation Buffer
- Cache Memory
- Data Routing and Alignment

L0004 UNIBUS INTERFACE MODULE - UBI

- Console TU58 Interface
- Console Terminal Interface
- Interrupt Handling
- CMI/UNIBUS Interface
- T.O.Y. Clock
- Power-up/down Sequencing

L0005 CPU CONTROL STORE MODULE - CCS

- 6KW PROM Control Store
- CPU Clock Source Oscillators
- Space for Systime PCS Update

L0008 PATCHABLE CONTROL STORE MODULE - PCS

- 6KW PROM Control Store
- 1KW RAM Control Store
- CPU Clock Source Oscillators

PROCESSOR MODULES

L0011 COMET MEMORY CONTROLLER 256KB ARRAYS - CMC

Memory Controller for:

SYSTIME 256KB Arrays
M8728 256KB Arrays

L0011 (modified) - CMC 1MB ARRAYS

Memory Controller for:

Systime MK1 1MB Arrays
Systime MK2 1MB Arrays
NS753 Arrays

L0016 MEMORY CONTROLLER 256KB/1MB ARRAYS

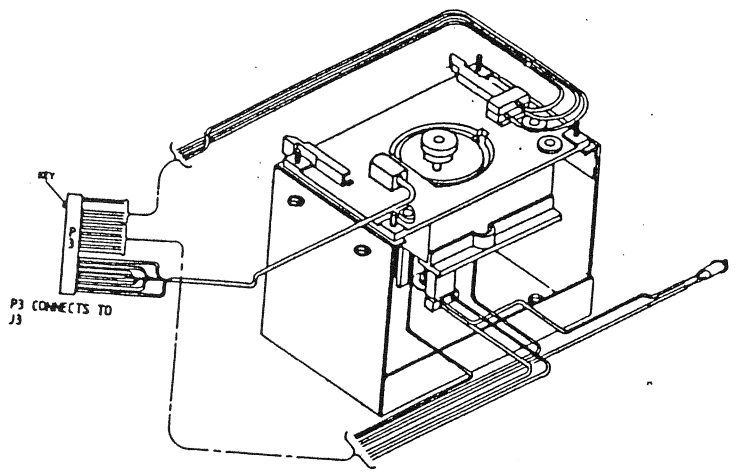
Memory Controller for:

Systime 256KB Arrays
Systime MK1 1MB Arrays
Systime MK2 1MB Arrays
NS753 1MB arrays
M8750 1MB Arrays
M8728 256KB Arrays

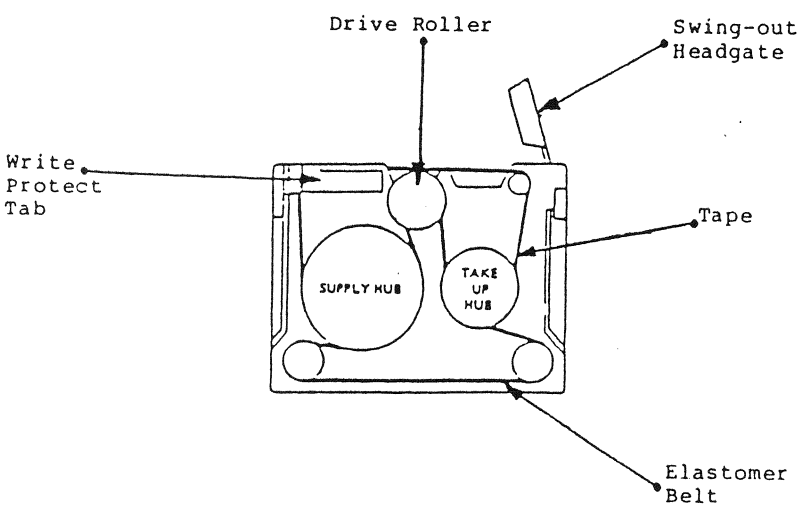
M9313 UNIBUS EXERCISER AND TERMINATOR - UET

TU58 CARTRIDGE

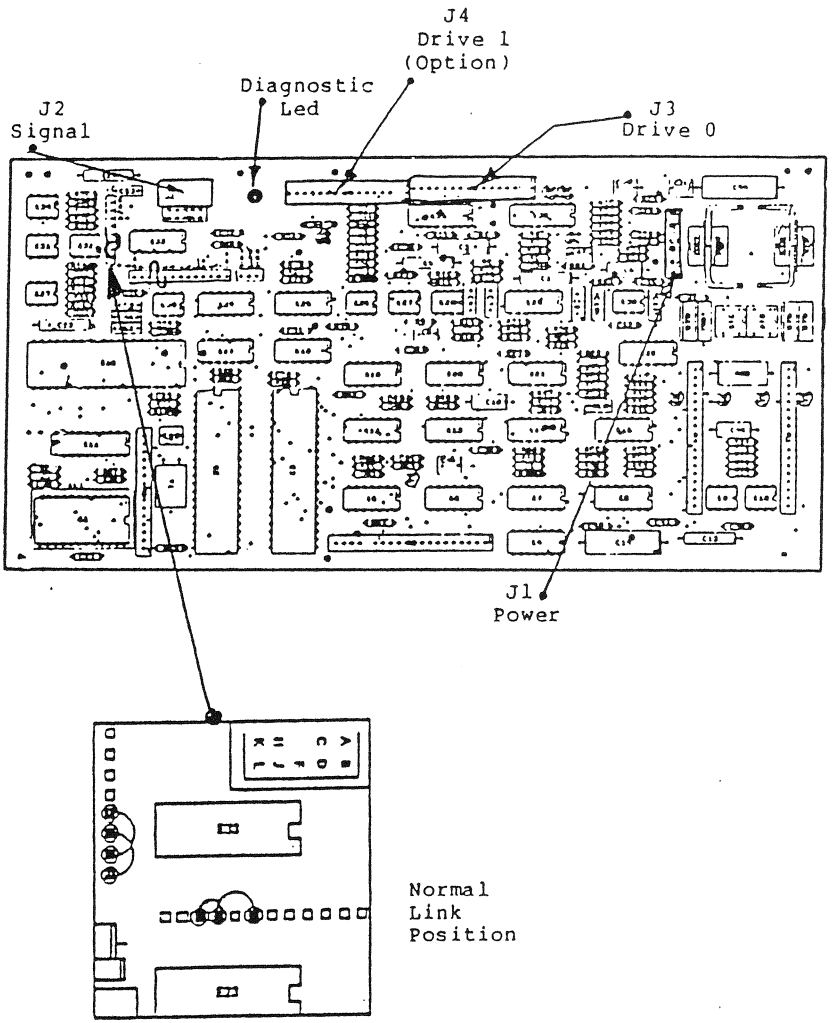
TU58 Drive Unit



TU58 Tape Cartridge



TU58 Controller



MACHINE CHECKS

A Machine Check is an exception that is reported when the CPU or external device detects a serious error. Examples of 8750 machine checks are:-

a) Control store parity error

b) Bad instruction register decode address

c) Double bit memory error.

d) Bus error

e) Cache parity error

f) Translation buffer parity error.

A machine check occurring while VMS is running may cause a FATAL BUGCHECK, which shuts the system down in an orderly fashion, The console terminal will print information about the bugcheck, including a reason for the bugcheck.

If the reason is a machine check, the STACK contents part of the console print out can be decoded. The first entry on the stack must be 28 to be able to decode the correct information.

A machine check that does not cause a FATAL error will be logged in the error log.

The diagram over the page describes the information as it appears on the stack in the event of a fatal bugcheck.

L003 - POSSIBLE

MACHINE CHECK STACK LOGOUT

STACK (SP)	LENGTH PARAMETER	MUST BE 28 IF NOT, THEN LOGOUT IS NOT VALID
(SP)+4	Summary Parameter	1 = CS Parity Error 2 = Memory, Bus, Cache, TB 6,7 = Bad or no IRD ROM Address
(SP)+8	Virtual Address	
(SP)+C	PC	PC at time of error
(SP)+10	MDR	Memory Data Register
(SP)+14	Mode (Part of IPR 17)	3: 0=modify 1=read; 2: 0=virtual 1=physical; 1: 0=kernel 2=super; 0: 1=exec 3=user
(SP)+18	Read Lock Timeout	1 = Read Locked Timeout or Write Vector Occurred (0)
(SP)+1C	Translation Buffer Error (IPR 24)	3: GROUP 1 TAG PARITY ERROR; 2: GROUP 0 TAG PARITY ERROR; 1: GROUP 1 DATA PARITY ERROR; 0: GROUP 0 DATA PARITY ERROR
(SP)+20	Cache Register (IPR 27)	3: TAG PARITY ERROR; 2: DATA PARITY ERROR; 1: LOST ERROR; 0: CACHE HIT
(SP)+24	Bus Error Register (Part of (IPR 17)	3: MEMORY ERROR CMI NO RESPONSE; 2: UNCORR-ECTABLE (DOUBLE) (BIT) ERROR; 1: LOST ERROR (DBL) (BIT) (ERROR); 0: CORRECT-ABLE (SINGLE) (BIT) ERROR
(SP)+28	Machine Check Error Summary (IPR 26)	3: BUS ERROR (SEE BUS ERROR REG.); 2: TRANSL-ATION BUFFER PARITY ERROR; 1: 0; 0: LAST READ 0 = OPERAND 1 = XB
(SP)+2C	PC at Start of Instruction	
(SP)+30	PSL at Start of Instruction	

PERIPHERAL OPTIONS

The 8750 may utilise any of the following controllers and peripherals.

Terminal Controllers

SZ11 or DZ11	8 Line Terminal Multiplexor
CS11/U2	DH11/DM11 Emulator
CS11/F1	DMF32 Emulator
CS21	DMF32 Emulator

Magtape Controllers

SE LABS 8800	TU10 Emulator
TC12	TS11 Emulator
TC13	TS11 Emulator
DU132	TS11 Emulator

Disk Controllers

SC21/V1	RH11 Emulator (Unibus)
SC31/BX	RH11 Emulator (Unibus)
SI9400	RH11 Emulator (Unibus)
SC750	RH750 Massbus Emulator

Other

DMC11	High Speed Interprocessor Link
DMR11	High Speed Interprocessor Link
LP11	Parallel Printer Interface

SYSTEM REVISION LEVELS

The current hardware revision level is:

REV: 7

The module revisions are:

L0003 - REV J

L0004 - REV M

PCS - L0008
- MODIFIED L0005

To perform a check on the hardware revision level:

Examine the system ID register:

```
>>>E/I 3E <cr>
>>>     I  0000003E 02005EXX
```

XX = Hardware Revision Level

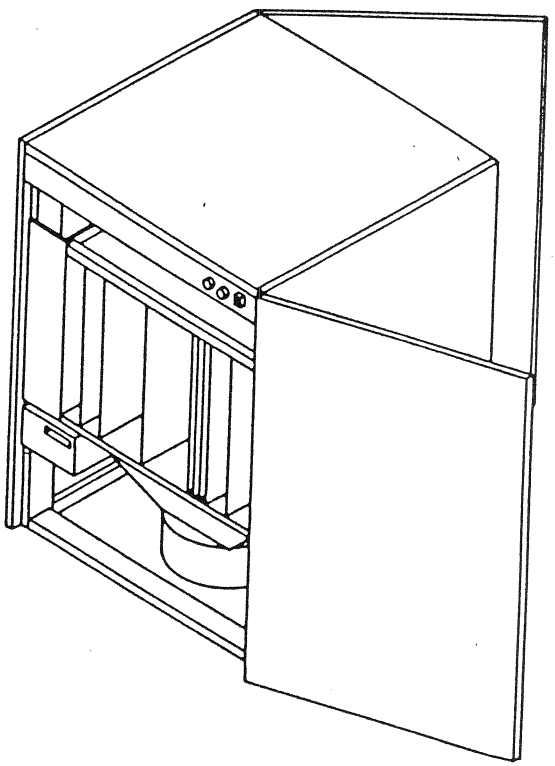
NOTE This is only true for systems using the SID switch module

2 - HARDWARE LOCATION

EXTERNAL COVER REMOVAL

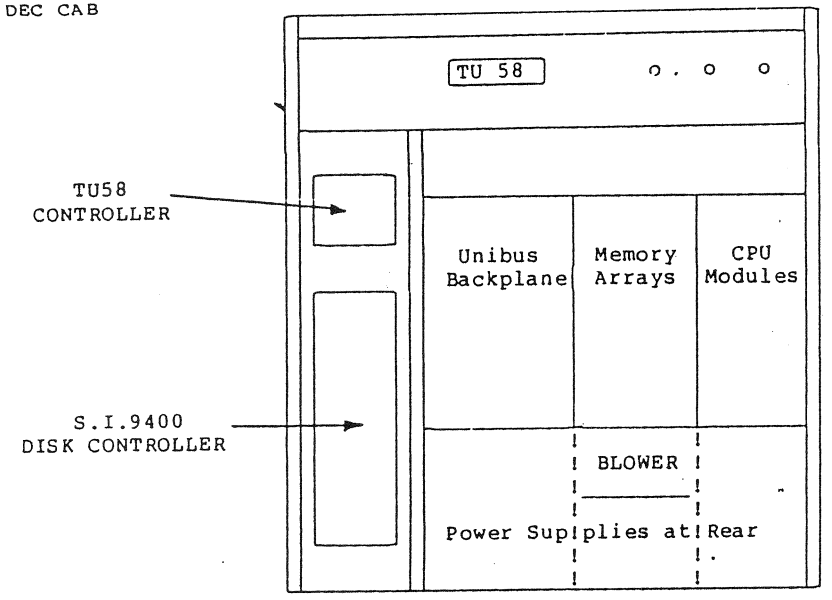
Access to the CPU and Unibus modules and backplanes is through the front and rear doors of the CPU cabinet. The doors are opened by releasing the keylock on both the front and rear door.

There is a metal cover over the module and the backplane access, both are removed in the same way, unscrewing the four retaining screws and lifting the covers off. Take care not to drop any screws. For this reason it is best done with the power switched OFF.

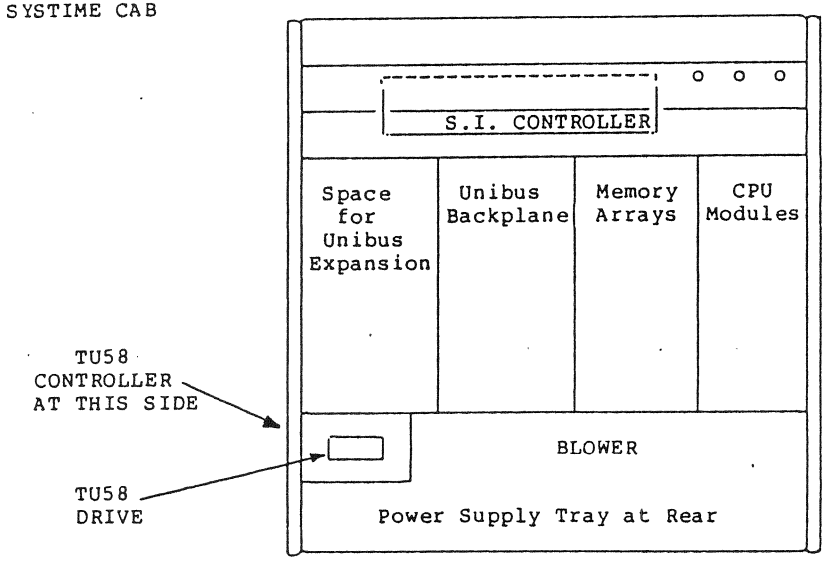


MAJOR ASSEMBLIES

DEC CAB



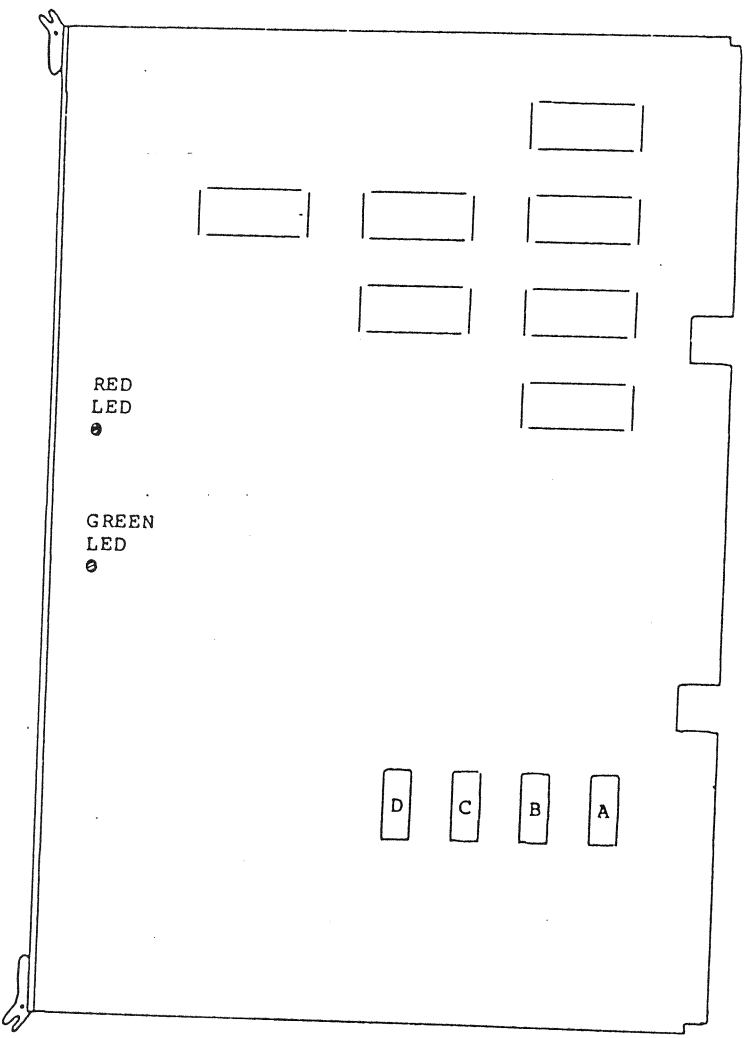
SYSTIME CAB



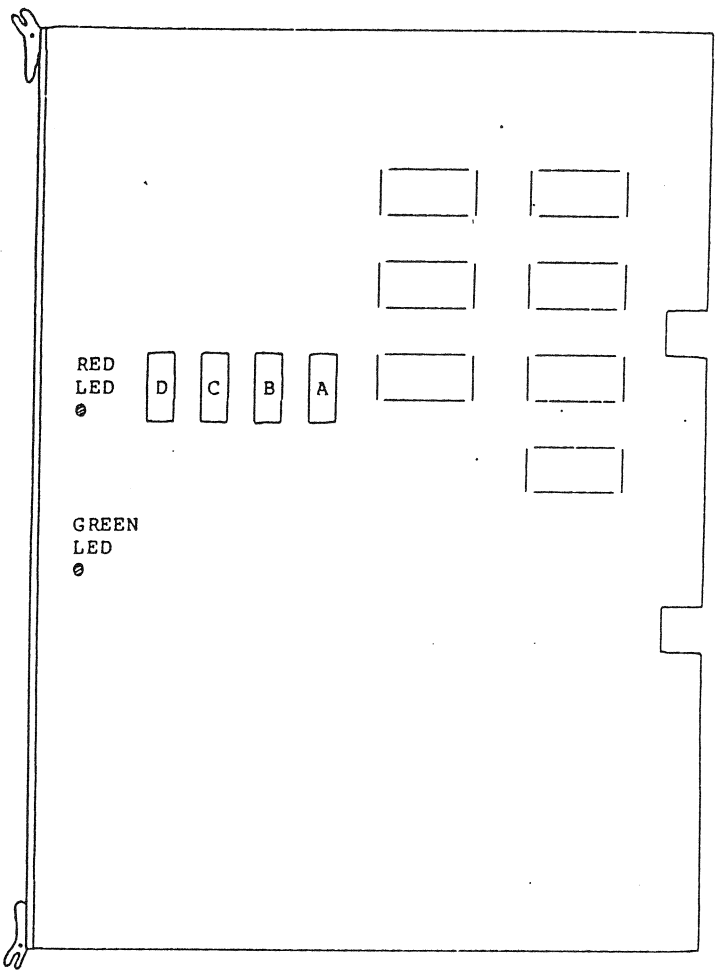
MODULE LOCATION

BACKPLANE SLOT			NOTES
Processor Backplane	1	L0001 FPA	Floating Point Accelerator Option
	2	L0002 DPM	
	3	L0003 MIC	
	4	L0004 UBI	
	5	L0005/L0008 CCS	
	6	L0006 RDM	Remote Diagnostic Module Option
	7	SC750	Option (One L0010 may be placed
	8	SC750	Option in slot 7, 8
	9	SC750	or 9). Option
	10	L0011/L0016 CMC	Memory Controller and Boot ROM's
	11	MEMORY 1MB	
	12	MEMORY	
	13	MEMORY	
	14	MEMORY	
	15	MEMORY	The memory slots 12 to 18 are for additional memory arrays
	16	MEMORY	
	17	MEMORY	
	18	MEMORY	
	19	UNIBUS ---RESERVED---	Bus Jumper/Reserved
Unibus SPC	1	UNIBUS QUAD SPC	Bus Jumper/Any Quad SPC
	2	HEX SPC	
	3	HEX SPC	Any Hex SPC (SZ11 etc)
	4	HEX SPC	As for slot 3
	5	HEX SPC	As for slot 3
	6	HEX SPC	As for slot 3
	7	HEX SPC	As for slot 3
	8	HEX SPC	As for slot 3
	9	M9313 QUAD SPC	Terminator/Any Quad SPC

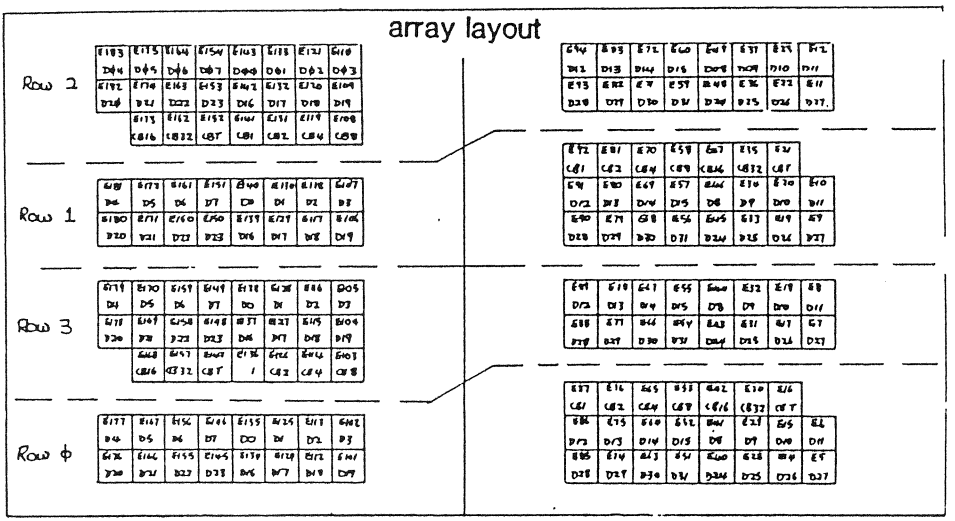
L0011 BOOTSTRAP ROM LOCATIONS



L0016 BOOTSTRAP ROM LOCATIONS



SYSTIME MEMORY RAM LOCATION



1MB SYSTIME MEMORY AND ERROR-LOGGING

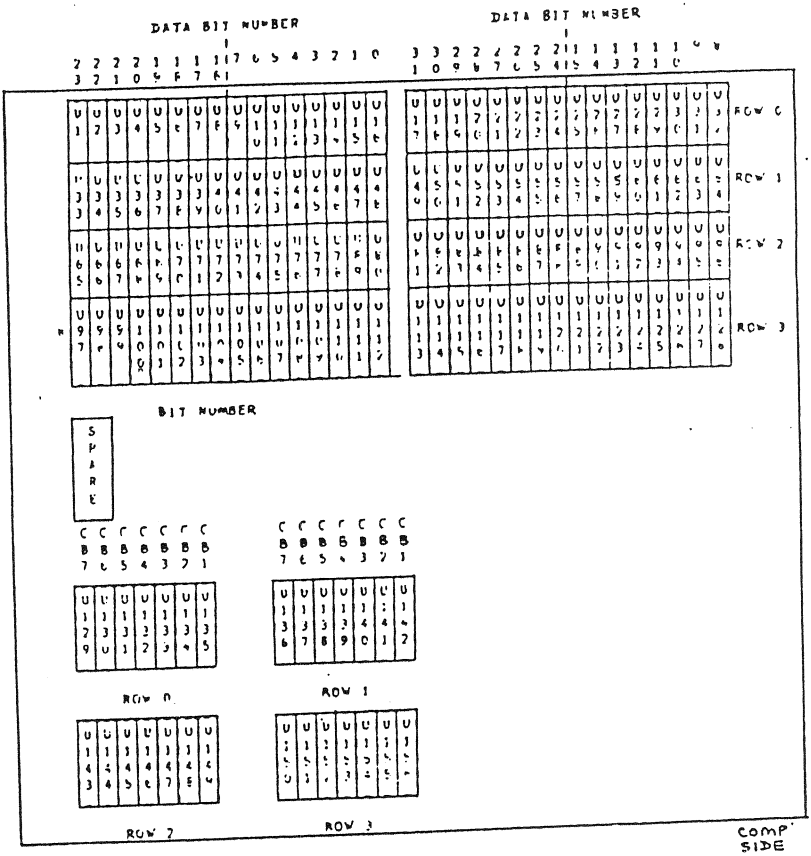
The V.M.S. error-log decodes the array of Systime 1Mb arrays wrongly giving very large numbers for the array number.

The correct array number can be identified using CSR0 bits as follows as given by the error-log printout.

BIT 18
BIT 19 used to select ROMS 0-3

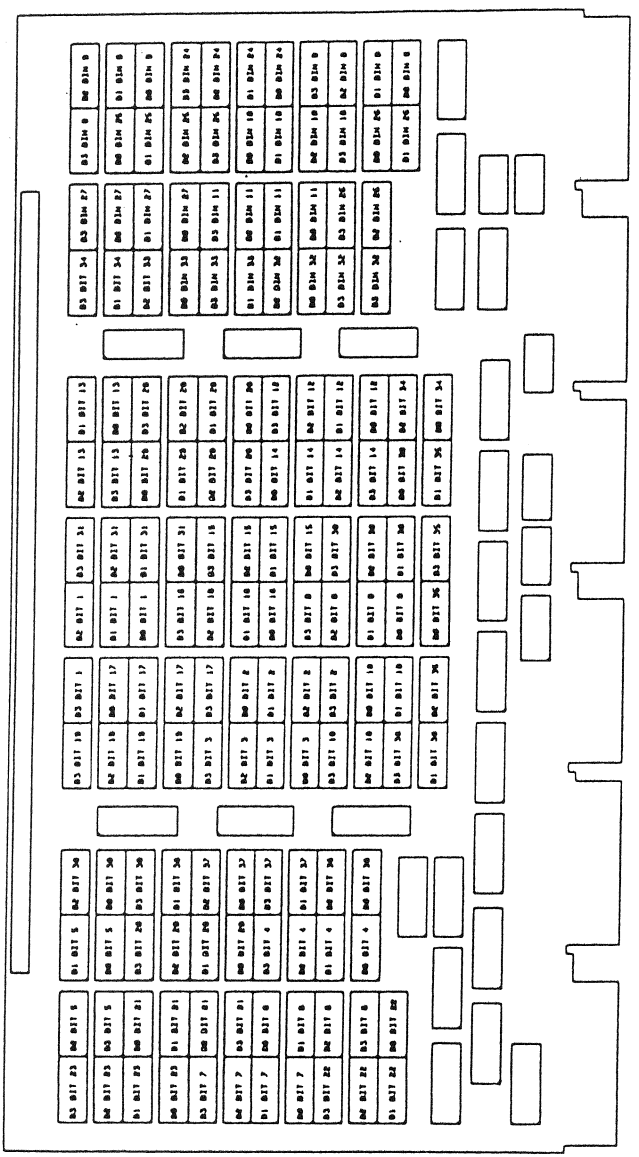
BIT 20
BIT 21
BIT 22 used to select ARRAYS 0-7

NS753 RAM LOCATION CHART



EDGE CONNECTORS

SYSTIME MK2 MEMORY, RAM LOCATION



11/750 OPTIONS

L0001 FLOATING POINT ACCELLERATOR - FPA

This is installed in slot 1 of the CPU Backplane.

L0006 DIAGNOSTIC MODULE - RDM

This is installed in slot 6 of the CPU Backplane. It is for engineering use only and is not normally installed in the field.

L0010 SECOND UNIBUS INTERFACE - SUB

This is installed in slot 7, 8 or 9 depending on what other options are also using these slots.

WCS WRITEABLE CONTROL STORE

This option is not normally used and it depends on the module type of CCS being used.

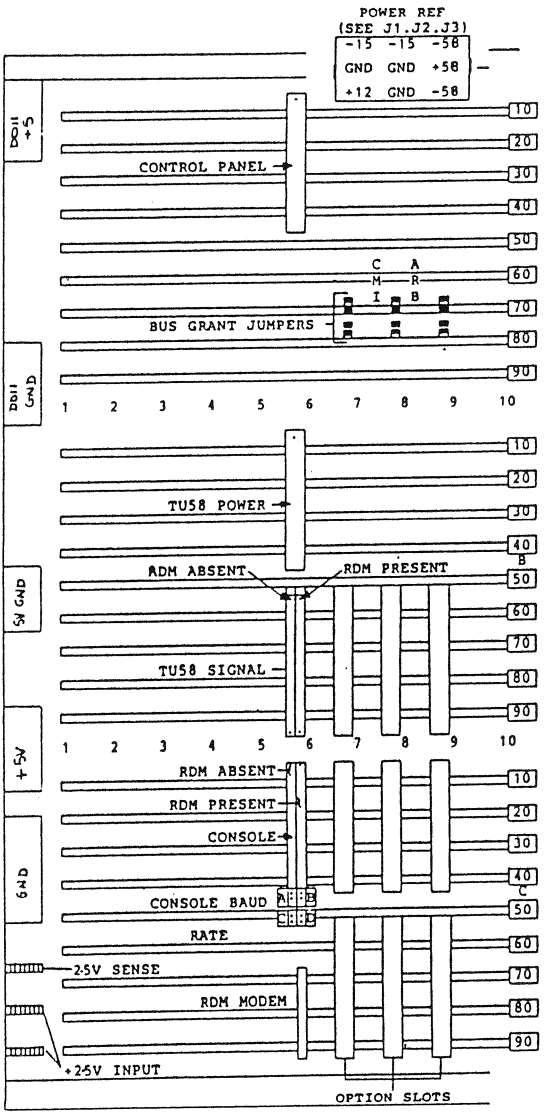
MEMORY BATTERY BACK-UP

H7112 For systems using DEC PSU's only.

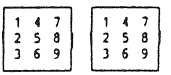
SYSTIME For systems with Farnell PSU's.

3 - SWITCH AND LINK SETTINGS

CPU BACKPLANE



J1- J2-

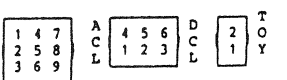


OPTION SLOT BUS GRANTS	
TO SELECT	REMOVE JUMPER
BG 4	AOOX 67
BG 5	AOOX 69
BG 6	AOOX 73
BG 7	AOOX 77
X = SLOT 7 8 9	

TEST POINTS		
RDM 19	MATCH PULSE	C00681
RDM 23	SA CLOCK	C00673
RDM 23	SA ST/SP	C00675
DPM 17	M CLOCK	B00205
DPM 17	BASE CLOCK	A00273
DPM 17	B CLOCK	B00209
MIC 04	MEM STALL	B00210
DPM 17	PHASE 1	A00590

HARDWARE REV LEVEL (SYS ID)	
BIT	PIN#
0	B00456
1	B00455
2	B00454
3	B00453
4	B00450
5	B00449
6	B00448
7	B00446

CONSOLE BAUD RATE				
CON BR				
RATE	A	B	C	D
300	0	0	1	0
600	0	1	1	0
1200	1	1	1	0
2400	0	0	0	1
3600	1	0	0	1
4800	1	1	0	1
9600	1	0	1	1
19200	0	1	1	1
38400	1	1	1	1
PIN #	C00645	C00646	C00649	C00650
JUMPER TO GND	C00643	C00644	C00651	C00652



SYSTIME 256KB MEMORY ARRAY LINKS

The SYSTIME 6700 memory board blank PCB can be filled with either 16K memory chips (256KB board) or 64K memory chips (1MB board). In each case the link settings on the board are different.

The 256KB board is normally used with a standard L0011 memory controller although it will work on the L0016. In both cases the links on the board are as follows:

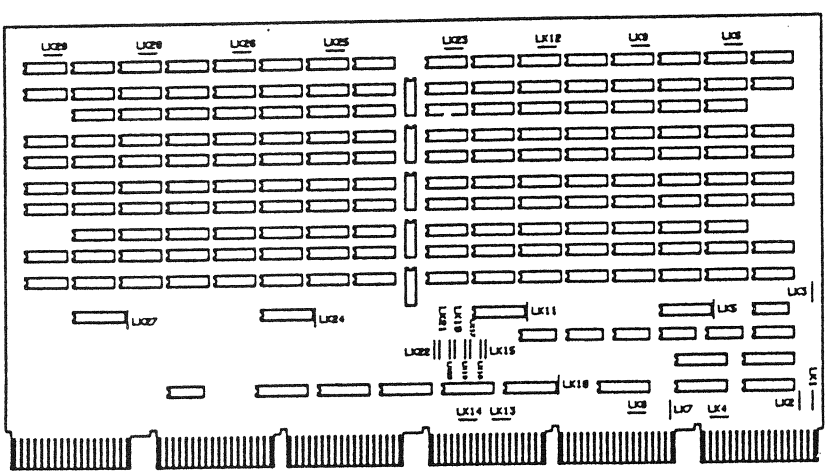
256KB Array on the Standard L0011:

Links IN:

1, 2, 4, 6, 7, 9, 10, 12, 13, 14, 16, 18, 20, 22, 23, 25, 26, 28, 29.

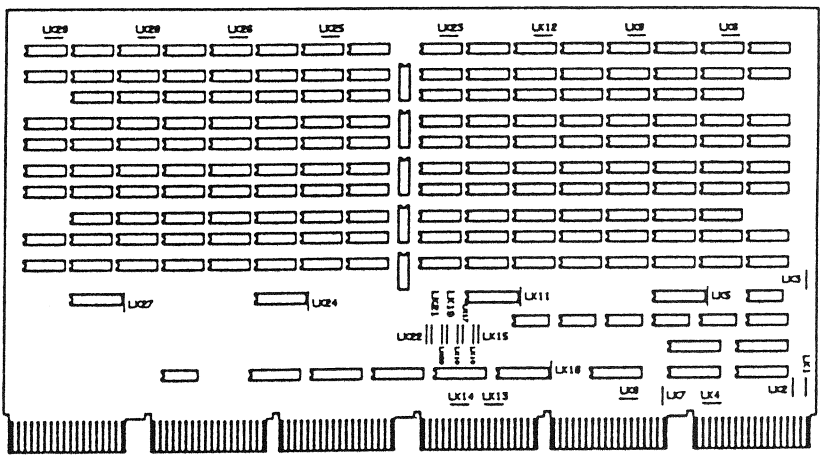
Links OUT:

3, 5, 8, 11, 15, 17, 19, 21, 24, 27.



MK1 MEMORY ARRAY LINKS

This is the Systime 1MB version of the 6700 memory array. It may be used with the modified L0011 or the L0016 memory controller. Using the following link settings a single link (W1), has to be modified depending on the controller.



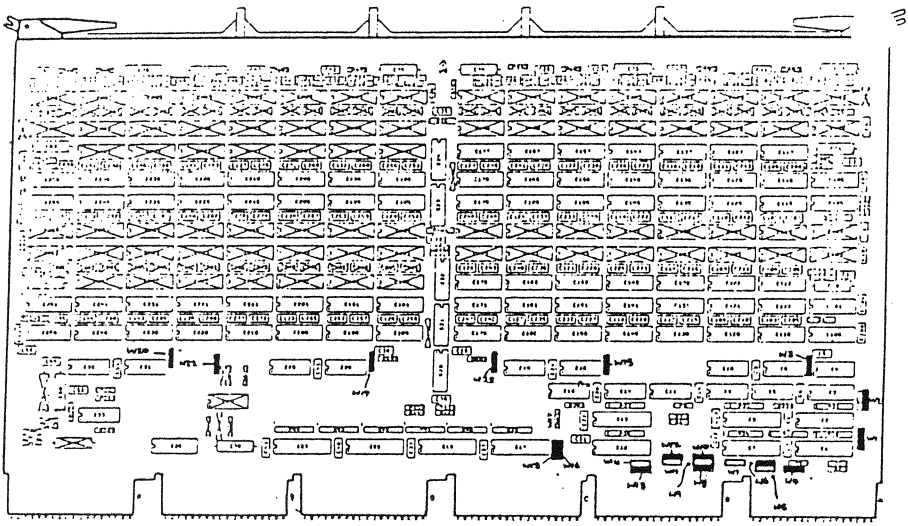
LINK	Modified L0011	L0016
W1	IN	OUT

LINK	Modified L0011 or L0016
2	IN
3	IN*
4	OUT
5	IN
6	OUT
7	IN
8	IN
9	OUT
10	OUT
11	IN
12	OUT
13	IN
14	IN
15	IN

* No battery back-up.
See page 2.B-1 for using battery back-up.

LINK	Modified L0011 or L0016
16	OUT
17	IN
18	OUT
19	IN
20	OUT
21	IN
22	OUT
23	OUT
24	IN
25	OUT
26	OUT
27	IN
28	OUT
29	OUT

M8750 MEMORY ARRAY LINKS



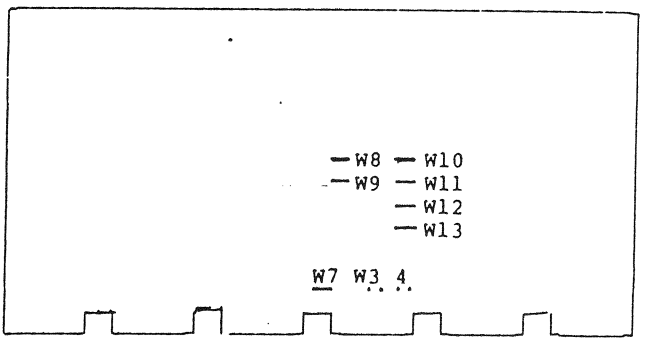
Shaded links should be fitted when installed on L0011

a) Using the M8750 array on the modified L0011 is not recommended, as the L0011 will require further modification.

b) The links that should be IN when using the M8750 array on the L0016 are:-

W2, 3, 4, 6, 8, 10, 12, 13, 15, 16, 18, 19, 20, 22, 25.

NS753 MEMORY ARRAY LINKS



NORMAL LINK SETTINGS

W3 - OUT
W4 - OUT
W7 - OUT
W8 - IN
W9 - IN
W10 - OUT (IN WITH MODIFIED L0011)*
W11 - OUT
W12 - OUT
W13 - OUT

* To use the NS753 on the modified L0011 requires an ECO to be fitted to the L0011 module. This is detailed on page 2.B-2.

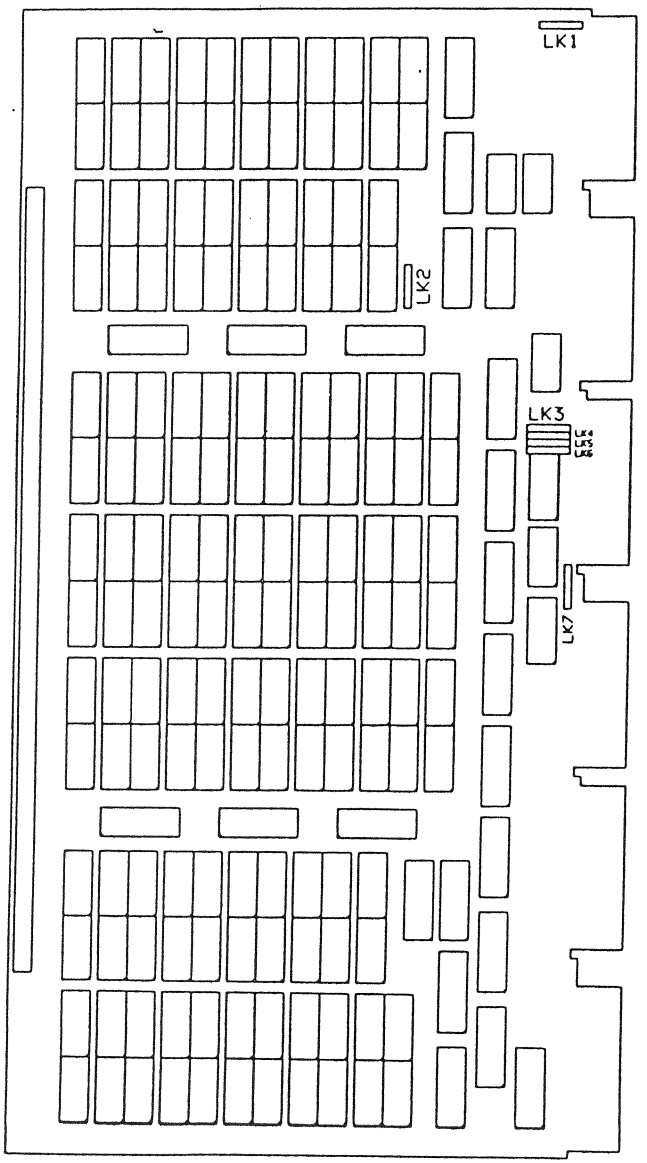
SYSTIME MK2, MEMORY ARRAY LINKS

NORMAL LINK SETTINGS

LK3 - IN FOR MODIFIED L0011
- OUT FOR L0016

LK7 OUT FOR MEMORY BATTERY BACK-UP

LK1 (Normally both IN)



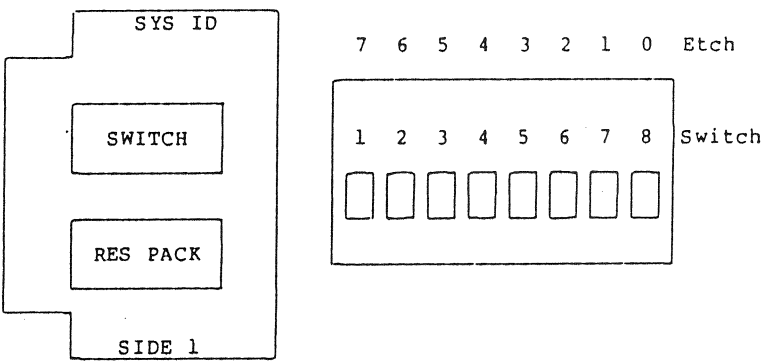
SID REGISTER SWITCH

For example, to set the SID switch pack for a hardware revision level of 70 (HEX) is as follows:

SYS ID	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
SWITCH	ON	OFF	OFF	OFF	ON	ON	ON	ON

N O T E

Use the System ID Register bit positions etched on the board to set the switches. Ignore the numbers stamped on the switch pack.



Install the Backplane Connector Housing in slot 4 so that the blind holes at each end of the connector cover SLOT 4 pins B17 and B18 on the top, and SLOT 4 pins B59 and B60 on the bottom.

4 - SET-UP PROCEDURES

SET-UP PROCEDURES

Note

There are no adjustments on any of the CPU modules. The power supplies are adjustable on systems using the Farnell PSU's. This is detailed on page 2.5-5.

5 - POWER SUPPLY

DEC PSU COMPONENTS

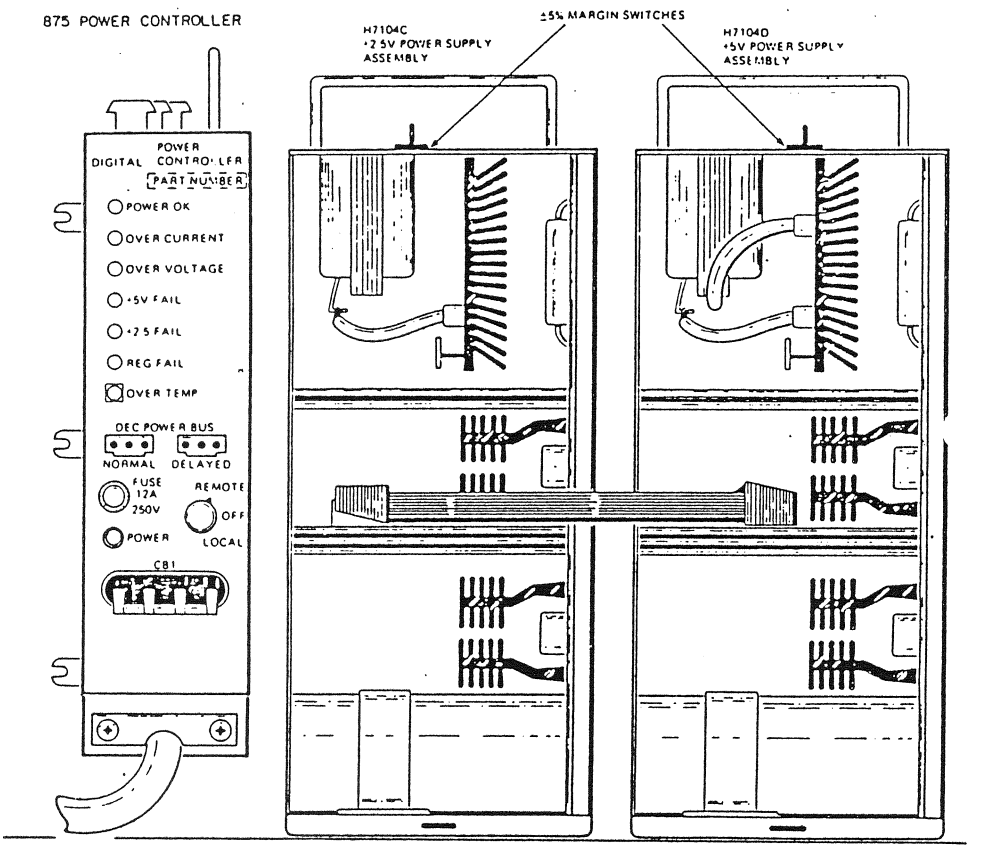
875 SINGLE PHASE POWER CONTROLLER

H7104C	+2.5v 85A POWER SUPPLY	
	+12v Plug-in Regulator 10a	H7102
	+ and - 5v Plug-in Regulator	H7106
	2.5v Control Board	
H7104D	+5V 135A POWER SUPPLY	
	+ and - 15V Plug-in Regulator	H7105
	H7104 Bias Control Card	

NOTE:

The plug-in regulators are dedicated to each power supply.

DEC PSU LAYOUT



DEC PSU FAULT ISOLATION GUIDE

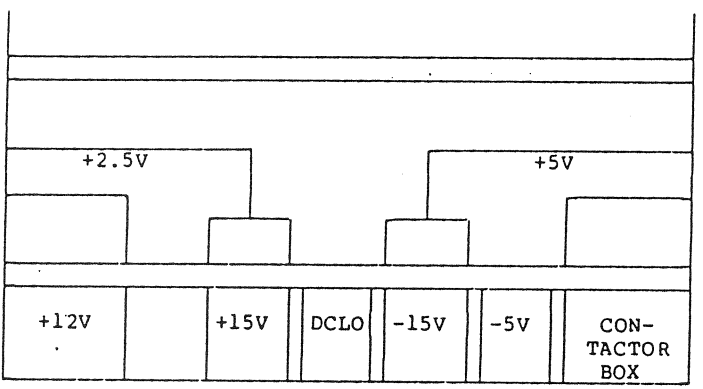
CONTROL PANEL		POWER CONTROLLER										POSSIBLE FAULT AREA(S)
Five Position Keyswitch	CPU State/Power	Power	Circuit Breaker	Remote/Off/Local	Power OK	Over Temp	Over Voltage	Over Current	+5 Fail	+2.5 Fail	Reg Fail	
ON+	OFF	OFF	X	X	X	X	X	X	X	X	X	AC POWER
ON	OFF	ON	OFF	X	X	X	X	X	X	X	X	AC LOAD OR AIR FLOW
ON	OFF	ON	ON	REM	ON	X	X	X	X	X	X	STATUS SIGNAL
ON	OFF	ON	ON	REM	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OVERTEMP, POWER CONTROLLER, POWER SUPPLY,OR CONTROL SIGNAL
ON	OFF	ON	ON	REM	OFF	ON	OFF	OFF	OFF	OFF	OFF	OVERTEMP, POWER SUPPLY
ON	OFF	ON	ON	REM	OFF	OFF	ON	OFF	ON	OFF	ON	+5V POWER SUPPLY
ON	OFF	ON	ON	REM	OFF	OFF	ON	OFF	OFF	ON	ON	+2.5V POWER SUPPLY
ON	OFF	ON	ON	REM	OFF	OFF	OFF	ON	ON	OFF	ON	+5V POWER SUPPLY OR LOAD
ON	OFF	ON	ON	REM	OFF	OFF	OFF	ON	OFF	ON	ON	+2.5V POWER SUPPLY OR LOAD
ON	OFF	ON	ON	REM	OFF	OFF	OFF	OFF	ON	OFF	ON	+5V POWER SUPPLY
ON	OFF	ON	ON	REM	OFF	OFF	OFF	OFF	OFF	ON	ON	+2.5V POWER SUPPLY
ON	OFF	ON	ON	REM	OFF	OFF	OFF	OFF	OFF	OFF	ON	REGULATOR OR LOAD

\+ SET AT ANY POSITION OTHER THAN OFF.
X DON'T CARE CONDITION
++ REM=REMOTE POSITION

FARNELL PSU

Farnell P.S.U.	Qty	Pt. No.
G15-45 (+15,-15)	2	0510590
G6-1P	1	0510592
G12-20	1	0510951
G5-120(ALCO,+5)	1	0510589
G5-120(Modified to +2.5)	1	0510588
D.C. Monitor PCB	1	
Full P.S.U. Kit		0100376

POWER SUPPLY TRAY



NOTE: The 2.5V supply is a modified 5V supply.

FARNELL PSU ADJUSTMENTS

DC Low boards as supplied by Farnell should already be set up for our requirements. If this is not true then the adjustments can be made as follows:

1. All supply voltages must be set as accurately as possible +2.5V, +5V, -5V, +15V and +12V. The Farnell 'DC Low' boards are set to detect voltage variations of 5% i.e if +5V drops to 4.75V then DCLO is asseted on the Unibus.

2. Once the voltages are set up correctly (all PSU's are adjustable) the board should work. If ACLO or DCLO do not work correctly (i.e; either signal is a logic '0' - causing the CPU to halt), then there are one or two things to look at.

A brief explanation of the operation of these boards follows: 'DC Low' board 2 (Farnell board with two IC's on it) monitors -5V, -15V, +15V and +12V on pins 1, 2, 3 and 4 respectively. If these voltage rails are correct then pin 7 should be a logic high. This logic high is passed to 'DC Low' board 1. If this signal is not high then either the voltage levels at the board are incorrect, or the threshold level on the board needs altering. This is achieved by moving the potentiometer on the board. Turn this pot. Until pin 7 goes 'high' - if it does not then the board is duff.

'DC Low' board 1 monitors the +5v and +2.5V. Assuming these are correct (and the DC OK signal from board 2 pin 7 is high), then pin 7 on this board should be high. Again if this signal is not high then either the DC voltage levels are incorrect or the potentiometer needs adjusting.

Before rejecting the unit it is advisable to adjust this pot. Until pin 7 goes high. Once this signal is high the ACLO/DCLO sequence is generated from the mother board.

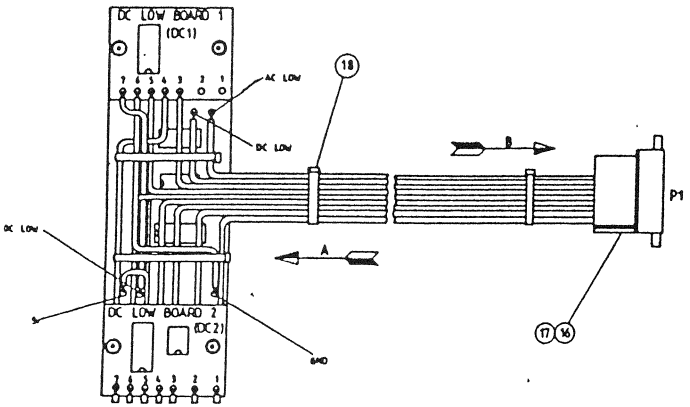
Monitoring the pins in connector P1 will determine whether these signals are generated correctly.

NB: ACLO and DCLO are open collector outputs so they must be connected to the CPU in order to work correctly.

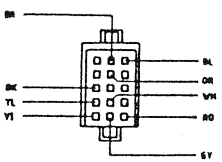
Lastly if the ACLO signal is high yet the DCLO signal is low then there exists an error on the mother board. A recent ECO was issued to cure this problem, and this should be checked. A 560pF capacitor should be soldered between pin 11 and 12 on E2.

If these adjustments still fail then request replacement.

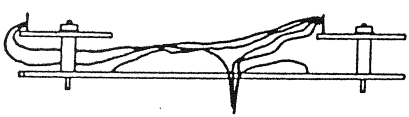
AC/DC LOW BOARD



VIEW IN B

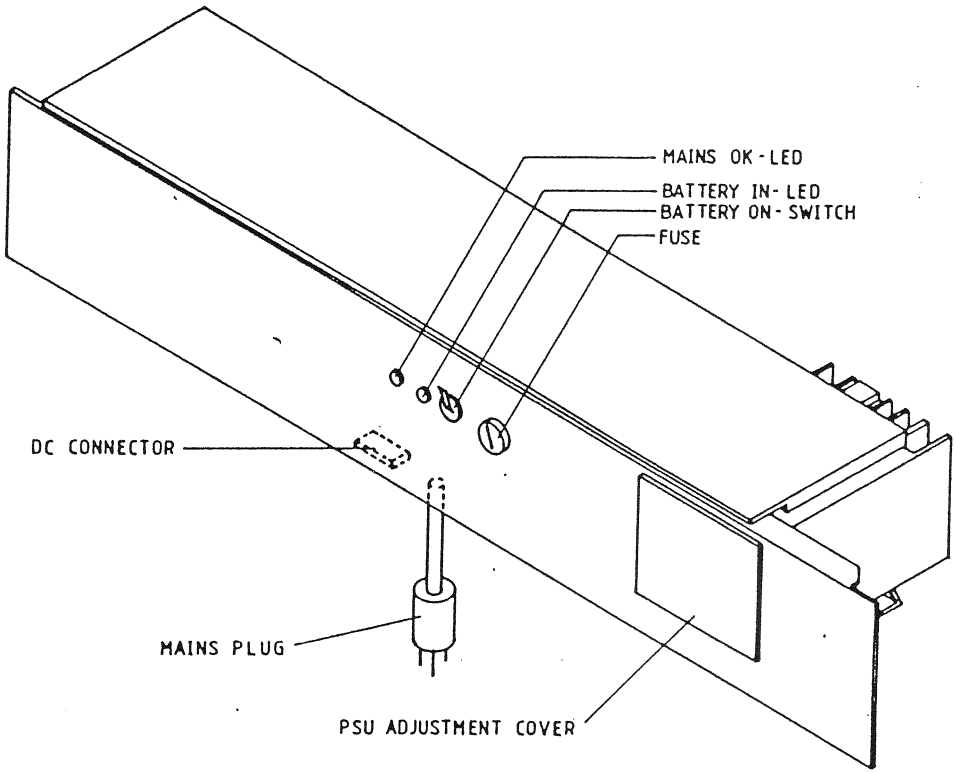


VIEW IN A



	SIGNAL NAME	FROM	TO	COLOUR
ITEM 1	GND	GND (PAD)	DC1 6	BLACK
ITEM 2	GND	DC1 6	DC2 6	ORANGE
ITEM 3	GND	DC2 6	P1 9	BLACK
ITEM 4	DC LOW	DC1 7	DC LOW (PAD)	VIOLET
ITEM 5	DC LOW	DC LOW (PAD)	P1 3	VIOLET
ITEM 6	5v	P1 1	DC1 5	RED
ITEM 7	5v	DC1 5	DC2 5	YELLOW
ITEM 8	5v	DC2 5	5v (PAD)	RED
ITEM 9		DC1 4	DC2 7	RED
ITEM 10	2·5v MONITOR	DC1-3	P1 5	WHITE
ITEM 11	AC LOW	AC LOW (PAD)	P1 6	YELLOW
ITEM 12	+12v MONITOR	DC2 4	P1 11	ORANGE
ITEM 13	+15v MONITOR	DC2 3	P1 2	GREY
ITEM 14	-15v MONITOR	DC2 2	P1 13	BLUE
ITEM 15	-5v MONITOR	DC2 1	P1 14	BROWN

8750 BATTERY BACK-UP UNIT



6 - POWER-UP ACTIONS AND RESPONSE

POWER-UP ACTIONS

The CPU will automatically enter the console I/O mode from power-up without the use of the console storage device.

The front panel switches are tested on power-up and will normally be set to boot VMS which again does not require the console storage device.

To override the switches place the power-up action switch into the halt position before powering on the CPU. The console will respond as shown on page 2.6-2, and await further commands.

TYPICAL RESPONSE

NORMAL POWER-UP

```
%%
00000000 16
>>>
```

This is with Power-up Action Switch at HALT position.

7 - CONSOLE COMMANDS

COMMAND SUMMARY

^P	Enter Console I/O Mode
^U	Ignore current line
H	HALT, reset console defaults
E[/qualifier]_[address]	EXAMINE
D[/qualifier]_[address]_[data]	DEPOSIT
I	INITIALISE CPU and Unibus.
T	TEST the CPU by running Microverify.
S_[address]	START Program (at address if specified).
C	CONTINUE program at address in PC.
B	BOOT (see page 2.8-1)
N	NEXT, executes one instruction

EXAMINE AND DEPOSIT QUALIFIERS

Data Type

/B Byte
/W Word
/L Longword

Address Type

/G GPR 0 to F
/I IPR
/P Physical Memory
/V Virtual Memory

SYMBOLIC ADDRESSES

P Processor Status Longword
* Last Address
+ Next Address

CONSOLE HALT ERROR CODES

Example

```
00010003 06
>>>
```

CONSOLE HALT ERROR CODES

Code	Description
01	Execute TEST console
02	CTRL/P halt or single macro instruction mode
04	Interrupt stack not valid
05	Double bus error halt
06	Halt instruction executed
07	Vector bits<1:0>=3,halt at vector
08	Vector bits<1:0>=2, WCS disabled or not present
0A	Change mode instruction executed on interrupt stack
0B	Change mode instruction executed and vector<1:0>not=0
11	Power up and can't find RPB, action swith at RESTART/HALT
12	Power up and warm start flag false, action switch at RESTART/HALT position
13	Power up and can't find good 64K of memory
14	Power up and booting, but bad or no Boot ROM
15	Power up and cold start flag set during boot subroutine
16	Power up halt, with action switch at HALT position
FF	Microverify test failure

CONSOLE COMMAND ERROR CODES

Example

```
?11

>>>
```

CONSOLE COMMAND ERROR CODES

Code	Description
20	Deposit or Examine of memory failed.(This could mean one of the following has occurred: access violation; translation not valid; bus error; TB parity error; control store parity error.)
11	Illegal access of an IPR
30	APT loading checksum error
33	Attempt to boot from unknown device type (DM, DL, DT, DR)
34	Boot device controller not A, B, C, or D.

BOOT58 COMMANDS

BOOT [<DEVSPEC>]

Boot from the device specified. If no device is specified, boot from the default boot device. This command cannot be used within an indirect command file.

DEPOSIT/<qualifier> <location> <value>

Deposit <value> at the location specified by <location>. The <location> is interpreted according to <qualifier>.

EXAMINE/<qualifier> <location>

Display the contents of <location>, where <location> is interpreted according to <qualifier>.

HELP

Print this text at the console. This command cannot be used within an indirect command file.

LOAD <filespec>[/START:<value>]

Load a file from the boot device into memory starting at the address specified <value>. If no starting location is specified, load the file beginning at the first free location in memory.

START <value>

Initialise CPU and Jump to <value>.

@ <filespec>

Execute command procedure from tape.

NOTE

You can abbreviate all BOOT58 commands to the first character

BOOT58 Command Parameters

<location> <value>!<register>

<value> <number>!<shorthand>

<number> Any nonnegative hexadecimal number

<register> 0..F! PSL

<shorthand> Any one of the following:

* = use last <location> specified
+ = use (last<location>)+1
- = use (last<location>)-1
0 = use contents of (last<location>)

<qualifier> Any one of the following:

P = physical memory address
G = general register
I = internal processor register
W = word, 16 bits
L = longword, 32 bits

<devspec> A device spec of the form: DDCU, where

DD = generic device type (e.g. DB)
C = controller designator (A ! B)
U = unit number (0..9)

<filespec> A legal RT-11 filename of the form: name.typ where:

name = any alphanumeric string of not more than 6 characters.

typ = any alphanumeric string of not more than 3 characters. A null typ is acceptable.

8 - BOOTSTRAP

BOOTSTRAP PROCEDURES

USING OPERATOR CONTROL PANEL SWITCHES

a) Select the device to boot using the BOOT DEVICE switch. The positions correspond to the following devices:

   A = TU58
   B = System Disk
   C = Spare
   D = Spare

b) Place the power on action switch in the BOOT position.

c) Ready the disk drive to be booted.

d) Power the system on, or if already on press the RESET button.

USING CONSOLE COMMANDS

a) Place the power on action switch in the HALT position.

b) Power on, or press the RESET switch, if the system is not in the console I/O mode. In console I/O mode the console prints >>>.

c) Enter the BOOT command as shown below:

B<cr>	This boots the device selected by the BOOT DEVICE SWITCH.
or:	
B_[dev]<cr>	This boots the device whose code is specified.

The boot device codes are as follows:

DDA0 = TU58
SIAn = Disks on SI 9400 Controller
UMAn = Disks on Emulex SC21/31 Controller
DBAn = Disks on Emulex SC750 Controller

n = Logical unit number of the drive.

CONVERSATIONAL BOOT

B/1_[dev]<cr>

or:

B/1<cr> (using the boot device switch)

DIAGNOSTIC BOOT

To boot diagnostic supervisor from a VMS disk:

B/10 [dev]<cr>

BOOTSTRAP ROMS

DEVICE	PART NO	ASCII CODE	DEVICE CODE
TU58	905A9	44 44	DD
DISKS ON SC21/31	287B	4D 55	UM
DISKS ON UNIBUS S.I. 9400 ..	8919B	49 53	SI
DISKS ON SC750	497B	42 44	DB

BOOTSTRAP EXAMPLE

```
%%

00000000 16

>>>B DBA0
%%

     VAX/VMS Version V4.1 26-APR-1985 16:21


%OPCOM 6-MAR-1985 11:58:05.44, Logfile initialised by
       operator OPA0:
       Logfile is SYS$MANAGER:OPERATOR.LOG

%PURGE-I-NOFILPURG, no files purged for
       SYS$SYSROOT:[[SYSERR]*.*;

Login Quotas - Interactive Limit = 64, current
interactive value = 0

SYSTEM Job terminated at 6-MAY-1985 11:59:09.23
```

9 - DIAGNOSTIC TESTING

MICROVERIFY

Microverify is a microcode based set of test routines which execute a basic sanity check on the DPM and MIC modules of the 750.

The routine uses a "%" character to indicate start of run and end of successful run.

If the microverify sequence fails, an error indication is provided, by printing a character indicating the failing test group. The value printed for the PC indicates the failing test within the identified group.

The example below shows the console response on a Microverify failure.

```
%F
00000062 FF.
```

This indicates a microverify failure on the "MTEMP EXPLICIT ADDRESS TEST".

The test is indicated by printed PC+2.

Microverify is invoked on:

Power up, prior to boot sequence execution and by a specific console I/O command.

MICROVERIFY CODES

Code	PC+2	Test Name/Error Message
'@'		RBUS, WBUS TEST
	000	BAD BIT IN DREG OR SUPPORT
	001	BAD BIT IN RBUS OR WBUS
'C'		MBUS TEST
	031	BAD BIT IN QREG
	033	BAD BIT IN MBUS
'E'		SCRATCH PAD BIT TEST
	051	ERROR CLEARING RTEMP
	052	ERROR FILLING RTEMP WITH ONES
	054	ERROR CLEARING GPR
	057	ERROR FILLING GPR WITH ONES
	058	ERROR CLEARING IPR
	05B	ERROR FILLING IPR WITH ONES
	05D	ERROR CLEARING MTEMP
	05E	ERROR FILLING MTEMP WITH ONES
'F'		MTEMP EXPLICIT ADDRESS TEST
	061	ERROR ADDRESSING MTEMPO
	062	ERROR ADDRESSING MTEMPl
	064	ERROR ADDRESSING MTEMP2
	067	ERROR ADDRESSING MTEMP4
	068	ERROR ADDRESSING MTEMP8
'I'		RTEMP EXPLICIT ADDRESS TEST
	091	ERROR ADDRESSING RTEMP0
	092	ERROR ADDRESSING RTEMPl
	094	ERROR ADDRESSING RTEMP2
	097	ERROR ADDRESSING RTEMP4
	098	ERROR ADDRESSING RTEMP8
'J'		IPR EXPLICIT ADDRESS TEST
	0A1	ERROR ADDRESSING IPRO
	0A2	ERROR ADDRESSING IPRl
	0A4	ERROR ADDRESSING IPR2
	0A7	ERROR ADDRESSING IPR4
	0A8	ERROR ADDRESSING IPR8
'L'		GPR EXPLICIT ADDRESS TEST
	0C1	ERROR ADDRESSING R0
	0C2	ERROR ADDRESSING Rl
	0C4	ERROR ADDRESSING R2
	0C7	ERROR ADDRESSING R4
	0C8	ERROR ADDRESSING R8
	0CE	ERROR ADDRESSING DUAL PORT

MICROVERIFY CODES (Cont)

Code	PC+2	Test Name/Error Message
'O'		XB/IR/OSR BIT TEST
	0F1	ERROR IN XB<31:0>
	0F2	ERROR IN XB<63:32>
	0F4	ERROR IN IR
	0F7	ERROR IN OSR
'Q'		SOURCE XB PC INCREMENT TEST
	111	ERROR SOURCING ONE BYTE FROM XB
	112	ERROR SOURCING 2 BYTES FROM XB XB OR INCREMENTING PC BY 1
	114	ERROR SOURCING AN UNALIGNED LONGWORD OR INC PC BY 2
	117	ERROR INCREMENTING PC BY 4
'R'		RNUM/DSIZE TEST
	121	ERROR READING DSIZE ROM OPERAND 1
	122	ERROR LOADING/READING RNUM
	124	ERROR READING SIZE ROM OPERAND 2
	127	ERROR LOADING/READING RNUM
	128	ERROR READING DSIZE ROM OPERAND 3
	12B	ERROR LOADING/READING RNUM
	12D	ERROR READING DSIZE ROM OPERAND 4
	12E	ERROR LOADING/READING RNUM
'T'		RNUM/DSIZE TEST CONTINUED
	141	ERROR READING DSIZE ROM OPERAND 5
	142	ERROR LOADING/READING RNUM
	144	ERROR READING DSIZE ROM OPERAND 6
'X'		CACHE PARITY ERROR TEST
	181	FAILED TO GET CACHE PARITY ERROR
	182	BAD MACHINE CHECK ERROR SUMMARY REGISTER
	184	BAD CACHE ERROR REGISTER
'['		TB PARITY ERROR TEST
	1B1	FAILED TO GET GROUP 0 TB PARITY ERROR
	1B2	BAD TB GROUP PARITY ERROR REGISTER
	1B4	BAD MACHINE CHECK ERROR SUMMARY REGISTER
	1B7	FAILED TO GET GROUP 1 TB PARITY ERROR
	1B8	BAD TB GROUP PARITY ERROR REGISTER
	1BB	BAD MACHINE CHECK ERROR SUMMARY REGISTER
']'		CONTROL STORE PARITY ERROR TEST
	1D1	FAILED TO GET CONTROL STORE PARITY ERROR
	1D2	ERROR IN CONTROL STORE PARITY ERROR
'^'		CACHE TEST
	1E1	ERROR FILLING CACHE WITH ONES LOCATION NOT INITIALLY = 0
	1E2	ERROR FILLING CACHE WITH ONES UNABLE TO WRITE ONES

MACRODIAGNOSTIC COMMAND SUMMARY

SET LOAD

This establishes the device from which diagnostics are to be loaded.

SET LOAD CSA0:

This will change the default load device from disk to TU58 on the 8750.

SHOW LOAD

This command displays the current load device and directory from which diagnostics will be loaded using the LOAD command.

LOAD

This command loads programmes from the current load device into memory,

For example: LOAD EVTAA<cr>.

ATTACH

This makes known to diagnostic supervisor the devices that are to be currently tested.

For example: DS>ATT DW750 CMI DW0.

SELECT

After specifying the testable hardware, the ones to be tested at the present time must be selected eg:

```
DS> ATT TSO4 DWO MSAO
DS> ATT RMO5 RHO DRAO
DS> SELECT DRAO (alternatively SELECT ALL)
```

DESELECT

Used to make all or some devices unavailable to testing.

START

Used after LOAD command to initiate program; other options are:

DS>START/SECTION:

DS>START/SECTION:XXXX/TEST:6:12 (starts program execution in section xxxx of the diagnostic and performs tests 6 to 12 within that section)

DS>START/TEST:10 (start program execution at test 10 and continues to end of tests)

DS>START/TEST:5/SUBTEST:6 (starts execution at test 5 and runs subtests 1,2,3,4,5,6.)

DS>START/PASS:0 (execute program indefinitely)

RUN

Loads and starts the program.

SET DEFAULT

Sets data length or radix(byte/word/longword, hex/decimal).

SET FLAGS/CLEAR FLAGS

Certain programs use flags to control program flow, error logging etc. The help section of the diagnostics usually list the flags that can be set. Certain flags are always available as follows:

IE1 Inhibit error messages at level 1 (inhibits all error messages except those forced by program)

IE2 Inhibit error messages at level 2 (prints header only)

IE3 Inhibit error messages at level 3(header and basic information only printed)

IES Inhibit summary report.

QUICK Quick verify test(depends on program)

TRACE Reports execution of each test.

OPER Indicates that operator is present, if not set the supervisor ensures that program is completed without intervention.

PROMPT Display long dialogue, shows limits and faults etc.

ALL Set all flags in this list.

SET/CLEAR event flags (depends on program running but controls program flow).

SUMMARY

Invokes the program's summary report code section which prints statistical reports.

ABORT

Passes control to the clean up code, then returns control to DS> which then entes a wait state. The operator may then enter any command except CONTINUE.

SHOW EVENT FLAGS

Shows event flags currently set.

```
DS>SHOW EVENT FLAGS
EVENT FLAGS SET: 15, 9, 1
```

LOADING DIANOSTIC SUPERVISOR

STAND ALONE FROM TU58 CARTRIDGES

a) Power-on the system with the power-on action in the HALT position.

b) Insert the TU58 containing ECSAA.EXE, (refer to following lists to locate the correct cartridge).

c) Type:

```
B DDA0
```

This will load and run diagnostic supervisor, which takes approximately 3 minutes.

STAND ALONE FROM VMS DISK

Currently this only works on SC750 Disks.

a) Ready VMS Disk for use, write protect drive as an extra precaution.

b) Type:

```
B/10 DBAn      (n is the unit number)
```

UNDER VMS

a) Bring up VMS as normal.

b) Log into the Field Service account, type:

```
FIELD
SERVICE
```

c) Type:

```
RUN ECSAA
```

DIAGNOSTIC DISTRIBUTION

There are currently two revisions of diagnostic cartridge distributions for the 8750 system, revision A and revision B. Revision B was introduced in January 1984.

REVISION A CARTRIDGES

TU58 5 - CACHE, TB, MEMORY

ECKAL - CACHE/TB DIAGNOSTIC
ECKAM - MEMORY DIAGNOSTIC
ECKAX - SPECIFIC CPU CLUSTER EXERCISER

TU58 6 - RH750, DW750

ECSAA - DIAGNOSTIC SUPERVISOR
ECCAA - RH750 DIAGNOSTIC(DEC ONLY)
ECCBA - DW750 DIAGNOSTIC
EVDAA - SZ-11 8-LINE DIAGNOSTIC

TU58 7 - VAX 11 INSTRUCTION EXERCISER

EVKAB - ARCHITECTURAL INSTRUCTION
EVKAC - FLOATING POINT INSRUCTION
EVKAD - COMPATIBILITY MODE
EVKAE - PRIVILEGED ARCHITECTURE INSTRUCTION

TU58 9 - CR/DISK USER MODE

EVAAA - LINE PRINTER DIAGNOSTIC
EVABA - CARD READER DIAGNOSTIC
EVRAA - DISK AND TU58 RELIABILITY DIAGNOSTIC
EVRAC - VAX DISK FORMATTER
EVTAA - LOCAL TERMINAL DIAGNOSTIC
EVTBA - MULTI-TERMINAL DIAGNOSTIC

REVISION B CARTRIDGES

8750 TAPE 1

ECSAA.EXE - DIAGNOSTIC SUPERVISOR
EVSAA.HLP - HELP FILE FOR ABOVE

8750 TAPE 2

ECK1M.EXE - MEMORY DIAGNOSTIC FOR 1MB SYSTEMS
ECKAL.EXE - TRANSLATION BUFFER/CACHE TEST
ECKAM.EXE - MEMORY DIAGNOSTIC FOR 1/4MB SYSTEMS
ECKAX.EXE - CLUSTER EXERCISER

8750 TAPE 3

EVDBA.EXE - DMC11 DIAGNOSTIC REPAIR LEVEL
EVDBB.EXE - DMC11 EXERCISER DIAGNOSTIC
EVDMA.EXE - DMR11 DIAGNOSTIC REPAIR LEVEL
EVDXA.EXE - DMR11 COMM.MICRO CPU REPAIR LEVEL
EVKAA.EXE - HARDCORE INSTRUCTION EXERCISER

8750 TAPE 4

EVKAB.EXE - ARCHITECTURAL INSTRUCTION TEST
EVKAC.EXE - FLOATING POINT INSTRUCTION TEST
EVKAD.EXE - COMPATABILITY MODE TESTS
EVKAE.EXE - PRIVILEGED ARCHITECTURE INSTRUCTIONS

8750 TAPE 5

ECCBA.EXE - UNIBUS ADAPTER DIAGNOSTIC
ESTAA.EXE - LOCAL TERMINAL DIAGNOSTIC
EVAAA.EXE - LINE PRINTER DIAGNOSTIC
EVDAA.EXE - DZ11 ASYNCHRONOUS MUX TESTS
EVMAA.EXE - TE16/TU77/TS11 DIAGNOSTICS
EVQTS.EXE - OFFLINE DRIVE FOR TS11
EVTAA.EXE - TU10 COMPATABLE TESTS(D/DATA, S/E LABS)

8750 TAPE 6 (EMULEX REV H DIAGNOSTICS)

ECS11.730)
ECS11.750)
ECS11.780)
ECS21.730)
ECS21.750)- ATTACH COMMAND FILES
ECS21.780)
ESC21.730)
ESC21.750)
ESC21.780)
ECS11.EXE - CS11 CONTROLLER DIAGNOSTIC
ESC21.EXE - SC21 CONTROLLER DIAGNOSTIC
ETC11.EXE - TC11 CONTROLLER DIAGNOSTIC
EDSKF.EXE - DISK FORMATTER DIAGNOSTIC
EDSKR.EXE - DISK RELIABILITY DIAGNOSTIC
EVQRB.EXE - OFFLINE RP DRIVER
EVQRR.EXE - OFFLINE RM DRIVER
EVQUM.EXE - OFFLINE SC21/SC31 DRIVER
ECS11.HLP)
ESC21.HLP)- HELP FILES FOR EMULEX DIAGNOSTICS
ETC11.HLP)

8750 TAPE 7 (EMULEX REV K DRIVERS)

UM-BOOTFILES

DRIVER PATCHES
DRIVERS FOR THE EMULEX DEVICES

EXAMPLES OF ATTACH STRINGS

The following is an example of the more common attach strings used on the 11/750.

```
DS> ATT KA750 CMI KA0 NO NO YES 0 0
DS> ATT DW750 CMI DW0
DS> ATT LP11 DW0 LP0 777514 200 5
DS> ATT DZ11 DW0 TTA 760100 300 5 EIA
DS> ATT TS11 DW0 MSA0 772520 224 5
DS> ATT TS04 DW0 MSA0 772520 224 5
DS> SEL ALL
DS> SET TRACE
```

EMULEX SC750:

```
DS> LOAD <program>
DS> ATT RH750 CMI RH0 5
DS> ATT RM RH0 DRA0
DS> ATT RM RH0 DRA1
DS>
```

EMULEX SC21 or SC31

See page 2.9-22

S.I. 9400 WITH UNIBUS INTERFACE

(This can only be tested under VMS)

See page 2.9-19 .

MACRODIAGNOSTIC PROGRAMS

This is a list of the more common diagnostics used on the 11/750 system:

DIAGNOSTIC	STAND ALONE ONLY	DESCRIPTION
ECSAA	-	DIAGNOSTIC SUPERVISOR
EVKAA	YES	HARDCORE INSTRUCTION
ECKAL	YES	CACHE/TB DIAGNOSTIC
EVKAB	NO	ARCHITECTURAL INSTRUCTION
EVKAC	NO	FLOATING POINT INSRUCTION
EVKAD	NO	COMPATABILITY MODE INSRUCTION
EVKAE	YES	PRIVILEGED ARCHITECTURE INSTRUCTION
ECKAX	YES	SPECIFIC CPU CLUSTER EXERCISER
ECKAM	YES	MEMORY (256KB ARRAY)
ECK1M	YES	MEMORY(1MB ARRAY)
ECCBA	YES	UNIBUS ADAPTER DW750
EVDAA	YES	DZ11-8 LINE ASYNC MUX TEST
EVAAA	VMS ONLY	LINE PRINTER DIAGNOSTICS
ESTAA	VMS ONLY	LOCAL TERMINAL DIAGNOSTIC
EVTAA	NO	MAGTAPE RELIABILITY DIAGNOSTIC
EVMAA	NO	TS11 RELIABILITY DIAGNOSTIC
EVTBA	VMS ONLY	MULTITERMINAL DIAGNOSTIC
EVRAC	NO	DEC RM DISK FORMATTER
EVRDB	YES	DEC RM DISK EXERCISER
EVRAA	NO	DEC RM DISK RELIABILITY
ESC21	YES	EMULEX SC21/SC31 CONTROLLER DIAGNOSTIC
EDSKF	NO	EMULEX DISK FORMATTER PROGRAM
EDSKR	NO	EMULEX DISK RELIABILITY PROGRAM
SIRAC	VMS ONLY	S.I. DISK FORMATTER
SIRAA	VMS ONLY	S.I. DISK RELIABILITY

EVKAA, ECKAL

```
      >>>B DDAO
%%

EVKAA V7.2 Hardcore Instruction Test
Hit any key to continue
EVKAA DONE!
EVKAA DONE!
EVKAA DONE!
EVKAA DONE!
EVKAA DONE!
V7.2 Pass £1 (x)
V7.2 Pass 10 (x)
V7.2 Pass 32 (x)
V7.2 Pass 38 (x)
V7.2 Pass 64 (x)
00004574  02
>>>
```

```
      >>>B DDAO
%%

End of Pass ECKAL V3.2
End of Pass ECKAL-V3.2
End of Pass ECKAL-V3.2
End of Pass ECKAL-V3.2
End of Pass ECKAL-V3.2
0000461C 02
>>>
```

ECCBA

```
DS> ATT DW750 CMI DW0
DS> SEL DW0
DS> SET TRACE
DS> R ECCBA

.. Program:    ECCBA-REV.  1.3      VAX 11/750 (UBI),  DW750
   Diagnostic, Rev  1.3, 32 tests, at 00:01:09.92.

Testing:  _DW0

Test 1:   Control and Status Register Test
Test 2:   Map Data Bus Test
Test 3:   Map Chip Select Test
Test 4:   Map Address Bus Test
Test 5:   Map Entry Test
Test 6:   CPU Read/Write Test
Test 7:   CMI to Unibus Addressing Test
Test 8:   Unibus to CMI Addressing Test
Test 9:   Data Path Select Test
Test 10:  Direct Data Path DATI Test
Test 11:  Direct Data Path DATIP/DATO Test
Test 12:  Direct Data Path DATOB Test
Test 13:  Buffered Address Register Test
Test 14:  Buffered Data Path DATI Test
Test 15:  Buffered Data Path DATIP Test
Test 16:  Buffered Data Path DATO Test
Test 17:  Buffered Data Path DATOB Test
Test 18:  Buffered Data Path Autopurse Test
Test 19:  Byte Offset DATI Test
Test 20:  Byte Offset DATIP/DATO Test
Test 21:  Byte Offset DDP DATO Test
Test 22:  Byte Offset BDP DATO Test
Test 23:  Byte Offset DDP DATOB Test
Test 24:  Byte Offset BDP DATOB Test
Test 25:  Map Entry Functional Test
Test 26:  CSR Status Bit Test
Test 27:  UET CSR1 Interrupt Test
Test 28:  UET CSR2 Interrupt Test [aborted]
Test 29:  UET CSR1/CSR2 ACLOW Test [aborted]
Test 30:  Map Invalid Test
Test 31:  UET PB Bit Test
Test 32:  UBE Block Transfer Test
NO UBES SELECTED, SKIPPING TEST
.. End of run.  0 errors detected.  Past count: 1.
   Time:  1-JAN-1981 00:01
```

EVKAB

```
DIAGNOSTIC SUPERVISOR.  ZZ-ECSAA-6.5-22B 1-JAN-1981 00:00:00
DS> ATT KA750 CMI KA0 N N Y 0 1 - FPA installed
DS> ATT DW750 CMI DW0
DS> SEL ALL
DS> SET TRACE
DS> R EVKAB

.. Program:  VAX Basic Instructions Exerciser, ZZ-EVKAB, Rev
   2.6, 10 tests, at 00:00:26.55.

Testing: KA0:

Accelerator type 1 is disabled.
Test 1:   Integer Arithmetic and Local Instructions
Test 2:   Variable Length Bit Field Instructions
Test 3:   Basic Branch Instructions
Test 4:   Single Bit Field Control Instructions
Test 5:   Integer Arithmetic Control Instructions
Test 6:   INDEX Instruction
Test 7:   Queue Instructions
Test 8:   Character String Instructions
Test 9:   Decimal String Instructions
Test 10:  Edit Instruction
Accelerator type 1 is enabled.
Test 1:   Integer Arithmetic and Logical Instructions
Test 2:   Variable Length Bit Field Instructions
Test 3:   Basic Branch Instructions
Test 4:   Single Bit Field Control Instructions
Test 5:   Integer Arithmetic Control Instructions
Test 6:   INDEX Instruction
Test 7:   Queue Instructions
Test 8:   Character String Instructions
Test 9:   Decimal String Instructions
Test 10:  Edit Instruction
.. End of run.  0 errors detected.  Pass count: 1.
   Time:  1-JAN-1981 00:01
DS>
```

NOTE Revision 3 of this diagnostic has changed the print out.

EVKAC, EVKAD AND EVKAE

```
DS> R EVKAC

.. Program:   VAX Floating Point Instructions Exerciser,
   ZZ-EVKAC, Rev 4.1, 4 tests, at 00:01:15.26.

Testing:  _KA0

Test 1:   Single Precision Floating Point Instructions
Test 2:   Double Precision Floating Point Instructions
Test 3:   Extended Range Dougle Precision Floating Point
          Instructions
Test 4:   Extended Range Quadruple Precision Floating Point
          Instructions
.. End of run.  0 errors detected.  Pass Count: 1.
   Time:  1-JAN-1981 00:01

          (Revision 5 has changed).


DS> R EVKAD

.. Program:  VAX Compatibility Mode Instructions Exerciser,
   EVKAD, Rev 1.2, 4 tests, at 00:01:21.03.

Testing:  _KA0

Test 1:   Compatibility Mode ENTRY and EXIT Test
Test 2:   Compatibility Mode SINGLE OPERAND Instructions
Test 3:   Compatibility Mode DOUBLE OPERAND Instructions
Test 4:   Compatibility Mode PROGRAM CONTROL Instructions
.. End of run.  0 errors detected.  Pass Count: 1.
   Time:  1-JAN-1981 00:01


DS> R EVKAE

.. Program:  VAX Privileged Architecture Exerciser,
   EVKAE, Rev 2, 11 tests, at 00:00:22.73.

Testing:  _KA0

Test 1:   Interrupt Test
Test 2:   Exception Test
Test 3:   REI Instruction Test
Test 4:   Change Mode Instructions Test
Test 5:   Processor Register Instructions
Test 6:   Interval Timer
Test 7:   MEMORY MANAGEMENT
Test 8:   KERNEL STACK NOT VALID
Test 9:   CHMx TO WRITE PROTECTED STACKS
Test 10:  PROBE Instruction Test
Test 11:  Process Context Switching
.. End of run.  0 errors detected.  Pass Count: 1.
   Time:  1-JAN-1981 00:01
DS>
```

ECKAX

```
DS> ATT KA750 CMI KA0 NO NO YES 0 0
DS> SEL KA0
DS> SET TRACE
DS> RUN ECKAX

.. Program:  VAX 11,750 Specific CPU Cluster Exerciser -
   ZZ-ECKAX-3.3, Rev 5.1.  14 tests, at 00:00:36.19.

Testing:  _KA0

Test 1:    Reserved Processor Registers
Test 6:    WCS Memory test
Exiting WCS test, WCS last address = 0

Test 7:    WCS Execution Test
Exiting WCS test, WCS last address = 0

Test 8:    Machine Check Exceptions and Interrupts
Exiting WCS parity subtest, WCS last address = 0

Test 9:    TU58 EXERCISER
Test 10:   TU58 EXERCISER READ/WRITE
The TU58 tape cartridge is not recognised as a scratch tape,
do you wish to overwrite the tape?  [(No), Yes] NO

TEST 11:   TU58 EXERCISER (WITH MRSP)
TEST 12:   TU58 EXERCISER READ/WRITE (WITH MRSP)

The TU58 tape cartridge is not recognised as a scratch tape,
do you wish to overwrite the tape? [(No), Yes] NO

TEST 13:   PCS Memory Test
TEST 14:   PCS Execution Test

.. End of run.  0 errors detected.  Pass Count: 1.
   Time:  1-JAN-1984 00:01
```

ECK1M

```
DS> RUN ECK1M

.. Program:    ECKAM  -  Rev.  2.3 MS750 Diagnostic, Revision
   2.16, 12 tests at 00:26:57.33.

Test 1:   Memory Map Verification Test
Memory Map Valid:  00000003(X) for:  L0011 Controller
Slot[0] is a 1024KB array
Slot[1] is empty
Slot[2] is empty
Slot[3] is empty
Slot[4] is empty
Slot[5] is empty
Slot[6] is empty
Slot[7] is empty
Test 2:   Data Bus Test
Test 3:   Row Select Bus Test
Test 4:   Address Bus Test
Test 5:   ECC Logic Test
Test 6:   CSRO Test
Test 7:   Bootstrap ROM Test
ROM NUMBER:  A   Device Type:  SI
ROM NUMBER:  B   Device Type:  DD
ROM NUMBER:  C   Device Type:  DB
Test 8:   CPU Lost Error Test
Test 9:   CPU XB Error Bit Test
Test 10:  Moving Inversions Test [aborted]
Array [0] Single Bit Errors:
  Row 1 - 0
  Row 2 - 0
  Row 3 - 0
Test 12:  Memory Quick Verify Test
Number of correctable erros = 1

Address (Page)      Bit Number/Syndrome
--------------      -------------------
  00024600(x)         15(D) (Data Bit)
```

```
EVKAM

          Welcome to VAX/VMS version V3.0

$R ECSAA

DIAGNOSTIC SUPERVISOR.  ZZ-ECSAA- 6.10-323 22-NOV-1983
09:33:28

DS>SET EV FL 1,10,11,12
DS>R EVKAM

.. Program:  VAX Memory user mode test, ZZ-EVKAM,
   Revision 1.1, 2 tests, at 09:33:46.70

*************************** WARNING ***************************
 This diagnostic disables cache - system performance will be
                          affected
*************************** WARNING ***************************

This system is a VAX-11/750

Slot 0 contains a 1024 Kbyte module
Slot 1 contains a 1024 Kbyte module
Slot 2 contains a 1024 Kbyte module
Slot 3 contains a 1024 Kbyte module
Slot 4 contains a 1024 Kbyte module
Slot 5 contains a 1024 Kbyte module
Slot 6 contains a 1024 Kbyte module
No memory present in slot 7
Total memory found -> -> -> 7168 Kbytes.
Beginning address is on the 0 Kbyte boundary.
Memory read test begun at 09:34:10.95
Testing controller number:  0
                    1024 Kbytes tested at 09:34:21.34
                    2048 Kbytes tested at 09:34:30.69
                    3072 Kbytes tested at 09:34:40.03
                    4096 Kbytes tested at 09:34:49.36
                    5120 Kbytes tested at 09:34:58.70
                    6144 Kbytes tested at 09:35:08.04
                    7168 Kbytes tested at 09:35:17.38

Memory read test done at 09:35:18.83
Memory error summary as of 09:35:20.28
Controller number 0

Array #     Correctable Errors     Uncorrectable Errors     Unknown Errors
   0                0                      0                      0
   1                0                      0                      0
   2                0                      0                      0
   3                0                      0                      0
   4                0                      0                      0
   5                0                      0                      0
   6                0                      0                      0

.. End of run.  0 errors detected.  Pass Count is 1,
   Time is 22-NOV-1983 09:35:40.59
```

S.I. DISK DIAGNOSTICS

Two of the 8780 S.I. Disk Subsystem Diagnostics may be run on the 8750. They are:

SIRAA - Disk Reliability Diagnostic
SIRAC - Disk Formatter Diagnostic

They have to be run under VMS to utilise the S.I. driver.

SIRAA must be run first in all cases to correct a problem with the drive type, (as seen by the diagnostic). SIRAA will report an illegal drive type error, but allows the program to continue.

After 'yes' has been entered to the question:

Do you wish to override the protection check?

SIRAA may be terminated and SIRAC can be run without error, (SIRAA requires a formatted disk pack).

If SIRAC is run first it will always fail.

Examples of SIRAA and SIRAC on the 8750 are included here.

The drive to be tested must be attached as shown below. The attach string given will only work on revision 6.5 or less of the diagnostic supervisor:

```
DS> ATT DW750 CMI DW0

DS> ATT RM03 DW0 SIA1

DS> SEL ALL
```

SIRAA DISK RELIABILITY

```
Username:  FIELD
Password:
           Welcome to VAX/VMS Version V2.3
$ R ECSAA
DIAGNOSTIC SUPERVISOR.  ZZ-ECSAA-6.1-175 19-MAY-1982 18:25:46
DS>
DS> ATT DW750 CMI DW0
DS> ATT RM03 DW0 SIA1
DS> SEL SIA1
DS> SET TR
DS>
DS> RUN SIRAA
.. Program:   RELIABILITY TESTS SYSTIME L.S.S.   ** EVRAA **
   rev 9.0. 6 tests, Testing: _SIA1

********RELIABILITY TESTS SYSTIME L.S.S.**EVRAA**-9.0********
PASS 0 INITIALIZATION SECTION ERROR 1 19-MAY-1982 18:29:28.05
SYSTEM FATAL WHILE TESTING SIA1:  ILLEGAL DRIVE TYPE

Function INITIAT^0
Do you wish to override the protection check? [(NO), YES] YES
Test 1:  qualification test
_SIA1 QA begun at 19-may-1982 18:29:40.93
_SIA1 QA complete at 19-MAY-1982 18:30:49.20
Test 2:  Seek_tests timing
seek tests on _SIA1 started at 19-MAY-1982 18:30:51.62
Seek Cylinder Range      Average Seek Time
                         (in milliseconds)
          1                   1.180
          2                   1.190
          4                   1.170
          8                   1.190
         16                   1.190
         32                   1.170
         64                   2.0
        128                   1.170
        256                   1.190
        822                   1.160
Seek tests on _SIA1 complete at 19-MAY-1982 18:31:15.61
Test 4:  multidrive functional tests
multi drive tests initiated at 19-MAY-1982 18:31:18.74
Error summary for _SIA1 at 19-MAY-1982 18:38:04.91

TOTAL XFERS     READ XFERS     WRITE XFERS     WRITECHECKS
 (BYTES)         (BYTES)        (BYTES)         (BYTES)
 67110412        22368648       22373116        22368648

TOTAL ERRORS    READ ERRORS    WRITE ERRORS    WRITECHECK ERRORS
     0               0              0               0

.. End of run.  1 Error Detected.  Pass Count:  1.
   Time:  19-MAY-1982 18:38:17.08
DS>
```

```
SIRAC DISK FORMATTER


DS>
DS> RUN SIRAC/SE:PACKINIT
.. Program:  SIRAC FORMAT SYSTIME LSS, rev 4.0, 8 tests, at
   18:40:14.07.
Testing:  _SIA1

Disk Type = RM03, Drive Serial Number = 8D21(D) for Physical
Device _SIA1, Pack Structure = FOREIGN, Pack Label =
Pack is not Labelled 'SCRATCH' do you wish to continue?
[(NO), YES] YES
Test 1:   Initialize manufacture bad sector file

************** WARNING **************
BAD SECTOR FILE WILL BE REFORMATTED

DO YOU WISH TO CONTINUE? [(NO), YES] YES

For physical device _SIA1
Enter pack serial number [(1), 1-2147483647(D)] 123456
Test 2:   Display manufacture bad sector file

CONTENTS OF BAD SECTOR FILE
PACK SERIAL NUMBER = 123456(D) FOR DEVICE _SIA1
NO BAD SECTORS IN FILE
Test 3:   Format pack
Format started   at 18:40:43.80 for device _SIA1
Format completed at 18:43:48.09 for device _SIA1
Test 4:   Surface verification
Verify started   at 18:43:50.80 for device _SIA1
BAD SECTOR FILE UPDATED BY 0(D) ENTRIES
Verify completed at 18:50:46.65 for device _SIA1
FOR PHYSICAL DEVICE _SIA1 DISK TYPE = RM03
PACK WAS LABELLED
PACK SERIAL NUMBER = 123456(D)
NUMBER OF BAD SECTORS ADDED TO BAD SECTOR FILE = 0(D)
.. End of run.  0 Errors Detected.  Pass Count:  1.
   Time:  19-MAy-1982 18:50:54.
DS>
DS>
DS>
```

```
ESC21 - SC21/SC31 DISK CONTROLLER DIAGNOSTIC
DIAGNOSTIC SUPERVISOR.  ZZ-ECSAA-6.6-185 1-JAN-1982 00:00:00
DS> LOAD ESC21
DS>
DS> ATT DW750 CMI DW0
DS>
DS>
DS> ATT SC21 DW0 UMA 776700
DS>
DS> SEL ALL
DS>
DS> SET TRACE
DS>
DS> ST/SECT:ALL

.. Program:  Emulex SC21/SC31 Disk Controller Diagnostic, at
   00:40:38.02.  Revision 1.6, 21 tests
Testing:  _UMA
Enter drive number to test [(0), 0-7(d)] 0

Test 1:   Address all registers
Test 2:   CS1 register (all 1 & 0)
Test 3:   Function bits (moving 1 & 0)
Test 4:   WC register (all 1 & 0)
Test 5:   WC register (moving 1 & 0)
Test 6:   BA register (all 1 & 0)
Test 7:   BA register (moving 1 & 0)
Test 8:   MR1 bits can be set & cleared
Test 9:   DC register (all 1 & 0)
Test 10:  DC register (moving 1 & 0)
Test 11:  DA register (all 1 & 0)
Test 12:  DA register (moving 1 & 0)
Test 13:  Invalid commands give error
Test 15:  SC bit set causes interrupt
Test 16:  IE & RDY set cause interrupt
Test 17:  Check that pack ack sets VV
Test 18:  Test IVC bit
Test 19:  Increment bus address register
Test 20:  Test BAI bit
Test 21:  Get controller configuration

Emulex SC21/SC31 Disk Controller CSR [176700]
Vector [254] is configured as an [RM02]
Port number [08]
Firmware rev [05]
Switches [000] octal
Maximum cylinder address = 823.
Maximum track address = 5.
Maximum sector address = 32.

.. End of run, 0 errors detected, pass count is 1, time is
   1-JAN-1982 00:40:57.87
DS>
DS>
```

```
EDSKF - EMULEX DISK FORMATTER DIAGNOSTIC (for SC21 or SC31)
B/10 DEVN:
DS> LOAD EDSKF
DS>
DS> ATT DW750 CMI DW0                    } For SC750 attach string
DS> ATT SC21 DW0 UMA0 776700 254         } see page 2.9-10
DS>
DS> SEL ALL*
DS>
DS> ST/SECT:FORVER

.. Program:  Emulex Disk Formatter, revision 2.0, 7 tests, at
   00:04:25.03
Testing:  _UMA0

UNIT:  UMA0
DRIVE SERIAL NUMBER:  88
DRIVE TYPE:  RM02 (823 CYLINDERS, 5 TRACKS, 32 SECTORS)
FILE STRUCTURE:  FOREIGN
VOLUME LABEL:   UNREADABLE
BAD AND/OR SKIP SECTOR FILE UNREADABLE
INIT UMA0 IS NOT A SCRATCH VOLUME;
DO YOU WISH TO CONTINUE? [(NO), Y] Y
DO  YOU WISH TO INITIALIZE THE BAD (AND SKIP) SECTOR FILE(S)?
[(NO), YES] Y
FOR   UNIT   UMA0,   ENTER   VOLUME   SERIAL   NUMBER   [(0),
1-2147483647(D)] 1234
Test 6:   Unit UMA0 Format started at 00:11:12.68   6 mins approx
UNIT UMA0 format completed at 00:18:01.12
UNIT UMA0 verify started at 00:18:01.26
UNIT UMA0 verify completed at 00:16:11.56
UNIT:  UMA0
   No OF ADDITIONAL BAD SECTORS: 14
   BAD SECTOR FILE CONTENTS:
     LOGICAL BLOCK    CYL    TRACK    SECTOR
           1831        11       2        7
           1991        12       2        7
           2149        13       2        5
           2150        13       2        6
           2151        13       2        7
           2306        14       2        2
           2307        14       2        3
           2308        14       2        4
           2309        14       2        5
           2310        14       2        6
           2311        14       2        7
           2312        14       2        8
           2468        15       2        4
         127490       796       4        2
.. End  of  run,  0 Errors Detected, Pass Count is 1, time is
   1-JAN-1982 00:26:18.41
DS>
```

* If Stand-Alone and ESC21 was run prior to EDSKF, Deselect UMA.

EDSKR - EMULEX DISK RELIABILITY DIAGNOSTIC (for SC21 or SC31)*

STAND ALONE

```
DS> LOAD EDSKR

DS> ATT DW750 CMI DW0
DS>
DS> ATT SC21 DW0 UMA 776700 254 5
DS> SEL UMA
DS> START
```

ONLINE (under VMS)

```
DS> LOAD EDSKR
DS> ATT DW750 CMI DW0
DS> ATT RM03 DW0 UMA0
DS> SET TR
DS> SEL ALL
DS> ST
```

```
.. Program:    Emulex VAX Disk and TU58 Reliability Test
   Program, Revision 1.1, 4 tests, at 00:53:41.75.
Testing: _UMA0 _UMA
_UMA, an RM02, with volume label 'SCRATCH', has been added to
test queue.
Test 1:   Qualification
_UMA0 Qualification started at 1-JAN-1982 00:53:43.10
_UMA0 Qualification completed at 1-JAN-1982 00:55:11.79
_UMA Qualification started at 1-JAN-1982 00:55:11.06
_UMA Qualification completed at 1-JAN-1982 00:56:40.35
Test 2:   Timing
Seek tests on _UMA0 started at 1-JAN-1982 00:56:40.44
Seek Cylinder Range   Average Seek Time
                      (in milliseconds)
         1                  4.150
         2                  5.80
         4                  7.60
         8                  8.150
        16                 10.150
        32                 14.10
        64                 19.30
       128                 24.80
       256                 32.60
       822                 54.60

Seek tests on _UMA completed at 1-JAN-1982 00:58:14.02
.. End of run, 0 errors detected, pass count is 1, time is
   1-JAN-1982 00:58:14.10
DS>
DS>
```

* For SC750 attach string
see page 2.9-10

DEC DIAGNOSTIC DISTRIBUTION

TU58 11 - VAX 11/750

TU58 7 - VAX Hardcore Instr

EVKAA .EXE	118
EVKAB .EXE	89
EVKAB .HLP	7

TU58 8 - VAX 11 Instr.

EVKAB .EXE	89
EVKAB .HLP	7
EVKAC .EXE	100
EVKAC .HLP	7
EVKAD .EXE	124
EVKAD .HLP	3
EVKAE .EXE	105
EVKAE .HLP	3
EVKAM .EXE	51
EVKAM .HLP	7

TU58 9 - CR/Disk User Mode

EVQDB .EXE	4
EVQDD .EXE	4
EVQDL .EXE	5
EVQDM .EXE	5
EVQDQ .EXE	5
EVQDR .EXE	5
EVQDY. EXE	5
EVQEM .EXE	4
EVQTF .EXE	13
EVAAA .EXE	78
EVAAA .HLP	10
EVABA .EXE	21
EVABA .HLP	8
EVRAA .EXE	105
EVRAA .HLP	6
EVRAC .EXE	115
EVRAD .EXE	87
EVRAD .HLP	8

TU58 20 - VAX SYS EXR/BUS INIT

EVLBA .SUP	4
EVXBA .EXE	120
EVXBB .EXE	110
EVXBB .HLP	9
EVXBB .COM	5
EVQDB .EXE	4
EVQDL .EXE	5
EVQDM .EXE	5
EVQDR .EXE	5
EVQTM .EXE	9
EVQTS .EXE	7
EVQUE .EXE	5
VSDP .COM	12

TU58 33 - VAX Bus Diagnostics

ECCAA .EXE	107
ECCBA .EXE	67
ECCBA .HLP	4
EVDAA .EXE	69
EVTAA .EXE	97
EVTAA .HLP	11
EVTBA .EXE	83
UBIATT.COM	2

TU58 43 - VAX Bus Test Diag.

ECCAA .EXE	107
ECCBA .EXE	67
EVCEA .EXE	58
EVCEA .HLP	16

TU58 51 - VAX Autosizer Diag.

EVSBA .EXE	76
EVSBA .HLP	21

APPENDIX A - PRODUCT BULLETINS

11/750 MK1 1MB MEMORY ARRAY

SYSTEM: 8750 with MK1 1MB memory arrays

PROBLEM: MK1 1MB Memory Array will not work with battery backup.

SOLUTION: Remove Link 3. Add Link from BD1 to handle side of Link 3. Connects +5VB to all memory chips.

Link 3 is now:

IN = No battery backup.
OUT = Battery backup installed.

NS753 1MB MEMORY WITH MODIFIED L0011 CONTROLLER

SYSTEM: Systime 8750 with modified L0011

PROBLEM: When installing the NS753 1MB National Semiconductor memory array on the modified L0011 memory controller, there are two modifications which need to be fitted to the modified L0011 and one link to be added to the memory array.

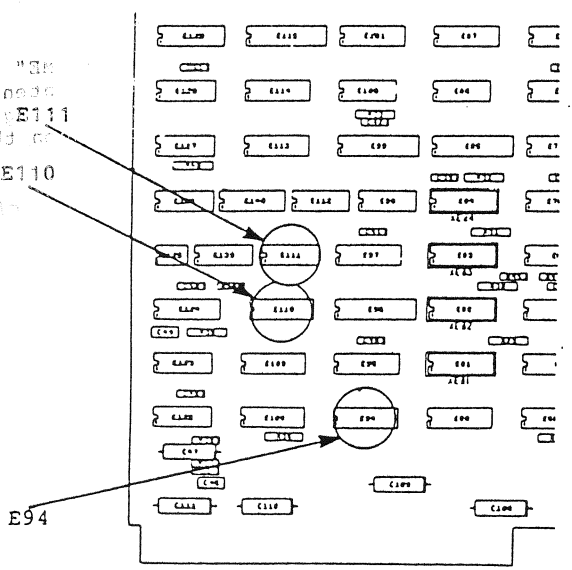
SOLUTION: Install link W10 on the National Semiconductor memory array.

Modifications to the L0011 (see below)

Cut pins : E110 pin 10
E 94 pin 3

Connect : E111 pin 8 to E110 pin 10*
E111 pin 1 to E 94 pin 3*

* Note these connections are to the leg of I.C.



T.O.Y. CLOCK PROBLEMS

SYSTEM: Systime 8750 with Farnell power supplies

PROBLEM: There is a high occurrence of T.O.Y. clock failures in the field where the system prompts for the time and date each time the system comes up, rather than using the contents of the T.O.D. register.

The following is a list of "known cures" at the present time.

a) Replace E50 on the L0004 module, from CD40114 to 74C89N.

b) Check presence of wire from PIN A00440 on backplane to connector J5 pin 1, this supplies power from battery to the T.O.Y. circuit on the L0004 board.

c) Failure of first batch of AC/DC low boards - due to glitches on the DC-Low signal, this was cured by extensive mods to the boards. A new revision board is now available.

d) The SYSGEN parameter "SETTIME" must be OFF(0)in order to use the contents of the T.O.D. register rather than having to enter date and time from the console when the system is booted.

e) There is a high failure rate of T.O.Y. batteries, normally one cell going short-circuit, causing the output voltage on load to drop to approximately 4V.

L0010 SUB OPTION INSTALLATION

SYSTEM: 11/

The DW750 will fit in slots 7, 8 or 9 of the processor backplane. Remove the 4 bus grant jumpers in connector A of the backplane on the slot chosen. If installed with other MBA's, for example SC750's, then the CMI arbitration level for the existing devices must be dropped by 1. Refer to the Controllers and Interfaces handbook for switch settings.

If the backplane is a Systime manufactured type (Part No 030-0465) and is revision C or earlier then it is necessary to add the following wires:-

From Slot 4 B89 to Slot 7 C48
From Slot 7 C48 to Slot 8 C48
From Slot 8 C48 to Slot 9 C48

The DEC backplane does not require these additions. Attach the three pin guides for the 3 x 40 way cables carrying the Unibus signals. These push over the backplane pins and the correct positions are:

Cable A from J1 on the M9012 board to pins B53-B92
Cable B from J2 on the M9012 board to pins C3-C42
Cable C from J3 on the M9012 board to pins C53-C92

Install the M9012 in slot 1 or 9 AB of the 9 slot backplane and fit a standard M9302 terminator to the end of the bus. A special terminator is not required because the UET test registers are contained on the L0010 module.

Boot Diagnostic Supervisor and attach the DW750:-

```
DS> ATT DW750 CMI DW1
```

Run EVCBA, version 1.3 or higher, version 1.2 will fail test 29 (AC LOW TEST).

AC/DCLO INITIALISE PROBLEMS

SYSTEM: Systime 8750 with Farnell power supplies.

PROBLEM: When the 8750 is powered up, AC DCLO signals remain asserted and the 8750 fails to initialise. This is because the signal DCLO, originating on the mother board remains asserted. The 8750, sensing this, refuses to negate ACLO. The DCLO D-type in position E2, doesn't clock due to the inadequate delay between pre-set going high and the clock input going to the DCLO D-type, E2.

SOLUTION: On side 1, solder a 1000pf capacitor between E2 pin 11 and E2 pin 7. Bend the capacitor over the body of E2.

PARTS AFFECTED: Add a 1000pf capacitor part no 0410021.

11/750 MK2 1MB MEMORY

SYSTEM: 8750 with Systime MK1 Memory

PROBLEM: When adding MK2 1MB memory modules to the 8750 with MK1 1MB memory boards already installed, due to the link configuration on the new board it may be necessary to alter the links on the existing boards.

If after installing the new memory VMS will not boot, reporting an "unexpected exception" before halting, the links on the existing arrays should be checked and installed according to the following tables.

This problem can occur on both the modified L0011 and L0016 memory controllers.

SOLUTION: The links on the MK1 Memory boards should be as follows:

L0016	Modified L0011
LK 15 IN	LK 15 IN
LK 16 OUT	LK 16 OUT
LK 17 IN	LK 17 IN
LK 18 OUT	LK 18 OUT
LK 19 IN	LK 19 IN
LK 20 OUT	LK 20 OUT
LK 21 IN	LK 21 IN
LK 22 OUT	LK 22 OUT
LK 1 OUT	LK 1 IN