digital

EK-MXV1B-CG-001

MXV11-B CONFIGURATION GUIDE

The M7195 module, designated MXV11-B, is a dual-height, multi-function option module compatible with LSI-11, LSI-11/2, and LSI-11/23 processors. The module can operate on the 22-bit Q-bus, the 18-bit Q-bus, and the 16-bit Q-bus. MXV11-B features include:

- Read/write memory capability (MOS RAM)
- 5 V battery backup for MOS RAMs
- Read only memory (ROM)
- ROM window map logic (page control register)
- Two asynchronous serial line ports (SLU0, SLU1)
- Multiple line time clock frequencies
- LED diagnostic display register.

> NOTE:
> **The page control register, line time clock register, and diagnostic display register are user options and can only be selected if the MXV11-B is strapped for console port and bootstrap mode. Also, the halt or boot functions may be optionally selected in this configuration.**

Figure 1 shows the default configuration of the Push-on connectors.

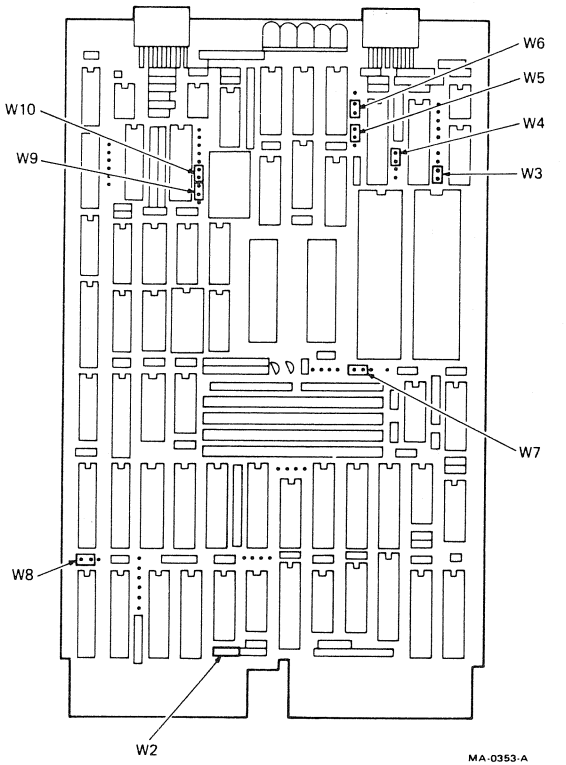

Figure 1 Shipped Configuration of Push-on Connectors

Before configuring the MXV11-B module, complete the following checklist. The checklist, jumper locations in Figure 2, the flow diagram in Figure 3 and Tables 1 through 7 should be used when configuring a system.

		User Configuration	Shipped Configuration
1	Do you wish to connect the system console to this MXV11-B? If no, disregard following questions marked with an *. If yes, the console must be connected to SLU #1.		Yes
2*	Do you wish system to halt on break from console?		Yes
3*	Do you wish system to reboot on break from console?		No
4	What is desired address/vector for SLU 0?	/	776500/300
5	What is desired address/vector for SLU 1?	/	777560/60
6*	Will this MXV11-B contain MXV11-B2 ROM?		No
7	Will this MXV11-B contain user ROM?		No
	If yes, at what address?		N/A
	*Are user ROMs to be addressed via page mode?		N/A
	What is ROM size?		N/A
	What is ROM type?		N/A

		User Configuration	Shipped Configuration
8*	Do you want software control of line time lock ( )?		No
9	Does this system have "Q" or "Q22" bus?		Q Bus
10	Do you wish this module to be source of line time clock (BEVENTL)?		No
11	If yes, at what frequency (50, 60, or 800 Hz)?		
12	Do you wish software control of baud rate?		No
13	What hardware controlled baud rates are desired? SLU0/SLU1		300/9600
14	Is battery backup desired for RAM memory?		No
15	What is RAM starting address?		000000

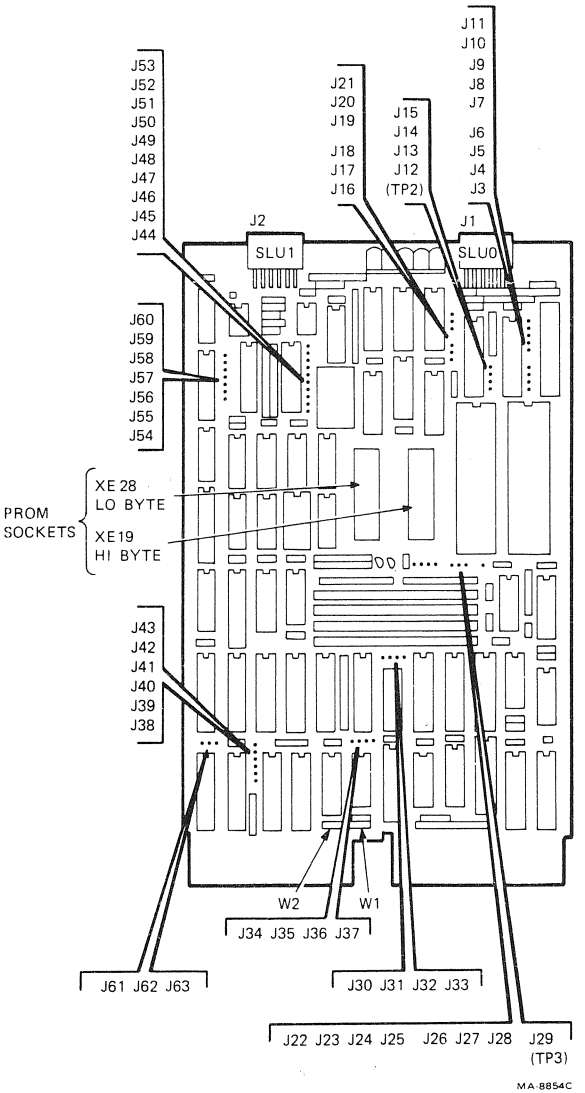

Figure 2 Jumper Locations

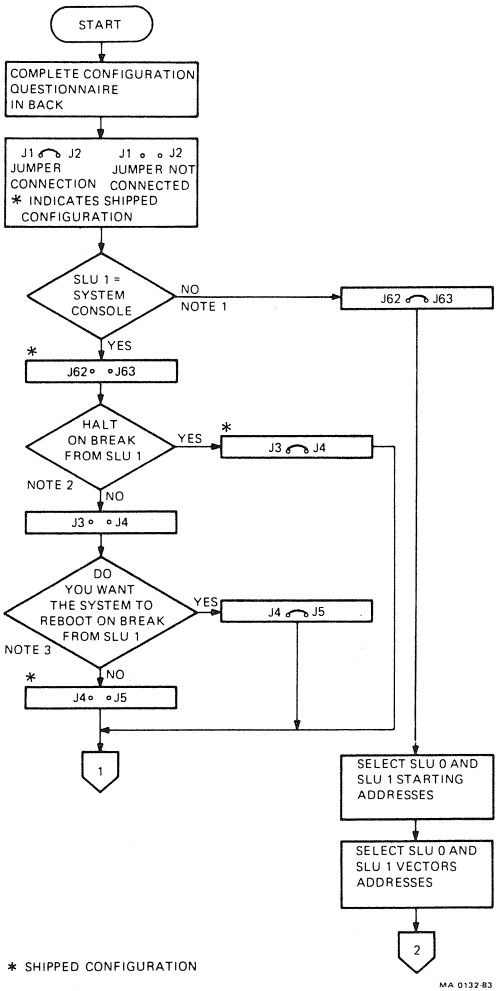

Figure 3 MXV11-B Flow Diagram (1 of 4)

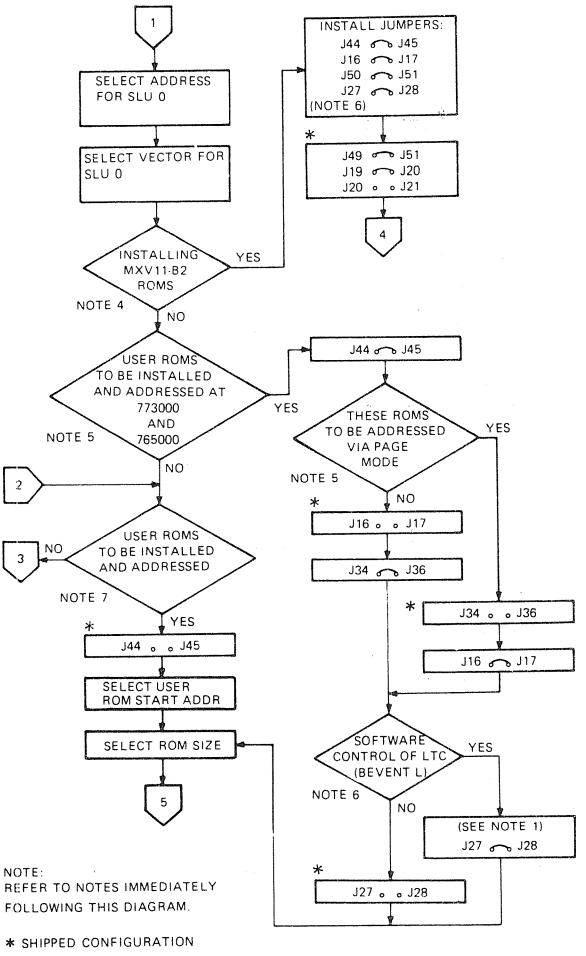

Figure 3 MXV11-B Flow Diagram (2 of 4)

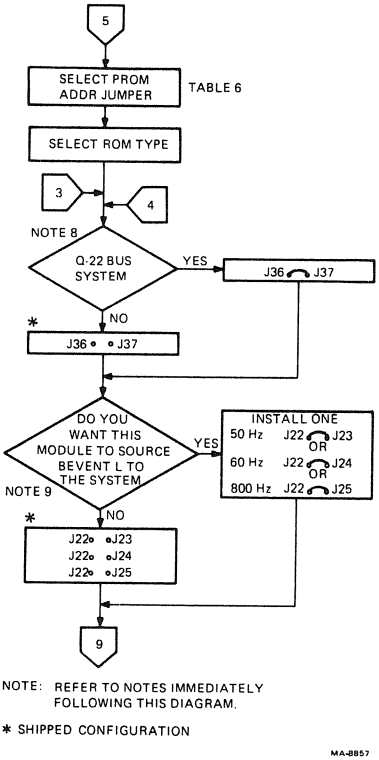

Figure 3 MXV11-B Flow Diagram (3 of 4)

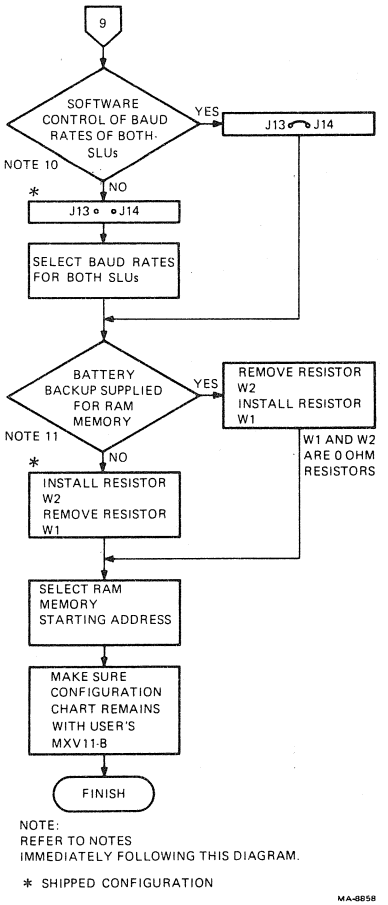

Figure 3 MXV11-B Flow Diagram (4 of 4)

FIGURE NOTES

1. If SLU1 is not selected to be the system console (jumper installed from J62 to J63) the following features cannot be selected:

   Halt on break condition from SLU1 (never available with SLU0)

   Reboot on break condition from SLU1 (never available with SLU0)

   Console address (777560)

   MXV11-B2 ROMs or user ROMs addressed at 773000 and 765000

   Software control of the LTC (BEVENT L) (address 777546 does not exist)

   Page control register (address 777520 does not exist)

   Diagnostic display register (address 777524 does not exist)

2. A framing error or continuous spacing (break) condition from SLU1 will cause the BHALT L signal on the bus to be asserted by the MXV11-B causing the system to halt.

3. A framing error or continuous spacing (break) condition from SLU1 will cause the BDCOK H signal on the bus to be de-asserted, and will cause the system to reboot if the CPU module is configured to do so on powerup.

4. MXV11-B2 ROMs are 8K × 8 UV PROMs and must have access to the page control register, diagnostic display register, and LTC control register.

5. User ROMs may be installed and addressed at 773000 and 765000. If more than 256 words are to be used in each address space, page mode must be enabled and addressing will be controlled by the page control register.

6. If control of LTC is selected (jumper installed from J27 to J28) the BEVENT L signal may be controlled by bit 06 in the LTC control register. If bit 06 is set, the BEVENT L signal on the bus will be driven by the source (usually by the power supply in Digital systems) allowing LTC interrupts. If bit 06 is reset, BEVENT L will be held low by the MXV11-B thereby inhibiting LTC interrupts.

   CAUTION:
   Bit 06 is reset on power up. If another control register is included in the system (e.g., CPU module) and jumper J27 and J28 is installed, LTC interrupts will never be enabled because the LTC control register on the MXV11-B will not be accessed to set this bit.

7. User supplied ROMs are installed and addressed as memory residing in low memory space.

8. The MXV11-B may be installed in a Q-22 bus system or a Q-Bus system. If a jumper is not installed from J36 to J37 the RAM starting address is limited to 64K or below.

9. The MXV11-B can be configured to be the source of the BEVENT L signal for the system. Power supplies normally are the source of this signal in Digital systems. Do not have two sources in a system.

10. Baud rates for the serial lines may be software controlled or fixed by jumpers. If software control is desired, both SLUs will have this feature enabled and the fixed jumpers will have no effect.

11. Battery backup for the RAM memory and support circuits via pin AV1 on the backplane. Installing W1 and removing W2 removes normal system +5 V from the memory circuits only. Digital systems do not supply battery backup voltages to the backplane.

Table 1 Jumpers for PROM Starting Address

BSK2 to GND (J53 to J51)	BSK1 to GND (J52 to J51)	User PROM Starting Address (octal) (See Note)
R	R	000000*
R	I	020000
I	R	040000
I	I	060000

R = jumper removed
I = jumper inserted to ground

Note: These addresses are for user supplied ROMs only. Jumpers BOOT L/PROM H to GND (J44 to J45) and PG L/DIR H to GND (J17 to J16) must be removed.

* Shipped configuration. Remove all jumpers from BSK1 (J52) and BSK2 (J53) if not in user mode.

Table 2 Serial Line Unit Baud Rates

SLU0 (See Note)

J0B to GND (J10 to J9)	J0A to GND (J11 to J9)	Baud Rates
R	R	300*
R	I	1200
I	R	9600
I	I	38.4K

SLU1 (See Note)

J1A to GND (J8 to J9)	J1B to GND (J7 to J9)	Baud Rates
R	R	9600*
R	I	38.4K
I	R	300
I	I	1200

R = jumper removed
I = jumper inserted to ground

Note: SOFT EN to GND jumper (J14 to J13) must be removed; otherwise these jumpers have no effect. If the SOFT EN to GND jumper (J14 to J13) is installed and PBRE bit 1 is set, baud rates are software controlled.

* Shipped configuration

Table 3 Serial Line Unit Starting Address Jumpers

SLUA3 to GND (J30 to J31)	SLUA2 to GND (J32 to J31)	SLUA1 to GND (J33 to J31)	Starting Address SLU0	SLU1 (See Note)
R	R	R	776500*	776510*
R	R	I	776510	776520
R	I	R	776520	776530
R	I	I	776530	776540
I	R	R	776540	776550
I	R	I	776550	776560
I	I	R	776560	776570
I	I	I	776570	776600

R = jumper removed
I = jumper inserted to ground

Note: If the GND to OPEN jumper (J62 to J61) is installed (console enabled), the SLU1 address is fixed at the standard console address of 777560 and this column does not apply.

* Shipped configuration

Table 4 Jumpers for SLU Vector Addresses

JU2 to GND (J39 to J40)	JU1 to GND (J38 to J40)	JL3 to GND (J43 to J40)	JL2 to GND (J42 to J40)	JL1 to GND (J41 to J40)	SLU0	SLU1 (See Note)
R	R	R	R	R	300*	310*
R	R	R	R	I	010	020
R	R	R	I	R	020	030
R	R	R	I	I	030	040
R	R	I	R	R	040	050
R	R	I	R	I	050	060
R	R	I	I	R	060	070
R	R	I	I	I	070	100
R	I	R	R	R	100	110
R	I	R	R	I	110	120
R	I	R	I	R	120	130
R	I	R	I	I	130	140
R	I	I	R	R	140	150
R	I	I	R	I	150	160
R	I	I	I	R	160	170
R	I	I	I	I	170	200
I	R	R	R	R	200	210
I	R	R	R	I	210	220
I	R	R	I	R	220	230
I	R	R	I	I	230	240
I	R	I	R	R	240	250
I	R	I	R	I	250	260
I	R	I	I	R	260	270
I	R	I	I	I	270	300
I	I	R	R	R	300	310
I	I	R	R	I	310	320
I	I	R	I	R	320	330
I	I	R	I	I	330	340
I	I	I	R	R	340	350
I	I	I	R	I	350	360
I	I	I	I	R	360	370
I	I	I	I	I	370	Undef.

I = jumper inserted from specified pin to ground. Where multiple connections are made, they are daisy-chained.

R = jumper removed

Note: If the GND to OPEN jumper (J62 to J61) is installed (console enabled), SLU1 vector address is fixed at 60 and this column does not apply.

* Shipped Configuration

Table 5 RAM Starting Address Jumpers

	AJ18 to GND (J60 to J57)	AJ17 to GND (J59 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
00	R	R	R	R	R	R	0*
01	R	R	R	R	R	I	4K
02	R	R	R	R	I	R	8K
03	R	R	R	R	I	I	12K
04	R	R	R	I	R	R	16K
05	R	R	R	I	R	I	20K
06	R	R	R	I	I	R	24K
07	R	R	R	I	I	I	28K
10	R	R	I	R	R	R	32K
11	R	R	I	R	R	I	36K
12	R	R	I	R	I	R	40K
13	R	R	I	R	I	I	44K
14	R	R	I	I	R	R	48K
15	R	R	I	I	R	I	52K
16	R	R	I	I	I	R	56K
17	R	R	I	I	I	I	60K
20	R	I	R	R	R	R	64K
21	R	I	R	R	R	I	68K†
22	R	I	R	R	I	R	72K†
23	R	I	R	R	I	I	76K†
24	R	I	R	I	R	R	80K†
25	R	I	R	I	R	I	84K†
26	R	I	R	I	I	R	88K†
27	R	I	R	I	I	I	92K†
30	R	I	I	R	R	R	96K†
31	R	I	I	R	R	I	100K†
32	R	I	I	R	I	R	104K†
33	R	I	I	R	I	I	108K†
34	R	I	I	I	R	R	112K†
35	R	I	I	I	R	I	116K†
36	R	I	I	I	I	R	120K†
37	R	I	I	I	I	I	124K†
40	I	R	R	R	R	R	128K†
41	I	R	R	R	R	I	132K†
41	I	R	R	R	I	R	136K†
43	I	R	R	R	I	I	140K†
44	I	R	R	I	R	R	144K†
45	I	R	R	I	R	I	148K†
46	I	R	R	I	I	R	152K†
47	I	R	R	I	I	I	156K†

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.

R = jumper removed

* Shipped configuration

† To use address above 64K words, SM/LG SYS TO GND jumper (J37 to J36) must be installed

Table 5 RAM Starting Address Jumpers (Cont)

	AJ18 to GND (J60 to J57)	AJ17 to GND (J59 to J57)	AJ16 to GND (J58 to J57)	AJ15 to GND (J56 to J57)	AJ14 to GND (J55 to J57)	AJ13 to GND (J54 to J57)	RAM Starting Address (Words)
50	I	R	I	R	R	R	160K†
51	I	R	I	R	R	I	164K†
52	I	R	I	R	I	R	168K†
53	I	R	I	R	I	I	172K†
54	I	R	I	I	R	R	176K†
55	I	R	I	I	R	I	180K†
56	I	R	I	I	I	R	184K†
57	I	R	I	I	I	I	188K†
60	I	I	R	R	R	R	192K†
61	I	I	R	R	R	I	196K†
62	I	I	R	R	I	R	200K†
63	I	I	R	R	I	I	204K†
64	I	I	R	I	R	R	208K†
65	I	I	R	I	R	I	212K†
66	I	I	R	I	I	R	216K†
67	I	I	R	I	I	I	220K†
70	I	I	I	R	R	R	224K†
71	I	I	I	R	R	I	228K†
72	I	I	I	R	I	R	232K†
73	I	I	I	R	I	I	236K†
74	I	I	I	I	R	R	240K†
75	I	I	I	I	R	I	244K†
76	I	I	I	I	I	R	248K†
77	I	I	I	I	I	I	252K†

I = jumper inserted from designated pin to GND. Where multiple connections are made, they are daisy-chained.

R = jumper removed

* Shipped configuration

† To use address above 64K words, SM/LG SYS TO GND jumper (J37 to J36) must be installed

Table 6 PROM Address Jumpers

NA12H BA12H (J20 to J19)	NA12H to +5 V (J20 to J21)	Description
R	R	Page mode – Boot ROM for 2K by 8 non-UV
I	R	PROMs, 4K by 8 or 8K by 8 PROMs.
R	I	Direct mode – for 2K by 8, non-UV PROMs, 4K by 8, or 8K by 8 PROMs.*
		Direct mode – for 2K by 8 UV PROMs.

R = jumper removed
I = jumper inserted to ground

* Shipped configuration

Table 7 Jumpers to Configure PROM Size

PROM 2 to GND (J50 to J51)	PROM 1 to GND (J49 to J51)	PROM Size
R	R	No ROMs*
R	I	2K by 8
I	R	4K by 8
I	I	8K by 8†

R = jumper removed
I = jumper inserted

* Shipped configuration. Additional jumpers are required depending on user mode/boot mode and direct addressing page addressing.

† If the MXV11-B2 Boot Diagnostic ROM set is installed, install PROM 2 to PROM 1 to GND jumper (J50 to J49 to J51).

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