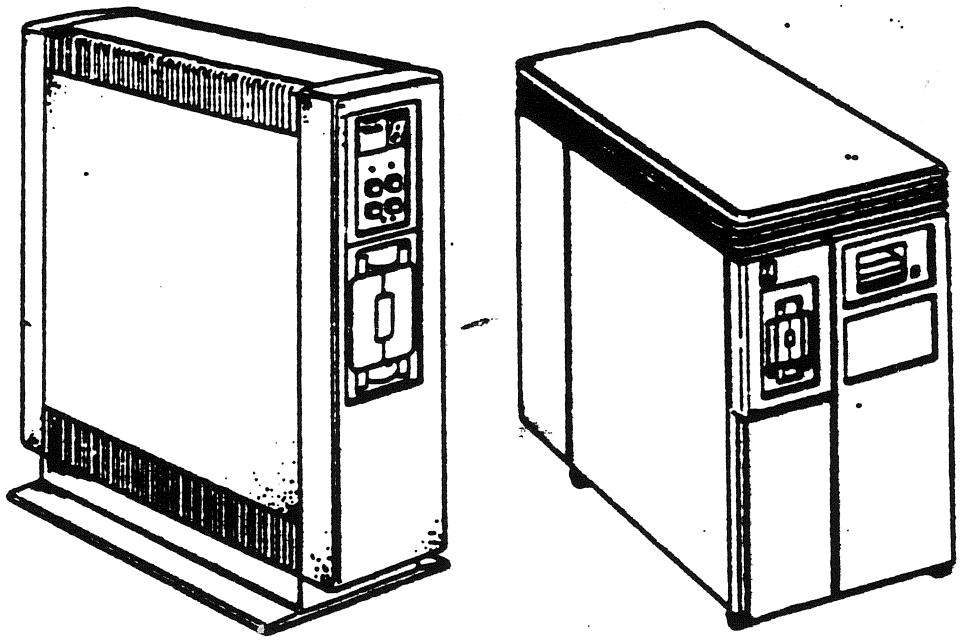
EK-MIC11-SG-PRE2

MicroPDP-11 Systems

MAINTENANCE GUIDE



digital

For Internal Use Only

KEPROM (2,048 by 8 bits in 1 KEPROM)

- Harware parameters
- Boot device selection
- Foreign language text
- Optional customer bootstrap programs

See Sections 2.4 - 2.5 for further information.

Figure 2-3 shows the location of a dual in-line package (DIP) switch, diagnostic LEDs, connectors, and jumpers on the board. The DIP switch (E83) enables the baud rate select switch on the SLU display panel (Section 2.2.2).

Table 2-1 lists the factory setting for the E83 DIP switch (Section 2.2.3) and the three jumpers. These jumpers are for manufacturing and factory test purposes only.

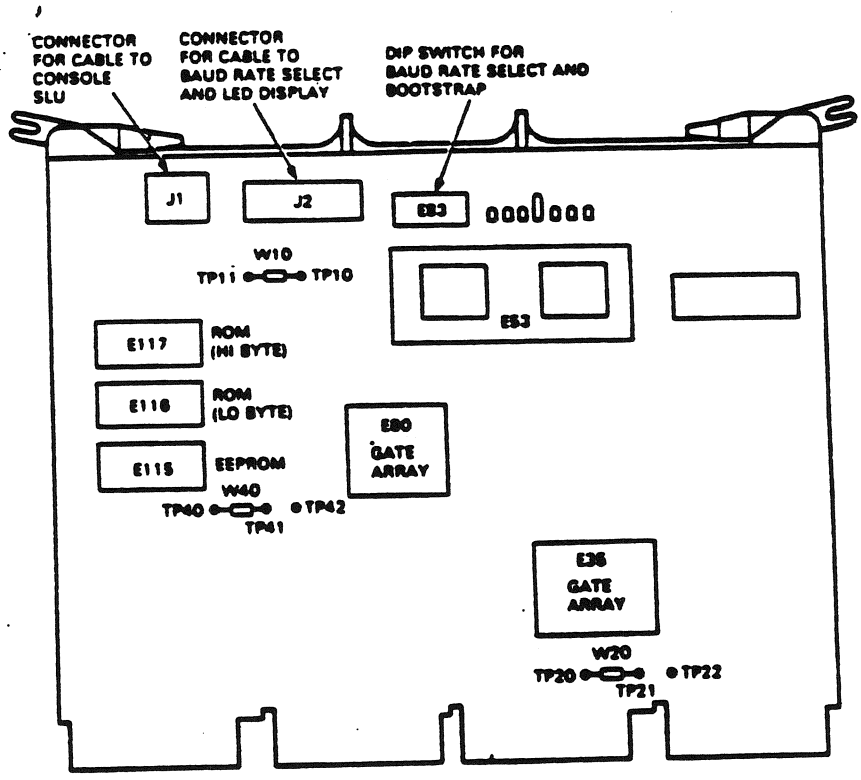
Table 2-1 KDJ11-B Factory setting

Switch/ Jumper	Setting
E83	all Off
W10	Between TP10 and TP11
W20	Between TP20 and TP21
W40	Between TP40 and TP41

2.2.1 KDJ11-B LEDs

Seven LEDs on the KDJ11-B provide status information. The green LED indicates the presence of +5 Vdc and +12 Vdc. The six red LEDs show error detection and diagnostic status codes. These codes are also shown in octal format on the SLU display panel. Refer to Chapter 4, Diagnostics, Section 4.3, for definitions of the codes and detailed diagnostic information.

Figure 2-3 KDJ11-B Module Layout



2.2.2 KDJ11-B Baud Rate Select Switch

The baud rate select switch on the SLU display panel has 15 positions (Figure 2-1), performing the following operations:

- Displays the settings (numbers 0 - 15) above the switch.
- Selects a baud rate (positions 0-7) and causes the system to boot as specified by the settings in the EEPROM (Section 2.3).
- Selects (positions 8-15) the same baud rate as positions 0-7 but puts the system into dialog mode (Section 2.4).

Table 2-2 lists the switch settings, baud rate and display mode.

Table 2-2 Baud Rate/Mode Select Switch

Switch Settings		
EEPROM Selects Baud Rate	Automatic Boot Mode	Dialog Mode
38400	0	8
19200	1	9
9600	2 *	10
4800	3 **	11
2400	4	12
1200	5	13
600	6	14
300	7	15

* Factory setting.
** Most digital terminals are set to 4800 baud.

2.2.3 KDJ11-B DIP Switch

Figure 2-3 shows the location of the Dual In-line package (DIP) switch. It contains eight switches that can optionally be used to:

- Set the SLU baud rate.
- Set the boot device.

The normal setting for all eight switches is Off and the SLU baud rate switch and the dialog mode settings stored in the EEPROM control these functions.

Setting switch 1 to On disables the console terminal. This setting is for factory use only*.

Switches 2, 3, and 4 select the boot device. The dialog mode features described in Section 2.5.6 allow you to define a boot device for different combinations of these switch settings.

Table 2-3 lists the KDJ11 settings for switches 2,3,and 4 and their functions.

* This feature is not implemented at this time.

Table 2-3 KDJ11 Switchs 2, 3, and 4

Switch 2	3	4	Function
Off	Off	Off	Boot automatically according to the dialog mode settings.
Off	Off	On	Boot device 1
Off	On	Off	Boot device 2
Off	On	On	Boot device 3
On	Off	Off	Boot device 4
On	Off	On	Boot device 5
On	On	Off	Boot device 6
On	On	On	If switch 1 is Off power up to ODT. If switch 1 in On run self test diagnostics in a loop.

When switch 5 is Off the system enters dialog mode on power-up.

Use switches 5 through 8 to set the baud rate if no SLU display panel is present.

Use switches 6, 7, and 8 to set the baud rate when the baud rate rotary switch is disconnected from the CPU module. When the rotary switch is connected, it interfers with the operation of these switches unless it is set to 7 or 15. Likewise, these three DIP switches interfere with the proper operation of the rotary switch unless they are all set to Off.

Table 2-4 show the switch settings for switches 6, 7, and 8 and their corresponding baud rates.

Table 2-4 Switch Settings For Switches 6, 7, and 8

Switch 6	7	8	Baud Rate
On	On	On	38400
On	On	Off	19200
On	Off	On	9600
On	Off	Off	4800
Off	On	On	2400
Off	On	Off	1200
Off	Off	On	600
Off	Off	Off	300

2.2.4 KDJ11-B Jumper Settings

Pending further information

2.2.5 KDJ11-B Location In MicroPDP-11/73 and MicroPDP-11/83 Systems

A MicroPDP-11/73 system uses the KDJ11-BC or KDJ11-BB CPU module and one or more MSV11-P memory modules (Section 2.6). Data tranfers between the CPU and meomry use the Q-Bus protocol.

Always install the KDJ11-BC or KDJ11-BB CPU module in the first slot of the backplane assembly. The MSV11-P memory module(s) must be installed in the slot(s) immediately following the CPU module.

A MicroPDP-11/83 system uses the KDJ11-BF CPU module and one or more MSV11-JD or MSV11-JE memory modules (Sectiion 2.7). Data transfers between the CPU and memory use the private memory interconnect (PMI) protocol resident on the KDJ11-BF CPU. All other communications, whether originated by the CPU or other bus master, use the Q-Bus protocol. PMI is implemented through the CD Bus on the backplane.

Always install the KDJ11-BF CPU in slot 2 or 3 of a BA23 enclosure backplane, or in slot 2, 3, or 4 of a BA123 enclosure backplane. The MSV11-JD or MSV11-JE memory module(s) MUST be installed immediately in front (lower slot number) of the CPU. There should be no open slot between and CPU and memory, nor should there be a open slot preceding the memory module. No other boards can be inserted in the CD rows of slots 1 through 3 in a BA23-A enclosure, or in slots 1 through 4 of a BA123-A enclosure..

If the MSV11-JD or -JE memory is installed following the KDJ11-BF CPU, the CPU and memory communicate using the Q-Bus protocol.

2.3 KDJ11-B AUTOMATIC BOOT MODE

When set to the factory configuration, the KDJ11-B automatically runs the diagnostic self-test every time the system is turned on or restarted.

Typing <CTRL> C during self-test stops the test and causes the system to attempt to boot, as if the self-test had completed successfully.

After successful completion of the startup self-test (described in Chapter 4, Diagnostics, Section 4.2), the ROM code loads the first 105 bytes of the EEPROM into memory beginning at location 2000. This area in memory is referred to as the setup table. The factory setting of the setup table (Section 2.5.2) initiates automatic boot mode, which directs the system to take one of the following actions:

- Boot from one or more of the previously selected devices.
- Enter dialog mode (Section 2.4).
- Enter console emulator mode (sometimes called halt mode).(See Chapter 4, Diagnostis, Section 4.5.)

The factory setting of the EEPROM code searches for and identifies available MSCP (mass storage control protocol) devices (units 0 - 7) and other available devices. It attempts to boot from the available devices in the following order:

- MSCP devices with removable media (RX50)
- MSCP devices with fixed media (RD5X)
- RL01/RL02
- TSV05/TK25

NOTE
You can change this sequence of devices with the Automatic Boot Setup command described in Section 2.5.4.

If no bootable medium is found, the system displays a message similiar to the following:

```
Testing in progress - Please wait
      1 2 3 4 5 6 7 8 9
Waiting for media to be loaded, or drive to go ready
    Press the RETURN key when ready to continue
```

This message indicates that the system has entered dialog mode and is waiting for user input.

If you load bootable media and press the Return key, the system returns to automatic boot mode and boots the appropriate device.

Typing <CTRL> P while the system is booting causes the system to stop the boot process and enter dialog mode.

If you press the Return key (without first loading media), the system displays the following message:

Message 07
None of the selected devices were bootable
Press the RETURN key when ready to continue or to
list boot messages:

2.4 KDJ11-B DIALOG MODE

Dialog mode allows you to perform the following operations:

- Change CPU parameters
- Select the boot source
- Display a listing of all boot programs
- Enter a bootstrap program
- List all memory and occupied register locations in the system
- Cause the startup self test to run in a loop
- Enter ROM ODT

2.4.1 Entering Dialog Mode

The system enters dialog mode if:

- No bootable medium is available, and you follow the procedure described in Section 2.3.
- You type <CTRL> P or <CTRL> C during the start-up self-test.
- The EEPROM is programmed to enter dialog mode.
- The baud rate select switch is set to a position from 8 to 15.

2.4.2 Dialog Commands

Dialog mode has the 6 commands listed below. Three other functions are present:

- <CTRL> R (redisplay current input line)
- <CTRL> U (clear current input line)
- Delete

Select a command by typing the first letter of the command.

HELP - Displays a one-screen help file that provides a short description of each command.

BOOT - Allows you to select the boot source. To Select the source, enter the device mnemonic followed by a unit number (for example, DU1). The program assumes decimal unit numbers. To specify the unit number as an octal value, type /O after the unit number (DU1/O). You can also assign a nonstandard CSR address by typing /A after the unit number (DU1/A). When you use both of these switches, do not repeat the slash; for example, type DU1/OA.

> **NOTE**
> Typing B and pressing <RETURN> causes the ROM code to check for an off-board ROM at address 17773000. When an off-board ROM exists and its first location is not zero, the ROM code disables the internal code and jumps to address 17773000 of the off-board ROM.

LIST - Displays a list of all the boot programs available in the ROM and EEPROM. The list includes the device name, unit number range, source of the program, and device type.

SETUP - Causes the system to enter Setup mode. This mode allows you to access and change the operating parameter settings and any bootstrap programs stored in the EEPROM. Setup mode consists of 15 commands (Table 2-5). See Sections 2.5.1 to 2.5.15 for a description of each command.

MAP - Searches for, identifies, and lists all memory in the system and all occupied register locations in the system I/O page.

TEST - Causes the ROM code startup self-test to run continously in a loop. Use this command for troubleshooting and analyzing intermittent CPU problems. <CTRL> C exits the loop.

2.5 KDJ11-B SETUP MODE

Table 2-5 lists the setup mode commands. A discussion of the features of each setup command follows the table. This discussion refers to versi 7 ROMs only. Refer to Appendix G for a comparison of version 6 and versi 7 ROMS. Refer to the KDJ11-B CPU User's Guide for more information.

Enter these commands by using the command numbers.

Table 2-5 Setup Mode Commands

Command	Description
1	Exit.
2	List/change parameters in the setup table.
3	List/change boot translation in setup table.
4	List/change the automatic boot selection in the setup table.
5	Reserved
6	List/change the switch boot selection in the setup table.
7	List boot programs.
8	Initialize the setup table.
9	Save the setup table into the EEPROM.
10	Load EEPROM data into the setup table.
11	Delete an EEPROM boot.
12	Load an EEPROM boot into memory.
13	Edit/create an EEPROM boot.
14	Save boot into the EEPROM.
15	Enter ROM ODT.

NOTE
ROM ODT is different from J11 micro ODT. Refer to Chapter 4, Diagnostics, Section 4.6, for a discussion and listing of J11 micro ODT hardware commands.

2.5.1 Setup Command 1: EXIT

This command returns you to dialog mode. Same as <CTRL> C.

2.5.2 Setup Command 2: List/Change Parameters In The Setup Table

During system power-up, the ROM program code copies the setup parameters into memory starting at address 2000. This area in memory is called the setup table.

You can use this table to set 15 CPU parameters (letters A -O). The ROM code prints out the current status of all parameters, repeats the first parameter, and then prompts you for input.

Keep pressing the Return Key until you reach the parameter you want, or go directly to the parameter by typing the letter shown in the setup table menu. To change a parameter, type in the new value and press the Return Key. Type ^ or - to back up to the previous parameter. If there is no change, press the Return Key to advance to the next selection. Use <CTRL> Z to exit.

This command does not save these values in the setup table in the EEPROM. Use setup command 9 to save the setup table into the EEPROM.

Table 2-6 shows the default values of the parameters.

Table 2-6 KDJ11-B Setup Default Parameter Values

A - Enable Halt on break			0=No	1=Yes	=0
B - Disable User friendly format			0-No	1=Yes	=0
C - ANSI Video terminal (1)			0=No	1=Yes	=1
D - Power up	0=Dialog	1=Automatic	2=ODT	3=24	=1
E - Restart	0=Dialog	1=Automatic	2=ODT	3=24	=1
F - Ignore battery			0=NO	1=Yes	=0
G - PMG count				(0 - 7)	=7
H - Disable clock CSR			0=NO	1=Yes	=0
I - Force Clock interrupts			0=No	1=Yes	=0
J - Clock	0=Power supply	1=50Hz	2=60Hz	3=80Hz	=0
K - Enable ECC test			0=No	1=Yes	=1
L - Disable long memory test			0=No	1=Yes	=0
M - Disable ROM	0=No	1=Dis 165	2=Dis 173	3=Both	=0
N - Enable trap on halt			0=No	1=Yes	=0
O - Allow alternate boot block			0=No	1=Yes	=0

A: Enable Halt on break - When this parameter is set to 0 (default setting), a break condition from the console terminal is ignored. When this parameter is set to 1, the processor halts when you press the break key on the console terminal.

B: Disable user-friendly format - When this parameter is set to 0 (default setting), the system sends user-friendly messages to the console terminal. This paramater is normally used with automatic boot mode.

C: ANSI Video terminal - Set this parameter to 1 (default setting) when your console terminal is an ANSI video terminal such as a VT220. The delete key erases the previous character on the screen. Set this parameter to 0 when you have a hard-copy console or a non-ANSI video terminal, such as the VT52. The delete key enters a slash character.

D: Power up mode and E - Restart mode - (Two seperate parameters) When the ROM code starts it determines if the power up or restart switch was activated. In either cases, the ROM code selects the mode as shown in Table 2-7.

Table 2-7 ROM Code Mode Selections

Value	Mode
0	Enters dialog mode at completion of the diagnostics.
1	Enters automatic boot mode at completion of diagnostics and tries to boot a previously selected device (default setting).
2	Enters ODT (on-line debugging technique) mode at completion of a limited set of tests. The ROM code executes a halt instruction and passes control to J11 micro ODT (see Chapter 4, Diagnostics, Section 4.6).
3	Enters 24 mode. The ROM code loads the PSW (processor status word) with the contents of location 26 and then jumps (passes control) to the address stored in location 24. You can use this mode to recover from a power failure when battery backup memory or nonvolatile memory is present.

F: Ignore battery - The ROM program uses this parameter only when power up or restart mode (see D and E) is set to 3 (24 mode). When set to 0 (default setting), the memory battery OK signal must be present to execute 24 mode. You can set this parameter to 1 to ignore the memory battery OK signal if you have non-volatile memory.

G: PMG (processor mastership grant) count - Make sure this parameter is set to 7 for normal operation. Do not set this parameter to 0.

This parameter sets the PMG count in the BCSR (boot control and status register). The PMG count allows the processor to perform a memory transfer and thus execute instructions periodically during DMA transfers. Table 2-8 shows how often the processor can perform a memory transfer during a DMA.

Table 2-8 PMG Count Settings

Value	Time for counter to overflow
0	Disabled
1	0.4 us
2	0.8 us
3	1.6 us
4	3.2 us
5	6.4 us
6	12.8 us
7	25.6 us (newer factory setting)

H: **Disable clock CSR** - When set to 0 (default setting), this command enables the clock CSR to interrupt the system. When set to 1, this command disables the clock CSR at address 17777546.

I: **Force clock interrupts** - When this parameter is set to 0 (default setting), the clock requests interrupts only when the clock CSR is enabled (see default value). If you set this parameter to 1, the clock unconditionally request interrupts when the processor priority is 5 or less. When set to 1, always disable the clock CSR.

J: **Clock select** - This parameter determines the source of the clock signal as shown in Table 2-9.

Table 2-9 Clock signal Sources

Value	Source
0	Clock signal from backplane pin BR1. The power supply normally drives this signal at 50 or at 60Hz, the default setting.
1	Clock signal generated internally at 50Hz.
2	Clock signal generated internally at 60Hz.
3	Clock signal generated internally at 800Hz.

K: **Enable ECC test** - When this parameter is set to 1 (default setting), the power-up and self-test runs the ECC (error correction code) memory test if the memory is of the ECC type (bit 4 or the memory CSR is a read/write bit). When set to 0, the ROM code bypasses the ECC test.

L: **Disable long memory test** - When this parameter is set to 0 (default setting), the processor runs a memory address shorts data test on all available memory. When this parameter is set to 1, the memory address shorts data test is bypassed for all memory above 256K bytes.

M: **Disable ROM** - The boot ROM occupies two 256 word blocks in the I/O address space. This parameter allows you to disable the ROM after a device boots, and to free this address space for use by special-purpose peripheral devices. Table 2-10 lists the ROM addresses that can be disabled.

Table 2-10 ROM Addresses Disabled

Parameter Value	ROM addresses disabled
0*	None
1	17765000-17765777
2	17773000-17773777
3	17765000-17765777 and 17773000-17773777

* Default setting

N: **Enable trap on halt** - When this parameter is set to 0 (default setting), the processor enters micro ODT if it executes a halt instruction while in Kernal mode. When this parameter is set to 1, the processor jumps to location 4 if it executes a halt instruction while in kernal mode.

O: **Allow alternate boot block** - The boot ROM code checks for bootable media on a device by loading the boot block from the device into memory and testing it. When set to 0 (default setting), the ROM code considers the medium bootable if the word at location 0 is between 240 and 277, and the word at location 2 is between 400 and 777. If the medium is bootable then the ROM code jumnps to location 0 of the boot block.

When set to 1, the ROM code considers the medium bootable if the word at location 0 is any nonzero number. Some non-Digital operating systems may require a setting of 1 to boot properly.

2.5.3 Setup Command 3: List/Change Boot Translation In The Setup Table

This command lists the contents of the translation table and allows you to specify nonstandard addresses for boot devices. It provides the following functions:

- Allows devices to be booted using nonstandard addresses.
- Allows CSR address changes when two or more devices share the same address.
- Allows multiple MSCP devices with different controllers to boot.
- Handles multiple controllers of the same type.

When the boot ROM code attempts to boot from a device, it uses the standard CSR address for that device unless a different address has been specified.

The following example shows a system with these devices:

- RD52 fixed-disk drive
- RX50 dual-diskette drive
- RC25 fixed and removable disk drive

To change an entry, type the device name, the unit number, and the CSR address. Press the Return key to proceed to the next entry. Type <CTRL> Z to return to the setup mode prompt.

The RX50 and RD52 use an RQDX1 controller module at the standard CSR address of 17772150. The RC25 controller module also uses a standard CSR address of 17772150. Since two devices cannot use the same CSR address, the CSR jumpers on one module must be changed. In this example the RC25 controller is set to respond to a non-standard address of 177760500.

The RD52 is unit 0 and the RX50 is unit 1 and 2. The RC25 contains two drives, so it has two unit numbers. On its front panel, the RC25 has a unit number select plug that is set for units 4 and 5 (the first unit number of an RC25 is always an even number). Since the RC25 has two units numbers, the translation table has two entries:

```
TT1     blank
Device name     = DU
Unit number     = 4
CSR address     = 17760500
TT1     DU4 address 17760500

TT2     blank
Device name     = DU
Unit number     = 5
CSR address     = 17760500
TT2     DU5 address 17760500

TT3     blank
Device name     = Press RETURN for no change
```

2.5.4 Setup Command 4: List/Change The Automatic Boot Selection in Setup Table

This command allows you to select the devices to be tried by the automatic boot sequence. The table allows up to six entries. For each entry, you specify the device mnemonic, the unit number, and the order to try to boot the devices. There are three special single-letter device names, A, B, and E.

A: MCSP automatic boot. Causes the ROM code to find up to eight MSCP devices (units 0 -7) at the standard CSR address. The ROM code first tries each removable media device in turn and then tries each fixed media device.

You must select MSCP devices with a nonstandard CSR address (setup command 3) individually.

B: An off-board boot. Causes the ROM code to boot from an off board ROM at address 17773000. The code checks that the ROM exists and that the first word is not zero. Then it disables the internal code and jumps to address 17773000 of the off-board ROM.

NOTE
Device name B implements a method of supporting non-Digital Equipment Corporation boot devices on the Q22-Bus.

E: Exit automatic boot. Signals the ROM code that there are no other devices to try. Follow the last device to be tried with this entry when fewer than six devices exist.

2.5.5 Setup Command 5: Reserved

The command is reserved for future use.

2.5.6 Setup Command 6: List/Change the Switch Boot Selection

This command allows you to define the value of switches 2, 3, and 4 of the E83 DIP switch in order to select a specific boot device. You can use this command to specify boot devices for six combinations of these switches. When these three switches are set to OFF (default setting), the EEPROM selects the boot device.

When switch 5 is set to Off and the baud rate select switch is set to 8 or greater, the ROM code overrides any settings for switches 2, 3, and 4 and it enters dialog mode.

2.5.7 Setup Command 7: List Boot Programs

This command displays a list of all the boot programs in the two EPROMS and the EEPROM. It displays the device mnemonic, unit number range, source of the program (EPROM or EEPROM), and a short device description. Same as the dialog modes LIST command.

2.5.8 Setup Command 8: Initialize the Setup Table

This command sets the current parameters of the setup table in memory to the dafault values. It does not affect the contents of the EEPROM itself. To save these values in the EEPROM you must execute the save command (setup command 9).

2.5.9 Setup Command 9: Save the Setup Table Into the EEPROM

This command copies the parameter values of the setup table in memory to the EEPROM. This is the only command that actually writes anything into the first 105 bytes of the EEPROM.

2.5.10 Setup Command 10: Load EEPROM Data into the Setup Table

This command restores the setup table in memory with the values actually stored in the EEPROM.

2.5.11 Setup Command 11: Delete EEPROM Boot

This command allows you to delete custom boot programs that you have stored in the EEPROM. After typing the command, the program prompts you for the device name of the EEPROM boot to be deleted. The ROM code then searches for the first boot program in the EEPROM. If the ROM code finds the boot program, it deletes the program and moves all of the following boot programs up to use the space made available by the deleted program.

2.5.12 Setup command 12: Load an EEPROM Boot into Memory

This command allows you to load an EEPROM boot program into memory to examine or edit it. The ROM code prompts you for the device name of the EEPROM boot.

2.5.13 Setup Command 13: Edit/Create and EEPROM Boot

This command allows you to create a new EEPROM boot program or to edit a program previously loaded with setup command 12. Use this command to change the following:

- Device name: Designated by the firmware for the Device; for example, DU (disk unit).
- Device description: description — Normally the physical name of the device. The maximum length allowed for this description is 11 characters and spaces.
- Allowable unit number range: — The highest unit number defines the allowable range of valid unit numbers for the device.
- Begining address of the program in memory: — First location of the program in memory
- Ending address of the program in memory: — The address of the last byte of code used in memory.
- Starting address of the program: — The address the ROM code passes control to.

The command lists the available space in the EEPROM for boots and prompts you for entries. After you have made all changes, the ROM code then enters ROM ODT to allow you to enter the boot program (see setup command 15). You must use setup command 14 to save any changes you have made.

2.5.14 Setup Command 14: Save Boot into EEPROM

This is the only command that actually writes a boot from memory into the EEPROM. Other commands only change a copy of the boot program that resides in memory. When saving a boot program into memory, the device name of the program must not match the name of a program already existing in the EEPROM. If two or more programs are written into the EEPROM with the same name only the first one is bootable.

2.5.15 Setup Command 15: Enter ROM ODT

This commands puts you into ROM ODT. The ROM code opens the address defined by the beginning address of the program. ROM ODT is not the same as J11 micro ODT.

The only allowable addresses in ROM ODT are the addresses of memory from 0 - 28 Kwords (0 - 00157776). You can not access any other addresses or the I/O page from ROM ODT. Table 2-11 provides the ROM ODT commands. (Refer to the KDJ11-BC CPU User's Guide for further information.)

Table 2-11 ROM ODT Commands

Command	Symbol	Use
Slash	/	Prints contents of specified address location or prints contents of last opened location. If opened location is an odd number, prints only the contents of the byte. If location is even, mode is even. If location is odd, mode is byte. Assumes leading zeros. Uses only the last six octal digits.

Table 2-11 (cont.)ROM ODT Commands

Command	Symbol	Use
Examples: ROM ODT > 200/1000000 ROM ODT > 1001/240 ROM ODT > 77777750020/100000 ROM ODT > 77770000/ ROM ODT >		; Open location 200 ; Open byte location 1001 ; Open location 00150020 ; Illegal location > 157776
RETURN	<CR>	Closes an open location.
LINE FEED	<LF>	Closes an open location and then opens the next location. If in word mode, increment by 2, if byte mode, increment by 1.
Period	.	Alternate character for line feed. This command is useful when the terminal is a VT220.
Up arrow	^	Closes an open location and then opens the previous location. If in word mode, decrement by 2, if byte mode, decrement by 1.
Minus	-	Alternate character for up arrow. Useful when the terminal is a VT200.
Delete	DELETE	Deletes the previous character typed.
CRTL Z	^Z	Exit ROM ODT and return to setup mode.

2.6 MSV11-P MEMORY MODULE (PK,-PL)

The MSV11-P memory is a quad-height module that occupies the slot adjacent to the CPU. This module contains 64K MOS chips that provide storage for 18-bit words (16 data bits and 2 parity bits). It also contains parity control circuitry and a control status register (CSR). Table 2-12 shows the memory modules and their storage capacity.

Table 2-12 MSV11-P Memory Modules

Model	Module Number	Memory Capacity
MSV11-PK	M8067-K	2.956K bytes
MSV11-PL	M8067-L	512.9K bytes

The MSV11-P memory module is configured by means of jumpers and wire-wrap pins. The -PK and -PL models have the same factory configuration. Figure 2-4 shows the location of jumpers and wire-wrap pins and Table 2-13 describes their function.

Figure 2-4 MSV11-P Module Layout

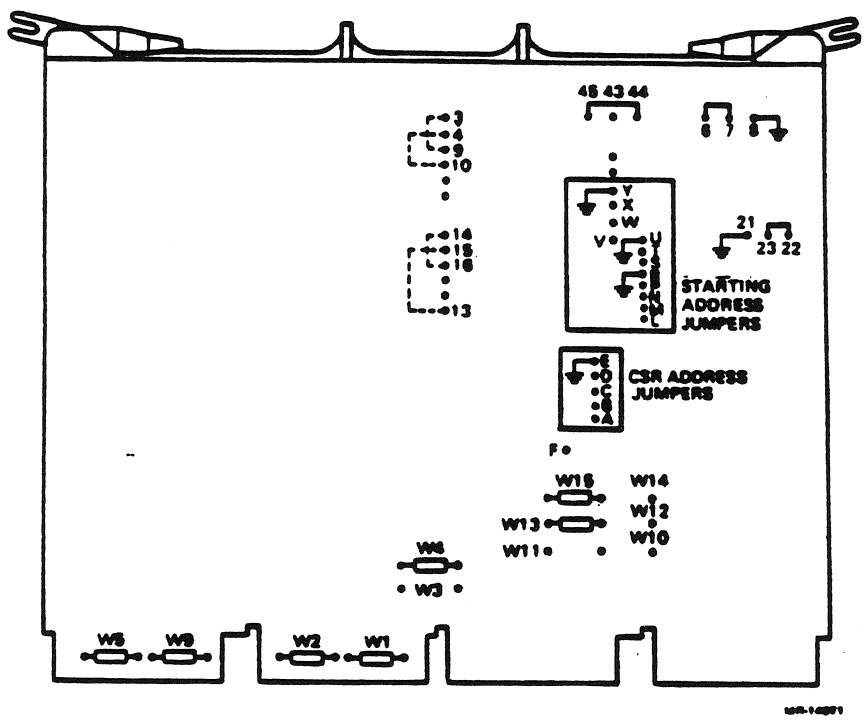


Table 2-13 MSV11-P Factory Jumper Configuration

Jumpers	State	Jumpered Pins	State
W1	I	2 to Y	R
W2	I	3 to 9	I
W3	R	4 to 10	I
W4	I	6 to 7	I
W5	I	13 to 15	I
		14 to 16	I
W9	I	22 to 23	I
W10	R	44 to 45	I
W11	R		
W12	R	A to E	R
W13	I	B to E	R
W14	R	C to E	R
W15	R	D to E	R
Ground pins		L to R	R
		M to R	R
8		N to R	R
21		P to R	R
E			
R		V to Y	R
U		W to Y	R
Y		X to Y	R

I = inserted R = removed

Two LEDs indicate module status. When lit, a green LED indicates that +5vdc is present on the module; when lit, a red LED indicates the detection of a parity error.

2.6.1 Expansion (CSR and Starting Addresses)

Additional MSV11-P modules can be added for system expansion. Each memory module added to a system requires a specific configuration. This is done by repositioning jumpers on the module's wire-wrap pins.

Each memory module added to the Q22-Bus must be configured to provide two addresses:

1. CSR address
2. Starting address

2.6.1.1 CSR Address

Figure 2-4 shows the CSR address jumpers on the MSV11-P. Table 2-14 lists the CSR address and corresponding jumper configurations for each memory module added to the system. The table is applicable to both the -PK and -PL models.

Table 2-14 MSV11-P CSR Configuration

Board # in System	Pins to Wire Wrap	CSR Address (X = 177721)
1st	None	x00
2nd	A to E	x02
3rd	B to E	x04
4th	A to B, B to E	x06
5th	C to E	x10
6th	A to C, C to E	x12
7th	B to C, C to E	x14
8th	A to B, B to C, C to E	x16

2.6.1.2 Starting Address

The starting address depends on the amount of memory already in the system. Table 2-15 lists the jumper configuration for additional MSV11-P modules.

Table 2-15 MSV11-P Starting Address Configuration

MSV11-PL (512kb increments)	
Board No. in System	Pins to Wire Wrap
1st	none
2nd	V to Y
3rd	W to Y
4th	V to Y, W to Y
5th	X to Y
6th	X to Y, V to Y
7th	X to Y, W to Y
8th	X to Y, W to Y V to Y

Table 2-15 (cont.) MSV11-P Starting Address Configuration

MSV11-PK (256kb increments)	
Board No. in System	Pins to Wire Wrap
1st	None
2nd	P to R
3rd	V to Y
4th	V to Y, P to R
5th	W to Y
6th	W to Y, P to R
7th	W to Y, V to Y
8th	W to Y, V to Y, P to R

For further information, refer to the MSV11-P User's Guide (EK-MSVOP-UG-001).

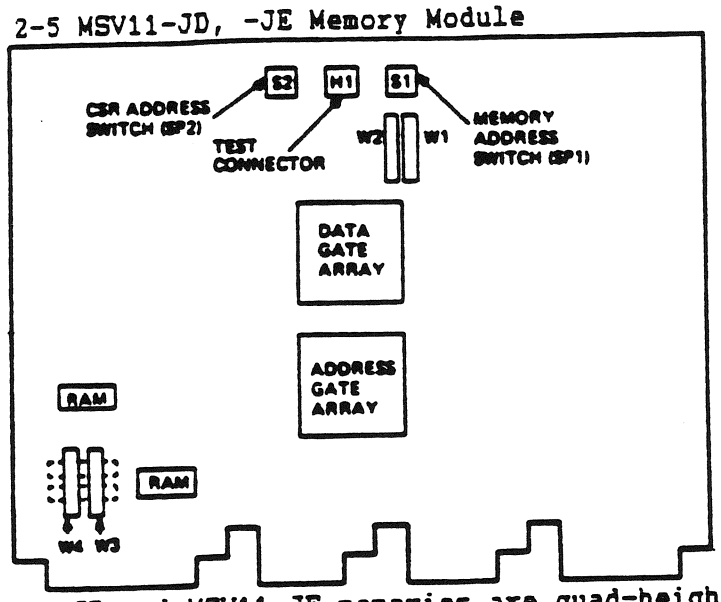
2.7 MSV11-JD and MSV11-JE MEMORY MODULES (M8637)

The MSV11-JD, -JE (Figure 2-5) is a metal oxide semiconductor (MOS), random access memory (RAM). The module has:

- Error detection and correction (ECC) for increased reliability
- A control and status register (CSR) to store status and error information
- Battery backup, available by resetting a jumper on the module.
- Support for private memory interconnect (PMI) protocol and normal Q22-Bus protocol
- Four jumpers and two switch packs
- Starting addresses on 8 KW boundaries
- Two LEDs

The board can be configured half or fully poplulated with 256 K dynamic RAMs. Maximum memory capacity is 2 MB using 256K RAMs.

Figure 2-5 MSV11-JD, -JE Memory Module



The MSV11-JD and MSV11-JE memories are quad-height Q22-Bus modules that occupy the slot(s) immediately prior to the KDJ11-BF CPU in the backplane assembly. They are available in the factory configuration shown in Table 2-16.

Table 2-16 MSV11-JD, -JE Memory Modules*

Option Number	Module Designation	Description
MSV11-JD	M8637-D	1 MB ECC using 256K dynamic RAMs
MSV11-JE	M8637-E	2 MB ECC using 256K dynamic RAMs

* MSV11-JB, -JC modules are used on MicorPDP-11/84 Unibus systems only. They can not be used on Q22-Bus systems.

The memory starting address can be set in any 8KW boundry within the 2048 KW extended address space. The extended address space contains 22 address lines.

2.7.1 Error Correction

The MSV11-JD, -JE contain ECC logic which detects and corrects single-bit errors and detects double-bit errors. Detecting and correcting single-bit errors is transparent to the master device accessing the memory.

2.7.2 Battery Backup

The MSV11-JD, -JE memory module has input for two sources of +5 V power. These inputs are designated +5 VBB (on battery back-up power systems) and +5 V (on non-battery back-up power systems).

NOTE
Neither the BA23-A nor the BA123-A MicroPDP-11 systems support battery backup.

In battery support mode, power is used only to refresh the MOS storage array so that battery backup and data retention time is maximized. A green LED on the module stays on as long as +5 V or +5 VBB is available. Modules are shipped in a non-battery backed-up configuration (Figure 2-6). The modules need a jumper change to configure them for battery backed-up applications (Figure 2-7).

Figure 2-6 +5 V Jumper Connections

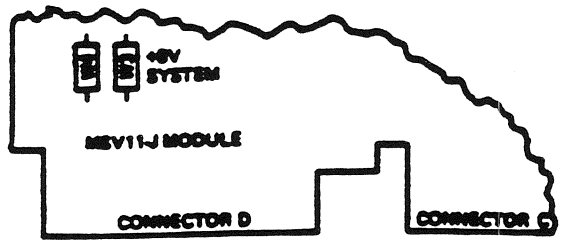
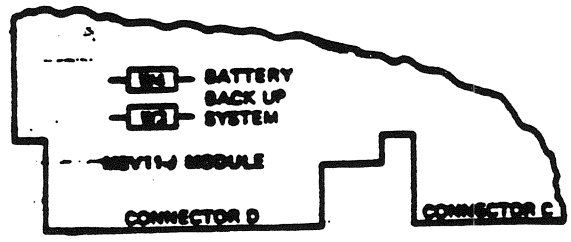


Figure 2-7 +5 VBB Battery Backup Jumper Connections



2.7.3 Private Memory Interconnect (PMI)

The MSV11-JD, -JE memories are designed for Q22-Bus systems and support the PMI protocol of the KDJ11-BF processor. The PMI bus is specifically designed for and used in the MicroPDP-11/83 Q22-Bus systems.

The MicroPDP-11/83 systems use the KDJ11-BF CPU module, one or more MSV11-JD of MSV11-JE memory modules and a selection of Q22-Bus compatible devices. Data transfers between the KDJ11-BF CPU and the MSV11-JD or -JE memory using the PMI protocol resident on the CPU. All other communications, whether originated by the CPU or other bus master, use the Q22-Bus protocol.

2.7.4 Location of the MSV11-JD, -JE Memory

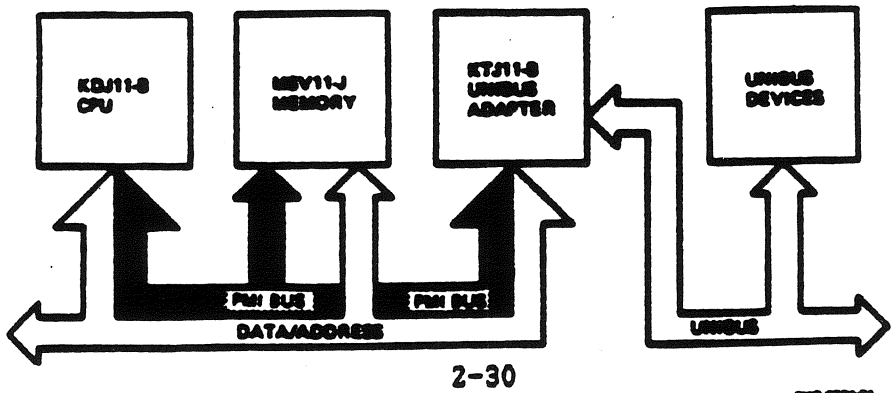
The location of the MSV11-JD, -JE in the MicroPDP-11/83 backplane determines the protocol used between the KDJ11-BF processor and the memory module (Figure 2-8). To use the PMI protocol, the MSV11-JD, -JE must be located immediatly in front (lower slot number) of the CPU; otherwise the memory and CPU communicate with the Q22-Bus protocol. There must be no open slot between memory and the CPU.

CAUTION
Static chartges can damage the MOS memory chips. Be careful how you handle the module and where you lay it down.

When you insall or remove the memory module, make sure there is no dc voltage applied to the module.

If the green LED is on, the module is receiving +5 V or +5 VBB power. The power source must be off before you remove or replace a memory module.

Figure 2-8 PMI/Q22-Bus Interface



2.7.5 Jumper Setting

The four factory installed jumpers (Figure 2-5), W1 through W4, establish the configuration of the module. Table 2-17 summarizes the possible MSV11-JD, -JE jumper configurations.

Table 2-17 MSV11-JD, JE Jumper Configurations

Jumper	Description
W1 In	Reserved ro Digital use only
W1 Out	256 K dynamic RAMs
W2 In	Half popluated module
W2 Out	Fully populated module
W3, W4 mounted left-right (Figure 2-7)	+5 VBB Battery backup system (see Note)
W3, W4 mounted up-down (Figure 2-6)	+5 V system (factory configuration)

NOTE
Neither the BA23-A nor the BA123-A MicroPDP-11 systems support battery backup

2.7.6 MSV11-JD, -JE Switch Settings

The MSV11-JD, -JE modules contain two switchpacks. One is an 8-switch DIP (dual in-line package) and one is a 4-switch DIP. The 8-switch DIP selects the starting memory address on an 8K boundary. The 4-switch DIP selects the CSR starting address. One of 16 possible CSR addresses may be selected.

2.7.7 Memory Address Switch Settings

The memory address switch (SP1 in Figure 2-5) is an 8-switch DIP. The switch settings are shown in Table 2-18. The table is divided into 3 columns as follows:

- The decimal switch setting in 8K increments
- The octal equivalent
- The actual switch settings shown in binary

The least four significant switch settings (5 through 8) of the memory address switch (SP1) represent 8K increments as shown in the upper half of Table 2-18. Switch setting 1 through 4 are all 0s in this portion of the table and do not come into play until 128K is reached.

For example, if these switch settings (5 through 8) are 0s, a memory address of 0 is represented. This assumes that switches 1 through 4 are also 0.

If switch setting 8 is a 1 (all others being 0s), the memory address increments by 8K.

If switch setting 7 is a 1 (all others being 0s), the memory address increments by another 8K.

The lower half of the table represents increments of 128K until 2 M is reached. Switch settings 4 through 8 come into playe here. Each increment of these switch settings represents an increase of 128K.

For example, if switch setting 4 is a 1 and switch settings 3 through 1 are 0s, a starting memory address range of 128K to 248K is selected.

The specific memory starting address selected within that range is determined by switch settings 8 through 5 (indicated by Xs in the lower half of Table 2-18.

Table 2-18 MSV11-JD, -JE Starting Memory Address Selection

Decimal (K word)	Octal	Switch Setting (SP1) 1 2 3 4 5 6 7 8
0	00000000	0 0 0 0 0 0 0 0
8	00040000	0 0 0 0 0 0 0 1
16	00100000	0 0 0 0 0 0 1 0
24	00140000	0 0 0 0 0 0 1 1
32	00200000	0 0 0 0 0 1 0 0
40	00240000	0 0 0 0 0 1 0 1
48	00300000	0 0 0 0 0 1 1 0
56	00340000	0 0 0 0 0 1 1 1
64	00400000	0 0 0 0 1 0 0 0
72	00430000	0 0 0 0 1 0 0 1
80	00500000	0 0 0 0 1 0 1 0
88	00540000	0 0 0 0 1 0 1 1
96	00600000	0 0 0 0 1 1 0 0
104	00640000	0 0 0 0 1 1 0 1
112	00700000	0 0 0 0 1 1 1 0
120	00740000	0 0 0 0 1 1 1 1
000-120	00000000-00740000	0 0 0 0 X X X X
128-248	01000000-01740000	0 0 0 1 X X X X
256-376	02000000-02740000	0 0 1 0 X X X X
384-504	03000000-03740000	0 0 1 1 X X X X
512-632	04000000-04740000	0 1 0 0 X X X X
640-760	05000000-05740000	0 1 0 1 X X X X
768-888	06000000-06740000	0 1 1 0 X X X X
896-1016	07000000-07740000	0 1 1 1 X X X X
1024-1144	10000000-10740000	1 0 0 0 X X X X
1152-1272	11000000-11740000	1 0 0 1 X X X X
1280-1400	12000000-12740000	1 0 1 0 X X X X
1408-1528	13000000-13740000	1 0 1 1 X X X X
1536-1656	14000000-14740000	1 1 0 0 X X X X
1664-1784	15000000-15740000	1 1 0 1 X X X X
1792-1912	16000000-16740000	1 1 1 0 X X X X
1920-2040	17000000-17740000	1 1 1 1 X X X X

1 = Switch on
0 = Switch off
X = Switch can be either on of off

Table 2-19 shows the most common configurations for the MSV11-JD and MSV11-JE memory address switches.

Table 2-19 Common Memory Starting Address, MSV11-J

MSV11-JD:	Starting Address	SW2 Switches 1 2 3 4 5 6 7 8
	0	0 0 0 0 0 0 0 0
	1 Mbyte	0 1 0 0 0 0 0 0
	2 Mbyte	1 0 0 0 0 0 0 0
	3 Mbyte	1 1 0 0 0 0 0 0
MSV11-JE:		
	0	0 0 0 0 0 0 0 0
	2 Mybtes	1 0 0 0 0 0 0 0

2.7.8 CSR Address Switch Settings

The Control and status register of the MSV11-JD, -JE allows program control of certain ECC functions and contains diagnostic infomation if an error has occurred. The CSR is a 16-bit register and has an assigned address. The CSR can be accessed through the Q22-Bus or PMI protocol.

ECC is performed only on memory accesses and is not used when accessing the CSR.

There is one CSR per memory module. Each CSR can be assigned to one of 16 predetermined addresses which range from 772100 to 772136 for 18-bit systems and from 17772100 to 17772136 for 22-bit systems.

The CSR address switch (Figure 2-5) is a 4-switch DIP which allows selection of one of these 16 CSR addresses. Table 2-20 shows the possible CSR address for 18-bit and 22-bit systems. The switch setting for a particular CSR address is the same whether the CSR is an 18-bit or 22-bit system.

For example, the switch setting is 1110 for a 22-bit CSR address of 17772134 or an 18-bit CSR address of 772134.

Table 2-20 M

22-Bit CSR Address
17772100
17772102
17772104
17772106
17772110
17772112
17772114
17772116
17772120
17772122
17772124
17772126
17772130
17772132
17772134
17772136

1 = Swi
0 = Swi

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Table 2-20 MSV11-J CSR Address Selection

22-Bit CSR Address	18-Bit CSR Address	Switch Setting 1 2 3 4
17772100	772100	0 0 0 0
17772102	772102	0 0 0 1
17772104	772104	0 0 1 0
17772106	772106	0 0 1 1
17772110	772110	0 1 0 0
17772112	772112	0 1 0 1
17772114	772114	0 1 1 0
17772116	772116	0 1 1 1
17772120	772120	1 0 0 0
17772122	772122	1 0 0 1
17772124	772124	1 0 1 0
17772126	772126	1 0 1 1
17772130	772130	1 1 0 0
17772132	772132	1 1 0 1
17772134	772134	1 1 1 0
17772136	772136	1 1 1 1

1 = Switch on
0 = Switch off

2.7.9 MSV11-JD, -JE LEDs

Two LEDs on the MSV11-JD, -JE modules indicate power and error conditions (Figure 2-5). The green LED indicates that the module is receiving +5 V, or +5 VBB from the power supply or battery backup. The power source must be off before you remove or replace a memory module.

The red LED indicates the detection of an uncorrectable single or double error when the module is in a read/write cycle or in diagnostic mode. Refer to the MSV11-J MOS Memory User's Guide (EK-MSV1J-UG-001) for further details.

2.8. MSV11-Q MEMORY

The MSV11-Q is a Q22-bus quad-height memory module with a 1, 2, or 4 Mbyte capacity using either 64K or 256K dynamic RAMs. There are two revision levels (Figures 2-9, 2-10) and three variants, listed in Table 2-21

Table 2-21 MSV11-Q Variants

Revision Level	Model	Number	Storage	RAM size
A,C *	MSV11-QA	M7551-AA	1 MB	56K
C	-QB	-BA	2 MB	256K (half pop.)
C	-QC	-CA	4 MB	256K (full pop.)

* Revision level is identifiable by printed circuit board number:
A = 5017547A1 on upper right corner of component side
C = 5017547-01-C1 on upper left corner of component side.

Figure 2-5 MSV11-QA Memory, Revision A

TBS

Figure 2-6 MSV11-QA, -QB, -QC Memory, Revision C

TBS

The MSV11-Q has a red LED. When lit, it indicates a parity error.

2.8.1 MSV11-Q Address Switches

Configure the MSV11-Q starting and ending addresses using DIP switches SW1 and SW2. Table 2-22 lists the switch settings.

Table 2-22 MSV11-Q Address Switches

Version	Board # in system	Starting Address SW1 4	SW1 5	SW2 6	Ending Address SW2 4	SW2 5
MSV11-QA Rev. A	1	0	0	0	1	1
	2	1	1	1	0	1
	3	0	1	1	1	0
	4	1	0	1	0	0

0 = switch ON
1 = switch OFF

SW2 switches 1,2 and 3 are all ON.
SW1 switches 1,2 and 3 are all ON. SW1 switch 6 is NOT USED.

Table 2-22 MSV11-Q Address Switches

Version	Board # in system	SW2 4	SW2 5	SW1 6	SW1 4	SW1 5
MSV11-QA Rev. C	1	0	0	0	1	1
	2	1	1	1	0	1
	3	0	1	1	1	0
	4	1	0	1	0	0
MSV11-QB Rev. C	1	0	0	0	0	1
	2	0	1	1	0	0
MSV11-QC Rev. C	1	0	0	0	0	0

0 = switch ON
1 = switch OFF

SW1 switches 1,2 and 3 are all ON.
SW2 switches 1.2, and 3 are all ON. SW2 switch 6 is NOT USED.

2.8.2 MSV11-Q CSR Address

The MSV11-Q CSR address is set using jumpers. Table 2-23 lists the settings.

Table 2-23 MSV11-Q CSR Address (cont.)

	Board # in system	Jumpers R	Jumpers P	Jumpers N	Jumpers M	CSR Address x = 177721
Rev. A						
Rev. C		J4 to J5	J6 to J7	J8 to J9	J10 to J11	
	1	in	in	in	in	x00 *
	2	out	in	in	in	x02
	3	in	out	in	in	x04
	4	out	out	in	in	x06

* factory configuration

Table 2-24 lists the remaining jumpers and their function.

Table 2-24 MSV11-Q Factory Jumper Settings

Rev. A

Jumper	State	Location	Condition
W1	IN	W1/W2 (upper)	block mode enabled
W6	IN	W5/W6 (horizontal)	manf. test (do not remove)
B	IN	A/B (lower)	CSR selection enabled
C	IN	C/D (vertical)	manf. test (do not remove)
H	IN	J/H (right)	parity error detection enabled
L	IN	K/L (lower)	22 bit addressing selected

Rev. C

Jumper	State	Condition
J1 to J2,	IN	manf. test (do not remove)
-QA only:		
J13 to J14	IN	selects 64K RAMs (do not remove)
J15 to J16	IN	selects 64K RAMs (do not remove)
-QB, -QC:		
J16 to J17	IN	selects 256K RAMs (do not remove)
J12 to J13	IN	selects 256K RAMs (do not remove)
W3, W1	IN	battery backup configuration

For further information, refer to the MSV11-Q MOS Memory User's Guide (EK-MSV1Q-QG).