

EK-DZQ11-MC-002

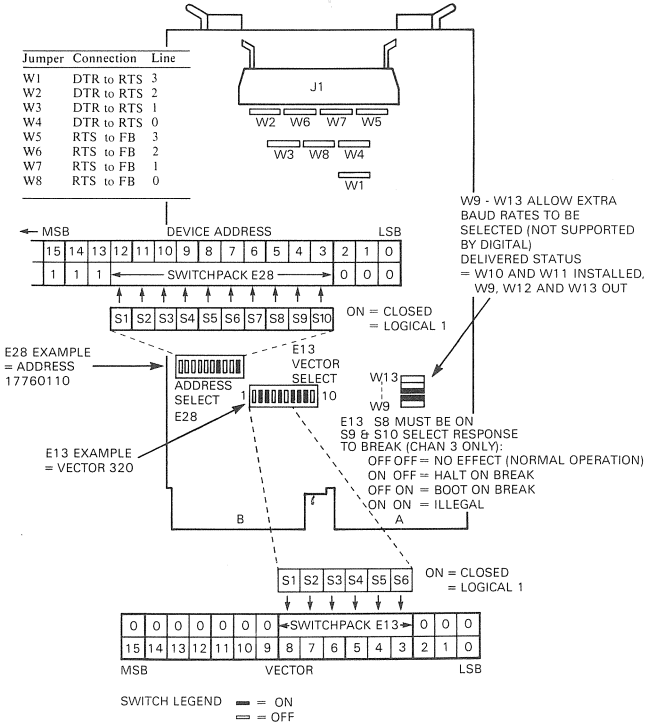
DZQ11

Maintenance Card

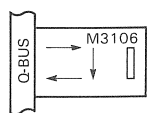
WARNING

Some of the procedures described on this card call for the removal of system covers. Such procedures should only be performed by suitably trained personnel. For the user, this material is provided for information only.

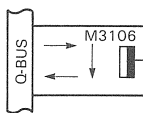
JUMPER AND SWITCH LAYOUT - VERSION 1



DZQ11 TEST CONFIGURATIONS FOR MicroVAX

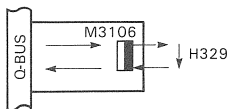


(CONFIGURATION A)



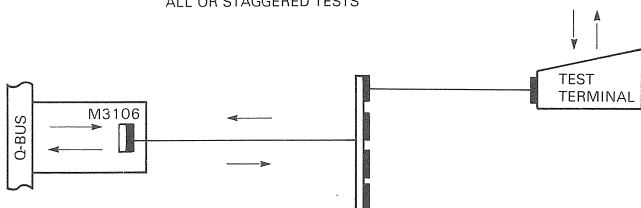
(CONFIGURATION B)

INTERNAL/DEFAULT OR MACROVERIFY TESTS



(CONFIGURATION C)

ALL OR STAGGERED TESTS



(CONFIGURATION D)

ECHO TEST

RD1909

MINIMUM REQUIREMENTS FOR EHKMV AND EHXDZ

EHKMV (MACROVERIFY) – MicroVAX with 30Kbyte Memory

EHXDZ – MicroVAX with DZQ11 and 512Kbyte Memory

- Terminal for Echo Test
- H329 Test Connector

DIAGNOSTICS (PDP-11)

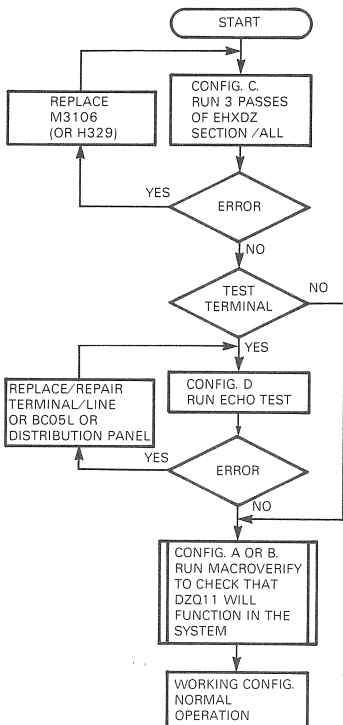
CVDZA	DZQ11 Logic Test – Part 1
CVDZB	DZQ11 Logic Test – Part 2
CVDZC	DZQ11 Cable/Echo Test
DVDZD	Overlay for ITEP
DZITA	Interprocessor Test Program (ITEP)
CXDZB	DECX/11 Module

DIAGNOSTICS (MicroVAX)

EHXDZ DZQ11 Test

EHKMV Macroverify MicroVAX System

TROUBLESHOOTING FLOWCHART FOR MicroVAX SYSTEMS



SECTIONS

Default = Tests 1 to 19

Internal = Tests 1 to 19

Staggered = Tests 20 and 21

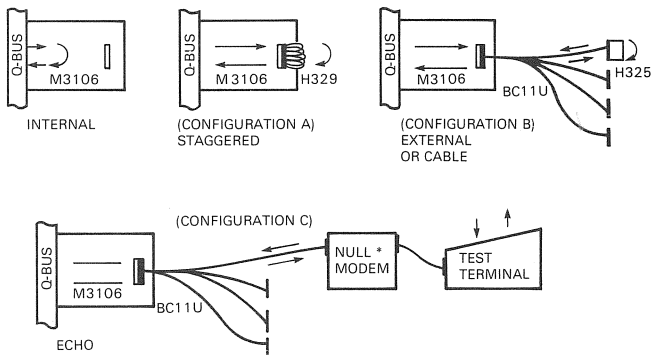
Modem = Test 20 only

All = Tests 1 to 21

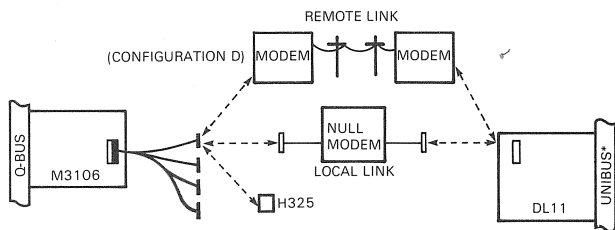
Echo = Test 22 only

Any configuration (A,B,C or D) can be used if Default/Internal Group of Tests is to be run.

DZQ11 TEST CONFIGURATIONS FOR PDP-11 SYSTEMS (EXAMPLES SHOW BC11U CABLE ASSEMBLY THROUGHOUT)



* DEPENDING ON THE TERMINAL USED FOR TEST, A NULL-MODEM SUCH AS THE H312 MAY BE NEEDED.



INTERPROCESSOR TEST 'ITEP' (DZQ11 OVERLAY IS DVDZD)

* BOTH PROCESSORS MUST BE RUNNING DZITA

RD1907

MINIMUM REQUIREMENTS FOR CVDZA, CVDZB AND CVDZC

Q-Bus CPU with 4K Memory

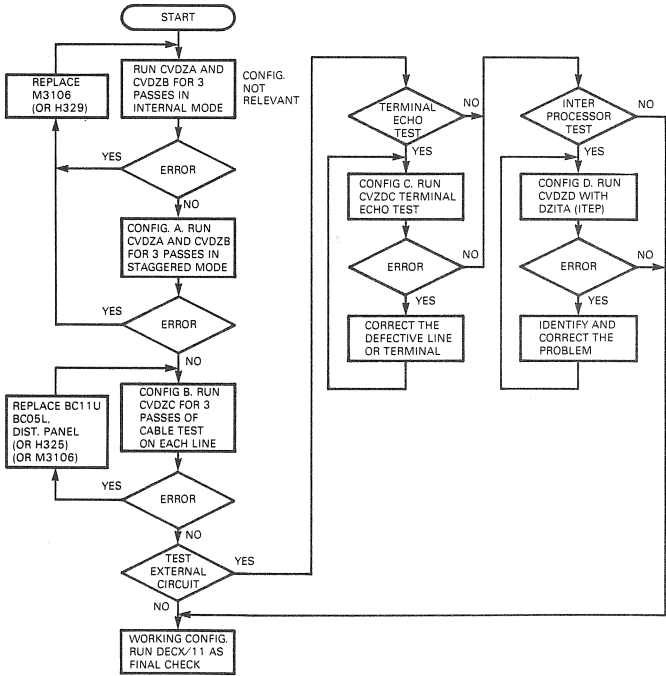
Console

DZQ11

H325 and H329 Test Connectors

Terminal, and possibly Null-Modem (CVDZC only)

TROUBLESHOOTING FLOWCHART FOR PDP-11 SYSTEMS



NOTE: FRUs ENCLOSED IN BRACKETS ARE UNLIKELY TO BE DEFECTIVE.

BASIC INSTALLATION PROCEDURE (MicroVAX SYSTEMS)

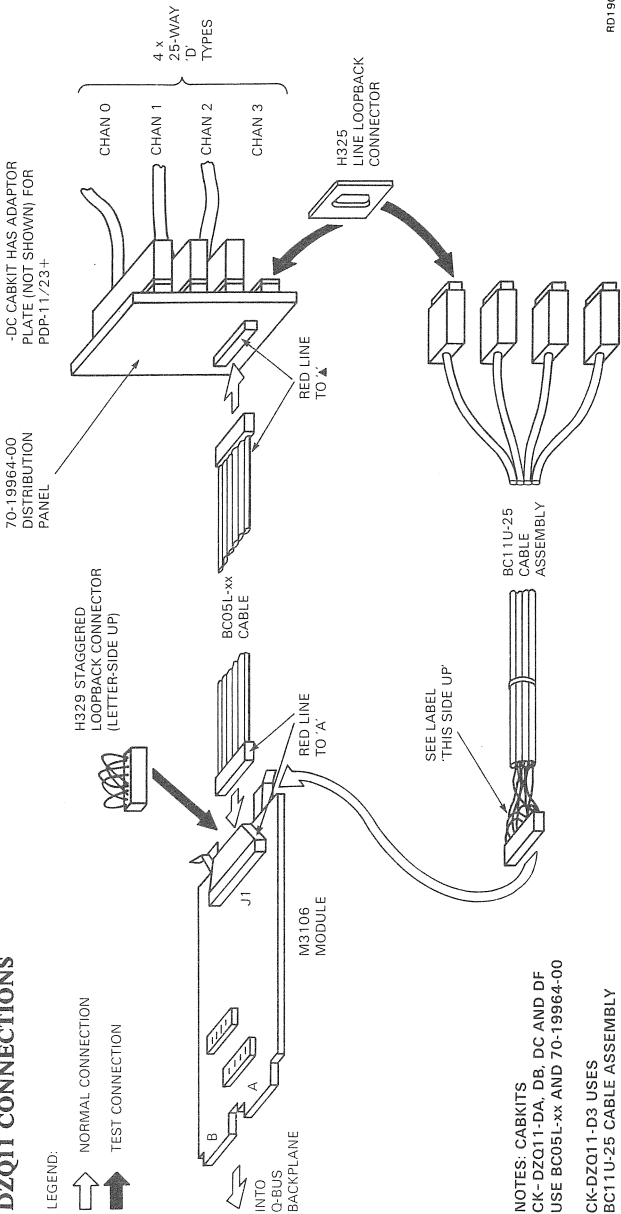
1. Unpack and check the components of the option.
2. Check and, if needed, set up device address, vector and break response switches. Make sure that jumpers W1 - W4 are installed or step 5 will fail.
3. Install an H329 loopback connector on J1.
4. Install the module in the correct backplane slot.
5. Run EHXDZ for 3 error-free passes of tests 1-21 (ST/SEC:ALL)
6. Configure W1 - W8 as appropriate for the customer.
7. Remove H329 and install BC05L cable and the 70-19964-00 panel. Make sure that jumpers W14 - W17 are installed or test will fail.
8. Run Macroverify without error as a final system check.
9. The DZQ11 should now be ready for connection to external equipment.

BASIC INSTALLATION PROCEDURE (PDP-11 SYSTEMS)

1. Unpack and check the components of the option.
2. Check and, if needed, set up device address, vector and break response switches. Make sure that jumpers W1 - W14 are installed or diagnostic tests will fail.
3. Install module in correct backplane slot.
4. Run 3 error-free passes of CVDZA and CVDZB in internal mode.
5. Install H329 and run 3 error-free passes of CVDZA and CVDZB in staggered mode.
6. Remove H329 and install BC11U-25 cable assembly or BC05L and 70-19964-00.
7. Install H325 on each line in turn. Run 3 error-free passes of CVDZC per line. Make sure that jumpers W14 - W17 are installed or test will fail.
8. Configure W1 - W8 as appropriate for the customer.
9. Run the DECX/11 system exerciser without error.
10. The DZQ11 should now be ready for connection to external equipment.

DZQ11 CONNECTIONS

LEGEND:



NOTES: CABKITS
 CK-DZQ11-DA, DB, DC AND DF
 USE BC05L-xx AND 70-19964-00

CK-DZQ11-D3 USES
 BC11U-25 CABLE ASSEMBLY

REGISTER CODES

REGISTER SET

DEVICE ADDRESS (BASE)	BYTES															LSB			
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	0	1	2
CONTROL & STATUS (CSR)	RO	RW	RO	RW	NOT USED	RO	RO	RO	RW	RW	RW	RW	RW	NOT USED	NOT USED	NOT USED			
	TRDY	TIE	SA	SAE	NOT USED	TLINE B	TLINE A	RDONE	RIE	MSE	CLR	MAINT							
RECEIVER BUFFER (RBUF)	RO	RO	RO	RO	NOT USED	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
	DATA VALID	OVN	FRAM ERR	PAR ERR	NOT USED	RX LINE B	RX LINE A	RBUF D7	RBUF D6	RBUF D5	RBUF D4	RBUF D3	RBUF D2	RBUF D1	RBUF D0		RBUF	RBUF	RBUF
LINE PARAMETER (LPR)	NOT USED	NOT USED	NOT USED	NOT USED	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
	SPEED CODE D	SPEED CODE C	SPEED CODE B	SPEED CODE A	WD ENAB	RX ENAB	STOP CODE	CHAR LGTH B	CHAR LGTH A								CHAR LGTH A	CHAR LGTH B	CHAR LGTH A
TRANSMIT CONTROL (TCR)	NOT USED	NOT USED	NOT USED	NOT USED	RW	RW	RW	RW	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	RW	RW	RW
	DTR 3	DTR 2	DTR 1	DTR 0													LINE ENAB	LINE ENAB	LINE ENAB
MODEM STATUS (MSR)	NOT USED	NOT USED	NOT USED	NOT USED	RO	RO	RO	RO	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	RO	RO	RO
	CO 3	CO 2	CO 1	CO 0													RI 3	RI 2	RI 1
TRANSMIT DATA (TDR)	NOT USED	NOT USED	NOT USED	NOT USED	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
	BRK 3	BRK 2	BRK 1	BRK 0													TBUF	TBUF	TBUF

LPR<11:08>	BAUD RATE	LPR<11:08>	BAUD RATE
0000	50	1000	1800
0001	75	1001	2000
0010	110	1010	2400
0011	134.5	1011	3600
0100	150	1100	4800
0101	300	1101	7200
0110	600	1110	9600
0111	1200	1111	19800

LPR<05:03>	CHAR LENGTH	STOP LENGTH
000	5 bits	1 bit
100	5 bits	1.5 bits
001	6 bits	1 bit
101	6 bits	2 bits
010	7 bits	1 bit
110	7 bits	2 bits
011	8 bits	1 bit
111	8 bits	2 bits