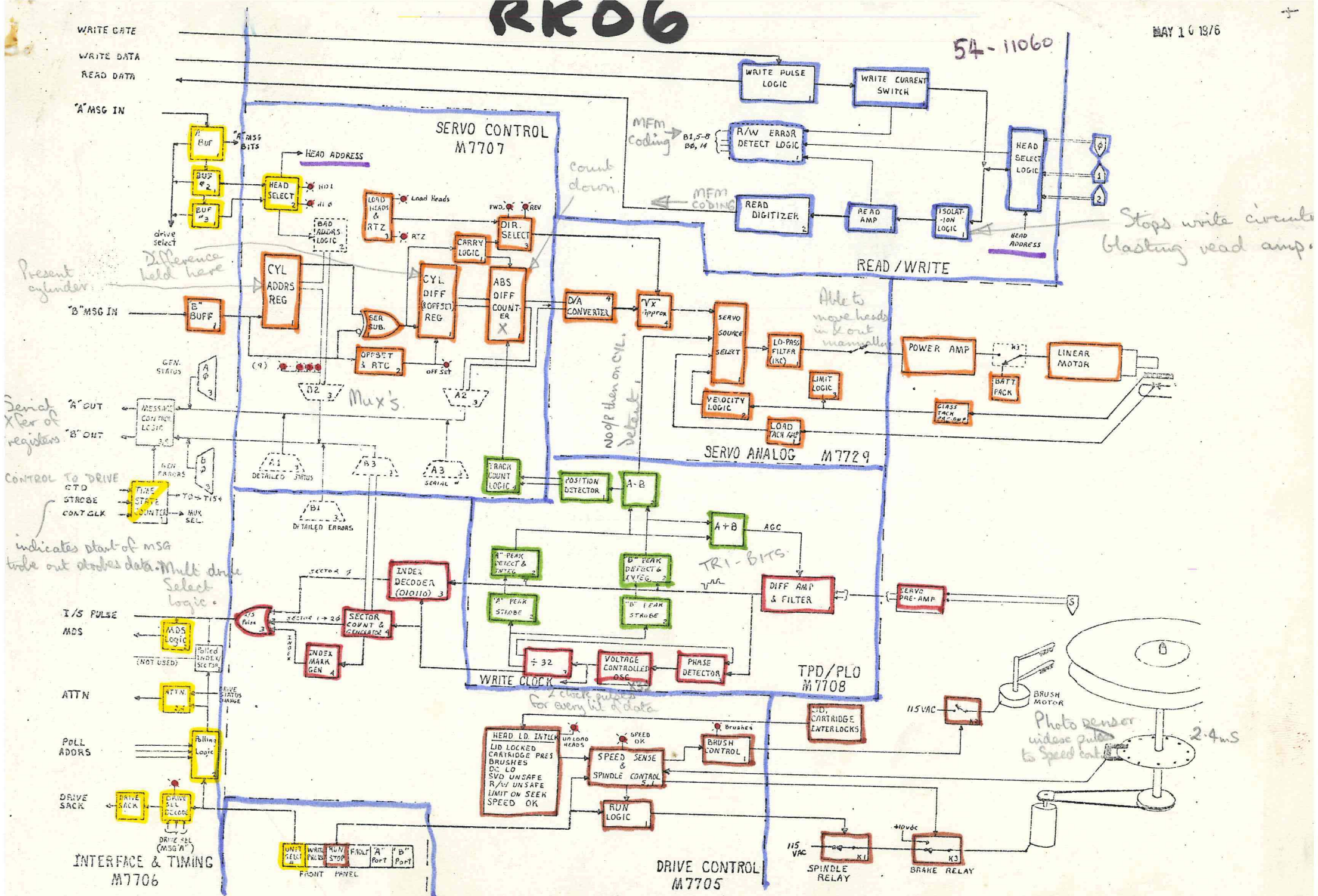


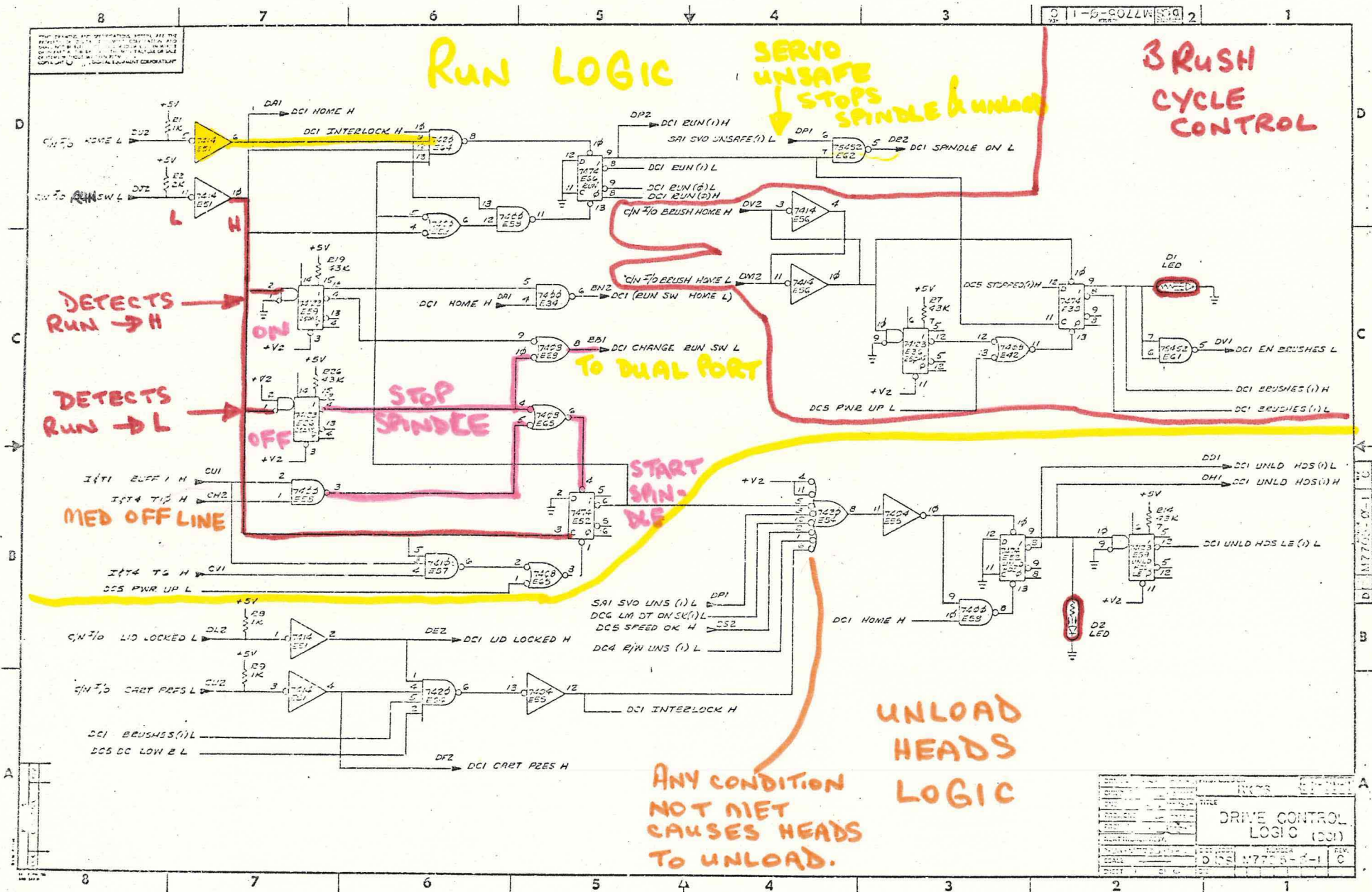
# RK06

MAY 10 1976

54-11060

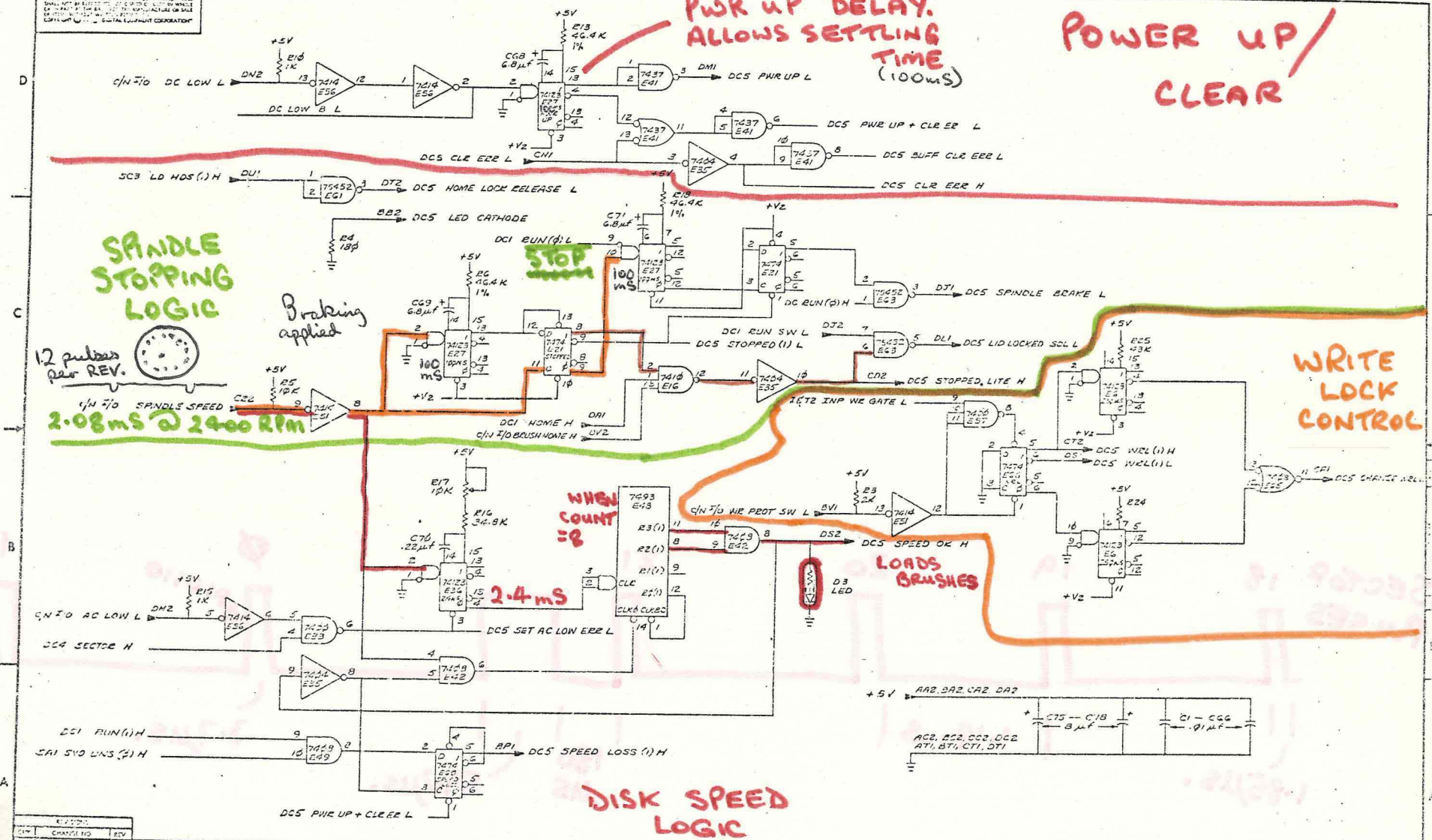






REVISIONS		DATE	BY	CHKD
1	INITIAL			
TITLE				
DRIVE CONTROL LOGIC (DCI)				
NO. OF SHEETS	SHEET NO.	REV.		
1	1	1		
DESIGNER	DRAWN	APP'D		

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**PWR UP DELAY. ALLOWS SETTLING TIME (100ms)**

**POWER UP / CLEAR**

**SPINDLE STOPPING LOGIC**



**Braking applied**

**STOP**

**WHEN COUNT = 8**

**2.4ms**

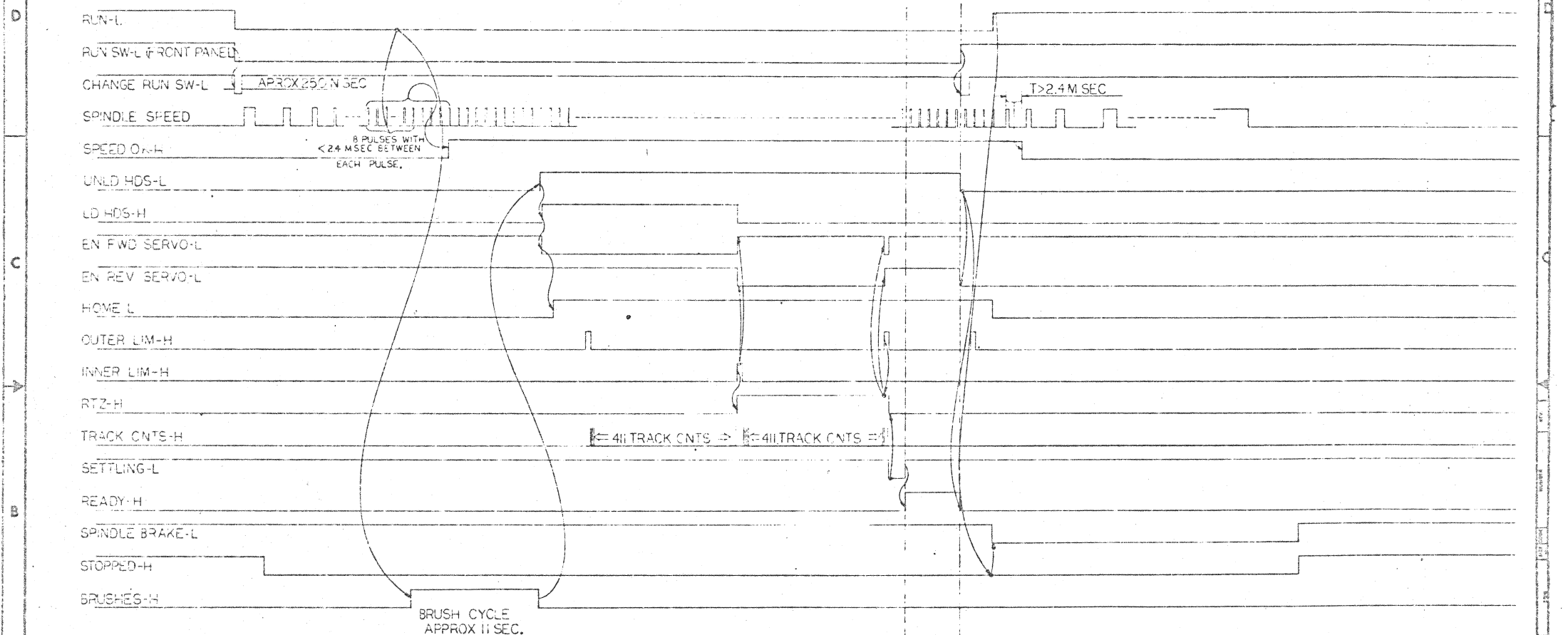
**LOADS GRASHES**

**WRITE LOCK CONTROL**

**DISK SPEED LOGIC**

REV	DATE	BY	CHKD	APP'D	TITLE	SCALE	SHEET	OF	NO.	REV.
1					DRIVE CONTROL LOGIC		5	5	DCSIM7705-0-1	C

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DRIVE START UP TIMING

DRIVE IS IN READY MODE, I.E. IT MAY SEEK, READ/WRITE, ETC.

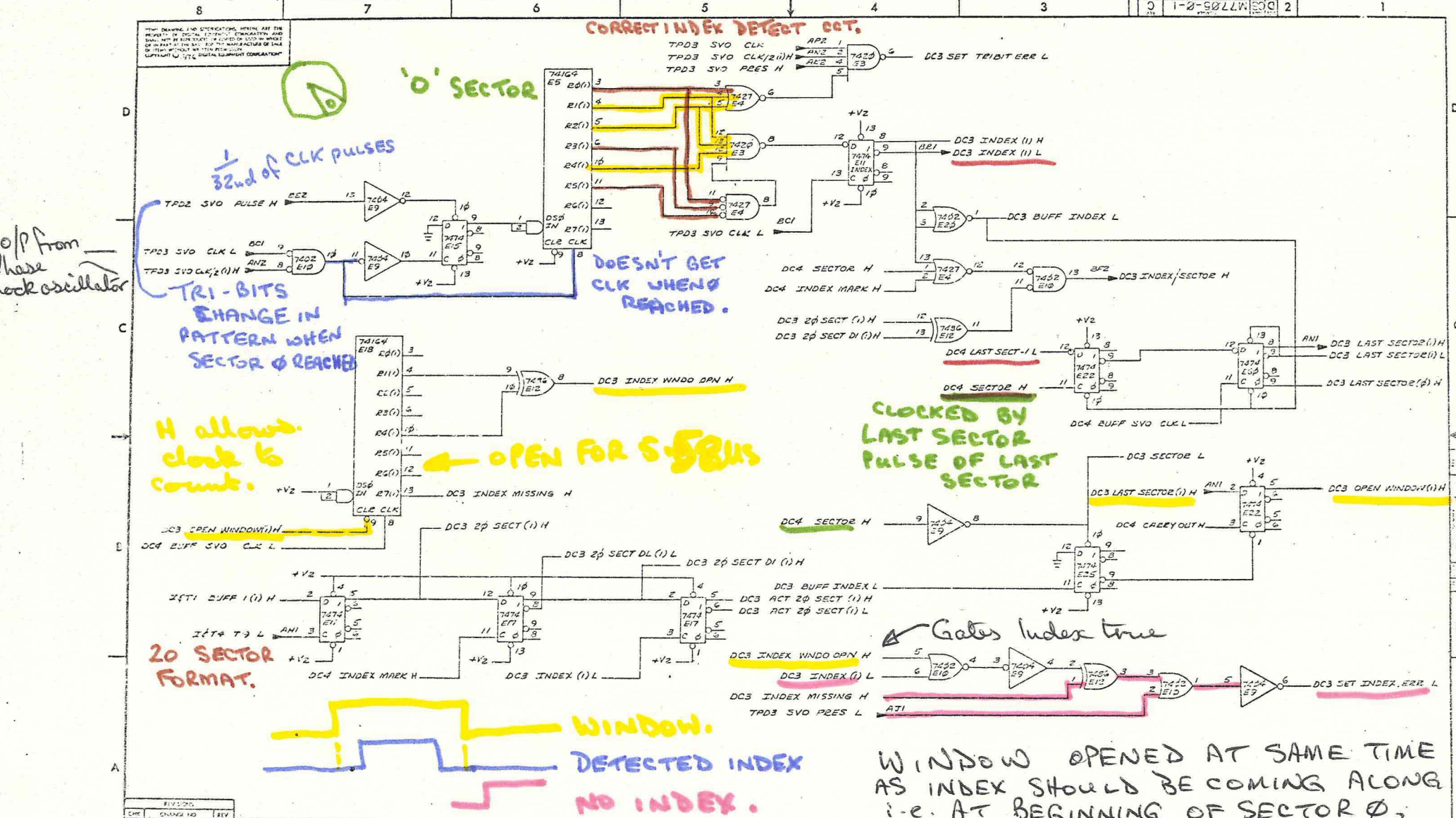
DRIVE CYCLE DOWN TIMING

DATE: 11/11/71  
 DRAWN BY: [Signature]  
 CHECKED BY: [Signature]  
 DESIGNED BY: [Signature]

DRW		FIRST USED ON	
CHK'D		TITLE	START UP AND CYCLE DOWN TIMING
ENG		SCALE	D
PROJ. ENG.		SHEET	2
PRCD		OF	1
NEXT HIGHER ASSY.		SIZE	CODE
		NUMBER	
		REV	

Hence Index produced on 010110

**CORRECT INDEX DETECT Ckt.**



o/p from these clock oscillator

1/32nd of CLK PULSES

TRI-BITS CHANGE IN PATTERN WHEN SECTOR 0 REACHED

H allows clock to count.

DOESN'T GET CLK WHEN 0 REACHED.

OPEN FOR 5-5 BUS

CLOCKED BY LAST SECTOR PULSE OF LAST SECTOR

20 SECTOR FORMAT.

WINDOW.

DETECTED INDEX

NO INDEX.

Gates Index true

WINDOW OPENED AT SAME TIME AS INDEX SHOULD BE COMING ALONG i.e. AT BEGINNING OF SECTOR 0.

REV	CHANGED BY	REV

NR CONDITIONS BUT NOT WRITING WRONG HD SELECT NO INTER PATTERN AT WRITE TIME 3 successive trunks missing LOST SERVO BITS WRITING AT WRONG TIME

ERROR CONDITIONS

B0 #14

B0 #11 Register condition PRODUCED IF WRITE LOCKED

SECTOR COUNT

COUNT FOR 22 SECT = 16 FOR 20 SECT = 15.7145

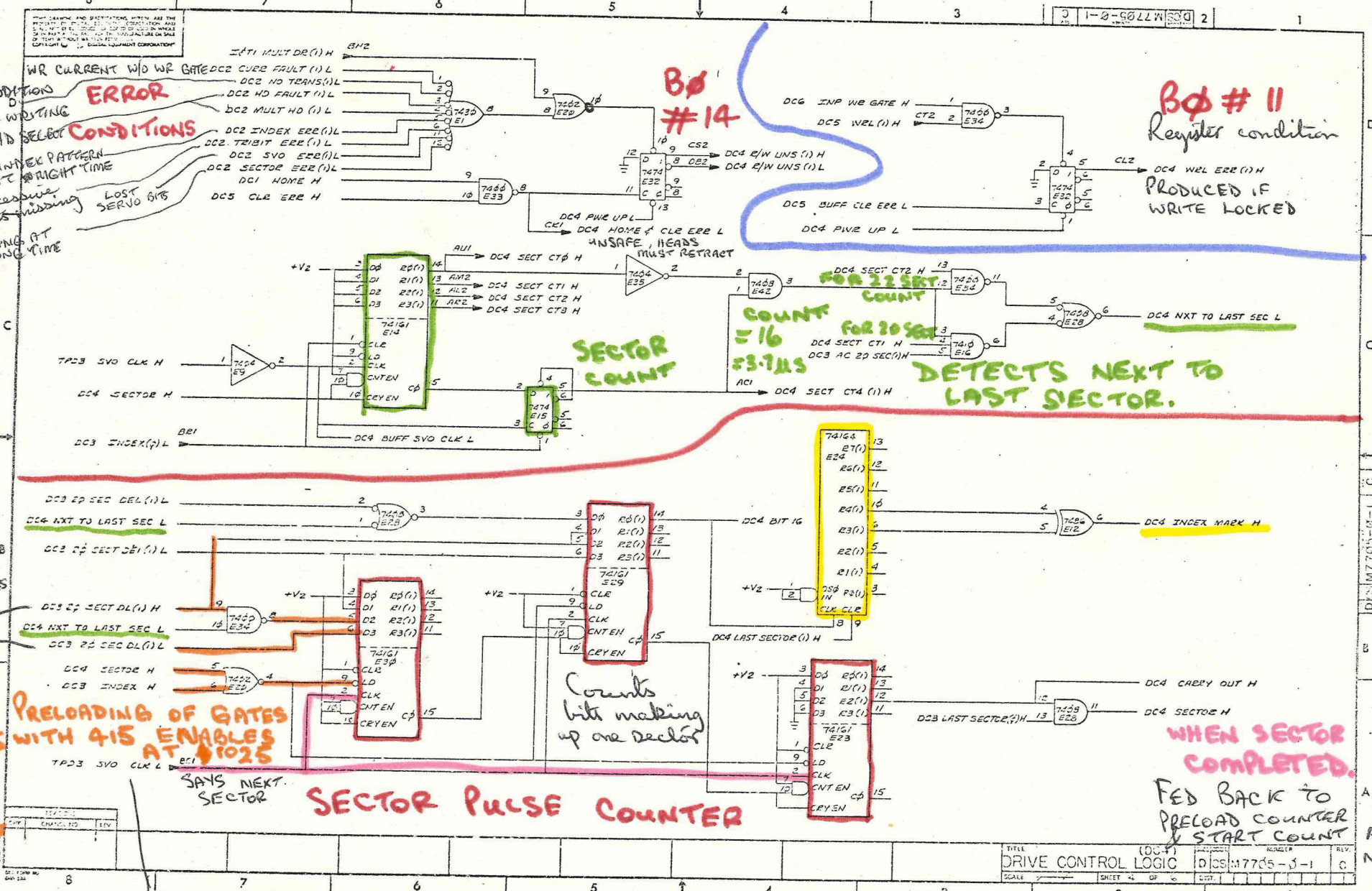
DETECTS NEXT TO LAST SECTOR.

SECTOR PULSE COUNTER

DETERMINES 20 or 22 sector 257 PRELOADING OF GATES WITH 415 ENABLES AT 1025 gives waveform @ 929 for 20 SECT. Preload different for last sector timing

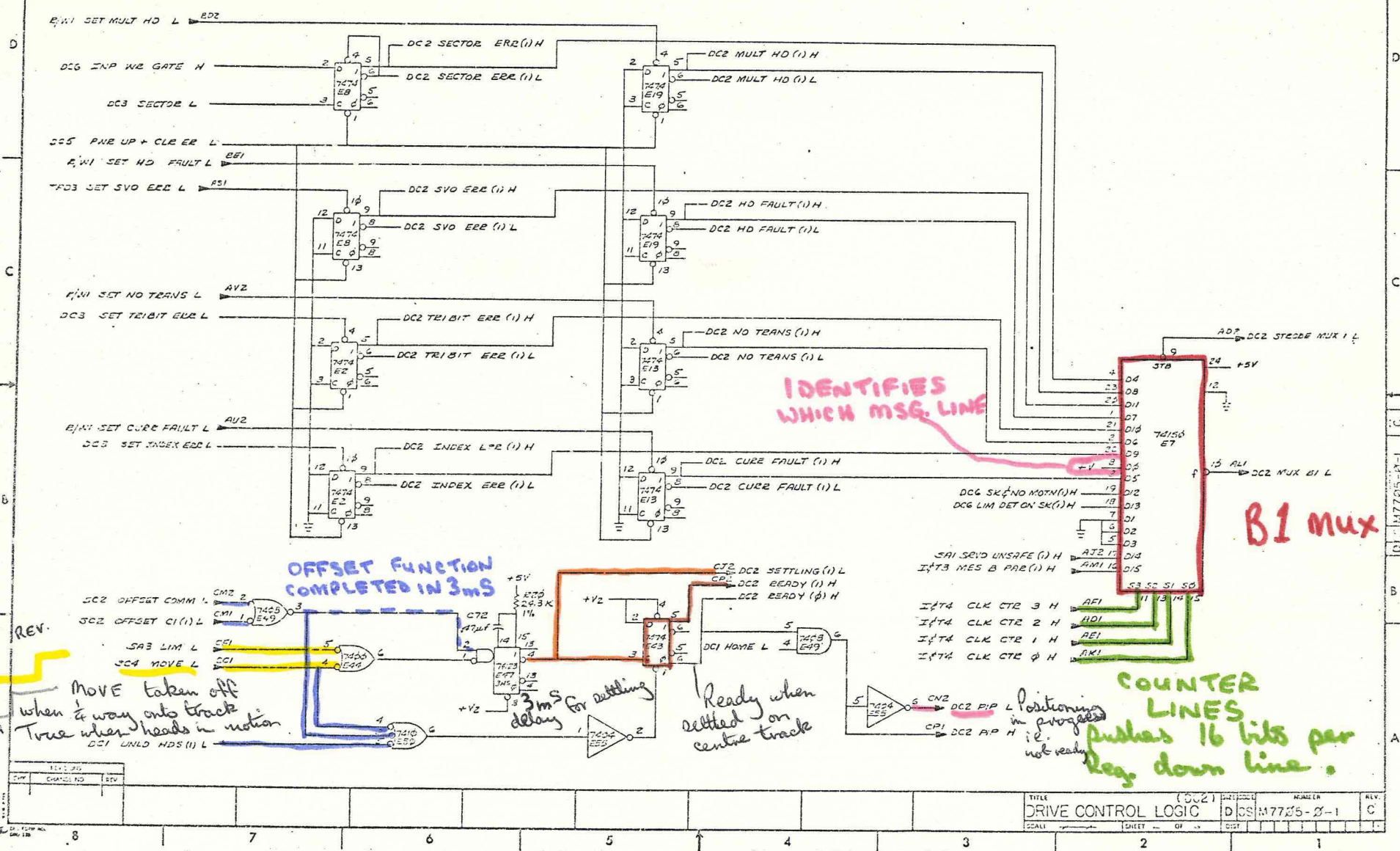
~~Preload for even trunks (odd trunks not preloaded)?~~

WHEN SECTOR COMPLETED. FED BACK TO PRELOAD COUNTER & START COUNT AGAIN FOR NEXT SECTOR





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IDENTIFIES WHICH MSG. LINE

B1 mux

OFFSET FUNCTION COMPLETED IN 3ms

COUNTER LINES pushes 16 bits per Reg. down line.

visible spikes when limit reached unit qual used eliminate this.

MOVE taken off when it way onto track True when heads in motion

3ms delay for settling

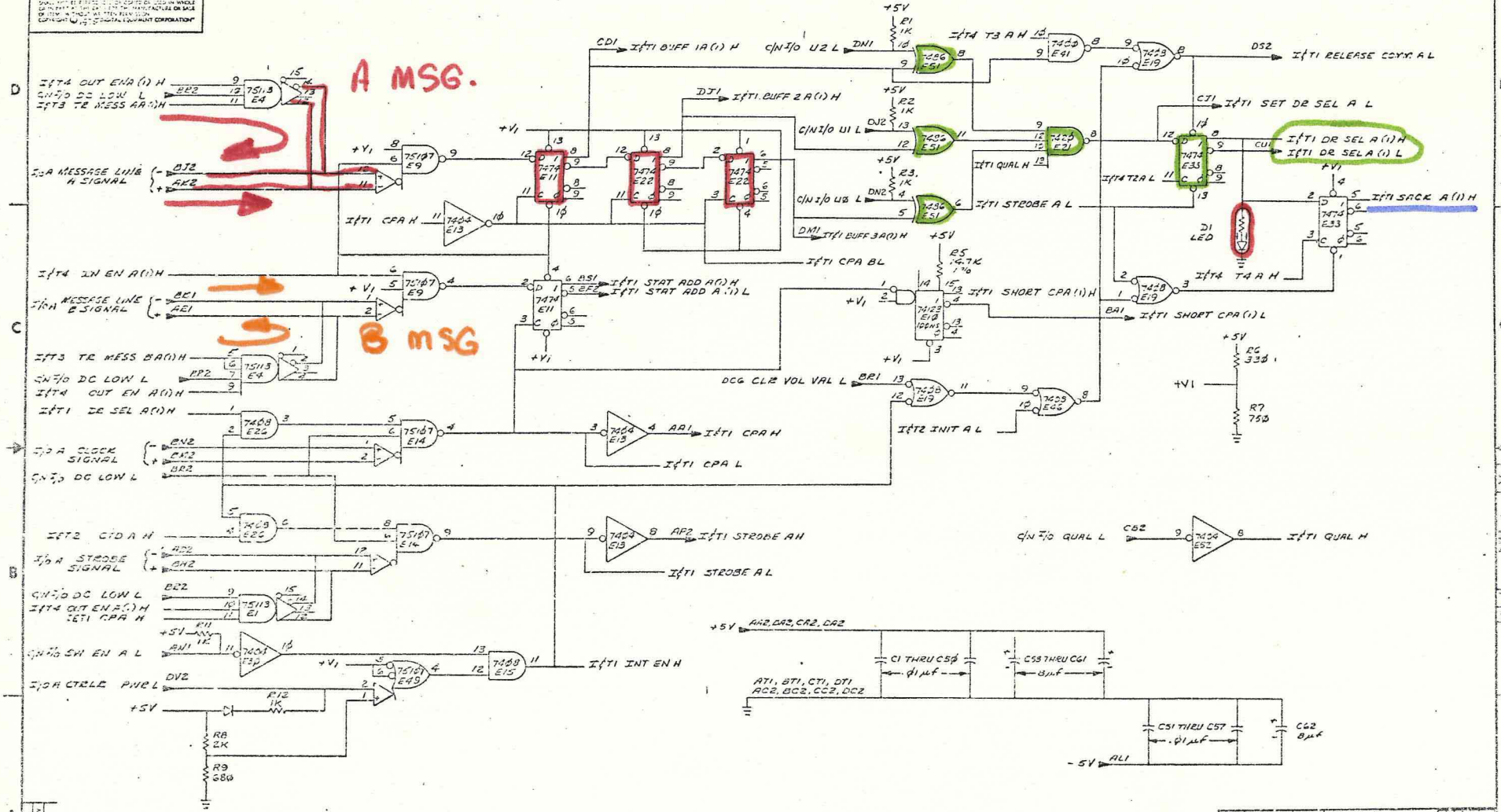
Ready when settled on centre track

Positioning in progress i.e. not ready

TITLE	(5021) DRIVE CONTROL LOGIC	NUMBER	DCS M7725-2-1	REV.	C
SCALE		SHEET	OF		



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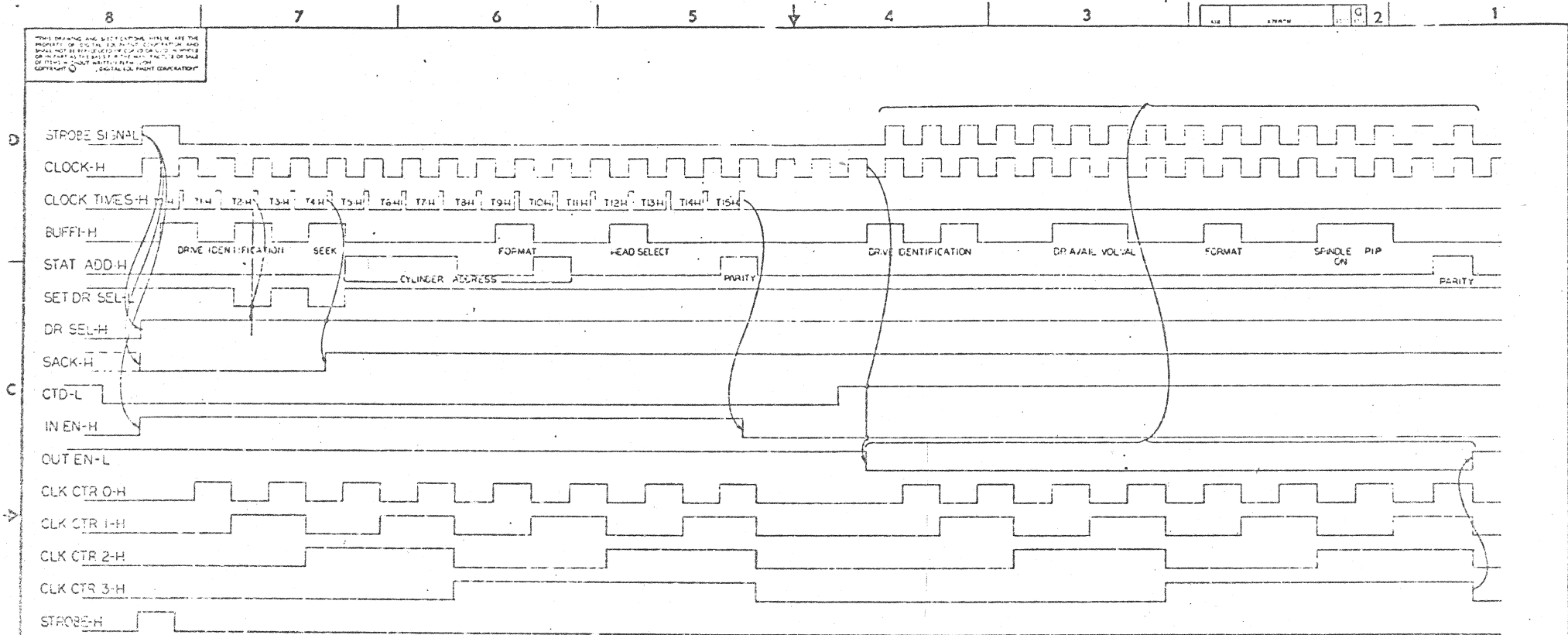
A MSG.

B MSG.

ORIGINATOR	DATE	BY	CHKD BY	DATE	REV
ENGINEER					
DESIGNER					
PROD. CONTROL					
REACT. HIGH. ASSY.					
<b>INTERFACE</b> <b>TIMING (IFTI)</b>					
SCALE	SIZE	CODE	NUMBER	REV.	
	CS	M7708-3-1	1	1	
SHEET 1	OF 4	551			



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**SYSTEM CONDITIONS.**

1. FRONT PANEL PORT ENABLE SWITCH IS DEPRESSED
2. DC VOLTAGES IN DRIVE ARE OK.
3. VOLTAGES IN CONTROLLER ARE OK.

**NOTE. DURING THE CONTROLLER TO DRIVE TRANSMISSION**

1. DRIVE NUMBER 5 IS SELECTED
2. A SEEK COMMAND TO CYLINDER 70 IS ISSUED.
3. FORMAT IS SET TO 20 SECTORS.
4. HEAD NUMBER 1 HAS BEEN SELECTED

**DURING THE DRIVE TO CONTROLLER TRANSMISSION**

1. THE DRIVE IDENTIFIES ITSELF
2. TELLS CONTROLLER:
  - DRIVE IS AVAILABLE | FORMAT IS SET TO 20 SECTORS
  - VOLUME VALID IS SET | SPINDLE IS ON.
  - THERE IS A SEEK IN PROGRESS

DATE	REV	BY	CHK	APP	DESIGNED BY	DATE
CHK'D					TITLE	
ENG'D					INTERFACING TIMING	
PROJ. ENG.					BOARD TIMING DIAGRAM	
FRG'D						
NEXT HIGHER ASSY.						
SCALE	D	SIZE	CODE	NUMBER	REV.	
SHEET	2	2	ST			

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**DRIVE STATUS CHANGE Aφ#14**

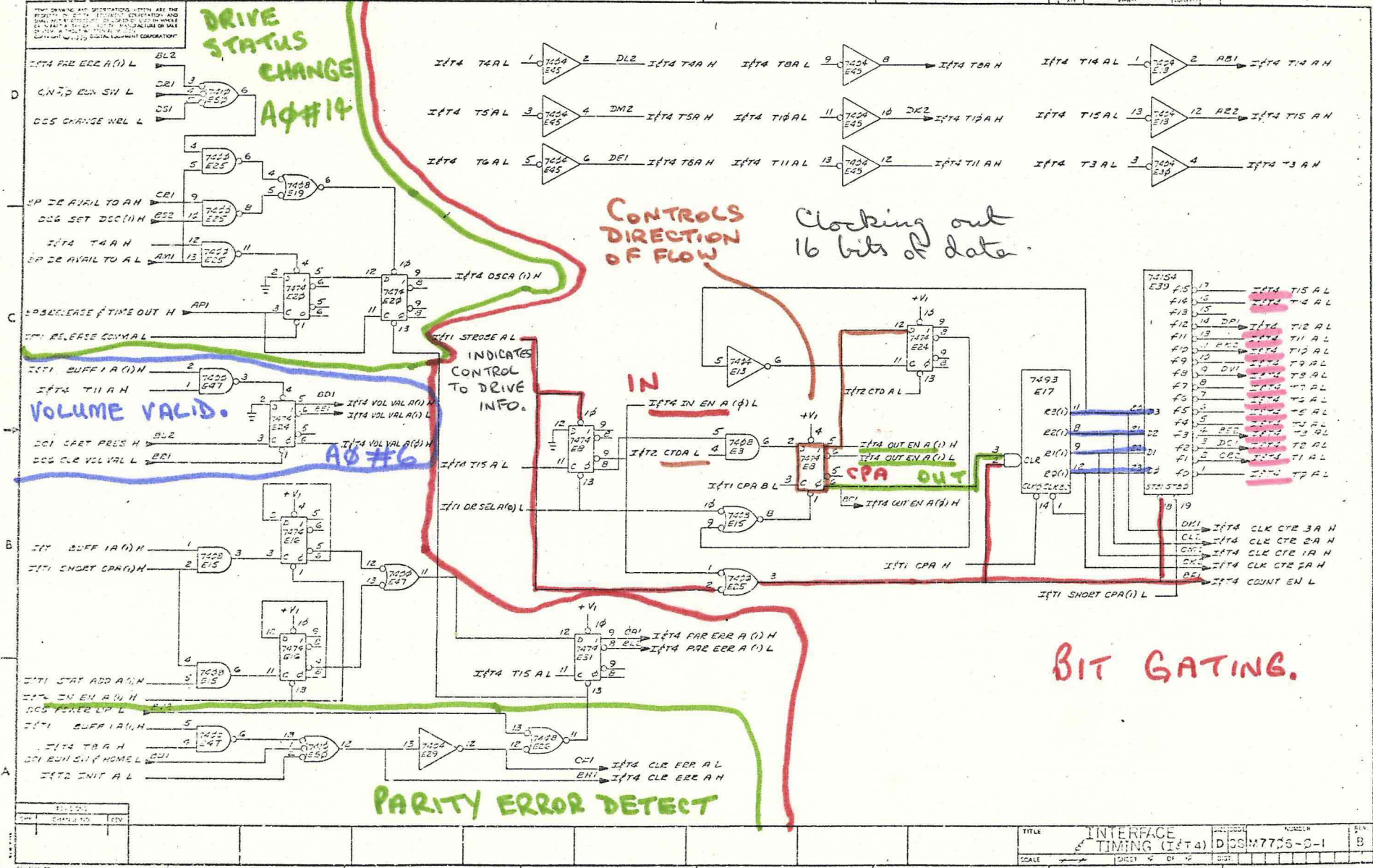
**CONTROLS DIRECTION OF FLOW**

Clocking out 16 bits of data.

**TIMING REFERENCE FOR BITS TO BE CLOCKED IN.**

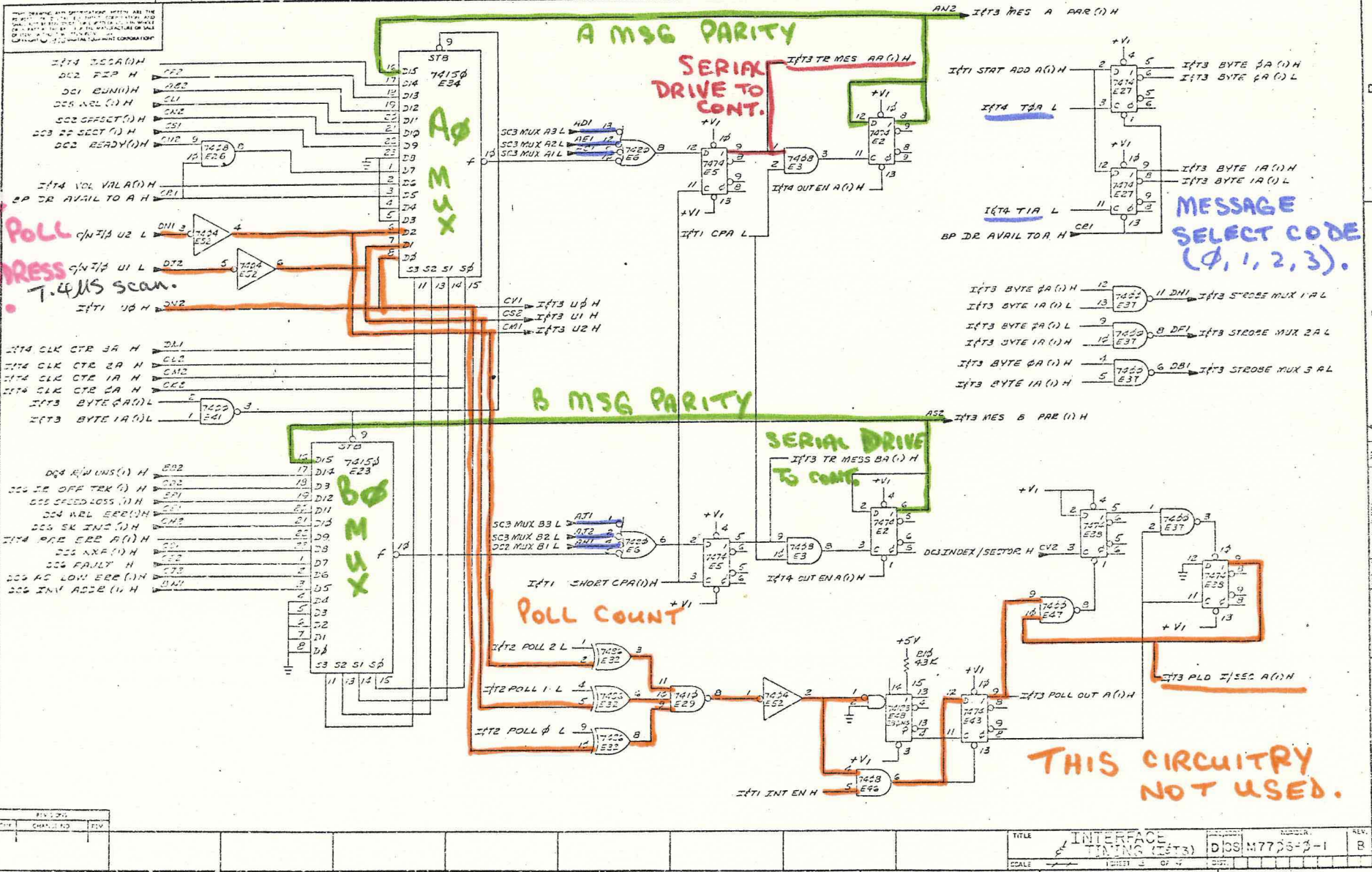
**BIT GATING.**

**PARITY ERROR DETECT**



TITLE	INTERFACE TIMING (IFT4)	NUMBER	DDCS M7705-0-1
SCALE		SHEET	2 OF 2

+



CONTROL/POLL REGISTER ADDRESS SELECTION  
7.4μS SCAN

A MSG PARITY

SERIAL DRIVE TO CONT.

Ag  
M  
X

B MSG PARITY

SERIAL DRIVE TO CONT.

Bg  
M  
X

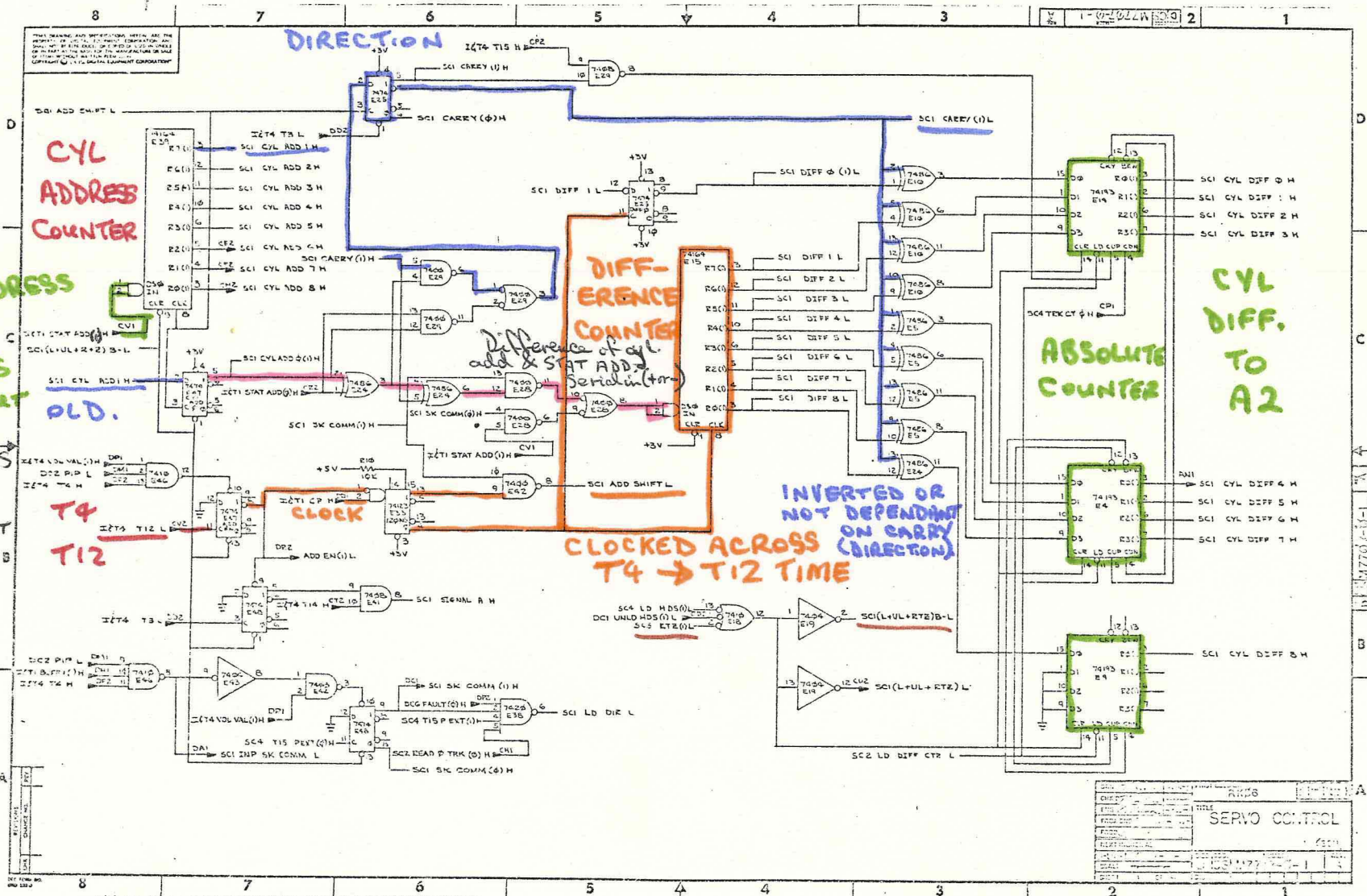
POLL COUNT

MESSAGE SELECT CODE (0, 1, 2, 3)

THIS CIRCUITRY NOT USED.

TITLE	INTERFACE TIMING (I/T3)	REVISION	1
SCALE	1 SHEET OF 4	DIST.	
D:\CS\M7735-3-1		REV.	B

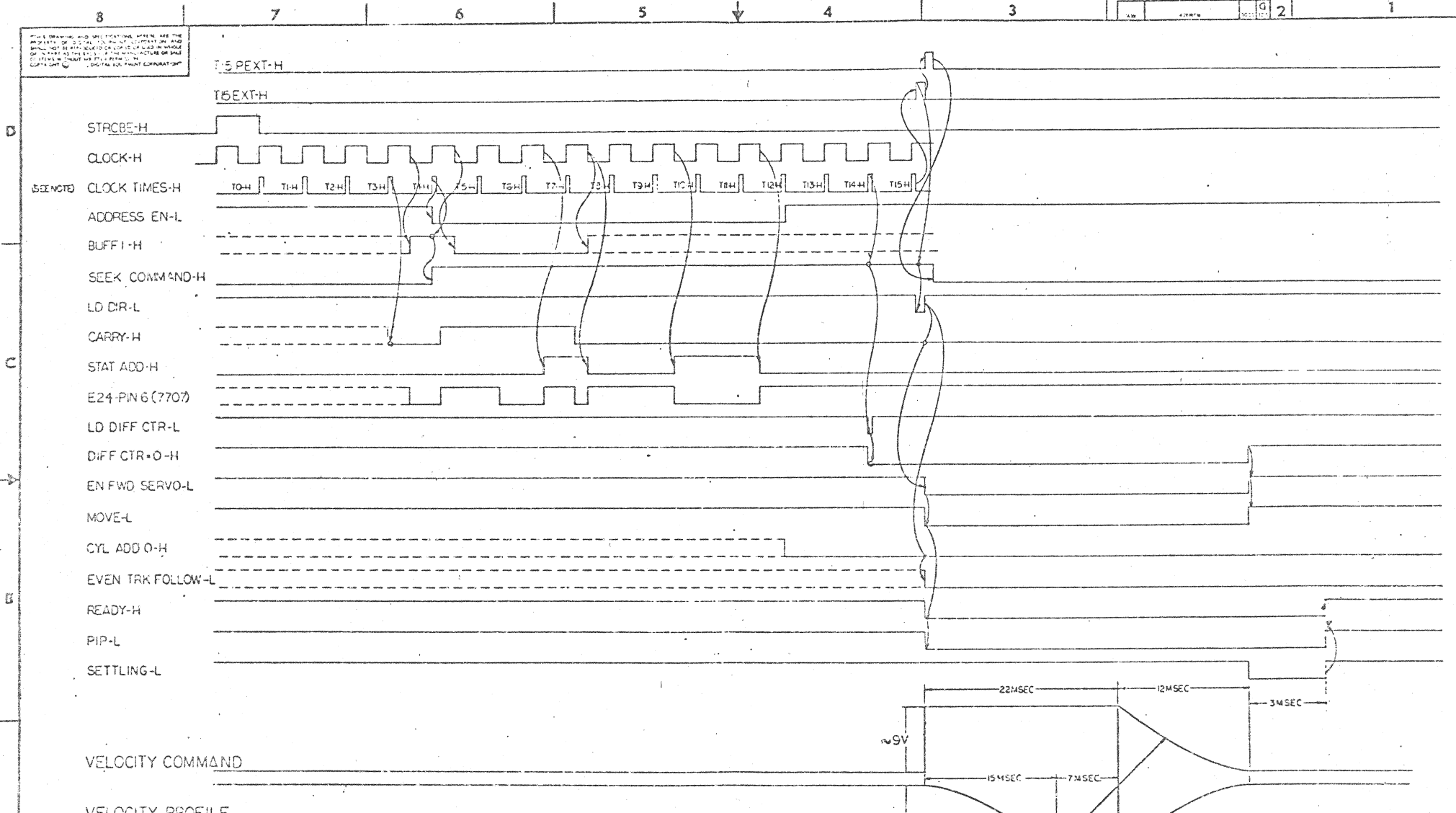




REV	1	DATE	11-17-77
DESIGNED BY	RKS		
ENGINEER	RKS		
PROJECT	SERVO CONTROL		
DESCRIPTION	SERVO CONTROL		
DATE	11-17-77		
BY	RKS		
CHECKED BY	RKS		
DATE	11-17-77		



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VELOCITY PROFILE

**SYSTEM CONDITIONS.**

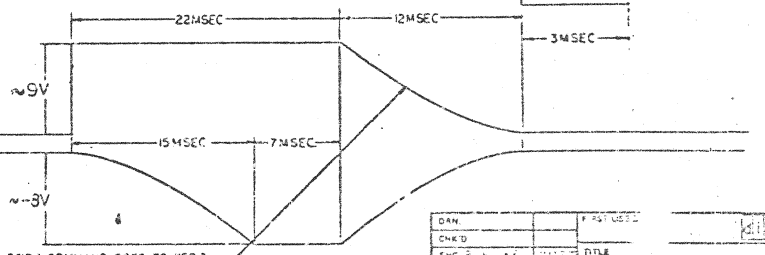
1. VOLUME VALID IS SET.
2. THERE ARE NO FAULTS.
3. THE DRIVE ISNT ALREADY DOING A SEEK.

**NOTE.**

ALTHOUGH THE CLOCK TIMES ARE AVAILABLE AS SEPARATE PULSES, THERE SHOWN AS A STRING OF PULSES TO CONSERVE SPACE.

THE ABOVE DIAGRAM IS FOR A 5 TO 200 CYLINDER SEEK.

VELOCITY COMMAND GOES TO ZERO AS THE POSITION APPROACHES ITS DESTINATION.



DRAWN	DATE	REVISED	BY
CHECKED	DATE	REVISED	BY
ENG. P. A. J.	DATE	REVISED	BY
PROJ. ENGR. P. A. J.	DATE	REVISED	BY
PROD.	DATE	REVISED	BY
NEXT HIGH PRIORITY	DATE	REVISED	BY
SCALE	DATE	REVISED	BY
SHEET	OF	TOTAL	REV

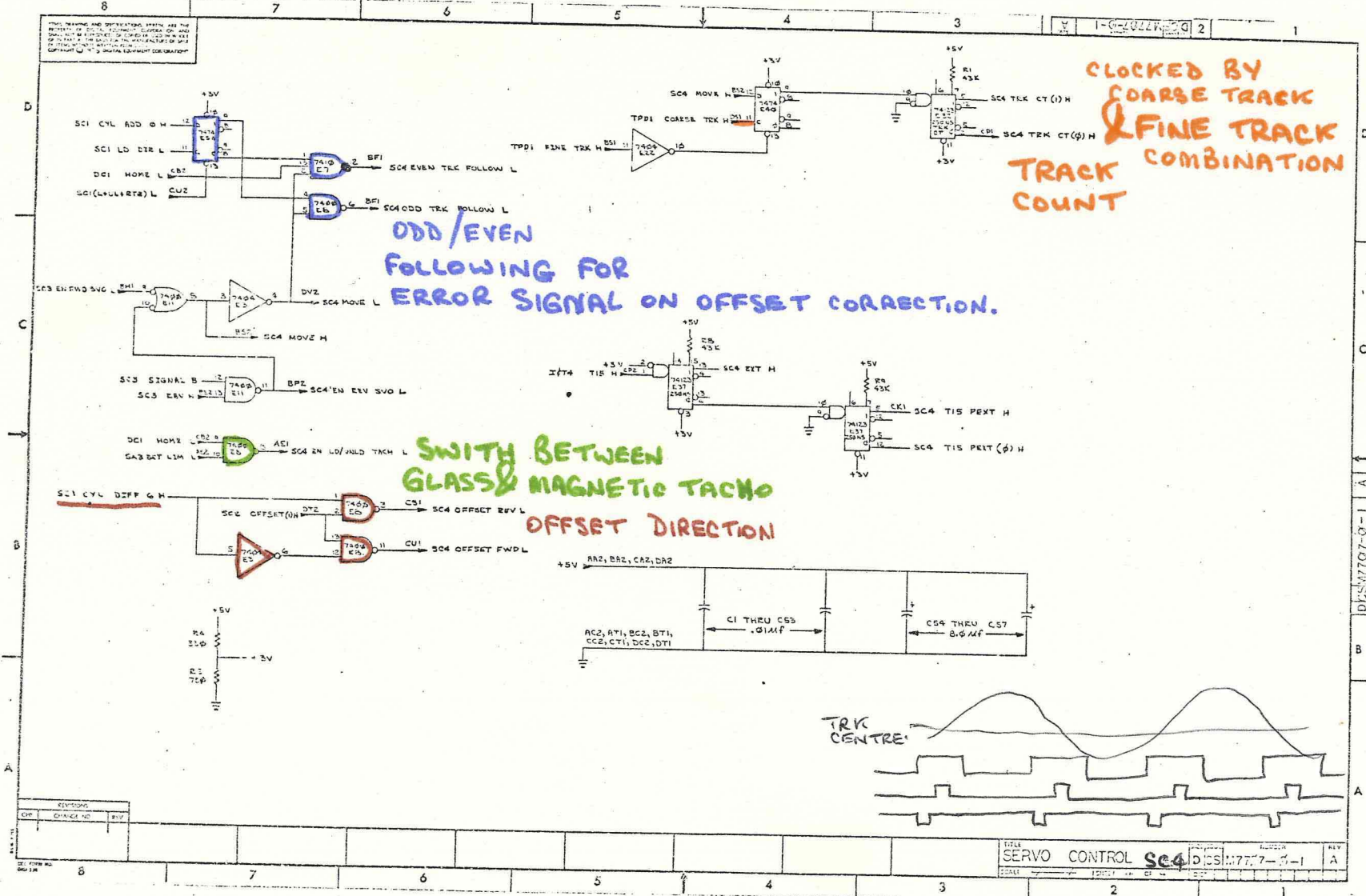
SEEK OPERATION TIMING DIAGRAM

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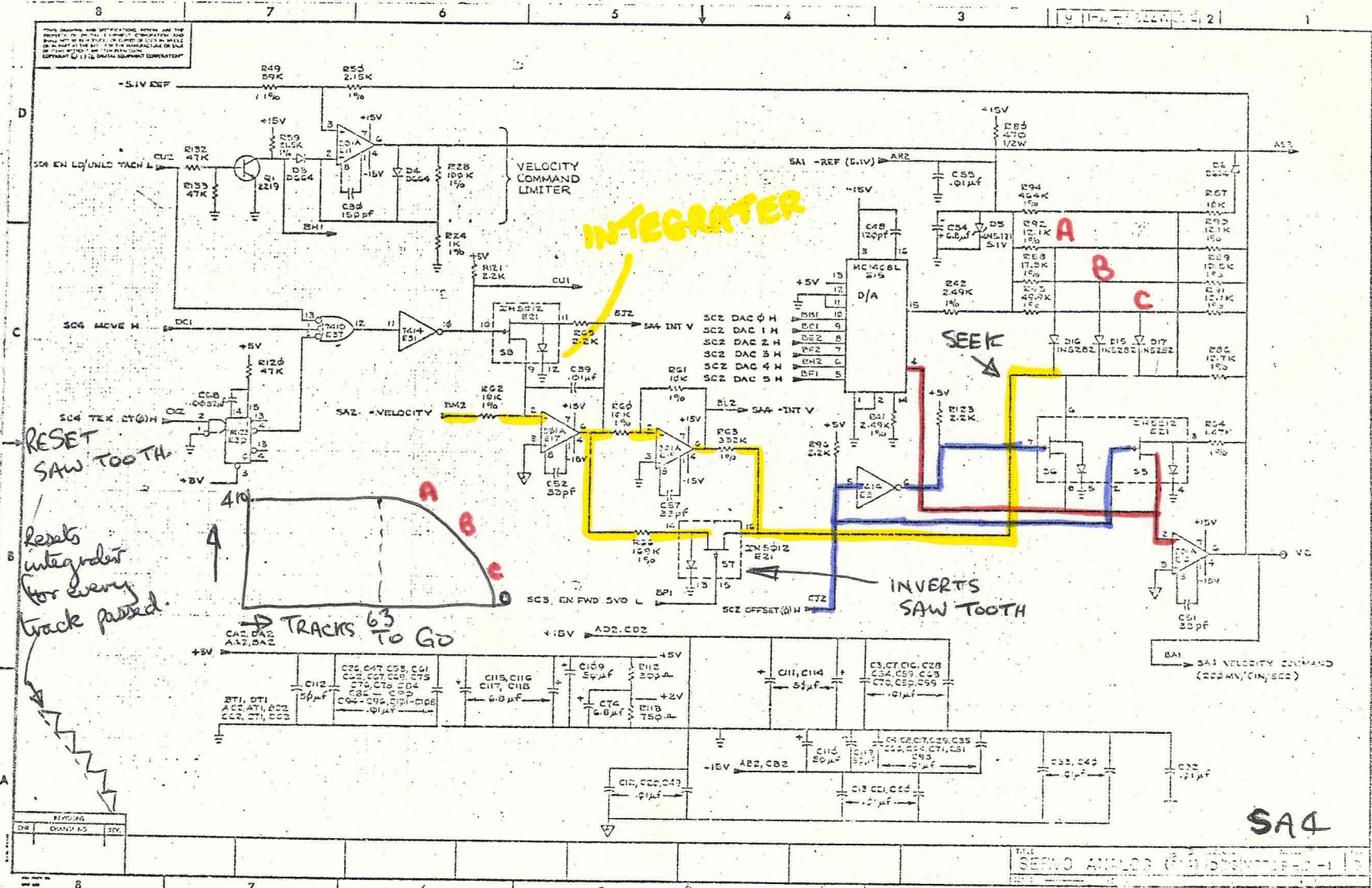
CLOCKED BY  
COARSE TRACK  
& FINE TRACK  
COMBINATION  
TRACK  
COUNT

ODD/EVEN  
FOLLOWING FOR  
ERROR SIGNAL ON OFFSET CORRECTION.

SWITCH BETWEEN  
GLASS & MAGNETIC TACHO  
OFFSET DIRECTION



TITLE SERVO CONTROL SC4 DIS: M77-7-1-1 REV A



SAW TOOTH  
GENERATED  
FROM OPTICAL  
TACHO & USED  
TO COMPENSATE  
FOR 'STEPPING'  
VELOCITY WAVEFORM  
TO GIVE US A SMOOTH  
RAMP.

RESET  
SAW TOOTH.

RESETS  
integrator  
for every  
track passed.

TRACKS TO GO

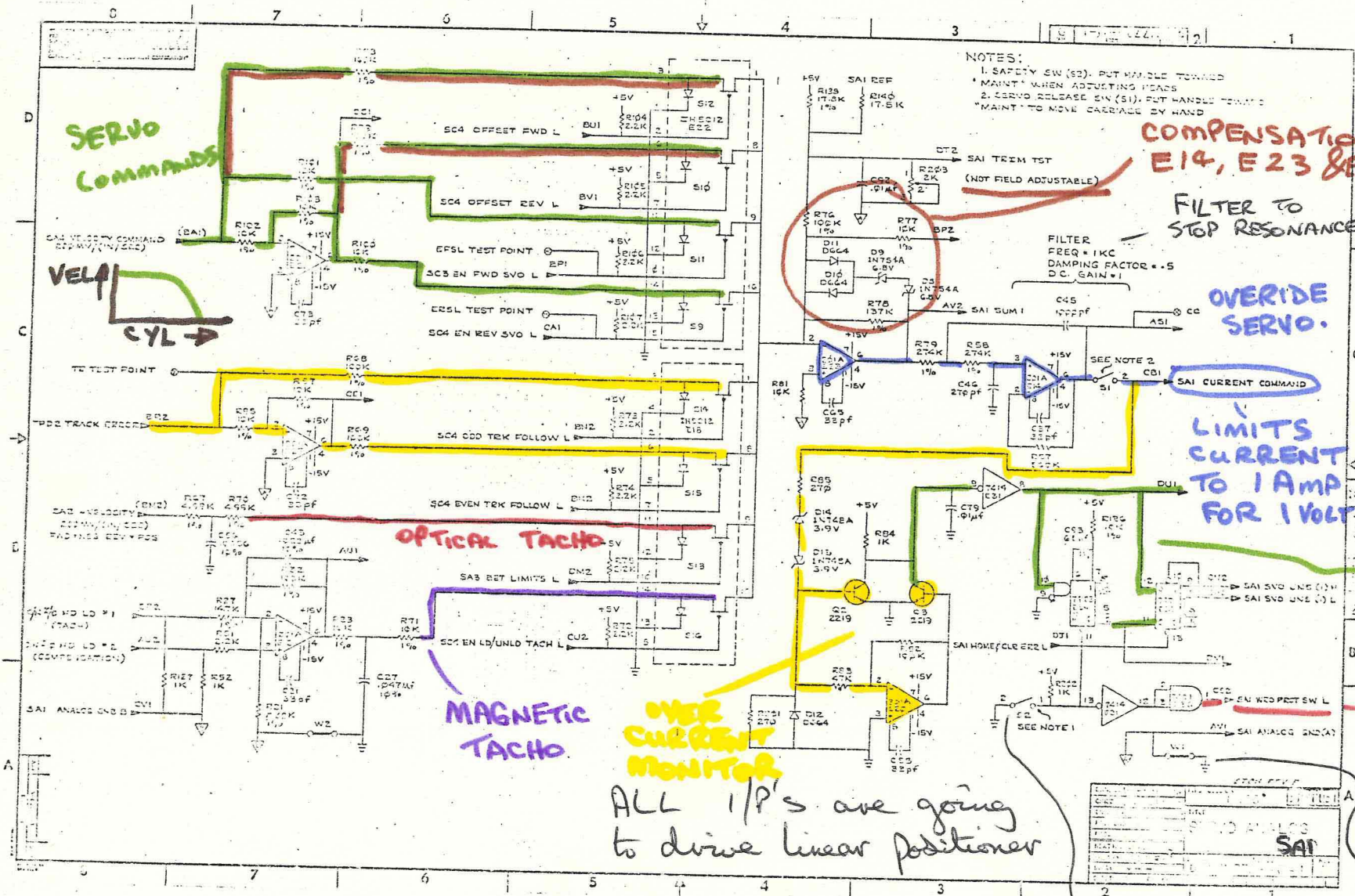
INTEGRATOR

SEEK

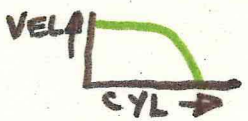
INVERTS  
SAW TOOTH

SAA

SEEVO AMPLO (S) BENTLEY-1 15



SERVO COMMANDS



OPTICAL TACHO

MAGNETIC TACHO

OVER CURRENT MONITOR

ALL I/P's are going to drive linear positioner

NOTES:  
 1. SAFETY SW (S2). PUT HANDLE TOWARD "MAINT" WHEN ADJUSTING HEADS  
 2. SERVO RELEASE SW (S1). PUT HANDLE TOWARD "MAINT" TO MOVE CARTRIDGE BY HAND

COMPENSATION FOR E14, E23 & E24 OP. AMPS. SUPPLIES STABLE REF. VOLTAGE IF FAULTY MAY TRIP OVER CURRENT MONITOR & STOP ANY DETENTING.

FILTER TO STOP RESONANCE

VERRIDE SERVO.

LIMITS CURRENT TO 1 AMP FOR 1 VOLT

VERRIDE, SERVO UNSAFE

AUTOMATICALLY SETS WRITE PROT. WHEN OVERRIDING SERVO UNSAFE

VERRIDES SERVO UNSAFE CONDITION.

GND RETURN. WON'T WORK W/O JUMPER, MODULE THOUGHT TO BE MISSING

100 TRACK / INCH.



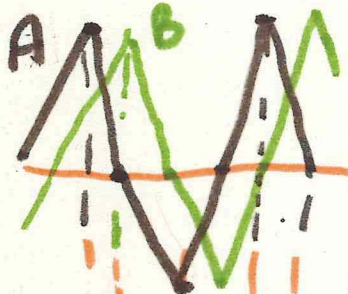
GRATICULE.

7

LEDS



TRANSDUCER BLOCK

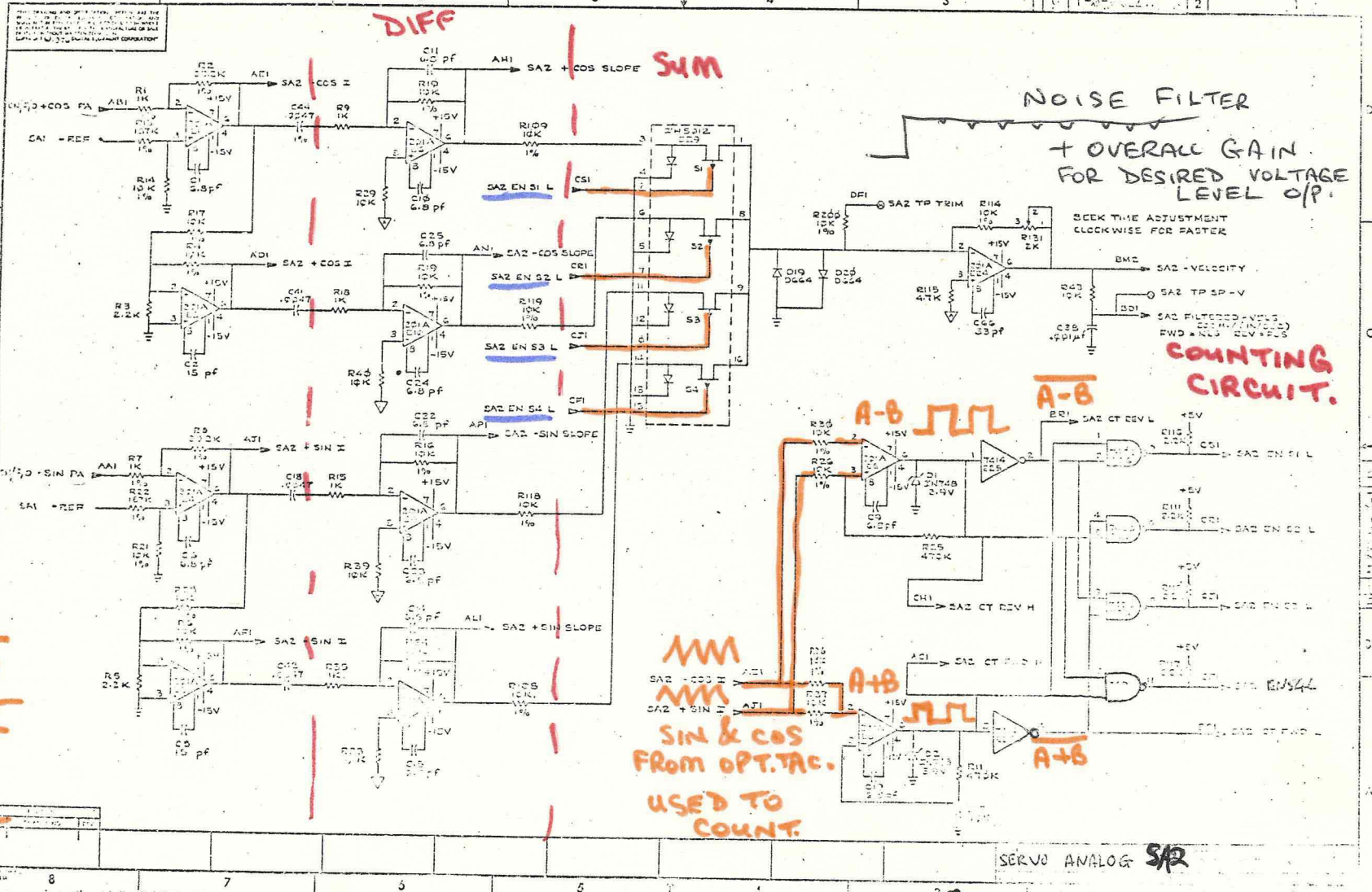


+B

-B

+B

-B



DIFF

SUM

NOISE FILTER

+ OVERALL GAIN FOR DESIRED VOLTAGE LEVEL C/P.

SEEK TIME ADJUSTMENT CLOCKWISE FOR FASTER

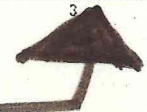
COUNTING CIRCUIT.

A-B

A-B

SAZ - COS I  
SAZ + SIN I  
SIN & COS FROM OPT. TAC.  
USED TO COUNT.

SERVO ANALOG SAZ



LIMIT PULSE  
 CLOCKS COS WAVEFORM.  
 PHASE DETECTS INNER  
 OR OUTER LIMIT

LOOKING AT  
 LIMIT PULSES  
 FROM OPT. TAC.

INNER & OUTER  
 LIMITS.



GREATER VOLTAGE  
 OUT IF X OVER  
 ABOVE 5.1V.

1.3V (NOM)  
 2.5V (MAX) } AGC Feedback  
 WITH MAX  
 COUNT.

FWD & REV  
 CONTROLLING  
 WHICH WAY  
 WE ARE GOING  
 AS WE WILL  
 BE OUT OF PHASE  
 NO

18V  
 P-P.



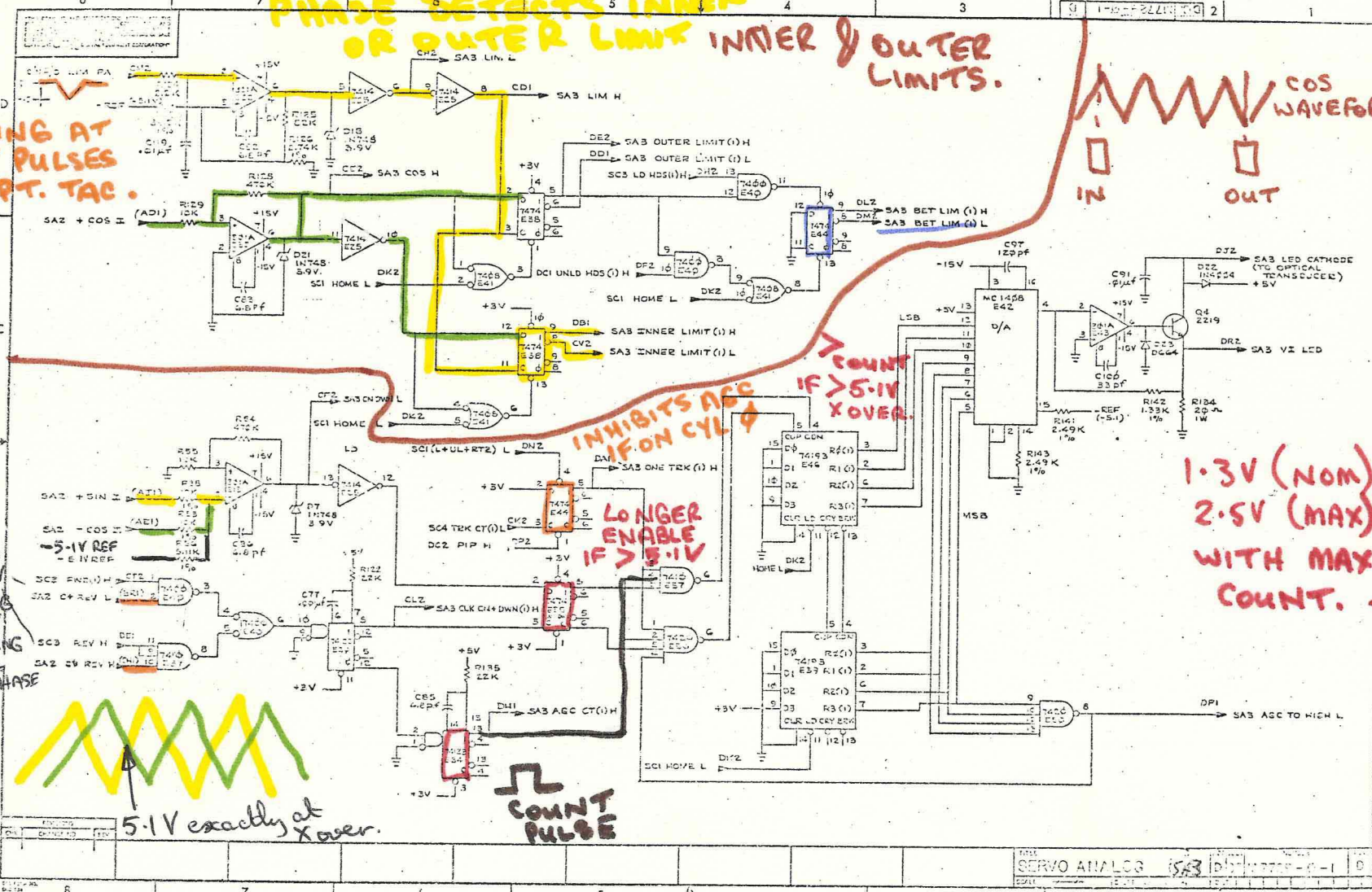
5.1V exactly at  
 X over.

COUNT  
 PULSE

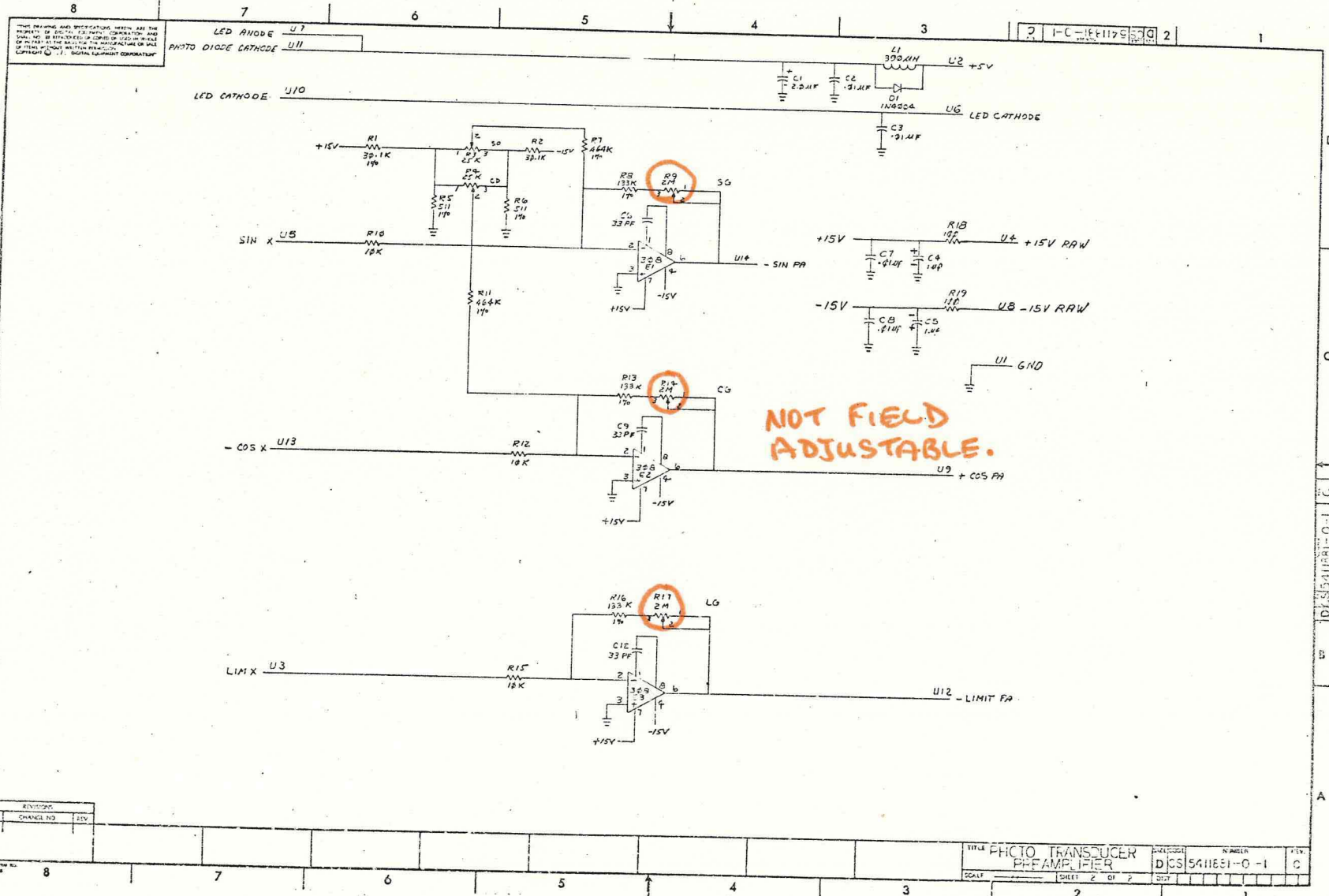
INHIBITS AGC  
 IF ON CYL 4

LONGER  
 ENABLE  
 IF > 5.1V

COUNT  
 IF > 5.1V  
 X OVER.







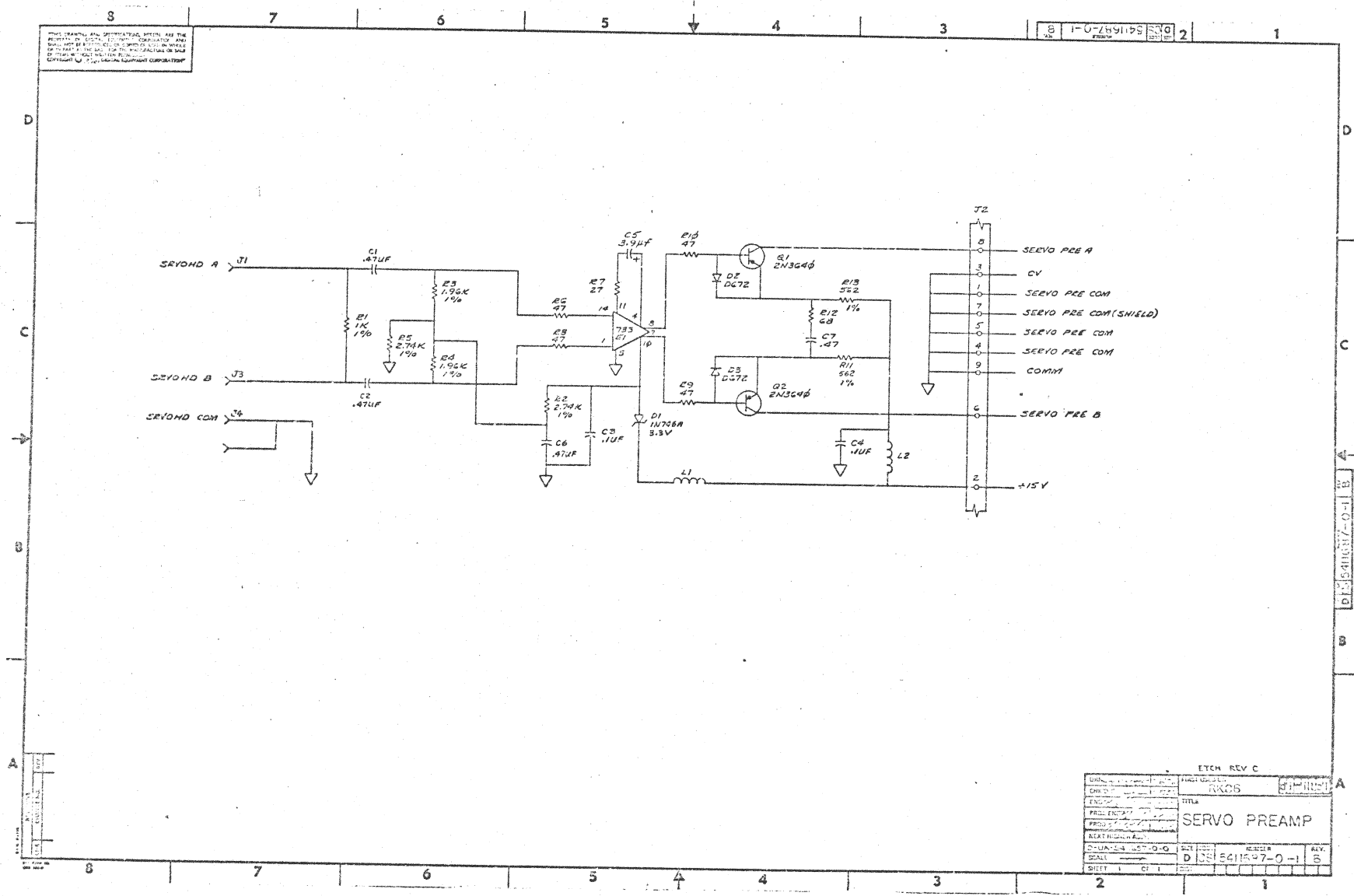
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REV	REVISIONS
1	CH1 CHANNEL NO 15V

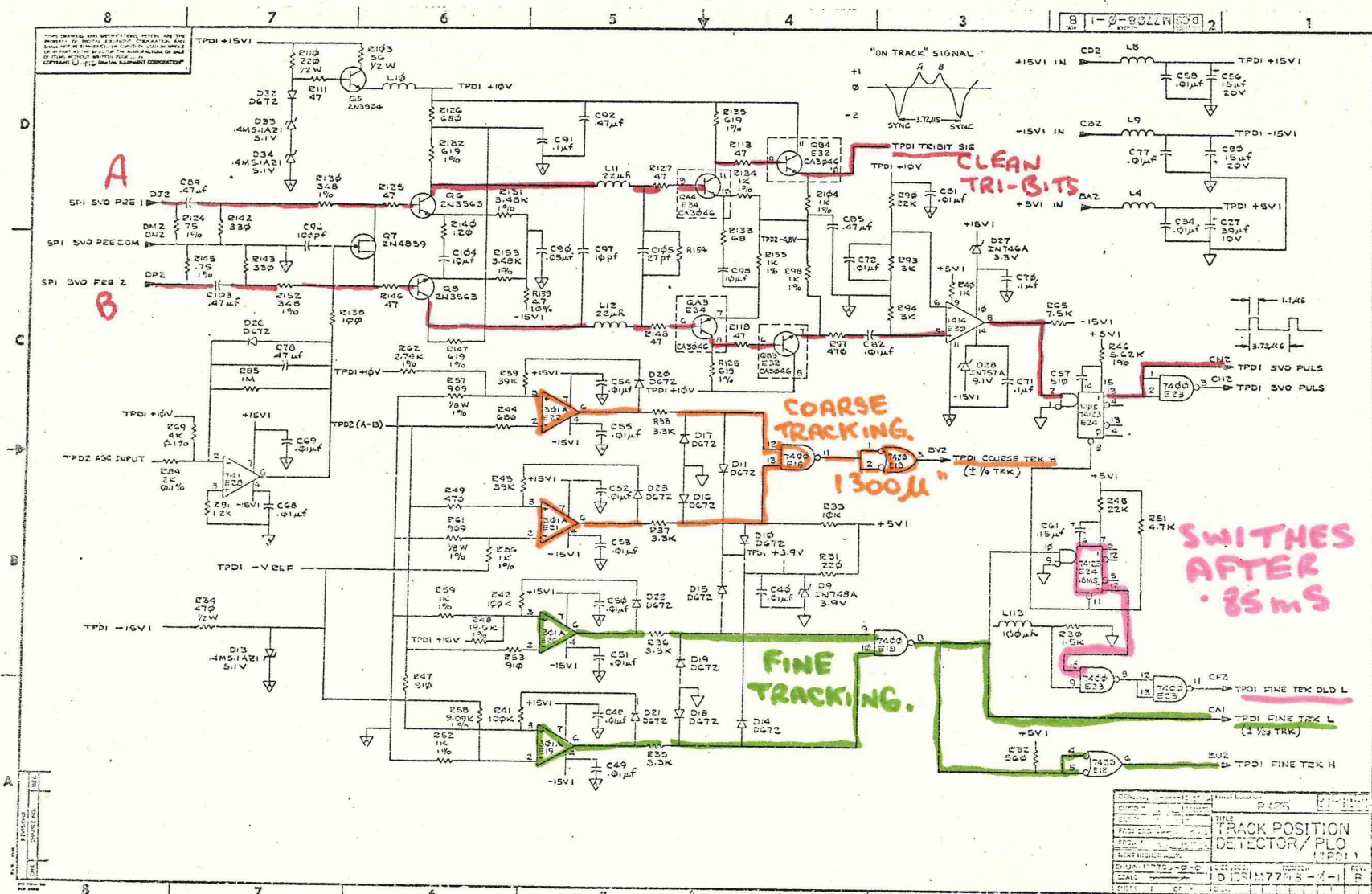
TITLE	PHOTO TRANSDUCER P-F AMPLIFIER	DESIGNER	NUMBER	REV
SCALE		DCS	5411631-0-1	C
		SHEET	2	OF
			2	

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1-0-7491105 2



ETCH REV C			
DESIGNED BY	DATE	REV	1
CHKD BY	DATE	REV	1
ENGR BY	DATE	REV	1
PROD ENGR BY	DATE	REV	1
PROD BY	DATE	REV	1
REVISIONS	DATE	REV	1
QUANTITY	DATE	REV	1
SCALE	DATE	REV	1
SHEET 1	OF 1	REV	1



A

B

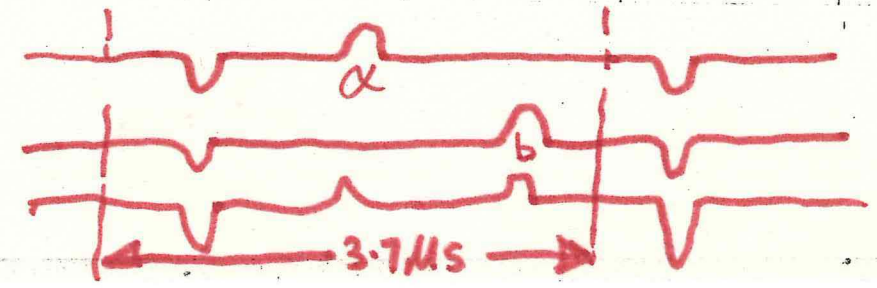
COARSE TRACKING.

FINE TRACKING.

CLEAN TRI-BITS

SWITCHES AFTER .85ms

BUMP DETECTOR IF OUTSIDE 250µ" FOR >.85ms.



TPD1.

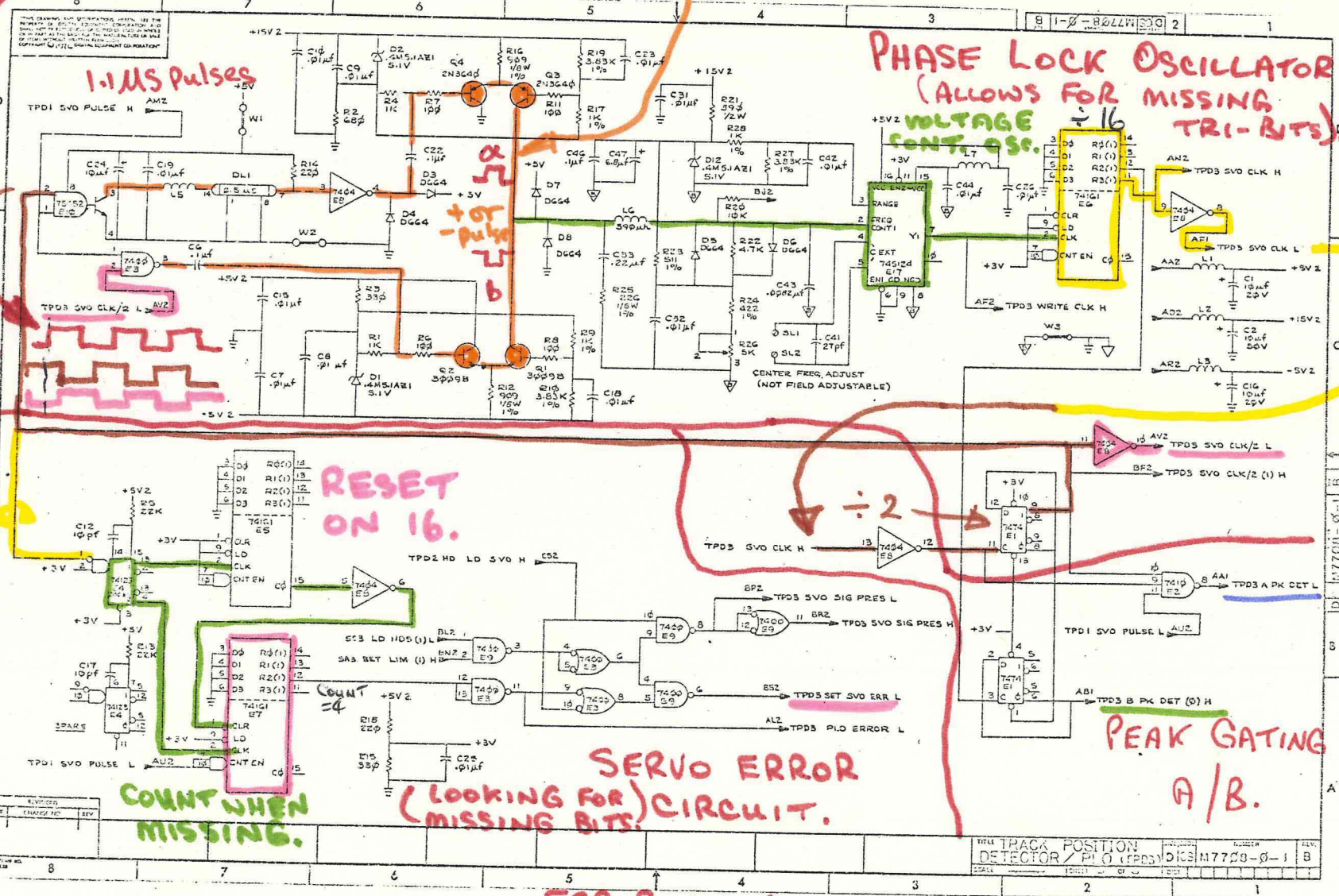
A  
B  
A+B

Pulse integrated & used as 1/P to VC8

SERVO PULSE

EVERY 3.72  $\mu$ S. SPLITS INCOMING WAVEFORM

SYNCHRONISED BITS.



1.1  $\mu$ S Pulses

PHASE LOCK OSCILLATOR (ALLOWS FOR MISSING TRI-BITS)

RESET ON 16.

SERVO ERROR (LOOKING FOR MISSING BITS) CIRCUIT.

COUNT WHEN MISSING.

PEAK GATING A/B.

GATES INCOMING PULSES

ERROR ON 4 MISSING BITS. (3 MISSING THEN O.K.)

TPD3

TITLE TRACK POSITION DETECTOR / P.O. (TPD3) DISM7700-0-1 B

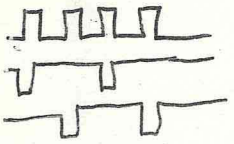


SPLIT DATA & CLK FF.

Power fluctuation compensation

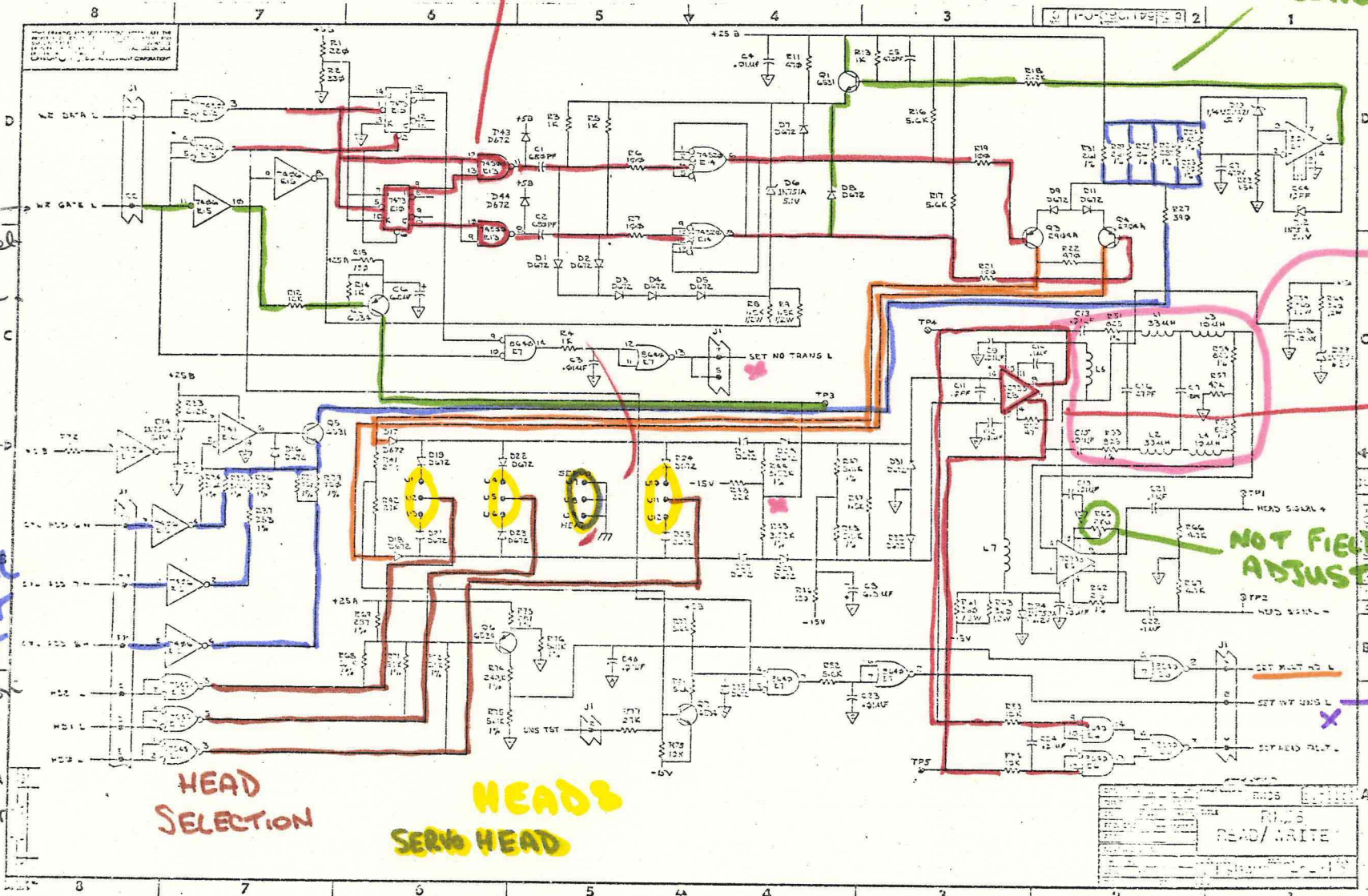
WRITE

Resets F/FS if not set hence we can't write



7-LEVEL CURRENT SELECT

Compensation for current dependant on inner or outer cylinder count



FILTER FOR MEC NOIS

FAULTY HEAD, BAD AM IMBALANCE IN HEAD O/P's.

NOT FIELD ADJUST

MULT HD SELECT

WRITE DATA BUT NO WRITE GATE.

HEAD SELECTION

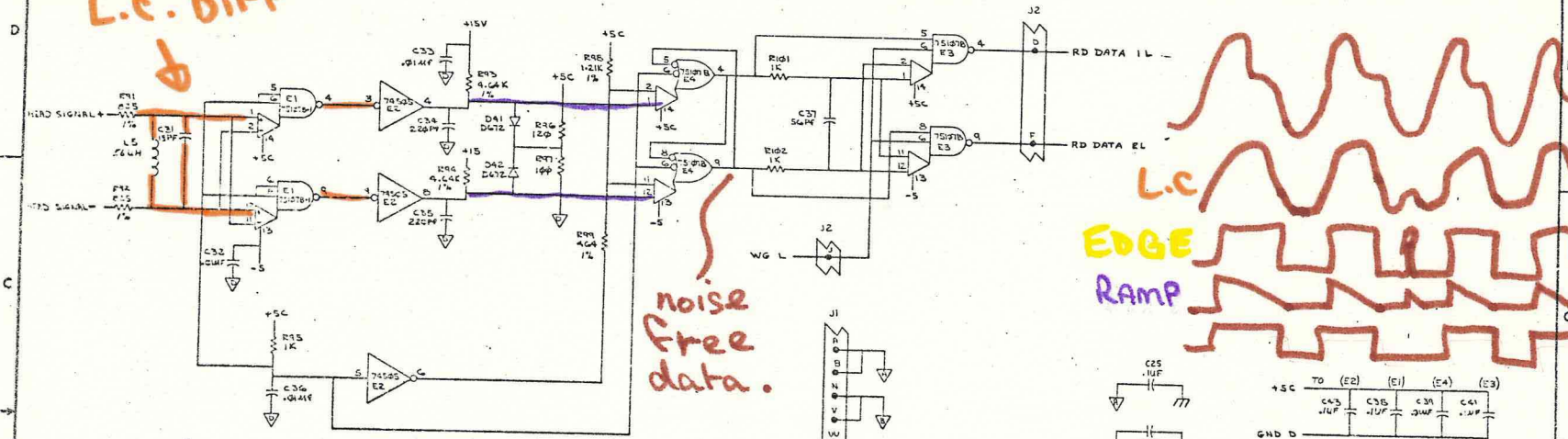
HEADS SERVO HEAD

ERRORS. i) x WR GATE BUT NO WRITE DATA → SET NO TRAN  
ii) x WR DATA - - - GATE → WT UNS

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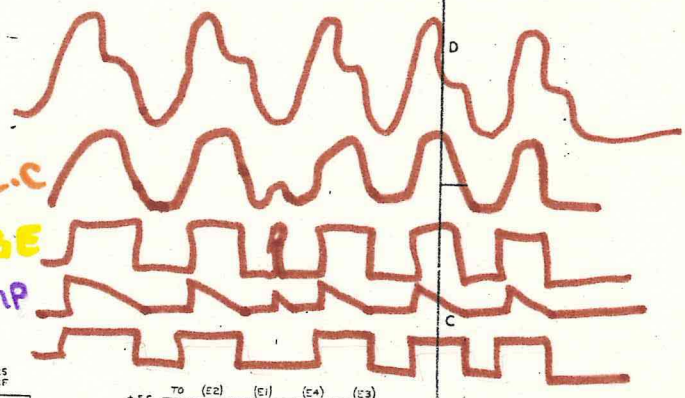
1-0-0-0-1  
 0 1 2 3 4 5 6 7 8

L.C. DIFF  
 ↓

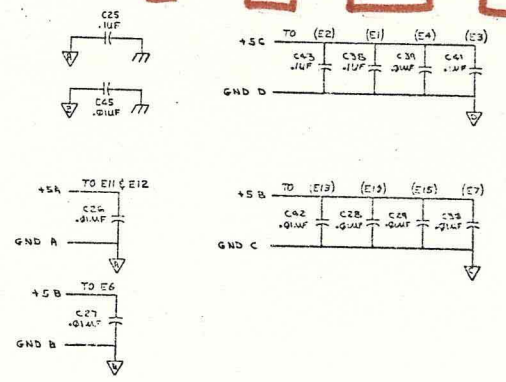
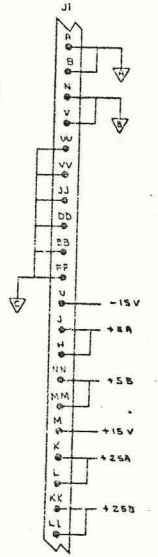
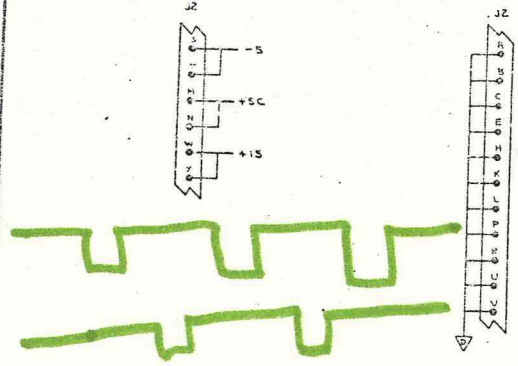


noise  
 free  
 data.

L.C.  
 EDGE  
 RAMP



READ  
 DATA  
 TO  
 CONTROLLER.



D.F.S.B. 11020-0-1

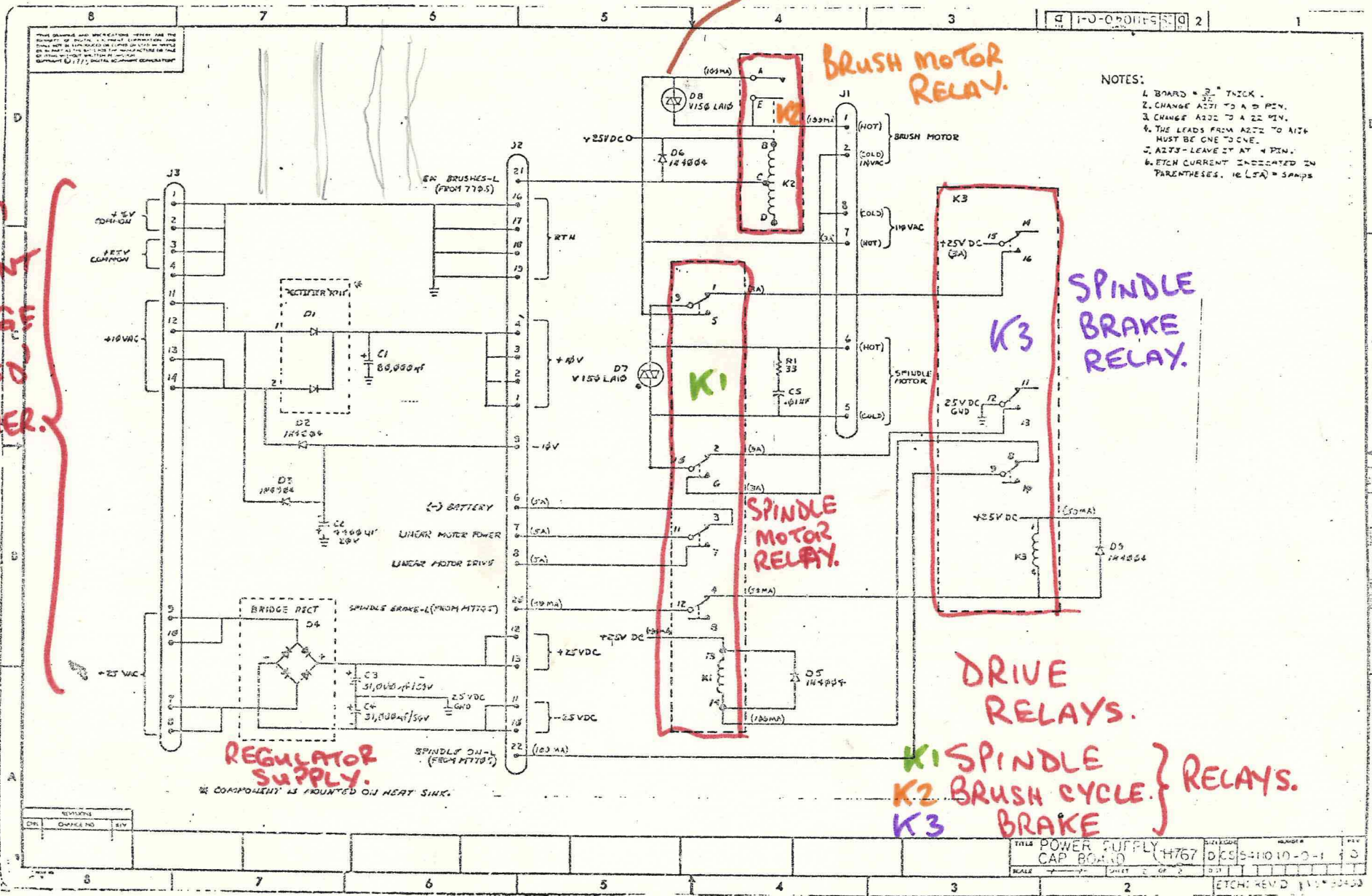
B

A

TITLE: RK05 READ/WRITE  
 SCALE: 10X  
 DRAWING: D.F.S.B. 11020-0-1  
 REV: C

VARISTOR.

From  
CONSTANT  
VOLTAGE  
'TUNED'  
X FORMER.



- NOTES:
1. BOARD = 3/16" THICK.
  2. CHANGE A271 TO A 25 PIN.
  3. CHANGE A232 TO A 22 PIN.
  4. THE LEADS FROM A271 TO A174 MUST BE ONE TO ONE.
  5. A273 - LEAVE IT AT 4 PIN.
  6. ETCH CURRENT INDICATED IN PARENTHESES. 16 (5A) = 5AMPS

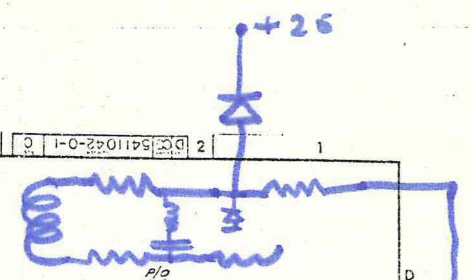
TITLE	POWER SUPPLY CAP BOARD	REV	1
DATE	11/10/77	DESIGNER	DES-11010-0-1
SCALE	1:1	DRW	3
ETCH: REV D		11/10/77	

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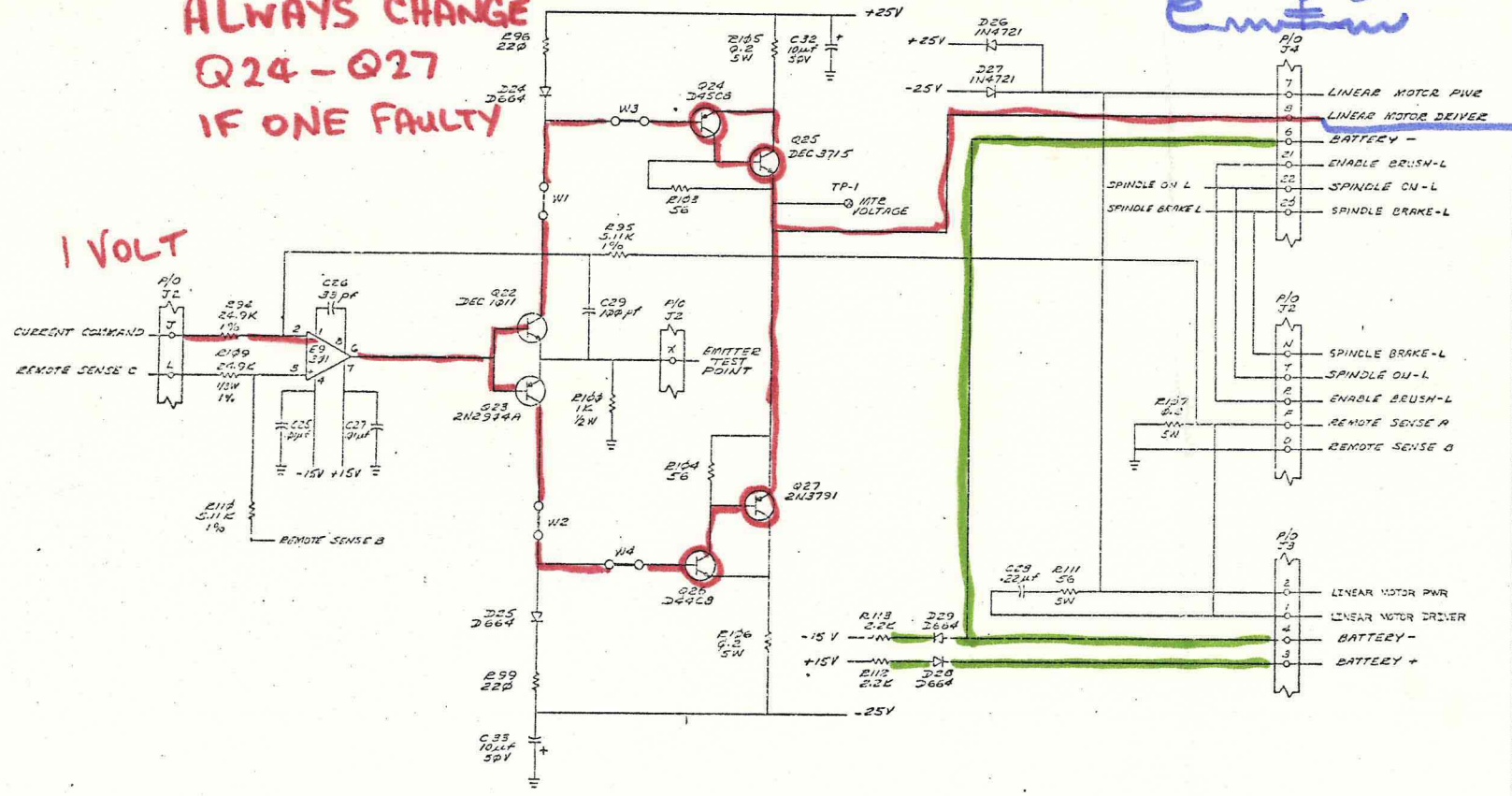
1-0-2-01119

**ALWAYS CHANGE  
Q24 - Q27  
IF ONE FAULTY**

**1 VOLT**



**POWER LOSS  
RELAY DROPS  
OUT. BATT.  
POWER  
RETRACTS  
HEADS.**



TITLE	H/67 POWER SUPPLY	REVISION	D/CS 54110-2-0-1	REV.	C
SCALE		DATE			

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BIASES X SISTER ON WHEN CURRENT FOLD BACK

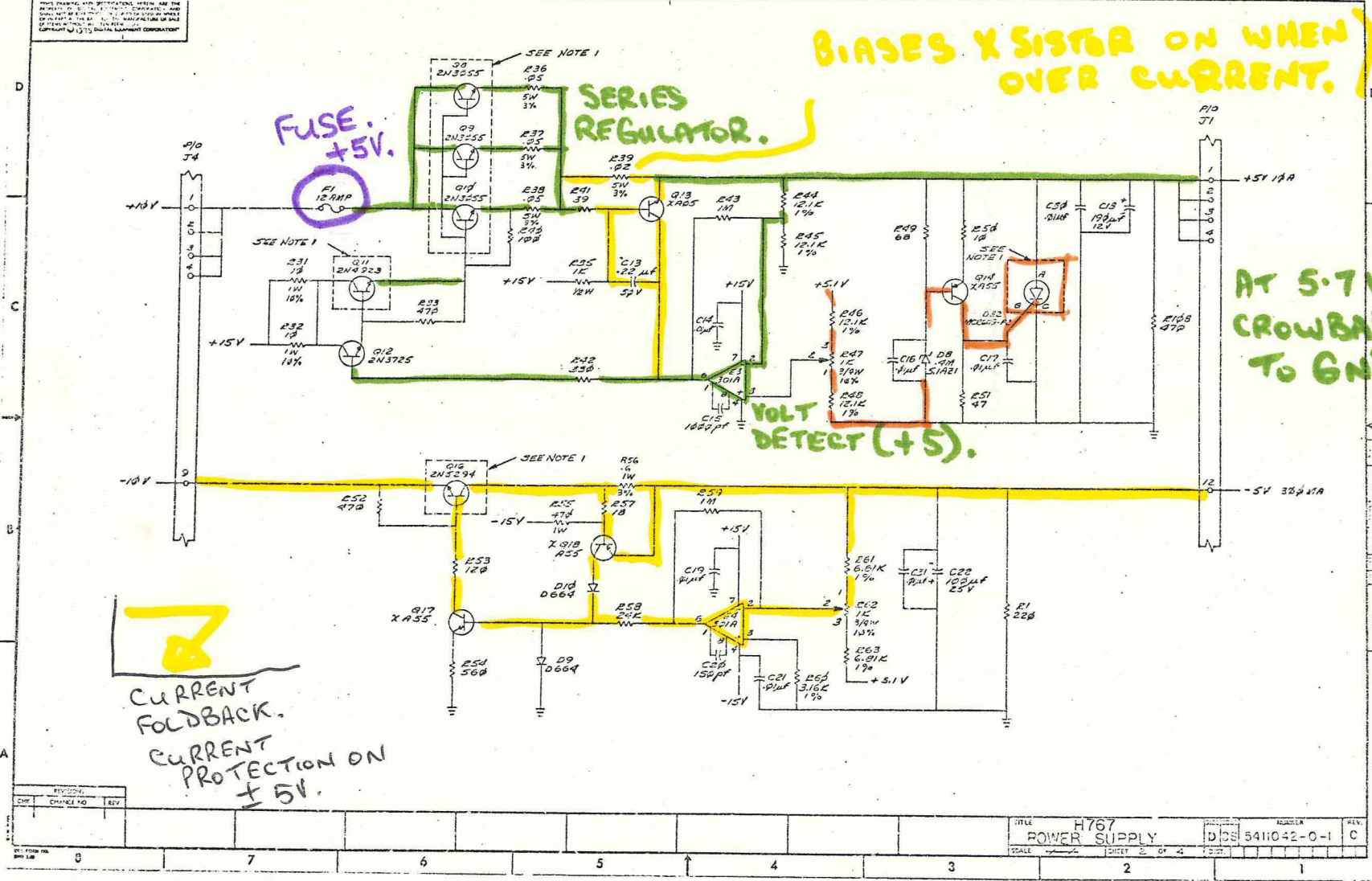
FUSE +5V.

SERIES REGULATOR.

AT 5.7V CROWBARS TO GND. VOLTAGE PROTECT +5V ONLY.

VOLT DETECT (+5).

CURRENT FOLDBACK. CURRENT PROTECTION ON ±5V.



REV	DATE	BY

