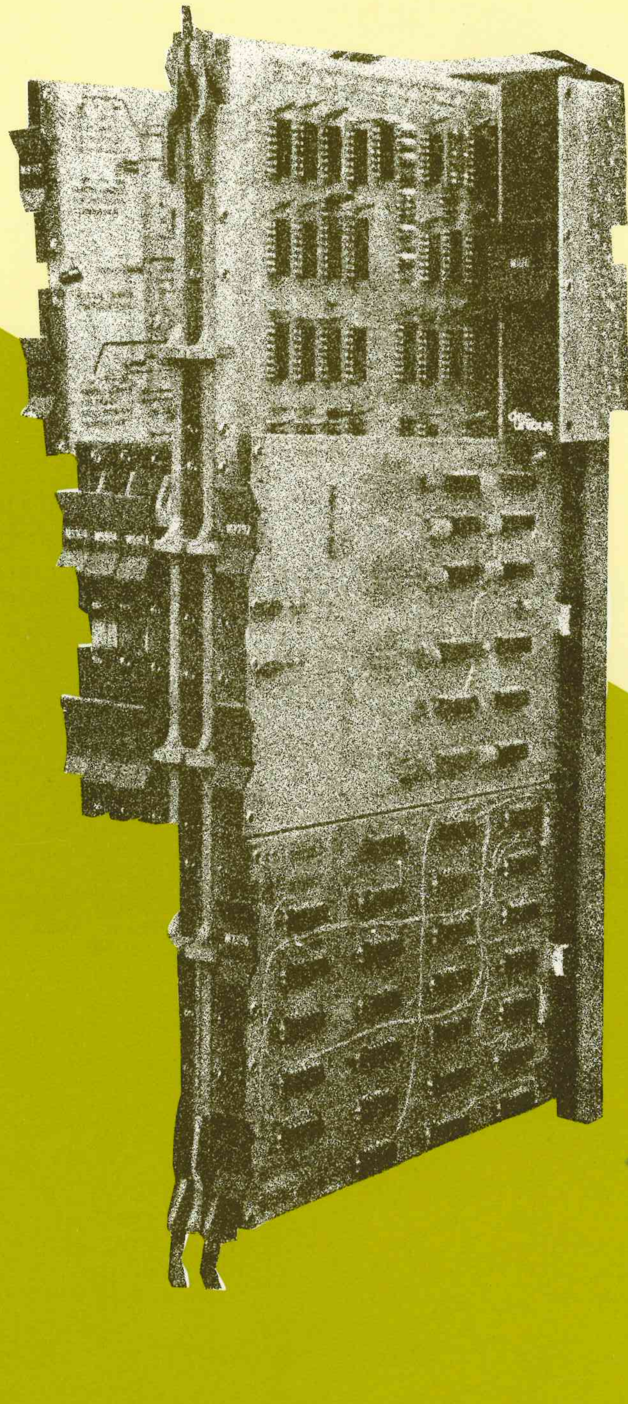
RH11/RH70 MASSBUS Controllers

A Self-Paced Course

Workbook 2



digital

RH11/RH70 MASSBUS CONTROLLERS SELF-PACED COURSE

WORKBOOK II

Document EY-D3022-WB-001
A Portion of Course EY-D3038-SP-001

Subsystem Registers

Register Control Path

Control Bus Interfacing

educational services development and publishing
digital equipment corporation
colorado springs, colorado

Printed in U.S.A.

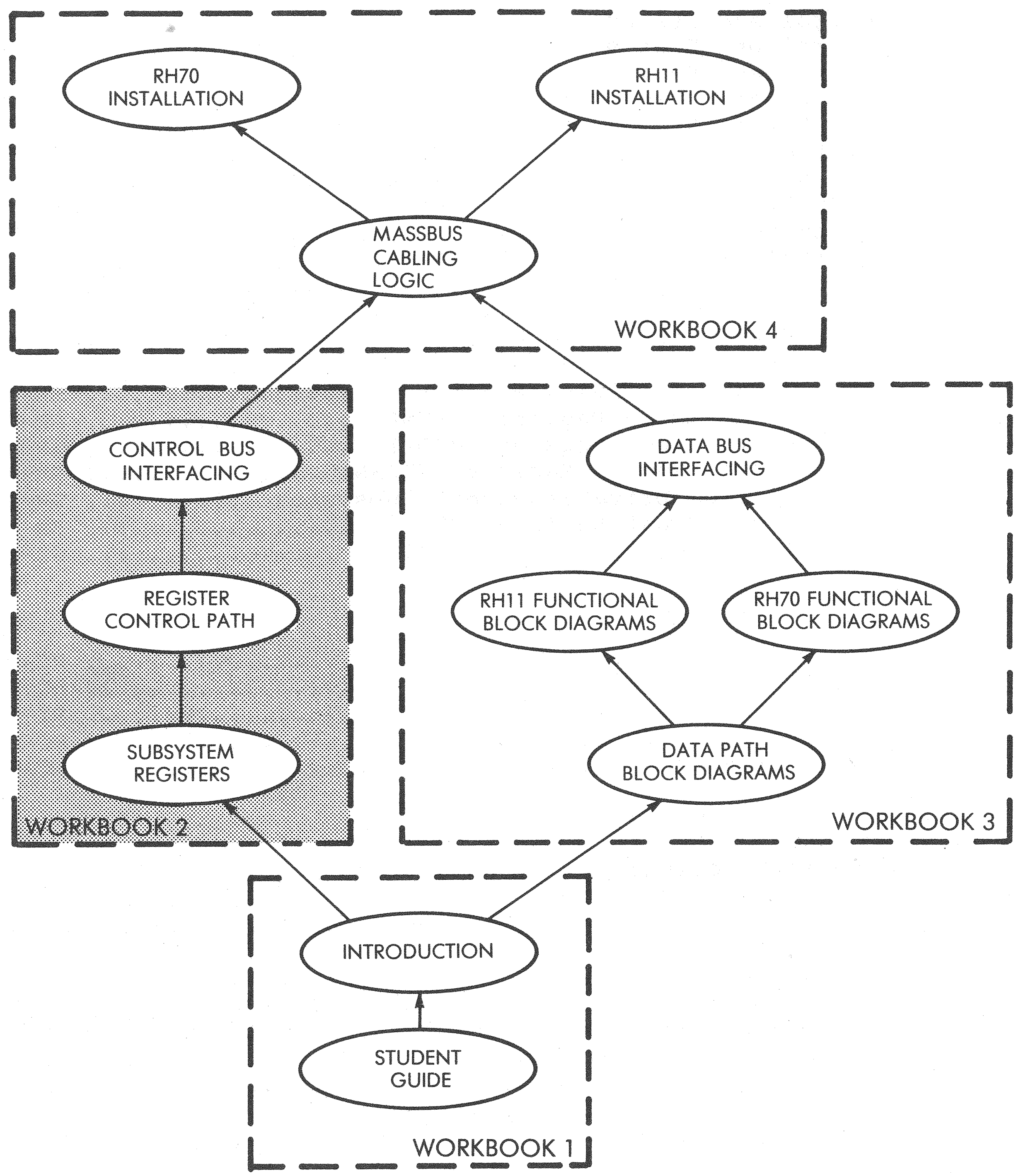
OUTLINE

Subsystem Registers

Register Control Path

Control Bus Interfacing

COURSE MAP



RH70 INSTALLATION
RH11 INSTALLATION
MASSBUS CABLING LOGIC
WORKBOOK 4
CONTROL BUS INTERFACING
REGISTER CONTROL PATH
SUBSYSTEM REGISTERS
WORKBOOK 2
DATA BUS INTERFACING
RH11 FUNCTIONAL BLOCK DIAGRAMS
RH70 FUNCTIONAL BLOCK DIAGRAMS
DATA PATH BLOCK DIAGRAMS
WORKBOOK 3
INTRODUCTION
STUDENT GUIDE
WORKBOOK 1

Subsystem Registers

SUBSYSTEM REGISTERS

INTRODUCTION

This module introduces the system of registers as used on Massbus controllers for the 11-family. The registers in any peripheral subsystem enables the subsystem to function independently of the central processor.

This module is divided into three sections. The first section describes the function and uses of the five registers in the RH11. These same five registers are also used in the RH7Ø. Only a few bits differ and the differences are pointed out in this first section. The second section describes the function and uses of two additional registers in the RH7Ø. The third section of this module contains a generalization of the registers contained within the peripheral devices themselves.

While reading through this module, it is not the intent to have you memorize the purpose of each bit in every register. Instead, learn the function of each register and how it is used in the subsystem.

OBJECTIVES

Given a list of RH subsystem registers and register definitions, be able to match the register with the definition.

ADDITIONAL RESOURCES

RJSØ4 Maintenance Manual, Paragraphs 3.6 - 3.1Ø, 3.15

RWPØ4 Maintenance Manual, Paragraphs 4.6 - 4.1Ø, 4.15

RJPØ5/Ø6 Maintenance Manual, Paragraphs 4.6 - 4.1Ø, 4.15

TJU16 Maintenance Manual, Paragraphs 3.6 - 3.6.5, 3.6.1Ø

SUBSYSTEM REGISTERS

There are two types of registers in an RH subsystem. Registers found in the controller are known as "local" registers, and registers located outside the controller are called "remote".

LOCAL REGISTERS

There are five registers in the RH11 Controller. Figure 1 represents the registers in an RH11/TMØ2 Tape Formatter subsystem. Notice the RH and TMØ2 share the CS1 register. The RH uses bits 15-13 and 1Ø-6. The device uses bits 12, 11 and 5-Ø. This sharing occurs with all RH-controlled peripheral devices.

The RH7Ø uses different buses than the RH11. Therefore some of the bits in these five registers have a different meaning in the RH7Ø. These differences are pointed out below. The added memory addressing requirements and parity control for the PDP-11/7Ø require two more registers in the RH7Ø. These two registers are discussed in the second section of this module.

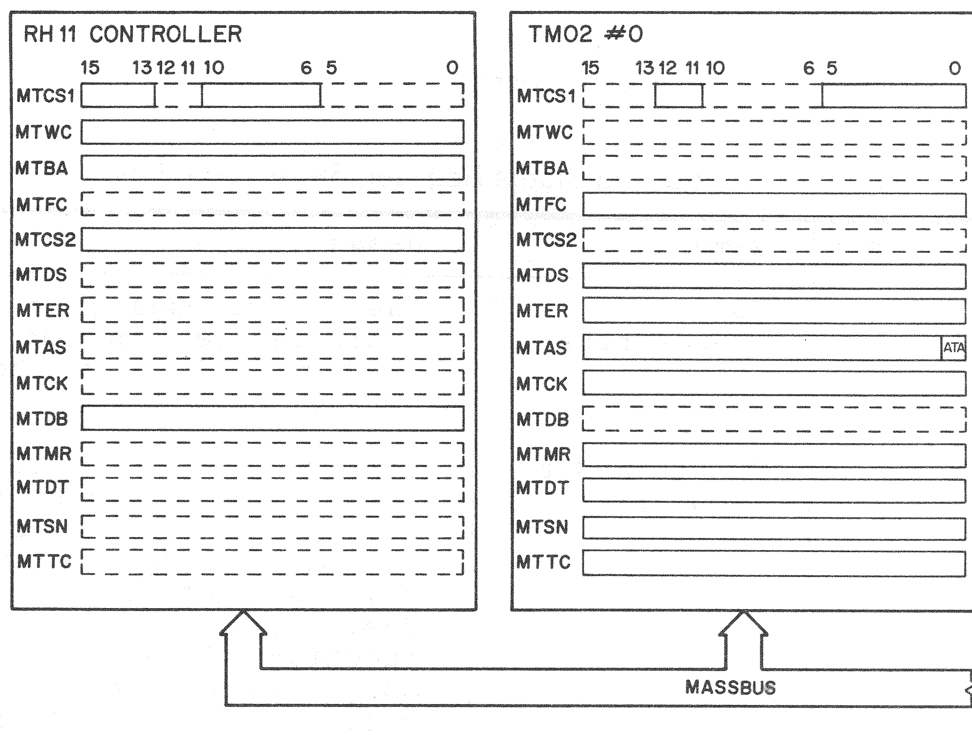


Figure 1 RH11/TM02 Tape Formatter Subsystem Registers

CONTROL AND STATUS REGISTER 1 (CS1)

This register is used by both the controller and the mass storage device to store the device commands and hold operational status. Register bits Ø through 5, 11 and 12 are dedicated for drive use and are physically located in each drive. When software is reading or writing this register, the selected drive (indicated by bits 2 through Ø in the Control and Status Register 2) will respond to those bit positions.

Figure 2 shows the register bit usage and Table 1 provides a description of each bit. The table also indicates whether a bit can be read or written by the system or host software.

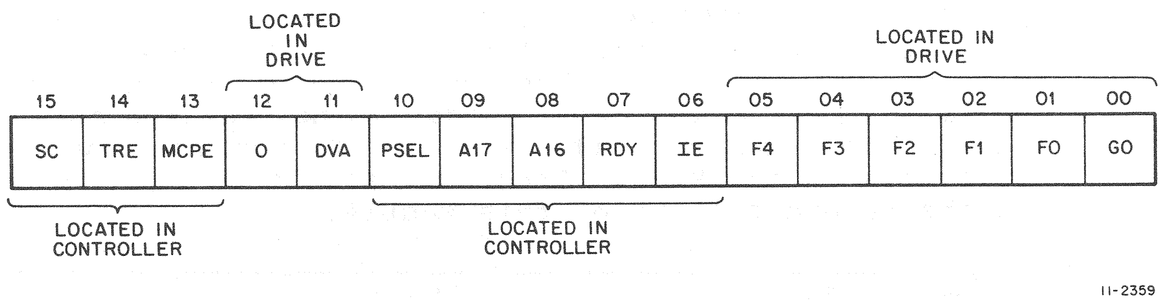


Figure 2 Control and Status Register 1

Table 1 Control and Status Register Bit Assignments

Bit(s)	Name	Usage
Ø	Go (Read/Write)	The device uses this bit to indicate the function loaded in bits 1-5 is to be executed.
1-5	Function Bits (Read/Write)	The exact definition of these bits depends on the particular peripheral. Because of the number of devices and codes, the RH does not have an illegal function checker. The RH only checks the function code to see if it is involved in the operation. The RH is not needed to carry out certain functions (such as a Seek).

Table 1 Control and Status Register

Bit Assignments (Cont)

Bit(s)	Name	Usage
6	Interrupt Enable (Read/Write)	When set this bit allows bus requests as a result of program interruptable conditions.
7	Controller Ready (Read Only)	A one indicates the controller is ready to receive a command.
8-9	Extended Bus Address Bits (Read/Write)	These two bits are an extension of the Bus Address register.
10	Data Port Select (Read/Write)	When this bit is set, data transfer is via Unibus B. When it is clear, data transfer is via Unibus A. **NOTE** **This bit is not used in the RH70.**
11	Device Available (Read Only)	This is a device-held status bit used for a dual-port disk drive to indicate to the RH whether the drive is available. (It may have its port select switch set to the opposite port, or set to A/B and in use by the other RH.)
12	Not Used	This is a device-assigned bit position, reserved for future use.
13	Massbus Control Bus Parity Error (Read Only)	This bit is set by a parity error on the Massbus control bus while reading a remote register. **NOTE** **The M7297 module in the RH11 has a LED to indicate this error.**

Table 1 Control and Status Register

Bit Assignments (Cont)

Bit(s)	Name	Usage
14	Transfer Error (Read/Write)	This RH error bit is set when any system errors are detected during data transfers.
15	Special Condition (Read Only)	This RH status bit is set by TRE or ATTN or Massbus Control Parity Error.

CONTROL AND STATUS REGISTER 2 (CS2)

This register contains the drive unit number and indicates the status of the controller. These bits indicate errors in the CPU/controller interface. (The one exception is bit 8; see Table 2.) The Field Service Engineer may waste a lot of time by assuming the problem is in the drive. Recognizing that the errors in this register are NOT associated with the drive will save troubleshooting time.

Figure 3 shows the register bit usage, and Table 2 provides a description of each bit.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

11-2363

Figure 3 Control and Status Register 2

Table 2 Control and Status Register 2 Bit Assignments

Bit(s)	Name	Usage
Ø-2	Unit Number (Read/Write)	These bits indicate the unit (device) number of the peripheral that is being accessed (or was last accessed). The RH11 could be controlling one unit that is performing a data transfer and simultaneously accessing a register in another unit. In this case, bits Ø-2 contain the unit number of the latter unit.
3	Bus Address Increment Inhibit (Read/Write)	When this bit is set, the RH will not increment the BA register during a data transfer.
4	Parity Test (Read/Write)	This is a maintenance diagnostic tool. While this bit is set, the RH generates even parity on both the control bus and data bus of the Massbus. When clear, odd parity is generated. While PAT is set, the RH checks for even parity received on the data bus but not the control bus.
5	Controller Clear (Write Only)	When a 1 is written into this bit, the RH and all drives are initialized.
6	Silo Input Ready (Read Only)	This serves as a status indicator for diagnostic check of the Silo buffer. This bit is set when software writes a word into the DB register.
7	Silo Output Ready (Read Only)	This serves as a status indicator for diagnostic check of the Silo buffer. This bit is set when a word is present in the DB and can be read by the software.

Table 2 Control and Status Register 2

Bit Assignments (Cont)

Bit(s)	Name	Usage
8	Massbus Data Bus Parity Error (Read Only)	This bit is set when a parity error occurs on the Massbus data bus while doing a read or write check operation. **NOTE** **The M7297 module in the RH11 has a LED to indicate this error.**
9	Missed Transfer (Read/Write)	This bit is set if the drive does not respond to a data transfer command within 250 milliseconds/(RH11) or 650 microseconds (RH70).
10	Program Error (Read Only)	This bit is set when the program attempts to initiate a data transfer operation while the RH is transferring data.
11	Nonexistent Memory (Read Only)	This bit is set when the controller is performing a DMA transfer and the memory address specified in the BA is nonexistent (i.e., does not respond to MSYN within 10 microseconds).
12	Nonexistent Drive (Read Only)	This bit is set when the program reads or writes a drive register in a drive which does not exist or is powered down.
13	Unibus Data Parity Error (RH11 Only) (Read/Write)	This bit is set if the Unibus parity lines indicate a parity error while the controller is performing a Write or Write Check command.

Table 2 Control and Status Register 2
Bit Assignments (Cont)

Bit(s)	Name	Usage
13 (Cont)	Unibus Data Parity Error (Cont)	**NOTE** **In the RH70 this error bit is called Parity Error (PE). The bit is set if a data parity error from memory is detected while the controller is performing a Write or Write Check command.**
14	Write Check Error (Read Only)	This bit is set when the controller is performing a Write Check operation and a word on the disk does not match the corresponding word in memory.
15	Data Late (Read Only)	This bit sets when either of the following occurs: • The controller is unable to supply a data word during a Write operation at the time the drive demands a transfer. • The controller is unable to receive a data word during a Read or Write Check operation at the time the drive demands a transfer.

BUS ADDRESS REGISTER (BA)

The RH uses this register to address the memory location involved in a data transfer. The BA register contains the lower 16 bits of the address. Combining the BA register with bits 8 and 9 of the CS1 register creates an 18-bit address used for the RH11. This register is loaded by the program with the starting memory address. Each time a DMA transfer is made, the register is incremented or decremented (read reverse for tape drive) twice. If the Bus Address Inhibit (BAI) bit (bit Ø3 of CS2) is set, the BA is not incremented. All transfers take place to or from the starting memory address. Figure 4 shows the BA register bit usage, and Table 3 provides a description of each bit.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	0

11-2361

Figure 4 Bus Address Register

Table 3 Bus Address Register Bit Assignments

Bit(s)	Name	Usage
ØØ	Not used	Always Ø
Ø1-15	Bus Address (Read/Write)	These bits are loaded by the program to specify the starting memory address of a transfer.

WORD COUNT REGISTER (WC)

This register is loaded by the program with the 2's complement of the number of words to be transferred. During a data transfer, it is incremented each time a word is transferred to or from memory. A maximum of 64,ØØØ words can be transferred with one WC register load operation. Figure 5 shows the register bit arrangement, and Table 4 provides a description of each bit.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

11-2360

Figure 5 Word Count Register

Table 4 Word Count Register Bit Assignments

Bit(s)	Name	Usage
ØØ-15	Word Count (Read/Write)	These bits are set by the program to specify the number of words to be transferred (2's complement form).

DATA BUFFER REGISTER (DB)

The Data Buffer (DB) register has three functions:

- A software-addressable register to test the Silo memory
- A software-addressable register to test the Data Late error logic
- An NPR-addressable register for data transfers.

The Data Buffer register provides a maintenance tool to test the Silo data buffer. Physically, the Data Buffer is two registers, the output and input buffers. A 64 word Silo memory is between these two registers. Any data applied to the input buffer is automatically moved through the Silo. Figure 6 is a simplified block diagram showing this function.

1. A MOV instruction passes a test word from core to the address known as DATA BUFFER.

2. This test word is moved from the input buffer through the Silo.

3. The test word is then loaded into the output buffer.

4. When the DATA BUFFER is accessed to read the test word, the contents of the <u>output buffer</u> is read.

   This tests the operation of the Silo and its two buffers.

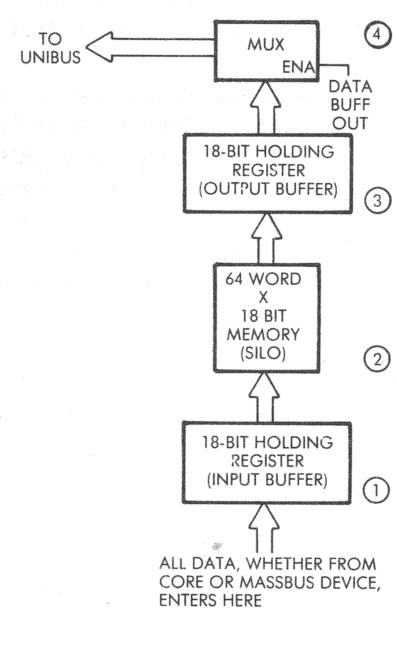


Figure 6 Silo Simplified Block Diagram

The Data Buffer register can be read and written only as an entire word. Any attempt to write a byte will write an entire word. Reading the DB register is a destructive readout operation. In this case, the top data word in the Silo buffer is removed. Then a new data word (if present) replaces it a short time later. Conversely, the action of writing the DB register does not destroy the contents of the DB. It merely causes one more data word to be inserted into the Silo buffer (if it was not full).

During a data Read, the output buffer is strobed onto the Unibus. During a data Write the data on the Unibus is strobed into the input buffer. This action is controlled by the NPR logic and does not involve software.

The Data Late (DLT) error circuitry is checked by addressing the data buffer. A DLT error occurs if the diagnostic program attempts to write into a full buffer (66 words). Also, if the software attempts to read data and the buffer is empty, the circuitry generates DLT. Successive MOV's from the DB read words in the same order in which they entered the Silo. The Input Ready (IR) and Output Ready (OR) status indicators in the CS2 register are provided for the programmer. They indicate when words can be read from or written into the DB. IR should be asserted before attempting a write into the DB. OR should be asserted before attempting a read from the DB.

Figure 7 shows the DB bit usage, and Table 5 provides a description of each bit.

NOTE

The Data Buffer is shown as 16 bits. Actually the RH11 is strappable to accommodate 18 bits. This allows a PDP-11 processor to communicate with a PDP-15 or a DECsystem-1Ø processor.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB15	DB14	DB13	DB12	DB11	DB1Ø	DBØ9	DBØ8	DBØ7	DBØ6	DBØ5	DBØ4	DBØ3	DBØ2	DBØ1	DBØØ

11-2491

Figure 7 Data Buffer Register

Table 5 Data Buffer Register Bit Assignments

Bit(s)	Name	Usage
00-15	Data Buffer (Read/Write)	When these bits are read, the contents of OBUF (internal RH register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When these bits are written, data is loaded into IBUF (internal RH register) and allowed to sequence into the Silo if space is available.

NOTE

The data buffer in the RH70 has the same functions. The difference is that the data buffer area is physically eight registers functioning as a First-In-First-Out buffer. The RH70 buffer operation is covered in detail in another module.

ADDITIONAL REGISTERS FOR RH70

The RH70 has the same registers as the RH11 plus two more, the Bus Address Extension Register and Control and Status Register 3 (illustrated by shaded areas on Figure 8).

BUS ADDRESS EXTENSION REGISTER (BAE)

The Bus Address Extension (BAE) register contains the six most significant bits of the memory address. They combine with the 16-bits of the BA register to form the complete 22-bit address. This register should be loaded in conjunction with the BA register. These two registers will then specify the starting memory address of a data transfer operation. The six bit field is incremented (decremented) each time a carry (borrow) occurs from the BA register.

Address bits A16 and A17 are set or cleared through the CS1 register. A16 and A17 should not be altered when loading CS1. This alteration can be avoided by using a "write low byte" instruction, or by writing the correct value of A16 and A17 into CS1.

Figure 9 shows the BAE register bit usage and Table 6 provides a description of each bit.

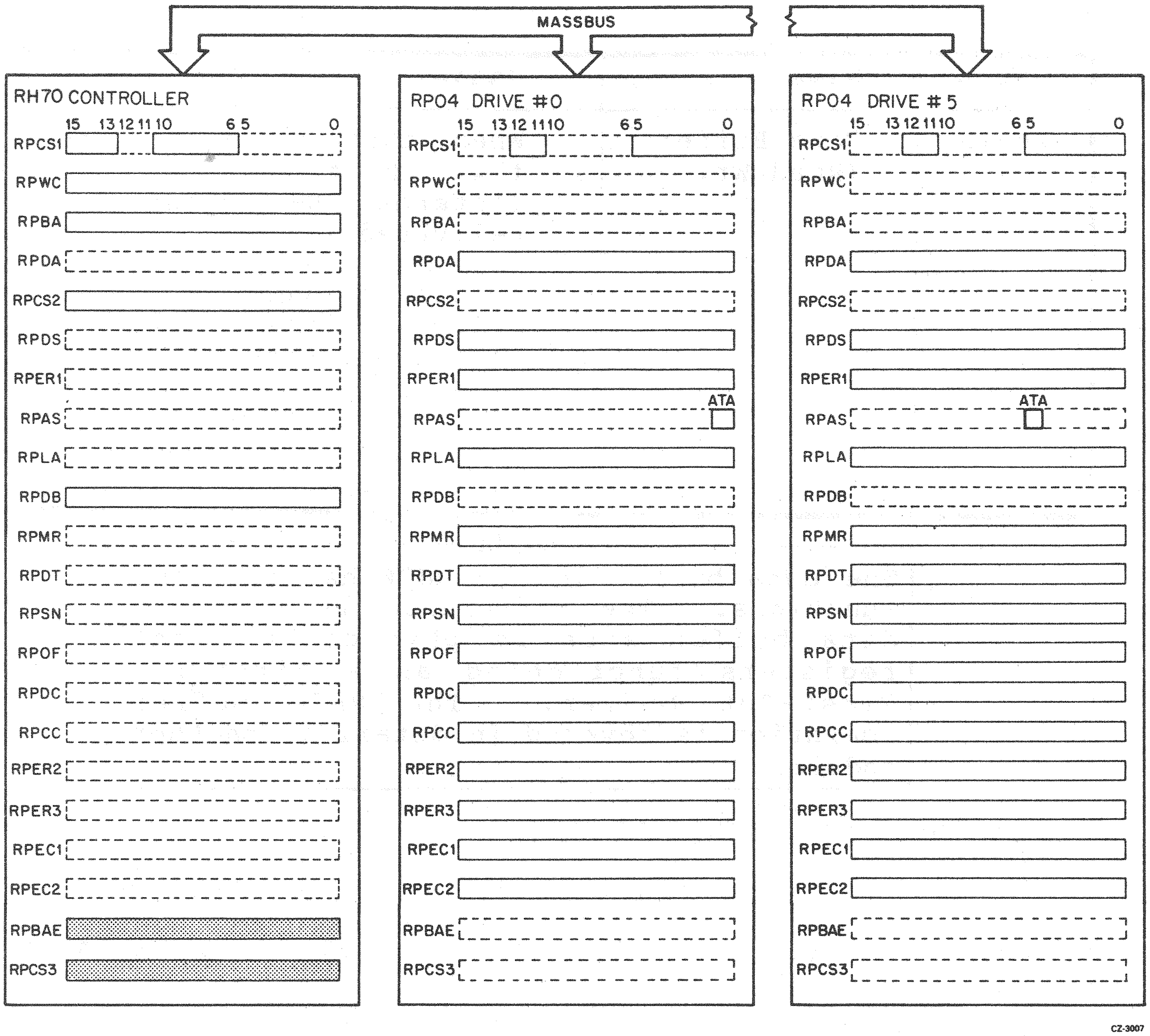


Figure 8 RWP04 Subsystem Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	A21	A20	A19	A18	A17	A16

11-2906

Figure 9 Bus Address Extension Register

Table 6 Bus Address Extension Register Bit Assignments

Bit(s)	Name	Usage
Ø6-15	Not used	-
Ø-Ø5	Bus Address (Read/Write)	These bits are a 5-bit extension of the BA register. These two register combine to make the 22-bit address for a data transfer.

NOTE

Bit Ø (A16) and bit 1 (A17) are the same as bits 8 and 9 of CS1.

CONTROL AND STATUS REGISTER 3 (CS3)

The Control and Status Register 3 (CS3) (Figure 1Ø) contains parity error information associated with the memory bus. Parity Error (bit 14 of CS2) indicates that a parity error occurred during the memory transfer. Bits 13 through 15 of CS3 further localize the error for diagnostic maintenance. In addition, bits Ø through 3 provide the diagnostic program with the ability to generate bad parity. This allows the diagnostic to verify operation of the parity circuits.

The Interrupt Enable bit (Ø6) in the CS3 register is the same as bit 6 in CS1. The IE bit in the CS3 register allows the program to enable interrupts without writing into a drive register. It is set or cleared by writing into either register.

Figure 1Ø shows the CS3 register bit usage and Table 7 provides a description of each bit.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
APE	DPE OW	DPE EW	WCE OW	WCE EW	DBL	Ø	Ø	Ø	IE	Ø	Ø	IPCK 3	IPCK 2	IPCK 1	IPCK 0

11-2907

Figure 10 Control and Status Register 3

Table 7 Control and Status Register 3
Bit Assignments

Bit(s)	Name	Usage
Ø-3	Invert Parity Check (Read/Write)	These bits are written by the program to control the data parity detection logic. When they are set, inverse parity is checked with data during memory transfers of Write and Write Check operations.
4-5	Not Used	
6	Interrupt Enable (Read/Write)	IE is a control bit which can be set under program control. When IE=1, an interrupt may occur due to RDY or SC being asserted.
7-9	Not Used	
1Ø	Double Word (Read Only)	This bit is set if the last memory transfer was a double word operation.
11-12	Write Check Error Even Word (11) Odd Word (12) (Read Only)	This bit is set when memory data does not match data from the drive.
13-14	Data Parity Error Even Word (13) Odd Word (14) (Read Only)	This bit is set if a parity error is detected on data from memory when the RH7Ø is performing a Write or Write Check command.
15	Address Parity Error (Read Only)	This bit is set if the address parity error line indicates that the memory detected a parity error on address and control information during a memory transfer.

REMOTE REGISTERS

The remote registers are located in the drives. This section of the module does not describe each bit in each remote register. Instead, the text lists which registers are in which devices and briefly describes their uses. These remote registers are described in detail in the specific device courses.

The number of remote registers vary from drive to drive. The RS04 has 8 registers, while the RP drives have 16 registers (see Figure 8). The following example describes the RP04 registers for a disk drive and then discusses the differences for a TM02/TU16 tape drive.

RWP04 DISK DRIVE SUBSYSTEM

Figure 11 contains the register summary for the RWP04 (RH70/RP04) subsystem.

Error Registers - The RP04 has three error registers (RPER 1, 2 and 3). RPER1 contains errors associated with data transfers. RPER2 and RPER3 contain detailed error status information and are primarly used for monitoring the electromechanical performance of the drive.

Address Registers - The RP has two registers that define the addresses on the disk pack:

- Disk Address register (RPDA) contains the sector and track address
- Desired Cylinder register (RPDC) contains the cylinder address.

Associated with the RPDC register is the Current Cylinder register (RPCC). This register contains the present cylinder address if the drive is not seeking.

The Look-Ahead register (RPLA) contains information pertaining to the present sector under the read/write heads. This register provides the programmer with the means of optimizing disk access by minimizing rotational delays.

The Offset register (RPOF) allows the software to move (offset) the positioner from data track centerline in small amounts. The register contains the amount of microinches that the positioner is to move. Offsetting allows the software to recover data that is not recoverable by the Error Correcting Code (ECC) logic due to small amounts of head misalignment.

Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RPDB (776722)	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB Ø
RPMR (776724)	Ø	Ø	Ø	Ø	Ø	Ø	SBD	ZDI	DEN	ECCE	MWR	MRD	MSCLK	MIND	MCLK	DMD
RPDT (776726)	NBA	TAP	MOH	Ø	DRQ	Ø	Ø	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT Ø
RPSN (776730)	SN 38	SN 34	SN 32	SN 31	SN 28	SN 24	SN 22	SN 21	SN 18	SN 14	SN 12	SN 11	SN 8	SN 4	SN 2	SN 1
RPOF (776732)	SGCH	Ø	Ø	FMT 22	ECCI	HCI	Ø	Ø	OFS 7	OFS 6	OFS 5	OFS 4	OFS 3	OFS 2	OFS 1	OFS Ø
RPDC (776734)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	DC 9	DC 8	DC 7	DC 6	DC 5	DC 4	DC 3	DC 2	DC 1
RPCC (776736)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	CC 9	CC 8	CC 7	CC 6	CC 5	CC 4	CC 3	CC 2	CC 1
RPCS1 (776700)	SC	TRE	MCPE	Ø	DVA	Ø	A17	A16	RDY	IE	F4	F3	F2	F1	FØ	GO
RPWC (776702)	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 9	WC 8	WC 7	WC 6	WC 5	WC 4	WC 3	WC 2	WC 1	WC Ø
RPBA (776704)	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 9	BA 8	BA 7	BA 6	BA 5	BA 4	BA 3	BA 2	BA 1	BA Ø
RPDA (776706)	Ø	Ø	Ø	TA 16	TA 8	TA 4	TA 2	TA 1	Ø	Ø	Ø	SA 16	SA 8	SA 4	SA 2	SA 1
RPCS2 (776710)	DLT	WCE	PE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	UØ
RPDS (776712)	ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	DE1	DL64	GRV	DIGB	DF20	DF5
RPER1 (776714)	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF
RPAS (776716)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA Ø
RPLA (776720)	Ø	Ø	Ø	Ø	Ø	SC 4	SC 3	SC 2	SC 1	SC Ø	EXT 1	EXT Ø	Ø	Ø	Ø	Ø
RPER2 (776740)	AC UNS	Ø	PLU	3ØVU	IXE	NAS	MHS	WRU	FEN	TUF	TDF	MSE	CSU	WSU	CSF	WCU
RPER3 (776742)	OCYL	SKI	Ø	Ø	Ø	Ø	Ø	Ø	Ø	ACL	DCL	PRE	UWR	Ø	VUF	PSU
RPEC1 (776744)	Ø	Ø	Ø	BLC 4096	BLC 2048	BLC 1024	BLC 512	BLC 256	BLC 128	BLC 64	BLC 32	BLC 16	BLC 8	BLC 4	BLC 2	BLC 1
RPEC2 (776746)	Ø	Ø	Ø	Ø	Ø	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RPBAE(776750)	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	A21	A20	A19	A18	A17	A16
RPCS3 (776752)	APE	DPE HI	DPE LO	WCE HI	WCE LO	DBL	Ø	Ø	Ø	IE	Ø	O	IPCK 3	IPCK 2	IPCK 1	IPCK Ø

11-2770

Figure 11 RH70/RP04 Subsystem Register Summary

Error Correction Code Registers (RPEC1 & 2) - The RP04 has an ECC capability which detects and locates errors (within limits) by reconstructing a portion of the data. The ECC Position (RPEC1) and ECC Pattern (RPEC2) registers are used in the system software correction process.

Drive Status (RPDS) and Attention Summary (RPAS) Registers - The Drive Status register contains the various status indicators for the selected drive. The Attention Active (ATA) bit is set whenever the drive has an error condition or has finished executing a non-data transfer function (i.e., Seek or Search). The ATA bit, in turn, sets the Special Condition bit (Bit 15 of RPCS1) which causes an interrupt if the IE bit is set.

During the interrupt service routine, the software will read the Attention Summary register. By reading this register and testing the bits, the service routine determines which drive needs servicing (attention).

The controller requests Attention Summary status from all drives simultaneously. Each drive places the output of its Attention Active flip-flop (Bit 15 of RPDS) on the Control Bus line that corresponds to its unit number (refer to the RPAS register shown in Figure 8).

Maintenance Register (RPMR) - The Maintenance register simulates various signals from the disk to allow diagnostic testing of the drive.

Drive Type Register (RPDT) - The Drive Type register contains a number (bits 0-8) representing the drive type (RS04 = 002, RP05 = 021, TU16 = 011). The most significant bits further define the type of peripheral. This register allows the program to distinguish between the different classes of drives.

Serial Number Register (RPSN) - The purpose of this register is to allow a drive to be distinguished from similar drives attached to the same controller. This information is useful during the decode of error logging because of errors associated with a particular drive. By error logging the serial number instead of the drive number, the field service engineer can determine the failing unit even if the user has switched unit number plugs. The serial number of the drive itself is provided in BCD form with jumpers or DIP switches.

TJU16 TAPE DRIVE TRANSPORT SUBSYSTEM

Figure 12 is the register summary for the TJU16 (RH11/TM021/TU16) subsystem.

The following registers have the same type of function in the TM02 as they do in the RP04:

- Drive Status (MTDS)
- Error (MTER)
- Attention Summary (MTAS)
- Data Check (MTCK)
- Maintenance (MTMR)
- Drive Type (MTDT)
- Serial Number (MTSN)

Frame Count Register (MTFC) - The Frame Count register counts tape events. During a data transfer operation this register is incremented for each character transfer (one frame). During space operations, however, the register is incremented each time a record is detected.

Tape Control Register (MTTC) - This register is loaded by the software to select a transport, the data format, and the density.

SUMMARY

The RH11 and RH70 contain registers that are found in any controller. These registers are:

- Control and Status 1 - stores commands and operational status and is shared between controller and drive
- Word Count - contains 2's complement of the number of words to be transferred to/from memory
- Bus Address - contains address of the memory location involved in a data transfer
- Control and Status 2 - indicates the status of the controller and contains the drive unit number
- Data Buffer - provides a maintenance tool to check the data buffer
- Bus Address Extension (RH70 only) - contains the upper six bits of the memory address
- Control and Status 3 (RH70 only) - contains parity error information associated with the memory bus

Register	Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTCS1	772440	SC	TRE	MCPE	O	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	FØ	GO
MTWC	772442	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC ØØ
MTBA	772444	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	BA ØØ
MTFC	772446	FC 15	FC 14	FC 13	FC 12	FC 11	FC 10	FC 09	FC 08	FC 07	FC 06	FC 05	FC 04	FC 03	FC 02	FC 01	FC ØØ
MTCS2	772450	DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	UØ
MTDS	772452	ATA	ERR	PIP	MOL	WRL	EOT	Ø	DPR	DRY	SSC	PES	SDWN	IDB	TM	BOT	SLA
MTER	772454	COR/ CRC	UNS	OPI	DTE	NEF	CS/ ITM	FCE	NSG	PEF/ LRC	INC/ VPE	DPAR	FMT	CPAR	RMR	ILR	ILF
MTAS	772456	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	ATA Ø7	ATA Ø6	ATA Ø5	ATA Ø4	ATA Ø3	ATA Ø2	ATA Ø1	ATA ØØ
MTCK	772460	Ø	Ø	Ø	Ø	Ø	Ø	Ø	CRCP / DTP	CRC7 / DT7	CRC6 / DT6	CRC5 / DT5	CRC4 / DT4	CRC3 / DT3	CRC2 / DT2	CRC1 / DT1	CRCØ / DTØ
MTDB	772462	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB ØØ
MTMR	772464	MDF Ø8	MDF Ø7	MDF Ø6	MDF Ø5	MDF Ø4	MDF Ø3	MDF Ø2	MDF Ø1	MDF ØØ	200 BPI CLK	MC	MOP Ø3	MOP Ø2	MOP Ø1	MOP ØØ	MM
MTDT	772466	NSA	TAP	MOH	7CH	DRQ	SPR	Ø	DT Ø8	DT Ø7	DT Ø6	DT Ø5	DT Ø4	DT Ø3	DT Ø2	DT Ø1	DT ØØ
MTSN	772470	SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 09	SN 08	SN 07	SN 06	SN 05	SN 04	SN 03	SN 02	SN 01	SN ØØ
MTTC	772472	ACCL	TCW	FCS	EAO DTE	Ø	DEN Ø2	DEN Ø1	DEN ØØ	FMT SEL Ø3	FMT SEL Ø2	FMT SEL Ø1	FMT SEL ØØ	EV PAR	SS 2	SS 1	SS Ø

CZ-3008

Figure 12 RH11/TM02 Register Summary

EXERCISES

Answer the following questions using any of your reference materials. Discuss any problems you have with another student or your course administrator. The solutions are on the next page.

1. Where is a "remote" register located?

2. Which register is shared by both the controller and the device?

3. Which register contains the 2's complement of the number of words to be transferred to memory?

4. Which register holds the unit number of the device being accessed?

5. Which register contains the lower sixteen bits of the address in memory to which the DMAs are to take place?

6. The Word Count register is a Local register.

   A. True

   B. False

SOLUTIONS

1. In the drive
2. Control and Status Register 1
3. Word Count register
4. Control and Status Register 2
5. Bus Address register
6. A. True

Register Control Path

REGISTER CONTROL PATH

INTRODUCTION

In the "Introduction" module, you had a brief look at the register access control path. In the Subsystem Registers module, the concept of "local" and "remote" registers was introduced to you. This module contains a detailed description of the register access control path. In particular, this module describes:

- Register selection
- Writing registers
- Reading registers.

Before the disk or tape drive can transfer data, seek, or move tape, the controller must load the subsystem registers.

As you read through the description, use the supplied block diagram as a reference. Each of the block diagram components has a mnemonic referencing a page in the Field Maintenance Print Set. The mnemonics will help you to correlate the diagram to the print set and illustrate the various register information paths.

OBJECTIVES

- Given the RH Register Control Path block diagram, be able to trace through the following functions:
  - Write to a local register
  - Write to a remote register
  - Read from a local register
  - Read from a remote register
- Given the Massbus Device Selection diagram, be able to specify the register select code and proper jumper configuration for any RH subsystem register.

ADDITIONAL RESOURCES

RJSØ4 Maintenance Manual, Pages 4-1 to 4-3

TJU16 Maintenance Manual, Pages 5-1 to 5-3

RJPØ4 Maintenance Manual, Pages 5-1 to 5-3

RJPØ5/Ø6 Maintenance Manual, Pages 5-1 to 5-3

RWPØ4 Maintenance Manual, Pages 5-1 to 5-5

REGISTER CONTROL

RH11 REGISTER CONTROL PATH

Figure 1 illustrates the RH11 Register Control Path in block diagram form. The upper portion consists of the registers and multiplexers. The lower portion consists of the register selection and control circuitry. The following discusses the selection of the registers and the signals generated to control register transfers.

REGISTER SELECTION

The receivers and associated decode circuitry in the lower left corner of the block diagram, use Unibus address bits 17 through Ø6 to select a register. These bits are compared with the device jumpers by the XOR gates. These jumpers are configured during installation to reflect the base address of the RH Controller Subsystem (i.e., 772Ø4Ø for the RSØ4 and 7767ØØ for the RP's). When there is a favorable comparison, the address logic asserts "DEVice SELected" (DEV SEL) at MSYN time. DEV SEL enables the register select decoder.

NOTE

Address line A5 is jumpered to the ROM if there are more than 16 registers in the subsystem. Otherwise, A5 is jumpered to the XOR gates.

Part of the register select circuitry is a 32 x 8 bit ROM. The ROM uses address bits 5 through 1 as inputs. Table 1 shows the 32 possible output combinations. Output bits Ø, 1, 6 and 7 are routed to the register decoder in order to select any local registers. Bits 4 through Ø are routed to the Massbus for remote register selection.

The direction control circuitry samples AØ, CØ and C1 for direction and byte control. The output is sent to the register decoder.

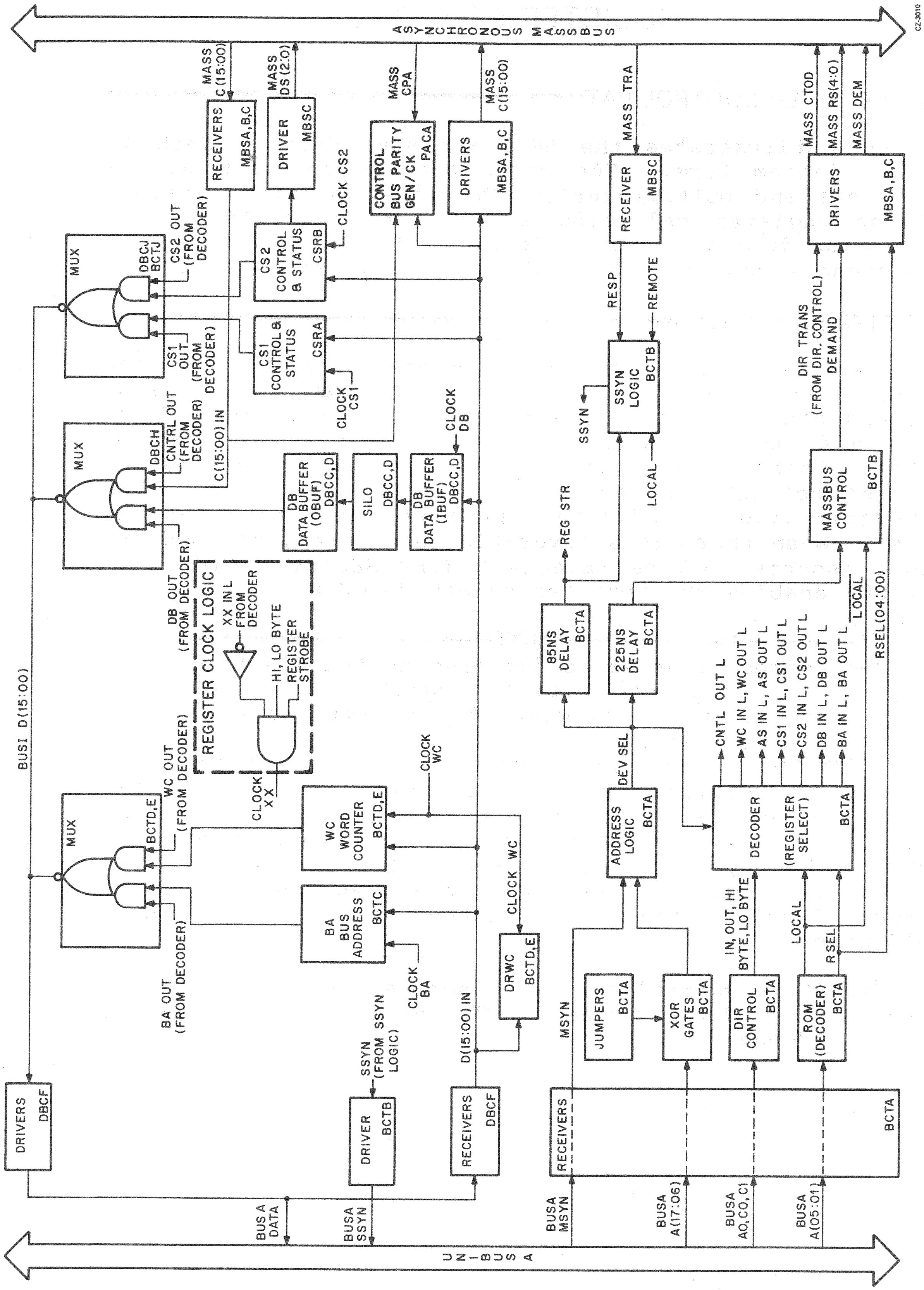


Figure 1 RH11 Register Control Path

A circuit, not shown on Figure 1 but represented in the lower right corner of Figure 2, is the magnitude comparator. It compares address lines 2, 3, 4 and 5 with jumpers representing the maximum number of registers in the subsystem. The output of the comparator logic (Legal Register) allows the RH to access the remote registers. This signal indicates the existance/non-existance of the desired register. If "Legal Register" is false, the signal DEMand (DEM) will not be issued to select the remote register. Without DEM, no SSYN response will be issued in reply to MSYN. This will result in a subsystem Non-Existant Device error. (See Figure 2.)

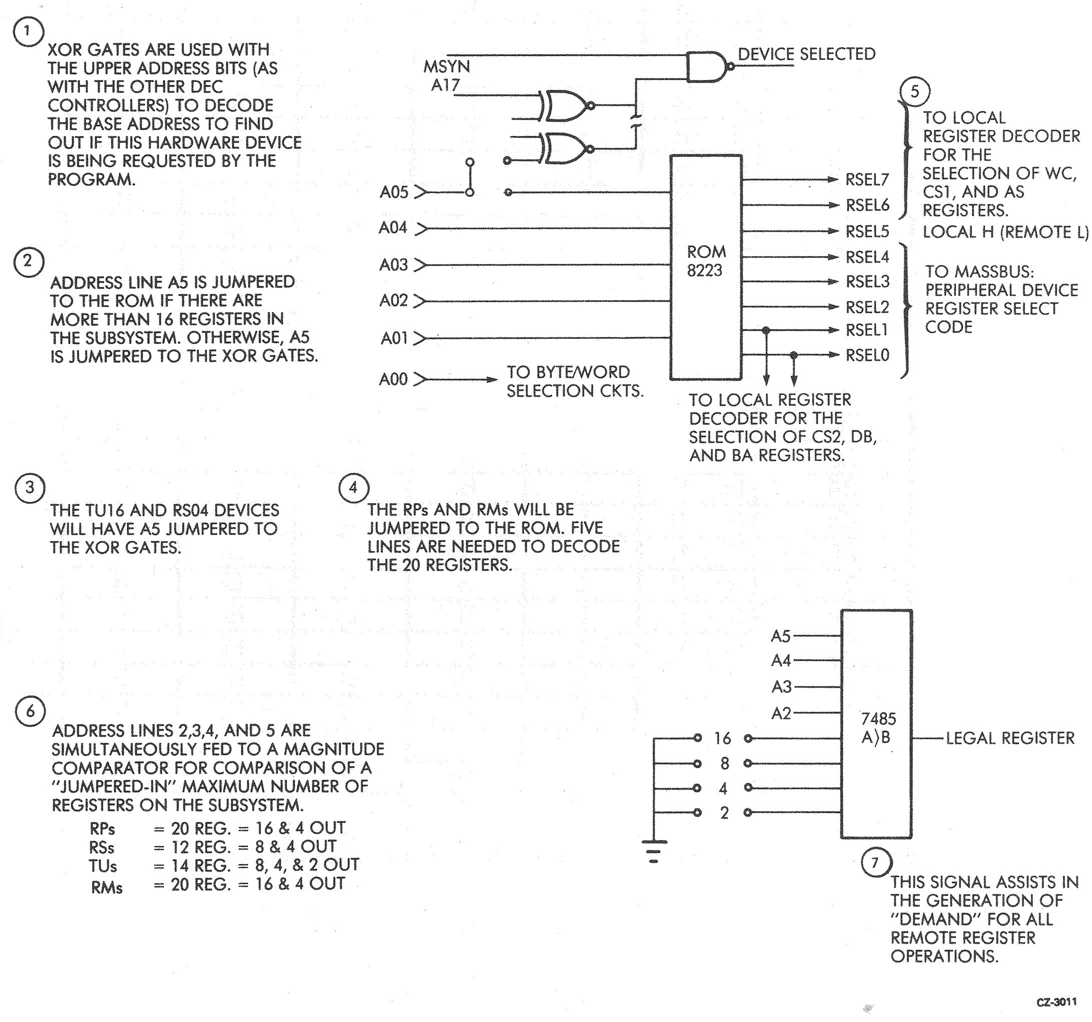


Figure 2 Massbus Device Register Selection

Table 1 Register Selection

INPUT TO ROM FROM ADDRESS LINES A5 TO A1.

REGISTER SELECT PROM - 23Ø4ØA1(8223)								
Octal Address	M7	M6	Local Reg M5	RSEL4 M4	RSEL3 M3	RSEL2 M2	RSEL1 M1	RSELØ MØ
ØØ	L	L	L	L	L	L	L	L
* Ø1	H	L	H	L	L	L	H	H
* Ø2	H	H	H	L	L	L	L	L
Ø3	H	H	L	L	L	H	L	H
* Ø4	H	H	H	L	L	L	H	L
Ø5	H	H	L	L	L	L	L	H
Ø6	H	H	L	L	L	L	H	L
Ø7	L	H	L	L	L	H	L	L
1Ø	H	H	L	L	L	H	H	H
* 11	H	H	H	L	L	L	L	H
12	H	H	L	L	L	L	H	H
13	H	H	L	L	L	H	H	L
14	H	H	L	L	H	L	L	L
15	H	H	L	L	H	L	L	H
16	H	H	L	L	H	L	H	L
17	H	H	L	L	H	L	H	H
2Ø	H	H	L	L	H	H	L	L
21	H	H	L	L	H	H	L	H
22	H	H	L	L	H	H	H	L
23	H	H	L	L	H	H	H	H
24	H	H	L	H	L	L	L	L
25	H	H	L	H	L	L	L	H
26	H	H	L	H	L	L	H	L
27	H	H	L	H	L	L	H	H
3Ø	H	H	L	H	L	H	L	L
31	H	H	L	H	L	H	L	H
32	H	H	L	H	L	H	H	L
33	H	H	L	H	L	H	H	H
34	H	H	L	H	H	L	L	L
35	H	H	L	H	H	L	L	H
36	H	H	L	H	H	L	H	L
37	H	H	L	H	H	L	H	H

* Indicates RH or "Local" Reg. All others are remote. This is indicated by the M5 output.

*Address bit Ø5 may be grounded if there are less than 16 registers in the subsystem.

Table 1 Register Selection (Cont)

REGISTER SELECTED	UNIBUS ADDRESS
RHCS1 MASSBUS (ØØ)	BASE ADDRESS
RHWC	BASE +2
RHBR	BASE +4
MASSBUS (Ø5)	BASE +6
RHCS2	BASE +1Ø
MASSBUS (Ø1)	BASE +12
MASSBUS (Ø2)	BASE +14
MASSBUS (Ø4)	BASE +16
MASSBUS (Ø7)	BASE +2Ø
RHDB	BASE +22
MASSBUS (Ø3)	BASE +24
MASSBUS (Ø6)	BASE +26
MASSBUS (1Ø)	BASE +3Ø
MASSBUS (11)	BASE +32
MASSBUS (12)	BASE +34
MASSBUS (13)	BASE +36
MASSBUS (14)	BASE +4Ø
MASSBUS (15)	BASE +42
MASSBUS (16)	BASE +44
MASSBUS (17)	BASE +46
MASSBUS (2Ø)	BASE +5Ø
MASSBUS (21)	BASE +52
MASSBUS (22)	BASE +54
MASSBUS (23)	BASE +56
MASSBUS (24)	BASE +6Ø
MASSBUS (25)	BASE +62
MASSBUS (26)	BASE +64
MASSBUS (27)	BASE +66
MASSBUS (3Ø)	BASE +7Ø
MASSBUS (31)	BASE +72
MASSBUS (32)	BASE +74
MASSBUS (33)	BASE +76

Table 2   Unibus Addresses for RH11

OCTAL INPUT TO ROM	MASSBUS (RS) ADDRESS	MNEMONIC	RSØ4	TU16	RP's and RM's
ØØ	ØØ	CS1	772Ø4Ø	77244Ø	7767ØØ
Ø1	LOCAL	WC	772Ø42	772442	7767Ø2
Ø2	LOCAL	BA	772Ø44	772444	7767Ø4
Ø3	Ø5	DA(FC FOR TU16)	772Ø46	772446	7767Ø6
Ø4	LOCAL	CS2	772Ø5Ø	77245Ø	77671Ø
Ø5	Ø1	DS	772Ø52	772452	776712
Ø6	Ø2	ER1	772Ø54	772454	776714
Ø7	Ø4	AS	772Ø56	772456	776716
1Ø	Ø7	LA(CK FOR TU16)	772Ø6Ø	77246Ø	77672Ø
11	LOCAL	DB	772Ø62	772462	776722
12	Ø3	MR	772Ø64	772464	776724
13	Ø6	DT	772Ø66	772466	776726
14	1Ø	SN		77247Ø	77673Ø
15	11	OF(TC FOR TU16)		772472	776732
16	12	DC			776734
17	13	CC(HR FOR RMØ2)			776736
2Ø	14	ER2(MR2 FOR RMØ2)			77674Ø
21	15	ER3(ER2 FOR RMØ2)			776742
22	16	EC1			776744
23	17	EC2			776746

The following is an example using Unibus address 772046:

Address 772046 (111 111 010 000 100 110) is the RS04 Desired Disk Address Register. (Table 2 and the "PDP-11 Programming Card" show the different peripheral registers.) Unibus Address bits 5 through 17 are routed to the XOR gates. Unibus Address bits 4 through 1 (0011; see Table 2) are decoded by the ROM with the following outputs as determined by the chart on Table 1.

NOTE

A5 is jumpered to the XOR gates.

MSB
- Local not asserted = Remote
- RSEL4=0
- RSEL3=0
- RSEL2=1 — Register select code 05 (Massbus Address)
- RSEL1=0
- RSEL0=1

LSB

REGISTER WRITES

During decoding, two delays are in the process of timing out. Local register writes will load the appropriate register at the trailing edge of the 85 nanosecond delay. (See example in dotted area on Figure 1.) The data contained within the Unibus data lines is then gated into the register. The output of the delay is ANDed with LOCAL to generate SSYN.

During remote register writes, the following signals will be asserted:

- C(15:00) - Control or status information
- CPA - Parity bit
- DS(2:0) - Device unit number
- Mass CTOD - Translation of Unibus C1 and C0 lines and is called Controller-To-Drive (direction).
- Mass RS(4:0) - Register select.

The second delay is used during these remote register writes. At the end of the 225 nanosecond delay, DEM will strobe the data into the remote register. The device should respond with TRAnsfer (TRA). Upon receipt of TRA, the RH logic produces the Unibus signal SSYN.

REGISTER READS

To accomplish a register read, a like decoding procedure takes place. The exception being that the C1 and CØ lines indicate a Read operation. One of the three MUX's on the block diagram is selected by the register decoder logic. This places the contents of the desired register on the internal bus (BUSI D 15:ØØ). The register contents are then placed on the Unibus by the drivers. SSYN is generated on the trailing edge of the 85 nanosecond delay.

If a remote read is indicated, the RS code of the ROM would be sent on the Massbus along with CTOD, DEVice SELect and finally DEMand. The selected peripheral device accepts this information and replies by gating the register contents onto the Massbus C lines. This information reaches the RH receivers that in turn input the selected MUX. The register information is gated onto the internal bus by the signal CNTRL OUT L. SSYN is generated from TRA being sent by the drive with the information on the C lines. The register information received is also parity checked by the RH.

RH70 DIFFERENCES

The RH7Ø Block Diagram (Figure 3) differs from the RH11 Block Diagram (Figure 1) in that it also has:

- Bus Address Extension (BAE) register (contains bits 16 through 21 of a memory address)
- Control and Status (CS3) register 3 (contains four parity bits, an interrupt enable bit, and five error bits)
- One MUX to handle the additional two registers.

The reading and writing of a local/remote register is the same.

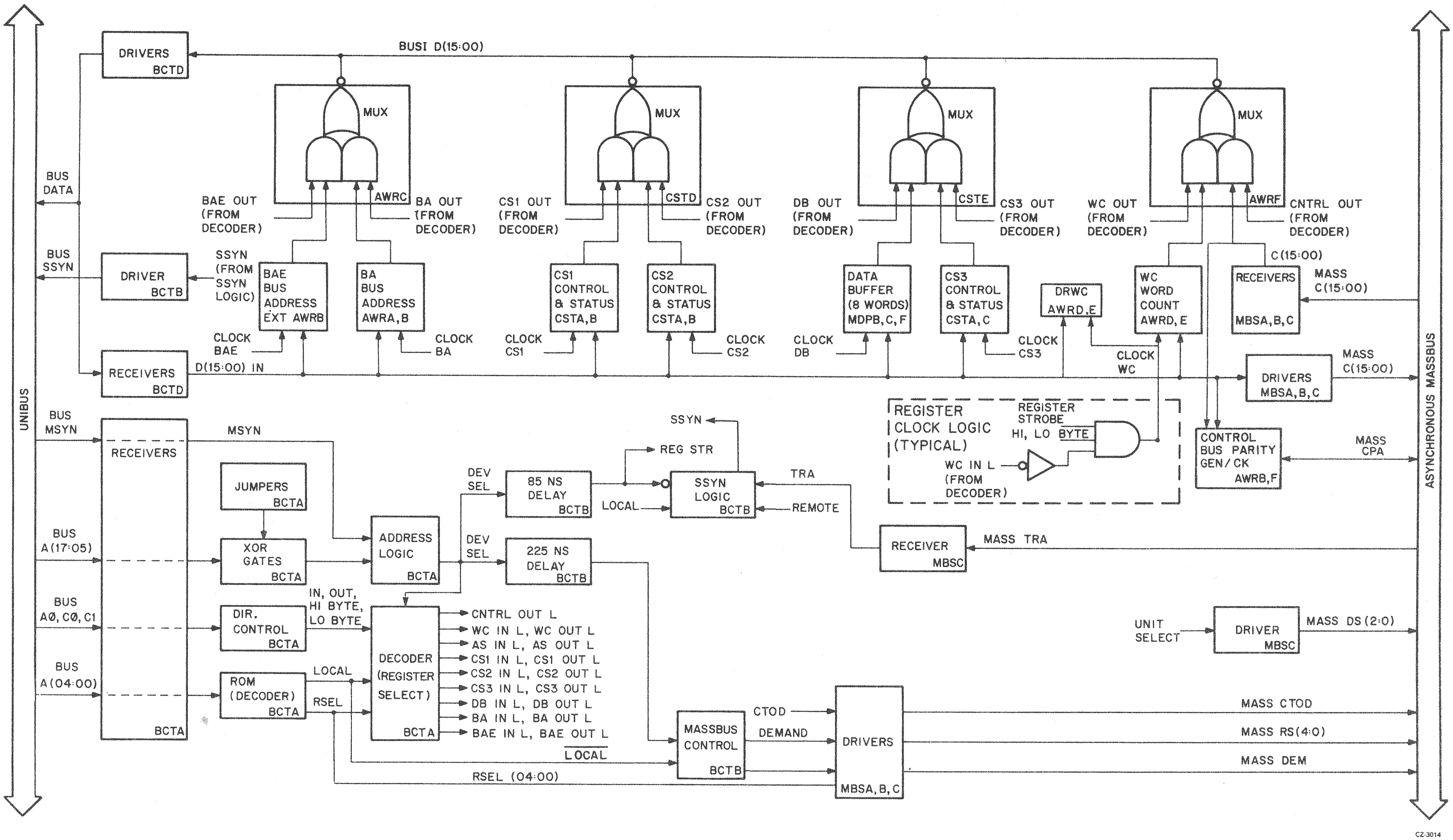


Figure 3 RH70 Register Control Path

SUMMARY

- In performing a local register write, the RH first decodes the address received from the Unibus. From this a device select, direction and register selection is made. After 85 nanoseconds, register strobe is generated, loading the local register, and SSYN is then sent to the Unibus.

- For a remote write the same selection is made and the signals CTOD (direction), RS4:Ø (register select), DS2:Ø (device select), and DEMand are sent on the Massbus along with the data and CPA (parity bit). After the device receives this information it responds with TRA which generates SSYN for the Unibus.

- To read a local register, the address is decoded and the appropriate MUX is qualified, allowing the register to be available to the Unibus. After 85 nanoseconds, SSYN is generated.

- To read a remote register, the address is decoded and DEVice SELect, CTOD, Register Select, and DEMand are sent on the Massbus. The device responds by placing the register contents on the C lines. The proper MUX is qualified by CNTRL OUT from the register control circuit. The device asserts TRA generating SSYN.

EXERCISES

Answer the following questions using any of your reference materials. Discuss any problems you have with another student or your course administrator. The solutions are on the next page.

1. What is the Unibus address for the SN register in the RP04?

2. What is the register select code for the ER1 register in the RS04?

3. Is A5 jumpered to the XOR gates or the ROM for the RP's?

4. Which jumper(s) must be out in the magnitude comparator for the RP04?

5. List the signals that are used on the Massbus for a remote register write.

   A.

   B.

   C.

   D.

   E.

   F.

6. Which signal does the drive assert after the data is on the C lines during a remote register read?

7. During a remote register operation which signal is responsible for the direction the data is to travel?

   A. Demand

   B. SSYN

   C. CTOD

   D. CPA

8. Which signal gates the C lines into the device register?

SOLUTIONS

1. 776730
2. 02
3. ROM
4. 16 and 4
5. A. CTOD

   B. Register Select (RS)

   C. DEMand

   D. C(15:00) Control or Status Information

   E. CPA (parity)

   F. Drive Select (DS)
6. TRA
7. C. CTOD
8. DEMand

Control Bus Interfacing

CONTROL BUS INTERFACING

INTRODUCTION

The Massbus consists of two sections:

- A data bus
- A control bus

These two buses provide the interface between the RH controller and the drives. This module deals only with interfacing on the control bus. Data bus interfacing is covered in a separate module.

This module further defines the Massbus signals described in the Register Control module. The interfacing signals as described in this course are common to all Massbus peripherals. Once you have learned these signals, understanding an individual Massbus peripheral will be easier.

OBJECTIVES

Given a list of Control Bus interfacing signals and their definitions, be able to match the signal with the definition. The signal names are:

- CPA
- TRA
- C Lines
- INIT
- DEM
- DS2:Ø
- CTOD
- RS4:Ø
- Fail
- ATTN

ADDITIONAL RESOURCES

RJSØ4 Maintenance Manual, Paragraph 2.3

TJU16 Maintenance Manual, Paragraph 2.3

RJPØ4 Maintenance Manual, Paragraph 2.3

RJPØ5/Ø6 Maintenance Manual, Paragraph 2.3

RWPØ4 Maintenance Manual, Paragraph 2.3

CONTROL BUS INTERFACING

GENERAL DESCRIPTION

The control bus is that part of the Massbus that is responsible for the transferral of register information between controller and peripheral (Figure 1). Register information consists of status, errors, function codes, and addresses. The control bus consists of:

- 17-bit, (16 bits plus parity) of parallel register information called the "C" lines (C15:00 and CPA)
- 14 control lines

The following paragraphs describe these bits.

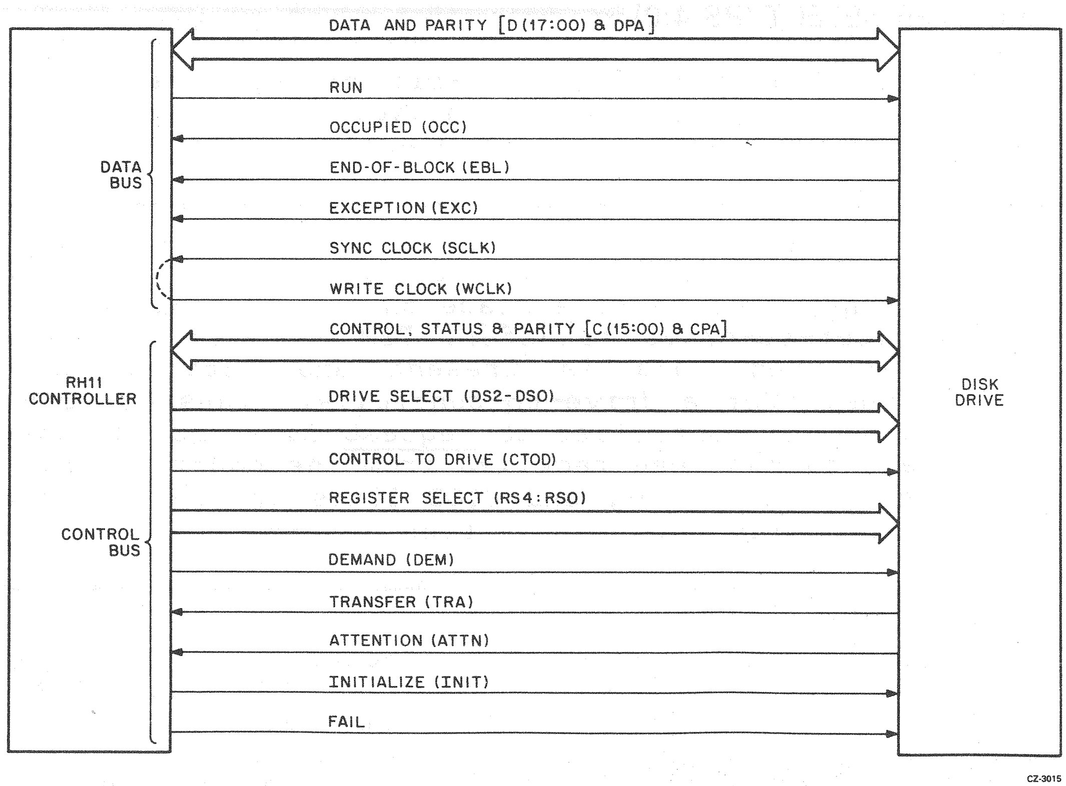


Figure 1 Massbus Interface Lines

DRIVE SELECT (DS 2:0)

These three lines form a binary code representing the unit number of the drive. Since the RH Controller can be cabled to more than one drive, the drive select code selects one of the eight possible drives. This is necessary to establish communication between the controller and the desired Massbus peripheral.

CONTROLLER-TO-DRIVE (CTOD)

Because the Massbus is bidirectional, the signal CTOD is used to indicate the direction of information transferral. Controller-to-Drive is developed from C1 and C0 (the direction signals from the Unibus). CTOD is asserted if the software is requesting to load a remote register. If status information is being requested from a Massbus peripheral, CTOD is negated.

REGISTER SELECT (RS 4:0)

These five lines transmit a 5-bit binary code from the controller to the selected drive. The binary code selects one of the Massbus peripherals.

DEMAND (DEM)

This signal is asserted by the controller to indicate that a transfer is to take place on the control bus. For a controller-to-drive transfer, DEM is asserted by the controller when data is present and settled on the control bus. For a drive-to-controller transfer, DEM is asserted by the controller to request data and is negated when the data has been received from the control bus. In both cases, the RS, DS, and CTOD lines are generated and allowed to settle before assertion of DEM.

TRANSFER (TRA)

This signal is asserted by the selected drive in response to DEM. For a controller-to-drive transfer, TRA is asserted after the data has been strobed and is negated after DEM is negated. For a drive-to-controller transfer, TRA is asserted after the data has been gated onto the bus and negated after DEM is dropped.

REMOTE REGISTER WRITE TIMING

Figure 2 illustrates the timing on the Massbus during a remote register write.

The RH Controller sends DS, RS, CTOD and the information to be loaded into the register on the C lines. After a short deskewing delay, DEM is asserted telling the device: "The data is there, load it". The device responds with TRA to inform the RH that it has accepted the information.

> **NOTE**
>
> There is an error timer in the controller waiting for the TRA response. If TRA is not received within its limits, the controller assumes the Massbus peripheral is not present and asserts the error Non-Existant Drive (NED).

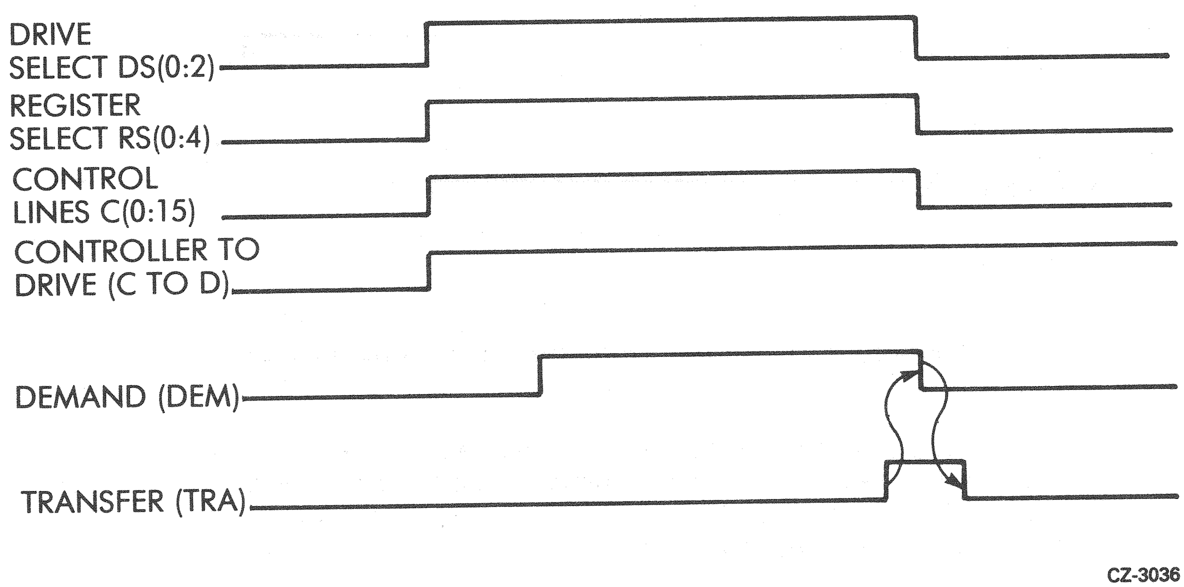


Figure 2 Remote Register Write Timing Diagram

REMOTE REGISTER READ TIMING

Figure 3 illustrates the timing on the Massbus during a remote register read.

The RH controller asserts DS, RS, CTOD and allows a short period of time for unit number selection and register selection decoding before asserting DEM. DEMand now acts as a request for a transfer. If the unit number agrees, the device accesses the desired register and places the contents on the Massbus C lines. TRA is then asserted by the device, indicating the register information is on the Massbus.

As described above, the NED timer is waiting for the TRA response from the device.

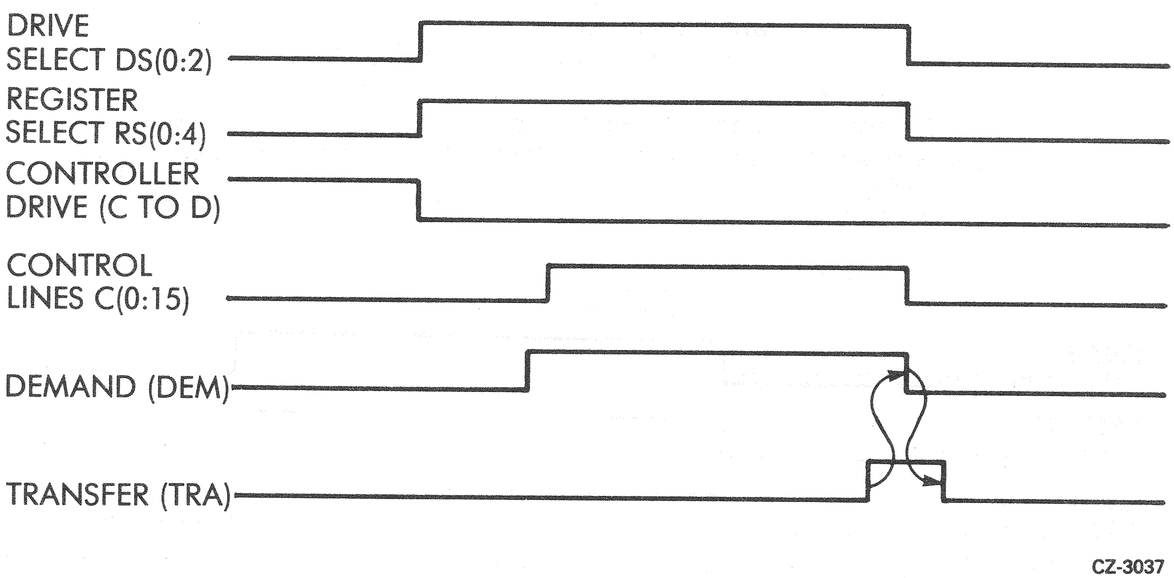


Figure 3 Remote Register Read Timing Diagram

This completes the discussion of all that is required to communicate register information to/from a Massbus device and the RH controller. There are, however, three more signals on the control bus.

INITIALIZE (INIT)

This signal is asserted by the controller to perform a system reset of all the Massbus peripherals. It is asserted when a 1 is written into the CLR bit (bit Ø5 of CS2) or when Unibus INIT is asserted on the Unibus. When a peripheral device receives the INIT pulse, it immediately aborts the execution of any current command and performs all actions described for the Drive Clear command.

FAIL

When asserted, this signal indicates that a power-fail condition has occurred in the controller. While FAIL is asserted, the drive inhibits reception of the INIT and DEM signals at the drive.

ATTENTION (ATTN)

The ATTN line is a shared line which connects all drives in common to the RH controller. Each drive asserts ATTN (and sets its own ATA bit) whenever it has an error condition or has finished executing a noncontroller function (i.e., Seek or rewind). Assertion of ATTN sets Special Condition (bit 15 of CS1). Setting this bit causes an interrupt to the CPU. The software knows which controller caused the interrupt, but not which drive. The software then moves the contents of the attention summary register into memory in order to check which drive raised the interrupt.

SUMMARY

The control bus is that portion of the Massbus Interfacing System that is responsible for transferring register information between the drive and the RH controller. It consists of:

- C Lines - Register information
- Drive Select - Establishes communications between controller and peripheral
- CPA - Parity bit
- Register Select - Selects one of the Massbus peripheral registers
- Controller-to-Drive - Direction of transfer
- Demand - Indicates to the drive that data is present and settled on the control bus during a register write. Also, requests data from drive during a register read
- Transfer - Reply to Demand
- Initialize - Clears the drives
- Fail - Indicates power-fail condition in the controller
- Attention - Indicates an error or change in status in the drive

EXERCISES

Answer the following questions using any of your reference materials. Discuss any problems you have with another student or your course administrator. The solutions are on the next page.

1. Which signal on the Massbus indicates that a transfer is to take place on the control bus?

2. Which signal on the control bus indicates the direction of the transfer?

3. Which signal on the control bus indicates that the transfer is complete?

4. Before generating DEMand, which control signals does the RH place on the Massbus for a remote register write?

   A.

   B.

   C.

   D.

5. The DS2:0 control signals select the proper register in the device.

   A. True

   B. False

6. Which signal on the Massbus clears the drive?

7. Which signal is generated when a drive has a change in status to report?

8. Which signal is asserted if the power should drop to the controller?

SOLUTIONS

1. Demand (DEM)

2. Control-to-Drive (CTOD)

3. Transfer (TRA)

4 A. Device Select (DS2:Ø)

   B. Register Select (RS4:Ø)

   C. CTOD

   D. Register information and Parity (C15:Ø and CPA)

5. B. False

6. Initialize (INIT)

7. Attention (ATTN)

8. Fail

EDUCATIONAL SERVICES