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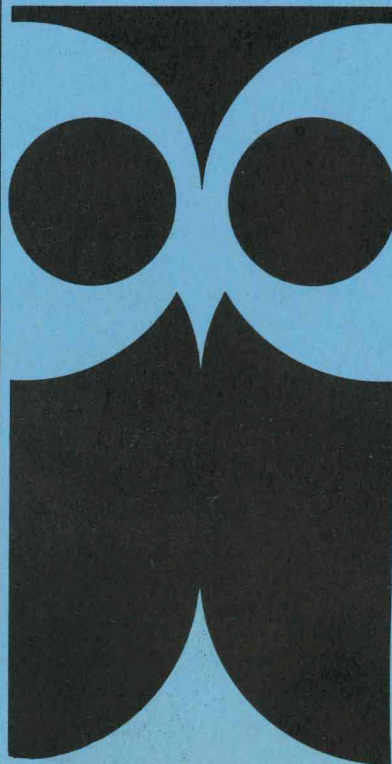
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PDP-11/44

SYSTEM USER'S GUIDE

**Training  
Center  
Munich**



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# PDP-11/44

## System User's Guide

Preliminary, May 1980

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## PREFACE

The PDP-11/44 is a midrange computer system which is available in a standard configuration and can be expanded by the user to conform to specific user requirements.

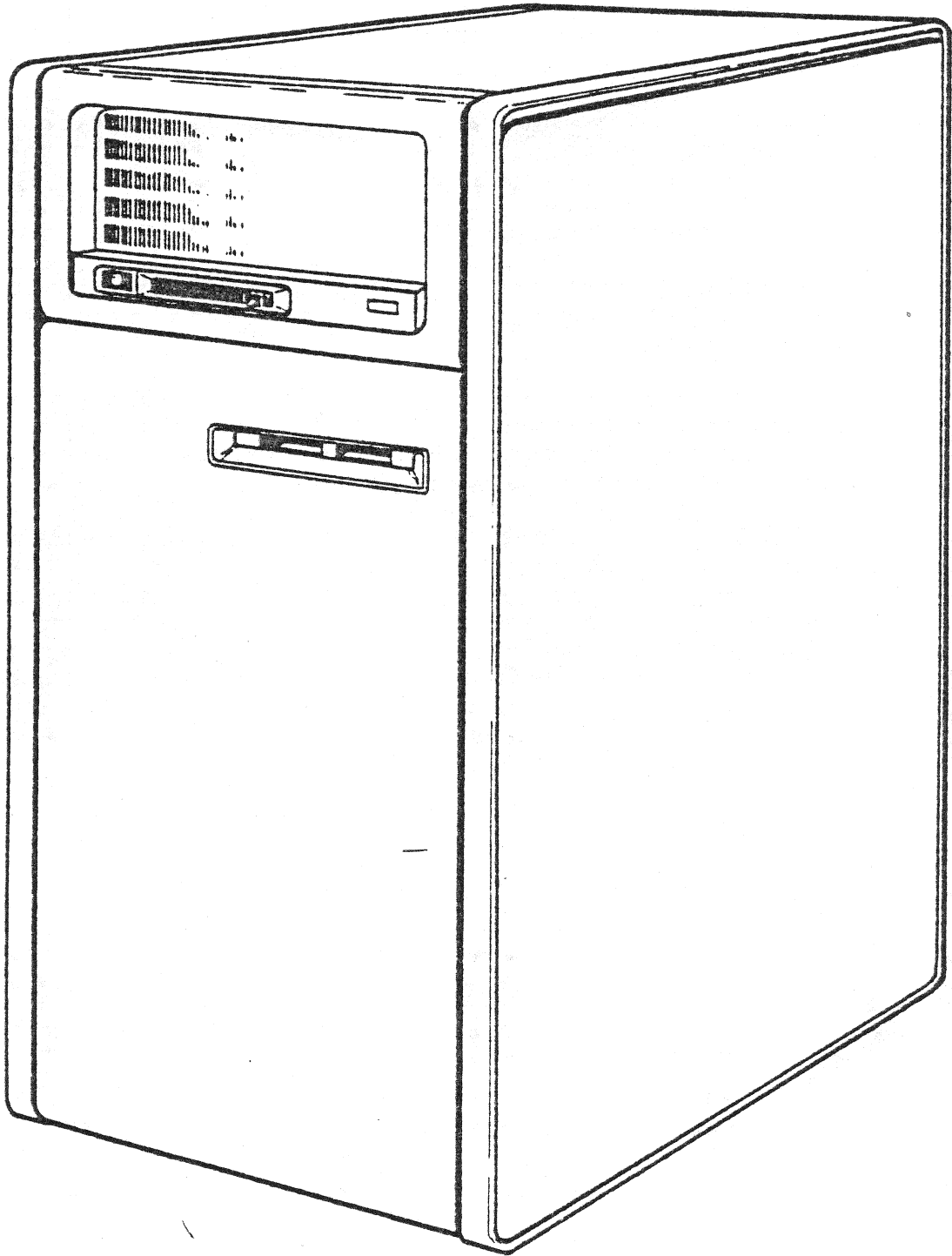
This guide defines the standard system and provides the information required to unpack, install the system in a cabinet and wire the system for operation.

Chapter 1 Introduction - Includes a general description of the PDP-11/44 system and the modules which are supplied with the unit. Also included are the features and capability of the system the options that are available, and the equipment specifications, which include the power supply.

Chapter 2 Operation - Contains a description of the front panel controls and indicators, the console commands available and register bit assignments.

Chapter 3 Configuration - Provides the module placement information in the processor backplane, and the jumper lead information required to configure the modules for specific requirements.

Chapter 4 Installation - Includes the information necessary to connect the unit to ac power, to mount the unit into a PDP-11/44 systems cabinet or standard 48.26 cm (19 inch) cabinet. It also includes the removal and replacement procedures for the power supply assembly and fan assembly. Information is also included to allow the user to install additional backplanes for expansion of the system functions.



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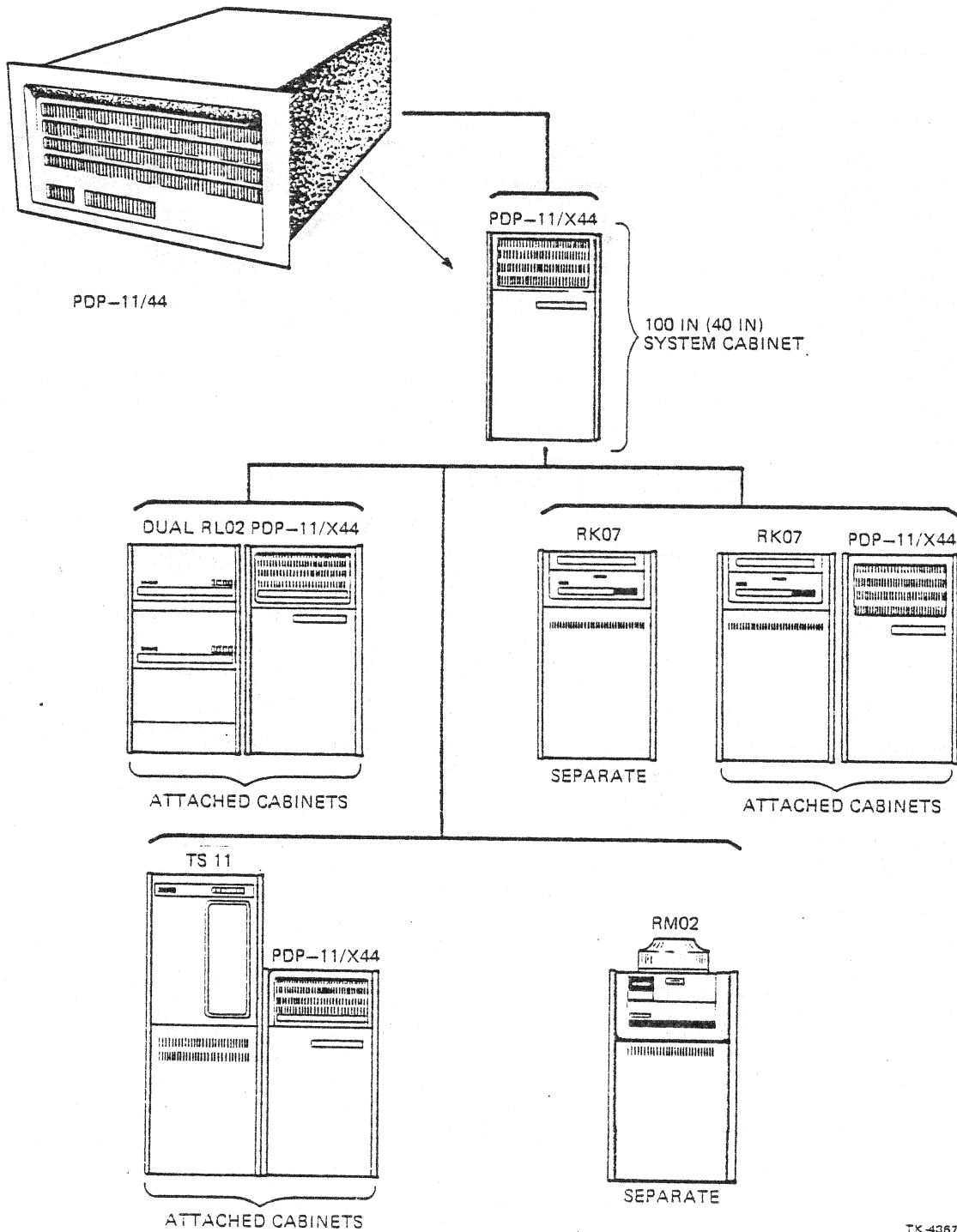
## CHAPTER I INTRODUCTION

This guide provides the information required to unpack the PDP-11/44 and PDP-11/X44 processor units, to install the units at their operating location and to configure the system for operation.

The PDP-11/44 processor consists of CPU modules, memory modules and interface modules enclosed in the BALL-AA or BALL-AB mounting box. The box also includes a front control panel and power supply. The mounting box can be installed in a standard 48.26 cm (19 inch) rack or cabinet or into a DIGITAL system cabinet.

The PDP-11/X44 processor consists of the PDP-11/44 processor mounted into the 100 cm (40 inch) low profile, top loading H9642 cabinet. This cabinet conforms in style to other DIGITAL PDP-11 peripheral unit cabinets.

Figure 1-1 shows several typical PDP-11/X44 system configurations that include disk drive units and magnetic tape units. The PDP-11/X44 cabinet attaches to the RL02 and RK07 disk drive units and to the TS11 magnetic tape unit.



TK-4367

Figure 1-1 PDP-11/44 System Configurations

## 1.1 GENERAL

The PDP-11/44 and the PDP-11/X44 are medium-range, general-purpose computer systems which operate with 16-bit data words and provide 22 bits for memory addressing. A total of one mega byte of main memory can be included with the system in increments of 256K bytes. The system includes the complete instruction set of the PDP-11/70 processor except for FD MAINT INST instruction. Two additional instructions, Move From Processor Type (MFPT) and Call to Supervisor Mode (CSM), are included.

The systems also include an 8K byte cache memory and the extended instruction set (EIS). A microprocessor is used to interpret the ASCII codes from the console terminal and allows the functions previously performed at the console switches to be initiated at the console terminal.

Available as an option with the system is a floating-point processor and a commercial instruction set processor.

The PDP-11/X44 system includes a dual TU58 cartridge tape transport used to load diagnostic programs and to update software. The following operating software systems are compatible with the PDP-11/44 and PDP-11/X44 systems.

Software	Version
RT-11	V4.0
RSX-11M	V3.2
RSX-11S	V2.2
RSX-11M+	V1.0
RSTS/E	V7.0
CTS-500	V5.0
DSM-11	V2.0
TRAX	V2.0
COBOL-11	V4B
MACRO-11	V4.0

## 1.2 EQUIPMENT DESCRIPTION

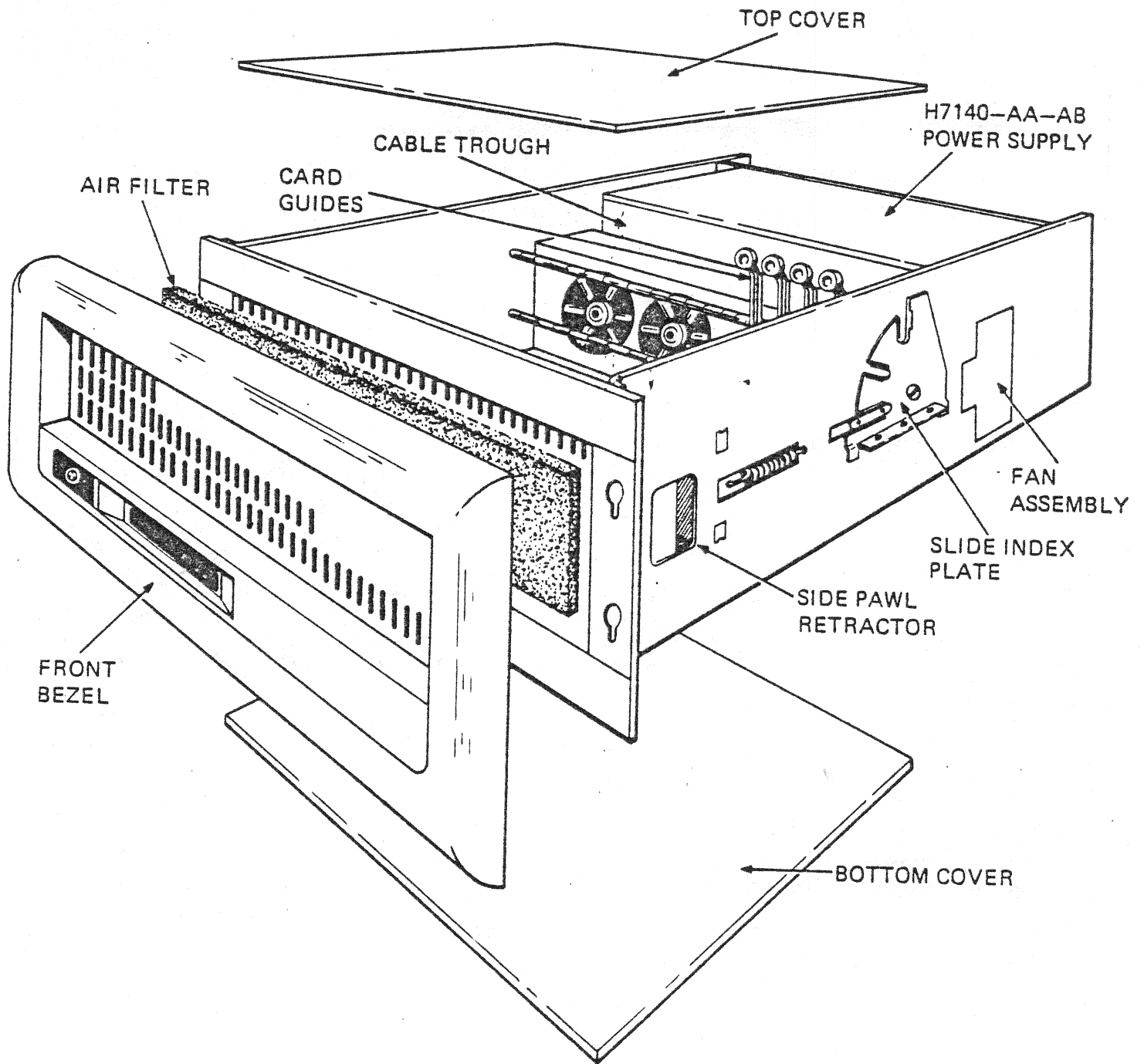
The PDP-11/44 and PDP-11/X44 processor systems are available to operate with either 120 Vac or 240 Vac output power. Table 1-1 lists and describes the components included with each system.

Table 1-1 Processor System Designations

Designation	Description
PDP-11/44-CA	Contains a CPU, 256 K bytes of ECC MOS memory, two EIA serial line unit, two serial line units, one for the console terminal and one for the TU58 tape transport (not included), BA11-AA mounting box with cabinet, mounting slides and a filter distribution panel. Operates with 120 VAC input power.
PDP-11/44-CB	Same as PDP-11/44-CA except the mounting box is a BA11-AB wired for 240 Vac input power.
PDP-11/X44-CA	Same as PDP-11/44-CA except the BA11-AA mounting box is installed in an H9642 system cabinet which includes a dual TU58 tape drive and power control unit for 120 Vac input power.
PDP-11/X44-CB	Same as PDP-11/X44 -CA except wired for 240 Vac input power.

### 1.2.1 PDP-11/44-CA, -CB Processor System

The PDP-11/44-CA, -CB processors are supplied in the BA11-AA, -AB mounting box shown in Figure 1-2. The mounting box contains a 14 slot (column) backplane assembly with the system modules installed, a fan assembly and an H7140-AA, -AB power supply assembly. The fan assembly contains three fans and provides cooling for the modules and power supply. The fans are mounted on a slide, for ease of removal, and are powered by the power supply. A front bezel is attached to the front of the mounting box and contains a control panel and ventilating slots to allow the circulation of air. An open cell, foam filter is located directly behind the front bezel and may be easily removed for cleaning.



TK-4368

Figure 1-2 PDP-11/44-CA, -CB in Mounting Box

A control panel, located on the lower section of the front bezel, contains a keyswitch, panel switch and indicators to select and indicate operating conditions. A removable top and bottom cover is also supplied with the mounting box.

Attached to each side of the mounting box is a slide index plate which allows the unit to be rotated to a vertical position when the unit is mounted in a cabinet onto the slides that are provided with the unit. The slide index plates are released by the side pawl retractors also located on each side of the unit, toward the front.

The BALL-AA, -AB box provides a 9 slot CPU backplane and 29 card guides at the front and rear of the unit to allow additional modules to be installed. One DD11-DK 9-slot double system unit and one DD11-K single system unit or three DD11-CK single system units may be added and installed and connected directly to the power supply by the cables and connectors attached to the system units. These system units provide additional mounting space for I/O device options.

#### 1.2.2 PDP-11/X44 Processor System

The PDP-11/X44-CA, -CB consists of the components described for the PDP-11/44-CA, -CB which are mounted in a systems cabinet as shown on the frontispiece. Mounted below the front bezel is a dual TU58 tape transport assembly which enables the loading of diagnostic programs from cassettes and provides data storage for up to 256 K bytes of information.

The BALL-AA, -AB mounting box is attached to the top of the cabinet and can be released and tilted vertically for servicing. When tilted, the mounting box is supported by two gas springs. A hinged panel is provided at the front and the rear of the cabinet to allow access to the power controller unit provided with the cabinet, to the battery backup unit which is supplied as an option, and to the I/O corrector panel.

#### 1.2.3 Standard Hardware Components

Table 1-2 lists the standard hardware supplied with each PDP-11/44 system.

Table 1-2 PDP-11/44 Standard Hardware Components

Quantity	Description
1	KD11-Z Central Processor consisting of: <ul style="list-style-type: none"> <li>a. (M7090) Console Interface Module</li> <li>b. (M7094) Data Path Module</li> <li>c. (M7095) Control Module</li> <li>d. (M7096) Multi-Function Module</li> <li>e. (M7098) Unibus Interface Module</li> </ul>
1	MS11-MB ECC MOS Memory (256K bytes)
1	8K byte cache memory on hex-height module (M7097).
1	BA11-AA (120 Vac) or BA11-AB (240 Vac) Mounting Box with Power Supply and DD11-DK Backplane (70-16502)
1	M9302 Unibus Terminator Module
1	M9642 Cabinet (PDP-11/X44-CA, -CB only)
1	TU58 Dual Tape Drive (PDP-11/X44-CA, -CB only)
1	872-D Power Controller Unit (PDP-11/X44-CA, -CB only)
1	I/O Connector Panel

#### 1.2.4 Hardware Options

The standard PDP-11/44 system capabilities can be expanded with the installation of several available hardware options which are listed in Table 1-3.

Table 1-3 Hardware Options

Designation	Description
MS11-MB	256K bytes ECC memory on hex-height module
MS11-MC	Same as MS11-MB except 512K bytes on two hex-height modules.
MS11-MD	Same as MS11-MB except 758K bytes
FP11-F	Floating-point processor on hex-height module (M7093)
KE44-A	Commercial instruction set processor on a quad-height module (M7091) and hex-height module (M7092).
H7750-BA	Battery backup unit 120 VAC/60 Hz, 240 Vac/50 Hz
H7750-BD	Same as H7750-BA except for 240 Vac/50 Hz
TU58-CA	Dual cassette tape transport.
BA11-AE, -AF	Expander box for PDP-11/44 system expansion, includes power supply

### 1.3 EQUIPMENT SPECIFICATIONS

The following paragraphs contain the mechanical-environmental specifications for the PDP-11/44 and PDP-11/X44 equipment. Detailed specifications for the peripheral devices supplied with these units are contained in the user guide associated with the device.

#### 1.3.1 PDP-11/44 System Specifications

Table 1-4 lists the equipment specifications for the basic PDP-11/44 unit. When the system is operated with a TU58 DECTape II option, the specifications will be similar to those listed on Table 1-5 for the PDP-11/X44 system.

Table 1-4 PDP-11/44-CA, -CB Equipment Specifications

Characteristics	Description
Mechanical	
Overall dimensions (with front bezel)	70.15 cm (27.62 in) length X 48.26 cm (19.0 in) width X 26.34 cm (10.37 in) height
Weight	
Unpackaged	32.66 kg (72.0 lbs)
Packaged	TBS
*Environmental	
Temperature Operating	+5°C (41°F) to +50°C (122°F)
Nonoperating	-40°C (-40°F) to +66°C (151°F)
Humidity Operating	10 to 95% relative (RH) with a maximum wet bulb of 32°C (90°F) and a minimum dew point of +2° (36°F)
Nonoperating	50% relative (RH) or less to 95% (RH) or less with a maximum wet bulb of +46°C (115°F)

Table 1-4 PDP-11/44-CA, -CB Equipment Specifications (Cont)

Characteristics	Description
<u>Vibration</u>	
Operating	5 to 22 Hz: 0.01 inch DA; 22 to 500 Hz: 0.25 Gpk. Sweep Rate of 1.0 octave per minute. All three axes.
Nonoperating (PDP-11/44 pack- aged for shipment)	Vertical Axis Random Vibration: 1.4 Grms overall from 10 to 300 Hz; duration: 1 hr. Longitudinal & Lateral Axis Random Vibration: 0.68 Grms overall from 10 to 200 Hz; duration: 1 hr. each.
<u>Altitude</u>	
Operating	0 to 2.4 Km (8000 ft.)
Nonoperating	9.1 Km (30000 ft.)
<u>Shock</u>	
Operating	10 Gpk for 10+3 ms, 1/2 sine wave, vertical axis only.
Nonoperating	Flat drop for a 6" height, 3 drops total (vertical direction only).

\*The operating temperature and humidity for PDP-11/44 systems which include magnetic tape units, disk units or card readers is the same as defined in Table 1-5 for the PDP-11/X44 system.

### 1.3.2 PDP-11/X44 System Specifications

Table 1-5 lists the equipment specifications for the PDP-11/X44 system including the TU58.

Table 1-5 PDP-11/X44-CA, -CB Equipment Specifications

Characteristics	Description
<b>Mechanical</b>	
Cabinet dimensions	76.2 cm (30.0 in) length X 54.29 cm (21.38 in) width X 100.33 cm (39.5 in) height (not including leveling feet)
<b>Weight</b>	
Unpackaged	140.6 kg (310 lbs)
Packaged	TBS
<b>Environmental</b>	
<b>Temperature</b>	
Operating	+10°C (50°F) to +40°C (104°F)
Non-operating	-40°C (-40°F) to +66°C (151°F)
<b>Humidity</b>	
Operating	10 to 90% relative (RH) with a maximum wet bulb of 28°C (82°F) and a minimum dew point of +2°C (36°F)
Non-operating	50% relative (RH) or less to 95% (RH) or less with a maximum wet bulb of +46°C (115°F)
<b><u>Vibration</u></b>	
Operating	5 to 22 Hz: 0.01 inch DA; 22 to 500 Hz: 0.25 Gpk. Sweep rate of 1.0 octave per minute. All three axes.
Non-operating (PDP-11X44 packaged for shipment)	Vertical Axis Random Vibration: 1.4 Grms overall from 10 to 300 Hz; duration: 1 hr. Longitudinal & Lateral Axis Random Vibration: 0.68 Grms overall from 10 to 200 Hz; duration: 1 hr. each.
<b><u>Altitude</u></b>	
Operating	0 to 2.4 Km (8000 ft.)
Non-operating	9.1 Km (30000 ft.)

Table 1-5 PDP-11/X44-CA, -CB Equipment Specifications (Cont)

Characteristics	Description
<u>Shock</u>	
Operating	10 Gpk for 10+3 ms, 1/2 sine wave, vertical axis only.
Non-operating	Flat drop from a 6" height, 3 drops total (vertical direction only).

1.3.3 H7140-AA, -AB Power Supply Electrical Specifications  
 Table 1-6 lists the electrical specifications of the H7140-AA, -AB power supplies.

Table 1-6 H7140-AA, -AB Power Supply Specifications

Characteristics	Description
Power supply	
H7140-AA	
Line voltage	90 Vrms - 128 Vrms, single phase, two wire and ground (120 Vrms nominal)
Frequency	47-63 Hz
Current (ac)	15 A (rms) max. at 120 Vac 55 A (peak) max. at 120 Vac
Power factor	Greater than 0.60 at full output load and low input voltage (90V)
Inrush current	65 amperes peak at 128 Vrms for 1/2 cycle, followed by repetitive peaks of decreasing amplitude for an additional 8 cycles of the input voltage
Power	1350 W with maximum load applied at nominal voltage output
Overvoltage condition	Can withstand input overvoltage of 150 Vrms for one second
Noise transient	
Low energy transients	300 V peak voltage spike* containing not more than 0.2 watt-seconds of energy per spike
High energy transients	1 KV peak voltage spike* containing not more than 2.5 watt-seconds of energy per spike
Conducted noise	CW-10 KHz to 30 MHz, 3 Vrms
Radiated noise	RF field strength - 10 KHz to 30 MHz, 1 V/M 30 MHz to 1 GHz, 10 V/m

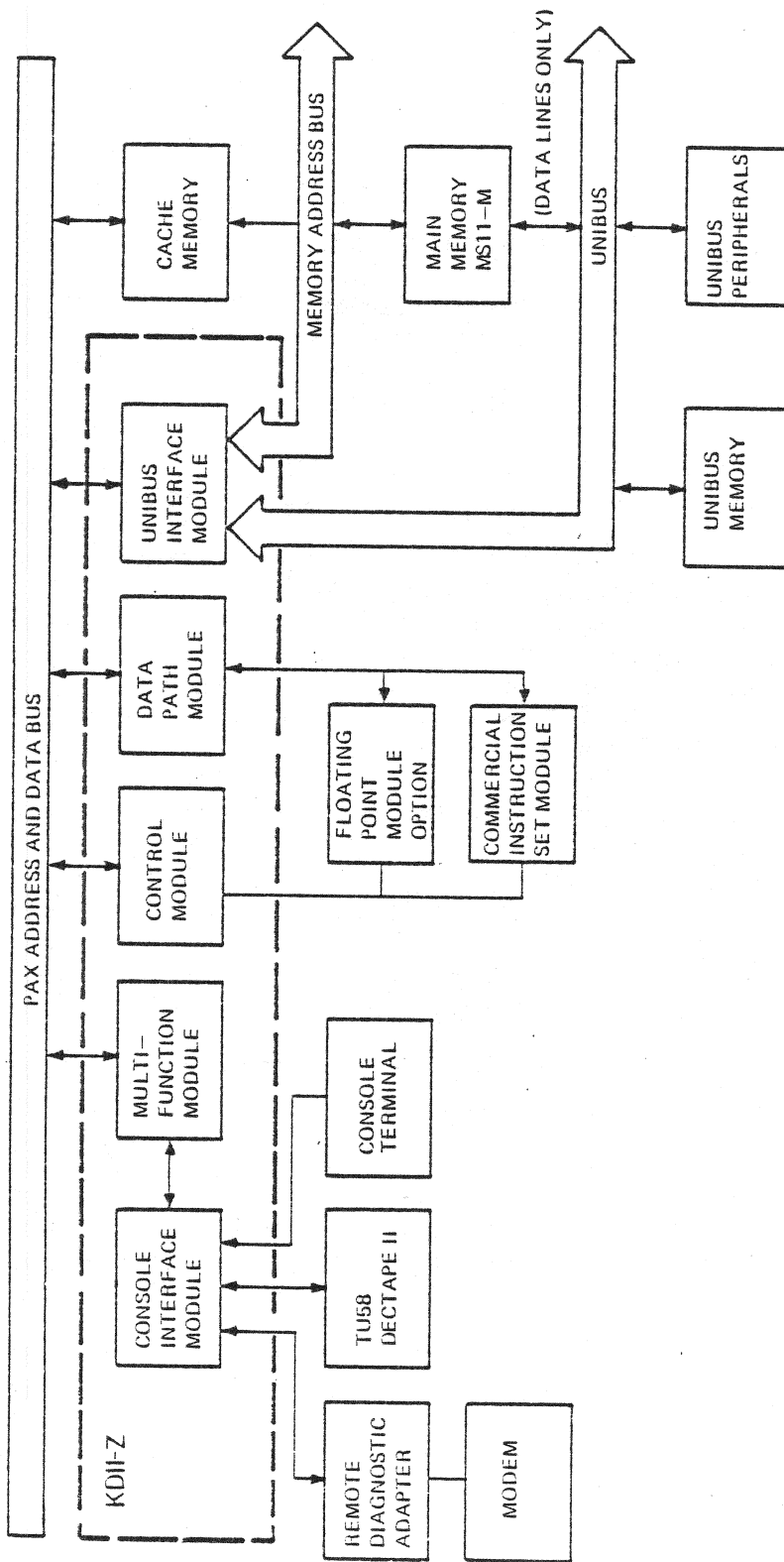
Table 1-6 H7140-AA, -AB Power Supply specifications (Cont)

Characteristics	Description
H7140-BB	
Line voltage	180 Vrms - 256 Vrms, single phase, two wire and ground (240 Vrms nominal)
Frequency	47-63 Hz
Current (ac)	9.0 A (rms) max. at 240 Vac 33 A (peak) max. at 240 Vac
Power factor	Greater than 0.60 at full output load and low input voltage (180V)
Inrush current	130 amperes peak at 256 Vrms for 1/2 cycle, followed by repetitive peaks of decreasing amplitude for an additional 8 cycles of the input voltage
Power	1350 W with maximum load applied at nominal voltage output
Overvoltage condition	Input overvoltage of 300 Vrms for one second
Noise transient	
Low energy transients	300 V peak voltage spike* containing not more than 0.2 watt-seconds of energy per spike
High energy transients	1 KV peak voltage spike* containing not more than 2.5 watt-seconds of energy per spike
Conducted noise	CW - 10 KHz to 300 MHz, 3 Vrms
Radiated noise	RF field strength - 10 KHz to 30 MHz, 1 V/M 30 MHz to 1 GHz, 10 V/M

\*A spike is a voltage transient, of either polarity and of either common or differential mode, with a rise time (10% to 90%) of 0.1 microseconds or less, and a fall time (to 10%) of 10 microseconds or more. The average power of spikes should not exceed 0.5 watt.

#### 1.4 SYSTEM DESCRIPTION

Figure 1-2 is a block diagram of a typical PDP-11/44 system which consists of a console terminal, modem, TU58 DECTape II unit and selected options. The PDP-11/44 processor incorporates the complete instruction set used in the PDP-11/70 processor series and two additional instructions, MFPT and CSM.



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Figure 1-3 Typical PDP-11/44 System and Selected Options

The main memory of the PDP-11/44 (MS11-L) is addressed by a 22-bit physical address bus (PAX) which provides the ability to access over 4 million bytes. In addition, the PDP-11/44 enables memory to be placed on the UNIBUS. This memory resides in the top 124K words of physical address space. The processor can perform transfers to and from the UNIBUS memory independently of main memory transfers. DMA devices making a reference to an address allocated to Unibus memory will never access main memory and, therefore, such transfers are not cached.

The PDP-11/44 includes a cache memory which is a high-speed memory that buffers words between the processor and main memory. The cache stores those memory locations that will most likely be accessed by the executing program. The program can be executed quickly by accessing the high-speed cache and must slow down only occasionally for main memory operations.

The memory management system of the PDP-11/44 provides the address relocation and memory protection facilities required in a multiprogramming system. This system enables several user programs to be located simultaneously in memory. Memory management includes three mapping schemes: 16-bit, 18-bit, or 22-bit. Mapping converts the 16-bit, processor-generated virtual address to a physical address. A separate mapping scheme, the UNIBUS map, converts 18-bit UNIBUS addresses to 22-bit memory addresses. This allows devices on the UNIBUS to communicate with main memory via Non-Processor Requests (NPRs).

The memory management system permits instructions or pure code to be mapped into physical memory separately from data. When this feature is enabled, instructions, index values and immediate operands are mapped through instruction (I) space. Data, or words that can be modified, are mapped through data (D) space. The I/D space facility is enabled under software control. When it is disabled, all memory references are mapped through I space.

The internal communication of the PDP-11/44 processor (KD11-Z) is through a 16-bit data bus and a 22-bit PAX bus. Communication between the processor and main memory is through the extended Unibus (EUB) and the data lines of the UNIBUS. The UNIBUS provides the path for transfers between the processor and its associated main memory, the peripherals, or the memory on the UNIBUS. The UNIBUS interface module (UBI) controls the information transfers to and from the PAX Bus, the EUB and the UNIBUS.

The multifunction module (MFM) consists of an 8085 microprocessor and the logic necessary to enable the execution of the console command set in the CPU. The 8085 software contains diagnostic programs to test logic and data paths.

In addition to the standard features of the PDP-11/44, the Commercial Instruction Set Processor (CISP) and Floating-Point Processor (FPP) can be installed in dedicated slots of the backplane.

The following paragraphs provide a brief description of each of the standard and optional components of the PDP-11/44 system.

#### 1.4.1 KD11-Z Central Processor

The KD11-Z central processor is comprised of four hex-height modules (M7094, M7095, M7096 and M7098) and one double-height module (M7090). The following provides a brief description of each.

1.4.1.1 Data Path Module (M7094) - The data path module contains the data path logic and the memory management logic. The data path performs arithmetic and logic processing, shifting of 8, 16, and 32-bit data formats, byte swapping and sign extension of data, storage of general register data, and storage of status information. Data comes from or goes to the CIS and floating-point options via the AMUX bus of the data path. The memory management section of this module performs address relocation and contains several of the memory management registers.

1.4.1.2 Control Module (M7095) - The control module contains the control store PROMs and associated logic required to decode and execute PDP-11 instructions. It also contains the system clock, power-fail/autorestart logic, boot control logic and trap handling logic.

1.4.1.3 Multifunction Module (M7096) - The multifunction module (MFM) contains an 8085 microprocessor, two serial line ports, a line clock and related logic. The microprocessor allows the system terminal to be used as a programmer's console. The 8085 software routines enable the execution of the console commands discussed in Chapter 2. The serial line port used for the system terminal also serves as a remote diagnosis serial port. The second serial line port of the MFM supports a TU58 tape drive or can be used with other serial line devices.

1.4.1.4 UNIBUS Interface Module (M7098) - The UNIBUS interface module (UBI) provides the logic which enables the processor to access the UNIBUS. It also includes bus arbitration logic for interrupts and NPRs, the boot circuits which allow booting of up to four devices, and buffers for the PAX data lines to and from the processor. The UNIBUS map contained on the module allows direct-memory-access (DMA) transfers between main memory and peripherals on the UNIBUS. The UBI also controls the operations of the EUB.

1.4.1.5 Console Interface Module (M7090) - The console interface module (CIM) links the central processor to the console terminal, TU58 tape drives and the remote diagnostic unit. Signals between the processor and these units are buffered by the CIM to provide noise and static immunity and converted to the proper voltage levels. The CIM also has voltage monitoring circuitry which can detect over or under voltage conditions of the power supply at the processor backplane.

#### 1.4.2 MOS Memory

The MOS memory (MS11-M) provides 256 kb on each module. A maximum of four modules can be installed in the PDP-11/44 system. Each memory module consists of a single hex-height module (M8722) that contains the UNIBUS/extended UNIBUS interface, timing and control logic, error correcting code (ECC) logic and a MOS storage array. The module also contains circuitry for ECC initialization and memory refresh, and a control and status register (CSR). The MS11-M also provides address interleaving for improved speed of operation.

#### 1.4.3 KK11-B Cache Memory

The KK11-B cache increases system performance by decreasing processor-to-memory read-access time. The cache is an 8K-byte, high-speed RAM which is used to store the most commonly accessed memory locations. It is contained on a single hex-height module (M7097) and is organized as a directly mapped cache with a write-through facility.

#### 1.4.4 UNIBUS Terminator (M9302)

The M9302 terminator is a double-height module that must be installed in all PDP-11/44 systems at the end of the UNIBUS furthest from the processor. This module contains terminating resistors and logic which generates a BUS SACK signal.

#### 1.4.5 Optional Modules and Devices

The following options can be used with the PDP-11/44 to expand the system's capabilities.

1.4.5.1 FP11-F Floating-Point Processor - The FP11-F is contained on a single hex-height module (M7093). It allows floating-point operations to be executed with greater speed than equivalent software routines. The floating-point instructions provide for both single-precision (32-bit) and double-precision (64-bit) operands.

1.4.5.2 KE44-A Commercial Instruction Set (CIS) Processor - The KE44-A is contained on one quad-height module (M7091) and one hex-height module (M7092). It enables the KD11-Z to execute the PDP-11 commercial instruction set. The commercial instruction set provides for manipulation of byte strings, character handling and decimal arithmetic operations.

1.4.5.3 TU58 DECTape II - The TU58 is a random-access, fixed-length-block, mass-storage tape system. It uses DIGITAL preformatted tape cartridges which have a storage capacity of 256 K bytes of data in 512-byte blocks. There are 256 blocks on each of the two tracks. The tape cartridges are miniature reel-to-reel packages containing 42.7 m (140 ft) of 3.81, (Ø.150 in) wide tape. The TU58 interfaces to the processor through the CIM module and through the serial line unit (SLU) on the multifunction module.

1.4.5.4 Standard PDP-11 Peripheral Devices - The I/O capabilities of the PDP-11/44 can be expanded through the use of PDP-11 peripheral devices such as card readers, alphanumeric display terminals, lineprinters, teletypewriters or high-speed paper tape readers. Available storage devices include magnetic tapes and disk memories.

#### 1.5 RELATED DOCUMENTS

Table 1-7 lists the manuals and publications that contain information related to the installation and operation of the PDP-11/44 processor system. This information is available from the locations listed in the following paragraphs.

Table 1-7 Related Publications

Title	Document Number
PDP-11/44 CPU Subsystem Technical Manual	EK-KD11Z-TM
BAll-AA,-AB Mounting Box and Power System Technical Manual	EK-BAllA-TM
FP11-F Floating-Point Technical Manual	EK-FP11F-TM
KE44-A CISP Technical Manual	EK-KE44A-TM
MS11-M MOS Memory User's Guide	EK-MS11M-UG
PDP-11 Peripherals Handbook	EB-Ø7667-2Ø/78
PDP-11/Ø4/34A/44/6Ø/7Ø Processor Handbook	EB-17716-18/79
Terminals and Communications Handbook	EB-Ø7666-2Ø/78
TU58 DECTape II Technical Manual	EK-ØTU58-UG
BAll-A Box Assembly Field Maintenance Print Set	MPØØ832
11/44 System Field Maintenance Print Set	MPØØ8Ø9
PDP-11/44 Unit Assembly (IPB)	EK-Ø1144-IP
BALL-A Unit Assembly (IPB)	EK-BALLA-IP
H714Ø Power Supply (IPB)	EK-H714Ø-IP

1.5.1 DIGITAL Personnel Ordering  
Additional copies of this document and printed copies of the documents listed may be obtained from:

Digital Equipment Corporation  
444 Whitney Street  
Northboro, Massachusetts 01532  
ATTN: Printing and Circulation Services (NR2/M15)  
Customer Services Section

1.5.2 Customer Ordering Information  
Purchase orders for supplies and accessories should be forwarded to:

Digital Equipment Corporation  
Accessories and Supplies Group  
Cotton Road  
Nashua, New Hampshire 03060

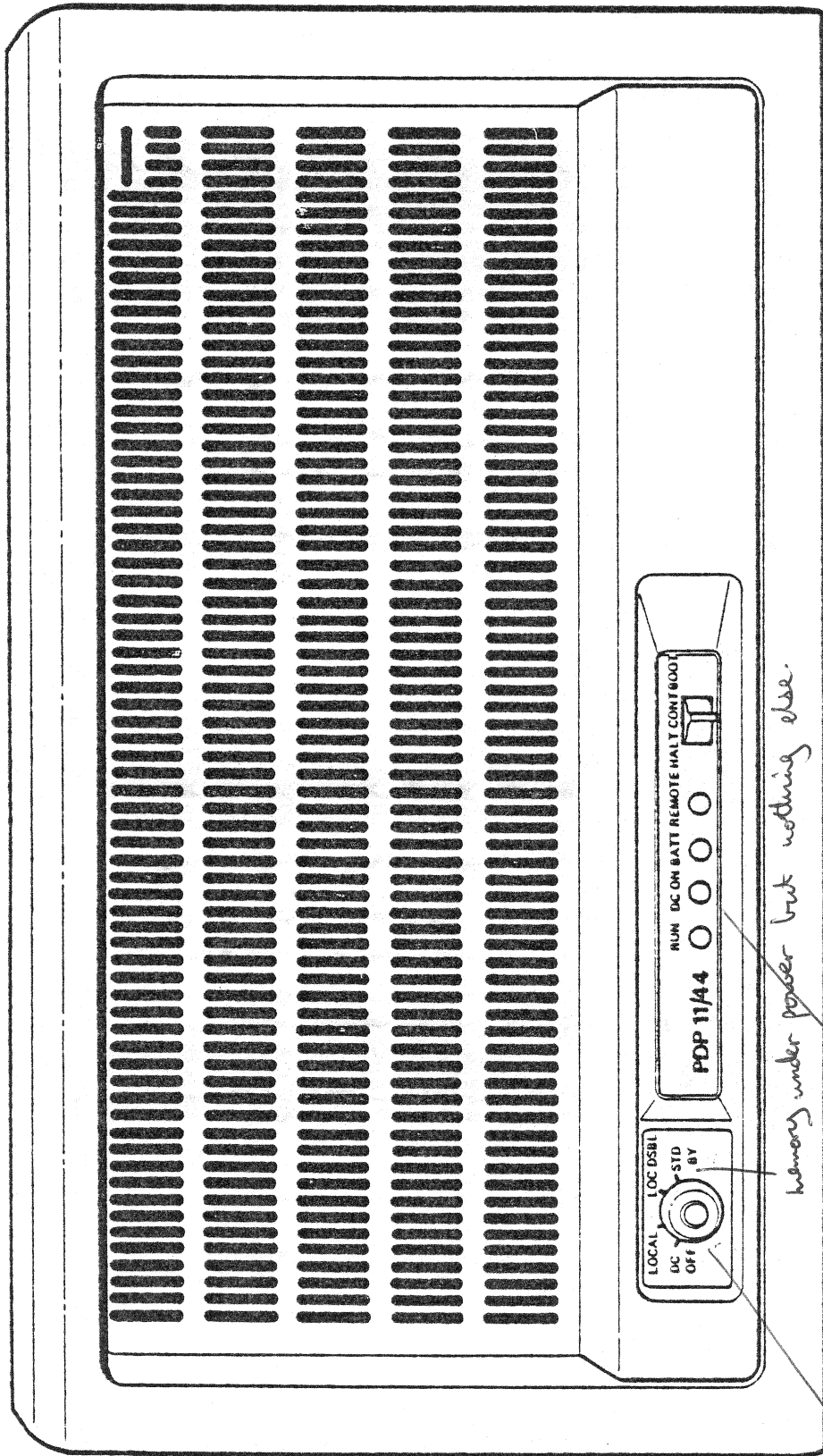
Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free 800-258-1710 from 8:30 a.m. to 5:00 p.m. eastern standard time (U.S. customers only). New Hampshire, Alaska and Hawaii customers should dial (603)-884-6660. Terms and conditions include net 30 days and F.O.B. DIGITAL plant. Freight charges will be prepaid by DIGITAL and added to the invoice. Minimum order is \$35.00. Minimum does not apply when full payment is submitted with an order. Checks and money orders should be made out to Digital Equipment Corporation.

This chapter describes the hardware characteristics of the PDP-11/44 system and includes the addresses assigned to the internal registers and detailed descriptions of the register bit functions. Additional information is contained in the PDP-11 Processor Handbook 1979/80 or the latest edition.

User programs for the PDP-11/44 can be developed using the information in this chapter and the information contained in the software operating system documents.

## 2.1 FRONT CONTROL PANEL

The operators control panel, shown on Figure 2-1, is located on the lower section of the front bezel.



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Figure 2-1 Front Control Panel

Requires to be plugged into that: ~~main~~ keyboard on that.

output from voltage checker. (all voltages). Flashes over 5 + / SEC. if any voltage out of tolerance.

memory under power but nothing else.

Table 2-1 lists and describes the function of the front panel controls and indicators.

Table 2-1 Front Panel Switches and Indicators

Description	Function
Power (4-position rotary keyswitch)	
DC OFF	dc power is removed from the system and cooling fans are off. The DC OFF position does not remove ac power from the system. ac power is removed only by disconnecting the line cord.
LOCAL	Normal ON position. dc power is applied to logic and fans are on. The system terminal can be used as the hardware console. The HALT position of the toggle switch is disabled.
LOC DSBL	Local disable. Normal power is applied to the system. Console mode is disabled but the console terminal can operate in program I/O mode.
STD BY	Standby. Main dc power (+5V, +15V, -15V) is off. Memory voltages are present and fans remain on.
HALT/CONT/BOOT (3-position toggle switch)	
HALT	The CPU program is stopped.
CONT	Continue. The CPU program is continued.
BOOT	A momentary position which enables the bootstrap program. When the toggle switch is released, it returns to the CONT position.

Table 2-1 Front Panel Switches and Indicators (Cont)

Description	Function
Indicators	
RUN	On - Processor is executing instructions.
	Off - Processor has halted.
DC ON	On - Indicates that dc power is present and all voltages are within specified levels.
	Blinking (5 Hz) - Indicates that one or more of the voltages is not within specified levels.
	Off - dc power is off.
BATT	On - Battery is present and charged to 90% or greater capacity. Used only when the battery backup unit (H7750) is installed.
	Slow Blinking - Battery is at less than 90% capacity and is charging.
	Fast Blinking - ac power has failed, battery is discharging, memory contents are valid.
	Off - Battery is fully discharged or not present and memory contents will be destroyed when the ac power fails.
REMOTE	On - CPU is under control of the remote diagnostic unit.
	Off - CPU is not being accessed by the remote diagnostic unit.

## 2.2 CONSOLE COMMANDS

The following paragraphs provide a description of the PDP-11/44 console commands and brief examples of their use. The system terminal can be used to input console commands only when the system is in console mode. Console mode can be entered in either of two ways:

1. The processor halting, or
2. The user typing the console break character, control-P (^P).

When the system is not in the console mode, it is in the program I/O mode and data to or from the terminal is controlled by the software currently being executed.

The commands that can be performed in the console mode are listed in Table 2-2.

Table 2-2 Console Mode Commands

Command Designation	
A. ADDER	I. INITIALIZE
B. BOOT	M. MICROSTEP
C. CONTINUE	N. SINGLE-INSTRUCTION STEP
D. DEPOSIT	R. REPEAT
E. EXAMINE	S. START
F. FILL	T. SELF-TEST
H. HALT	X. BINARY LOAD/UNLOAD

### NOTE

All addresses specified in a console command are assumed to be 22-bit physical addresses and all data transfers are 16-bit word transfers.

### 2.2.1 Special Functions

In the descriptions of each console command, several expressions, special characters and qualifiers are used. Angle brackets, < >, are used to denote category names. For example, the category name <ADDRESS> is used in an expression to represent any valid address. In an actual command, an address (e.g., 17775604) would be typed in place of the category name. Table 2-3 lists and describes the terms and characters used in the syntax expressions.

Square brackets, [ ], surrounding an expression in a command description indicate that the expression is optional and is not required to issue a valid command.

Table 2-3 Console Command Terms and Characters

Name	Description
<SP>	One space
<COUNT>	A numeric count in octal
<ADDRESS>	An address argument in octal
<DATA>	A data argument in octal
<QUALIFIER>	A command modifier
<INPUT-PROMPT>	The console's prompt string (>>>)
<CR>	Carriage Return
<LF>	Line Feed

2.2.1.1 Console Command Qualifiers -- Several of the console commands can be modified by typing qualifiers. Qualifiers expand the capability of commands by providing a number of options. All qualifiers are optional and are not required to issue a valid command. A qualifier always begins with a slash (/). Table 2-4 lists the qualifiers and describes their function.

Table 2-4 Console Command Qualifiers

Qualifier	Function
/G	A general register-qualifier that provides a method of specifying a general register as the address argument. In the examine or deposit command, an E or D can be typed followed by the /G qualifier and the register number (0 to 17 <sub>8</sub> ), rather than the full 22-bit address (eight octal digits).
/N	This qualifier permits examine or deposit commands to be performed on sequential addresses without issuing a new command for each address. The /N qualifier has an associated qualifier value (COUNT), which specifies the number of sequential operations to be performed. The syntax for the /N qualifier is:

/N [:<COUNT>]

Table 2-4 Console Command Qualifiers (Cont)

Qualifier	Function
-----------	----------

The actual number of operations to be performed can be expressed as: the initial operation (1) plus <COUNT - 1> additional operations. The default condition for <COUNT> is one.

/M	This qualifier allows a machine dependent register to be specified as the address argument similar to the /G qualifier that specifies a general register. The address of each machine dependent register is defined as follows:
----	---

Address	Register
0	Floating-Point Data
1	CIS Micro PC (CPC)
2	CIS Data
3	CPU Data
4	CPU Micro PC (MPC)
5	Cache Data
6	CPU Error Register
7	MFM Data
10	Unibus Data
11	Signal Register

/TB	The take bus qualifier is a maintenance feature which allows the console to perform bus transfers even though the bus may be hung.
-----	--

/CB	The cache bypass qualifier allows main memory transfers to be performed even though cache is turned on and the transfer would normally result in a cache hit. This only inhibits a hit for the current command.
-----	---

/E	This qualifier specifies test-extensive and is used only with the self-test (T) command.
----	--

/A	This qualifier specifies test-extensive-APT and is used only with the self-test (T) command for manufacturing use.
----	--

2.2.1.2 Special Address Field Characters -- The special characters used in the <ADDRESS> field of a command to modify the address argument are listed and defined on Table 2-5.

Table 2-5 Special Address Field Characters

Character	Function
+	The plus sign in the <ADDRESS> field of a command will cause the last address used to be incremented by 2 and used as the address argument of the command. If the /G or /M qualifier is also specified in the command, the last address is incremented by 1.
-	The minus sign in the <ADDRESS> field of a command will cause the last address to be decremented (by 2) and used as the address argument of the command. If the /G or /M qualifier is also specified in the command, the last address is incremented by 1.
@	The "at" sign in the <ADDRESS> field of a command will cause the command to use the last data as the address argument. The "at" sign may be used following an indirect addressing chain of instructions.
*	The asterisk in the <ADDRESS> field of a command will cause the command to use the last address as the address argument.
SW	The letters SW in the <ADDRESS> field of a command will cause the command to use the address of the switch register as the address argument. This may be used with examine or deposit commands.

NOTE

When accessing the switch register by the Unibus address 17 777 570, only a read operation can be performed.

2.2.1.3 Control Characters -- A number of control characters are available to the user. Table 2-6 lists control characters and functions.

Table 2-6 Control Characters

Control Character	Echo	Function
<CTRL-C>	^C	Causes all the repetitive console operations to be aborted.
<CTRL-O>	^O	Alternately suppresses and continues the display of data at the terminal. While the display is suppressed, the operation continues but no results are printed. An error or the end of the command will cancel the effect of the control character.
<CTRL-P>	^P	Initiates the console mode if the keyswitch is in the LOCAL position.
<CTRL-Q>	^Q	Restarts the terminal output that was suspended by CTRL-S.
<CTRL-S>	^S	Suspends the terminal output until CTRL-Q is typed. No output is lost.
<CTRL-U>	^U	Cancels the current input line and discards it.
<RUBOUT>OR <DELETE>		Deletes the last character typed on the terminal. The terminal responds to the first RUBOUT by echoing a slash (\) and the character being deleted. Successive RUBOUT will only echo the character being deleted. If the RUBOUT will continue to echo the first character of the input string. The first character typed by the user that is not a RUBOUT will result in the terminal echoing a slash (\) and the new character entered. As an example, the user typing:

```
>>>E<SP>17713<RUBOUT><RUBOUT>65000<CR>
```

The displayed echo is:

```
>>>E17713\31\65000
```

This is equivalent to the user typing the following:

```
>>>E<SP>17765000<CR>
```

### 2.2.2 ADDER Command

This command prints the 16-bit result of the current address pointer and the last data examined plus 2. This command can be used to calculate the effective address for an instruction using mode 6, register 7 or mode 7, register 7.

The syntax for the ADDER command is as follows:

A<CR>

Examples of the ADDER command:

001000	016767	MOV	2000,3000
001002	000774		
001004	001772		
001006	000000	HALT	

E 1000<CR>  
00001000 016767

E<CR>  
00001002 000774

A<CR>  
002000

E<CR>  
000001004 001772

A<CR>  
003000

E<CR>  
00001006 000000

Table 2-7 Device Bootstrap Identifiers

Device Identifier	Device
CT	TA11
DB	RP04/05/06 RMO2/03
DD	TU58
DK	RK03/05/05J (UNITS 2)
DL	RL01
DM	RK06/07
DP	RP02/03
DS	RS03/04
DT	TU55/56
DX	RX01
DY	RX02
MM	TU16/E16(TM02/03)
MS	TS04
MT	TU10/TE10.TS03
PR	PC05 (HI SPEED READER)
TT	ASR 33(LO SPEED READER)
XM	DMC-11
XW	DUP-11
XU	DU11
XL	DL11

### 2.2.3 BOOT COMMAND

The syntax for the BOOT command is as follows:

B [<SP><DEVICE-IDENTIFIER>] <CR>

The BOOT command can be performed only if the processor is halted. When typing B<CR> without the optional device code a default boot is performed depending on the setup of the boot switches located on the Unibus interface (UBI) module (M7098). The optional device identifier is a two character code which identifies the peripheral bootstrap to be performed. Device codes for some typical peripherals are listed on Table 2-7.

The device identifier may also include the unit number of the peripheral (e.g., DK1 boots RK05 unit number 1). If a unit number is not typed, the default number is 0.

When the BOOT command is issued, the device code typed is compared to the device identifiers of the boot ROMs. If the device is not supported by the boot ROMs (i.e., no device match), the console will respond with the console prompt (>>>). If the device is supported or if no device code was typed (default boot), an initialize is issued. The priority bits of the processor status word are set to 7 and the carry bit is set or cleared, depending on the setting of the boot switches. If the carry bit is cleared, the diagnostic programs will be performed prior to the initiation of the bootstrap program for the specified device. General register 0 is loaded with the unit number, or zero if none is typed. The PC is then loaded with the starting address of the boot program. If a device code was not typed, the PC is loaded with the starting address indicated by the boot switches. Once the PC is loaded, the processor is started and the system enters program I/O mode.

Examples of BOOT command:

>>>B <CR>	Perform the default boot.
>>>B <SP> DK1 <CR>	Boot the RK05, Unit 1.

2.2.3.1 Device ROM Identification -- Up to four devices can be selected for program loading. To determine the number of the starting address selected by the switch pack E58 on the UBI module and the devices which are controlled by a bootstrap ROMs perform the following procedure:

1. Examine address 773024 and evaluate the response as follows:

165 XYZ = CPU diagnostic (ODT)  
 173 XYZ = Device bootstrap

The remaining three octal digits (XYZ) can be separated into the binary values associated with the E58 switch positions as follows:

Switch	53	54	55	56	57	58	59	510	
value	x	x	x	y	y	y	z	z	
	⏟ 0-7 <sub>8</sub>			⏟ 0-7 <sub>8</sub>			⏟ 0-4 <sub>8</sub>		
binary 1 =	on								
binary 0 =	off								

2. To identify the device bootstrap ROMs that are installed, initiate the diagnostic program Maindec CZM9B or examine the following five addresses and compare the response with the device ROM identification numbers listed on Table 2-8.

1. 775774 (CPU diagnostic ROM)
2. 773000 (Device ROM #1)
3. 773200 (Device ROM #2)
4. 773400 (Device ROM #3)
5. 773600 (Device ROM #4)

An 177776 response will indicate the continuation of a ROM diagnostic program to an additional ROM.

An XXX777 response will indicate a ROM failure or NO ROM present at the addressed location.

Table 2-8 Bootstrap ROM Identifiers

Octal ID Number	Device ROM
041524	TA11
042104	TU58
042113	RK03/05/05J
042113	TU55/56
042114	RL01
042115	RK06/07
042120	RP02/03
042120	RP04/05/06
042120	RM02/03
042123	RS03/04
042130	RX01
042131	RX02
046515	TU16/45/77/TE16
046523	TS04
046524	TU10, TE10, TS03
050122	PC05 (hi speed reader)
050122	ASR 33 (lo speed reader)
054114	
177776	DL11
177776	
054115	
177776	DMC-11
177776	
054125	
177776	DU11
177776	
054127	
177776	DUP-11
177776	

If the processor was halted when the CONTINUE command was initiated the processor will begin operating and the system will enter the program I/O mode. If the processor was running, when the CONTINUE command was initiated, the system will only enter the program I/O mode.

#### 2.2.4 CONTINUE Command

The syntax for the CONTINUE command is as follows:

C <CR>

If the processor was halted when the CONTINUE command was initiated, the processor will begin operating and the system will enter the program I/O mode. If the processor was running, when the CONTINUE command was initiated, the system will only enter the program I/O mode.

#### 2.2.5 DEPOSIT Command

The syntax for the DEPOSIT command is as follows:

D [<QUALIFIER>]<SP><ADDRESS><SP><DATA><CR>

The DEPOSIT command will deposit <DATA> into the <ADDRESS> specified. The address space will depend upon the qualifiers specified with the command.

Initiating deposits while the processor is running is illegal unless the deposit is to the console switch register (D<SP>SW<SP><DATA><CR>). Since the switch register is internal to the console, the qualifiers /TB and /CB would be useless.

Table 2-9 lists the qualifiers that can be used with the DEPOSIT command.

Table 2-9 Deposit Command Qualifiers

Qualifiers	Function
/G	Enables deposits into the general registers without typing the full eight digit octal address. The qualifiers /N, /TB or /CB can be used in conjunction with the /G qualifier.
/M	The only machine dependent register that can be deposited into is the CPU micro PC register (address 00000004). The data deposited into this register will be used as the next processor micro PC.
/N	Allows deposits into sequential locations.

Table 2-9 Deposit Command Qualifiers

Qualifiers	Function
/TB	The take bus qualifier is used for maintenance purposes only.
/CB	Using the cache bypass qualifier may cause a cache invalidate if the address specified is in cache.

The <ADDRESS> in the DEPOSIT command can be a one to eight digit octal number, SW or any of the special address characters (+, -, \*, @). The <DATA> in the command can be a one to six digit octal number.

Upon completion of the deposit, the console will respond with the console prompt (>>>).

Examples of the DEPOSIT command:

```
>>>D<SP>1000<SP>5           Deposits 5 into location 1000.
>>>D<SP>+<SP>776           Deposits 776 into last address +2. If
                             preceded by above example, then data
                             would be deposited into location 1002.
>>>D<SP>*<SP>400           Deposits 400 into last address. If
                             preceded by above example, then data
                             would be deposited into location 1002.
>>>D/M<SP>4<SP>240         Deposits 240 into the processor micro PC.
>>>D/G/N:5<SP>0<SP>35      Deposits 35 into the next 5 general
                             registers starting with R0.
```

### 2.2.6 EXAMINE Command

The syntax for the EXAMINE command is as follows:

```
E [[<QUALIFIER>]<SP><ADDRESS>]<CR>
```

Examines are legal while the processor is running. The console will respond to the examine command by printing the eight digit physical address examined followed by the six digit octal data contained in that location. This will occur unless the printout is inhibited by control character. Upon completion of the examine, the console will respond with the console prompt (>>>).

The qualifiers that can be used with the EXAMINE command are listed in Table 2-10.

Table 2-10 Examine Command Qualifiers

Qualifier	Function
/G	Enables the general registers to be examined without typing the full eight digit octal address. The qualifiers /N, /TB, /CB can be used in conjunction with the /G qualifier.
/M	Allows the machine dependent registers to be examined. The qualifiers /N, /TB or /CB can be used in conjunction with the /M qualifier.
/N	Allows examines of sequential locations.
/TB	The take bus qualifier is used for maintenance purposes only.
/CB	Using the cache bypass qualifier may cause a cache invalidate if the address specified is in cache.

The <ADDRESS> in the EXAMINE command can be a one to eight digit octal number, SW or any of the special address characters (+, -, \*, @). The <ADDRESS> in the EXAMINE command is optional. If none is typed, the last address is incremented by 2 or 1 if the /G or /M qualifier is used.

Examples of the EXAMINE command:

```
>>>E<SP>1000<CR>           Examine location 1000
00001000 002625
>>>E<CR>                   Examine the next location. An equivalent
00001002 005646             command would be: E<SP>+<CR>

>>>E/G<SP>7<CR>            Examine the PC
17777707 001514
>>>E<SP>@<CR>              Now examine the location pointed to by
00001514 012737             the PC (i.e., use the last data for the
                             new address).

>>>E/M/N:5<SP>0<CR>       Examine the next 5 machine dependent
00000000 130260             registers starting with the machine
                             dependent register 0.
00000001 177777
00000002 177777
00000003 177777
00000004 000010
```

### 2.2.7 FILL Command

The syntax for the FILL command is as follows:

F[<SP><COUNT>]<CR>

The console will send <COUNT> null characters after each <CR> before any further transmissions. Where a power failure occurs, the <COUNT> will be cleared.

The FILL command sets the fill count to the value typed in the <COUNT> field, where <COUNT> is a one to six digit octal number. However, the maximum fill count is 17 (octal). If the <COUNT> entered is greater than 17, then the fill count is set to 17. If no <COUNT> is entered, the fill count is set to zero. Also, on power-up, the fill count is set to zero. Upon completion of the FILL command, the console responds with the console prompt (>>>). The effect of the FILL command on console operation is to cause the <COUNT> number of null characters to be echoed following a <CR>.

Examples of the FILL command:

>>>F<SP>4<CR>                   Set fill count to 4. Subsequent carriage returns will be followed by 4 null characters generated by the MFM module as shown below.

>>>E<SP>1000<CR><NULL><NULL><NULL><NULL><LF>  
00001000 002625 <CR><NULL><NULL><NULL><NULL><LF>

>>>F<CR>                         Resets the fill count to 0.

### 2.2.8 HALT Command

The syntax for the HALT command is as follows:

H<CR>

The HALT command initiates a HALT by asserting the CPU halt request. If the request is honored and the clock is stopped, the console examines register R7 (the PC), and prints 17777707 and the updated PC value. If the processor does not halt within 600 ms, an error message is printed.

If the processor is halted when the halt command is issued, the halt request is not asserted and the console responds with the console prompt (>>>). No error message is issued.

Examples of the HALT command:

```
>>>H<CR>                               Halt the CPU and print the contents of
17777707 001000 <CR>                   R7.
>>>H<CR>                               [Since processor is already halted, this
>>>                                       command is ignored.]
```

#### 2.2.9 INITIALIZE Command

The syntax for the INITIALIZE command is as follows:

I<CR>

The INITIALIZE command is valid only if the processor is halted. Upon receiving a valid INITIALIZE command, the console issues a Unibus initialize. The console then issues the console prompt (>>>).

#### 2.2.10 MICROSTEP Command

The syntax for the MICROSTEP command is as follows:

M[<SP><COUNT>]<CR>

The CPU is allowed to execute the number of microinstructions specified by the <COUNT> value. If no count is specified, one instruction is performed.

The MICROSTEP command is valid only if the processor is halted. The <COUNT>, if specified, is a one to six digit octal number. The command will cause the console to perform an initial microinstruction plus <COUNT>-1 additional microinstructions. For each microstep, the console enables the processor clock for one cycle, examines the micro PC register and prints the register address (00000004) and contents of the PC register.

The count is decremented after each microinstruction is performed. When the count equals 0, the console will print out the last micro PC and the console prompt (>>>). The console is then in the space-bar-step mode and an additional microinstruction is performed each time the space-bar is missed. When no count is specified, the console enters space-bar-step mode after the first microinstruction is performed.

Example of the MICROSTEP command:

```
>>>M<SP>3<CR>                           Perform 3 microinstructions
00000004 000010
00000004 000015
00000004 000210
>>>                                       The console is now in the space-bar-step
                                       mode and another microinstruction can be
                                       executed by pressing the space-bar.
```

Execution of the MICROSTEP command causes the address of the CPU micro PC (00000004) and the contents of that location to be printed. This is the default printout for the MICROSTEP command. Other machine dependent registers may be monitored during microstepping. The following example illustrates this capability.

```
>>>M<CR>
00000004 000015
>>>E/M<SP>10<CR>
10 00000010 000777
>>>00000010 000000
```

This command executes one microstep, sets the console into the space-bar-step mode. The second command examines the machine register 10 (Unibus data) and changes the default printout. Pressing the space-bar will then cause another microstep to be performed and the new contents of machine register 10 to be printed.

### 2.2.11 SINGLE-INSTRUCTION-STEP Command

The syntax for the SINGLE-INSTRUCTION-STEP command is as follows:

N[<SP><COUNT>]<CR>

The SINGLE-INSTRUCTION-STEP command is valid only if the processor is halted. The <COUNT>, if specified, is a one to six digit octal number. This command will cause the console to perform an initial instruction plus <COUNT>-1 additional instructions. For each instruction step, the console enables the processor clock for one instruction, examines the PC and prints its address (17777707) and contents.

The count is decremented after each instruction step is performed. When the count equals 0, the console will print out the last PC and the console prompt (>>>). The console is then in space-bar-step mode. In this mode, an additional instruction step can be performed by pressing the space-bar. When no count is specified, the console enters space-bar-step mode after the first instruction step is performed.

Example of the SINGLE-INSTRUCTION-STEP command:

```
>>>N<SP>3<CR>
17777707 001000
17777707 001002
17777707 001004
>>>
```

Perform 3 single-instruction steps.

The console is now in space-bar-step mode and another instruction can be performed by pressing the space-bar.

### 2.2.12 START Command

The syntax for the START command is as follows:

S[<SP><DATA>]<CR>

The START command is valid only if the processor is halted. The <DATA>, if specified, is a one to six digit octal number that is deposited into the PC when the command is performed. The console responds to a valid START command by issuing an initialize and depositing data into the PC. If no data is specified the PC is unchanged. Following the initialize and deposit, the processor continues and the system enters the program I/O mode.

Examples of the START command:

>>>S<SP>1000<CR>                    Deposits 1000 into the PC and starts the processor from that location.

The following combination of commands is equivalent to the above command:

>>>D/G<SP>7<SP>1000<CR>    Deposits 1000 into the PC.  
>>>S<CR>I                    Initialize - Continue the processor at current PC (1000).

### 2.2.13 SELF-TEST Command

The syntax for the SELF-TEST command is as follows:

T[<QUALIFIER>]<CR>

The SELF-TEST command is valid while the processor is running only if no qualifiers are specified. If qualifiers are specified, the processor must be halted. The qualifiers that may be used are /E (test-extensive) or /A (test-extensive-APT).

The self-test is executed in response to this command and also upon entry into console mode via control-P or processor halt.

If the self-test is completed without error, the message "console" is printed followed by the console prompt. If the self-test was entered as a result of a processor halt, then the test is run, the PC is examined, the contents are printed, and the console prompt (>>>) is printed.

If the T/E or T/A command is entered, additional tests are performed along with the self-test. The console responds to the T/E command by printing "CONSOLE-TESTB" followed by the console prompt.

#### NOTE

Caution should be exercised in performing these commands because the T/E and T/A commands modify main memory. The T/A command restarts the processor after execution of the command.

If any of the tests being performed detect an error, the appropriate error message is printed and the test program will loop on the error.

#### 2.2.14 BINARY LOAD/UNLOAD Command

The syntax for the BINARY LOAD command is as follows:

```
X<SP><ADDRESS><SP><COUNT><CR><COMMAND>  
CHECKSUM><DATA><LOAD CHECKSUM>
```

The syntax for the BINARY UNLOAD command is:

```
X<SP><ADDRESS><SP><COUNT><CR><COMMAND CHECKSUM>
```

#### NOTE

Bit 15 of the <COUNT> field indicates direction control (1=UNLOAD, 0=LOAD).

The BINARY LOAD/UNLOAD command enables strings of bytes of binary data to be read from or written into memory. The number of binary bytes is represented by the <COUNT> field. The console does not perform byte transfers. The load or unload command is executed by assembling the bytes into words before performing the transfer. Since only word transfers are supported, the <COUNT> field must represent an even number.

During the BINARY LOAD command, the processor cannot process control characters typed by the user since the binary data contains similar characters. To prevent the binary load command from being initiated erroneously, the command is terminated by a special <CHECKSUM> character.

During either the binary load or unload command, the checksum is calculated in a similar manner. The command checksum is a binary byte of data that represents the 2's complement of the sum of the ASCII characters that comprise the command string including <CR>. As the command string is read by the console, each character is added to a memory location which is initially set to 0. If no errors occur, the result of the addition will be zero. If the

checksum is correct, the console echoes the prompt string but remains in binary mode. If the command is a binary load, the echo of the input data is suppressed. If the checksum is incorrect, an error is reported. The command checksum is not loaded into memory and does not cause the <COUNT> to be decremented.

In the BINARY LOAD command, a binary string of data of length <COUNT>+1 will be sent to the console once the requestor receives the input prompt which indicates the console's acceptance of the command. The console will sequentially deposit all but the last byte into memory, starting at <ADDRESS>. As the console receives the binary data, it calculates the load checksum. Similar to the command checksum, the load checksum is a binary byte of data which when added to the total checksum should yield a zero result. Once the <COUNT> is exhausted, the load checksum is sent by the console. If an error is encountered during the load or checksum, the error is reported. If no errors occur, the console will respond with the console prompt.

In the BINARY UNLOAD command, the console processes the command and checks the checksum. If the checksum is correct, the console responds with the input prompt followed by a string of bytes, which is the binary data requested. As each binary byte is sent, the 2's complement is added to a byte, initially set to zero. This byte will be sent upon completion of the command and it is followed by the input prompt. The receiver of the unloaded data can now check to issue that all bytes were correctly received.

#### 2.2.15 REPEAT Command

The syntax for the REPEAT command is as follows:

R<SP>(COMMAND)<CR>

This command will repeatedly execute the EXAMINE or DEPOSIT command and is terminated by the control character CTRL-C (^C).

#### 2.2.16 Summary of Errors

When an error is detected during the performance of a console command, the errors listed on Table 2-11 may be reported by the console.

Table 2-11 Summary of Errors

Character	Definition
?01	Syntax error, illegal command.
?11	Illegal internal processor register designated using /M qualifier.
?15	Command is illegal while processor is running.
?20	Transfer error. The console tried to examine or deposit but failed due to memory time-out or parity error.
?21	Halt error. The console tried to halt the processor but failed.
?22	CPU hung. As opposed to ?20, the console directed the processor initiate a transfer, but the transfer was never started.
?30	Checksum error. In executing a BINARY LOAD/UNLOAD command, a checksum error occurred.
?81	Checksum error. In executing the self-test, the console control store was found to have a checksum error in PROM number 1.
?82	Checksum error. In executing the self-test, the console control store was found to have a checksum error in PROM #2.
?85	Error in read/write test for console RAM.
?A7	Halt/continue test of test/extensive failed.
?A8	Pax data bus test of test/extensive failed.
?A9	Pax address test of test/extensive failed.
?AA	Switch register test of test/extensive failed.

## 2.2.17 Summary of Commands

Table 2-12 is a list of the console commands, special characters, modifiers and qualifiers.

Table 2-12 Console Command Summary

### Commands

B	[<SP> <DEVICE IDENTIFIER>] <CR>	Boot
C	<CR>	Continue
D	[<QUALIFIERS>]<SP><ADDRESS><SP><DATA >CR>	Deposit
E	[<QUALIFIERS><SP><ADDRESS>] <CR>	Examine
F	[<SP> <COUNT>] <CR>	Fill
H	<CR>	Halt
I	<CR>	Initialize
M	[<SP> <COUNT>] <CR>	Microstep
N	[<SP> <DATA>] <CR>	Single-instruction step
S	[<SP> <DATA>] <CR>	Start
T	[<QUALIFIER>] <CR>	Self-test
A	<CR>	Adder
R	<COMMAND> <CR>	Repeat

### Special Characters

Control C	- causes the aborting of all repetitive console operations
Control O	- enables/disables terminal output
Control P	- forces entry into console mode if keyswitch is in LOCAL position. Programs in operation will continue, however no I/O operations to a terminal can occur by program until the program I/O mode is reentered.
Control U	- deletes entire line currently being typed
Control S	- stops terminal output
Control Q	- starts terminal output

### Address Modifiers

+	autoincrement
-	autodecrement
*	use last address
@	use last data as address
SW	switch register

*Halt at 165714 after booting  
means test run OK*

Table 2-12 Console Command Summary (Cont)

Qualifiers

/G	general register
/N:<COUNT>	multiple operations
/M	machine dependent registers
/TB	take bus
/CB	cache bypass
/E	test-extensive
/A	test-extensive-APT

### 2.3 PDP-11/44 REGISTERS

The upper 4K of the physical address space is assigned to the CPU registers and I/O device registers. Table 2-13 lists some of the registers and their associated addresses.

Table 2-13 PDP-11/44 CPU and I/O Device Register Address

Address	Register
17 777 776	Processor Status Word (PSW)
17 777 772	Program Interrupt Request (PIRQ)
17 777 766	CPU Error
17 777 707 - 17 777 700	CPU General Registers
17 777 676 - 17 777 660	User Data PAR, Reg. 0-7
17 777 656 - 17 777 640	User Instruction PAR, Reg. 0-7
17 777 636 - 17 777 620	User Data PDR, Reg. 0-7
17 777 616 - 17 777 600	User Instruction PDR, Reg. 0-7
17 777 576	MM Status Register 2 (SR2)
17 777 574	MM Status Register 1 (SR1)
17 777 572	MM Status Register 0 (SR0)
17 777 566 - 17 777 560	Console Terminal SLU
17 7XX XX6 - 17 7XX XX0	TU58 DECTape SLUs (Normally 17776500)
17 777 570	Switch Register
17 772 516	MM Status Register 3 (SR3)
17 772 376 - 17 772 360	Kernel Data PAR, Reg. 0-7
17 772 356 - 17 772 340	Kernel Instruction PAR, Reg. 0-7
17 772 336 - 17 772 320	Kernel Data PDR, Reg. 0-7
17 772 316 - 17 772 300	Kernel Instruction PDR, Reg. 0-7
17 772 276 - 17 772 260	Supervisor Data PAR, Reg. 0-7
17 772 256 - 17 772 240	Supervisor Instruction PAR, Reg. 0-7
17 772 236 - 17 772 220	Supervisor Data PDR, Reg. 0-7
17 772 216 - 17 772 200	Supervisor Instruction PDR, Reg. 0-7
17 770 372 - 17 770 200	MAP Registers

### 2.3.1 CPU Registers

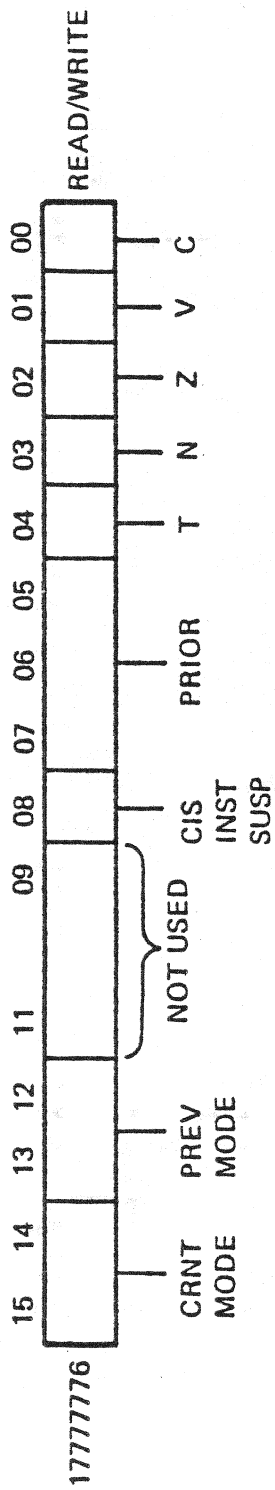
The CPU contains several registers which can be used to store processor status information, error information and interrupt requests. Eight general purpose registers are also included to be used as accumulators, counters, index registers, or other programming functions.

2.3.1.1 Processor Status Word (PSW) - The format of the processor status word (PSW) register is shown on Figure 2-2. Table 2-14 lists the functions of the PSW bits.

Table 2-14 Processor Status Word Register Bit Descriptions

Bits 15:14 Current Mode - These bits specify the current processor mode as follows:

1. 00 - The processor is in kernel mode and all operations are legal.
2. 01 - The processor is in supervisor mode. A HALT instruction will trap to location 4 and the instructions RESET and SET PRIORITY LEVEL (SPL) are treated as a NO OPERATION (NOP).
3. 10 - An illegal mode. If memory management is enabled, a memory management abort occurs.
4. 11 - The processor is in user mode. A HALT instruction will trap to location 4 and the instructions RESET and SPL are treated as a NOP.



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Figure 2-2 PSW Register Format

Bits 13:12 Previous Mode - Specify the previous processor mode, prior to the last trap, interrupt or loading of the PSW. The modes are the same as defined for the current mode (bits 15:14).

Bits 11:09 - Not used.

Bit 08 CIS Instruction Suspension - This bit is set to 1 when a CIS instruction is entered and cleared when the instruction is completed. If this bit is set when an interrupt occurs, it indicates that the instruction was not completed and must be continued upon return from the interrupt. If this bit is set, the T-bit cannot be set. This prevents looping in trace trap mode.

Bits 07:05 Priority - These bits specify the current level of the processor priority. The central processor operates at any of eight levels of priority, 0-7. When the CPU is operating at level 7, an external device cannot interrupt it with a request for service. The central processor must be operating at a lower priority than the priority of the external device's request in order for the interruption to take effect. The eight processor levels provide an interrupt mask, which can be altered through use of the set priority level (SPL) instruction which can only be used by the kernel mode. This instruction allows a kernel mode program to alter the central processor's priority without affecting the rest of the processor status word.

Bits 04:00 Condition Codes - The condition codes contain information which occurred as a result of the previous CPU operation. The bits are defined as follows:

T (bit 04) Trap bit - Set to 1 or cleared under program control. When set, a processor trap will occur through location 14 on completion of instruction execution and a new processor status word will be loaded. This bit is useful for debugging programs by providing a method of tracing the execution of programs.

N (bit 03) Negative - Set to 1 if the result of the last data manipulation was negative.

Z (bit 02) Zero - Set to 1 if the result of the last data manipulation was zero.

V (bit 01) Overflow - Set if the result of the last data manipulation caused an overflow.

C (bit 00) Carry - Set if the last data manipulation produced a carry bit.

2.3.1.2 Program Interrupt Request Register - System software may request an interrupt by setting one of bits (PIR) 15 through 09 for PIR7-PIR1 in the program interrupt request (PIRQ) register. The hardware sets bits 07:05 and 03:01 to the encoded value of the highest PIR bit set. Bits 07:05 allow the program interrupt active (PIA) field to be moved into the processor status word register and set the processor priority to the level of the request honored. This disables all requests on the same level or below. Bits 03:01 can be used as an index constant in branching to an interrupt service routine for the appropriate priority level request.

When a priority interrupt request is granted, the processor traps to location 240. A new program count is taken from location 240 and a new PSW from location 242. The interrupt service routine must queue requests within a priority level and clear the PIR bit before the interrupt is dropped.

The bit assignments of the PIRQ are shown on Figure 2-3 and Table 2-15 lists the functions of the bits.

Table 2-15 Processor Interrupt Request Register Bit Descriptions

Bits 15:09 PIR7-PIR1 - Seven program interrupt request bits which may be set to request an interrupt at a given priority level.

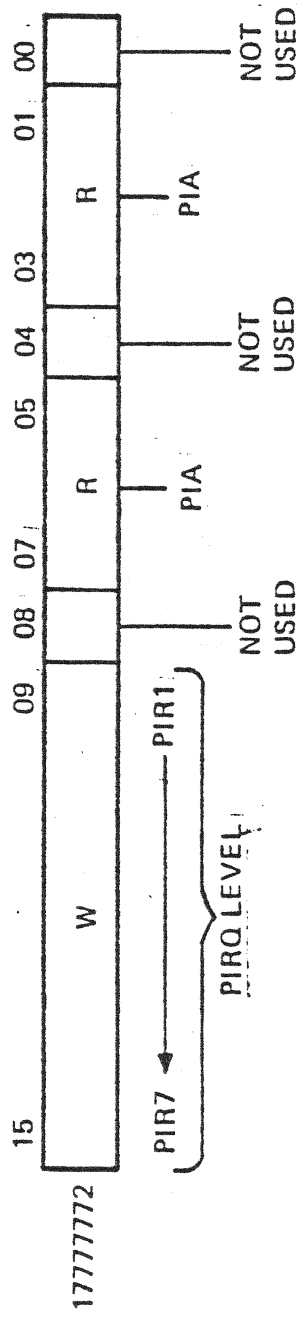
Bit 08 - Not used.

Bits 07:05 and 03:01 PIA - Program interrupt active bit, which is the encoded value of the highest PIR bit set.

Bit 04 - Not used.

Bit 00 - Not used.

1



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Figure 2-3 PIR Register Format

2.3.1.3 Error Register - This register identifies the source of the abort or trap that used the vector at location 4. Bits 07:04, bit 02 and bit 00 are cleared when the CPU error register is written; the remaining bits are software transparent and are accessible only when the console has control. Figure 2-4 descriptions are listed on Table 2-16.

Table 2-16 Error Register, Bit Descriptions

Bit 15 Data Transfer - This bit monitors the DATA TRAN line of the processor. When clear, this bit indicates the processor is initiating a data transfer on the Unibus.

Bit 14 C1 - This bit is set to 1 when the Unibus control signal BUS C1 is asserted, indicating a DATO or DATOB transfer is being performed.

Bit 13 Cache Restart - This bit when set to 1 indicates that the cache has generated the signal necessary to restart the processor clock.

Bit 12 KTE - This bit when set to 1 indicates that one of the memory management errors (nonresident, page length or read-only abort) has occurred.

Bit 11 Bus Error - This bit when set to 1 indicates that the processor has attempted to access nonexistent memory, odd address during word reference or there was no response on the Unibus within approximately 20 ns.

Bit 10 Parity Error - This bit when set to 1 indicates that the processor has received a memory parity error.

Bit 09 AC LO - This bit when set to 1 indicates that Unibus AC LO is asserted. This signal is not latched and therefore bit 09 is not affected by a processor INIT.

Bit 08 DC LO - This bit when set to 1 indicates that Unibus DC LO is asserted. This signal is not latched and therefore bit 08 is not affected by a processor INIT.

Bit 07 Illegal Halt - This bit is set to 1 when a HALT instruction is attempted when the processor is in user or supervisor mode.

Bit 06 Odd Address Error - This bit is set to 1 when the program attempts a word reference on an odd address.

Bit 05 Memory Time-Out - This bit is set to 1 when the program attempts to read a word from a nonexistent memory location. This does not include Unibus addresses.

Table 2-16 Error Register, Bit Descriptions (Cont)

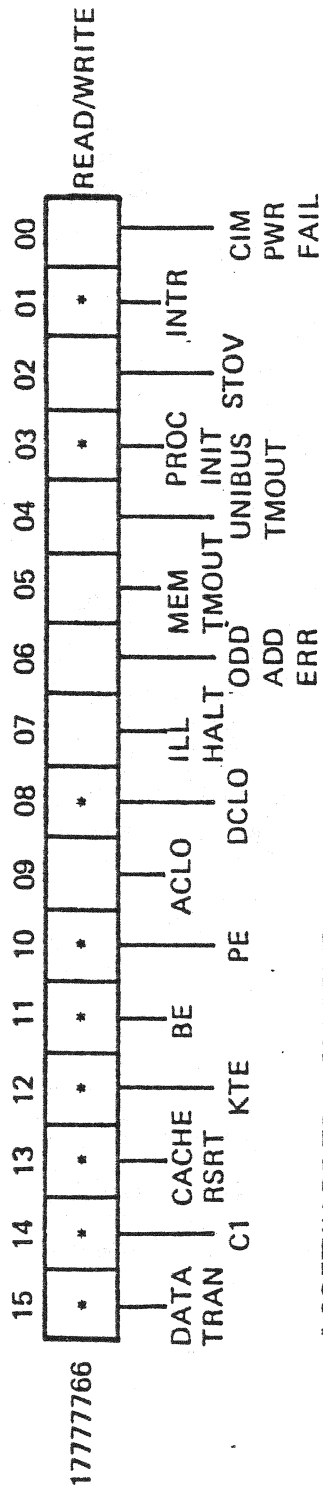
Bit 04 Unibus Time-Out - This bit is set to 1 when there is no response on the Unibus within approximately 20  $\mu$ s.

Bit 03 Processor Initialize - This bit monitors the processor initialize signal.

Bit 02 Stack Overflow - This bit is set to 1 when the Kernel hardware stack is less than octal 400.

Bit 01 Interrupt - This bit is set when the PAX interrupt line is asserted.

Bit 00 CIM Power Failure - This bit when set to 1 indicates that DC power to the machine has exceeded voltage tolerance limits for a period of 1.5  $\mu$ s or greater.



\* SOFTWARE TRANSPARENT

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Figure 2-4 CPU Error Register Format

2.3.1.4 General Registers - The CPU contains several 16-bit general registers that can be used as accumulators, index registers, autoincrement registers, autodecrement registers or as stack pointers for temporary storage of data. A few of these registers are used for special purposes. Register 7 (R7) is used as the program counter (PC) and contains the address of the next instruction to be executed. R6 is generally used as the processor stack pointer (SP), if the processor is in kernel mode. If the processor is in supervisor or user mode, R16 or R17 is used as the processor stack pointer respectively. Table 2-17 lists the general registers and their addresses and functions.

Table 2-17 General Register Addresses

Address	Function
17 177 705 - 17 177 700	R5-R0, General Purpose Registers
17 777 706	R6, Kernel Mode Stack Pointer
17 777 707	R7, Program Counter
17 777 710	R10, Temporary Storage
17 777 711	R11, Unused
17 777 715 - 17 777 712	R15-R12, Temporary Storage
17 777 716	R16, Supervisor Mode Stack Pointer
17 777 717	R17, User Mode Stack Pointer

### 2.3.2 Multifunction Module Register

The multifunction module (MFM) contains two serial line units (SLUs) which provide the interface ports between the serial line devices and the PDP-11/44 processor. The SLU can be connected to a console terminal to the TU58 DECTape transport or to a remote diagnostic facility. The console terminal operates as a standard I/O device or as a programmer's console to access and load registers within the CPU.

2.3.2.1 Console Terminal Receiver Control/Status Register (RCSR)  
Figure 2-5 shows the format of the console terminal receiver control/status register (RCSR) and Table 2-18 lists and describes the functions of the bits.

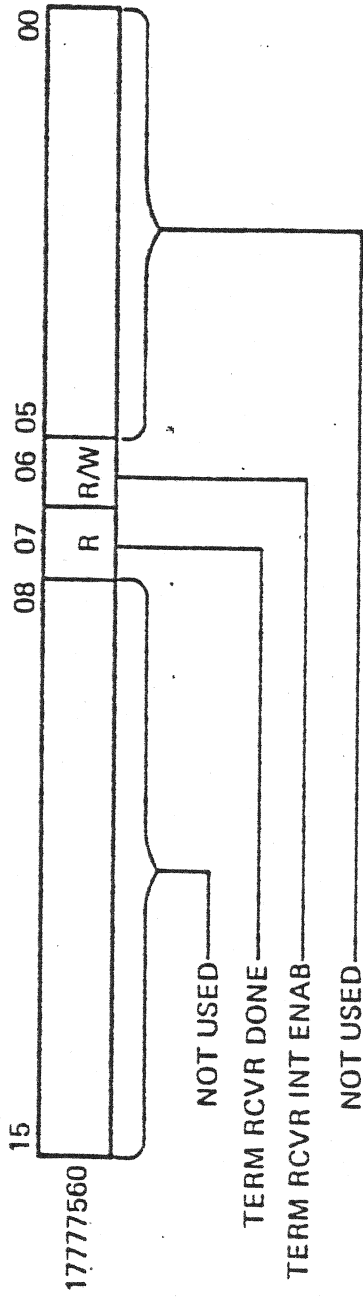
Table 2-18 Console Terminal RCSR Bit Description

Bits 15:08 - Not used.

Bit 07 Terminal Receiver Done - A read-only bit that is set to 1 during the program I/O mode when a complete character is contained in the console terminal RBUF. Cleared when the RBUF is addressed and when an initialize operation occurs.

Bit 06 Terminal Receiver Interrupt Enable - A read/write bit, set to 1 to allow the interrupt sequence to be initiated when the RCVR DONE bit is set.

Bit 05:00 - Not used.



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Figure 2-5 Console Terminal RCSR Format

2.3.2.2 Console Terminal, Receiver Data Buffer (RBUF) - Figure 2-5 shows the format of the console terminal receiver data buffer register and Table 2-19 lists and describes the function of the bits.

Table 2-19 Console Terminal RBUF Bit Descriptions

Bit 15 Terminal Error - A read-only bit that is set to 1 when the TERM OR ERROR (bit 14), the TERM FR ERROR (bit 13) or the TERM PAR ERROR (bit 12) is set to 1. Cleared by an initialize operation or by the reception of new and correct data.

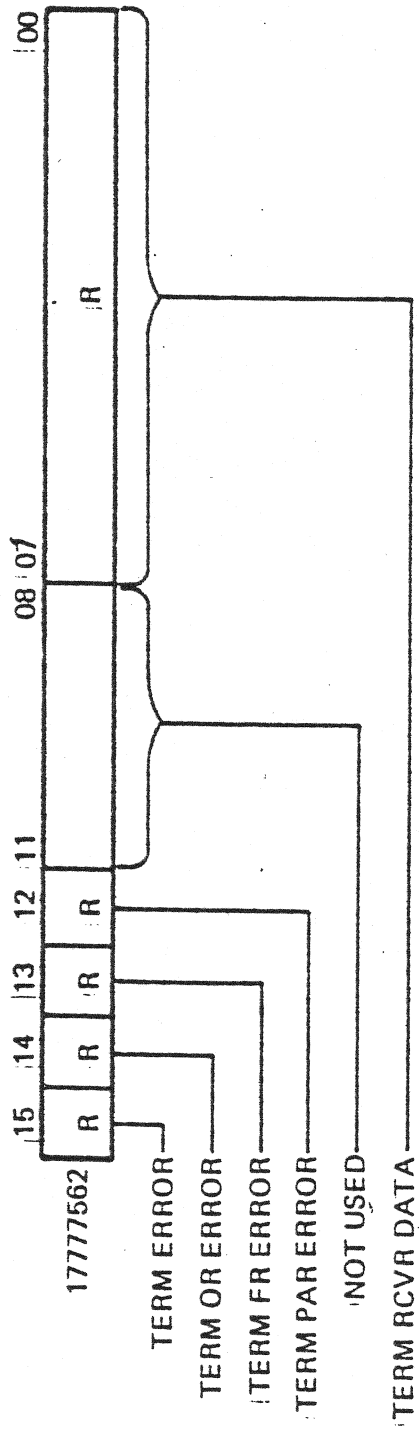
Bit 14 Terminal Overrun Error - A read-only bit that is set to 1 if the character in the RBUF has not been read before another character is received. Cleared by an initialize operation or when the RBUF is emptied.

Bit 13 Terminal Framing Error - A read-only bit that is set to 1 when the character read does not include a valid stop bit(s). Cleared when a valid character is received. This bit may indicate an error in transmission or the reception of a "break" character.

Bit 12 Terminal Parity Error - A read-only bit that is set to 1 when the parity of the data in the RBUF is incorrect relative to the parity mode selected. This indicates an error in transmission. Cleared when the parity of the next character is validated.

Bits 11:08 - Not used.

Bits 07:00 Terminal Receiver Data - Read-only bits that is the data character that was read from the terminal.



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Figure 2-6 Console Terminal RBUF Format

2.3.2.3 Console Terminal Transmitter Control/Status Register (XCSR) - Figure 2-7 shows the format of the console terminal, transmitter control and status register (XCSR) and Table 2-20 lists the function of the bits.

Table 2-20 Console Terminal XCSR Bit Descriptions

Bits 15:08 - Not used.

Bit 07 Terminal Transmitter Ready - A read-only bit that is set to 1 when the console terminal XBUF register is ready to accept a character or when an initialize operation occurs. It initiates the interrupt sequence if the TERM XMIT INT ENB bit (06) is set to 1. Cleared when the XBUF receives a character.

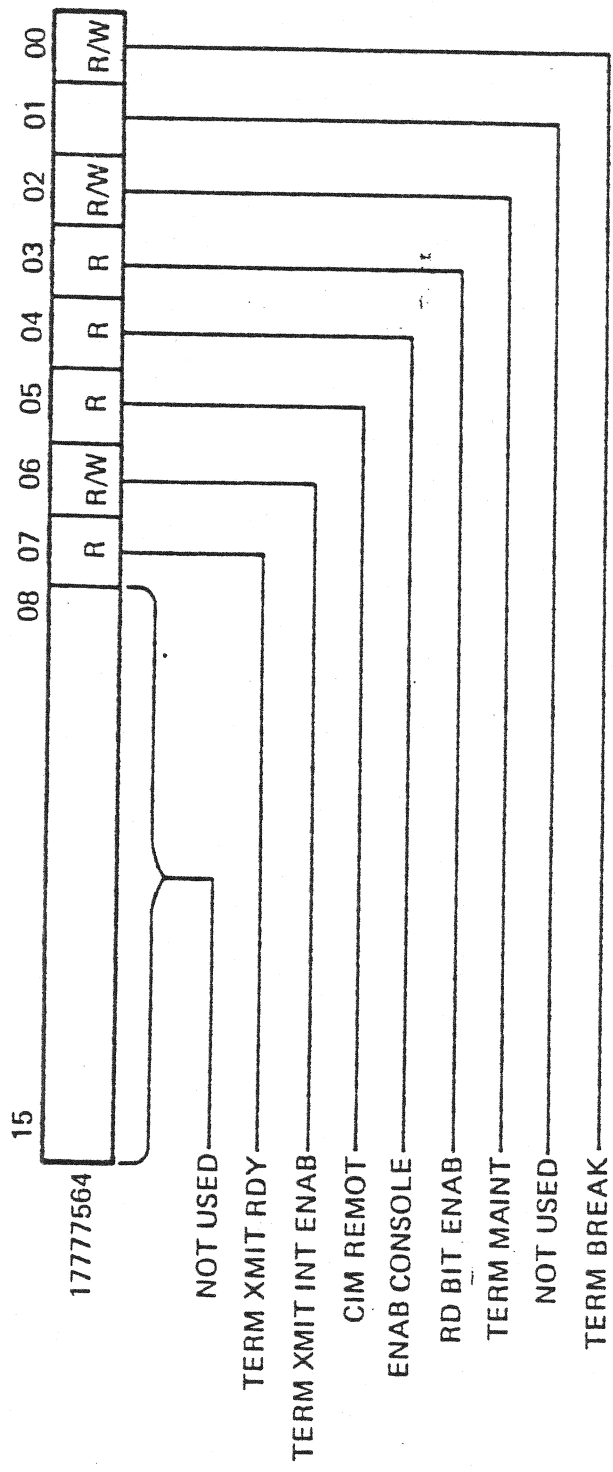
Bit 06 Terminal Transmitter Interrupt Enable - A read/write bit that is set to 1 by program to enable the interrupt sequence to be initiated if the TERM XMIT RDY (bit 07) is set to 1. Cleared by program or by the initialize sequence.

Bit 05 Console Interface Remote - A read-only bit that is set to 1 when the CPU is operating in the remote diagnostic mode.

Bit 04 Enable Console - A read-only bit that is set to 1 by program to indicate that the CPU is operating in the console mode.

Bit 03 Remote Diagnostic Bits Enable - A read-only bit set by switch S3-4 (E79) on the MFM module. When the switch is on, the status of bits 04 and 05 is entered into this register and when the switch is off, the bits will be zero's.

Bit 02 Terminal Maintenance - A read/write bit which when set to 1 by the program, will cause a closed loop test of the console terminal UART. The serial output of the XBUF will be returned to serial input of the RBUF. The data transfer rate will be at the baud rate of the transmitter. Cleared by an initialize operation or by the program.



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Figure 2-7 Console Terminal XCSR Format

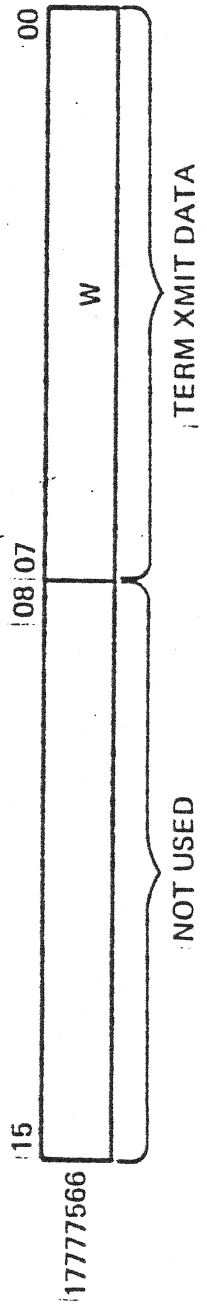
Bit 00 Terminal Break - A read/write bit that is set to 1 by program and causes the transmission of a continuous space character. This will cause a framing error (bit 13) of the RBUF to be set. Cleared by program or by an initialize sequence. Can be disabled permanently by removing the jumper lead W5 on the MFM module.

2.3.2.4 Console Terminal Transmitter Buffer Register (XBUF) - Figure 2-8 shows the format of the console terminal transmitter buffer register (XBUF) and Table 2-21 lists the function of the bits.

Table 2-21 Console Terminal (XBUF) Bit Descriptions

Bits 15:08 - Not used.

Bits 07:00 Terminal Transmitter Data - Write-only bits which are the data character to be transferred to the console terminal.



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Figure 2-8 Console Terminal XBUF Format

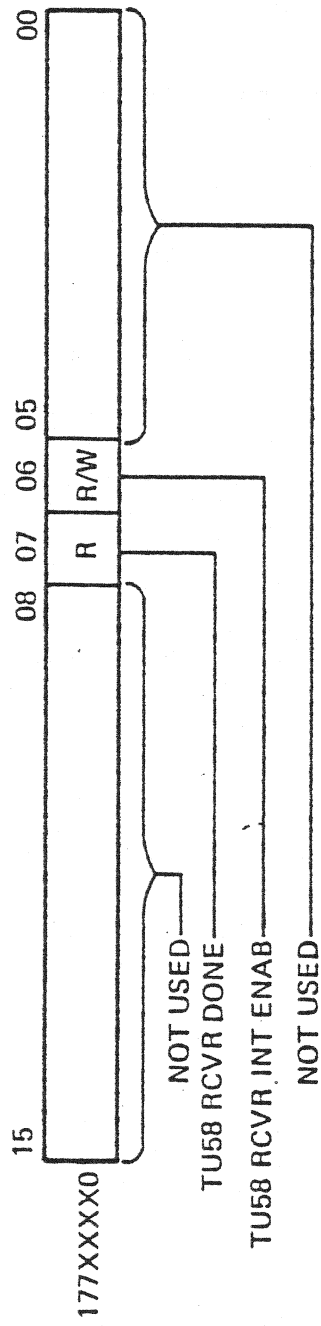
2.3.2.5 TU58 Receiver Control/Status Register (RCSR) - Figure 2-9 shows the format of the TU58 receiver control/status register (RCSR) and Table 2-22 lists the function of the bits. The typical addresses assigned to the TU58 registers are from 17776500 to 17776506.

Table 2-22 TU58 RCSR Bit Descriptions

Bits 15:08 - Not used.

Bit 07 TU58 Receiver Done - A read-only bit that is set to 1 during the program I/O mode only when a complete character is contained in the TU58 RBUF. Cleared when the TU58 RBUF is addressed or when an initialize operation occurs. Initiates the interrupt sequence when the TU58 RCVR INT ENAB bit (06) is set to 1.

Bit 06 TU58 RCVR Interrupt Enable - A read/write bit which is set to 1 by program to allow the interrupt sequence to be initiated by the TU58 RCVR DONE bit (07).



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Figure 2-9 TU58 RCSR Format

Bits 05:00 - Not used.

2.3.2.6 TU58 Receiver Buffer Register (RBUF) - Figure 2-10 shows the format of the TU58 receiver buffer register (RBUF) and Table 2-23 lists the function of the bits.

Table 2-23 TU58 RBUF Bit Descriptions

Bit 15 TU58 Error - A read-only bit that is set to 1 when the TU58 OR ERROR (bit 14), TU58 FR ERROR (bit 13) or the TU58 PAR ERROR (bit 12) is set to 1. Cleared by an initialize operation or by the reception of new and correct data.

Bit 14 TU58 Overrun Error - A read-only bit that is set to 1 if the character in the RBUF has not been read before another character is received. Cleared by an initialize operation or when the RBUF is emptied.

Bit 13 TU58 Framing Error - A read-only bit that is set to 1 when the character read in the RBUF does not have a valid stop bit(s). Cleared when a valid character is received. This bit may indicate an error in transmission or the reception of a "break" character.

Bit 12 TU58 Parity Error - A read-only bit that is set to 1 when the parity of the character read in the RBUF is incorrect relative to the parity mode selected. Cleared when the parity of the next character is validated.

Bits 11:08 - Not used.

Bits 07:00 TU58 Received Data - Read-only bits that are the data character received from the TU58.

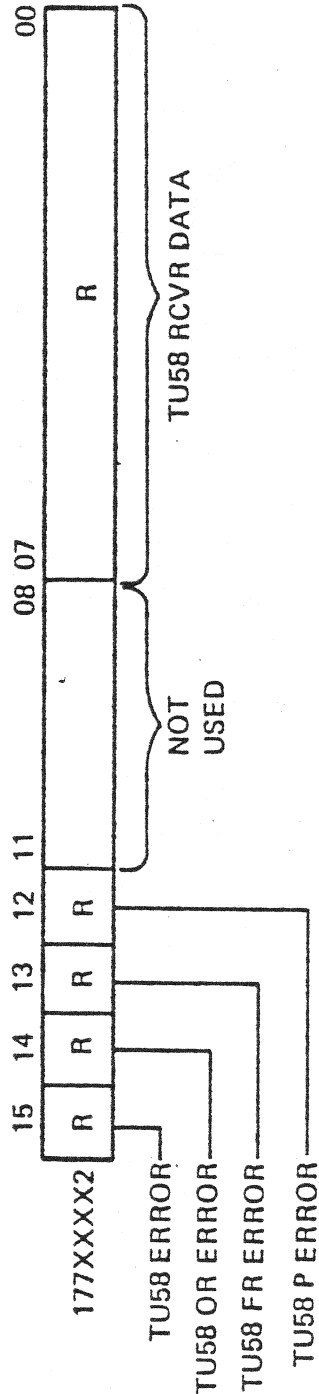


Figure 2-10 TU58 RBUF Format

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2.3.2.7 TU58 Transmitter Control/Status Register (XCSR) - Figure 2-11 shows the format of the TU58 transmitter control/status register (XCSR) and Table 2-24 lists the functions of the bits.

Table 2-24 TU58 XCSR Bit Description

Bits 15:08 - Not used.

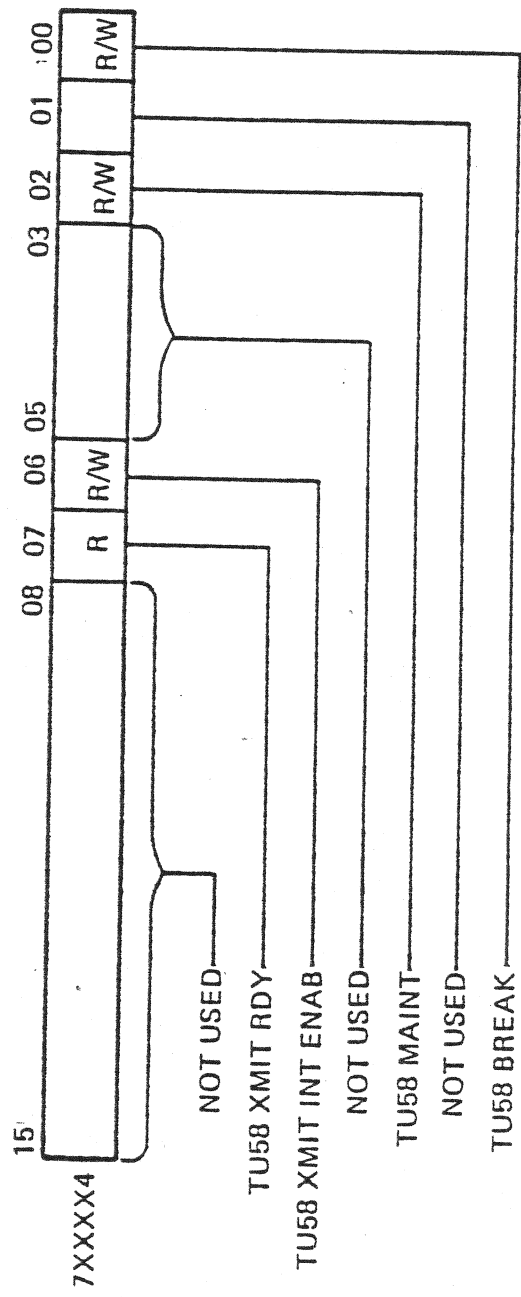
Bit 07 TU58 Transmitted Ready - A read-only bit that is set to 1 when the TU58 XBUF is ready to accept a character or when an initialize operation occurs. Setting the bit initiates an interrupt sequence if the TU58 XMIT ENAB (bit 06) is set to 1. Cleared when a character is written into the XBUF.

Bit 06 TU58 Transmitter Interrupt Enable - A read/write bit that is set to 1 by program. Enables the interrupt sequence to be initiated if the TU58 XMIT RDY (bit 07) is set to 1. Cleared by the program or by the initialize sequence.

Bits 05:03 TU58 Maintenance - A read/write bit that when set to 1 by program will cause a closed loop test of the TU58 UART. The serial output of the transmitter will be returned to the serial input of the receiver. The data transfer rate will be the baud rate of the transmitter. Cleared by program or by an initialize operation.

Bit 01 - Not used.

Bit 00 TU58 Break - A read/write bit that is set to 1 by program and that causes a space character to be continuously transmitted to the TU58. Cleared by program or by an initialize sequence. The break function can be permanently disabled by removing jumper lead W10 on the MFM module.



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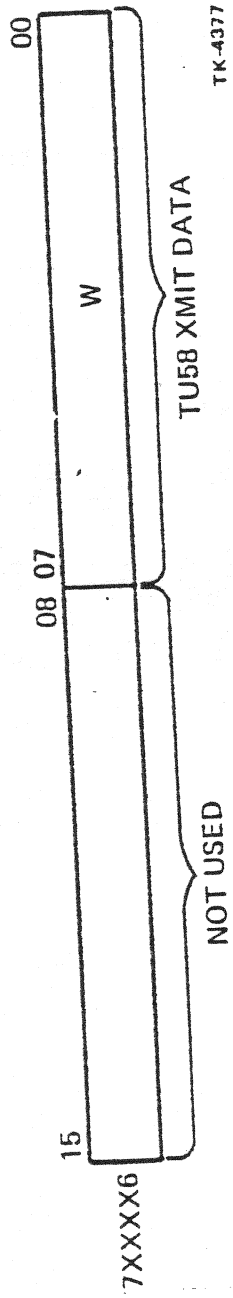
Figure 2-11 TU58 XCSR Format

2.3.2.8 TU58 Transmitter Data Buffer (XBUF) Register - Figure 2-12 shows the format of the TU58 transmitter buffer register (XBUF) and Table 2-25 lists the functions of the bits.

Table 2-25 TU58 XBUF Bit Descriptions

Bits 15:08 - Not used.

Bits 07:00 TU58 Transmitter Data - Write-only bits that are the data character to be transferred to the TU58.



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Figure 2-12 TU58 XBUF Format

2.3.2.9 Signal Register - The signal register provides information of the operational status of the MFM module and CPU. Figure 2-13 shows the format of the signal register and Table 2-26 lists the function of the bits.

Table 2-26 Signal Register, Bit Description

Bits 15:06 - Not used.

Bit 05 Run - Set to 1 to indicate that the processor is executing instructions.

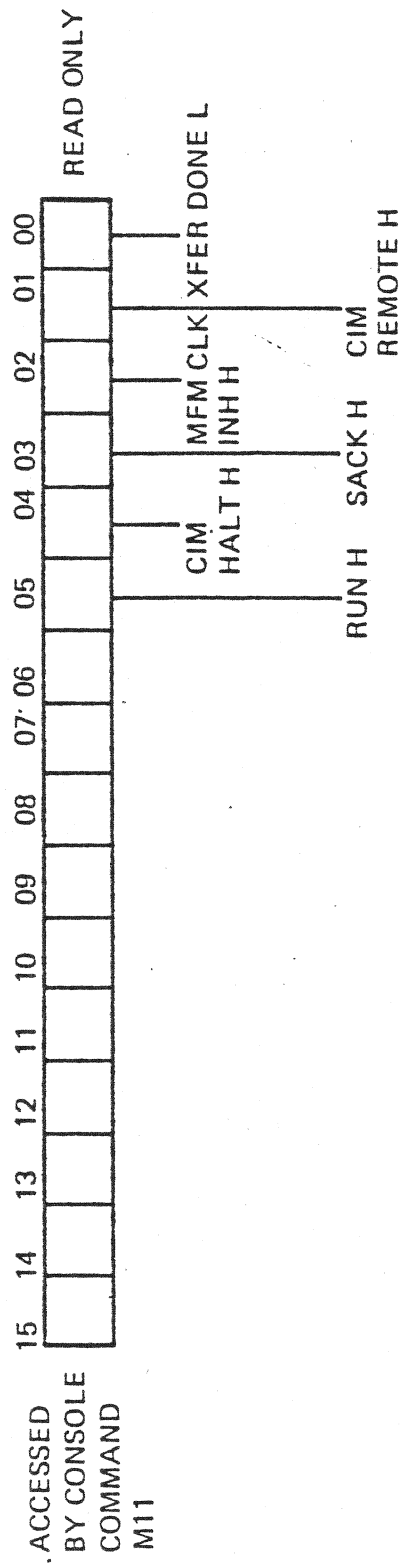
Bit 04 Console Interface Module Halt - Set to 1 to indicate that the toggle switch on the control panel of the PDP-11/44 is in the HALT position.

Bit 03 Selection Acknowledge - Set to 1 to indicate that a device has acknowledged the bus grant.

Bit 02 Multifunction Module Clock Inhibit - Set to 1 when the MFM is inhibiting the operation of the CPU clock.

Bit 01 Console Interface Module Remote - Set to 1 when the CPU is operating in the remote mode.

Bit 00 Transfer Done - Set to indicate a data transfer error has occurred.



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Figure 2-13 Signal Register Format

2.3.2.10 Line Time Clock Control/Status Register (LKS) - Figure 2-14 shows the format of the Line Time Clock Control Status Register (LKS) and Table 2-27 lists the functions of the bits.

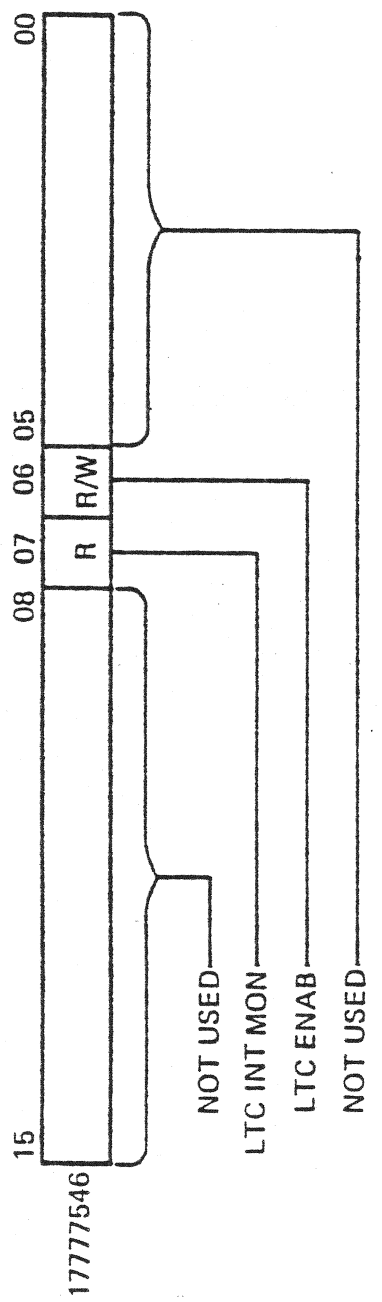
Table 2-27 Line Time Clock LKS, Bit Descriptions

Bits 15:08 - Not used.

Bit 07 Line Time Clock Monitor - A read-only bit set to 1 for each cycle of the ac voltage and cleared by the program. Provides an interrupt request at an interval of 16.66 ms for the 60 Hz version and 20 ms for the 50 Hz version. Also set during the initialize sequence.

Bit 06 Line Time Clock Interrupt Enable - A read-write bit set to 1 by the program to allow the interrupt sequence to be initiated when the LTC MON (bit 07) is set.

Bits 05:00 - Not used.



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Figure 2-14 Line Time Clock (TCSR) Format

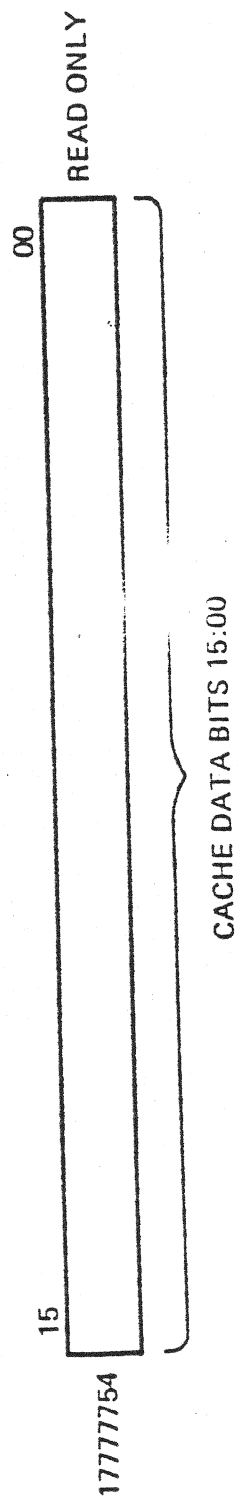
### 2.3.3 Cache Memory I/O, Page Registers

The cache memory module (KK11-B) contains several registers that are used to store data information, error indications and control and status information.

2.3.3.1 Cache Memory Data Register (CDR) - The cache memory data register (CDR) is loaded from the 16-bit data array section of the cache RAM when a read access occurs to main memory below 256K. Figure 2-15 shows the CDR format and Table 2-28 lists the functions of the bits.

Table 2-28 Cache CDR Bit Description

Bits 15:00 - These bits are read-only and are loaded from the 16-bit data array section of the cache RAM on every read access to main memory, except the top 256K bytes. This register can be used with the Hit on Destination Only bit to aid the cache diagnostics in identifying failures in the data section of the cache array.



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Figure 2-15 Cache CDR Format

2.3.3.2 Cache Hit Register (CHR) - The cache hit register (CHR) is a dual purpose register used as an address match register when written and as a tag address/hit register when read. Figure 2-16 shows the CHR format and Table 2-29 lists the functions of the bits.

Table 2-29 Cache CHR Bit Descriptions

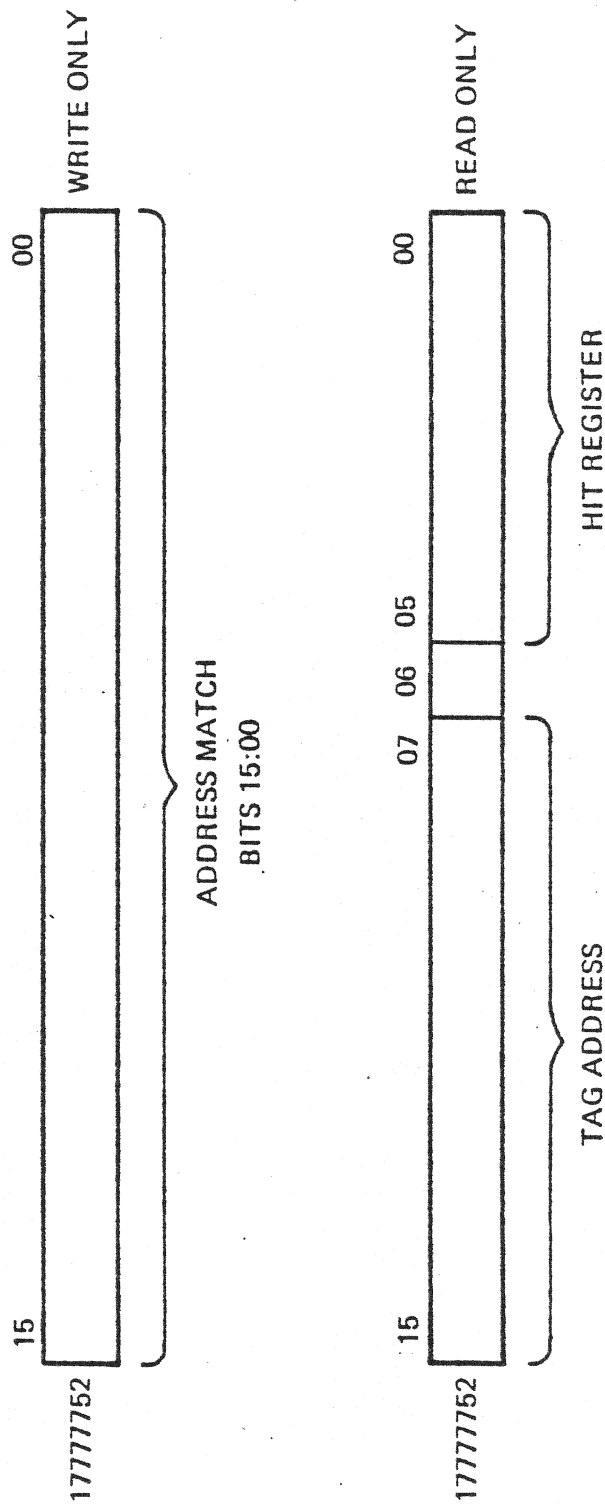
Bits 15:00 Address Match Bits 15:00 - These write-only bits correspond to bits 15:00 of the address match register. Bits 21:16 of the address match register are contained in the cache maintenance register. When bits 21:00 of the address match register are the same as memory address lines 21:00, a sync pulse is provided to a user accessible test point.

Bits 15:07 Tag Address - These read-only bits contain the nine tag store memory bits of the last main memory access. When used in conjunction with bits 01 and 00 of the cache maintenance register, the tag address bits will allow cache diagnostics to read the tag field of any location in the array.

Bit 06 - Not used.

Bits 05:00 Hit Register - These read-only bits indicate the number of read and write cache hits on the last processor accesses to non-I/O page memory. These bits flow from the LSB to MSB of the field with a 1 indicating a hit and a 0 indicating a miss.

2.3.3.3 Cache Maintenance Register (CMR) - The cache maintenance register (CMR) is a dual purpose register. The high byte is used as an address match register when written and contains maintenance bits when read. The lower byte contains read/write maintenance bits. Figure 2-17 shows the format of the CMR and Table 2-30 lists the function of the bits.



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Figure 2-16 Cache CHR Format

Table 2-30 Cache CMR Bit Descriptions

Bits 15:10 Address Match Bits 21:16 - These write-only bits correspond to bits 21:16 of the address match register. Bits 15:00 of the address match register are contained in the cache hit register. When bits 21:00 of the address match register are the same as memory address lines 21:00, a sync pulse is provided to a user accessible test point.

Bits 15:13 Compare 3:1 - These read-only bits represent the value of the compare lines of the cache hit detect logic. When these bits are set, it indicates that the 9-bit tag field, currently being read, matches the upper 9 bits of the PAX address (bits 21:13).

Bit 12 Valid - This read-only bit, when set, indicates that the word currently being read from cache is a valid copy of a backing store location.

Bits 11:09 High Parity, Low Parity, Tag Parity - These read-only bits indicate the parity of the high byte of the data field, low byte of the data field and the tag field respectively.

Bit 08 Hit - The read-only bit, when set, indicates that all the conditions necessary for a processor read hit have been met.

Bit 04 Enable Stop Action - The read/write bit, when set, will cause the processor clock to stop when a cache parity error or address match condition is detected.

Bit 03 Address Matched - This read/write bit is set when the 22-bit address match register is equal to the 22-bit PAX address.

Bit 02 Enable Halt Action - This read/write bit, when set, will cause a processor halt upon detection of a cache parity error or address match condition.

Bit 01 Hit on Destination Only - This read/write bit, when set, causes the cache to be enabled only during the destination memory access portion of an instruction. Read hits and updates will occur only during the final destination access.

Bit 00 Tag Data from Address Match Register - This bit, when set, enables the tag field of the cache to be written with data from bits 08:00 of the address match register. When this bit is set, all cache writes will cause the valid bit to be cleared in that location

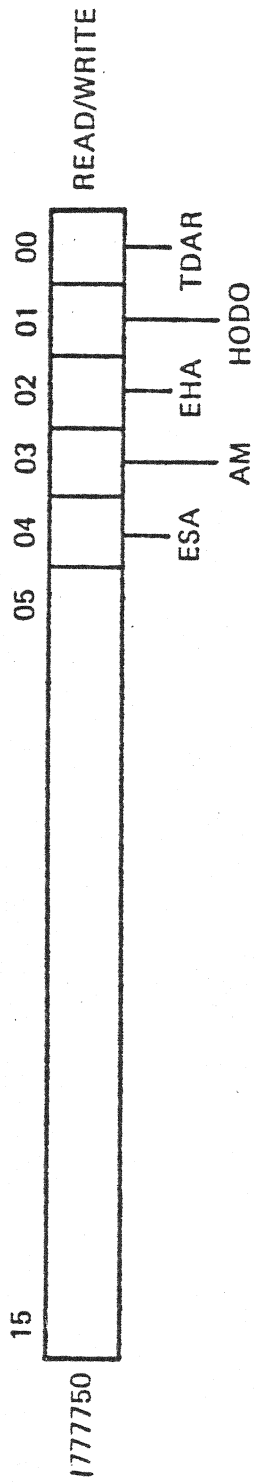
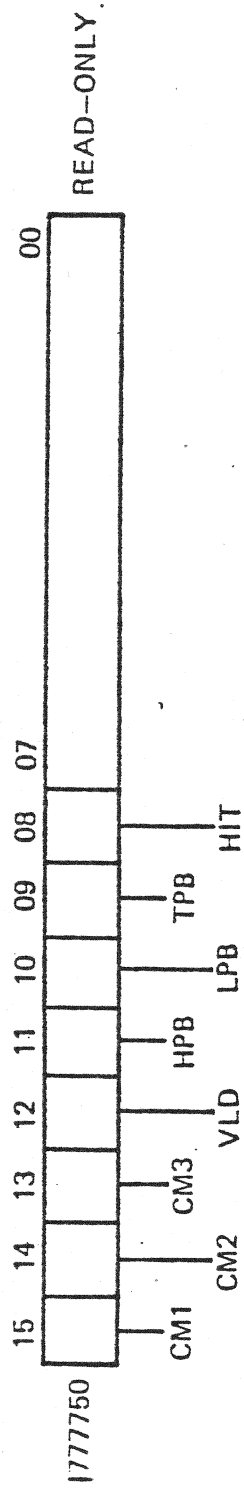
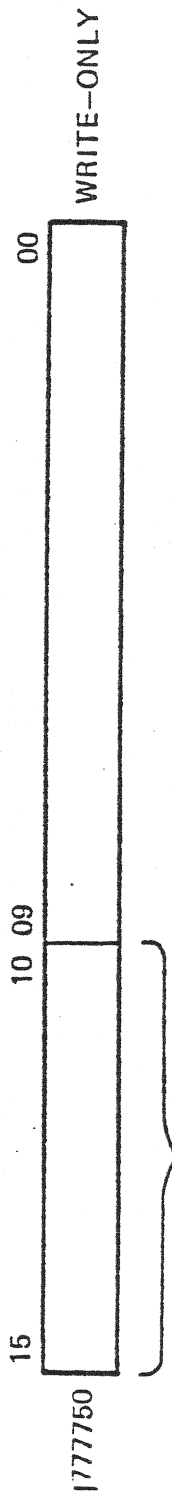


Figure 2-17 Cache CMR Format

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2.3.3.4 Cache Control/Status Register (CCSR) - Figure 2-18 shows the format of the cache (CCSR) and Table 2-31 lists the functions of the bits.

Table 2-31 Cache CCSR Bit Descriptions

Bits 15:14 - Not used.

Bit 13 Valid Store in Use - This read-only bit controls which set of valid store bits is currently being used to determine the validity of the contents of the tag store memory. When this bit is set to 1, valid bit B is in use; when clear, bit A is in use. This bit is complemented each time the cache is flushed.

Bit 12 Valid Clear in Progress - This read-only bit, when set, indicates that the cache is currently in the process of clearing a valid store set. A cache clear cycle is initiated on power-up and when the flush cache bit is set.

Bit 11 - Not used.

Bit 10 Write Wrong Parity Tag - This read/write bit, when set, causes tag parity bits to be written with wrong parity on processor read misses and write hits. This will cause a parity error to occur on the next access to that location. This feature is used by the cache diagnostic programs.

Bit 09 Unconditional Cache Bypass - This read/write bit, when set, will force all memory references by the processor to go to main memory. Read or write hits will result in invalidation of those locations in cache and misses will not change the contents.

Bit 08 Flush Cache - This write-only bit, when set, will cause the entire contents of the cache to be declared invalid.

Bit 07 Parity Error Abort - This read/write bit controls the response of cache to a parity error. When this bit is set, a cache parity error will cause a force miss and an abort to occur. When cleared, this bit inhibits the abort and enables an interrupt to parity error vector 114. All cache parity errors result in force misses.

Bit 06 Write Wrong Parity Data - This read/write bit, when set, causes high and low parity bytes to be written with wrong parity on all updates (processor read misses and write hits). This will cause a cache parity error to occur on the next access to that location. This feature is used in the cache diagnostic programs.

Bits 05-04 - Not used.

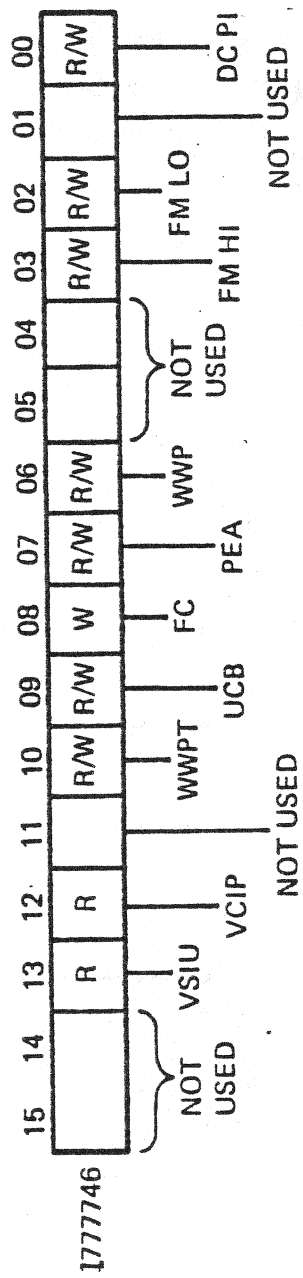
Bit 03 Force Miss High - This read/write bit, when set, causes a forced miss on CPU reads where bit 12 of the location's address is a 1. This bit can also be set by a toggle switch (S1) on the cache board. When switch S1 is returned to the cache-on position, bit 03 remains set until cleared by the program or by an initialization.

Bit 02 Force Miss Low - This read/write bit, when set, causes a forced miss on CPU read operations when bit 12 of the location's address is a 0. This bit can also be set by a toggle switch (S2) on the cache board. When switch S2 is returned to the cache-on position, bit 02 remains set until cleared by the program or by an initialization. Setting both bits 03 and 02 will cause all CPU read operations to be misses thereby effectively disabling the cache.

Bit 01 - Not used.

Bit 00 Disable Cache Parity Interrupt - This read/write bit, when set, overrides the cleared condition of the parity error abort bit (bit 07), thereby disabling the interrupt to location 114. The following shows the relationship between bits 00 and 07 and the effect on cache parity errors.

Bit 07	Bit 00	Result of Cache Parity Error
0	0	Interrupt to location 114 and force miss
0	1	Force miss only
1	0/1	Abort and force miss



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Figure 2-18 Cache CCSR Format

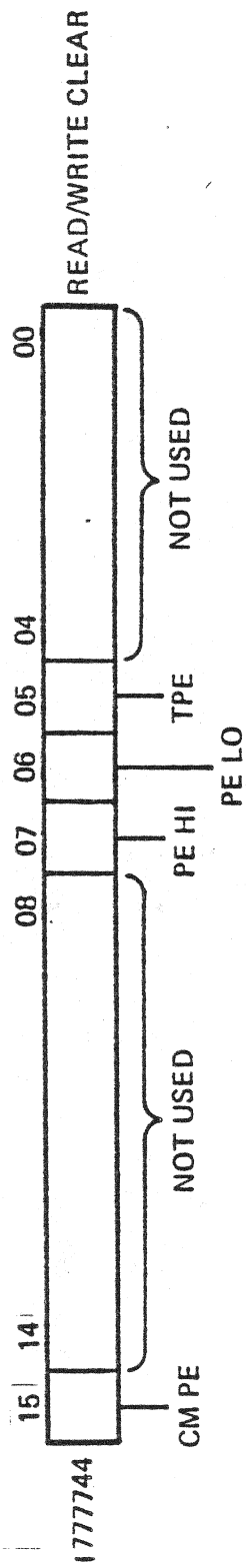
2.3.3.5 Cache Error Register (CME) - Figure 2-19 shows the format of the cache CME register and Table 2-32 lists the functions of the bits.

Table 2-32 Cache CME Bit Descriptions

Bit 15 Cache Memory Parity Error - This bit is set if a cache parity error is detected while the cache parity abort bit (control register bit 07) is set or if a memory parity error occurs. If this bit is set, the cache will force a miss. This bit is cleared by any write to the cache memory error register or by a console INIT.

Bits 14:08 - Not used.

Bit 07 Parity Error High Byte - Set to 1 when a parity error occurs in the high byte of data and the PEA (bit 07) of the CSSR is set to 1. If the cycle is not aborted (PEA = 0), bit 06:05 of the CME will also be set by this error. All parity bits are cleared by a write operation to the CME or by an initialize sequence.



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Figure 2-19 Cache CME Format

Bit 06 Parity Error Low Byte - Set to 1 when a parity error occurs in the high byte of the CDR and the PEA (bit 07) of the CCSR is set to 1. If the cycle is not aborted (PEA = 0), bits 07 and 05 will also be set to 1 by this error.

Bit 05 Tag Parity Error - Set to 1 when a parity error occurs in the tag address field of the CHR and the PEA (bit 07) of the CCSR is set to 1. If the cycle is not aborted (PEA = 0) bits 06 and 07 of the CME will also be set to 1. All parity bits are cleared by a write operation to the CME or by an initialize sequence.

Bits 04:00 - Not used.

#### 2.3.4 Memory Management Registers

The 16-bit virtual address is translated to a 22-bit physical address by the memory management function. Four status registers, 48 page address registers (PAR) and 48 page descriptor registers (PDR) are associated with the memory management.

2.3.4.1 Status Register 0 (SR0) - Memory management status register 0 (SR0) contains error flags, the page number whose reference caused the abort and various status flags. The format of SR0 is shown in Figure 2-20 and bit descriptions are listed on Table 2-33.

Bits 15:13 Error Flags - These error bits are prioritized, i.e., flags to the right are less significant and are ignored if a flag to the left is present. For example, a nonresident fault service routine would ignore page length and access control faults.

#### Table 2-33. SR0 Bit Descriptions

Bit 15 Nonresident Abort - This bit is set to 1 when an attempt to access a page with an access control field (ACF) key equal to 0 or 3. It is also set if there is an attempt to use memory relocation with a processor memory management mode of 2.

Bit 14 Page Length Abort - This bit is set to 1 if there is an attempt to access a location in a page with a block number (virtual address bits 12:06) that is outside the area authorized by the page length field (PLF) of the page descriptor register (PDR) for that page. It is also set if there is an attempt to use memory relocation with a processor mode of 2. Bits 15 and 14 can be set simultaneously by the same access attempt.

Bit 13 Read-Only Abort - This bit is set if there is an attempt to write in a read-only page. Read-only pages have an access key of 1.

Bits 12:09 - Not used.

Bit 08 Maintenance/Destination Mode - This bit, when set, specifies that only destination mode references will be relocated using memory management. This bit is used for maintenance purposes only.

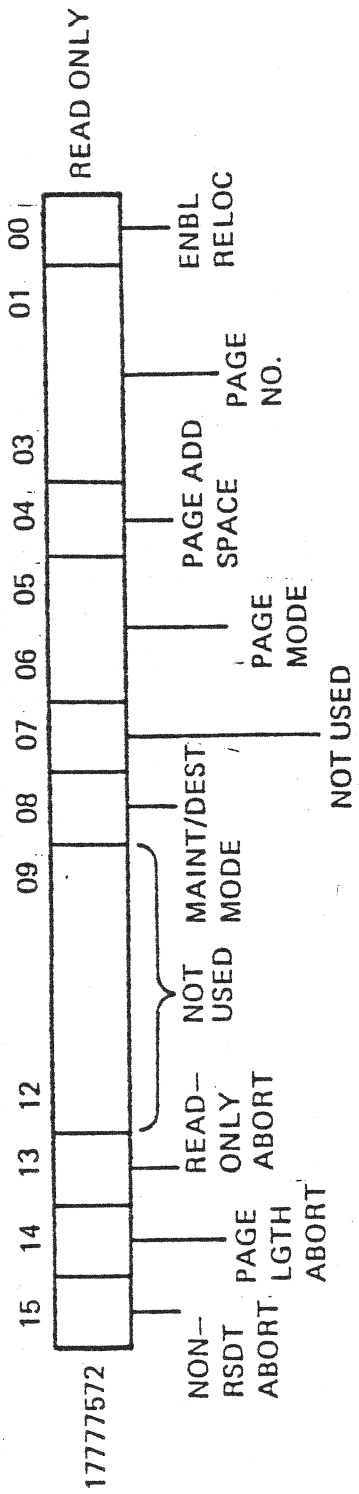
Bit 07 - Not used.

Bits 06:05 Page Mode - These bits indicate the processor mode (kernel/supervisor/user) associated with the page causing the abort; kernel = 00, supervisor = 01, user = 11, illegal mode = 10. If an illegal mode is specified, bits 15 and 14 will be set.

Bit 04 Page Address Space - This bit indicates the type of address space (I or D) the memory management was using when the fault occurred; 0 = I space, 1 = D space.

Bits 03:01 Page Number - These bits contain the page number of the reference causing a memory management fault.

Bit 00 Enable Relocation - When this bit is set, all addresses are relocated. When this bit is clear, the memory management facility is inoperative and addresses are not relocated or protected.



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Figure 2-20 Memory Management SR0 Format

2.3.4.2 Status Register SR1 - The format of memory management status register 1 (SR1) is shown in Figure 2-21. SR1 records any autoincrement/decrement of the general purpose register, including explicit references through the PC. SR1 is cleared at the beginning of the fetch cycles for each instruction. Whenever a general purpose register is either autoincremented or autodecremented, the register number and the amount in 2's complement notation by which the register was modified are written into SR1. A single operand instruction will only set the lower byte with the source register change and the upper byte with the destination register change. Table 2-34 describes each of the bits in the SR1.

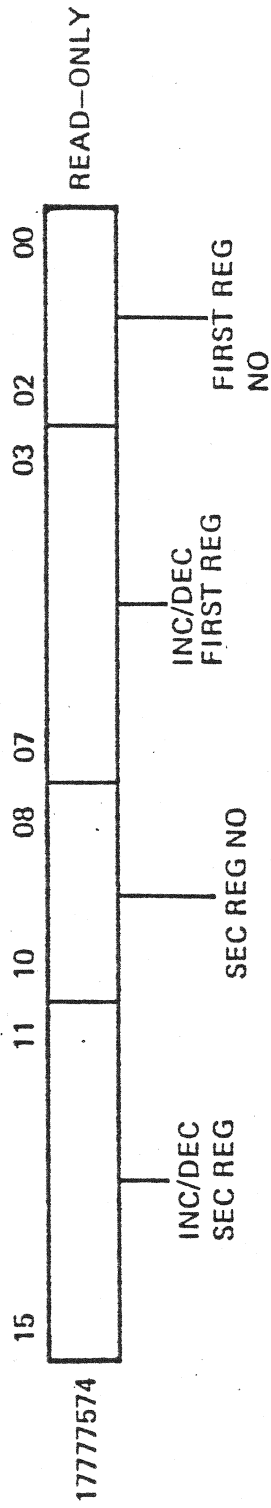
Table 2-34 SR1 Bit Descriptions

Bits 15:11 Increment/Decrement Second Register - The 2's complement value of the incrementing or decrementing of the second general register.

Bits 10:08 Second Register Number - The octal value of the second general register number. (Octal 0 for register 0.)

Bits 07:03 Increment/Decrement First Register - The 2's complement value that is a result of the incrementing or decrementing of the first general register.

Bits 02:00 First Register Number - The octal value of the first general register.



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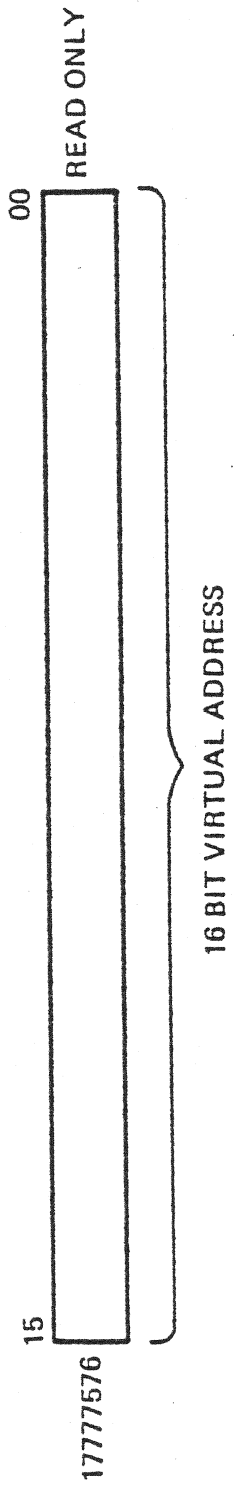
Figure 2-21 Memory Management SRI Format

2.3.4.3 Status Register SR2 - The status register SR2 is loaded with the value of the program counter at the beginning of the fetch cycle of each instruction.

At the beginning of an interrupt SR2 contains the address trap vector, the T bit, parity traps, odd address, parity and time-out aborts. Figure 2-22 shows the format of SR2 and Tables 2-35 and 2-36 list the function of the bits.

Table 2-35 SR2 Bit Description

Bits 15:00 Virtual Address - Read-only bits that are the virtual address at the beginning of the fetch cycle of each instruction.



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Figure 2-22 Memory Management SR2 Format

2.3.4.4 Status Register SR3 - Figure 2-23 shows the format of SR3 and Table 2-36 describes the bits.

Table 2-36 SR3 Bit Descriptions

Bits 15:06 - Not used.

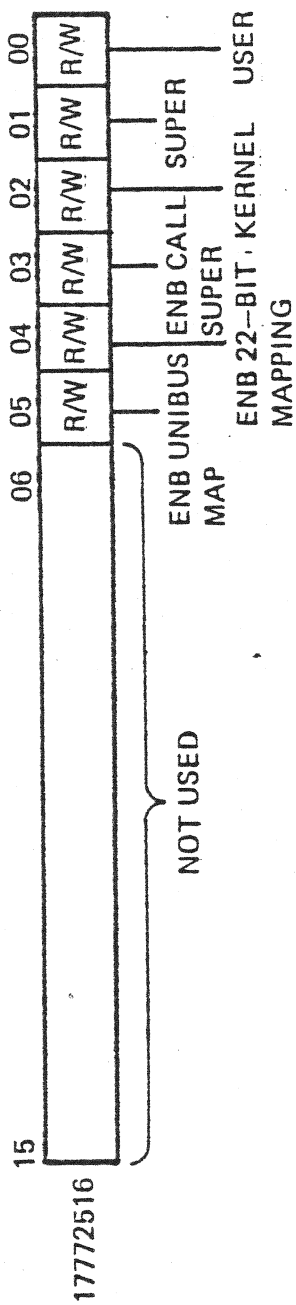
Bit 05 Enable Unibus Map - Set to 1 by program control to enable the Unibus map which converts 18-bit Unibus addresses to 22-bit memory addresses.

Bit 04 Enable 22-Bit Mapping - Set to 1 by program control to enable 22-bit mapping when the ENBL RELOC (bit 01) of SR0 is set to 1. When cleared to 0, 18-bit mapping is enabled.

Bit 03 Enable Call Supervisor - Set to 1 by program to enable the CALL TO SUPERVISOR MODE instruction to be performed.

Bit 02 Kernel - Set to 1 by program control to enable data space the kernel mode D space.

Bit 01 Supervisor - Set to 1 by program control to enable data space the supervisor mode D space.

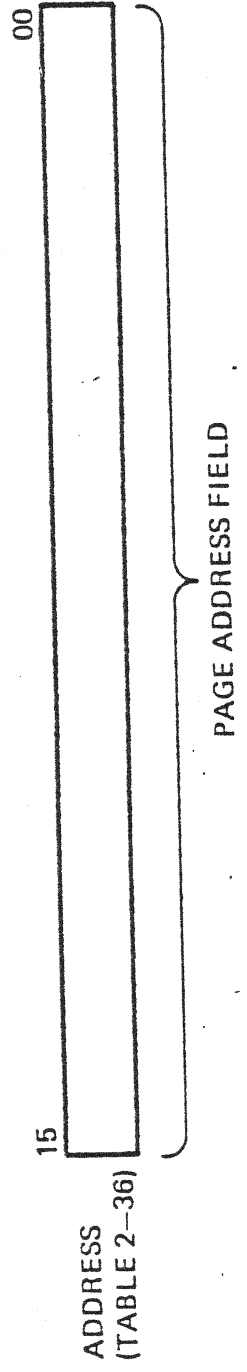


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Figure 2-23 Memory Management SR3 Format

Bit 00 User - Set to 1 by program control to enable data space in the user mode. When data space is disabled, all references use the instruction (I) space registers. When D space is enabled, either the I space or the D space registers are used, depending upon the phase that the instruction is in.

2.3.4.5 Page Address Registers (PAR) - The page address registers (PAR) contain the 16-bit page address field that specifies the base address of the page as a block number in physical memory. Figure 2-24 shows the format of a PAR and Table 2-37 describes the bits.



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Figure 2-24 Memory Management PAR Format

Table 2-37 PAR Bit Descriptions

Bits 15:00 Page Address Field - Read/write bits that are the page address field. There are six sets of eight PARs, one set each for kernel data space, kernel instruction space, supervisor data space, supervisor instruction space, user data space and user instruction space. The addresses of these registers are listed in Table 2-38.

#### 2.3.4.6 Page Descriptor Register (PDR)

The page descriptor registers (PDR) contain information relative to page expansion, page length and access control. There are six sets of eight PDRs which are allocated in the same manner as the PARs. The addresses of these registers are listed in Table 2-38. The format of the PDR is shown in Figure 2-25 and bit descriptions are listed on Table 2-39.



Table 2-38 PAR/PDR Unibus Addresses

Kernel

I Space			D Space		
No.	PAR	PDR	No.	PAR	PDR
0	17 772 340	17 772 300	0	17 772 360	17 772 320
1	17 772 342	17 772 302	1	17 772 362	17 772 322
2	17 772 344	17 772 304	2	17 772 364	17 772 324
3	17 772 346	17 772 306	3	17 772 366	17 772 326
4	17 772 350	17 772 310	4	17 772 370	17 772 330
5	17 772 352	17 772 312	5	17 772 372	17 772 332
6	17 772 354	17 772 314	6	17 772 374	17 772 334
7	17 772 356	17 772 316	7	17 772 376	17 772 336

Supervisor

I Space			D Space		
No.	PAR	PDR	No.	PAR	PDR
0	17 772 240	17 772 200	0	17 772 260	17 772 220
1	17 772 242	17 772 202	1	17 772 262	17 772 222
2	17 772 244	17 772 204	2	17 772 264	17 772 224
3	17 772 246	17 772 206	3	17 772 266	17 772 226
4	17 772 250	17 772 210	4	17 772 270	17 772 230
5	17 772 252	17 772 212	5	17 772 272	17 772 232
6	17 772 254	17 772 214	6	17 772 274	17 772 234
7	17 772 256	17 772 216	7	17 772 276	17 772 236

User

I Space			D Space		
No.	PAR	PDR	No.	PAR	PDR
0	17 777 640	17 777 600	0	17 777 660	17 777 620
1	17 777 642	17 777 602	1	17 777 662	17 777 622
2	17 777 644	17 777 604	2	17 777 664	17 777 624
3	17 777 646	17 777 606	3	17 777 666	17 777 626
4	17 777 650	17 777 610	4	17 777 670	17 777 630
5	17 777 652	17 777 612	5	17 777 672	17 777 632
6	17 777 654	17 777 614	6	17 777 674	17 777 634
7	17 777 656	17 777 616	7	17 777 676	17 777 636

Table 2-39 PDR Bit Descriptions

Bit 15 Cache Bypass - When set to 1 by the program, will cause all references to this page to bypass the cache memory and directly access the main memory.

Bits 14:08 Page Length Field - Specifies the octal number of 32-word blocks in the current page. The block number of the virtual address is compared against the page length field to detect length errors. An error occurs when expanding upwards if the block number is greater than the page length field, and when expanding downwards if the block number is less than the page length field.

Bit 07 - Not used.

Bit 06 Page Written Into - This bit is set to 1 to indicate to the program that the page being accessed has been modified since the PAR or PDR has been loaded. This bit is used in applications that involve disk swapping and memory overlays. It determines which pages have been modified and must be saved in their new form, and which pages have not been modified and can be overlaid and not saved.

Bits 05:04 - Not used.

Bit 03 Expansion Direction - Specifies the direction in which a page is authorized to expand. When cleared to 0, the page expands upward from relative 0 by adding blocks with higher memory addresses. When set to 1, the page expands downward from block number  $178_8$  or  $127_8$  by adding blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.

Bits 02:01 Access Control Field - A two-bit field which defines the access rights for the addressed page as follows:

Bit		Function
02	01	
0	0	Nonresident - abort all accesses
0	1	Read-only - abort all attempts to write
1	0	Unused - abort all accesses
1	1	Read/write - read or write allowed, no trap or abort occurs

Bit 00 - Not used.



CHAPTER 3  
CPU CONFIGURATION

The BA11-AA, -AB mounting box contains a 6 row, 14 column CPU backplane which is dedicated to the PDP-11/44 system modules. Space is provided within the mounting box to allow the installation of additional backplanes.

Some of the system modules, which are installed, contain switches and jumper leads which must be set or configured for particular system applications.

3.1 PROCESSOR BACKPLANE ASSIGNMENTS

Figure 3-1 shows the location of the modules within the system backplane. Row A is positioned toward the rear of the mounting box where the power supply is mounted. The asterisked (\*) modules are optional and not supplied with the basic system. Table 3-1 lists and describes the standard modules supplied with the system and Table 3-2 lists the modules that are available as options.

		ROWS					
		A	B	C	D	E	F
SLOTS	1	M7090 (KD11-Z/CIM)			* M7091	(KE44-A)	
	2			* M7092	(KE44-A)		
	3			* M7093	(FP11-F)		
	4			M7094	(KD11-Z/DATA PATH)		
	5			M7095	(KD11-Z/CONTROL)		
	6			M7096	(KD11-Z/MFM)		
	7			M7097	(CACHE)		
	8			M7098	(KD11-Z/UBI)		
	9			M8722	(MS11-M)		
	10			* M8722	(MS11-M)		
	11			* M8722	(MS11-M)		
	12			* M8722	(MS11-M)		
	13				* SPC		
	14	M9302, * M9202, * BC11-A				* SPC	

FRONT

\* MODULE OPTIONS AVAILABLE (TABLE 3-2)

NOTE:

1. A G 727, G7270 CARD IS REQUIRED IN ROW D OF ANY UNUSED SPC SLOT TO PROVIDE BUS GRANT CONTINUITY.
2. A G7273 CARD IS REQUIRED IN ROW C AND D OF ANY UNUSED SPC SLOT TO PROVIDE BUS GRANT CONTINUITY.
3. MODULES ARE INSERTED WITH COMPONENT SIDE TOWARD RIGHT SIDE OF BACKPLANE.

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Figure 3-1 Backplane, Module Locations

Table 3-1 Standard CPU Backplane Modules

Function	Description
CPU Modules KD11-Z	M7090 - Console Interface Module (CIM)
	M7094 - Data Path Module
	M7095 - Control Module
	M7096 - Multifunction Module (MFM)
	M7097 - Cache Memory Module
	M7098 - Unibus Adapter and Map Module
Memory MS11-MB option	M8722 - 256 KB ECC MOS memory
Unibus	M9302 - Bus Terminator Module

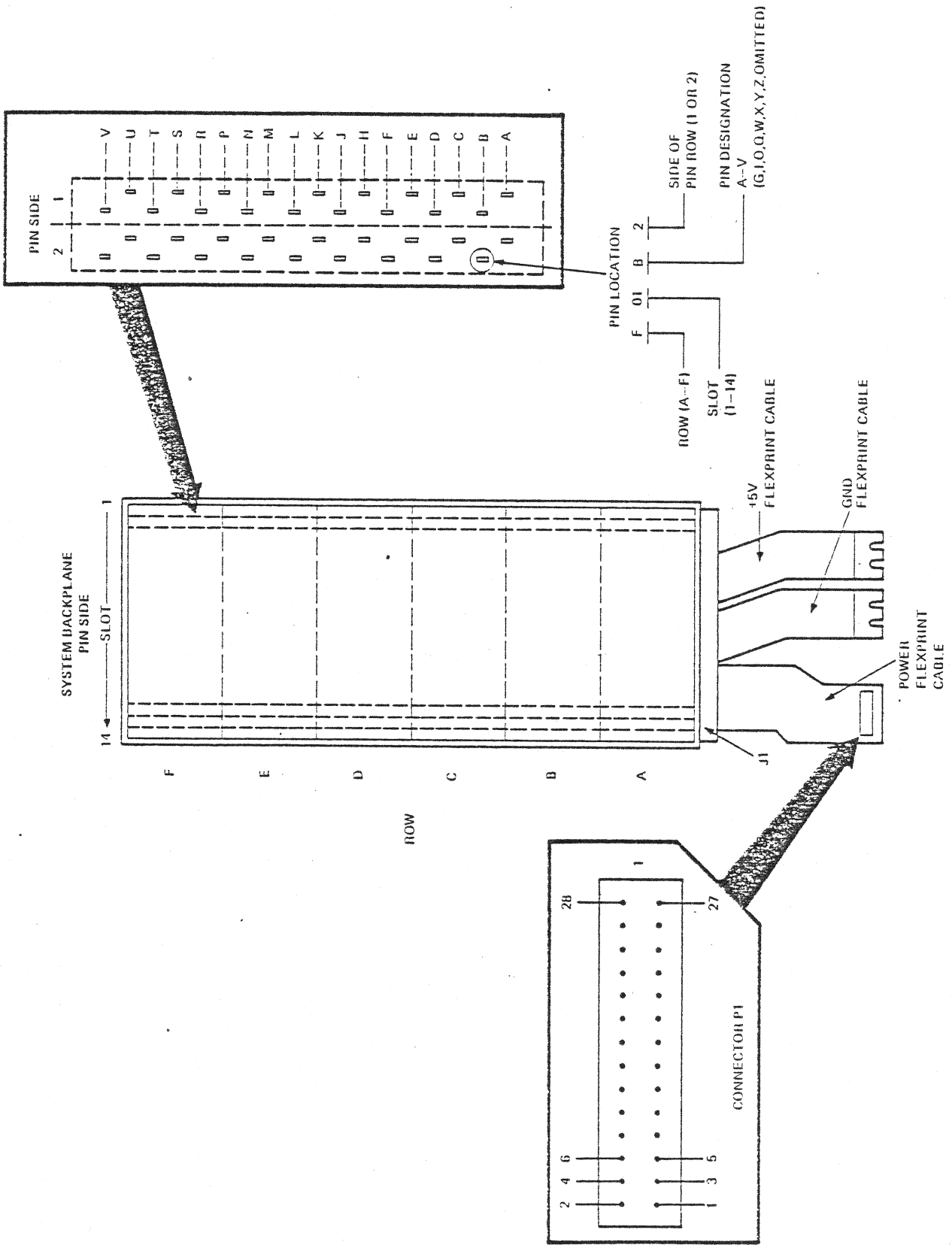
Table 3-2 Optional CPU Backplane Modules

Function	Module
Commercial Instruction Set Processor KE44-A option	M7091 - Control Module
	M7092 - Data Path Module
Floating-Point Processor FP11-F	M7093 - Floating-Point Processor Module
Memory Expansion MS11-MC	Two M8722 modules - a total of 512 KB of ECC MOS memory
	MS11-MD
Unibus Connector	M9202 - connects the CPU Unibus to an additional backplane mounted adjacent to CPU backplane
Unibus Cable Assembly	BC11-A - connects the Unibus of the CPU backplane to a remote backplane
Bus Grant Continuity	G727, G7270, G7273 modules - inserted into unused slots to continue bus grant continuity

### 3.1.1 Backplane Assembly Pin Designations

The system backplane assembly consists of connector blocks mounted to a metal frame. The front of the backplane contains slats into which the module contacts are inserted and the rear of the backplane provides the wire wrap pins. Figure 3-2 shows the wiring side of the system backplane that contains 14 slots (columns) and 6 rows (A-F). With the mounting box tilted to its servicing position, row F will be located at the top of the assembly and slot 1 (column) will be located at the right side when facing the wirewrap pins. Each slot has 36 pins associated with the slot connectors and a pin is identified by the row, slot, pin designation and side of the pin row where it is located as shown.

Table 3-3 lists the voltages and signals supplied by connector P1. Table 3-4 lists the voltages distributed to the connector pins of the backplane and Table 3-5 lists the ground lead distribution.



11-1200

Figure 3-2 Backplane Assembly, Pin Designations

Table 3-3 CPU Backplane Connector P1, Signals and Voltages

Pin	Function
1-10	+5 VB
11-16	+12 VB
17,18	-12 VB
19	LTC
20	BUS ACLO L
21	BOOT ENAB L
22	BUS DCLO L
23	GND SENSE
24	+5 SENSE
25,27	-15
26,28	+15

Table 3-4 CPU Backplane Voltage Distribution

Voltage	Connector Pin
+12	A01R1 A09R1 - A12R1
+12 VB	J1-11 to J1-15
+15	B01C2 C06U1, C12U1 - C14U1 J1-26 to J1-28
+5	A01A2 - A014A2 A01V1 - A08V1 B01A2 - B14A2 C01A2 - C14A2 C01V1 - C08V1 J2-1, J1-24
+5-1	D01A2 - D14A2 D01V1, D02V1 E01A2 - E14A2 F01A2 - F14A2 F01V1 - F08V1
+5B	B01B1, B09B1 - B012B1 B09D1 - B012D1
+5 VB	J1-1 to J1-10
-12	A01S1, A09S1 - A12S1
-12 VB	J1-17, J1-18
-15V	B01T1 C12B2 - C14B2 D12B2 - D14B2 E12B2 - E14B2 F12B2 - F14B2 J1-25, J1-27

Table 3-5 CPU Backplane Ground Distribution

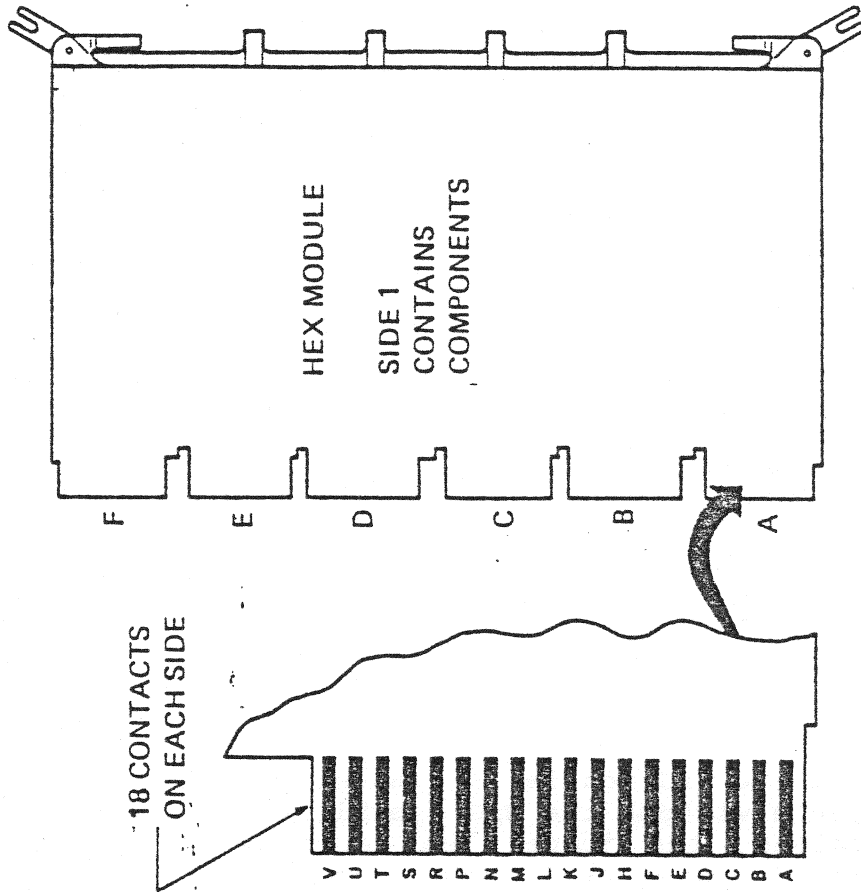
Ground	Connector Pin
GND 01	A01C2, A01T1 B01C1, B01T2 C01C2, C01T1 D01C2, D01T1 E01C2, E01T1 F01C2, F01T1
J00123	
GND 02	A02C2, A02T1 B02C2, B02T1 C02C2, C02T1 E02C2, E02T1 F02C2, F02T1
GND 03	A03C2, A03T1 B03C2, B03T1 C03C2, C03T1 D03C2, D03T1 E03C2, E03T1 F03C2, F03T1
GND 04	A04C2, A04T1 B04C2, B04T1 C04C2, C04T1 D04C2, D04T1 E04C2, E04T1 F04C2, F04T1
GND 05	A05C2, A05T1 B05C2, B05T1 C05C2, C05T1 D05C2, D05T1 E05C2, E05T1 F05C2, F05T1
GND 06	A06C2, A06T1 B06C2, B06T1 C06C2, C06T1 D06C2, D06T1 E06C2, E06T1 F06C2, F06T1
GND 07	A07C2, A07T1 B07C2, B07T1 C07C2, C07T1 D07C2, D07T1 E07C2, E07T1 F07C2, F07T1

Table 3-5 CPU Backplane Ground Distribution (Cont.)

Ground	Connector Pin
GND 08	A08C2, A08T1
	B08C2, B08T1
	C08C2, C08T1
	D08C2, D08T1
	E08C2, E08T1
	F08C2, F08T1
GND 09	A09C2, A09T1
	B09C2, B09T1
	C09C2, C09T1
	D09C2, D09T1
	E09C2, E09T1
	F09C2, F09T1
GND 10	A10C2, A10T1
	B10C2, B10T1
	C10C2, C10T1
	D10C2, D10T1
	E10C2, E10T1
	F10C2, F10T1
GND 11	A11C2, A11T1
	B11C2, B11T1
	C11C2, C11T1
	D11C2, D11T1
	E11C2, E11T1
	F11C2, F11T1
GND 12	A12C2, A12T1
	B12C2, B12T1
	C12C2, C12T1
	D12C2, D12T1
	E12C2, E12T1
	F12C2, F12T1
GND 13	A13C2, A13T1
	B13C2, B13T1
	C13C2, C13T1
	D13C2, D13T1
	E13A1, E13C2, E13T1
	F13C2, F13T1, F13J2
GND 14	A14B2, A14C2, A14N1, A14P1,
	A14R1, A14S1, A14T1, A14V1
	B14B2, B14C2, B14D1, B14E1,
	B14T1, B14V2
	F14C2, F14T1, F14J2

### 3.1.2 Module Contact Designations

Figure 3-3 shows the contact designations for the a hex-height module. The contact designations for single, double and quad height modules will be similar starting with row A and proceeding to the maximum number of rows. When components are mounted on the module, they will be located on side 1.



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NOTES:

1. SIDE 1 IS COMPONENT SIDE
2. EACH SIDE CONTAINS 18 CONTACTS THAT ARE DESIGNATED A-V (OMITTING G,I,O,Q,W,X,Y,Z)
3. A COMPLETE MODULE CONTACT DESIGNATION CONTAINS A CONNECTOR LETTER PREFIX, CONTACT LETTER, AND SIDE SUFFIX NUMBER. FOR EXAMPLE: AD2

Figure 3-3 Module Contact Designations

### 3.1.3 SPC Module Installation

Slot 13, rows A through F and slot 14, rows C through F of the system backplane are allocated to the installation of small peripheral control (SPC) modules. The SPC modules provide control for the transfer of data between the CPU and peripheral devices. Slot 13 can contain a hex-height SPC module and slot 14 can contain a quad-height module. If no module is installed in an SPC slot, a G727 module must be inserted in row D to maintain the bus grant continuity of the backplane.

Some SPC modules allow block data transfers to or from a device without processor intervention. These modules use a nonprocessor grant (NPG) line of the Unibus to initiate the data transfers. The NPG line continuity is maintained by jumper wires wrapped to pins on the backplane.

When a module with NPG capability is installed in an SPC location, the jumper lead between pins A1 and B1 of row C must be removed. Figure 3-4 shows the location of the jumper wires on the backplane.

#### NOTE

When the NPG module is removed or when a module without the NPG capability is installed, the jumper lead must be connected to maintain the signal continuity.

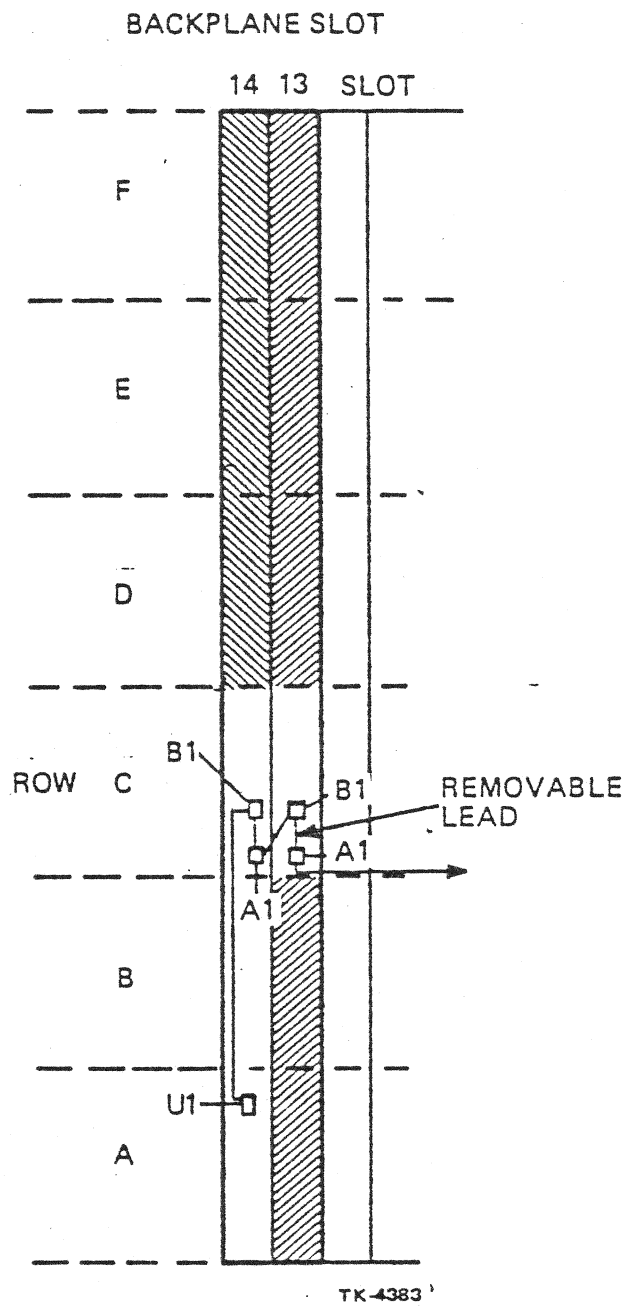


Figure 3-4 SPC Slots, NPG Jumper Lead Locations

Table 3-6 identifies the signals on the connector pins of row C through row D of the SPC locations. The XX designation in the "Pin" column of the table is slot 13 or 14 unless otherwise indicated.

Table 3-6 SPC Location, Signal Identification

Pin	Signal Mnemonics
C (XX) A1	BUS NPG H (IN)
A2	+5 V
B1	BUS NPG H (OUT)
B2	-15 V
C1	BUS PA L
C2	GND
D1	LTC
D2	BUS D15 L
E1	
E2	BUS D14 L
F1	
F2	BUS D13 L
H1	BUS D11 L
H2	BUS D12 L
J1	INT B
J2	BUS D10 L
K1	
K2	BUS D09 L
L1	INT ENB L
L2	BUS D08 L
M1	
M2	BUS D07 L
N1	BUS DCLO L
N2	BUS D04 L
P1	
P2	BUS D05 L
R1	
R2	BUS D01 L
S1	BUS PB L
S2	BUS D00 L
T1	
T2	BUS D03 L
U1	
U2	BUS D02 L
V1	
V2	BUS D06 L
D (XX) A1	
A2	
B1	
B2	
C1	SEL 6
C2	
D1	OUT LOW
D2	BUS BR7 L
E1	SEL 4
E2	BUS BRG L

Table 3-6 SPC Locations, Signal Identification (Cont)

Pin	Signal Mnemonics
F1	SEL 0
F2	BUS BR5 L
H1	IN
H2	BUS BR4 L
J1	SEL 2
J2	BR OUT
K1	OUT H
K2	UBA BG7 OUT H
L1	BUS INIT L
L2	BUS BG7A H
M1	
M2	MFM BG6 OUT H
N1	INT A
N2	BUS BG6A H
P1	
P2	UBA BG5 OUT H
R1	
R2	BUS BG5A H
S1	
S2	MFM BG4 OUT H
T1	
T2	BUS BG4A H
U1	
U2	BG IN
V1	SSYN IN H
V2	BG OUT
E (XX) A1	
A2	
B1	SSYN IN H
B2	
C1	BUS A12 L
C2	
D1	BUS A17 L
D2	BUS A15 L
E1	BUS MSYN L
E2	BUS A16 L
F1	BUS A02 L
F2	BUS C1 L
H1	BUS A01 L
H2	BUS A00 L
J1	BUS SSYN L
J2	BUS CO L
K1	BUS A14 L
K2	BUS A13 L
L1	BUS A11 L
L2	
M1	IN
M2	OUT H
N1	OUT LOW

Table 3-6 SPC Location, Signal Identification (Cont)

Pin	Signal Mnemonics
N2	BUS A08 L
P1	BUS A10 L
P2	BUS A07 L
R1	BUS A09 L
R2	SEL 4
S1	SEL 6
S2	SEL 0
T1	
T2	SEL 2
U1	BUS A06 L
U2	BUS A04 L
V1	BUS A05 L
V2	BUS A06 L
F (XX) A1	BR OUT
A2	
B1	BG IN
B2	
C1	
C2	
D1	BUS BBSY
D2	F13N1 (F14N1)
E1	F13V2 (F14V2)
E2	
F1	
F2	
H1	
H2	INT ENB B
J1	BUS NPR L
J2	
K1	
K2	INT B
L1	
L2	F13L2 (F14L2)
M1	BUS INTR L
M2	F13M2 (F14M2)
N1	F13N1 (F14N1)
N2	
P1	BR OUT
P2	F13P2 (F14P2)
R1	F13L2 (F14L2)
R2	F13N1 (F14N1)
S1	F13M2 (F14M2)
S2	F13P2 (F14P2)
T1	
T2	BUS SACK L
U1	INT A
U2	BR OUT
V1	INT ENB B
V2	F13V2 (F14V2)

### 3.2 MODULE CURRENT REQUIREMENTS

Table 3-7 lists the typical current requirements of the modules which can be inserted into the CPU backplane.

Table 3-7 CPU Module Current Requirements

Option (Modules)	dc Current			
	+5.1 V	+12 V	-12 V	+5.1 BB
KD11-Z				
M7090	0.5A			
M7094	7.5A			
M7095	7.5A			
M7096	5.0A			
M7098	7.0A			
KK11-B (M7097)	6.5A			
FP11-F (M7093)	7.0A			
KE44-A				
M7091	3.1A			
M7092	6.0			
MS11-MB (M8722-BA)	4.8A	1.0A	50mA	1.5A
M9302	1.5A			

### 3.2.1 dc Power Requirements

The H7140-AA, -AB provides the dc power to the modules installed in the CPU backplane and any additional SPU backplane assemblies. The total amount of current available at the dc outputs of the power supply must be considered when installing additional modules to ensure that adequate power is available.

### 3.2.2 H7140-AA, -AB dc Power Output

Table 3-8 lists the total current supplied from the H7140-AA, -AB power supply. The current output of the +5.1 V output is derated by the amount of current required by the +15 V and -15 V outputs according to the following formula:

$$I_{+5.1 \text{ V}} = 120 - 5 [(I_{+15 \text{ V}} - 1) + I_{-15 \text{ V}} - 1]$$

Table 3-8 H7140-AA, -AB Power Supply Maximum Output Current

dc Outputs	Current in (A)
+5.1 V	120
+15 V	3.0
-15 V	3.0
+5.1 BB	10.0 (battery backup)
+12 V	5.0
-12 V	1.0

\* derated by the current drawn at the +15 and -15 V dc outputs

120 A is the maximum current supplied at the +5.1 Vdc output with 1.0A or less drawn from each of the +15 Vdc and -15 Vdc outputs. The minimum current available at the +5.1 Vdc output is 100 A where maximum current of 3 A is supplied at both the -15 Vdc outputs.

Table 3-9 lists some of the Unibus options that are available that are available for use in the PDP-11/44 systems and the typical -15 V and +15 Vdc power requirements of the modules. Refer to the following DIGITAL handbooks for more detailed information on these options.

1. PDP-11 Peripherals Handbook
2. Terminals and Communications Handbook

Table 3-9 -15 V, +15 Vdc Option Power Requirements

Option Designation	Current Requirements (amperes)	
	+15 Vdc	-15 Vdc
DH11-AD	0.40	0.65
DH11-AE	0.10	0.34
DL11-E	0.05	0.15
DL11-WA	0.05	0.15
DL11-WB	0.05	0.15
DMC11-DA	0.03	0.31
DMC11-FA	0.03	0.31
DMC11-MA	0.18	0.46
DMC11-MD	0.18	0.46
DUP11-DA	0.08	0.08
DV11-AA	0.60	1.00
DZ11-A	0.10	0.13
DZ11-B	0.10	0.13
DZ11-C	0.12	0.40
DZ11-D	0.12	0.40
DZ11-E	0.20	0.26
DZ11-F	0.24	0.80
RJM02, RJP06, TJE16, TJU77	0.00	0.40
RK711-PA	0.18	0.40
RL11-AK, RL211-AK	0.50	0.50

### 3.3 MODULE SWITCHES, JUMPERS AND INDICATORS

Several of the modules provided with the PDP-11/44 system contain switches and jumper leads which must be set and configured for specific system requirements. The description of the switch and jumper lead configurations for the memory modules (M8722) is contained in the User's Guide for the MS11-M MOS Memory. Configuration information for the optional modules is contained in the respective documents listed in Table 1-2.

#### 3.3.1 Console Interface Module (M7090)

The CIM Figure 3-5 contains 21 jumper lead locations and a LED indicator. The jumpers are used to select transmission methods for compatibility between the CPU and the console terminal, TU58 DECTape II transport, and the remote diagnostic unit. The jumper leads as shown on Figure 3-5 select R5-232-C transmission mode for SLU1 (console terminal) and SLU2 (DECTape II transport).

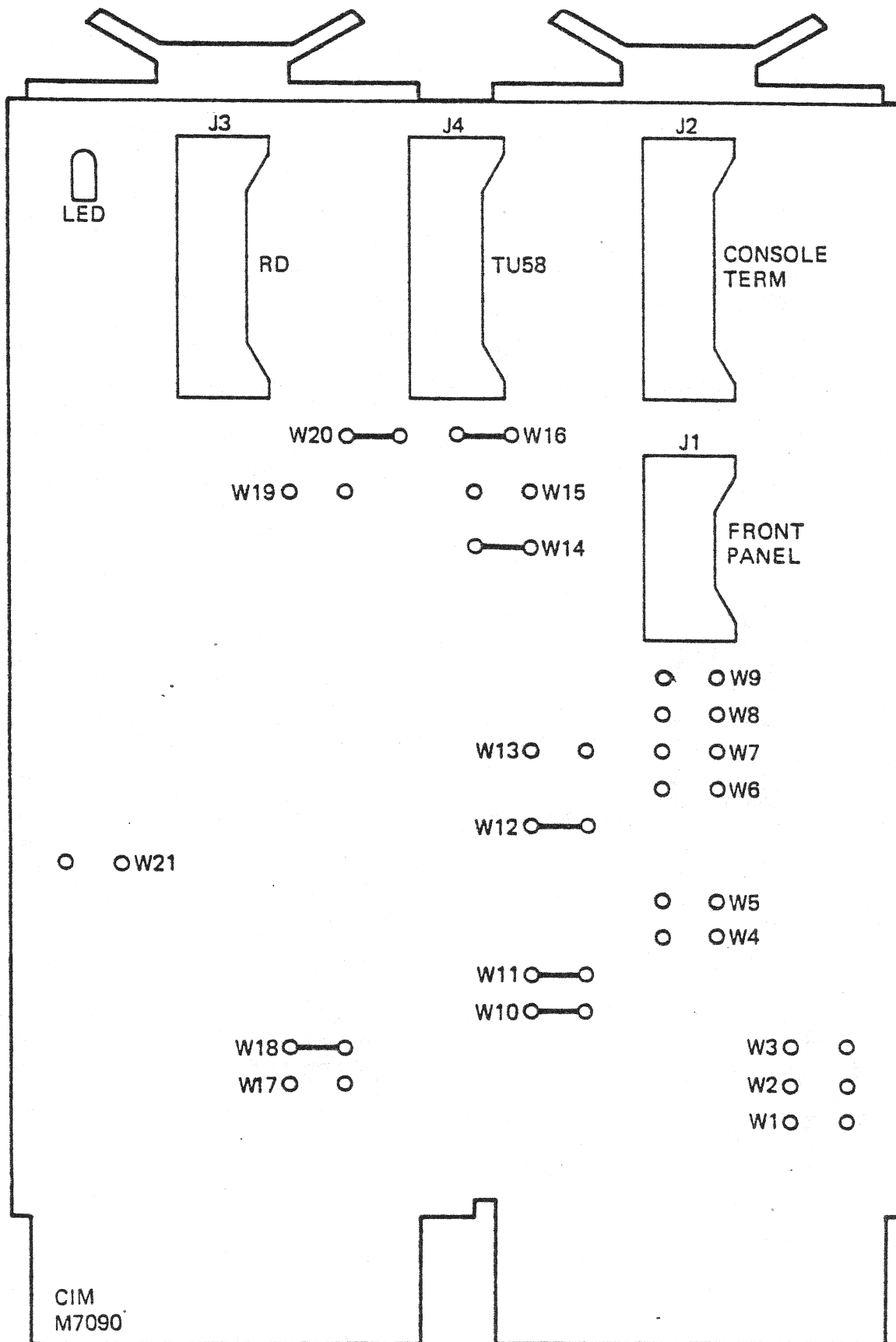


Figure 3-5 CIM Jumper Lead Locations, Connectors and LED Indicator

3.3.1.1 Console Terminal Configurations - The console terminal cable attaches to connector J2. The following methods of data transmission are selectable.

- a. 20 mA current Loop: active or passive mode
- b. Electronic Industries Association (EIA) Standard: RS-232C, RS-423 and RS-422.

Table 3-10 lists the jumper lead configuration for the 20 mA interface and Table 3-11 for the EIA interface.

Table 3-10 Console Terminal Interface 20mA Configuration

Mode	Jumper Leads*											
	W4	W5	W6	W7	W13	W1	W2	W3	W8	W9	W17	W18
<b>Transmitter</b>												
Active	OUT	IN	IN	OUT	IN	IN	OUT	IN	OUT	IN	IN	OUT
Passive	IN	OUT	OUT	IN	OUT	IN	OUT	IN	OUT	IN	IN	OUT
EIA device	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN
<b>Receiver</b>												
Active	IN	OUT	IN	OUT	IN	IN	OUT	IN	OUT	IN	IN	OUT
Passive	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	IN	OUT
EIA device	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN

\* Jumper lead W11 should always be installed except for module testing. When 20mA operation is selected, jumper leads W12, W15, W16, W19 and W20 may remain installed.

Table 3-11 Console Terminal Interface EIA Configuration

Mode	Jumper Leads							
	W12	W15	W16	W17	W18	W19	W20	W1-W9,W13
RS-232C	IN	OUT	IN	OUT	IN	OUT	IN	OUT
RS-423	OUT	OUT	IN	OUT	IN	OUT	IN	OUT
RS-422	OUT	IN	OUT	OUT	IN	IN	OUT	OUT

3.3.1.2 TU58 DECTape II Configuration - The TU58 DECTape II device cable attaches to connector J4 and Table 3-12 lists the jumper lead configuration for selecting the EIA transmission mode.

Table 3-12 TU58 DECTape II, EIA Configuration

Mode	Jumper Lead W14
RS-232C	IN
RS-423	OUT

3.3.1.3 Remote Diagnosis Configuration - The remote diagnosis cable attaches to connector J3. When jumper lead W21 is not installed, the remote diagnostic unit has control of the CPU when the front panel switch is set to either the LOCAL or LOC DSBL position. When jumper lead W21 is installed the remote diagnostic unit cannot take control of the CPU when the front panel switch is in the LOC DSBL position.

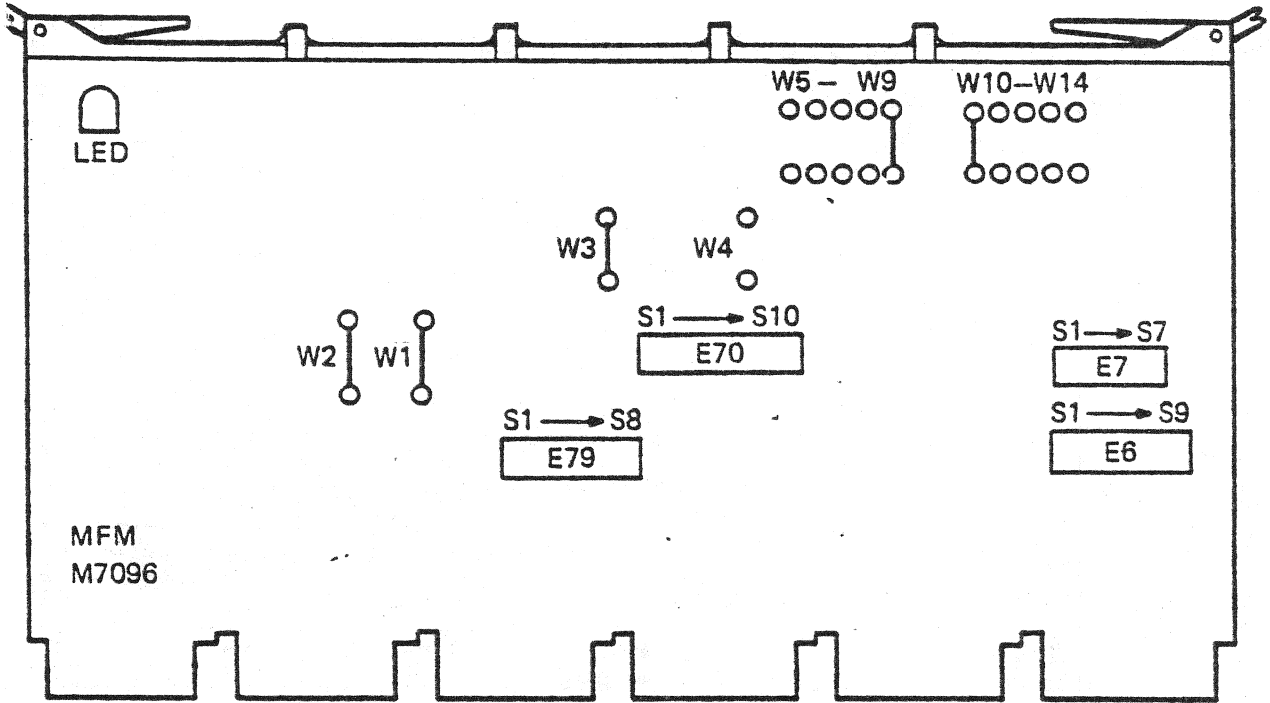
3.3.1.4 Voltage Monitoring - The voltage monitoring circuits detect over or under voltage conditions. Jumper lead W10, when IN, enables the  $\pm 12$  V supply voltages to be monitored. When jumper W10 is OUT, the  $\pm 12$  V supply voltages are not monitored.

3.3.1.5 LED Indicator - The LED indicator is lighted when EIA data transmission to the console terminal has occurred in both directions.

### 3.3.2 Multifunction Module, (M7096)

The multifunction module, Figure 3-6, contains a LED indicator, 14 jumpers lead locations and 4 switchpacks. The LED on the module is a self-test command indicator and is lighted at the beginning of a self-test command and is extinguished after the completion of the test.

3.3.2.1 Console Terminal Jumper Leads Selections - Table 3-13 lists the configuration and functions of the console terminal jumper leads on the multifunction module.



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Figure 3-6 MFM Jumper Lead Locations Switches and LED Indicator

Table 3-14 MFM Console Terminal Baud Rate Selection

	Switch Pack E6			
Receiver Switch Locations	2	3	4	5
Transmitter Switch Locations	6	7	8	9
Baud Rate				
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
200	ON	OFF	ON	OFF
300	ON	OFF	OFF	ON
600	ON	OFF	OFF	OFF
1200	OFF	ON	ON	ON
1800	OFF	ON	ON	OFF
2000	OFF	ON	OFF	ON
2400	OFF	ON	OFF	OFF
3600	OFF	OFF	ON	ON
4800	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON
19200	OFF	OFF	OFF	OFF

3.3.2.3 MFM TU58 DECTape II Jumper Leads - Table 3-15 lists the jumper leads that select the operating parameters of the TU58 DECTape II device.

Table 3-15 MFM TU58 Jumper Lead Configurations

Jumper Lead	Function															
W3	When IN, the receiver error bits (15:12) of the TU58 receiver buffer register are enabled. When OUT, the error bits are read as zero.															
W10	When IN, the break bit (bit 0) of the TU58 transmitter status register is enabled and can be set or cleared. When OUT, the break bit is disabled and will remain clear.															
W11	When IN, TU58 receiver parity detection is enabled and parity will be generated. If W3 is IN, the parity error bit (bit 12) of the TU58 receiver buffer register will be set on a parity error. When W11 is OUT, parity detection and generation is disabled and the parity error bit will remain cleared.															
W12 and W13	These jumpers specify the character length for the TU58 UART, as follows:															
	<table border="0" style="margin-left: 40px;"> <thead> <tr> <th style="text-align: left;">Jumper Leads</th> <th style="text-align: left;">5 bits</th> <th style="text-align: left;">6 bits</th> <th style="text-align: left;">7 bits</th> <th style="text-align: left;">8 bits</th> </tr> </thead> <tbody> <tr> <td>W12</td> <td>IN</td> <td>IN</td> <td>OUT</td> <td>OUT</td> </tr> <tr> <td>W13</td> <td>IN</td> <td>OUT</td> <td>IN</td> <td>OUT</td> </tr> </tbody> </table>	Jumper Leads	5 bits	6 bits	7 bits	8 bits	W12	IN	IN	OUT	OUT	W13	IN	OUT	IN	OUT
Jumper Leads	5 bits	6 bits	7 bits	8 bits												
W12	IN	IN	OUT	OUT												
W13	IN	OUT	IN	OUT												
W14	When IN, odd parity will be generated and checked, if jumper W11 is also IN. When W14 is OUT, even parity will be generated and checked, if jumper W11 is IN.															

3.3.2.4 MFM TU58 Baud Rate Selection - Switches S1 through S6 of switch pack E7 are used to select the baud rates of the TU58 transmitter and receiver. The location of E7 is shown on Figure 3-6. Switch S7 of E7 selects the stop bit: ON is one stop bit and OFF is two stop bits. The OFF position will also select 1.5 stop bits if a five-bit character is selected by jumper leads W12 and W13 (Table 3-15). Switch position, S2 through S6 should only be set to the combinations shown in Table 3-16. The baud rate for the transmitter and receiver can be different.

Table 3-16 TU58 Baud Rate Selection

Receiver Switch	Switch pack E7 *		
	1	2	3
Transmitter Switch	4	5	6
Baud Rate			
38,400	ON	OFF	OFF
9600	OFF	ON	OFF
Same baud rate as selected for the console terminal	OFF	OFF	ON

\* Switch S7 is not used

3.3.2.5 MFM TU58 Device Address Selection - Switch pack at locations E70 contains switches S1 through S10 and is used to select the base address of the TU58 DECTape II device from 17760000 to 17777777. Figure 3-7 shows the address bits effected by the switch settings. An example of the switch positions required to set the TU58 address to 17776500 is as follows:

3.3.2.6 TU58 Vector Address Selection - Switch pack at location E79 contains switches S1 through S8. Switch S1 when ON enables the TU58 address to be decoded. Switch S2 is related to console terminal operation. Switches S3 through S8 are used to set the TU58 vector address from 0 to 770 (octal). The recommended vector address for use with Digital software is 300. The transmitter vector equals the receiver vector plus 4. Figure 3-8 shows the correspondence between the switch positions and the TU58 vector address.

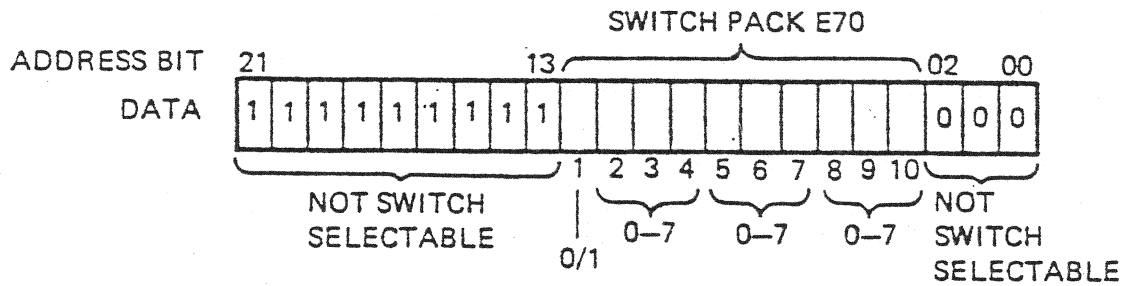
An example of the switch positions required to select a vector address of 300 is as follows:

S8 to S6 = Off  
 S5, S4 = On  
 S3 = Off

3.3.2.7 Line Time Clock Enable/Disable - Jumper lead location W2 on the MFM module controls the operation of the line time clock as listed on Table 3-17.

Table 3-17 Line Time Clock Operation

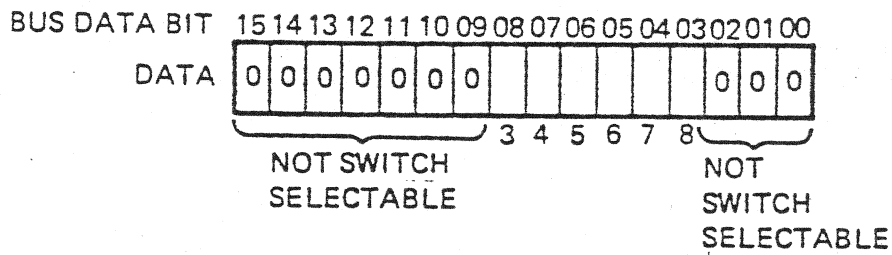
W2	Line Time Clock Address
IN	Enable decode
OUT	Disable decode



SWITCH ON= LOGICAL 1, OFF= LOGICAL 0

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Figure 3-7 TU58 Device Address Selection



SWITCH ON = LOGICAL 1, OFF = LOGICAL 0

NOTE: DATA BIT # 2 IS 0 FOR RECEIVER VECTOR AND 1 for TRANSMITTER VECTOR

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Figure 3-8 TU58 Vector Address Selection

### 3.3.3 Unibus Interface Module (M7098)

The Unibus interface (UBI) module shown on Figure 3-9 contains 14 jumper lead locations and one switch pack at location E28.

3.3.3.1 UBI Jumper Leads and Memory Page Selection - Table 3-18 lists the function of the jumper leads on the UBI module

Table 3-18 UBI Module Jumper Lead Functions

Jumper Lead	Function
W1	When IN, enables parity error abort
W2	When IN, enables diagnostic ROM
W3-W7	Unibus map page number, upper limit
W8-W12	Unibus map page number, lower limit
W17,W18	Always IN

Jumpers leads W12-W8 and W7-W3 specify the lower and upper limit, respectively, of a set of Unibus addresses not mapped to main memory (asserted on the Unibus only). Except for the I/O page, every Unibus address not in this set is mapped to main memory (asserted on the memory bus) by the Unibus map. Devices on the Unibus should be addressed only in unmapped or I/O page address space.

When the upper and lower limits are set to the same octal (page) number, every non- I/O page address is mapped to memory.

Table 2-19 lists the jumper leads selections for the lower limit of the set of unmapped addresses. Unibus addresses from zero just below this limit are mapped to main memory. The octal number in this table is the first bank of the unmapped set except when the lower and upper limits are set to the same bank number in which case only the I/O page is unmapped.

Table 2-20 lists the jumper selections for the upper limit of the set of unmapped addresses. Unibus addresses above this limit and below 760 000 are mapped to main memory. The octal bank number in this table is the first mapped bank after the unmapped set except when it is bank 37, the I/O page (always unmapped).

Table 3-20<sup>19</sup> Unibus Map Jumper Leads, Lower Limit

LOWEST ADDRESS IN UNMAPPED SET	DECIMAL WORDS	OCTAL BANK	J U M P E R L E A D S				
			W12	W11	W10	W9	W8
NONE	124	37	OUT	OUT	OUT	OUT	OUT
740 000	120	36	IN	OUT	OUT	OUT	OUT
720 000	116	35	OUT	IN	OUT	OUT	OUT
700 000	112	34	IN	IN	OUT	OUT	OUT
660 000	108	33	OUT	OUT	IN	OUT	OUT
640 000	104	32	IN	OUT	IN	OUT	OUT
620 000	100	31	OUT	IN	IN	OUT	OUT
600 000	96	30	IN	IN	IN	OUT	OUT
560 000	92	27	OUT	OUT	OUT	IN	OUT
540 000	88	26	IN	OUT	OUT	IN	OUT
520 000	84	25	OUT	IN	OUT	IN	OUT
500 000	80	24	IN	IN	OUT	IN	OUT
460 000	76	23	OUT	OUT	IN	IN	OUT
440 000	72	22	IN	OUT	IN	IN	OUT
420 000	68	21	OUT	IN	IN	IN	OUT
400 000	64	20	IN	IN	IN	IN	OUT
360 000	60	17	OUT	OUT	OUT	OUT	IN
340 000	56	16	IN	OUT	OUT	OUT	IN
320 000	52	15	OUT	IN	OUT	OUT	IN
300 000	48	14	IN	IN	OUT	OUT	IN
260 000	44	13	OUT	OUT	IN	OUT	IN
240 000	40	12	IN	OUT	IN	OUT	IN
220 000	36	11	OUT	IN	IN	OUT	IN
200 000	32	10	IN	IN	IN	OUT	IN
160 000	28	7	OUT	OUT	OUT	IN	IN
140 000	24	6	IN	OUT	OUT	IN	IN
120 000	20	5	OUT	IN	OUT	IN	IN
100 000	16	4	IN	IN	OUT	IN	IN
60 000	12	3	OUT	OUT	IN	IN	IN
40 000	8	2	IN	OUT	IN	IN	IN
20 000	4	1	OUT	IN	IN	IN	IN
0	0	0	IN	IN	IN	IN	IN

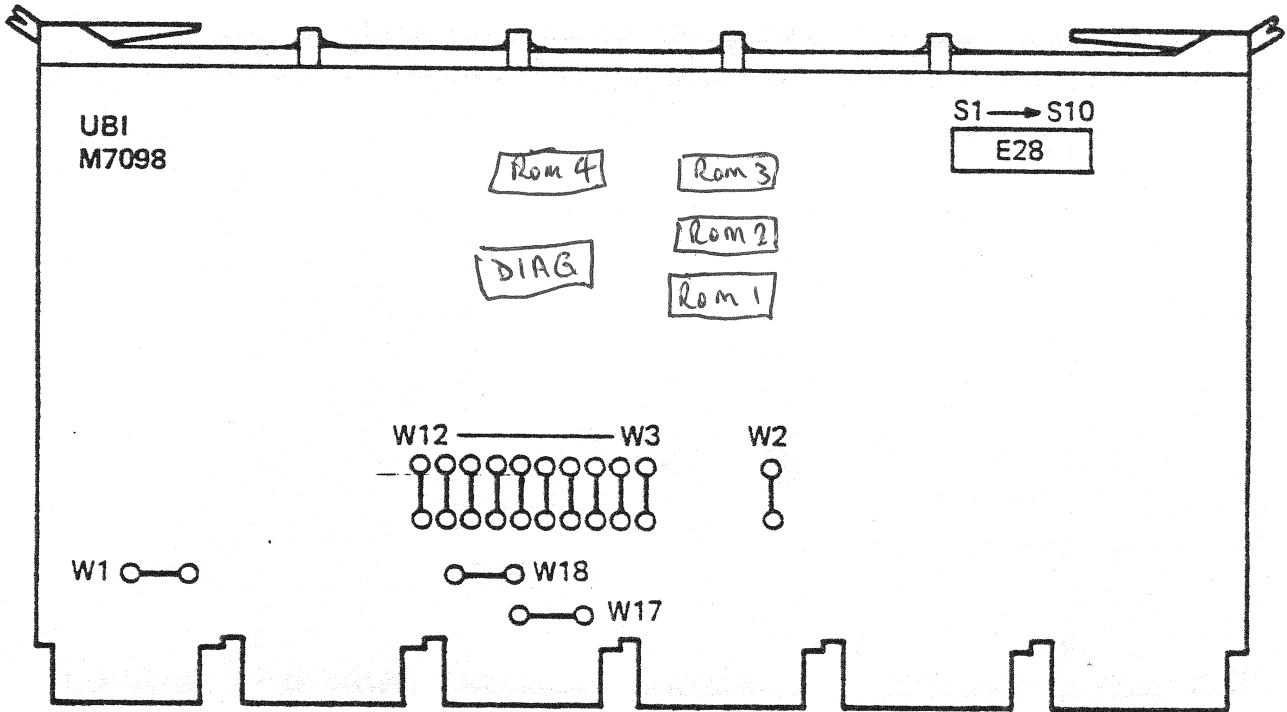
The following example describes the jumper selections for 3 pages (12 decimal K words) of Unibus device addresses immediately following the I/O page.

1. Page (bank) 37 is the I/O page therefore the three pages to be unmapped are 34, 35, and 36.
2. Read jumper settings for W12 through W8 from the lower limit Table 3-19 at bank 34, the first unmapped bank: W12=IN, W11=IN, W10=OUT, W9=OUT, and W8=OUT.
3. Read jumper settings for W7 through W3 from the upper limit Table 3-20 at bank 37, the next bank after the unmapped set desired (34, 35, and 36): W7=OUT, W6=OUT, W5=OUT, W4=OUT, and W3=OUT.

Notice that the upper limit "Decimal KW" amount minus the lower limit "Decimal KW" amount is equal to 12KW. This is the size of the area desired.

20  
Table 3-19 Unibus Map Jumper Lead, Upper Limit

HIGHEST ADDRESS IN UNMAPPED SET	DECIMAL WORDS	OCTAL BANK	J U M P E R				
			W7	W6	W5	W4	W3
757 777	124	37	OUT	OUT	OUT	OUT	OUT
737 777	120	36	IN	OUT	OUT	OUT	OUT
717 777	116	35	OUT	IN	OUT	OUT	OUT
677 777	112	34	IN	IN	OUT	OUT	OUT
657 777	108	33	OUT	OUT	IN	OUT	OUT
637 777	104	32	IN	OUT	IN	OUT	OUT
617 777	100	31	OUT	IN	IN	OUT	OUT
577 777	96	30	IN	IN	IN	OUT	OUT
557 777	92	27	OUT	OUT	OUT	IN	OUT
537 777	88	26	IN	OUT	OUT	IN	OUT
517 777	84	25	OUT	IN	OUT	IN	OUT
477 777	80	24	IN	IN	OUT	IN	OUT
457 777	76	23	OUT	OUT	IN	IN	OUT
437 777	72	22	IN	OUT	IN	IN	OUT
417 777	68	21	OUT	IN	IN	IN	OUT
377 777	64	20	IN	IN	IN	IN	OUT
357 777	60	17	OUT	OUT	OUT	OUT	IN
337 777	56	16	IN	OUT	OUT	OUT	IN
317 777	52	15	OUT	IN	OUT	OUT	IN
277 777	48	14	IN	IN	OUT	OUT	IN
257 777	44	13	OUT	OUT	IN	OUT	IN
237 777	40	12	IN	OUT	IN	OUT	IN
217 777	36	11	OUT	IN	IN	OUT	IN
177 777	32	10	IN	IN	IN	OUT	IN
157 777	28	7	OUT	OUT	OUT	IN	IN
137 777	24	6	IN	OUT	OUT	IN	IN
117 777	20	5	OUT	IN	OUT	IN	IN
77 777	16	4	IN	IN	OUT	IN	IN
57 777	12	3	OUT	OUT	IN	IN	IN
37 777	8	2	IN	OUT	IN	IN	IN
17 777	4	1	OUT	IN	IN	IN	IN
NONE	0	0	IN	IN	IN	IN	IN



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Figure 3-9 UBI Module, Switch and Jumper Lead Locations

E28

S1 OFF  
 S2 ON  
 S3-6 OFF  
 S7 ON  
 S8-10 OFF

165020 start address  
 normal settings

3.3.3.2 Diagnostic and Bootstrap Loader ROMs -- The UBI module contains a CPU diagnostic ROM and provides four 16-pin DIP sockets for the installation of device bootstrap loader ROMs. The CPU diagnostic ROM checks the performance of the central processor and main memory when power is initially applied to the system or when a device bootstrap loader is initiated.

The device bootstrap loader ROMs contain device independent programs that will load device programs from a selected peripheral device into main memory. The number and type of ROMs that are installed is dependent upon the devices included in the system. A bootstrap loader program is initiated by the operator from the console terminal, when selected by the BOOT position of the toggle switch on the front panel, or when requested by a device. The processor executes the bootstrap loader directly without the operator keying in the initial program.

Table 3-21 lists the location of the CPU diagnostic and bootstrap loader ROMs and the starting addresses associated with each. The selection of the first device starting address determines whether the CPU diagnostic will be performed when the bootstrap program is enabled. The second devices listed on the table are for selecting a second device bootstrap program contained in the same ROM as the first device bootstrap program. Switches S1 through S10 at location E28 of the UBI module select the starting address of the bootstrap loading program. Switch S1 determines the starting address of the upper three digits as follows:

S1 = ON (765 XXX) (device bootstrap program)  
S1 = OFF (775 XXX) (CPU diagnostic program)

Switch S2 controls the execution of the CPU diagnostic program and the device internal bootstrap program as follows:

S2 = ON (bootstrap/diagnostic enabled)  
S2 = OFF (bootstrap/diagnostic disabled)

Switches S3 through S10 are bits <08:01> of the starting address.

Table 3-21 CPU Diagnostic and Bootstrap Loader, ROM Addresses

ROM Location	CPU Diagnostic	First Device Address	S1 <1:10>	
			Second Device Address	Second Device
			23-755A9	23-764A9
CPU Diagnostic	No	2004		
	Yes	2006		
Device #1	No	0004	0050	0034
	Yes	0006	0052	0036
Device #2	No	0204	0250	0234
	Yes	0206	0252	0236
Device #3	No	0404	0450	0434
	Yes	0406	0452	0436
Device #4	No	0604	0650	0634
	Yes	0606	0652	0636

The position of the bootstrap ROMs on the module must be sequential, starting with BT1 and progressing to BT4 as listed on Table 3-22. The IC location is indicated on the module etch.

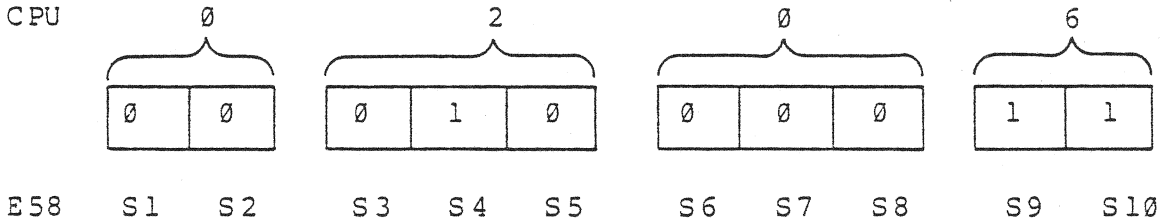
Table 3-22 Bootstrap ROM Locations

IC Location	Bootstrap ROM
E48	Device 1
E49	Device 2
E50	Device 3
E59	Device 4

To select an RL01 installed in the second ROM location (E49) and run the CPU diagnostic program, set the switches as described in the following example:

Example:

RL01 ROM in location E49  
Run, diagnostics and then boot RL01



0 = Off  
1 = On

Table 3-23 lists the part numbers for the available bootstrap ROMs. Some of the ROMs contain more than one device program. The bootstrap loaders for the communication devices DL11, DMC-11, DU11 and DUP-11 are supplied in three ROMs for each device.

Table 3-23 Device ROM Part Numbers

Device	ROM Part Number
ASR33	23-760A9
DL11	23-926A9 23-927A9 23-928A9
DMC-11	23-862A9 23-863A9 23-864A9
DU11	23-868A9 23-869A9 23-870A9
DUP-11	23-865A9 23-866A9 23-867A9
PC05	23-760A9
RK03/05	23-756A9
RK06/07	23-752A9
RL01	23-751A9
RP02/03	23-755A9
RP04/05/06	23-755A9
R503/04	23-759A9
RX01	23-753A9
RX02	23-811A9
TS04	23-764A9
TU10, TE10, TS03	23-758A9
TU16, 45, 77, TE16	23-757A9
TU55/56	23-756A9
TU58	23-765A9
TU60	23-761A9

### 3.3.4 Cache Memory Module (M7097)

The cache memory module is shown on Figure 3-10 and contains three LED indicators, two toggle switches and two jumper lead locations.

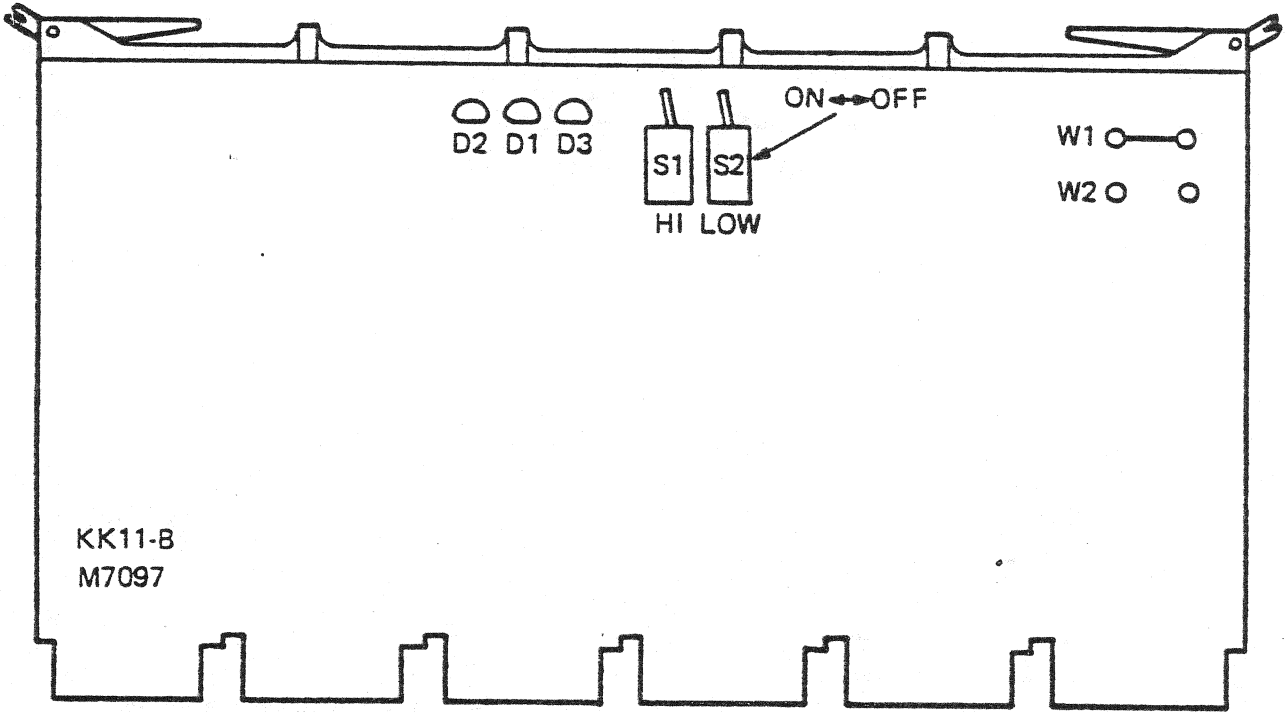
3.3.4.1 LED Indicator Functions - Table 3-24 lists the function of the LED indicators.

Table 3-24 Cache Module, LED Indicator Functions

LED	Function
D 3	Parity Error
D 1	Hit
D 2	Address Match

3.3.4.2 Multiport Memory Selection - Jumpers W1 and W2 are provided to accommodate multiported memory. In the PDP-11/44 (without multiported memory), jumper W1 should be IN and jumper W2 should be OUT. In systems using multiport memory, jumper W1 is OUT and jumper W2 is IN.

Switches S1 and S2, when ON, will force misses to the high and low cache address space, respectively. The ON position is when the switch is positioned to the left toward the LED indicators.



TK-3635

Figure 3-10 Cache Memory Module, Switches, LED Indicators and Jumper Lead Locations

The PDP-11/44 and PDP-11/X44 systems and peripheral devices can be operated in most contaminant free environments such as offices, laboratories or light manufacturing areas; however, to ensure reliable operation, certain environmental conditions are recommended.

#### 4.1 SITE CONSIDERATIONS

The computer equipment should be operated in an environment that is controlled by an air-conditioning system. The air-conditioning system should provide temperature controlled, filtered air at the specified levels of humidity. The air-conditioner should also increase the air pressure in the computer area to prevent the infiltration of dust and other contaminants from adjacent areas if they exist.

The air-conditioning equipment should conform to the requirements of the Standard for the Installation of Air-Conditioning and Ventilating Systems (Non-Residential), N.F.P.A. No. 90A, as well as the requirements of the Standard for Electronic Computer Systems, N.F.P.A. No. 75.

##### 4.1.1 Temperature and Humidity

Temperature cycling and thermal gradients can induce changes in materials which will affect the performance of the system. High temperatures also increase the rate of deterioration of materials. An environment of high absolute humidity can cause dimensional changes in paper tapes, line printer papers and cards. Low humidity can produce static electricity, which results in dust accumulation on magnetic tape and disk devices which will adversely affect the system operation.

The PDP-11/44 systems are designed to operate in a temperature range of 5° C (41° F) to 50° C (122° F) at a relative humidity of 10 to 95% without condensation. System configurations that use I/O devices, such as magnetic tape units, card readers, disks, etc., require an operational temperature range from 10° C (50° F) to 40° C (104° F) at a relative humidity of 40 to 66% without condensation. The nominal operating conditions for a system configuration are a temperature of 20° C (70° F) and a relative humidity of 45%.

#### 4.1.2 Acoustical Dampening

Some peripheral devices such as character printers, line printers and magnetic tape transports generate noise when operating. When many of these units are located in an area, sound absorbent materials may be used to reduce the noise level. Sound absorbent ceiling materials are available and antistatic carpets may be installed. In addition, the wall areas may be covered with drapes or other suitable materials which will reduce the reflected noise levels.

#### 4.1.3 Lighting

When video displays (CRTs) are used with the system a reduced lighting level at the site will prevent excessive reflection from the face of the CRT and enable the display to be more easily viewed by the operator. The light levels may be controlled by dimmers or by the installation of translucent materials between the light source and the surrounding areas.

#### 4.1.4 Static Electricity

The PDP-11/44 and related cabinets should be adequately grounded to prevent the effects of static electricity from interfering with the equipment operation. The static charges generated can be reduced by ensuring that the relative humidity of the room is at the specified 45% nominal value. Antistatic carpeting is also available to minimize the static charges generated. When raised floors are used at the computer installation, the framing of the floor panels should be adequately grounded.

#### 4.1.5 Shock and Vibration

When the PDP-11/44 units are to be installed at locations which are subjected to excessive shock and vibration, special cabinet mounting hardware may be required. Contact a local DIGITAL sales representative for information related to special environmental conditions.

#### 4.1.6 Electrical Interference

Several types of electrical interference may be indigenous to the site location and may require special filtering to prevent equipment malfunctions.

The interference transmitted through the air is electromagnetic interference (EMI) and may be caused by TV and radio waves, radar transmissions, lightning discharges, ignition systems and power line transmissions. Interference may also be transmitted through the ac power lines. If the interference is suspected to be causing problems with the operation of the equipment, shielding may be required, or filtering of the ac power to the site. Contact your local DIGITAL sales office or field service representative for information related to interference problems.

## 4.2 UNPACKING

The system equipment, associated devices and cabinets are packaged and shipped in reinforced cartons and protected internally by foam inserts and poly bags. Accessories and supplies such as documentation, magnetic tape or disks and connecting cables and hardware are packaged in separate containers. Before unpacking any carton, remove the packing list from the container and check to ensure that the items ordered are listed. When the items are unpackaged, use the list to check that all the items are contained in the package. The unpacking information for consoles, printers, disk drives and magnetic tape is contained in the user's guide supplied with each device.

### NOTE

Retain the packaging materials and shipping containers in the event that reshipping is required.

#### 4.2.1 PDP-11/44-CA, -CB Unit Removal

The PDP-11/44-CA and CB units are packaged in reinforced cartons and protected by foam inserts and by a poly bag as shown on Figure 4-1. To remove the unit from the container, perform the following procedure.

### CAUTION

The PDP-11/44-CA, -CB units weigh approximately 75 lbs (34 kg). Use care when lifting the unit from the carton.

1. Open the leaves of the outer carton by cutting the tapes at the seams.
2. Remove the inner carton from the foam protector.
3. Open the leaves of the inner carton by cutting the tape at the seams.
4. Remove the side and rear protectors.
5. Remove the unit from the poly bag.
6. Remove the bezel protector.
7. Inspect the unit for visible damage and to ensure that the contents are complete.

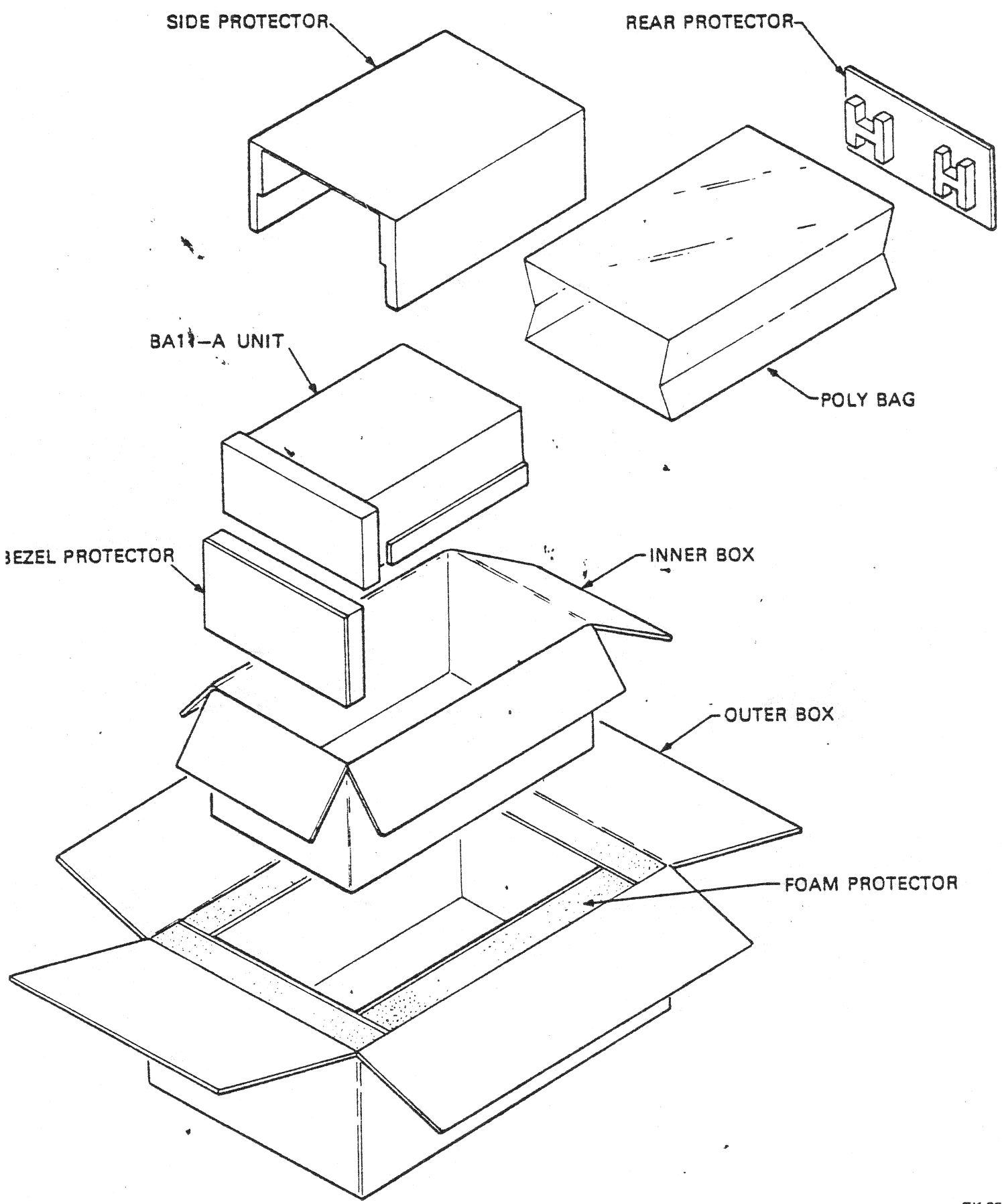


Figure 4-1 PDP-11/44 Unit Unpacking  
4-4

#### 4.2.2 PDP-11/X44-CA, -CB Cabinet Removal

The PDP-11/X44-CA, -CB units are attached to a wooden base, covered with a poly bag and enclosed by a carton as shown on Figure 4-2. To remove the unit, perform the following procedures.

1. Cut the polyester straps used to secure the carton and unit to the base.
2. Slide the carton up and away from the unit.
3. Remove the poly bag from the unit.
4. Remove the bolts that hold the bottom of the unit to the wooden base.
5. Remove the unit from the wooden base and set the unit in its operating location.
6. Attach the stabilizer feet to the bottom of the unit.

CARTON SEALING TAPE

HALF SLOTTED CARTON WITH  
BOTTOM FLANGE

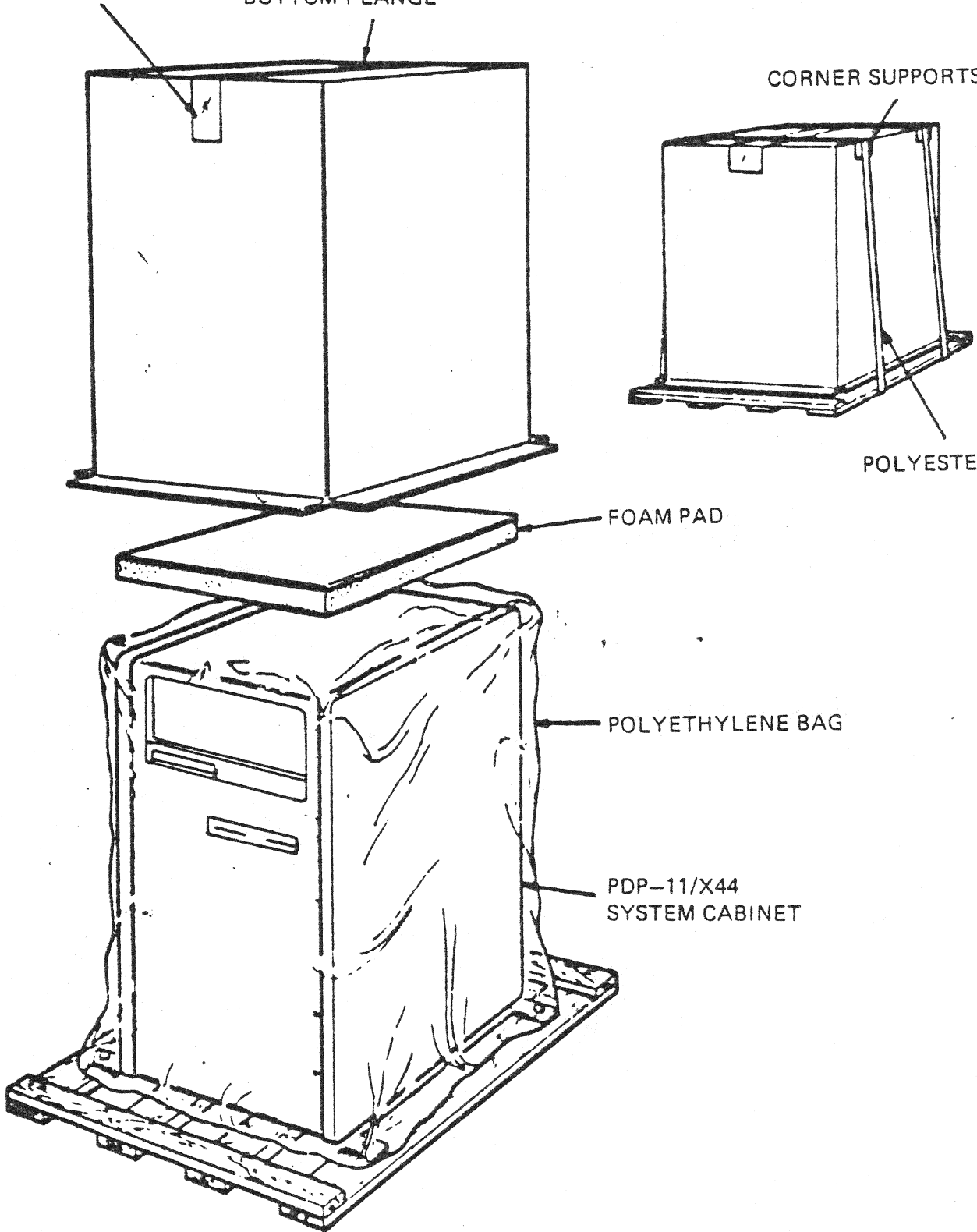
CORNER SUPPORTS

POLYESTER STRAP

FOAM PAD

POLYETHYLENE BAG

PDP-11/X44  
SYSTEM CABINET



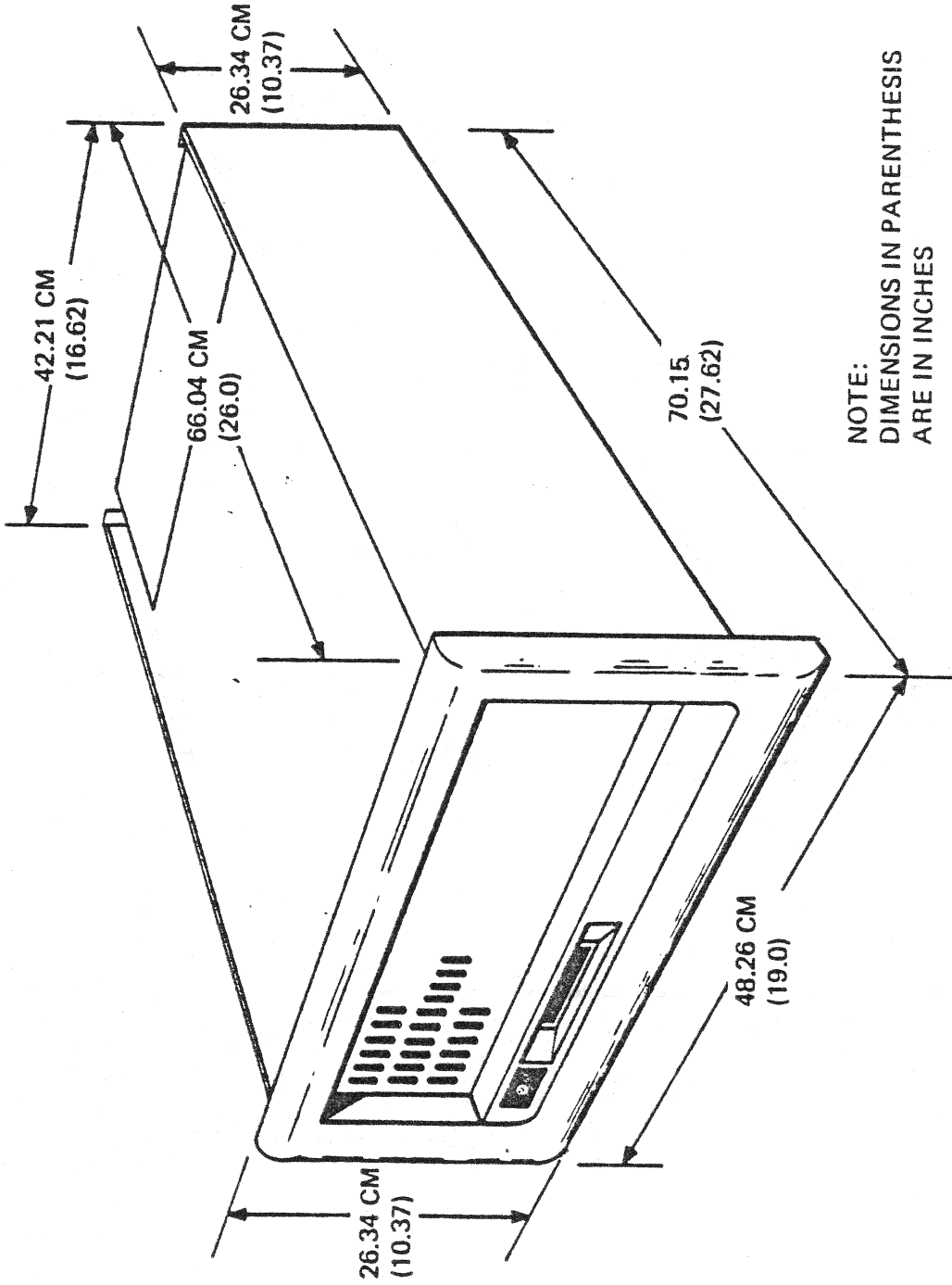
TK-4385

Figure 4-2 PDP-11/X44 Cabinet Unpacking

### 4.3 EQUIPMENT DIMENSIONS

Figure 4-3 shows the overall dimensions of the PDP-11/44 unit. The unit will occupy a 10 1/2 inch vertical space within a rack or cabinet.

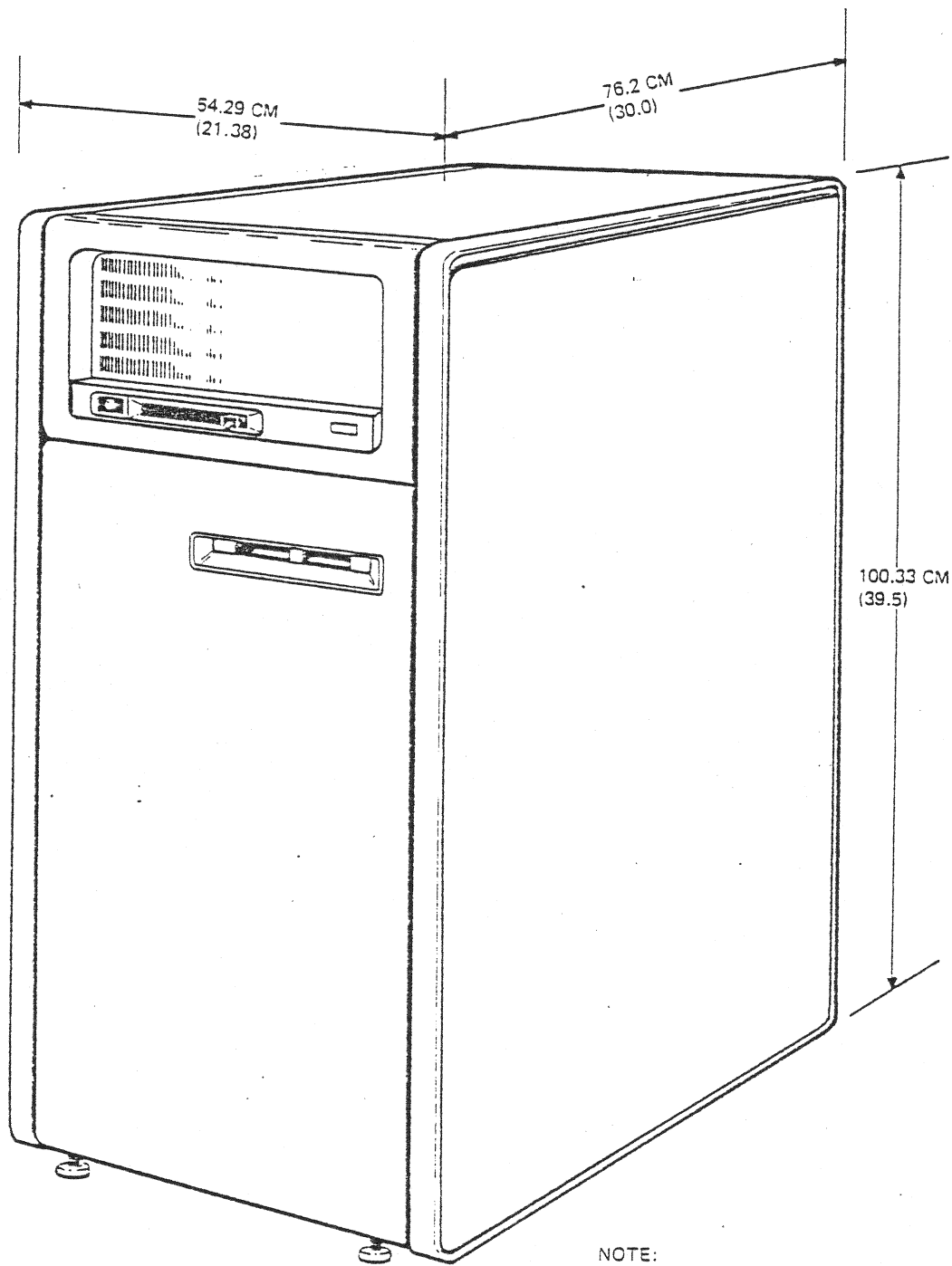
Figure 4-4 shows the overall dimensions of the PDP-11/X44 unit. This system is enclosed within a standard system cabinet. When additional units are included in the system configuration, refer to the respective user's guide for the space requirements of each cabinet.



NOTE:  
DIMENSIONS IN PARENTHESIS  
ARE IN INCHES

TK-4384

Figure 4-3 PDP-11/44 Unit Dimensions



NOTE:  
DIMENSIONS IN PARENTHESES  
ARE IN INCHES

TK-4326

Figure 4-4 PDP-11/X44 System Cabinet Dimensions

#### 4.4 ac INPUT POWER REQUIREMENTS

The ac input power to the PDP-11/44 system equipment should be supplied by a separate power circuit which is dedicated only to the system.

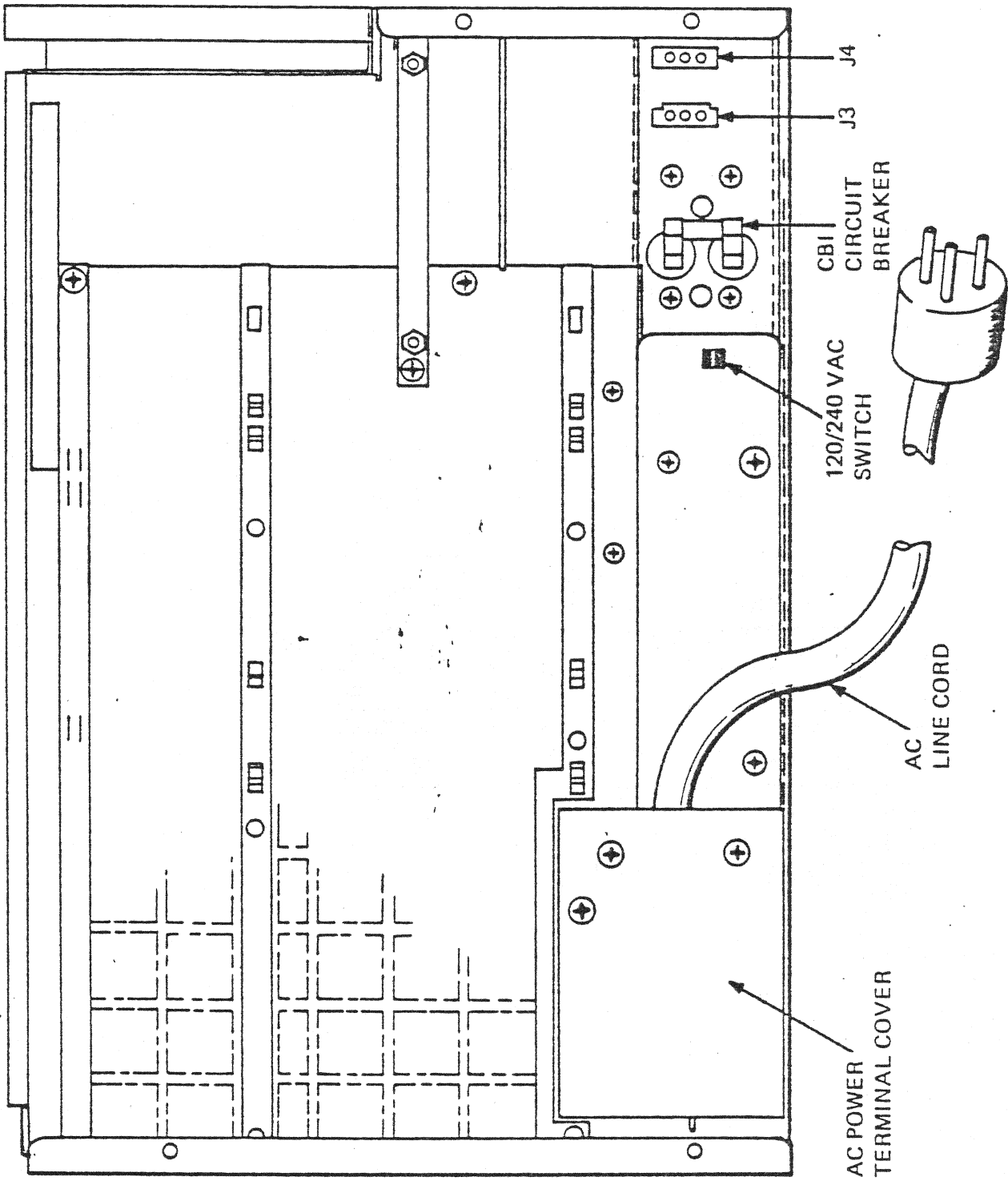
Table 4-1 lists the power requirements for the four basic system configurations. Any additional equipment installed into the cabinet of the PDP-11/X44-CA, -CB system or modules installed into the mounting box may increase the power consumption. Refer to the respective user's guide for the power requirements of the peripheral devices that are supplied with the system.

Table 4-1 System ac Input Power Requirements

System Designation	AC Voltage Tolerance	Frequency Tolerance	Phases(s)	Steady State Current (RMS)	Surge Current	Surge Duration
PDP-11/44-CA	90-128V	47-63Hz	1	16A rms max	65A peak	1/2 cycle
PDP-11/X44-CA						
PDP-11/44-CB	180-256V	47-63Hz	1	9.5A rms max	130A peak	1/2 cycle
PDP-11/X44-CB						

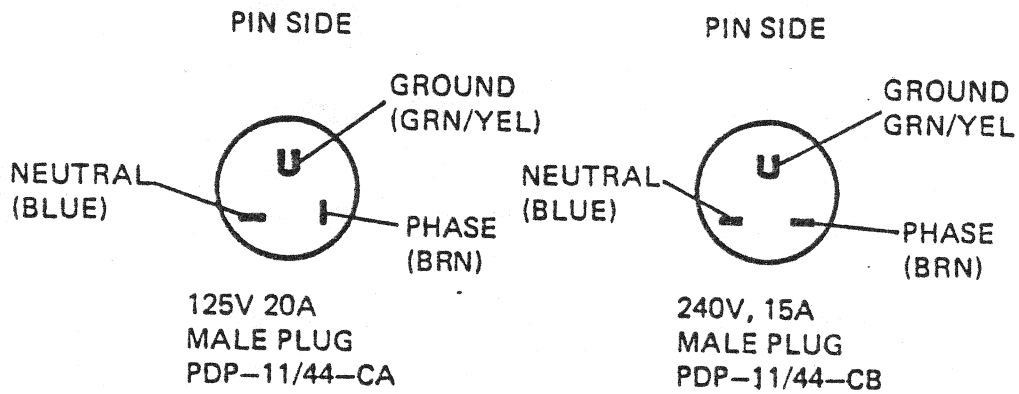
#### 4.4.1 Power Connections (ac)

The PDP-11/44-CA, -CB units are supplied with a 9 ft (2.74 m) line cord attached to the rear of the unit. Figure 4-5 shows the ac line cord circuit breaker and connectors. The line cord plug may be connected to an 872-D, -E power controller unit (or equivalent) or directly to the ac power receptacle at the site location. Figure 4-6 shows the type of connector plugs and receptacles used and the DIGITAL part numbers for the connectors. The color of the cable wires connected to the plug is also indicated. The NEMA 5-20 P plug is attached to the PDP-11/44-CA (120 Vac) cable and the NEMA 6-15 P is attached to the PDP-11/44-CB cable. The NEMA 5-20 R and 6-15 R are dual receptacle outlets which can be installed within a wall outlet box or a power distribution unit.



TK-4389

Figure 4-5 Mounting Box, Rear Panel Components



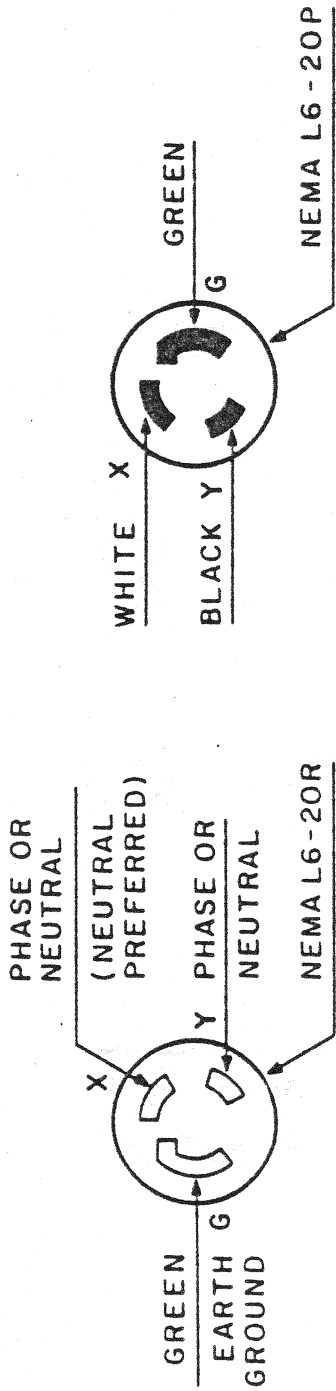
NEMA * DESIGNATION	POWER RATING	DIGITAL PART NO.
5-20 P	125V, 20A	12-15183-00
5-20 R **		12-12265-00
6-15 P	240V, 15A	90-08853-00
6-15 R **		12-11204-01

- \* P = PLUG
- R = RECEPTACLE
- \*\* DUAL RECEPTACLE OUTLET

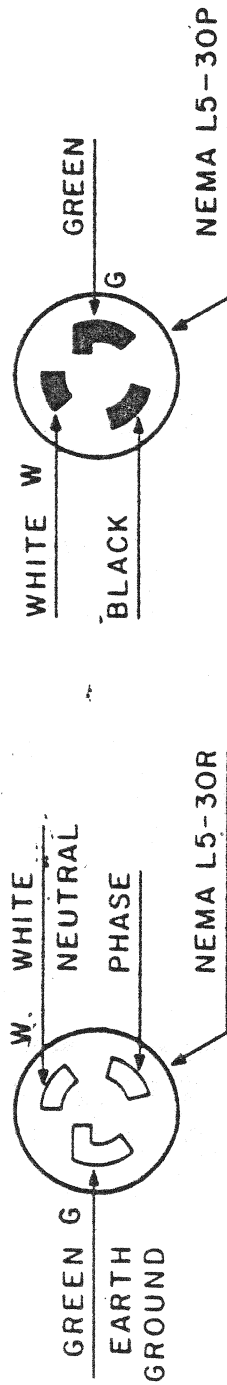
TK-4390

Figure 4-6 PDP-11/44-CA, -CB ac Connector Specifications

Mounted at the lower rear of the PDP-11/X44-CA, -CB cabinets is a power controller unit which controls and distributes the ac power to the units within the cabinet. The PDP-11/X44-CA contains an 872-D (120 Vac) power controller and the PDP-11/X44-CB contains an 872-E (240 Vac) power controller. Each controller is supplied with a 15.0 ft (4.57 m) cord and plug which connect to a receptacle at the site location. Figure 4-7 shows the connector configurations and DIGITAL part numbers for the plugs and receptacles.



230 V USED WITH THE 872-E



115 V USED WITH THE 872-D

CONNECTOR SPECIFICATIONS

MODEL NUMBER	POWER	RATING	PLUG NEMA CODE	RECEPTACLE (SUPPLIED BY CUSTOMER)	
				NEMA CODE	DEC PART NO.
872-D	115 V	30 A	L5-30P	L5-30R	12-11191
872-E	230 V	20 A	L6-20P	L6-20R	12-11194

Figure 4-7 872-D, -E Power Controller Input Power Specifications

TK-4391

#### 4.4.2 System Grounding

The PDP-11/44 and PDP-11/X44 systems are commonly grounded to the main power lines through the ac power cord. All units which are part of the system should be connected to a separate and common ac power distribution source to ensure the integrity of the grounding network. If a grounding problem is evident, the potential of the cabinet or mounting box grounds may be checked by connecting a voltmeter between two cabinet frames or between the cabinet frames and the BA11-A mounting box. To ensure positive grounding between the cabinets of the system, it is recommended that a grounding strap or cable be attached, in common to each of the cabinet frames. Contact a local Digital Equipment Corp. Field Service office for information related to grounding problems.

#### 4.5 PDP-11/44 MOUNTING BOX INSTALLATION

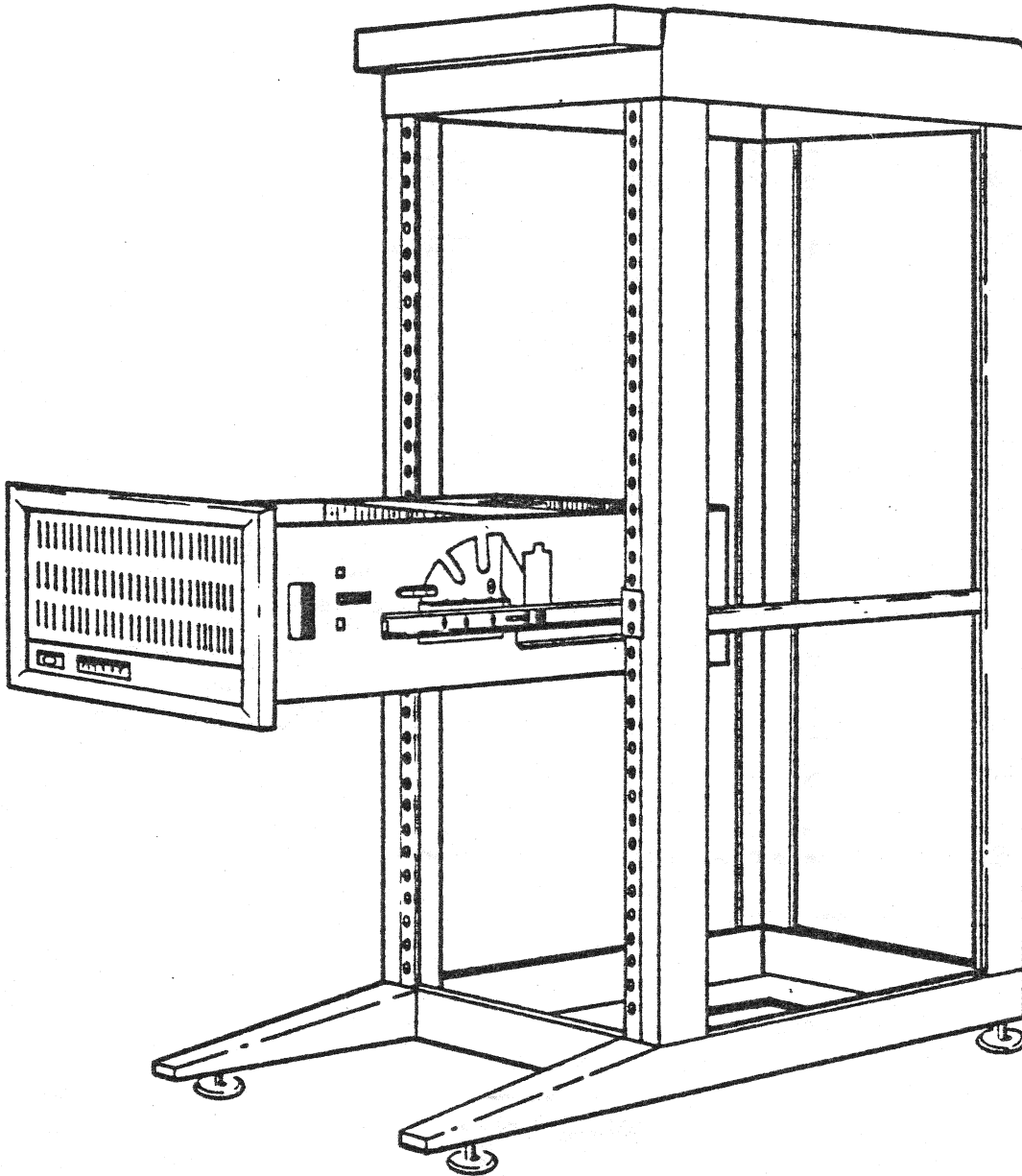
The BA11-AA, -AB mounting box is designed to be installed within a standard 19 inch (48.26 cm) rack or cabinet on slide mounting assemblies as shown on Figure 4-8.

A slide kit is available and includes the items listed on Table 4-2.

Table 4-2 Slide Kit Option Hardware

Quantity	Description	Part Number
1	Left and right index plates and mounting hardware	
1	Left and right slide assembly and mounting hardware	(12-16971)
1	BA11-A top cover	

*Tax from States  
Slide assy.  
12-11825-01*



NOTE:  
SLIDE AND SLIDE INDEX PLATE  
ARE USED WITH RACK MOUNTED VERSION.

TK-4183

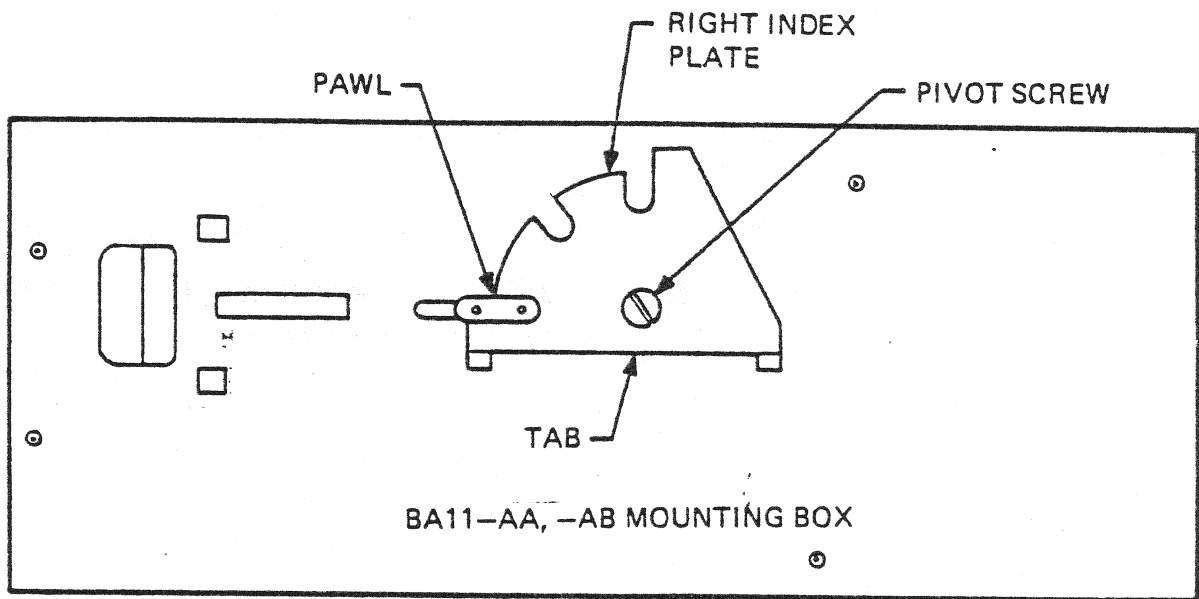
Figure 4-8 Mounting Box in H961 Cabinet

The index plates supplied with the kit are to be mounted onto the sides of the BALL-AA, -AB mounting box and permit the box to be tilted on the slides for servicing.

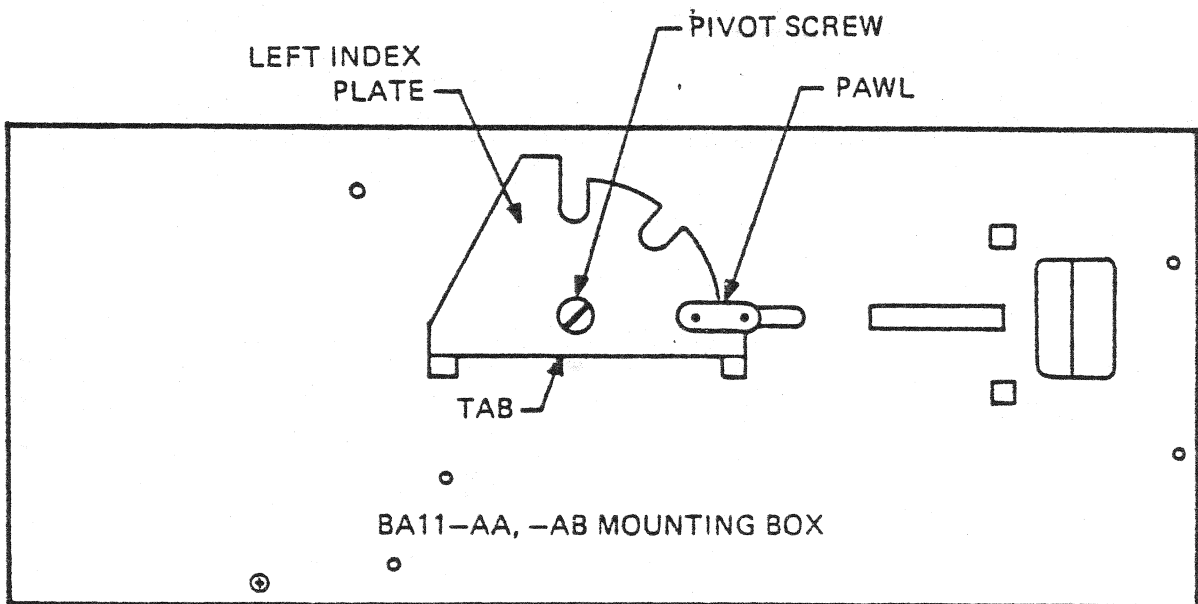
#### 4.5.1 Index Plate Mounting

To install the index plates refer to Figure 4-9 and perform the following procedures.

1. Position the right index plate onto the pawl as shown. The index plate mounting tab protrudes away from the side of the box.
2. Insert the pivot screw and tighten with a screwdriver.
3. Ensure that the index plate rotates freely when the locking pawl is released.
4. Perform steps 1 and 3 using the left index plate.



RIGHT SIDE VIEW



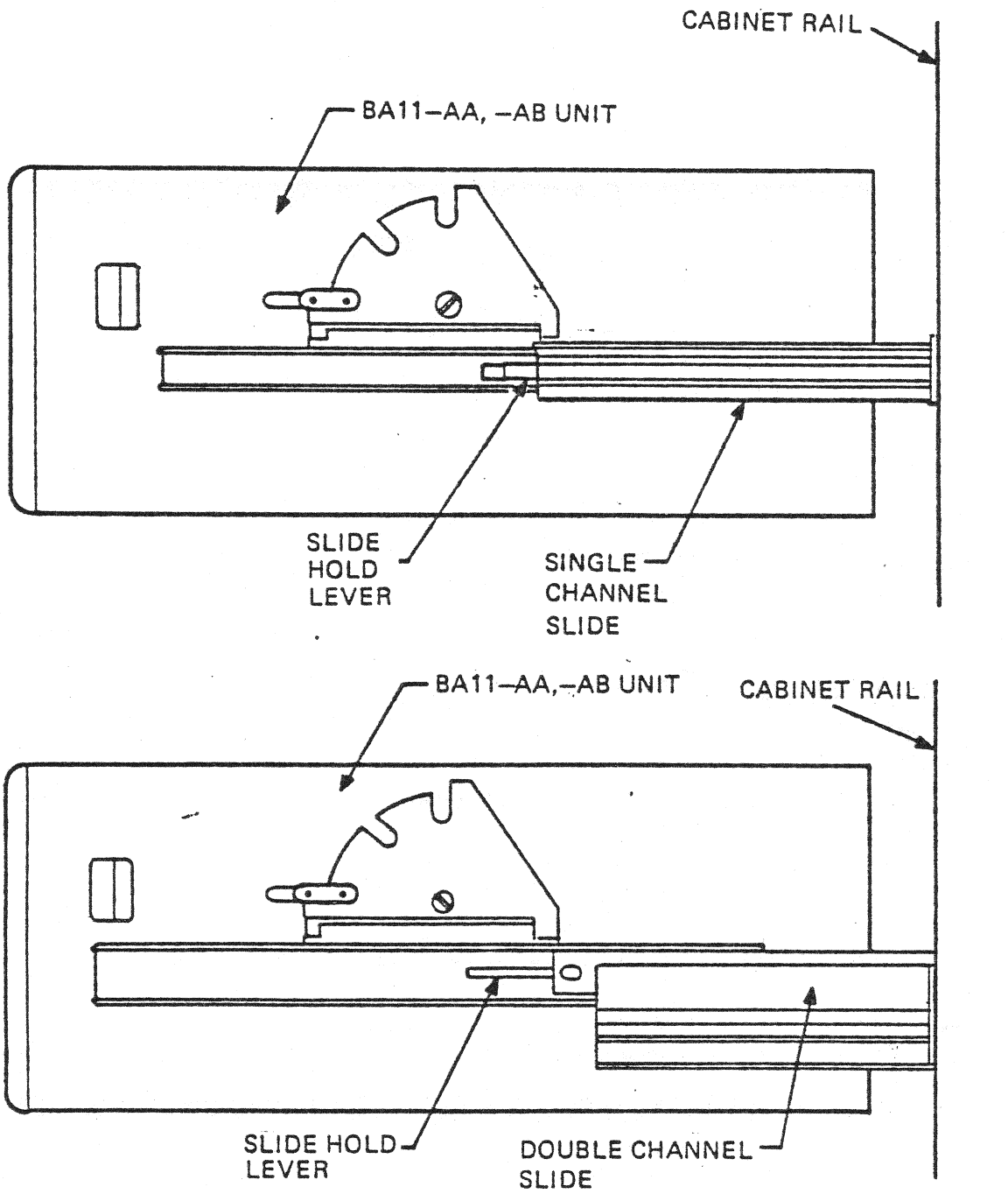
LEFT SIDE VIEW

TK-4392

Figure 4-9 BA11-AA, -AB Mounting Box Index Plate Installation

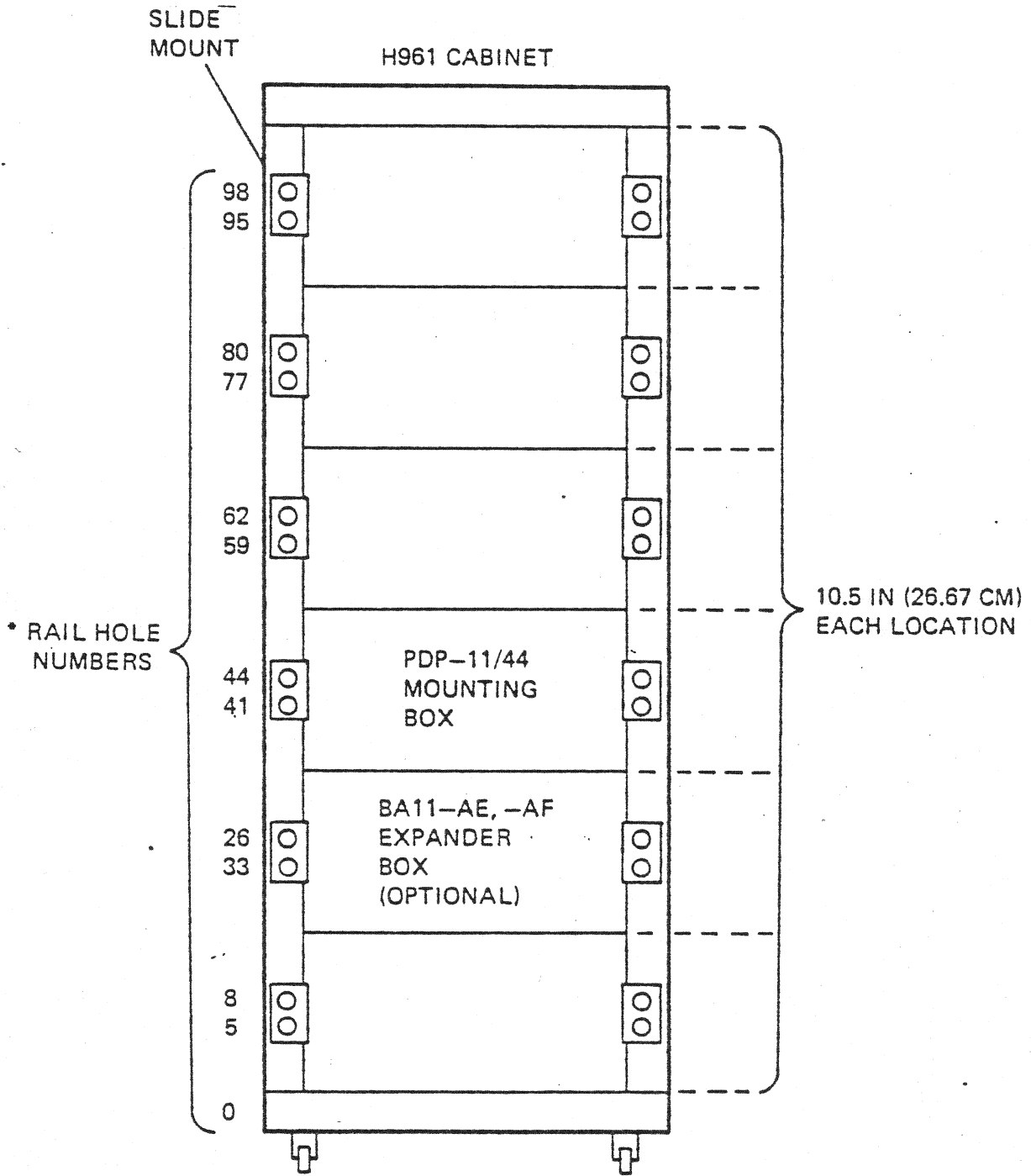
#### 4.5.2 Slide Assembly Mounting

One of two types of slide assemblies is provided with the slide kit option: a single channel slide set and a double channel slide set. Figure 4-10 shows each type mounted to the BA11-AA, -AB unit and fully extended from the cabinet. The mounting location of the slides will vary depending on the type of slide. Figure 4-11 shows a typical H961 standard cabinet with the PDP-11/44-CA, -CB unit and a BA11-AE, -AF expander box mounted directly below. The mounting location holes of the single channel slides for each 10.5 inch (26.67 cm) unit are indicated on Figure 4-11. When installing double channel slides, the hole location numbers will be decreased by two for the same mounting position of the units.



TK-4393

Figure 4-10 Single and Double Channel Slide Assemblies



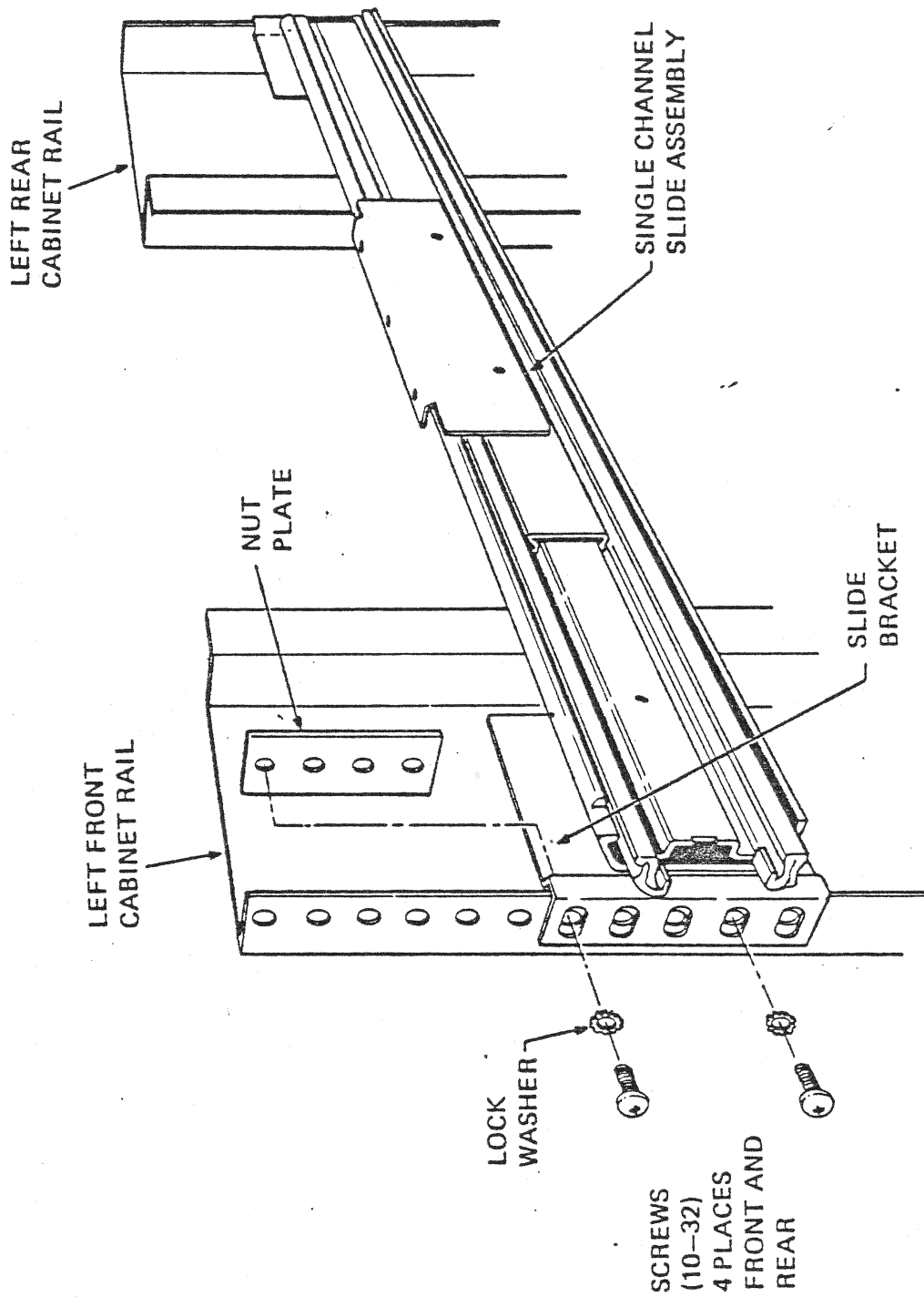
\* NOTE  
 DECREASE RAIL HOLE NUMBERS  
 BY TWO (2) WHEN INSTALLING  
 A DOUBLE CHANNEL SLIDE SET.

TK-4394

Figure 4-11 H961 Cabinet Slide Mounting Locations

Figure 4-12 shows the hardware and installation of a single channel slide assembly. The double channel slide assembly is mounted in a similar manner. To install the slide, perform the following procedures.

1. Position the left slide against the left front and left rear cabinet rail as shown.
2. Insert one 10-32 screw and washer through the top hole in the slide bracket, through the hole in the front rail and into the top threaded hole in the nut plate. Do not tighten.
3. Perform the same procedures in step 1 and step 2 at the left rear rail of the cabinet.
4. Insert one 10-32 screw and washer through the second hole from the bottom in the slide bracket, through the hole in the front rail and into the nut plate. Tighten both screws in the front rail.
5. Perform the same procedure in step 4 at the left rear rail of the cabinet.
6. Perform steps 1 through 5 to install the remaining slide onto the right side of the cabinet.



TK-4395

Figure 4-12 Cabinet Slide Installation

### 4.5.3 Mounting Box to Slide Installation

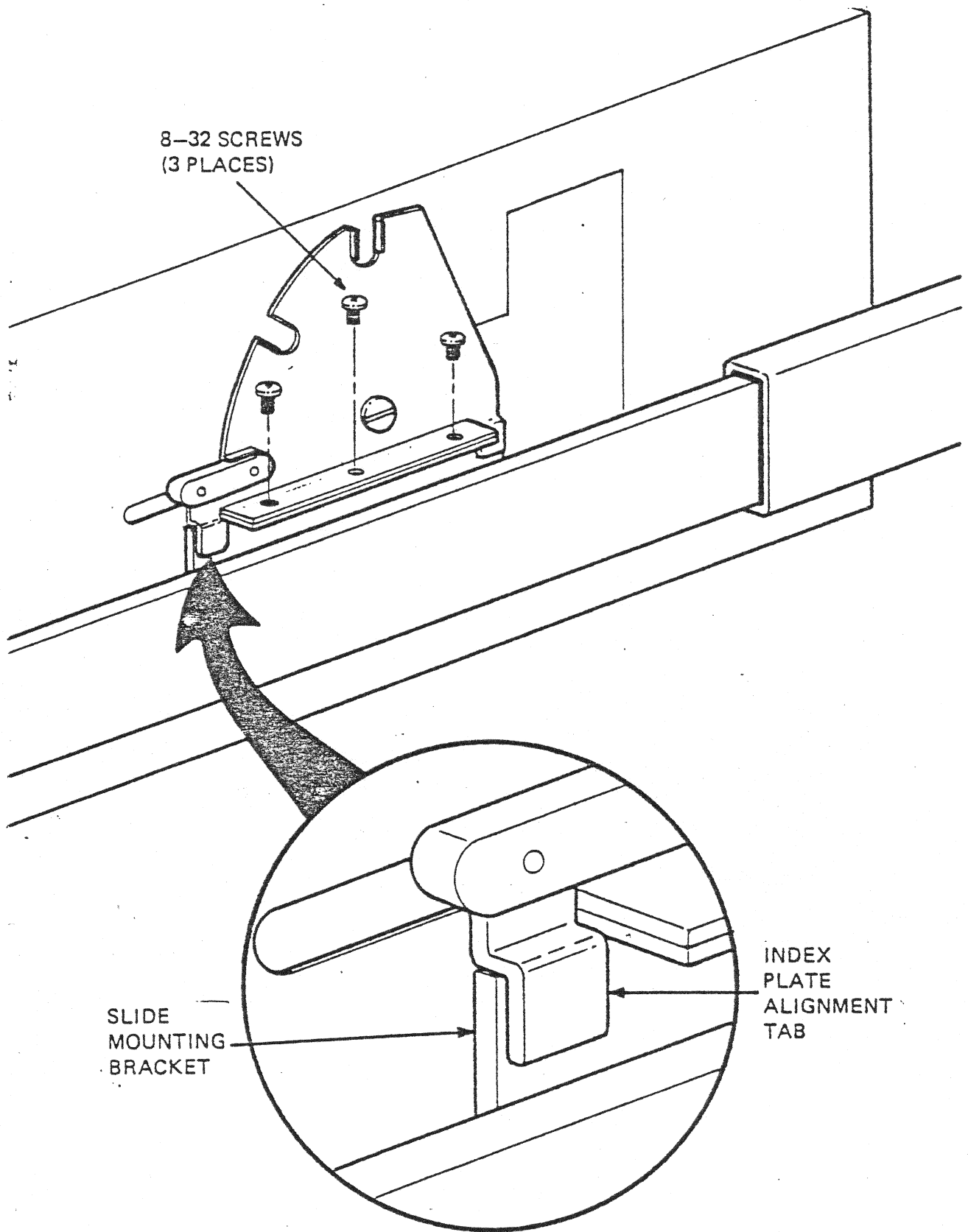
Figure 4-13 shows the method and hardware used to install the mounting box onto the slide mounting bracket. Perform the following procedures.

1. Extend the left and right slide channel to their maximum position at the front of the cabinet. When fully extended, the channels will be held in place by the slide hold lever shown on Figure 4-10.
2. Carefully lift the mounting box over and above the extended slides and set the index plate over the slide mounting bracket on each side of the box. The index plate alignment tabs will engage the sides of the slide mounting bracket.

#### NOTE

When the slides are fully extended, it may be necessary to force the ends of the slides inward toward the sides of the mounting box.

3. Insert the three 8-32 screws through the left index plate tab and into the threaded holes of the slide mounting bracket.
4. Perform the same procedure in step 3 for the right index plate.



TK-3486

Figure 4-13 Mounting Box to Slide Installation

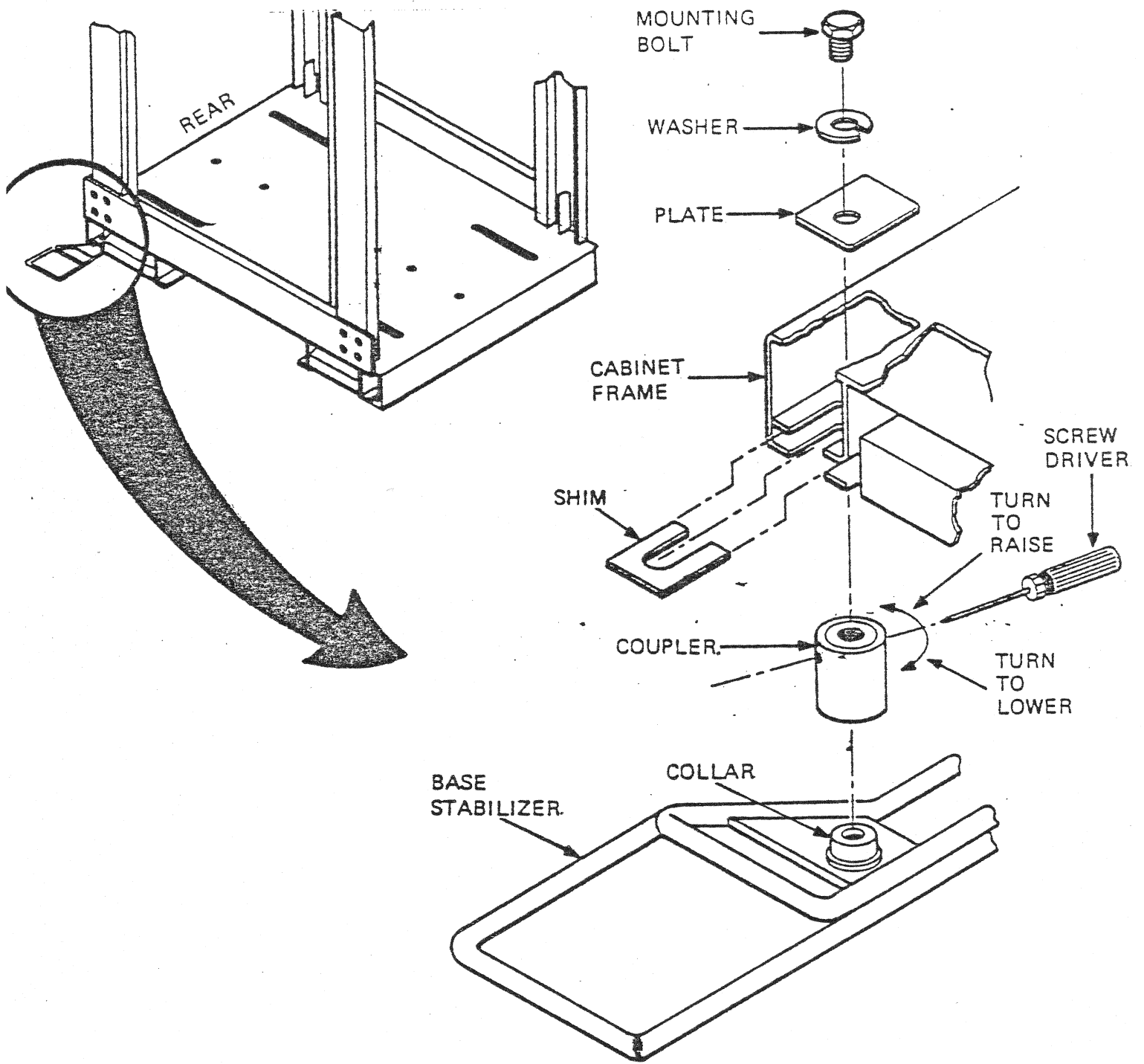
#### 4.6 PDP-11/X44 SYSTEM CABINET INSTALLATION

The PDP-11/X44-CA, -CB system cabinet is supplied with four rollers on the bottom frame and four leveler feet. The cabinet can be positioned alone or attached to another H9640 series cabinet. When operating alone a stabilizer bar (option No. H9544-MJ) must be attached to the rear of the unit to prevent the cabinet from tilting when the BALL-AA, -AB box is raised to the servicing position.

##### 4.6.1 Base Stabilizer Installation

Figure 4-14 shows the mounting position and hardware used to install the base stabilizer onto the PDP-11/X44 system cabinet. To mount the stabilizer, perform the following procedures:

1. Position the left and right coupler over the collars on the base stabilizer as shown.
2. Slide the stabilizer under the rear of the cabinet, to its normal mounting position.
3. Insert the mounting screw and washer, through the plate, through the slot in the frame and into the threaded hole of the coupler. Do not tighten.
4. To level the cabinet turn the coupler by inserting the shank of a screwdriver through the hole, in the direction desired.
5. Insert the shim into the location as shown.
6. Tighten the mounting screw with a 13/16 box end wrench while holding the coupler in position with the screwdriver.

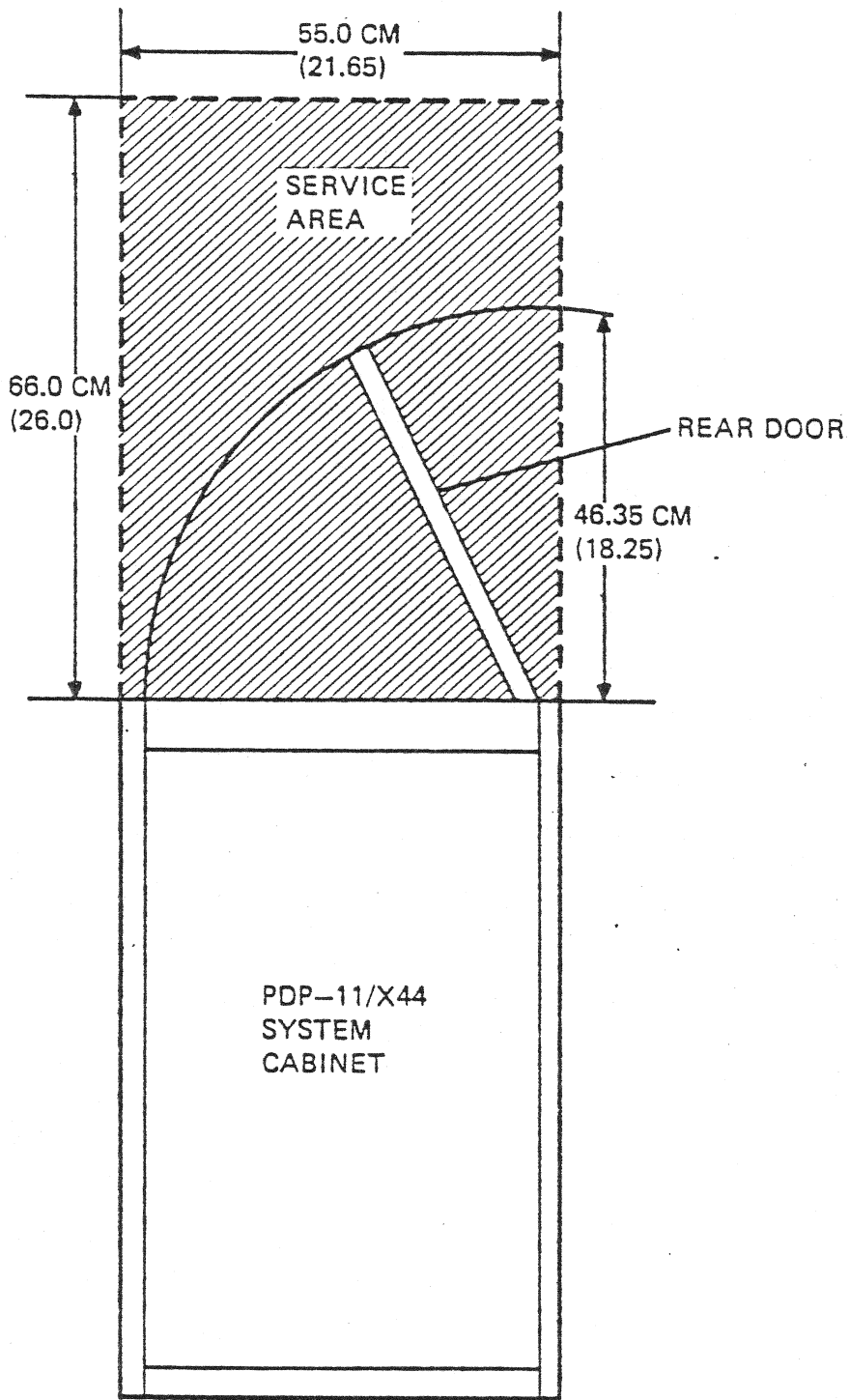


TK-4388

Figure 4-14 Cabinet Stabilizer Mounting

#### 4.6.2 Servicing Area

The rear door of the PDP-11/X44 system cabinet can be opened to gain access to the 872-D, -E power controller, the connectors attached to the I/O panel and the rear panel of the BA11-AA, -AE Mounting box. Figure 4-15 shows the service area clearance at the rear of the cabinet to permit the opening of the door and access to the internal units. The clearance also prevents the obstruction of air flow through the cabinet.



NOTE:  
DIMENSIONS IN PARENTHESES  
ARE IN INCHES

TK-4387

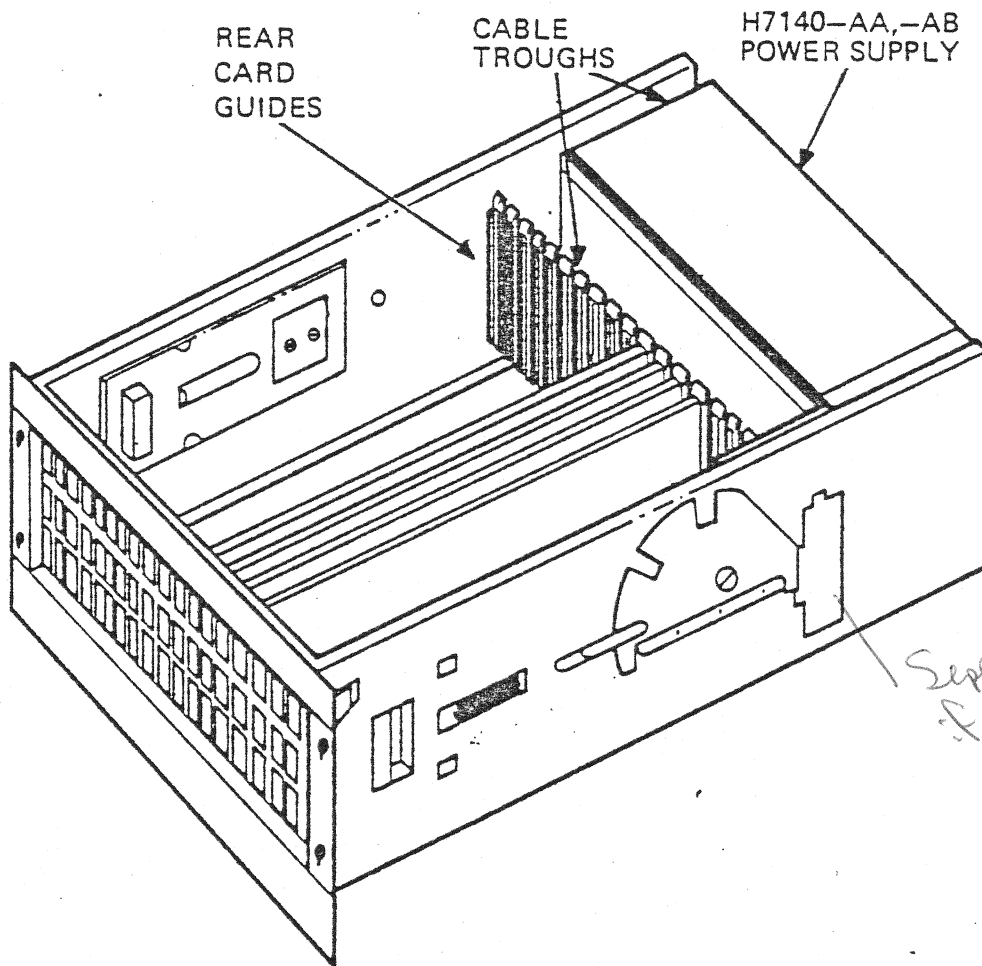
Figure 4-15 PDP-11/X44 System Cabinet Service Area

#### 4.7 CABLE ROUTING

The power and signal cables routed between assemblies within a cabinet and externally between cabinets should be properly secured away from sharp objects. Cables connected between cabinets should be protected from damage by routing through a channel or by covering with protective padding. The ac power cables and signal cables should be routed separately from each other to prevent the possibility of signal interference.

##### 4.7.1 Mounting Box Cable Routing

The cable assemblies that are attached to connectors on the modules are routed between the rear card guides through the cable trough directly behind the card guides and through the trough on the left side of the power supply. Figure 4-17 shows the position of the rear card guides and cable troughs.



TK-3478

Figure 4-16 BALL Cable Routing Locations

#### 4.7.2 PDP-11/X44 Cabinet Cable Routing

Figure 4-17 shows the routing of the cables at the rear of the system cabinet. The Unibus cable is folded and clamped at the rear of the power supply as shown. All other cables such as the console terminal cable from the I/O panel should be clamped to the cabinet channels. The length of all cables should be adequate to allow the mounting box to be raised for servicing without causing cable strain. Nylon tiwraps can be used to secure the cables to cabinet channels.

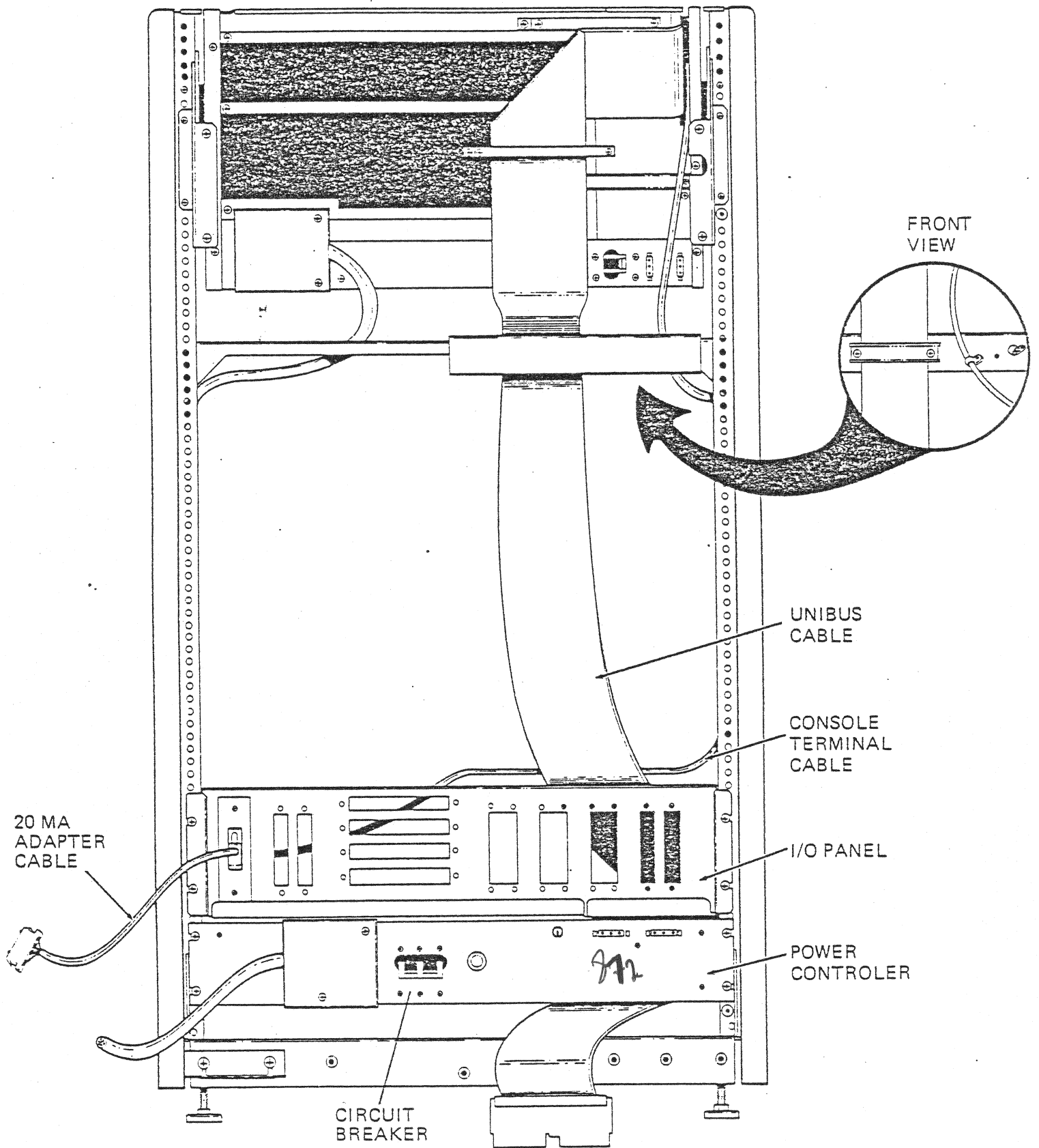


Figure 4-17 PDP-11/X44 Cabinet Cable Routing

TK-364C



The PDP-11/44 system is designed to permit units and assemblies to be easily removed and replaced. This section includes the procedures for the BALL-AA, -AB mounting box, the H7140-AA, -AB power supply and the fan assembly. For detailed removal and replacement procedures related to other units supplied with the system, refer to the appropriate manuals supplied.

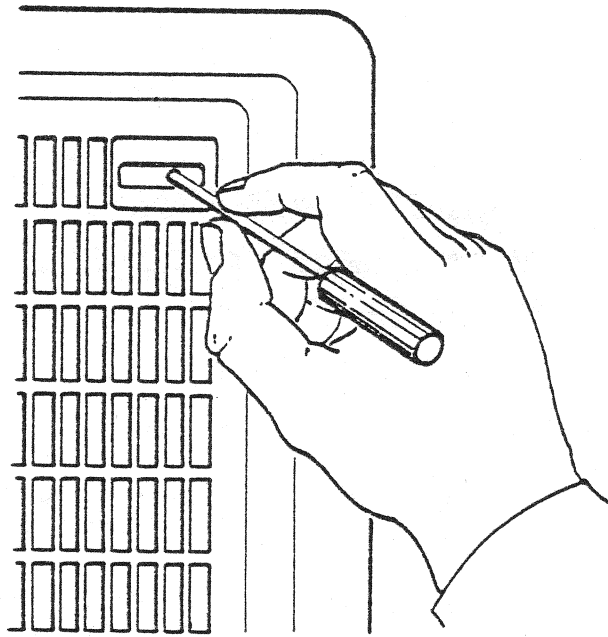
#### 5.1 BALL-AA, -AB MOUNTING BOX IN SYSTEM CABINET

In the PDP-11/X44 system, the BALL-AA, -AB mounting box is located at the top of the system cabinet. To remove or replace the unit, perform the following procedures.

##### 5.1.1 Mounting Box Removal

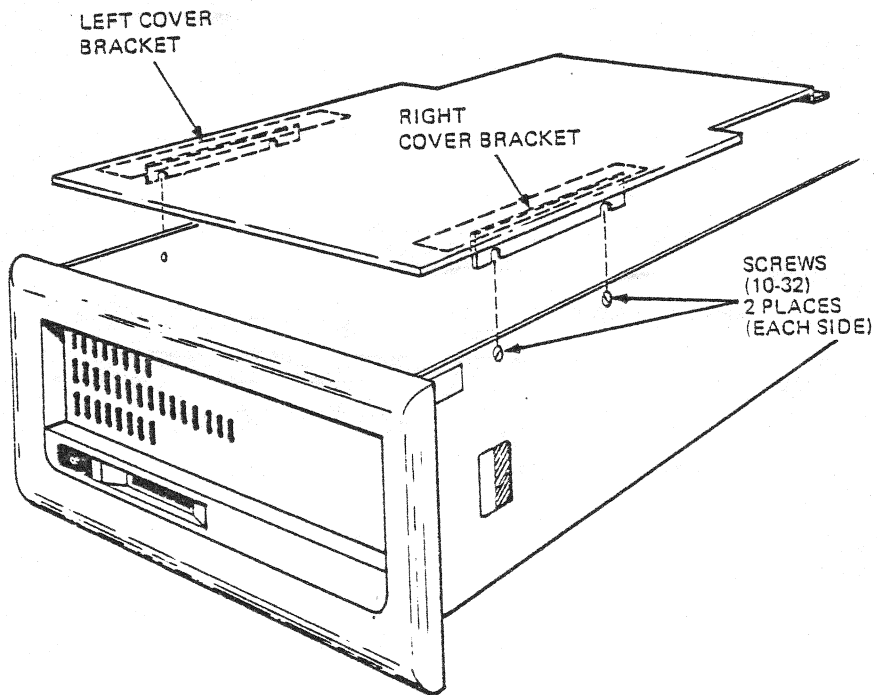
To remove the BALL-AA, -AB mounting box from the PDP-11/X44 system cabinet, perform the following procedure:

1. Open the rear door of the cabinet. Use a 0.396 cm (5/32 inch) hex wrench to release the door fastener.
2. Remove the ac power from the power controller by setting the circuit breaker in the down position (Figure 4-17).
3. Remove the BALL-AA, -AB power cord plug from the connector in the power controller.
4. Cut or release any fasteners used to secure the power cord to the cabinet frame.
5. Insert a screwdriver blade into the hole behind the slot which is located at the top right side of the front bezel (Figure 5-1).
6. Release the latch which holds the mounting box by sliding the screwdriver blade in the direction shown.
7. Raise the front of the mounting box until the unit is at an angle of approximately 45° with the top of the cabinet.
8. Release the four (10-32) screws which hold the cover brackets to the left and right sides of the mounting box (Figure 5-2). Do not remove the screws.
9. Remove the top cover.
10. Lower the front of the mounting box until it is in the normal position and the latch engages.



TK-3458

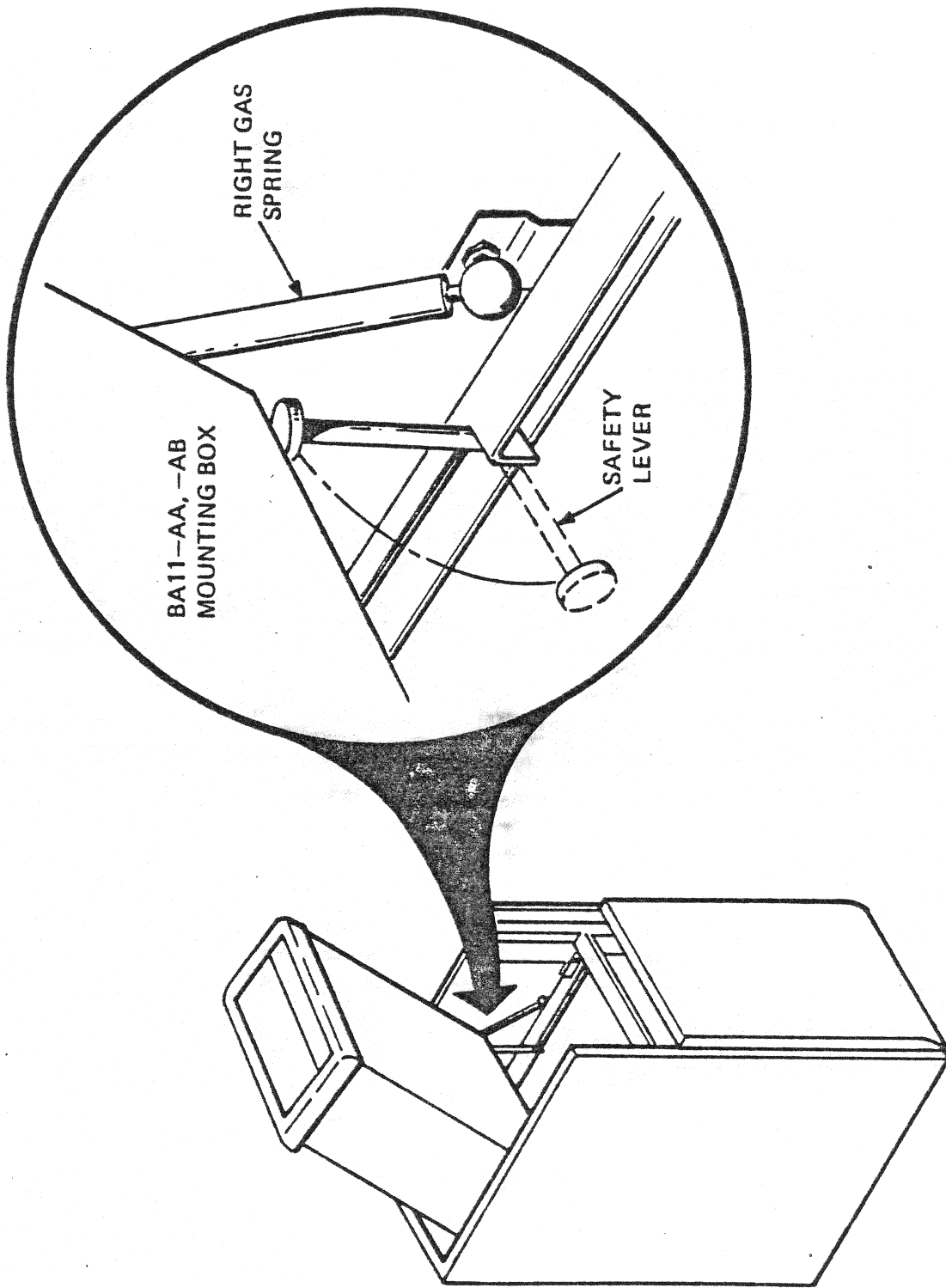
Figure 5-1 Mounting Box Release Lever



TK-4396

Figure 5-2 PDP-11/X44 Top Cover Mounting

11. Disconnect all bus and I/O cables attached to the modules within the unit.
12. At the rear of the BA11-AA, -AB box, remove and retain the two (6-32) screws used to secure the cable clamp bar to the power supply (Figure 4-16).
13. Remove the cables from the cable trough in the BA11-AA, -AB box and feed the cables toward the rear of the cabinet and away from the mounting box.
14. Release the latch on the front of the mounting box as described in steps 5 and 6.
15. Raise the front of the mounting box to the position shown on Figure 5-3 and raise the stop lever to hold the mounting box.
16. Remove the retaining clip from the piston ball connectors of the gas spring on the left and right pivot bracket (Figure 5-4). Use needle nose pliers to facilitate the clip removal.
17. Remove the retaining clip from the body ball connector of the gas spring on the right side of the cabinet.
18. Remove the ball connectors on the right side of the cabinet from the studs by inserting a screwdriver blade between the ball connector and the ball stud mounting surface.
19. Remove the ball connector from the ball stud on the left pivot bracket using the procedure described in step 18.



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Figure 5-3 PDP-11/X44 Cabinet Safety Lever

20. Rotate the left gas spring toward the front of the cabinet until the gas spring is horizontal.
21. Remove the retaining clip from the body ball connector on the left gas spring and remove as in step 18.
22. At the rear of the cabinet remove the two (10-32) interface bracket screws and washers which secure the pivot bracket to the cabinet frame on the left and right side of the cabinet. (Figure 5-4)
23. At the front of the cabinet, lower the safety lever, and lower the mounting box to its normal position. (Figure 5-3)

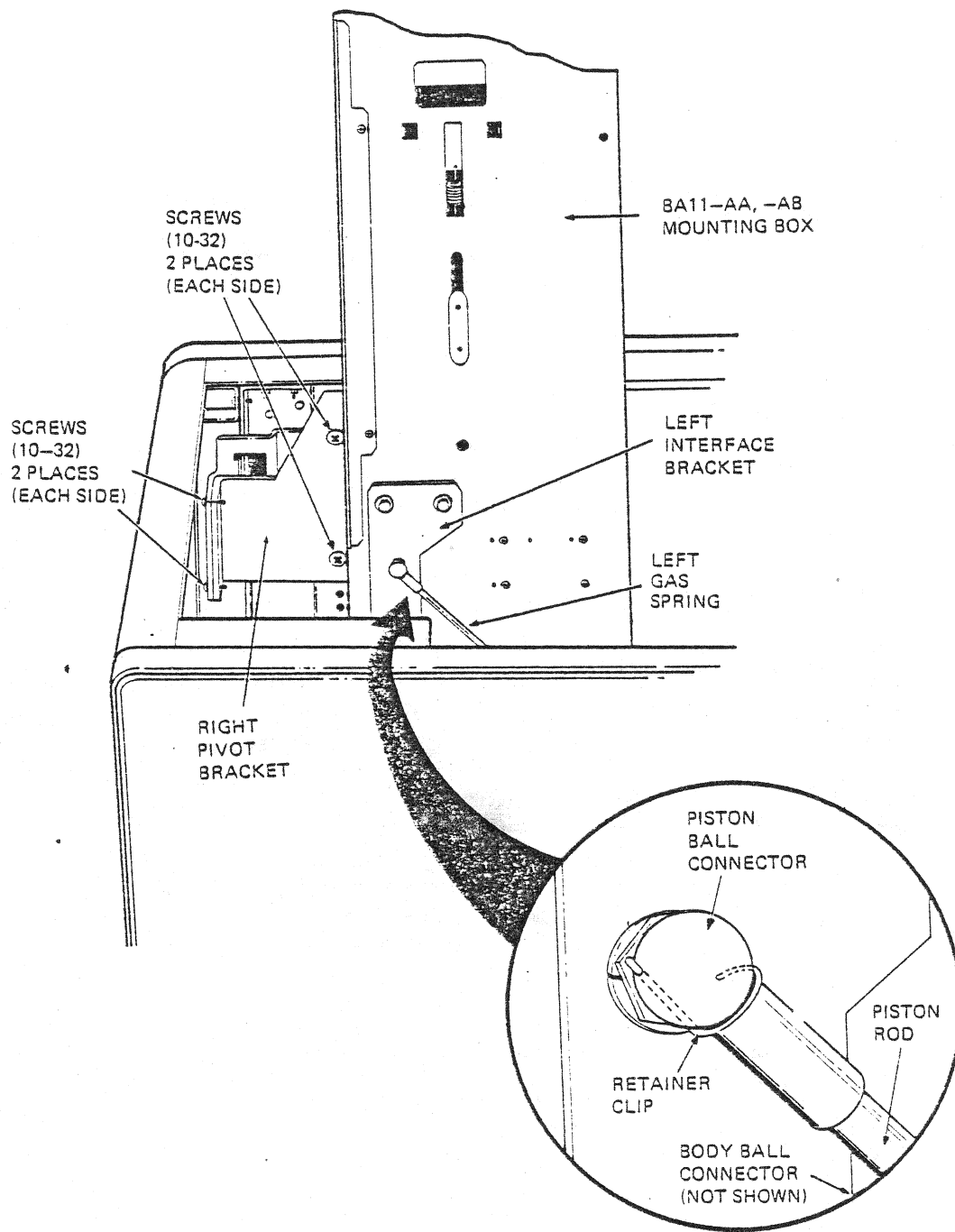
#### NOTE

When the gas springs have been removed, the mounting box may not be properly balanced.

24. At the rear of the cabinet, remove and retain the two (10-32) screws and washers on the left and right side of the cabinet which secure the pivot bracket angle to the interface bracket. (Figure 5-4)
25. Grasp the bottom of the mounting box at the front and rear and gently slide the box toward the front of the cabinet. Lift the back of the mounting box and slide the box forward and away from the cabinet frame.

#### CAUTION

Removal of the mounting box may require two persons due to its weight, one person lifting from the left side and one person lifting from the right side of the cabinet.



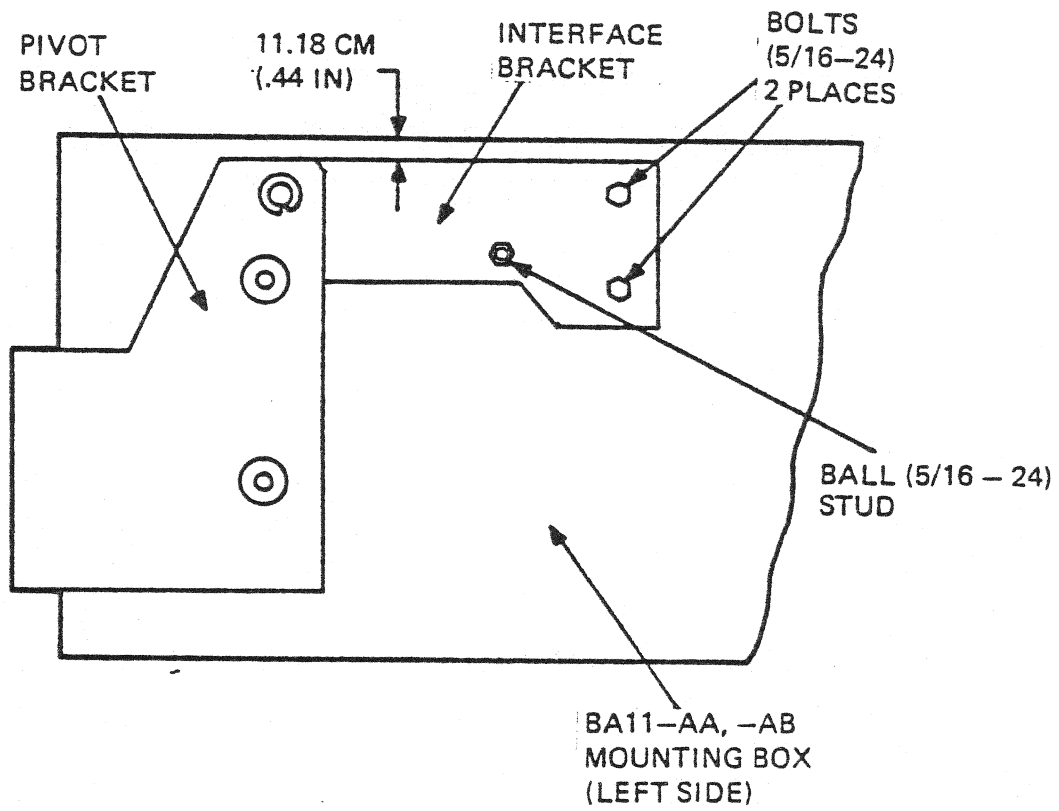
TK-3469

Figure 5-4 PDP-11/X44 Cabinet, Mounting Box Hardware

### 5.1.2 Interface Bracket Removal/Installation

If the mounting box to be installed does not have the interface and pivot bracket mounted on each side, remove the brackets from the box to be replaced and install using the following procedures.

1. Using a 12.7 mm (1/2 inch) open or box end wrench, remove the two (5/16 - 24) bolts and the (5/16 - 24) ball stud located on the left and right side of the mounting box (Figure 5-5).
2. Remove the two bracket assemblies and using the hardware previously removed, install onto the left and right side of the replacement mounting box. Do not tighten bolts.
3. Align the top of the interface bracket to be parallel with the top of the mounting box and at the dimension shown on Figure 5-5.
4. Tighten the two (5/16 - 24) bolts and the ball stud.



TK-4398

Figure 5-5 Interface Bracket Mounting

### 5.1.3 Mounting Box Replacement

To install the BALL-AA, -AB mounting box into the PDP-11/X44 system cabinet perform the following procedures.

1. Grasp the bottom of the mounting box at the front and rear and position the box on the slide rails with the front of the unit extending away from the front of the system cabinet.

#### CAUTION

Installation of the mounting box may require two persons due to its weight, one person lifting from the left side and one person lifting from the right side of the cabinet.

2. Slide the mounting box toward the rear of the unit while lifting the rear of the box.
3. At the rear of the cabinet, install the two (10-32) screws and washers, removed in step 24 of paragraph 5.1.1, in the angle part of the left and right interface bracket (Figure 5-4). Do not tighten the screws.
4. Raise the front of the mounting box to the position shown on Figure 5-4 and raise the stop lever to hold the mounting box in position.
5. Replace the two (10-32) interface bracket screws and washers, removed in step 22 of paragraph 5.1.1, into the left and right cabinet frame (Figure 5-4).

#### NOTE

It may be necessary to shift the position of the mounting box in a direction that will cause the holes of the interface bracket to be properly aligned with cabinet frame holes.

6. Tighten the screws installed in step 5.
7. Place the left gas spring in the same horizontal position as it was removed in step 20 of paragraph 5.1.1.
8. Press the body ball connector onto the ball stud and install the retaining clip removed in step 21 of paragraph 5.1.1.

9. Press the piston ball connector onto the ball stud that is located on the left pivot bracket. Install the retaining clip that was removed in step 16 of paragraph 5.1.1.
10. Press the piston ball connector onto the ball stud that is located on the right pivot bracket. Install the retaining clip removed in step 16 of paragraph 5.1.1.
11. Press the body ball connector onto the ball stud and install the retaining clip that was removed in step 17 of paragraph 5.1.1.
12. Lower the stop lever and lower the mounting box to its normal operating position.
13. Route the cables removed in step 13 of paragraph 5.1.1 through the cable trough.
14. Insert the cable connectors removed in step 11 of paragraph 5.1.1.
15. Install the cable clamp removed in step 12 of paragraph 5.1.1.
16. Release the latch on the front of the mounting box as described in steps 5 and 6.
17. Raise the front of the mounting box as described in step 7 of paragraph 5.1.1.
18. Install the top cover onto the mounting box and tighten the screws which were released in step 8 of paragraph 5.1.1.
19. Lower the front of the unit to its normal operating position until the latch engages.

## 5.2 BALL-AA, -AB SLIDE MOUNTED REMOVAL/REPLACEMENT

Refer to Chapter 4 for the installation of the BALL-AA, -AB mounting box on the slide assemblies.

## 5.3 FAN ASSEMBLY

The fan assembly is installed on the right side of the BALL-AA, -AB mounting box and can easily be removed for servicing. The assembly contains three fans, each of which can be removed and replaced.

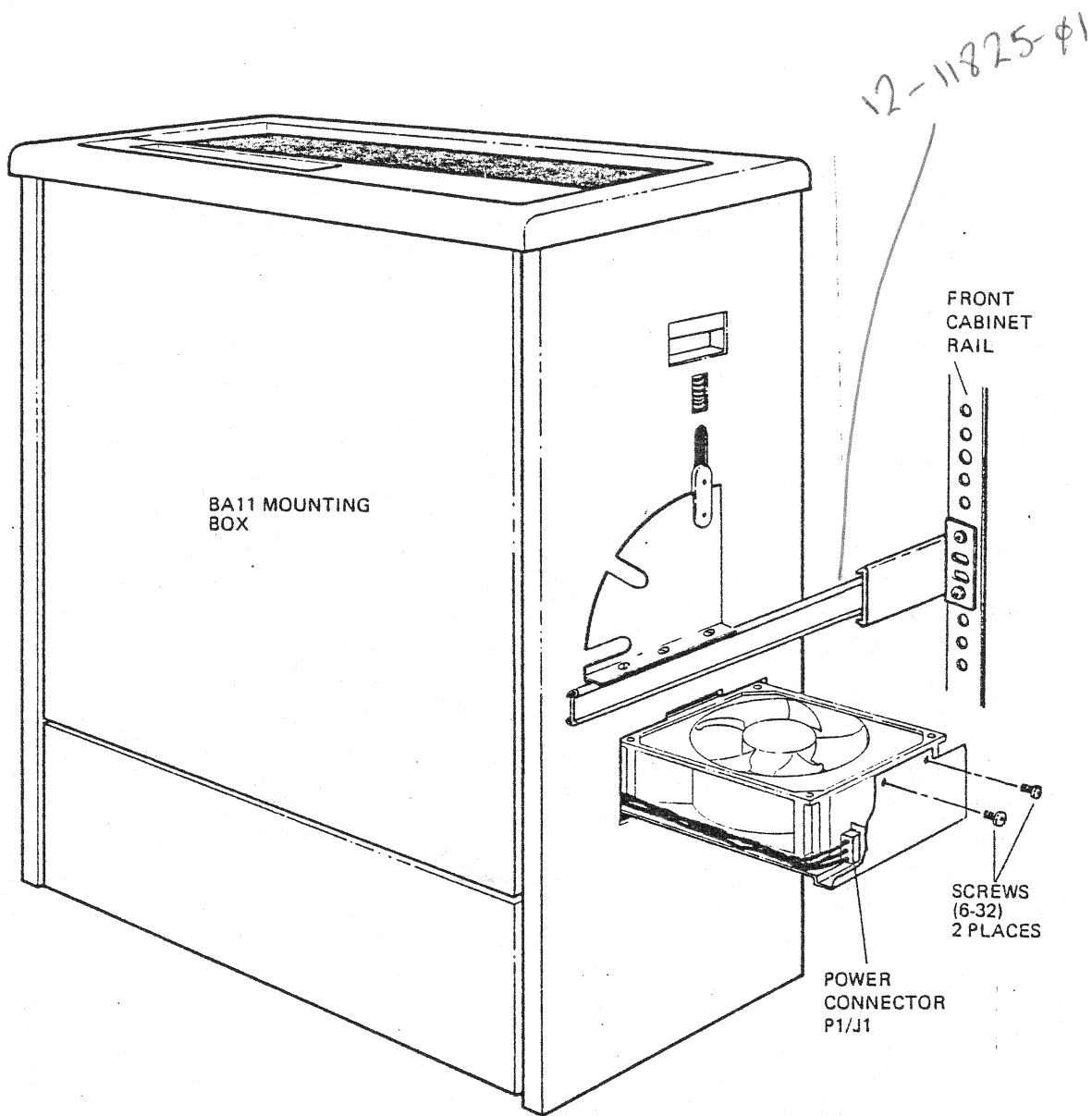
### 5.3.1 Fan Assembly Removal/Replacement

To remove the fan assembly and fans, perform the following procedure.

1. Remove the ac power from the BA11-AA, -AB mounting box by removing the ac power cord plug from its receptacle.
2. Insert a screwdriver blade into the hole behind the slot which is located at the top, right side of the front bezel (Figure 5-1).
3. Release the latch which holds the mounting box by sliding the screwdriver in the direction shown.
- 4a. In the PDP-11/X44 system, raise the front of the mounting box to its maintenance position and raise the safety lever (Figure 5-3).
- 4b. If the mounting box is installed on slides, pull the front of the box until the slide hold levers are engaged (Figure 4-10).
5. Release the pawl retractors on each side of the mounting box and tilt the box 90° to the maintenance position.
6. Remove the two (6-32) screws which secure the fan assembly to the side of the box (Figure 5-6).
7. Slide the fan assembly away from the side of the box approximately 5 cm (2 in) and disconnect connector P1 from J1.
8. Continue to slide the assembly away from the box.

#### NOTE

Any of the three fans can be replaced by disconnecting the power plug on the fan and removing the four (6-32) mounting screws which secure the fans to the slide. Use only the specified replacement fan and mount the new fan to assembly using the hardware removed.



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Figure 5-6 Fan Assembly Removal

9. To replace the fan assembly, perform the instructions described in steps 8, 7 and 6 in the reverse order and reset the mounting box in its normal operating position.

NOTE

The slide holding levers (Figure 4-10) must be released by pressing inward before the slides will retract.

5.4 H7140-AA, -AB POWER SUPPLY REMOVAL/REPLACEMENT

Before removing the power supply assembly from the mounting box, remove the power cord plug of the power supply from the ac power distribution connector. To remove and replace the power supply, perform the following procedures.

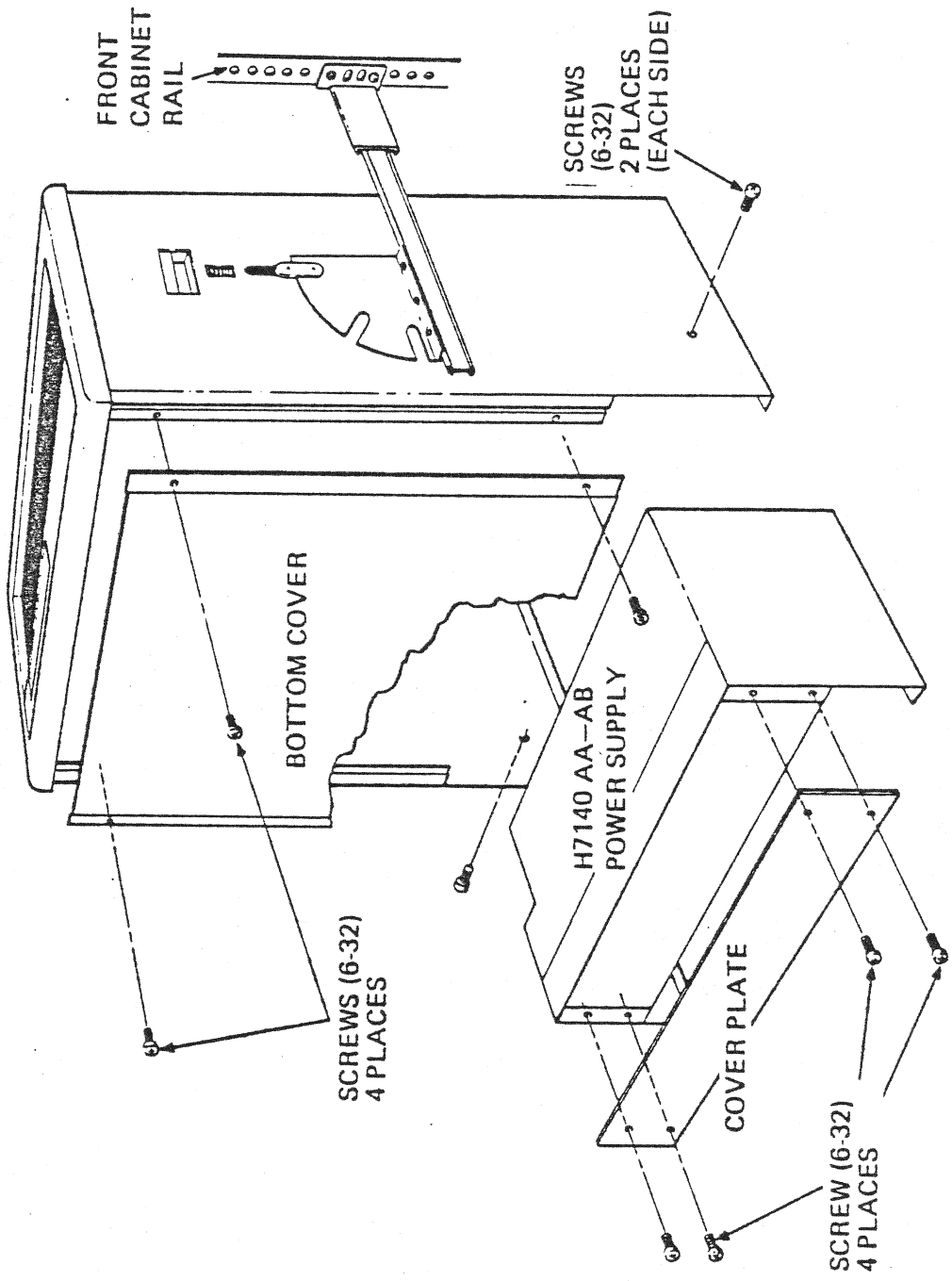
5.4.1 Power Supply Removal

1. From the rear of the cabinet, remove and retain the two (8-32) screws located in each of the two chassis angles at the rear of the mounting box (Figure 5-7).
2. Perform steps 1 through 4 of paragraph 5.3.1
3. Remove and retain two of the four (6-32) screws that secure the left side of the bottom cover to the mounting box (Figure 5-8). Release the two (6-32) screws from the right side of the bottom cover. Do not remove the screws. Remove the cover.
4. Remove and retain two of the four (6-32) screws that secure the left side of the cover plate to the bottom of the power supply assembly. Release the two (6-32) screws from the right side of the cover plate. Do not remove the screws. Remove the cover.
5. Remove and retain the (10-32) screw that secures the ground lead to the ground bus (Figure 5-9).
6. Loosen the two nuts (3/8 inch) on the clamp that holds the ground flex print cable to the ground bus bar.



TK-4400

Figure 5-7 Power Supply Assembly, Rear Mounting Screws



TK-4401

Figure 5-8 Power Supply Assembly Removal

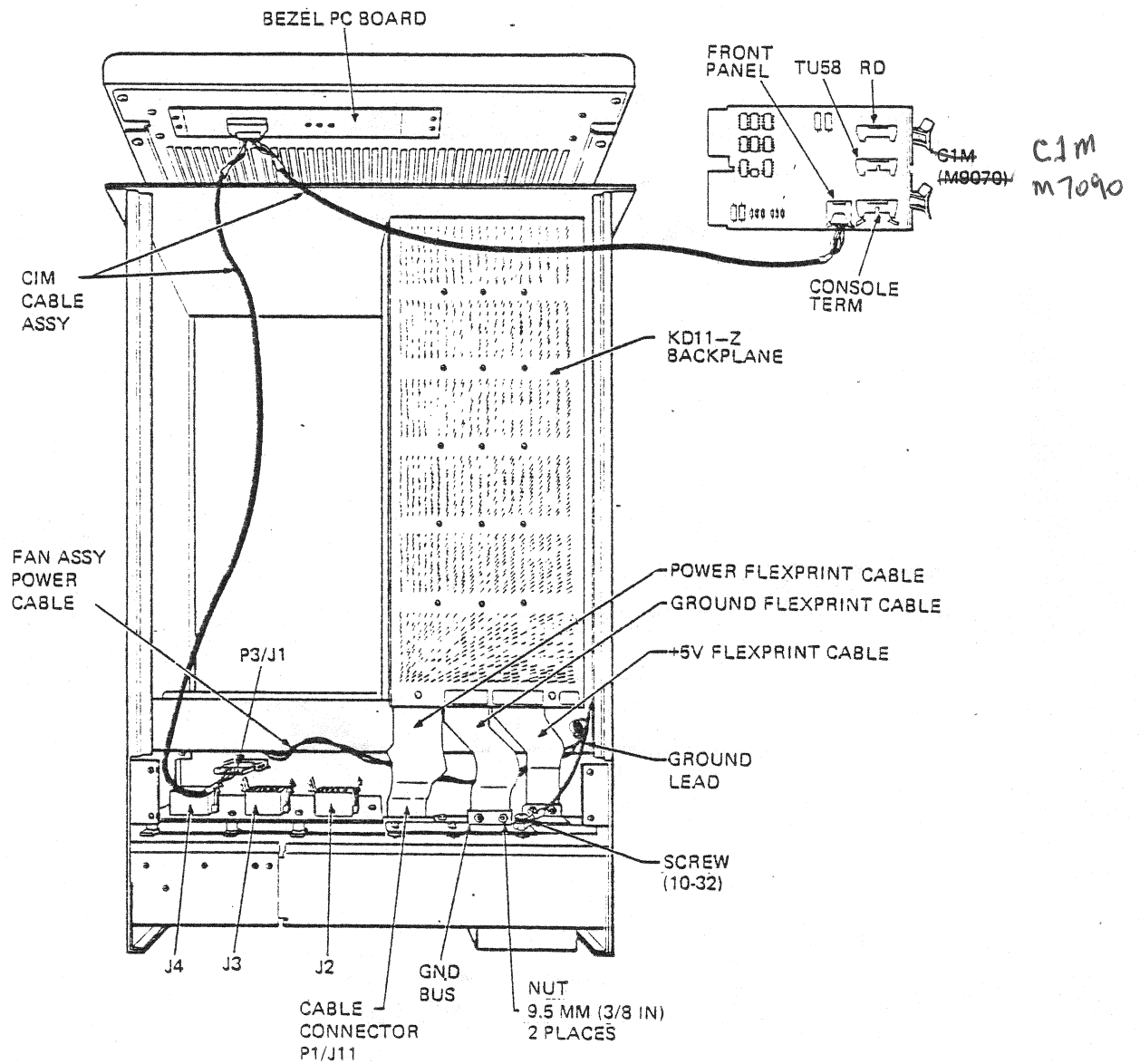


Figure 5-9 Power Lead Connections

7. Loosen the two nuts (3/8 inch) on the clamp that holds the +5 V flex print cable to the +5 V bus bar.
8. Slide the ground and +5 V flex print cables away from the clamps and bend upwards towards the backplane.
9. Remove the power flex print connector P1 from power supply connector J11 and bend upwards toward the backplane.
10. Remove connector P3 of the CIM cable assembly from connector J1 of the power supply. Move the tabs on each side of J1, to release P3. (Figure 5-10)
11. Remove the nut (3/8 inch) that secures the ground lead of connector P3, removed in step 10, to the chassis ground stud.
12. If one or more an additional backplanes are mounted in the box, remove the connectors attached to J2, J3 and J4 of the power distribution board. Remove the backplane connectors from P2, P3 and P4 of the power distribution harness.
13. In a slide mounted installation, remove and retain the (8-32) screw located on each side of the mounting box, towards the rear (Figure 5-8).
14. In a PDP-11/X44 installation, remove the side panels of the system cabinet.
15. Release the stop lever and position the mounting box so that (8-32) screws located on each side of the mounting box can be removed (Figure 5-8).

#### CAUTION

The H7140 power supply assembly will tend to slide forward when the screws in step 15 are removed.

16. Remove and retain the two (8-32) screws described in step 15.
17. Slide the power supply assembly forward approximately 5.0 cm (2.0 inches) and disconnect the fan assembly power cable shown on Figure 5-9 from connectors J2 and J3 (not shown) on the power supply PC board.
18. Slide the power supply assembly from the mounting box and away from the cabinet.

H7140-AA, -AB POWER SUPPLY UNIT

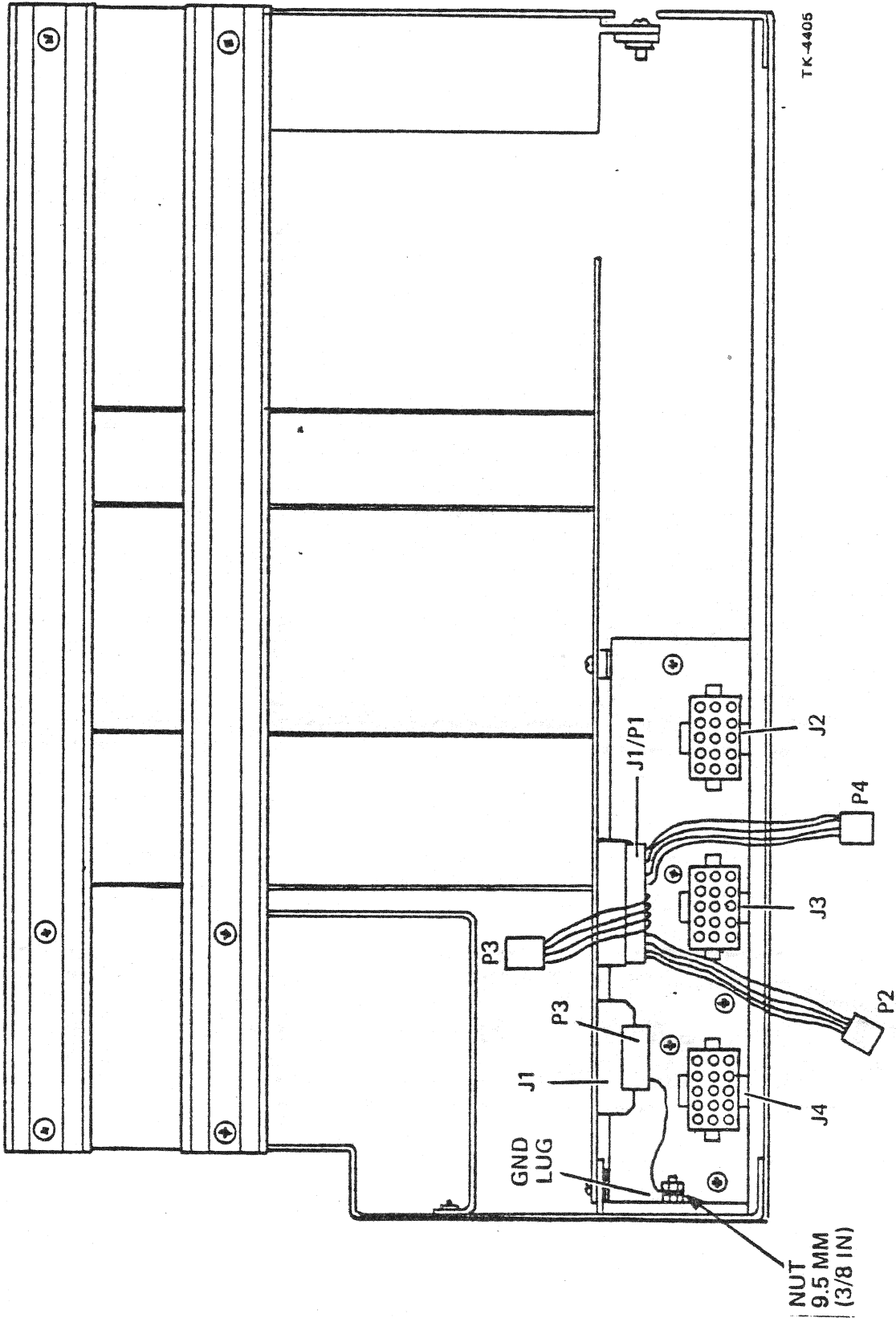


Figure 5-10 Power Distribution Panel and Connectors

#### 5.4.2 Power Supply Replacement

1. With the mounting box in the maintenance position, slide the power supply into the mounting box chassis.

#### NOTE

When the power supply assembly is being inserted, check that the I/O and bus cables are properly positioned and do not interfere with the supply installation. Before the supply is fully inserted, connect the fan assembly power leads that were removed in step 16 of paragraph 5.4.1.

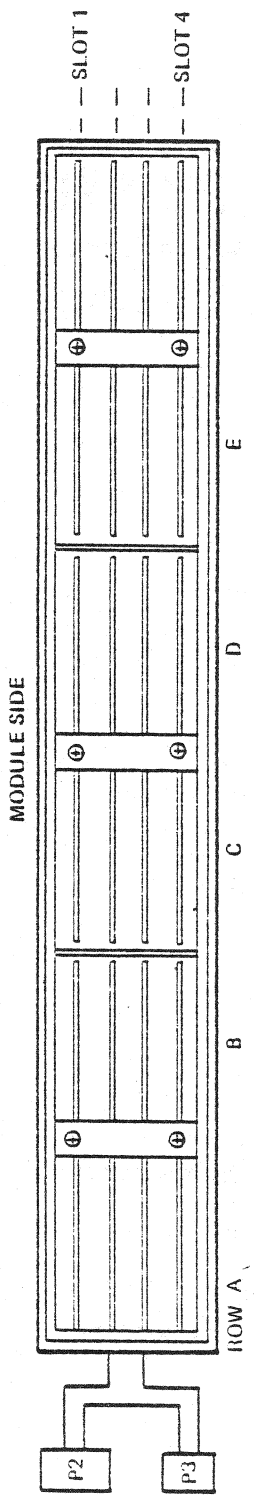
2. Replace the two screws (8-32) removed in step 16 or 13 of paragraph 5.4.1.
3. Replace the backplane connectors removed in step 12 of paragraph 5.4.1.
4. Replace the ground lead removed in step 11 of paragraph 5.4.1.
5. Replace connector P3 removed in step 10 of paragraph 5.4.1.
6. Replace the power flex print cable connector removed in step 9 of paragraph 5.4.1.
7. Replace the +5 V and ground flex print cables removed in steps 8, 7 and 6 of paragraph 5.4.1.
8. Replace the ground lead removed in step 5 of paragraph 5.4.1.
9. Replace the cover plate removed in step 4 of paragraph 5.4.1.
10. Replace the bottom cover removed in step 3 of paragraph 5.4.2.

11. In the PDP-11/X44 system, release the safety lever and lower the mounting box until the front latch engages.
12. If the mounting box is installed on slides, release the slide hold levers on each side slide rail and slide the mounting box into the cabinet until the front latch engages.
13. From the rear of the cabinet, replace the four (8-32) screws removed in step 1 of paragraph 5.4.1.

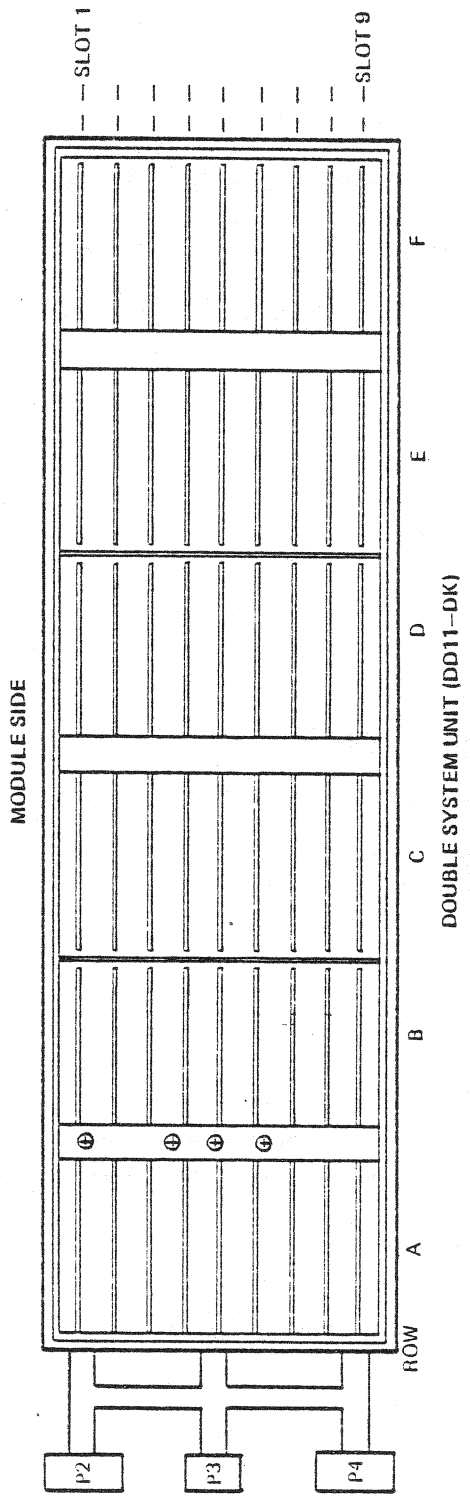
## 5.5 OPTIONAL BACKPLANE ASSEMBLIES

Two types of backplane assemblies are available for installation in the mounting box. The DD11-CK backplane is defined as a single system unit and the DD11-DK is a double system unit. The backplane assemblies are shown on Figure 5-11 and consist of module connector blocks that are mounted in a metal frame. The connector block pins are prewired for the PDP-11 bus signals and for the dc power and ground. Table 5-1 lists the slot-columns and rows available in each backplane.

The backplane assemblies are installed within the mounting box in the area adjacent to the CPU backplane. The dc power is supplied to the backplane through a wire harness and connectors that mate with the power supply connectors. Table 5-2 lists the maximum number of each type of backplane which can be installed.



SINGLE SYSTEM UNIT (DD11-CK)



DOUBLE SYSTEM UNIT (DD11-DK)

TK-4402

Figure 5-11 Optional Backplane Assemblies

Table 5-1 Optional Backplane Assemblies

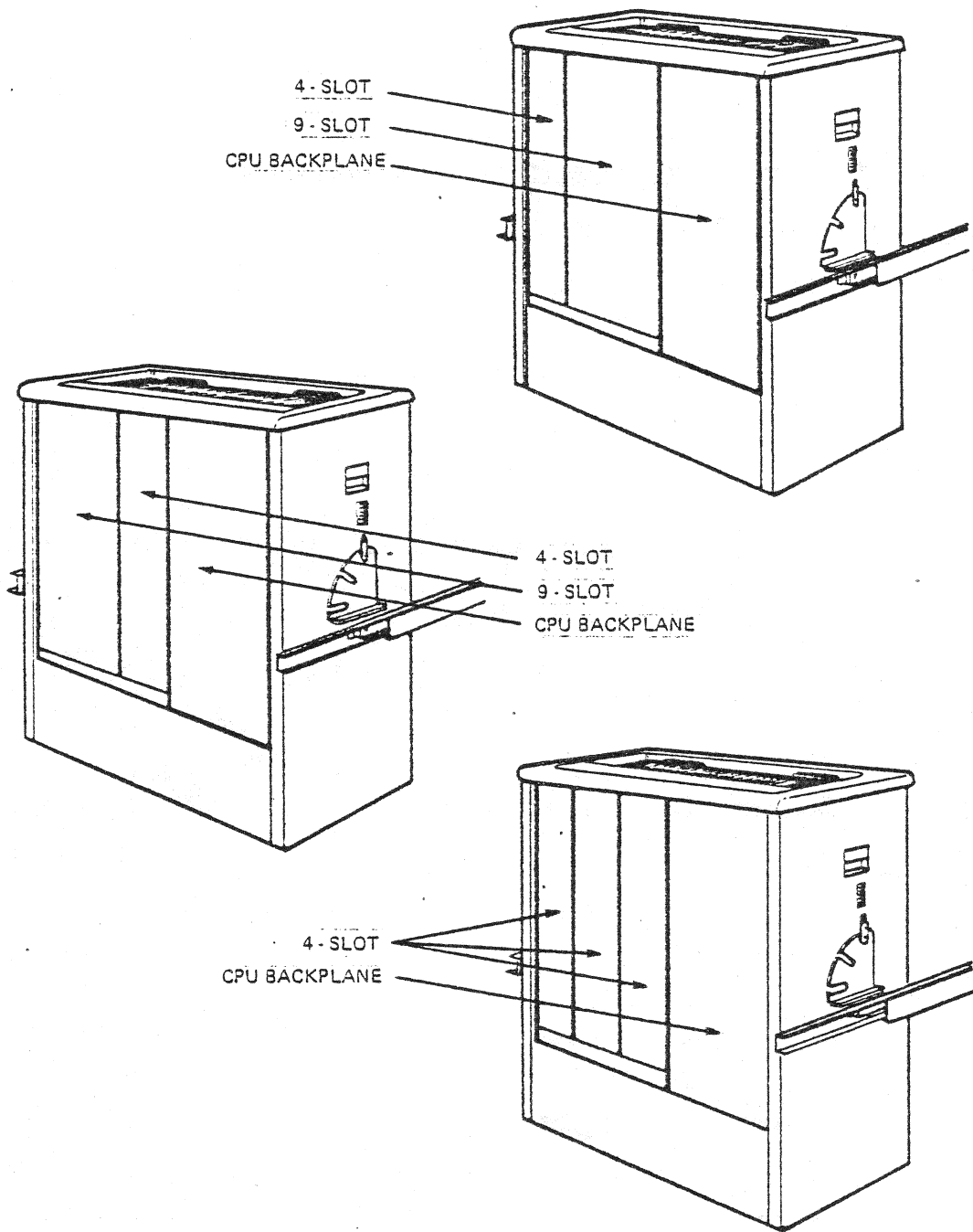
Designation	Type	Slot Columns	Rows	Modules
DD11-CK	single	4	6	2 quad-height and 2 quad/hex-height
DD11-DK	double	9	6	2 quad-height and 7 quad/hex-height

Table 5-2 Backplane Assembly Types

Option Number	Total Slot-Columns
one DD11-DK	9
one DD11-CK and one DD11-DK	13
three DD11-CK	12

#### 5.5.1 Optional Backplane Configurations

Figure 5-12 shows three configurations of the DD11-CK (4 slot) and DD11-DK (9 slot) backplanes installed in the mounting box.



TK-3467

Figure 5-12 Optional Backplane Configurations

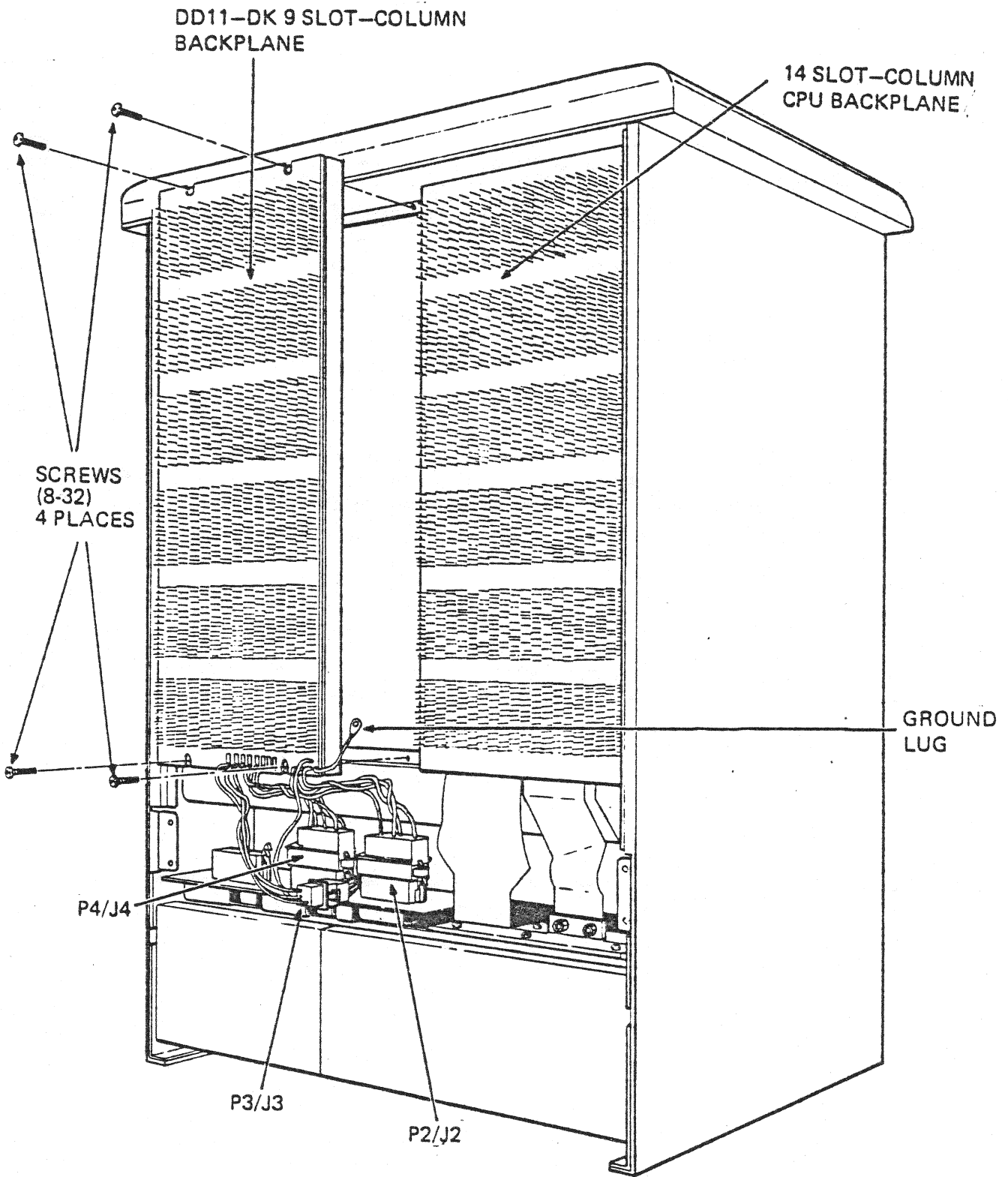
### 5.5.2 Backplane Assembly Installation

To install the DD11-CK or DD11-DK backplane assembly, perform the following procedures:

- 1a. In the PDP-11/X44 system cabinet perform steps 1 through 3 and steps 5 through 9 of paragraph 5.1.1.
- 1b. When the BA11-A mounting box is attached to the slide assemblies, perform steps 1 through 3 and 4b of paragraph 5.3.1.
2. Release the pawl retractors on each side of the mounting box and tilt the box 90° to the maintenance position.
3. Perform steps 3 and 4 of paragraph 5.4.1.
4. Position the backplane assembly on the mounting rails so that the tapped holes in the rails are aligned with the backplane mounting holes (Figure 5-13).

#### NOTE

The backplane harness includes a ground lead with a lug attached which must be installed under the mounting screw.



TK-4403

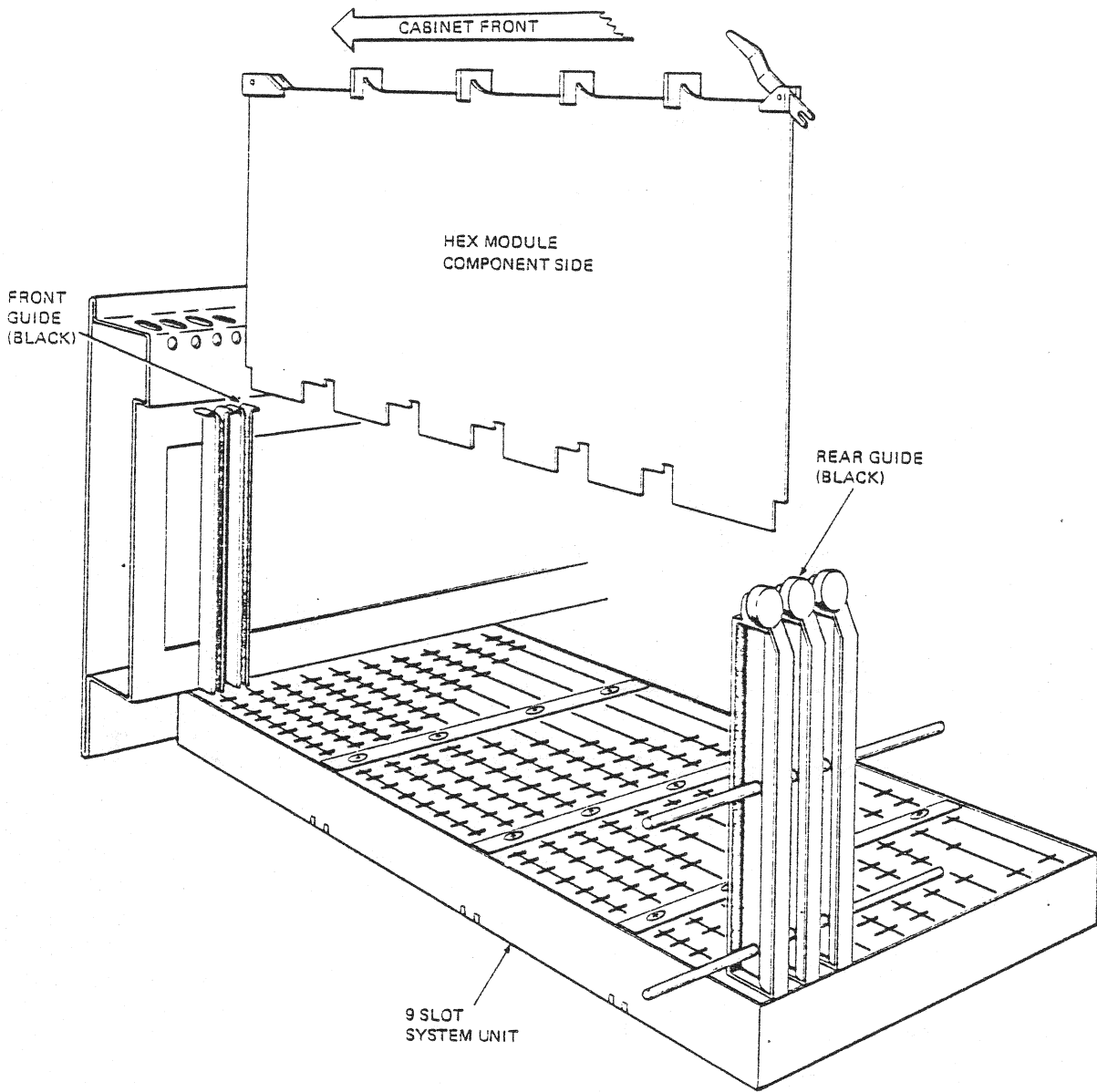
Figure 5-13 Backplane Assembly Mounting

6. Install the four (8-32) screws that are supplied with the backplane assembly. Do not tighten the screws.
7. Lower the mounting box to its normal horizontal position and insert a hex-height module into the module guides that are aligned with the slot columns on each side of the backplane assembly (Figure 5-14).

NOTE

The backplane assembly can be shifted in position to enable the module connectors to be properly aligned with the module slots.

8. Raise the mounting box to the maintenance position and tighten the four (8-32) screws that were installed in step 4.
9. Install the backplane wiring harness connectors P2, P3 and P4 into the power distribution connectors J5, J4 and J6 respectively. For the DD11-CK backplane assembly, install connector P2 and P3 into connectors J5 and J4 respectively (Figure 5-10).
10. Perform steps 9 and 10 of paragraph 5.4.2.
11. Lower the mounting box to its normal operating position.
12. Remove the hex modules used for alignment in step 7.
13. Install the Unibus jumper module, SPC modules and Unibus terminator modules.
14. In the PDP-11/X44 system cabinet, perform steps 5 through 7 of paragraph 5.1.1 and steps 18 and 19 of paragraph 5.1.3.
15. In the PDP-11/44 slide mounted system, replace the top cover of the mounting box using the four (6-32) screws.
16. Perform step 12 of paragraph 5.4.2.



TK-1404

Figure 5-14 Backplane Assembly Alignment

### 5.5.3 Backplane Connector Assignments

The connectors in the backplane are classified into three categories: standard Unibus, modified Unibus and small peripheral control (SPC) connectors. Particular areas of the backplane are reserved for the different types of connectors as shown in Figure 5-15.

The standard Unibus connectors contain all the Unibus connections. Sections A and B of slot 1 are the beginning of the Unibus in the DD1-CK and DD11-DK and should be occupied by the BC11-A Unibus cable since they are expander backplanes. Sections A and B of slot 9 in the DD11-DK or of slot 4 in the DD11-CK are the end of the Unibus on the backplane. These sections should be occupied by the BC11-A Unibus cable or a terminator module.

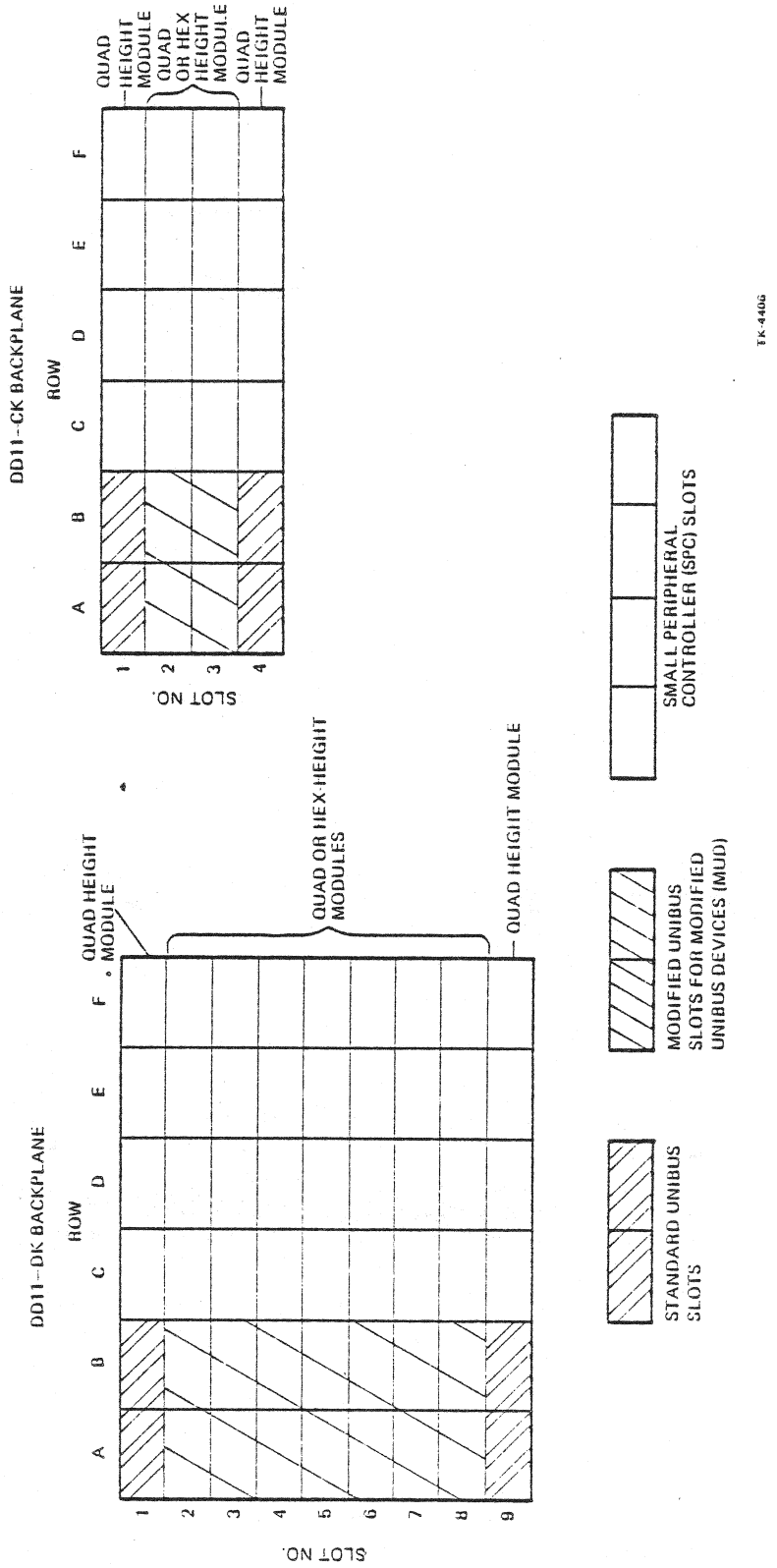


Figure 5-15 Optional Backplane Slot Assignments

TK-4406

#### 5.5.4 NPG and BG Jumper Lead Routing

The NPG line is the Unibus grant line for devices that perform data transfers without processor intervention. Continuity of the NPG line is provided by wire wrap jumpers on the backplane. When an NPR device is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 5-16. Grant priority decreases from slot 1 to slot 9 in the DD11-DK (i.e., slot 1 has the highest priority and slot 9 the lowest).

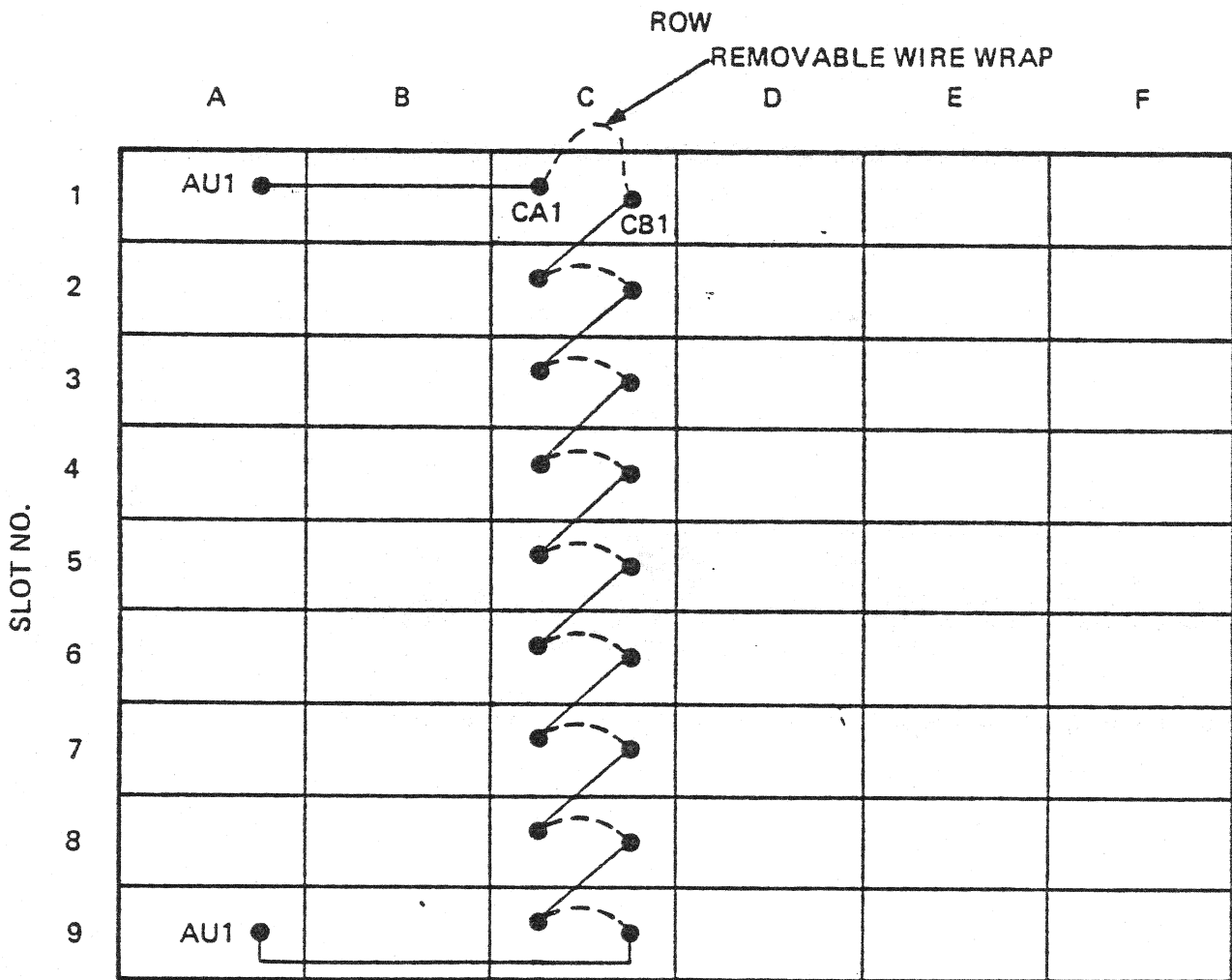
#### NOTE

If an NPR device is removed from a slot, the jumper wire from CA1 to CB1 must be reconnected.

The bus grant lines (BG4:BG7) for devices requiring processor intervention during data transfers are routed through each small peripheral control section in slot D. Each of the four GRANT signals is routed on a separate line. Grant priority for each level decreases from slot 1 to slot 9.

#### NOTE

A bus grant jumper card (G727 G7270, or G7273) must be placed in connector D of any unoccupied SPC section. If an SPC section is left open, bus grant continuity will be lost.



TK-4407

Figure 5-16 NPG Jumper Leads Routing

#### 5.5.5 Standard and Modified Backplane Locations

Figure 5-17 shows the pin designations of the standard and modified Unibus connectors. The modified Unibus differs from the standard Unibus in that certain pins have been redesignated. Some ground connections, BUS GRANT signals and the NPG signal have been removed from the modified Unibus and have been redesignated with core memory voltage pins, battery backup voltage pins for MOS memory, parity signal pins, several reserved pins and test point pins.

Dual height modules that are standard Unibus compatible must not be placed in the Unibus sections.

#### 5.5.6 SPC Backplane Locations

The small peripheral control sections (C, D, E and F) collectively contain all the Unibus lines as well as power voltages (+5 V, +15 V, -15 V). These sections can be used by hex-height or quad-height modules containing the control logic for peripheral devices. Figure 5-19 shows designations for the SPC connectors.

#### 5.5.7 Backplane Power Connections

Power is supplied to the backplane via a wire harness that connects to the power distribution board with the power supply. The wires run from the backplane to a set of Mate-N-Lok connectors that run directly into the distribution board.

The power harness from the DD11-DK contains two large connectors (15-pin Mate-N-Lok) and one small connector (6-pin Mate-N-Lok). The DD11-CK backplane has only one 15-pin connector and one 6-pin connector. The connector pin locations are shown in Figure 5-20 and the signal assignments for each pin are listed in Table 5-3 (DD11-CK) and Table 5-4 (DD11-DK).

STANDARD UNIBUS  
PIN DESIGNATIONS

Side Pin	ROW A		ROW B	
	1	2	1	2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 SO	GND	MSYN L	GND

MODIFIED UNIBUS  
PIN DESIGNATIONS

SIDE PIN	ROW A		ROW B	
	1	2	1	2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	-15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	.5 (CORE)

NOTE:  INDICATES A REDESIGNATED PIN.

TK-4409

Figure 5-17 Standard and Modified Backplane Pin Assignments

		ROW C		ROW D		ROW E		ROW F	
SIDE	PIN	1	2	1	2	1	2	1	2
	A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
	B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
	C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
	D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	88SY L	FO1 N1
	E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
	F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
	H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
	J	A INT 8	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
	K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT 8
	L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
	M	TP	D07 L	AINT ENBA	BG6 SO	A1N	AOUT HIGH	INTR L	FO1 M2
	N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
	P	HALT REQ	D05 L	TP	BG5 SO	A10 L	A07 L	ABR OUT	FO1 P2
	R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
	S	PB L	D00 L	TP	BG4 SO	ASEL 6	ASEL 0	FO1 M2	FO1 P2
	T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
	U	+15/+8	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
	V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

TK-4410

Figure 5-18 SPC Backplane Pin Assignments

Table 5-3 Power Connector Signal Assignments for DD11-CK

15-Pin Mate-N-Lok Connector

Pin	Signal	Wire Gauge	Color
1	+5 V	No. 14	Red
2	+15 V	No. 18	Gray
3	+20 V	No. 18	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	-	-
6	+15B	No. 18	Green
7	Ground	No. 14	Black
8	Ground	No. 14	Black
9	Spare (not connected)	-	-
10	Spare (not connected)	-	-
11	Spare (not connected)	-	-
12	+5B	No. 14	Red
13	-15 V	No. 18	Blue
14	-5 V	No. 18	Brown
15	-15B	No. 18	White

6-Pin Mate-N-Lok

Pin	Signal	Wire Gauge	Color
1	LO GND	No. 14	Black
2	LTC (line clock)	No. 18	Brown
3	DC LO	No. 18	Violet
4	AC LO	No. 18	Yellow
5	Spare (not connected)	-	-
6	Spare (not connected)	-	-

Table 5-4 Power Connector Signal Assignments for DD11-DK

15-Pin Mate-N-Lok Connector 1

Pin	Signal	Wire Gauge	Color
1	+5 V	No. 14	Red
2	+15 V	No. 18	Gray
3	+20 V	No. 14	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	-	-
6	Spare (not connected)	-	-
7	Spare (not connected)	-	-
8	Ground	No. 14	Black
9	Ground	No. 14	Black
10	Spare (not connected)	-	-
11	Spare (not connected)	-	-
12	+5B	No. 14	Red
13	Spare (not connected)	-	-
14	-5 V	No. 18	Brown
15	Spare (not connected)	-	-

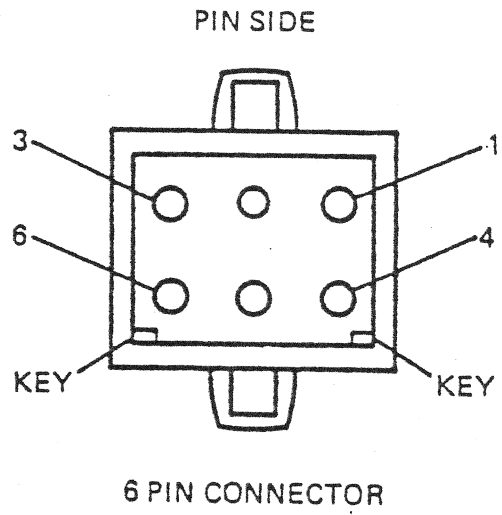
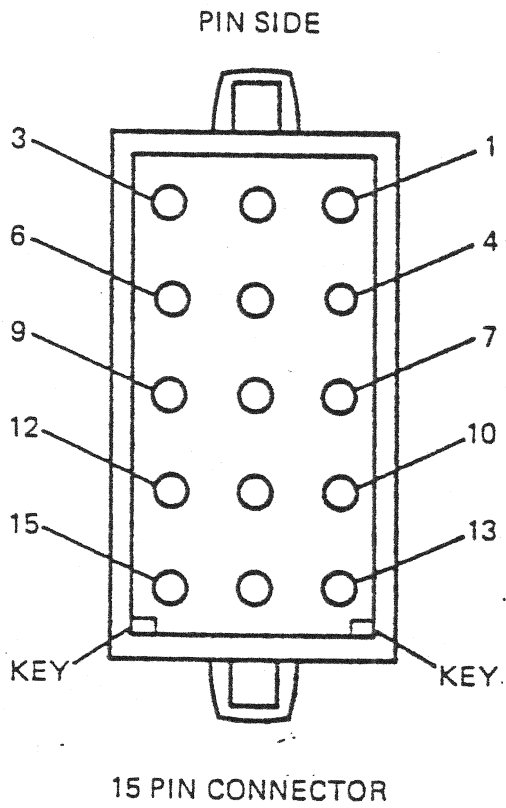
15-Pin Mate-N-Lok Connector 2

Pin	Signal	Wire Gauge	Color
1	+5 V	No. 14	Red
2	Spare (not connected)	-	-
3	+20 V	No. 14	Orange
4	+5 V	No. 14	Red
5	Spare (not connected)	-	-
6	+15B	No. 18	White
7	Spare (not connected)	-	-
8	Ground	No. 14	Black
9	Ground	No. 14	Black
10	Spare (not connected)	-	-
11	Spare (not connected)	-	-
12	Spare (not connected)	-	-
13	-15 V	No. 18	Blue
14	Spare (not connected)	-	-
15	-15B	No. 18	Green

Table 5-4 Power Connector Signal Assignments for DD11-DK (Cont)

6-Pin Mate-N-Lok Connector

Pin	Signal	Wire Gauge	Color
1	LO GND	No. 14	Black
2	LTC (line clock)	No. 18	Brown
3	DC LO	No. 18	Violet
4	AC LO	No. 18	Yellow
5	Spare (not connected)	-	-
6	Spare (not connected)	-	-



TK-4411

Figure 5-19 Backplane Power Connector Pin Designations

All block diagrams  
in 11/44 H/B are wrong

## Reader's Comments

PDP-11/44 System User's Guide  
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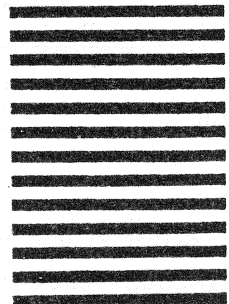
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E

AP gives access to 8085 processor  
A then halts.

B & boots as per front panel

B<sub>L</sub> DEV & for other boots

T for self test, if CONSOLE  
printed then O.K. If not replace MPMA  
board

T/E Console test, means  
8085 can communicate with CPU

T/A

E/M 6 examines CPU error reg.

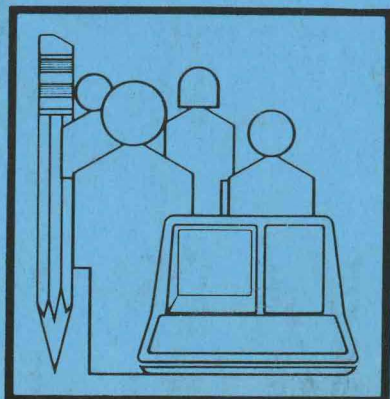
M7092 switch forward

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