CHAPTER 5
RL8A PROGRAMMING INFORMATION

5.1 GENERAL DESCRIPTION

The RL8A controller consists of a single hex-height M8433 module. It interfaces the PDP-8 OMNIBUS with the RL01/RL02 disk drive bus and contains the control, monitor, and data handling logic for disk operation. The RL8A can handle up to four drives via a daisy-chained I/O cable. A PDP-8 can handle two RL8A controllers, providing control for up to eight drives.

The RL8A has six addressable registers that are detailed in Section 5.2. The PDP-8 computer communicates with the controller by accessing these registers using Input Output Transfer (IOT) instructions which have a format of 6XXX. The device codes X60X and X61X are assigned to the first controller. If there is a second controller, it uses device codes X62X and X63X. The specific instructions that cause a response in a controller are shown in Table 5-1. The instructions are used to monitor and control the controller and are not used to transfer data. Data is transferred using Direct Memory Access (DMA) operation via data break cycles on the OMNIBUS. The result is an exchange of data between the controller and memory directly, one 12-bit word at a time. The controller has a silo which can buffer up to 16 words. The controller can transfer 12-bit words to the disk as 12-bit words or can transform them into 8-bit bytes by dropping the high order four bits in each word. The controller can transfer data coming from the disk onto the OMNIBUS as 12-bit words or it can group the data as 8-bit bytes and fill in the remaining four bits as zeros. The advantages and disadvantages of both the 8-bit and 12-bit mode are covered in Paragraph 5.4.

Table 5-1 RL8A Instruction Set

OCTAL CODE *	MNEMONIC	FUNCTION
6600	RLDC	Clear controller, all registers, AC and flags. (Do not use to terminate a disk function.)
6601	RLSD	Skip on function done. Then clear if set to a one.
6602	RLMA	Load break MA register from AC 0:11
6603	RLCA	Load command register A from AC 0:11
6604	RLCB	Load command register B from AC 0:11, execute command
6605	RLSA	Load sector address register from AC 0:5
6607	RLWC	Load word count register from AC 0:11
6610	RRER	Read error register into AC 0, 1, 2, 10, 11

Table 5-1 RL8A Instruction Set (Cont)

OCTAL CODE *	MNEMONIC	FUNCTION
6611	RRWC	Read word count register into AC 0:11
6612	RRCA	Read command register A into AC 0:11
6613	RRCB	Read command register B into AC 0:11
6614	RRSA	Read sector address register into AC 0:5
6615	RRSI	Read silo word into AC 0:11
6617	RLSE	Skip on composite error, then clear if set to a one.

The RL8A controller is capable of performing eight operations. These are listed briefly in Table 5-2 and detailed in Paragraph 5.3.

Errors and error recovery are covered in Paragraph 5.5.

Table 5-2 RL8A Controller Commands

Function Code	Operation
0	Maintenance
1	Reset
2	Get Status
3	Seek
4	Read Header
5	Write Data
6	Read Data
7	Read Data Without Header Check

5.2 ADDRESSABLE REGISTERS

5.2.1 Command Register A

Command Register A is a 12-bit register used during the Seek, Read Data, and Write Data commands. The register is loaded by an RLCA (6603) command and may be read by an RRCA command (6612). Initialize from the bus will clear this register and the other addressable registers.

5.2.1.1 Command Register A During a Seek Command – To perform a Seek function, it is necessary to provide cylinder address difference, head select, and head direction information to the selected drive as indicated. Figure 5-1 shows the bit layout and Table 5-3 describes the bit format.

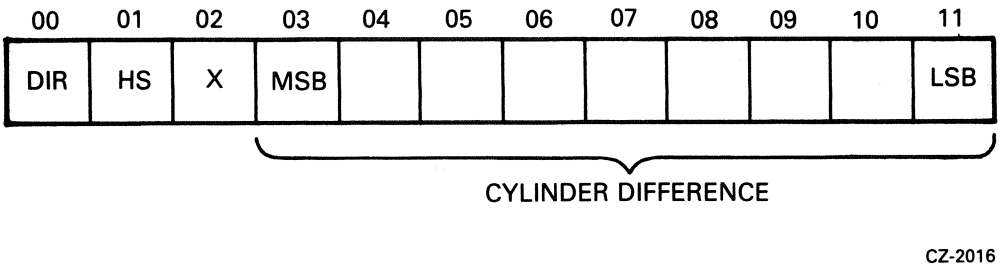


Figure 5-1 Command Register A During a Seek Command

Table 5-3 Command Register A Bit Description for Seek Commands

Bit	Name	Function
AC0	Direction (DIR)	This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move toward the spindle (to a higher cylinder address). When the bit is cleared, the heads move away from the spindle (to a lower cylinder address). The actual distance moved depends on the cylinder address difference (bits 3-11).
AC1	Head Select (HS)	Indicates which head (disk surface) is to be selected. A one indicates the lower head; a zero, the upper head.
AC2	–	Spare
AC3:11	Cylinder Address Difference	Indicates the number of cylinders the heads are to move on a seek.

5.2.1.2 Command Register A During Read or Write Data Command – For a Read or Write operation, the Command Register A is loaded with part of the address of the first sector to be transferred (cylinder address and head select). This information is transferred to the disk address register along with the contents of the Sector Address register to make the complete address of the sector. Figure 5-2 shows the bit layout and Table 5-4 describes the bit format.

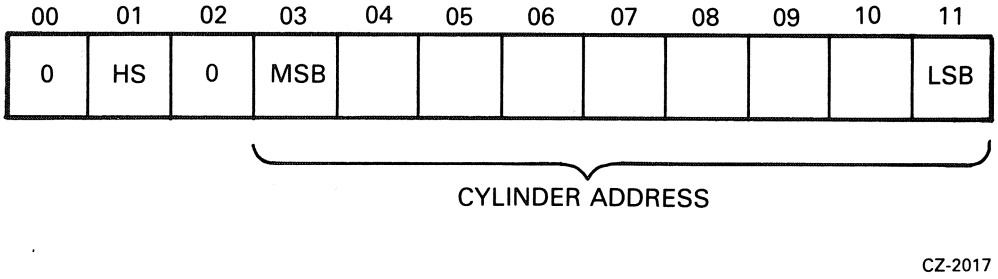


Figure 5-2 Command Register A During a Read/Write Data Command

Table 5-4 Command Register A Bit Description For Data Transfer Commands

Bit	Name	Function
AC0	–	Must be zero
AC1	Head Select (HS)	Head-select bit – a one indicates the lower head; a zero, the upper head
AC2	–	Must be zero
AC3:11	Cylinder Address	Cylinder address

5.2.2 Command Register B

Command Register B is a 12-bit register that contains the mode, drive number, extended memory address bits, interrupt enable, and the function code. The RLCB command (6604) is used to load the register and the RRCB command (6613) reads the register. The RLCB command also executes the function. Figure 5-3 shows the bit layout and Table 5-5 describes the bit format.

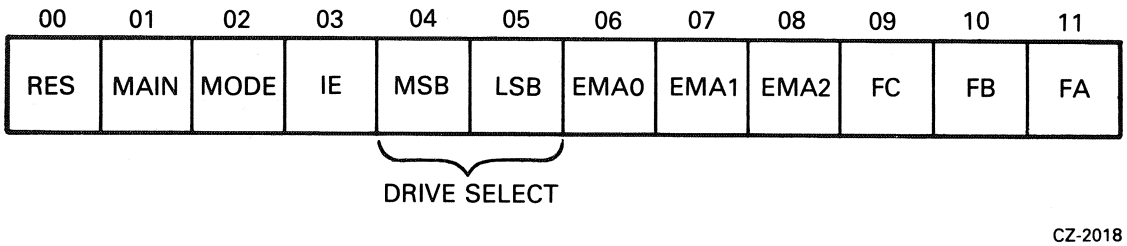


Figure 5-3 Command Register B

Table 5-5 Command Register B Bit Description

Bit	Name	Function
AC0	–	Reserved.
AC1	Maintenance	The contents of the Disk Address (DA) register are looped back to the silo for maintenance purposes. Bit 2 of command register B must also be set for this function to work correctly. See Paragraph 5.3.9.
AC2	Mode	When set, this bit indicates that the data field will be 256 8-bit bytes per sector. When zero, the data field is truncated to 170 12-bit words per sector. This bit must be set when a Maintenance, a Get Status or a Read Header command is to be executed.
AC3	Interrupt Enable (IE)	When this bit is set, the controller is allowed to interrupt the processor at the conclusion of a normal command or error termination.
AC4:5	Drive Select (DS0, DS1)	These bits determine which drive will communicate with the controller via the drive bus.
AC6:8	Extended Memory Addressed (EMA)	These three bits define the memory field location. This allows up to 32K memory locations to be addressed on processors having more than 4K of memory.
AC9:11	Function Code	These bits indicate the command to be executed by the controller/disk subsystem.

Bit 9	Bit 10	Bit 11	Command
0	0	0	Maintenance
0	0	1	Reset
0	1	0	Get Status
0	1	1	Seek
1	0	0	Read Header
1	0	1	Write Data
1	1	0	Read Data
1	1	1	Read Data Without Header Check

5.2.3 Break Memory Address Register

The Break Memory Address (BRK MA) register is a 12-bit register that points to the memory location of the data to be transferred. It is loaded by the RLMA command (6602). The contents of the BRK MA register are automatically incremented as each word is transferred between memory and controller.

The register is cleared by initializing the controller or by loading the register with zeros (Figure 5-4).

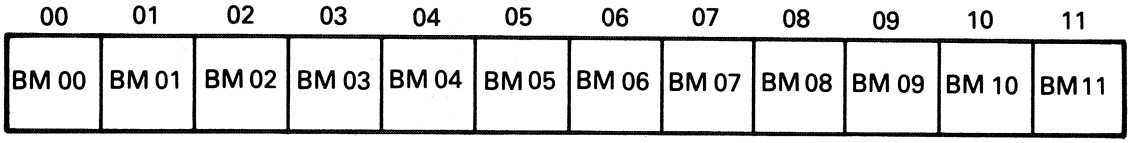


Figure 5-4 Break Memory Address Register

5.2.4 Word Count Register

The Word Count (WC) register is a 12-bit register loaded by the RLWC command (6607) and read by the RRWC command (6611). Before reading or writing data, the word counter is loaded with the two's complement of the number of words to be transferred. As each Direct Memory Address (DMA) transfer takes place, the word counter is incremented and terminates the command on overflow. It can count from 1 to 4096 data words. This corresponds to 24 sectors while operating in 12-bit word mode. In the 8-bit byte mode the transfer is limited to one sector (170 bytes) (Figure 5-5).

NOTE

The disk drive will not do spiral Read/Writes. The program must break up a data transfer if track-to-track Read/Writes are to be done. Between two such data transfers, a seek to the next track or surface must be made.

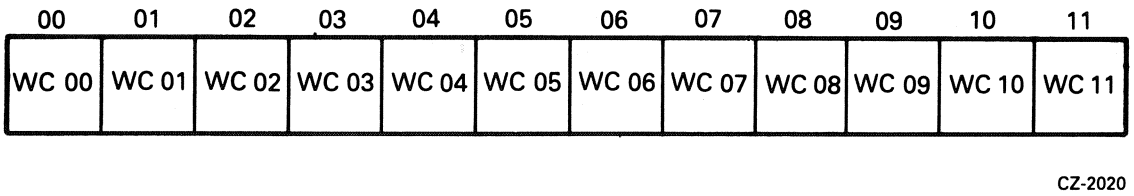


Figure 5-5 Word Count Register

5.2.5 Sector Address Register

The Sector Address (SA) register is a 6-bit register loaded by an RLSA command (6605) and read by an RRSA command (6614). Before executing a Read or Write operation, the sector address is loaded into the SA register (Figure 5-6).

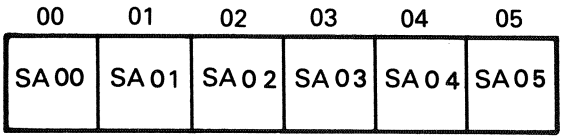


Figure 5-6 Sector Address Register

5.2.6 Error Register

The Error register is a 5-bit register that is read by the RRER command (6610). Bits 0:2 are cleared by initialize or when Command Register B is loaded. Figure 5-7 shows the bit layout and Table 5-6 describes the bit format.

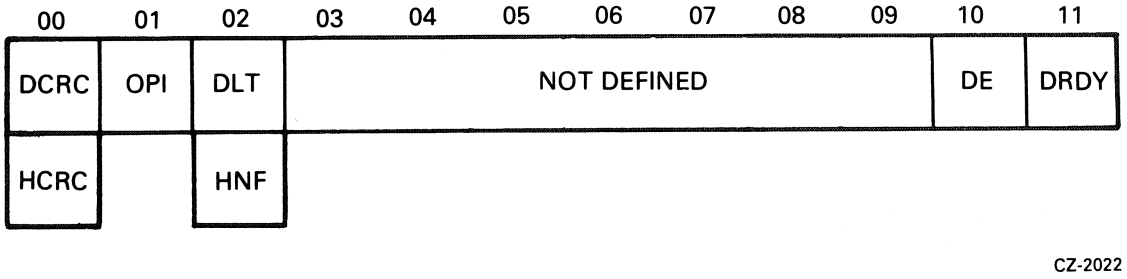


Figure 5-7 Error Register

Table 5-6 Error Register Bit Description

Bit	Name	Function
AC0	Data CRC (DRCR) or Header CRC (HCRC)	If OPI is cleared and this bit is set, the CRC error occurred in the data (DCRC). If OPI is set and this bit is also set, the CRC error occurred on the header (HCRC).
AC1	Operation Incomplete (OPI)	When set, this bit indicates that the current command was not completed within 200 ms. It is also used in conjunction with bits 0 and 2 of this register.
AC2	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a write if the silo is empty and the word count is not yet zero (meaning that no word was available for writing). OPI will not be set.

Table 5-6 Error Register Bit Description (Cont)

Bit	Name	Function
AC2	Data Late (DLT) or Header Not Found (HNF)	This bit is set during a write if the silo is empty and the word count is not yet zero (meaning that no word was available for writing). OPI will not be set. This bit is set during a read if the silo is full and the word count is not yet zero (meaning that the word being read could not enter the silo). OPI will not be set. When this bit and OPI are both set, then a 200 ms timeout occurred while the controller was searching for the correct sector to read or write (no header compare - HNF).
AC0:2	Error Code	Summary **Error** / **Bits** 00 01 02 DLT 0 0 1 OPI 0 1 0 HNF 0 1 1 DCRC 1 0 0 HCRC 1 1 0
AC10	Drive Error (DE)	This bit is tied directly to the Drive Error interface line. When set, it indicates that the selected drive has flagged an error. The source of the error can be determined by writing a Get Status command. The DE bit is cleared with a Reset command to the drive.
AC11	Drive Ready (DRDY)	When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a Seek operation is initiated and set again when the Seek operation is completed.

5.2.7 Silo Data Buffer

The RRSI command (6615) is used to transfer the contents of the silo data buffer to the AC. The silo data buffer contains four different types of information.

5.2.7.1 Data Buffer Contents Following a Get Status Command – When a Get Status command is executed and a status word is returned to the controller, the contents of the silo data buffer appear as shown in Figures 5-8 and 5-9. Figure 5-8 shows the bit layout of the error/status bits for the first RRSI command. Figure 5-9 shows the bit layout of the remaining error/status bits when a second RRSI command is executed. Table 5-7 describes the error/status bits for the first data buffer read, and Table 5-8 describes the error/status bits for the second data buffer read.

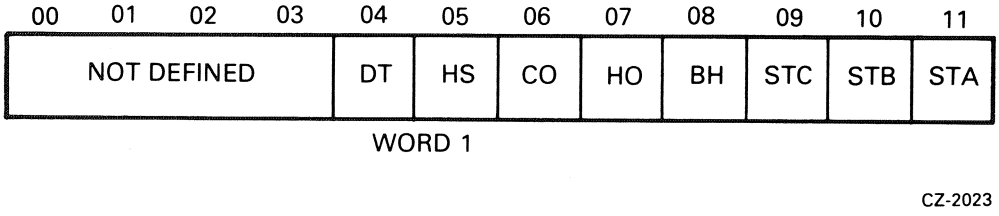


Figure 5-8 Silo Buffer for Status Word 1

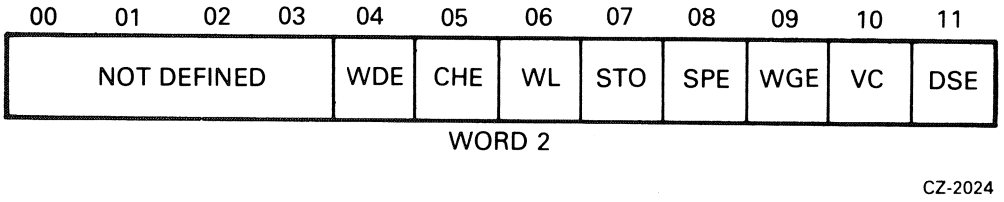


Figure 5-9 Silo Buffer for Status Word 2

5.2.7.2 Silo Data Buffer Contents Following a Read Header Command – When a Read Header command is executed, six 8-bit bytes are stored in the silo as six 12-bit words. The first two are header words and contain the sector address, head select, and cylinder address information. The second two words are zeros. The last two words contain the header CRC information. All six words are read by the RRSI command (6615) (Figure 5-10).

5.2.8 Register Summary

Figure 5-11 is a bit and function summary of the addressable registers.

5.3 CONTROLLER COMMANDS

The RL8A controller is capable of performing eight operations by responding to the function code in the low order three bits of Command Register B. In many cases it is necessary to load other registers prior to loading the function code into Command Register B. No registers should be loaded unless the controller is ready. This condition can be checked by using the appropriate IOT instruction that checks the function done status or by using the interrupt mode.

Table 5-7 Silo Data Buffer Word 1 of Get Status Command

Bit(s)	Name	Function
AC0:3	–	Undefined
AC4	Drive Type	A zero indicates an RL01; a one, an RL02.
AC5	Head Select (HS)	Indicates currently selected head. A zero indicates the upper head; a one, the lower head.
AC6	Cover Open (CO)	Set when the drive access cover is open or the dust cover is not in place.
AC7	Heads Out (HO)	A one indicates that the heads are over the disk; a zero indicates that the heads are home.
AC8	Brush Home (BH)	Set when the brushes are home.
AC9:11	State Bits	These bits define the state of the disk drive.

State Bit Definitions

Bit C	Bit B	Bit A	Definition
0	0	0	Load State
0	0	1	Spin-up
0	1	0	Load Heads
0	1	1	Brush Cycle
1	0	0	Seek (Track Counting)
1	0	1	Lock-on (keeping on track)
1	1	0	Unload Heads
1	1	1	Spin-down

Table 5-8 Silo Data Buffer Word 2 of Get Status Command

Bit(s)	Name	Function
AC0:3	–	Undefined
AC4	Write Data Error (WDE)	This bit is set when the write gate is on but no transitions were detected on the write data line.
AC5	Current Head Error (CHE)	This bit is set when write current is detected in the heads but the write gate has not been asserted.
AC6	Write Lock (WL)	Set when the drive is write-protected.
AC7	Seek Time Out Error (SKTO)	Set when the heads do not come on track in the required time during a seek operation, or when the heads drift off track and do not return within 1.5 seconds.
AC8	Spin Error (SPE)	Set when the spindle does not come up to speed within 40 seconds or when the spindle speed is too high.
AC9	Write Gate Error (WGE)	Set if write gate is asserted and one or more of the following conditions are true. 1. Drive is not "Ready to Read/Write" 2. Drive is write-protected 3. Drive is sensing a sector pulse 4. Drive has another error asserted
AC10	Volume Check (VC)	Set when a new cartridge has been loaded or when the power has been cycled down, then up. This bit is reset by a Reset command.
AC11	Drive Select Error (DSE)	Set when one or more drives has/have the same number (unit select plug) or have responded to the same number.

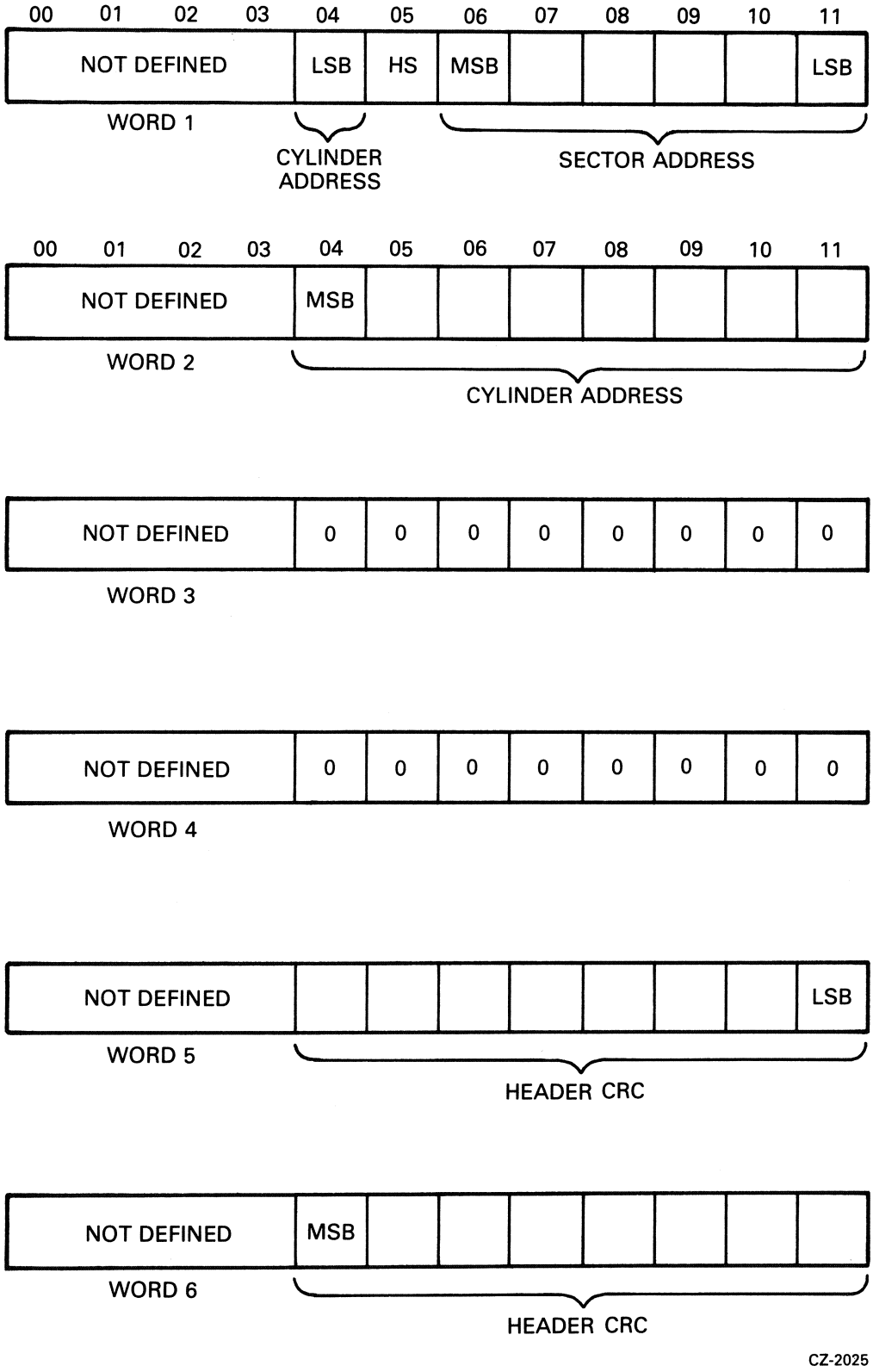
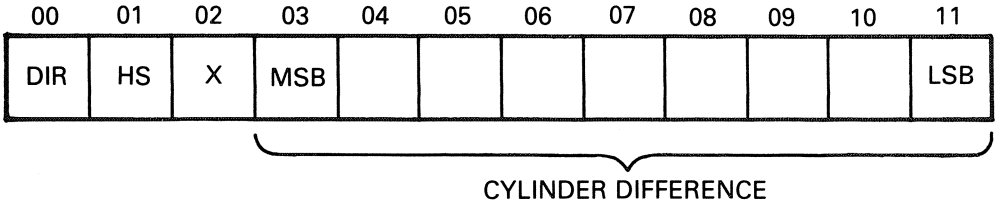
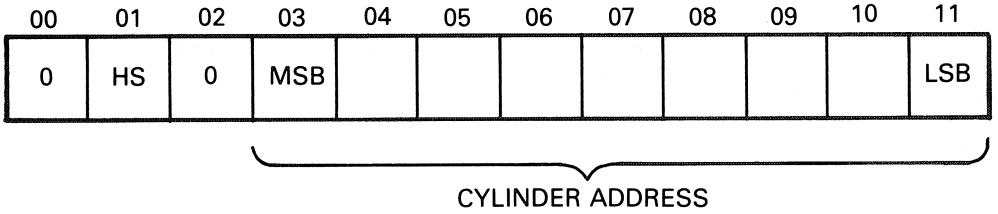


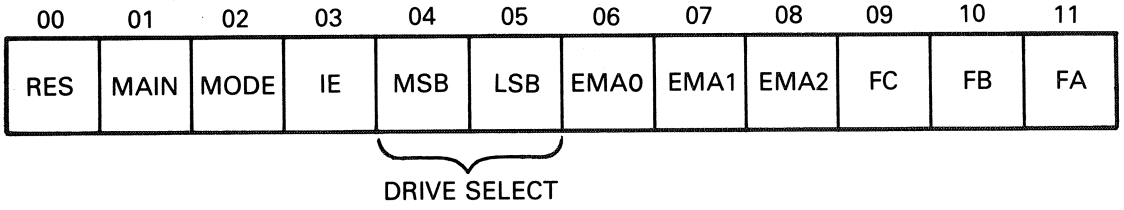
Figure 5-10 Silo Buffer for Header Words



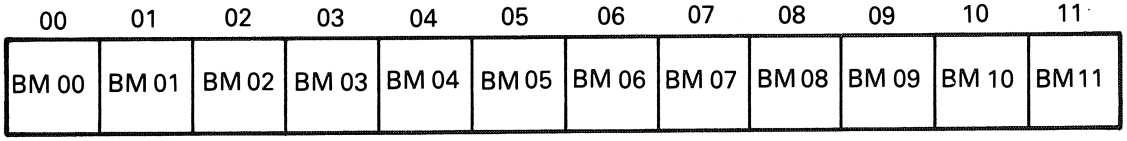
CZ-2016



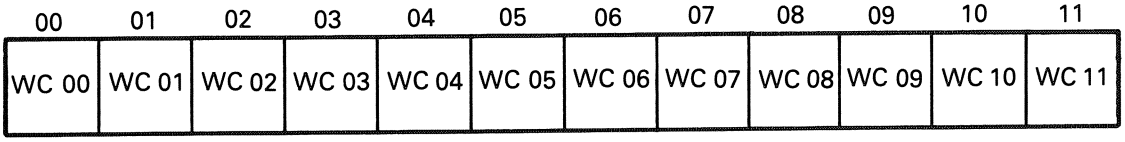
CZ-2017



CZ-2018

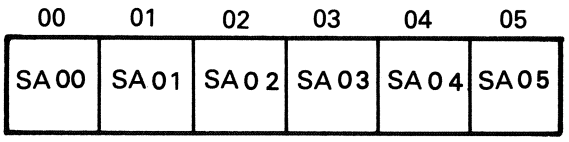


CZ-2019

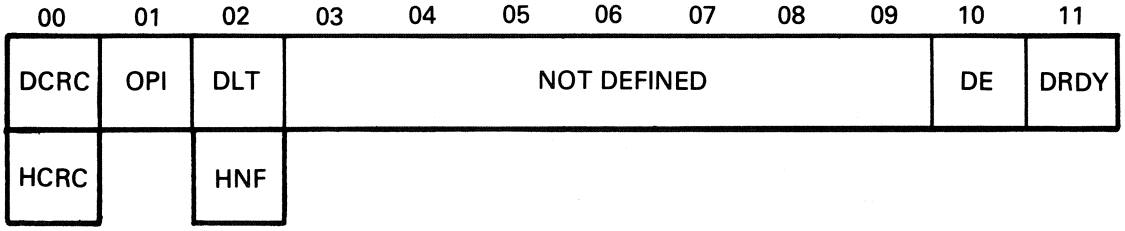


CZ-2020

Figure 5-11 Register Summary (Sheet 1 of 3)



CZ-2021



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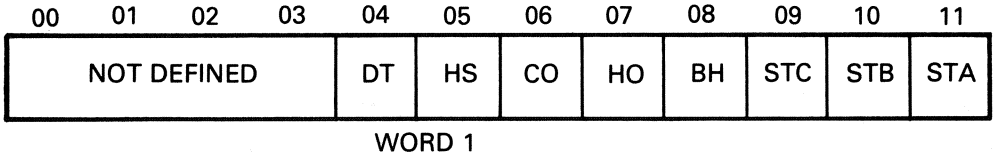

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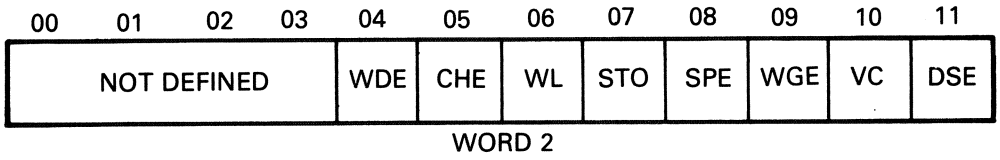

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Figure 5-11 Register Summary (Sheet 2 of 3)

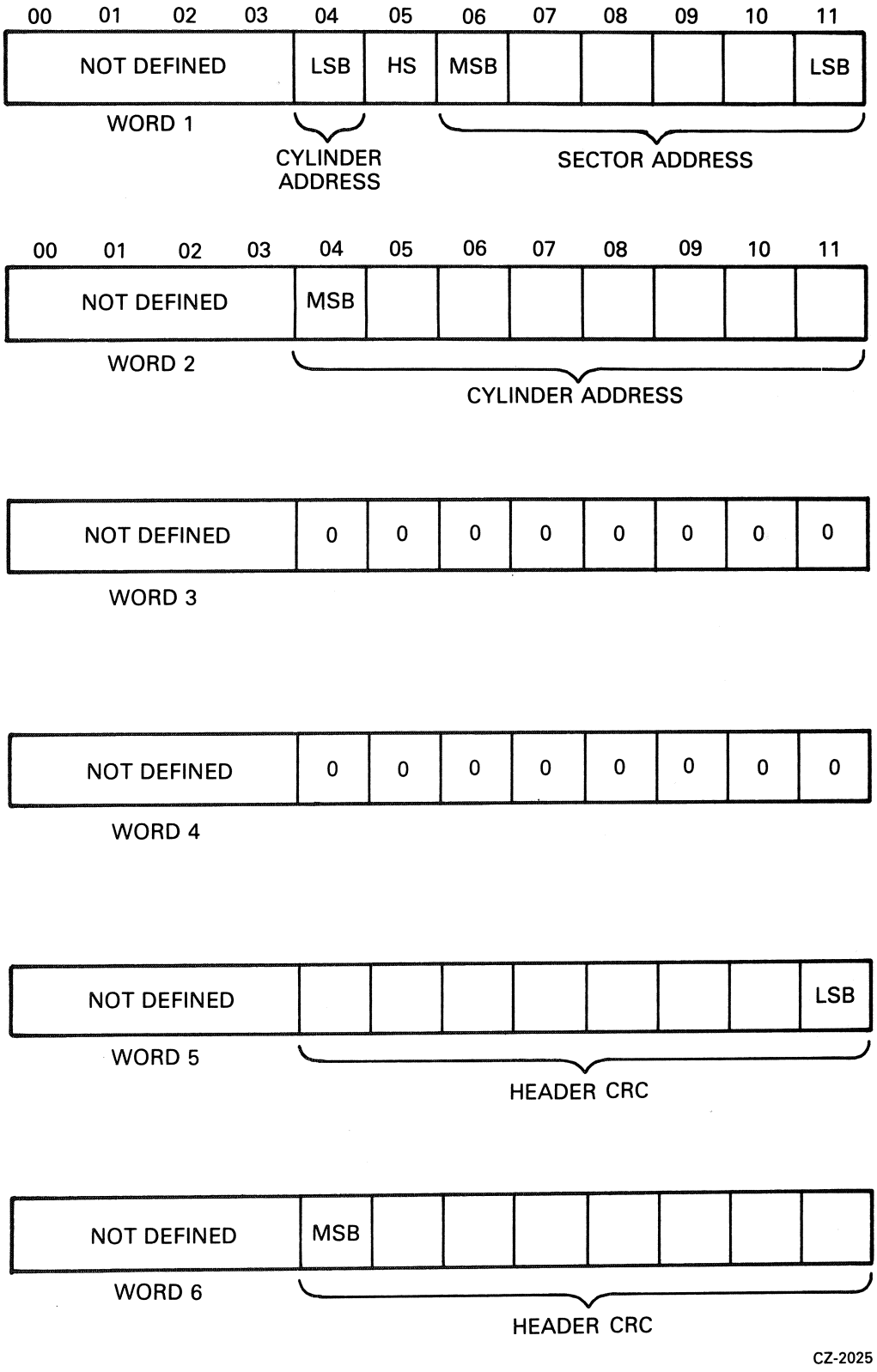

Figure 5-11 Register Summary (Sheet 3 of 3)

5.3.1 Maintenance Command

This command tests the controller by causing it to perform the following tasks.

- The controller requests a data word from memory via the OMNIBUS using the Break Memory Address (BRK MA) register as an address. When the controller receives this word, the BRK MA and the Word Count (WC) register are both incremented.

- The data word is bubbled through the silo, serialized and transferred (in 8-bit mode) through the CRC-generating logic where two more 8-bit bytes are appended. This 24-bit data stream goes through the write data precompensation logic and then is looped back and brought in as if it were read data from the drive. The data passes through the phase-locked loop and data separator logic and into the silo where it is converted back to parallel (eight bits per word), and bubbles through the silo to be available to the OMNIBUS.

- The controller requests three memory accesses and transfers the three words back to memory using the BRK MA register as a pointer. The BRK MA register and WC register are incremented for each transfer. The words are now available for the program to check for diagnostic purposes.

- The above processes repeat and the cycle continues until the WC register equals zero.

Prior to starting this command it is necessary to load the following registers.

- The BRK MA register should be loaded with the address of the first word of data to be transferred to the controller. The next three words of memory will receive three words of data from the controller.

- The WC register should be loaded with the desired count (in two's complement form). A complete cycle takes four counts.

- The Command Register B should be loaded with 10X0 or 14X0. This sets the mode bit to indicate 8-bit mode. The maintenance bit is a zero. The function code is 000. The remaining bits are irrelevant.

5.3.2 Reset Command

This command is used to reset all of the error bits in the selected drive unit. It does not reset any conditions in the controller nor does it cause any head movement in the drive. Prior to executing this command, the Sector Address Register and Command Register A must be cleared by using appropriate IOT instructions.

5.3.3 Get Status Command

The Get Status command reads the 16-bit status word from the selected drive and transfers it into two 8-bit bytes in two consecutive words in the silo. The computer can then extract them with two IOT RRSI instructions. The format of the bits are shown in Paragraph 5.2.7.1. Prior to performing a Get Status command it is necessary to clear both the Sector Address Register and Command Register A. When Command Register B is loaded with the function code, the appropriate drive-select bits should be set, the interrupt enable bit should be set if desired, and the mode bit must be set for 8-bit mode. The controller should be ready before performing any of these load register operations but the drive does not have to be ready.

5.3.4 Seek Command

The Seek command is used to move the heads or to select the other head on the selected drive. Prior to executing the seek command, the Sector Address Register should be cleared and Command Register A should be loaded with a direction bit, a head-select bit, and cylinder difference word. Command Register B is then loaded with the drive-select bits and the seek function code. The controller will send a command to the selected drive to cause it to start a seek operation. The controller will become ready and can then perform another command even though the drive is still seeking.

If the drive attempts to move the head past the innermost or outermost tracks, the head will retreat from the guard band and stop at the first even-numbered track it encounters.

5.3.5 Read Header Command

The Read Header command will read the first header encountered on the selected drive and load the header into six consecutive word locations in the silo, one 8-bit byte per word. The computer can then extract this information with IOT RRSI instructions. The format of the information is shown in Paragraph 5.2.7.2. A check is performed on the header that is read.

5.3.6 Write Data Command

The Write Data command requests data from memory, one word at a time, via the OMNIBUS using the DMA mode. It then transfers the data through the controller silo buffer to the selected drive. The data is written at the specified sector data area. This operation continues, incrementing both the Break Memory Address register and the Word Count register once for each OMNIBUS transfer until the Word Count register reaches zero.

Prior to starting this command it is necessary to position the head over the desired track using a Seek command. Then the registers should be loaded as follows:

- The Break Memory Address register with the address of the first memory word to be transferred,
- The Sector Address register with the address of the first sector to be written,
- The Word Counter register with the two's complement of the number of words to be transferred,
- The Command Register A with the head-select bit and the cylinder address word,
- The Command Register B with a mode bit (8-bit or 12-bit mode), interrupt-enable bit (optional), drive-select bits, extended memory address bits, and the Write Data function code.

The Write Data command will then read headers and perform header checks until the desired header is located. After the header is checked, the data is transferred. The header check includes a header CRC check. There is no implicit seek performed, so if the selected head is not positioned over the desired track, the desired header will not be found and an OPI error will occur. If only a partial sector is written, the remainder of the sector is written with all zeros. A CRC word (16 bits) is generated and written for each sector automatically. Since the word count is limited to 4096, this means that the maximum amount of data that can be written with one Write Data command is 16 sectors in 8-bit mode. If 12 bit mode is used, a maximum of 170 words (one sector) can be transferred. The hardware will not perform a spiral (mid-transfer) seek. Therefore, if data must be written that would overflow to the next track, it is necessary to write the data to the end of the track, seek to the next track, and then continue to write the remainder of the data.

5.3.7 Read Data Command

The Read Data Command will cause the controller to read data from the selected drive. It will read from the track that is currently under the selected head, starting at the specified sector. The data is transferred through the controller silo buffer. The controller requests DMA transfers to memory via the OMNIBUS. The Break Memory Address and the Word Count registers are incremented once for each 12-bit word transferred over the OMNIBUS. When the Word Count register reaches zero, the Read Data command is terminated. Prior to starting the Read Data command, the head should be positioned over the desired track with a Seek command. Load the registers as follows:

- The Break Memory Address register with the address of the first location in memory to which the data is to be transferred,
- The Sector Address register with the address of the first sector from which the data is to be read,
- The Word Counter register with the two's complement of the number of words of data to be read,
- The Command Register A with a head-select bit and a cylinder address word,
- The Command Register B with a mode bit and interrupt-enable bit (optional) drive-select bits, extended memory address bits, and the function code for Read Data.

The Read Data command then reads headers, comparing them to the desired disk address. The data transfer begins when the desired header is found. The header checks include header CRC checks. There is no implicit seek, so if the selected head is not over the desired track, the desired header will not be found and an OPI error will occur.

The RL8A cannot perform a spiral (mid-transfer) seek. If a block of data to be read passes the end of a track and continues on the other surface or on the next cylinder, it is necessary to program a Read Data just to the end of the track. The drive must then Seek to the next track and then continue reading data.

A CRC check is performed on each sector during a Read Data operation.

5.3.8 Read Data without Header Check Command

This command is the same as a Read Data command except that no header check is performed. The next header read is considered a match so that sector is the first sector read. Since no header check takes place, the header CRC is performed.

5.3.9 Maintenance Bit

The maintenance bit in Command Register B enables a path for the serial information leaving the DA register. When this bit is set, the data that is going out to the drive is looped back and shifted into the silo. The data bubbles through the silo and becomes accessible (as two 8-bit bytes) to IOT RRSI instructions. The program can then monitor the operation of the DA register which is not a directly addressable register. This feature must be used only with Reset, Get Status, and Seek commands. Because the DA register is a 16-bit register, the 8-bit mode bit should be set. This insures that the contents of the DA register fit into two 8-bit bytes. The contents of the DA register and the two silo words are illustrated in Figure 5-12. During the loading of the DA register (which occurs on every command), there is more than one input to some of the bit positions. These inputs are ORed together. Normally, Status Register A is cleared before any Reset, Get Status, or Seek command and Control Register A is cleared before any Reset or Get Status command. It is possible to test all the bits in the DA register by using selected patterns in Control Register A and Status Register A.

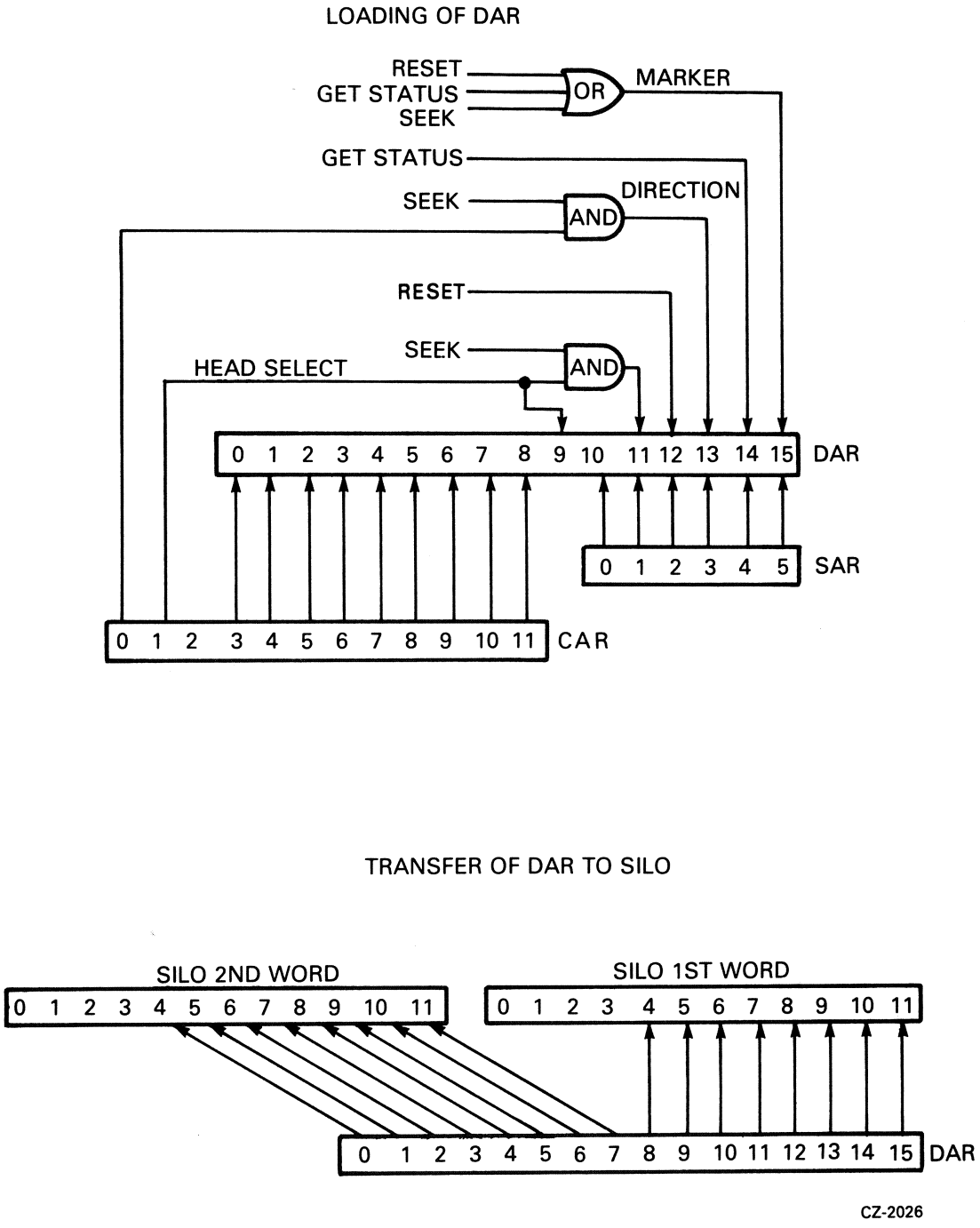

Figure 5-12 Maintenance Mode Bit

5.4 OPERATIONAL CONSIDERATIONS

5.4.1 8-Bit Mode Versus 12-Bit Mode

The disk cartridge is formatted in 8-bit bytes. For instance, the header contains a 16-bit word address, another 16-bit word, then a 16-bit header. The data area is 256 8-bit bytes and the data area CRC is 16 bits. None of these areas are evenly divisible by 12, which is the PDP-8 word length. Therefore, the RL8A controller has the capability of operating in either 8-bit mode or 12-bit mode.

When reading in 8-bit mode, the serial data from the disk is broken into 8-bit bytes and put into the silo with eight bits per word. Since the silo is 12 bits wide, the data goes into the eight low order bit positions and zeros are put into the remaining four high order bit positions. That is the format used when the computer transfers a 12-bit word from the silo to the CPU accumulator or to memory. The 8-bit mode is necessary when performing a Read Header, Get Status, or Maintenance command where 16 bits of data are read. Otherwise, information would be lost.

The 8-bit mode can be used for data on the disk. In such a case, 256 8-bit bytes are read from each sector and transferred to memory as 8-bit words. In some cases, this may be an advantage. For example, if 8-bit ASCII data is being handled, the 8-bit mode is preferable to the 12-bit mode. In most cases, however, the 8-bit mode wastes 33% of the memory space. Because the 12-bit mode uses 12-bit words it uses less memory. In the 12-bit mode, each sector contains 170 words with only 8 wasted bits at the end of each sector.

In the 12-bit mode, the RL8A controller hardware blocks data into 170 words per sector. The operating system for the PDP-8 uses only 128 words per sector, so that while memory is used more efficiently, some disk space is wasted.

5.4.2 Interrupt

The RL8A will interrupt the processor if the Interrupt Enable bit is set and the controller is done. If an error occurs during an operation, the done condition is set.

5.4.3 Seek Operation

If the program does not keep track of the current position of the head (cylinder and surface), and it is desired to read or write from a particular area from the disk, it is necessary to:

- Read Header to obtain the current position of the head,
- Calculate the difference (if any) from the desired position,
- Issue a Seek with the proper difference, direction and head-select information.

5.4.4 Overlapped Seeks

Since a Seek operation does not involve data transfer, it is possible to have one drive seeking while another is transferring data. Only one drive at a time can transfer data, but up to four drives can be seeking simultaneously.

5.4.5 Recovery of Data with Bad Headers

Function 7, Read Data Without Header Check, allows the recovery of data with unreadable headers. If HNF or HCRC errors are repeatedly encountered on a particular sector, and the data is not recoverable by the standard Read command, proceed as follows. Read successive headers until the sector preceding the bad sector is found. Then, within 300 microseconds, issue a Read Data Without Header Check. The data portion of the next sector will be read without either header compare or header CRC check. Data CRC errors will be reported.

5.4.6 Non-Interchangability of Disk Cartridges

5.4.6.1 RL01K/RL02K – These two types of cartridges are physically interchangable but not functionally interchangeable. If a cartridge is installed on the incorrect type of drive, no physical damage will take place and data will not be destroyed. However, the unit will not operate in a normal manner. The symptoms exhibited depend upon the program running at the time. If the system is exhibiting abnormal characteristics, the operator should ensure each drive contains the correct type of cartridge.

5.4.6.2 RL8A/RL11/RLV11/RLV12 – RL01K cartridges are interchangeable with other RL01K cartridges assuming that the RL8A has written the cartridges in 8-bit mode. RL02K cartridges are interchangeable with other RL02K cartridges under the same condition.

5.4.7 Use of Two RL8A Controllers

A PDP-8 system can be configured with two RL8A controllers to increase the capacity of the system up to eight drives. However, if both controllers are trying to perform data transfers at the same time, the throughput capacity of the OMNIBUS may be exceeded. In this case, conflicts (DLTs) will occur.

5.5 ERROR RECOVERY

There are several errors that can be detected and flagged in the RL01/RL02 subsystem. Some of them are considered recoverable. In this case, if the operation is retried, it is possible that the error will not recur and use of the subsystem can continue. Some of the errors are considered fatal, however, because retries may cause damage to the data, media, or equipment. The errors are listed with the recommended reaction in Table 5-9.

The nature of these errors should be considered when determining how many times to retry the operation. For instance, a DLT error could be a hardware system failure but it could also be the result of bus activity due to other I/O devices exceeding the throughput capability. In the latter case, it is likely that the operation will be successful on the first retry. The rate of occurences is a good indicator of overall system performance and an error logging routine should count the rate at which errors occur. A general increase in the rate of DLT errors could indicate that system usage is approaching its throughput capacity in its present configuration.

Another example of applying practical reaction to an error is the handling of an HNF error. It should be retried once. If it recurs, then the head may not be positioned over the correct track. If a Read Header operation is performed and the address from the media is examined, the current cylinder and head can be determined to see if it is a position problem. If not, then possibly there is a bad spot on the media. If there is a bad header, that sector address should be entered into the Bad Sector File and the software should avoid using the original sector.

Whenever an error occurs, the program should log it, along with the contents of the registers, the status of the unit, and whether or not a retry was successful. The more complete the error log, the easier it is to diagnose the cause of errors.

Table 5-9 Errors

Controller Errors	Recommended Reaction
OPI	Retry some practical number of times.
DCRC/HCRC	Retry. Be sure to record the contents of the DA register.
DLT/HNF	Retry. If an HNF error, perform a Read Header and verify cylinder.
Drive Error	Perform a Get Status and check the bits listed below.
Drive Errors	**Recommended Reaction**
DSE	Retry once before notifying operator to verify UNIT SELECT plug.
WGE	Retry.
SPE	Retry.
SKTO	Retry. Wait for 1.5 sec after Reset.
CHE	Fatal. Do not retry.
WDE	Fatal. Do not retry.

5.6 DIFFERENCE SUMMARY (RK05 AND RL01/RL02)

This section may be helpful to users who have used DIGITAL's RK05 disk cartridge subsystem. It points out the differences between programming the RK05 subsystem and programming the RL01/RL02 subsystem.

In general, the RK05 subsystem provides more hardware support of functions while the RL01/RL02 subsystem requires that the software provide some of the functionality. The major differences are explained below.

5.6.1 Spiral Read/Write or Mid-Transfer Seeks

A spiral read/write is a transfer of data that continues past the end of a track. The RK05 subsystem provides hardware support for this by using the hardware to detect the end-of-track condition. The hardware will cause a mid-transfer seek to the next track and then restart the read/write operation at sector 0 of the next track. Note that this seek is either a head switch from the upper surface to the lower surface on the same cylinder with no head positioner movement, or a switch from lower surface to upper surface with a positioner movement to the next cylinder. The RL01/RL02 subsystem hardware cannot handle this. If a read/write operation continues past the 40th sector, the sector counter in the DA register advances to 50 (octal), which is illegal and therefore sets the OPI error flag. It is necessary for the software to 1) prevent this from occurring by calculating the remaining area left versus the amount of data left before the operation or 2) to detect that it has occurred. The software must initiate a separate seek function and initiate a continuance of the read/write function. A head switch from the upper to the lower surface without a positioner movement is considered a Seek in the RL01/RL02 subsystem. After a head switch, the positioner will seek the center of the new track.

5.6.2 Implicit Seeks Versus Explicit Seeks

The RK05 subsystem can perform either implicit or explicit seeks. An explicit Seek is a software-directed seek operation. An implicit Seek is a seek initiated by the hardware at the beginning of a read/write operation if the desired position is different from the present position. The RL01/RL02 subsystem cannot do an implicit seek. The software must ensure that the positioner is over the desired cylinder and that the desired head is selected before starting a read/write operation.

5.6.3 Recalibrate

The RK05 subsystem has a return-to-zero or recalibrate function which causes the positioner to move to cylinder 0. There is no similar function in the RL01/RL02 subsystem. An explicit seek to cylinder zero must be performed. If the current cylinder address is not known and the drive is commanded to seek beyond the outer guard band, this guard band will be detected and the head will retreat to cylinder zero.

5.6.4 Bad Sector File

There is a bad sector file feature on each RL01/RL02 disk cartridge. Its use is explained in Paragraph 1.6. There is no standard Bad Sector File used with the RK05.

5.6.5 Reformatting

The RK05 cartridge can be reformatted in the field while the RL01K/RL02K cartridges cannot. The embedded servo information and Bad Sector File features greatly reduce the need to reformat in the field.

5.6.6 Seek Interrupt

The RK05 will provide two interrupts as the result of a seek operation. The first interrupt occurs as soon as the controller has caused the drive to start its movement, indicating that the controller is free to handle another function. The second interrupt occurs when the drive finishes the seek movement. The RL01/RL02 subsystem does not provide the second interrupt. Thus, the software must perform the proper monitoring of the drive to determine when the seek has been completed.

APPENDIX A
RL11 CONFIGURATION AND INSTALLATION CONSIDERATIONS

A.1 SPC CONSIDERATIONS

The RL11 is a Small Peripheral Controller (SPC) but does not unconditionally fit into any SPC slot. Early SPCs were always quad-height modules or combinations of smaller (single or dual) modules that involved only four rows. Thus, the standard pin assignments applied only to rows C, D, E, and F on a hex-height modules and therefore required that rows A and B be vacant since some SPC slots use rows A and B for UNIBUS cables or power connectors. Some hex-height options require standard UNIBUS pinning on rows A and B and some require Modified UNIBUS Device (MUD) pinning. In the case of the RL11, the only connections used on rows A and B are the +5v and ground. Thus, these rows can be either standard UNIBUS or MUD pinning.

The early SPCs did not utilize Direct Memory Access (DMA) data transfers to/from memory and therefore those signals were not part of the origianl SPC pin assignments. Some of the newer options, such as the RL11, do utilize DMA transfers. There is a new pin assignment called SPC PRIME that includes these signals. If the RL11 is to be used in an older (non SPC-PRIME) slot, then it is necessary to ensure that the following signals are wired on the backplane.

- Pin CA1 – NPG In
- Pin CB1 – NPG Out
- Pin FJ1 – NPR
- Pin CV1 – AC LO
- Pin CU1 – +15v

If the slot has SPC PRIME pinning, then another precaution must be taken. NPG continuity is maintained across an empty SPC PRIME slot by a backplane jumper from pin CA1 to pin CB1. This jumper must be removed whenever a DMA-type option is installed, such as an RL11, and the jumper must be added if the module is removed. This consideration is in addition to the normal Bus Grant Continuity card used in row D of all empty SPC slots.

A.2 CONFIGURATION CONSIDERATIONS

When configuring a UNIBUS system for the best priority assignments, two characteristics of a peripheral option must be taken into consideration. These are the peak word transfer rate and the T1 time (T1 time is a function of the peak transfer rate and the silo size). The RL11 has a peak transfer rate of 256 kHz (3.9 microseconds/word) and a T1 time of 62.4 microseconds. This dictates its position in the priority scheme. The recommended priority scheme is listed below.

CPU
- Memory
- RK11/RK05
- TM11/TU10
- TC11/TU56
- RL11/RL01-RL02
- RJS04
- RM02
- RJP04
- RK611/RK06-RK07
- RP11C/RP03
- RJS03
- TJU16
- RF11/RS11

DB11

Other general configuration rules are:

- On a PDP-11 UNIBUS, a combination of two disk subsystems and a tape or floppy disk subsystem is considered maximum.
- On a PDP-11/70 system, on UNIBUS disk subsystem is considered maximum if there are MASSBUS disks.
- A disk subsystem should not be installed beyond a bus expander.