

**KW11-P
programmable
real-time clock
manual**

1st Printing January 1972
2nd Printing (rev) July 1972

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CHAPTER 1

INTRODUCTION

The KW11-P Programmable Real-Time Clock is an option for the PDP-11 System which provides a method of accurately measuring time intervals. The KW11-P consists of a quad-height module (M7228) that provides programmed real-time interval interrupts and interval counting in several modes of operation. Addition of this module to a PDP-11 System allows hardware interval counting which reduces program instruction time and allows more efficient use of computer time.

Although signals are transferred between the KW11-P module and the Unibus[™], this manual does not describe the operation of the Unibus. A detailed description of the Unibus is presented in the *PDP-11 Unibus Interface Manual*, DEC-11-HIAB-D.

This manual provides the user with the theory of operation necessary to understand and maintain the KW11-P Programmable Real-Time Clock. The level of discussion assumes that the reader is familiar with basic digital computer theory.

The manual is organized into four chapters: Introduction, General Description, Detailed Description, and Programming Information. A set of engineering logic drawings is provided with each KW11-P. The drawing set is identified as D-CS-M7228-0-1, sheets 1 through 5.

- Sheet 1 – Component Placement and Parts Reference (KW-1)
- Sheet 2 – Clock Control (KW-2)
- Sheet 3 – Counter (KW-3)
- Sheet 4 – Interrupt Control (KW-4)
- Sheet 5 – Address Control (KW-5)

CHAPTER 2 GENERAL DESCRIPTION

2.1 INTRODUCTION

The KW11-P provides programmed real-time interval interrupts and interval counting in several modes of operation. It is a quad-height module (M7228) that can be installed in either a DD11-A peripheral mounting unit or in one of the two PDP-11 processor small peripheral controller slots. A wide range of system programming requirements can be met with the KW11-P.

It operates in the single-interrupt mode and the repeat-interrupt mode and also functions as an external event counter. Four selectable clock rates include: 100 kHz, 10 kHz, line frequency, and external clock.

This chapter presents an overview of the KW11-P operation. The discussion is keyed to the block diagram level. A detailed discussion of the KW11-P is presented in Chapter 3.

2.2 FUNCTIONAL UNITS

The major functional units of the KW11-P include a 16-bit synchronous binary up/down counter, 16-bit count set buffer, 9-bit control and status register, clock, gating control, interrupt control, and an address selector (Figure 2-1). The purpose of each of these functional units is as follows:

- 16-Bit Counter** — Counts up or down at four selectable rates and can be read while operating. The interrupt sequence is initiated at zero (underflow) during a count down from a preset interval count. The count-up mode is used to count external events; an interrupt is initiated at zero (overflow).
- 16-Bit Count Set Buffer** — Stores the preset interval count. At underflow, depending on the operating mode, the buffer automatically reloads the counter or is cleared.
- 9-Bit Control and Status Register** — Provides various control and status signals related to the operation of the buffer and counter. These signals are discussed in detail in Chapter 3.
- Clock** — Provides two crystal-controlled signals of 100 kHz and 10 kHz to clock the counter. Two external clock signals are provided: 50/60 Hz line frequency and an analog signal input.
- Gating Control** — Provides input/output signal access for the functional elements of the KW11-P.
- Interrupt Control** — Permits the KW11-P to make bus requests, gain bus control, and generate interrupts. Consists of circuitry to duplicate some of the functions of an M782 Interrupt Control Module.
- Address Selector** — Decodes the address information from the bus and provides gating signals for the selected element (status register, buffer, or counter). Consists of circuitry to duplicate some of the functions of an M105 Address Selector Module.

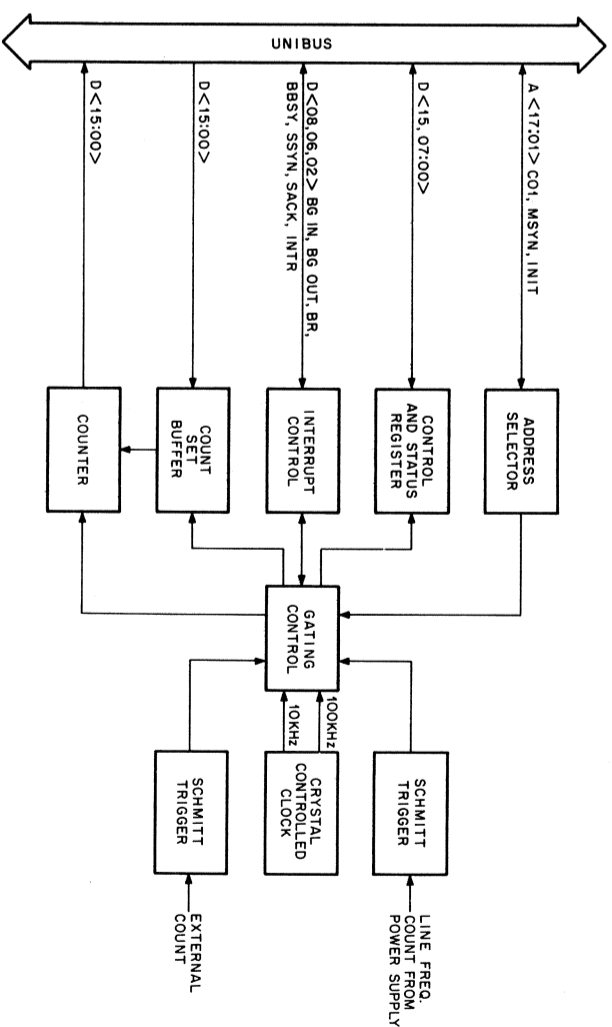


Figure 2-1 KW11-P Programmable Real-Time Clock, Simplified Block Diagram

2.3 MODES OF OPERATION

The KW11-P has three program selectable modes of operation:

- Single-Interrupt Mode** — A program specified time interval is preset and an interrupt is generated at the end of the interval. The time interval, represented as a specific count, is loaded into the counter. Count down or count up is initiated at one of four selectable rates, and at underflow or overflow and interrupt is generated. The clock is stopped and the counter is reset to zero.
- Repeat-Interrupt Mode** — A program specified time interval is preset and repeated interrupts are generated at a rate corresponding to the time interval. The time interval, represented as a specific count, is loaded into the counter. Count down or count up is initiated, and at underflow or overflow an interrupt is generated. The counter is automatically reloaded from the count set buffer and the clock is restarted. At the second underflow or overflow, another interrupt is generated.

(continued on next page)

The sequence is repeated to produce a series of interrupts at program specified intervals. It is possible for a non-recoverable error to occur if the counter underflows or overflows before the previous interrupt has been serviced.

External-Event Counter — The external input is used to clock the counter in the count-up or count-down mode. The counter may be read during operation to determine the number of events that have occurred.

The control and status register, count set buffer, and counter can be addressed. The address selector decodes a specific address. The results of the decoding operation, along with control signal BUS C01, are combined in the gating circuitry to provide a group of control signals that are used on the KW11-P module.

The overall operation of the KW11-P is controlled by signals from the control and status register. This 9-bit register responds to programmed information from the processor. It generates signals to provide the following functions.

- a. Control mode operation.
- b. Control count up/down and count rate.
- c. Start counter.
- d. Indicate counter underflow or overflow.
- e. Provide an interrupt enable signal to the interrupt control logic.
- f. Provide an error signal if a second underflow or overflow occurs in the repeat-interrupt mode before the interrupt generated by the previous underflow or overflow has been serviced. This condition may require restarting of the operation.
- g. Provide a signal to single-clock the counter for maintenance purposes.

The count set buffer receives the preset interval count from the bus via Unibus receivers. Coincident with a load pulse, all 16 bits of input data are transferred to the buffer output. The counter inputs are connected directly to the buffer outputs. The buffer load pulse asserts a counter load pulse that transfers the 16 bits of data from the counter inputs to the counter outputs. The counter is loaded with a preset interval count and is ready for operation. The preset interval count is also retained in the buffer. The counter outputs are connected to the bus with Unibus drivers. A control signal to the drivers transfers the counter output to the bus so it can be read during operation.

The interrupt control contains the logic circuits that permit the KW11-P to gain control of the bus (become bus master) and perform an interrupt operation. Single interrupts or repeated interrupts are generated depending on the mode selected.

The basic interval clock is a 100-kHz crystal-controlled oscillator. Its output is also divided down to provide a 10-kHz clock signal. A signal is provided by the PDP-11 processor power supply as the line frequency (50/60 Hz) count rate. An external clock signal can also be used. Both the external clock and line frequency signals are conditioned by Schmitt triggers. A clock selector/multiplexer provides the desired clock rate in accordance with programmed information.

2.4 INSTALLATION

The KW11-P module plugs into a DD11-A Peripheral Mounting Panel or into a prescribed slot in any of the PDP-11 family of computers. In each case, a wire must be installed to pick up the LTC L signal from the power supply and apply it to the line frequency input of the KW11-P.

When installed, the LTC L input to the KW11-P is located on pin CE1 of the slot into which it is plugged. Connect a piece of 30 AWG wire from this pin (CE1) to the pin designated below for each application.

Application	Pin Number
DD11-A Peripheral Mounting Panel	A03P2
PDP-11/20 Computer (KA11 Processor)	A13P2
PDP-11/45 Computer (KC11 Processor)	A13P2
PDP-11/05 Computer (KD11 Processor)	C01D1
PDP-11/45 Computer (KB11 Processor)	C01R1