

DIGITAL EQUIPMENT CORPORATION									
MAYNARD, MASSACHUSETTS									
ENGINEERING SPECIFICATION									
TITLE D2V11 ASYNCHRONOUS MULTIPLEXOR									
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REVISIONS									
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE			
							APPD	Willis Smith	Willis Smith
							SIZE	CODE	NUMBER
							A	SP	D2V11-0-2
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1.0 General Description

The DZV11 is a multiplexor interface between four asynchronous serial data communications channels and the LSI-11 bus. The DZV11 provides an EIA level interface and enough data-set control to permit dial up (auto answer) operation with modems capable of full duplex operation such as the Bell models 103, 113, 212 or equivalent. The DZV11 does not support half duplex operations or the secondary transmit and receive operations available with some modems such as the Bell model 202. Program compatibility is maintained with the Unibus option, D211-A. The only compatibility exception being the number of serial channels supported. The DZV11 has applications in data concentration and collection systems in front-end systems interfacing to a host computer, and for use in a cluster controller for terminal applications.

The following is a summary of the programmable features offered for each line:

Character length: 5,6,7 or 8 level code

Number of stop bits: 1 or 2 for 6,7,8 level code
1 or 1.5 for 5 level code

Parity generation and detection: Odd, even or none

Operating speed: 50, 75, 110, 134.5, 150, 300
600, 1200, 1800, 2000, 2400,
3600, 4800, 7200 and 9600.

Breaks: Generation and detection

1.1 Available Options:

The DZV11 can be supplied in two different configurations, each designated by a suffix letter (A or B). Each multiplexor configuration utilizes a quad height module designated as the M7957. All input and output leads of the M7957 conform to EIA Standard RS232C and are available on a Berg header.

The required hardware for the DZV11-A option is just the M7957 module. Cabling assemblies to terminals and modem channels are not supplied with this option, but are available in the DZV11-B configuration. Each DZV11-B configuration consists of an M7957 module, BC11U-25 cable assembly, and two accessory test connectors, H329 and H325.

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2.0 Performance Specifications

2.1 Bus Loading:

The DZV11 represents one unit load to the LSI-11 bus.

2.2 Power Consumption

1.15 Amps @ +5 Volts
0.39 Amps @ +12 Volts

2.3 Environmental:

The DZV11 operates in an environment from 5 to 50 degrees centigrade with a relative humidity of 10% or less to 95%.

2.4 Maximum Configurations:

The DZV11 multiplexor is assigned a device address in the floating address space. The floating address space starts at 760010 and extends to 764000. A maximum configuration of DZV11's would not be limited by floating address space, but would be limited by the rules governing an intermediate size system configuration. Therefore, a maximum of seven DZV11 multiplexors may reside in a nine by four backplane. Refer to Section 3.5 for throughput limitations.

2.5 Available Interrupts:

A. Receiver Done Interrupt - occurs every time a character appears at the output of the Receiver Buffer Register and the Silo Alarm is disabled. Can be enabled or disabled from the bus.

B. Silo Alarm Interrupt - occurs after sixteen entries have been made into the Receive Buffer Register by the scanner. This interrupt disables Receiver Done Interrupt and is rearmed when the Receive Buffer Register has been read.

C. Transmit Interrupt - occurs everytime the scanner finds a UART buffer empty condition, and the Transmitter Control Register bit is set for that line. Can be enabled or disabled from the bus.

2.5 Receivers:

The receivers provide serial to parallel conversion of 5,6,7, 8 level code with one start space and at least one stop mark. The character length, number of stops bits,

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parity generation and operating speed are programmable parameters for each line. A Receiver and Transmitter of a corresponding line share the same operating speed with provisions for enabling/disabling of that receive line. Each receiver is double-buffered and has an allowable input distortion of 43.75% on any bit. Also, the accumulated character distortion must not exceed 43.75%. This limits the speed distortion to 4.8% for an eight bit character. Break detection is provided on each receiver. 2.7 Transmitters: The transmitters provide parallel to serial conversion of 5,6,7,8 level code with or without parity. The parity sense when selected can be either odd or even. The stop code can be either 1 or 2 units except when 5 level code is selected. When 5 level code is selected, the stop code can be set to 1 or 1.5 units. The character length, number of stop units, parity generation and sense, and operating speed are programmable parameters for each line. The operating speed for the transmitter is common with the receiver. Breaks are capable of being transmitted on any line. The gross start-stop distortion for a transmitter's TTL output will be less than 2.5% for an eight bit character. 2.8 Baud Rate Generator: The baud rate generator is a MOS/LSI device, which provides the DZV11 multiplexor with full programmable capability for operating speed selection. Each line has an independent generator capable of producing one of fifteen selectable baud rates. Speed tolerance for all rates is less 0.3% with a clock duty of 50% $\pm$ 5%. 3.0 Hardware Description 3.1 Receiver Control: The receiver control section utilizes a forty pin MOS/LSI device for each line to provide serial to parallel assembly of received characters. These devices are designated as a Universal Asynchronous Receiver/Transmitters (UART). In addition to receive character assembly, the UART provides parity checking, break detection and overrun detection. The UART is double buffered, allowing a full character time to remove the received character to a hardware buffer. The UARTs are serviced by a four phase scanner, which runs at a nominal one megahertz rate. Each cycle of the scanner sequentially checks for a new UART Data Available					
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flag. When a flag is found, the scanner deposits the character into a sixteen by sixty-four First In/First Out buffer. This buffer has the following characteristics: If space is available in the FI/FO buffer, the character will be written into the buffer. It will then automatically propagate down to the first available open slot. It will be stored there until a character is removed from the output side, remaining characters propagate toward the output. The character is stored with the following format. The data bits are stored in the low byte or first eight bits, the channel number is stored in two bits, and the status information is stored in three bits (parity, overrun and framing error). Bit 15 indicates a valid entry when it is present. Once any character reaches the output of the buffer, a Receiver Done occurs, thus indicating the service routine must read the buffer to obtain the character. As the character is read, the FI/FO buffer output is incremented, causing the contents to propagate down, now providing the next character stored in the buffer. The software services the Receiver Done flag on either an interrupt or flag checking basis. In either case, characters are serviced out of the FI/FO buffer. As each character is read from the buffer, the next character is presented at the output (assuming that one was in the buffer). The service routine should process all characters in the FI/FO to avoid overhead involved in entering and leaving the service routine. The service routine deals with only the output of the FI/FO buffer and cannot alter or affect the scanner phases. 3.2 Transmitter Control: The transmitter control section utilized UARTS for parallel to serial conversion of transmit characters for each line. The transmitter uses four bits of the low byte of the Transmitter Control Register (TCR) for the enabling of each transmitter of a per-line basis. Setting the bit for a particular line will cause the "pseudo-scanner" to stop at this line if Transmit Buffer Empty (TBMT) is set and thus set the Transmitter Ready bit. If the Transmitter Interrupt Enable bit is set, an interrupt will be generated. Note, that if all TCR bits are clear, the Transmitter Ready bit will be clear, this is a departure from conventional single line unit ready flags. If the TCR bit is set for a particular line, the "pseudo-scanner" will stop when it detects the AND condition of TCR and TBMT for this particular line. Transmitter Ready will then set. An interrupt will be generated if Transmitter Interrupt Enable is set. The service routine should read the TRANSMITTER LINE bits located in the high byte					
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of the Control and Status Register. The routine then loads the appropriate character into the low byte of the Transmit Data Register, and the "pseudo scanner" automatically clears Transmitter Ready and begins searching for another AND condition of TBMT and TCR. The "pseudo-scan" is a four level priority encoder. A sampling clock records the respective states of the AND conditions of TBMT and TCR for the lines. The states are then presented to a priority encoder which produces the Transmitter Line bits and Ready Flag. The clock then stops, waiting for the character to be loaded. Once loading of the Transmit Data Register has occurred, the clock is restarted and a new sample is produced for the priority encoder. Transmitter Line Number three has the highest priority, while line number zero has the lowest.

When operating in interrupt mode, the service routine should check to assure no other lines require servicing before exiting. This would reduce the number of times that the service routine would have to be entered, thus reducing the overhead per character.

Breaks may be transmitted on any line by asserting the corresponding bit in the high byte of the Transmit Data Register. This pulls the output line to a space and holds it there until the bit is cleared. Timing of the breaks must be done by the software.

3.3 Maintenance Provisions:

Three methods of maintenance testing are provided with the DZV11. For systems testing, the multiplexor has a maintenance bit (CSR03) which will internally loopback all the data leads. In this mode, only the data leads are disconnected from the EIA drivers and receivers.

For complete line testing of the EIA logic, an H329 module test connector can be installed on the socket housing of the M7957. This provides staggered loopback in the following manner:

Transmitted Data Line 00	to	Received Data Line 01
Transmitted Data Line 01	to	Received Data Line 00
Transmitted Data Line 02	to	Received Data Line 03
Transmitted Data Line 03	to	Received Data Line 02
Data Term Rdy Line 00	to	Ring & Carrier Line 01
Data Term Rdy Line 01	to	Ring & Carrier Line 00
Data Term Rdy Line 02	to	Ring & Carrier Line 03
Data Term Rdy Line 03	to	Ring & Carrier Line 02

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The third level of maintenance testing is offered at the option acceptance level. An H325 cable test connector can be used with the BC11U cable assembly to provide single line loopback capabilities. The H329 and H325 test connectors are supplied as a basic item of the DZV11-B option only.

3.4 BC11U, Interface Cable:

The interfacing cable for modem and terminal connections to the DZV11-B is provided by the BC11U cable assembly. It consists of four separate cables. Each cable is terminated by a separate DB25-P type connector and a common Berg housing. The housing connects the EIA input/output leads of the module to the appropriate pinning of a DB25-P connector. The following list of connector pins are typical for each line on the assembly.

PIN NUMBER	DESCRIPTION
1	Protective Ground *
2	Transmitted Data *
3	Received Data
4	Request to Send *
7	Signal Ground
8	Carrier
20	Data Terminal Ready
22	Ring Indicator
25	Forced Busy **

* Common Connection
** Optionally Controlled by Request to Send

Request to Send is connected to Data Terminal Ready through a jumper on the module. This allows Request to Send control for full duplex 202 Modem applications. Additional per line jumpers are also provided to allow Request to Send to control Forced Busy.

3.5 Throughput:

Each DZV11 is capable of a throughput rate of 10,970 characters per second. This rate is calculated as follows:

(Bits/Seconds x No. Lines X Direction) divided by Bits/Character. (9600 x 4 x 2) 1/7 equals 10,970 Character/Second.

For a character service routing of 100 usec or less, the device throughput rate can be sustained.

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Programming

The DZV11 contains six addressable registers. They are listed as follows:

- 4.3 Control & Status Register: (CSR) 76XXX0
- The Control and Status Register is a byte and word addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device Master Clear (CSP. 04). The bit assignment is as follows:

Description

00-02

Unused. Read as zero

03

Maintenance

This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is Read/Write.

"Initialize" within the DZV11. A read back of the CSR with this bit set, indicates initialize in progress within the device. This bit is self-clearing. All register, silos and UARTS are cleared with the following exceptions:

within the device. This bit is self-set, indicates initialize in progress, clearing. All register, silos and UARTS are cleared with the following exceptions:

05

B. The high byte of the Transmitter Control Register is not cleared by Master Clear.

C. The Modem Status Register is not cleared by Master Clear.

Master Scan Enable
This Read/Write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, Transmitter Ready

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enable bits and then lower the Processor Status Word to zero. Using this method prevents false interrupts from being generated.

Control & Status Register: (CSR) 76XXX0

The Control and Status Register is a byte and word addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device Master Clear (CSP 04). The bit assignment is as follows:

The Control and Status Register is a byte and word addressable register. All bits in the CSR are cleared by an occurrence of BINIT or by setting device Master Clear (CSR 04). The bit assignment is as follows:

Bit	Description
00-02	Unused. Read as zero
03	<u>Maintenance</u> This bit, when set, loops all the transmitter's serial output leads to the corresponding receiver's serial input leads on a TTL basis. While operating in maintenance mode, the EIA received data leads are disabled. Normal operating mode is assumed when this bit is cleared. This bit is Read/Write.
04	<u>Master Clear</u> When written to a one, generates "Initialize" within the DZVll. A read back of the CSR with this bit set, indicates initialize in progress within the device. This bit is self-clearing. All register, silos and UARTS are cleared with the following exceptions: A. Only bit 15 of the Receiver Buffer Register (VALID DATA), the remaining bits 00 through 14 are not. B. The high byte of the Transmitter Control Register is not cleared by Master Clear. C. The Modem Status Register is not cleared by Master Clear.
05	<u>Master Scan Enable</u> This Read/Write bit must be set to permit the receiver and transmitter control sections to begin scanning. When cleared, Transmitter Ready

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(CSR 15) will be inhibited from setting and the received character buffers (Silos) will be cleared. <u>Receiver Interrupt Enable</u> This bit, when set, permits the setting of CSR 07 or CSR 13 to generate a receiver interrupt request. This bit is Read/Write. <u>Receiver Done</u> This is a read only bit that will set when a character appears at the output of the FI/FO buffer. To operate in interrupt per character mode, CSR 06 must be set and CSR 12 must be cleared. With both CSR 06 and CSR 12 cleared, character flag mode would be indicated. Receiver Done will clear when the Receiver Buffer Register (RBUF) is read or when Master Scan Enable (CSR 05) is cleared. If the FI/FO buffer contains an additional character, the Receiver Done flag will stay cleared a minimum of one micro-second before presenting that character. <u>Transmitter Line Number</u> These read only bits indicate the line number whose transmit buffer requires servicing. These bits are valid only when Transmitter Ready (CSR 15) is set and will be cleared when Master Scan Enable is cleared. Bit 08 is the least significant bit. Unused. Read as zero. <u>Silo Alarm Enable</u> This is a Read/Write bit, when set, enables the silo alarm counter to keep count of the number of characters stored in the FI/FO buffer. The counter will be			
06			
07			
08-09			
10-11			
12			

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cleared when the Silo Alarm Enable bit is cleared. Conditioning of this bit must occur prior to any character reception.

13

Silo Alarm

This is a read only bit set by the hardware after 16 characters have been entered into the FI/FO buffer. Silo Alarm will be held cleared when Silo Alarm Enable (CSR 12) is cleared. This bit will be reset by a read to the Receiver Buffer Register and will not set until 16 additional characters are entered into the buffer. If Receiver Interrupt Enable (CSR 06) is set, the occurrence of Silo Alarm will generate a receiver interrupt request. Reception with CSR 06 cleared, permits flag mode operation of the Silo Alarm bit.

14

Transmitter Interrupt Enable

This bit must be set for Transmitter Ready to generate an interrupt. It is Read/Write.

15

Transmitter Ready

This bit is read only and is set by the hardware. This bit will set when the transmitter clock stops on a line whose transmit buffer may be loaded with another character and whose associated TCR bit is set. The Transmitter Line Number, specified in CSR 08 and CSR 09, is only valid when Transmitter Ready is set. Transmitter Ready will be cleared by any of the following conditions:

1. Master Scan Enable cleared.
2. When the associated TCR bit is cleared for the line number pointed to in CSR 08 and CSR 09.

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3. At the conclusion of the load instruction of the Transmit Data Register (low byte only). If additional transmit lines require service, Transmitter Ready will reappear within a min. of 1.4 usec from the completion of the Transmit Data Register load instruction. The occurrence of Transmitter Ready with Transmitter Interrupt Enable set, will generate a transmitter interrupt request.					
4.4 Receiver Buffer Register: (RBUF) 76XXX2 READ ONLY This is a 16 bit read only register which contains the received character at the output of the FI/FO buffer. A read of the register causes the character entry to be extracted from the buffer and all other entries to bubble down to the lowest unoccupied location. Only the Valid Data bit (RBUF 15) is cleared by BINIT or by setting device Master Clear (CSR 04). Bits 00-14 are not affected. The format of the RBUF register is defined as follows:					
Bit		<u>Description</u>			
00-07		<u>Received Character</u> These bits contain the received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.			
08-09		<u>Received Character Line Number</u> These bits contain the line number upon which the aforementioned character was received. Bit 08 is the least significant bit.			
10-11		Unused. Read as zero.			
12		<u>Parity Error</u> This bit is set if the sense of the parity of the received character does not agree with that designated for that line.			
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13	<u>Framing Error</u>	This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.	
14	<u>Overrun Error</u>	This bit is set if the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer on that line.	
15	<u>Valid Data</u>	This bit, when set, indicates that the data presented in bits 00-14 is valid. This bit permits the use of a character handling program that takes characters from the FI/FO buffer until there are no more available. This is done by reading this register and checking bit 15 until the program obtains a word for which bit 15 is zero.	
4.5 Line Parameter Register: (LPR) 76XXX2 WRITE ONLY			
This register controls the operating parameters associated with each line in the DZV11. The LPR register is a word addressable, write only register. The line parameters for all lines must be reloaded following an occurrence of either BINIT or device Master Clear.			
<u>Bit</u>	<u>Description</u>		
00-01	<u>Parameter Line Number</u>	These bits specify the line number for which the parameter information (bits 3 through 12) is to apply. Bit 00 is the least significant bit.	
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		NUMBER	
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02

Unused. Must always be written as a zero when specifying the Parameter Line Number. Writing this bit as a one will extend the Parameter Line Number field into non-existent lines. Parameters for lines 00 through 03 will not be affected.

03-04

Character Length

These bits are set to receive and transmit characters of the length (excluding parity) as shown below.

04	03
0	0
0	1
1	0
1	1
	5 bit
	6 bit
	7 bit
	8 bit

05

Two Stop Bits

This bit, when set, conditions a line transmitting with 6, 7 or 8 bit code to transmit characters having two stop marks. If the line is transmitting 5 bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.

06

Parity Enable

If this bit is set, characters transmitted on the line have an appropriate parity bit affixed; and characters received on the line have their parity checked.

07

Odd Parity

If this bit is set and bit 06 is set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 06 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 06 is not set, the setting of this bit is immaterial.

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08-11

Speed Code

The state of these bits determine the operating speed for the transmitter and receiver of the selected line.

11	10	09	08	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	1	600
0	1	1	0	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Invalid

12

Receiver Enable

This bit must be set before the UART receiver logic can assemble characters from the serial input line. This bit will be cleared following a BIVIT or device Master Clear.

13-15

(Unused)

4.6 Transmitter Control Register: (TCR) 76XX4

The TCR register is a byte and word addressable register. The low byte of the TCR register contains the transmitter control bits which must be set to initiate transmission on a line. Each TCR bit position corresponds to a line number. For example, TCR bit 00 corresponds to line 00, bit 01 to line 01, etc. Setting of a TCR bit causes the transmitter scanner clock to stop if the UART for this line has a transmit buffer empty condition. An interrupt will then be generated if Transmitter Interrupt Enable is set. The scanner clock will restart when either the Transmit Data Register is loaded with a character or the TCR bit is cleared for the line on which the clock has stopped. TCR bits must only be cleared when the scanner is not running, i.e., Transmitter Ready is set or Master Scan Enable is cleared.

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The TCR bits are represented in bits 00 through 03. These bits are Read/Write and cleared by BINIT or device Master Clear. Bits 04 through 07 are unused and read as zero. The high byte of the TCR register contains the writeable modem control lead, Data Terminal Ready (DTR). Bit designations are as follows: <table><tr><td>Bit</td><td>Name</td></tr><tr><td>08</td><td>DTR Line 00</td></tr><tr><td>09</td><td>DTR Line 01</td></tr><tr><td>10</td><td>DTR Line 02</td></tr><tr><td>11</td><td>DTR Line 03</td></tr><tr><td>12-15</td><td>Unused. Read as zero</td></tr></table> Assertion of a Data Terminal Ready bit puts an ON condition on the appropriate modem circuit for that line. Data Terminal Ready bits are Read/Write and cleared only by BINIT. Jumpers have been provided to allow the Request to Send circuits to be asserted with Data Terminal Ready assertions. 4.7 Modem Status Register: (MSR) 76XXX6 READ ONLY This is a sixteen bit read only register. A read to this register results in the status of the readable modem control leads, Ring and Carrier. The ON condition of a modem control lead is interpreted as a logical one. Bits 04 through 07 and 12 through 15 are unused and read as a zero. Remaining bit designations are as follows: <table><tr><td>Bit</td><td>Name</td></tr><tr><td>00</td><td>Ring Line 00</td></tr><tr><td>01</td><td>Ring Line 01</td></tr><tr><td>02</td><td>Ring Line 02</td></tr><tr><td>03</td><td>Ring Line 03</td></tr><tr><td>04-07</td><td>Unused. Read as zero.</td></tr><tr><td>08</td><td>Carrier Line 00</td></tr><tr><td>09</td><td>Carrier Line 01</td></tr><tr><td>10</td><td>Carrier Line 02</td></tr><tr><td>11</td><td>Carrier Line 03</td></tr><tr><td>12-15</td><td>Unused. Read as zero.</td></tr></table>				Bit	Name	08	DTR Line 00	09	DTR Line 01	10	DTR Line 02	11	DTR Line 03	12-15	Unused. Read as zero	Bit	Name	00	Ring Line 00	01	Ring Line 01	02	Ring Line 02	03	Ring Line 03	04-07	Unused. Read as zero.	08	Carrier Line 00	09	Carrier Line 01	10	Carrier Line 02	11	Carrier Line 03	12-15	Unused. Read as zero.
Bit	Name																																				
08	DTR Line 00																																				
09	DTR Line 01																																				
10	DTR Line 02																																				
11	DTR Line 03																																				
12-15	Unused. Read as zero																																				
Bit	Name																																				
00	Ring Line 00																																				
01	Ring Line 01																																				
02	Ring Line 02																																				
03	Ring Line 03																																				
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12-15	Unused. Read as zero.																																				
SIZE		CODE	NUMBER	REV																																	
A		SP	D2V11-0-2	18																																	
DEC FORM NO EN-01022-16-NJ70-(381) ORA 108																																					

ENGINEERING SPECIFICATION		CONTINUATION SHEET		
TITLE D2V11 ASYNCHRONOUS MULTIPLEXOR				
4.8 Transmit Data Register: (TDR) 76XXX6 WRITE ONLY The TDR Register is a byte and word addressable, write only register. Characters for transmission are loaded into the low byte. TDR bit 00 is the least significant bit. Loading of a character should occur only when Transmitter Ready (CSR 15) is set. That character which is loaded into this register is directed to the line defined in CSR bits 08 and 09. The high byte of the Transmit Data Register is designated as the Break Control Register. Each of the four multiplexor lines has a corresponding break bit for that line. TDR bit 08 represents the break bit for line 00, TDR bit 09 for line 01, etc. TDR bits 12 through 15 are unused. Setting a break bit will force that lines output to space. This condition will remain until cleared by the program. This register is cleared by BINIT or device Master Clear. The Break Control Register can be utilized regardless of the state of the device Maintenance bit (CSR 03).				
SIZE		CODE	NUMBER	REV
A		SP	D2V11-0-2	18
DEC FORM NO EN-01022-16-NJ70-(381) ORA 108				