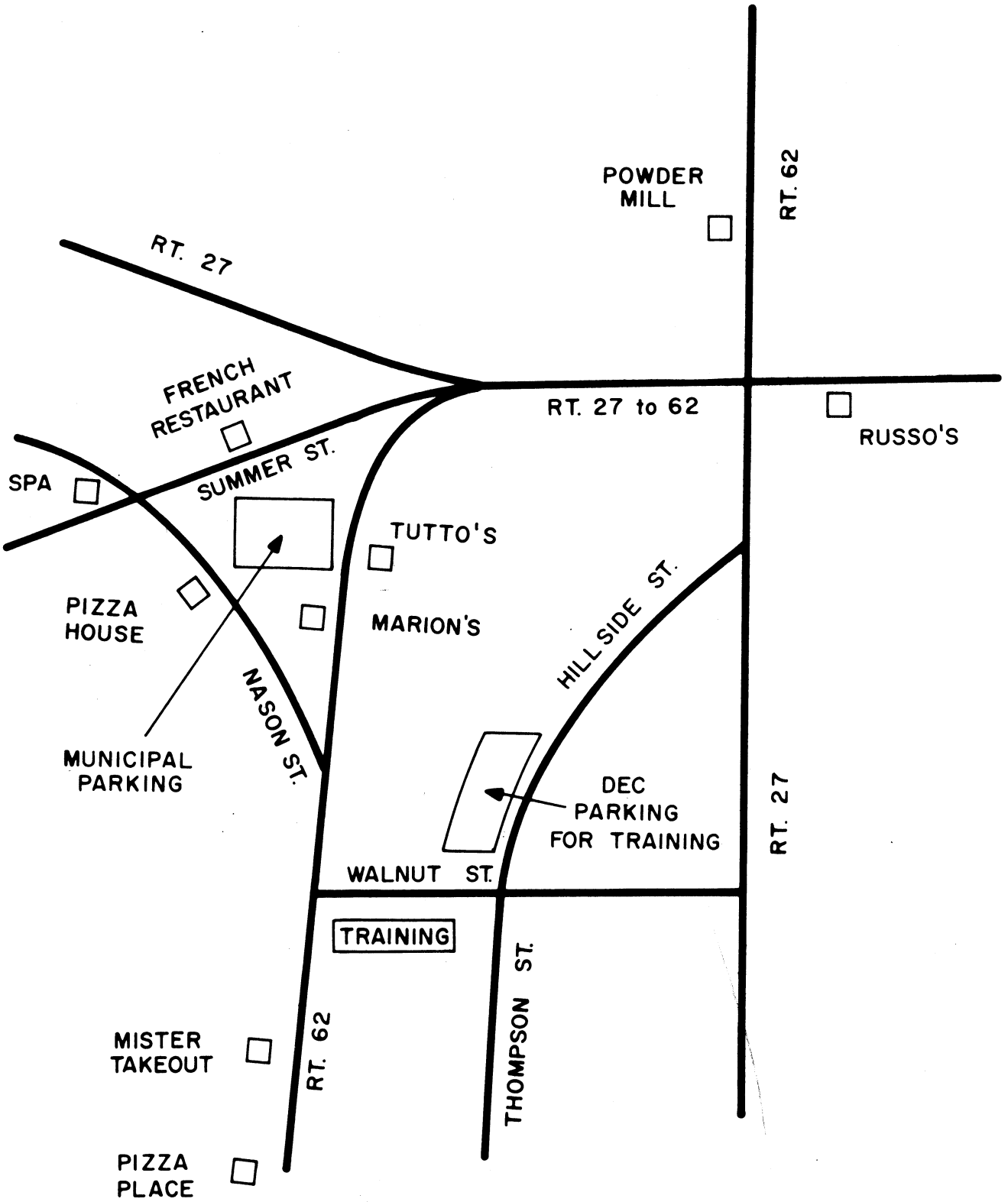


PLACES TO EAT IN MAYNARD

PDP-9 MAINTENANCE HOMEWORK SHEET #1

1. Code the following instructions:

DZM	1723	141723
LAC	50	200050
TAD*	12	360012
LAW	301	760301
CLA*	17	can't do Operate Instruction

2. Decode the following instructions:

130266	JMS=10 + Indirect	JMS * 10266
521234	AND=50 + Indirect	AND * 1234
760132	LAW 132	
750044		

3. List the Memory Reference instructions that can alter normal program sequencing.
JMP, SAD, ISZ, JMS, CAL

4. What will be in the following registers after doing an Examine Next operation?

AR	?
PC	unchanged
MB	word from Core Memory
MA	Address of Location Examined
AC	unchanged because only Examining NOT Running

5. Auto-Indexing can only be used with Memory Reference instructions.

True ✓ False _____

PDP-9 MAINTENANCE HOMEWORK SHEET #2

1. When all inputs to an R111 are negative, its output will be 0 volts.

   Øv/-3v

2. What is the minimum delay through a B310 tapped delay?

   27.5NS

3. What controlling flip flops would have to be set to transfer the contents of the AC to the AR?

   ACO, ARI Mosh Boing open

4. Print KCØ9#17. Address Mixer 2 (B169 module at B-6). Input pin H is tied to gnd. What effect will inputs either positive or negative on pin F have on the output?

   will always be −3

5. KCØ9#19-3. The SAO F/F is a Control Memory F/F.

   True _____ False _____

6. Print KCØ9#14. Function called CI 17. Write a logical expression for CI 17 to be true.

   +1(1) ∨ [PCO(1) ∧ SKIP ∧] ∨ [ADRL(1) ∧ AXS(1)] ∨ [CTIT(1) ∧ IS2] ∨ [SAO(1) ∧ OCH ∨ AUTINX(1)]

7. The following program has been run. What are the contents of the AC, 700, and 150?

600	LAC	700
601	AND	702
602	DAC	700
603	JMS	150
604	HLT	
150	TAD *	601
151	XCT	602
152	HLT	
700	124056	
702	016000	

   C(AC) = 004 000 (8)

   C(700) = 004 000 (8)

   C(150) = 00604 (8)

8. Print KCØ9#1. The MB contains 357162; the following conditions exist: SUB is set, CMPL and CI 17 are present, MQ1 is set. What will be the octal result in the MQ?

   357162 Sub + CMPL cause Complete reversal of states CI 17 does not effect.

PDP-9 HOMEWORK SHEET #3

1. The last memory location in an 8K PDF-9 is 17777 (8).

2. The total time required to complete three sequential main memory cycles is:

   A. 3.0 μsec
   B. 3.025 μsec
   C. 3.075 μsec
   D. 3.25 μsec

3. MC #3. The CP has access to memory, MB 17 is (0), and AM 17 is (1). The voltage on the output of the mixer producing MBS 17 is positive (gnd).

   True ✳ False _____

4. If the SM flip flop is reset, and a CLK is generated (input to MC#2), will the memory logic produce a SYNC CLK (MC #2) and do an MEM?

   Yes

5. The SM Flip flop is set, and a CLK signal is applied to MC#2. The Digit Write Sink flip flop can not be reset. How will this effect the memory cycle?

   no read or write

6. The determining factor for Digit Current during the write portion of a memory cycle is:

   A. The word read from memory
   B. The contents of the MA.
   C. The Word current.
   D. The contents of the MB.

PDP-9 HOMEWORK SHEET #4

1. The CMA contains $24_{(8)}$, the IR contains 10010. If the logic producing REP failed and generated REP at this time, what would be the next Control Memory location to be cycled?

2. Any Control Memory location that sets the Cont. F/F when cycled, will be followed in 188ns by a CLR pseudo-cycle.

   True _____ False _____

3. KC09 #17. G210 at D-4. Given the following inputs, what will be the selected output?
   HV (-), JV(-), HU(-), HS(+), HT(-), HD (-), HE (+), JU (+), JS (+), JT (+), JD (+), JE (+)

   A. CMP-7
   B. CMG-7
   C. CMP-6
   D. CMG-6

4. The Register Display can not display the contents of the selected register when the computer is running due to the speed at which the registers contents is changing.

   True _____ False _____

5. How would an operator normally keep track of the locations in memory that are being deposited into, when manually loading data via the console switches?

6. How many times will the computer perform the instruction in location 201?

200	LAC	205
201	DAC*	16
202	ISZ	206
203	JMP	201
204	HLT	
205	632 000	
206	777 717	
16	401 606	

PDP-9 HOMEWORK SHEET # 6

1. When doing a TAD *12 instruction, when will the AUT INX flip flop be reset?

TI resets when cycling 24 after Last digit in IR goes to Ø

2. If the ADR = Ø SAVE flip flop can not be set, would this effect the proper operation of the SAD instruction?

NO

3. Write a logical expression that describes ADD overflow (ADOF).

$(C0\emptyset\emptyset \cdot \overline{C0\emptyset 1}) + (\overline{C00\emptyset} \cdot C001)$

4. Control Memory location 63 when cycled fails to set the MBI flip flop. This will not effect normal operation of the instruction.

True ____ False ✓

5. What CM location must be cycled to get address 20, when performing a CAL instruction?

24

6. The computer executes the instruction 300 100. The AC contains 400 146 and location 100 contains 643 277.

What will be the result in the AC/ ok
Will there be end around carry?
Will ADD overflow exist?
What will be the sign of the result?
What will the LINK contain?

7. When performing the instruction JMP 500, IR1 is set when CML 12 is cycled. When will IR1 reset?

94 cycles Clear does not reset IR1

8. Write a logical expression to describe when the IR will make up the last 4 bits of the CM address.

9. What instructions would fail to function correctly if CML 23 failed to set the CJIT flip flop?

CAL + JMS

PDP-9 HOMEWORK SHEET #7

1. What instruction/s could fail to operate properly if the AC SIGN flip flop could not be set?

2. Could a negative $12435_{(8)}$ be loaded into the AC in two's complement form using a LAW instruction? If yes, what would be the octal code?

3. The Repeat Switch on the console, when used in conjunction with the Single Instruction Switch and Cont. key, allows the computer to continuously perform the same instruction.

   True _____ False _____

4. The following program is in memory. Single Step Switch is up, Key IO Reset is activated, address 177 is set on the Address Switches and Start Key is activated. What will be in the PC, MB, MA, and AC when the computer halts?

177	DZM IO	PC _____
200	CLC	MB _____
201	HLT	MA _____
		AC _____

9. What will be in the AC after the following program has been run?

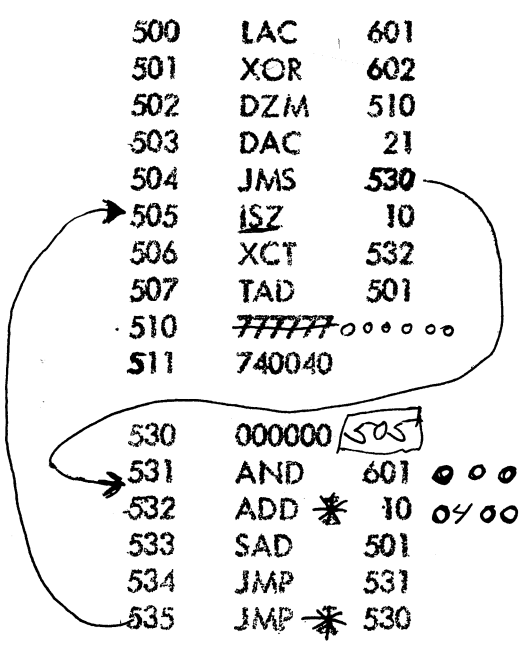
1010	LAC	1010
1011	AND	263
1012	XOR	16
1013	HLT	
16	000 262	
263	741 041	

540, 041

PDP-9/9L Homework

The following program is stored in the computer. The operator does an IO Reset, puts address 500 on the Address Switches, and activates the Start Key. What will be the contents of the Link and Accumulator when the computer Halts?

a) L(1), AC 740674
b) L(1), AC 701356
c) L(Ø), AC 441373
d) L(Ø), AC 740673



500	LAC	601	200601
501	XOR	602	240602
502	DZM	510	140510
503	DAC	21	040021
504	JMS	530	100530
505	ISZ	10	440010
506	XCT	532	400532
507	TAD	501	340501
510	~~777777~~ 000000		
511	740040		
530	000000 505		
531	AND	601	500601
532	ADD *	10	320010
533	SAD	501	540501
534	JMP	531	600531
535	JMP *	530	620530
10	000502		
20	000000		
21	~~746040~~		
601	000041		
602	740001		

000041
740 040
500071
740 673
000040
040061
740040

PDP-9 Homework Sheet #1 - ANSWERS

1. 141 723
   200 050
   360 012
   760 301
   Illegal Instruction

2. JMS * 10266
   AND * 1234
   LAW 132
   CLA OAS HLT or LAS HLT

3. CAL, JMS, JMP
   ISZ and SAD if conditions aremet.
   XCT can if it executes one of the instructions that are listed

4. AR - The address of the location that was examined
   PC - Unchanged
   MB - The word from memory
   MA - The address of the location that was examined
   AC - Unchanged

5. True

PDP-9 Homework Sheet #2 - ANSWERS

1. Øv

2. 27.5 NS

3. ACO, ARI

4. None

5. False

6. +1(1) v [PCO (1) ·SKIP (1)] v [ADRL· AXS (1)] v [CJIT(1)· ISZ]
   v {SAO (1)· [DCH INX + AUT INX (1)]}

7. C(AC) = 004 000
   C (700) = 004 000
   C (150) = 000 604

8. 357 162

PDP-9 Homework Sheet #3 - ANSWERS

1. $17777_{(8)}$

2. B

3. True

4. Yes

5. Memory cycle will not take place (No read or write).

6. D

PDP-9 Homework Sheet #4 - ANSWERS

1. 71

2. False

3. C

4. False - RUN must be reset to use the REPT CLK.

5. Monitor the AR on the REgister Display

6. 49 times

PDP-9 Homework Sheet #6 - ANSWERS

1. When cycling CML 24

2. No

3. $(CO\ \emptyset\emptyset \cdot \overline{CO\emptyset I}) + (\overline{CO\emptyset\emptyset} \cdot CO\emptyset 1)$

4. False

5. 24

6. AC = 243 446
   There will be end around carry
   There will be ADD overflow
   Positive result
   LINK will be set

7. When cycling CML 74

8. $\left[CMA\emptyset\ (1) + REP\right] \cdot CMA1(1)$

9. CAL, JMS

PDP-9 Homework Sheet #7 - ANSWERS

1. SMA, SPA

2. Yes 765 342

3. False

4.
~~DC~~ PC	00200
MB	140 010
MA	00177
AC	000 000