EK-VT220-TM-001

VT220

Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

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INTRODUCTION

GENERAL

This manual provides information to aid field service engineers and other personnel trained by Digital Equipment Corporation in the isolation of VT220 Series terminal malfunctions. To this end, this manual identifies the major circuits within the VT220 Series terminal and provides functional descriptions of those circuits.

Where appropriate, only summarized discussions of operating and programming information is presented; and only to the extent necessary to understand how a specific hardware component or circuit functions.

MANUAL ORGANIZATION

The first three chapters of this manual provide an introduction to the VT220 Series terminal.

Chapter 1 provides a brief introduction to the VT220 Series terminal.

Chapter 2 provides brief descriptions of all VT220 Series terminal controls, indicators, and connectors.

Chapter 3 provides an overview of the VT220 Series terminal system interactions.

Chapters 4 -- 9 provide a functional breakdown and description of the major logic circuits that comprise the VT220 Series terminal.

Chapter 4 explains the CPU logic, responsible for overall control of VT220 Series terminal operation.

Chapter 5 explains the system communication logic, responsible for communication with host and auxiliary devices.

Chapter 6 explains the video logic, responsible for developing output to monitor circuits.

Chapter 7 explains the LK201 keyboard module, responsible for operator input.

Chapter 8 explains the monitor circuits and the cathode ray tube (CRT), responsible for visual output to the operator.

Chapter 9 explains the power supply, responsible for converting ac input to dc potentials needed for terminal operation.

The final part of this manual is made up of appendices which provide specification, differences information, and programming reference data.

Appendix A describes specifications for the VT220 Series terminal.

Appendix B describes differences between the VT220 Series terminal and the VT102 terminal.

Appendix C provides summary of bit values for register devices.

RELATED DOCUMENTATION

The following is a list of related documents for the VT220 Series terminal.

VT220 Series Documentation

Pocket Service Guide - EK-VT220-PS
Programmer Reference Manual - EK-VT220-RM
Programmer Pocket Guide - EK-VT220-HR
Owner's Manual - EK-VT220-UG
Installation Guide - EK-VT220-IN
Video Terminal IPB - EK-VT220-IP
Modem User's Guide - EK-VT22M-UG

Maintenance Print Sets

VT220 (terminal assembly) - MP-01732-01
LK201 (keyboard module) - MP-01395-00
VT22X-AA (modem module) - 70-21205-01

CHAPTER 1
SYSTEM INTRODUCTION

1.1 GENERAL

The VT220 Series terminal is a 1/4-page (up to 24 displayable lines of text) conversational terminal that uses ANSI standard functions to create, store, and edit text.

1.2 PHYSICAL DESCRIPTION

The VT220 terminal (Figure 1-1) consists of up to three units: a monochrome monitor/terminal module, a keyboard, and an optional modem module.

NOTE
Specifications for the VT220 Series terminal are provided in Appendix A.

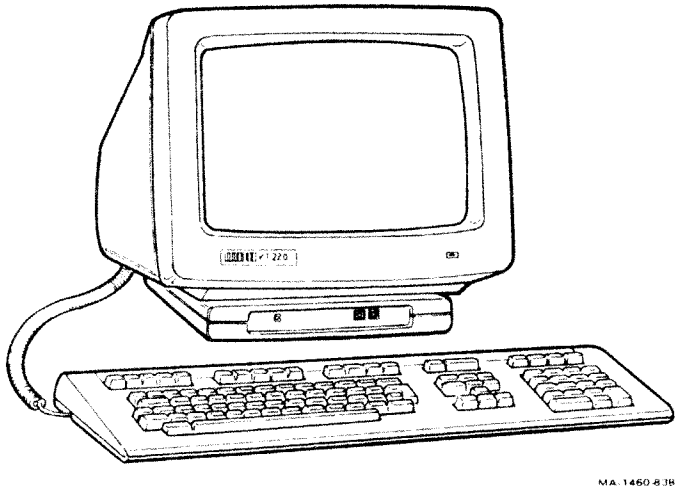


Figure 1-1 VT220 Series Terminals

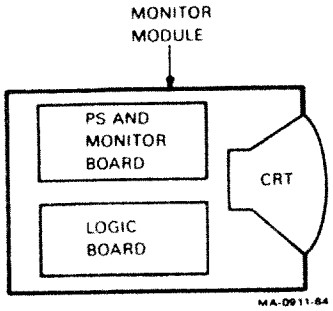


Figure 1-2 Monitor Assembly
Major Components

1.2.1 Monitor Assembly (VT220)

The monitor assembly is the center of the terminal. Figure 1-2 shows the major monitor assembly components.

- Logic board -- contains the components needed to control terminal operation.
- Power supply (PS) and monitor board -- contain the components used to convert ac input to the dc voltages required by the terminal, as well as circuits used to drive the cathode ray tube (CRT).
- Cathode Ray Tube (CRT) -- provides visual output to terminal operator.
- Communication ports -- provide for cable connection between the monitor assembly and a local host (EIA or 20 mA connection), remote host (via a modem), keyboard, and printer.

1.2.2 Keyboard (LK201)

The VT220 terminal uses the LK201 keyboard with the following features.

- Four LEDs -- provide visual indication of operational conditions.
- Typewriter-Style keypad -- contains 57 keys for text entry.
- Auxiliary keypad -- contains 18 keys, including 4 keys which have their function assigned by application programming.

- Editing keypad -- contains 6 screen function keys, and 4 cursor movement keys.

- Top-Row function keys -- are 20 keys aligned across the top of the keyboard which are provided for various functions.

A description of controls and indicators (Chapter 2) explains in greater detail how the LK201 keyboard functions when used with the VT220 terminal.

1.2.3 Modem Module Option (VT22X-AA)

The optional modem provides telephone line communication with a remote host. The module mounts beneath the monitor assembly, raising the actual height of the monitor by about 1 1/2 inches.

1.3 DISPLAY CHARACTERISTICS AND CAPABILITIES

The VT220 terminal's display capabilities are upward compatible with the text capabilities of the VT102 terminal.

The terminal has four text modes. Three modes execute standard ANSI functions (VT100 mode, VT200 mode with 7-bit controls, and VT200 mode with 8-bit controls), and one mode executes Digital private functions (VT52 mode). The following major text capabilities are available within these various modes.

- 24 rows of text with either 80 or 132 characters per row (characters are formed within a 7 X 9 dot matrix in a 10 X 10 cell for 80 characters per row, and within a 7 X 9 dot matrix in a 9 X 10 cell for 132 characters per row)

- Hard character set of 288 characters, with set made up of 256 characters in Digital's control representation mode (CRM) set, 31 characters from Digital's special graphics set, and one character, the reverse question mark, used as an error character

- Down-Line loadable character set

- Reverse video

- Underline

- Double height/width characters, on a line-to-line basis

- Bold/normal intensity

- Character blinking

- ANSI compatible control functions

1.4 COMMUNICATION ENVIRONMENT

The major communications features of the terminal include the following.

- Asynchronous communications at up to 19.2K bits per second
- EIA RS232C host port
- 20 mA host port for passive only 20 mA loop communications
- 9-pin EIA RS232C printer port
- 7- or 8-bit character formats
- BNC connector for composite video output to an optional slave monitor

NOTE

The composite video output is an RS170-like output; however, the use of dc coupling is not in strict agreement with RS170 specifications.

1.5 MAJOR OPERATING STATES

The VT220 Series terminal has three major operating states.

- Set-Up
- On-Line
- Local

The operating states are described in greater detail in the system overview (Chapter 3).

1.6 OPERATING MODES

The VT220 Series terminal has four major operating modes which can be selected either from the keyboard (while in set-up), or by the host (via control codes).

- VT100 mode
- VT200 mode, 7-bit controls
- VT200 mode, 8-bit controls
- VT52 mode

1.6.1 VT100 Mode

The VT100 mode executes standard ANSI functions and emulates the text mode functionality of Digital's VT102 terminal. (VT102/VT220 differences are described in Appendix B).

The VT100 mode provides some backward compatibility with existing software written for the VT102 terminal (when in VT100 mode, the VT220 responds as a service level, class 2 terminal, and VT100 programs which do not recognize this class of terminal functionality will not execute on the VT220). This mode restricts use of the keyboard to those keys which have a direct functional counterpart at the VT102's keyboard. All data is restricted to 7-bit format, and only ASCII, UK, or special graphics characters are generated.

1.6.2 VT200 Mode, 7-Bit Controls

This mode supports Digital Multinational Characters or National Replacement Character sets, depending on the character set mode selected. Both character groups can be accessed via the keyboard or from the host computer via control codes. This operating mode also provides some backward compatibility for existing VT100 software.

1.6.3 VT200 Mode, 8-Bit Controls

This mode supports Digital Multinational Characters or National Replacement Character sets, depending upon the character set mode selected. As in the VT200 mode, 7-bit controls, both character groups can be accessed via the keyboard or programmed control codes.

1.6.4 VT52 Mode

The VT52 mode is a text mode that executes Digital private functions, but not ANSI. This mode has a degree of compatibility with a VT102 operating in that terminal's VT52 mode.

The VT52 mode restricts use of the keyboard to those keys which have a direct functional counterpart at the VT102's keyboard when the VT102 is in VT52 mode. All data is restricted to 7-bit format, and only ASCII, UK, or special graphics characters are generated.

CHAPTER 2
CONTROLS, INDICATORS, AND CONNECTORS

2.1 GENERAL

This chapter provides information about the terminal's controls, indicators, and connectors, including those for the VT22X-AA modem option. It also includes information on the various keypads and special function keys of the LK201 keyboard.

2.2 MONITOR ASSEMBLY (VT220)

The monitor assembly controls, indicators, and connectors (Figures 2-1 and 2-2) are as follows.

Power controls, indicators, and connectors

- Power on/off switch -- turns the terminal on or off.
- "Power OK" indicator -- lights to indicate power is applied to the terminal and all dc voltages are present.

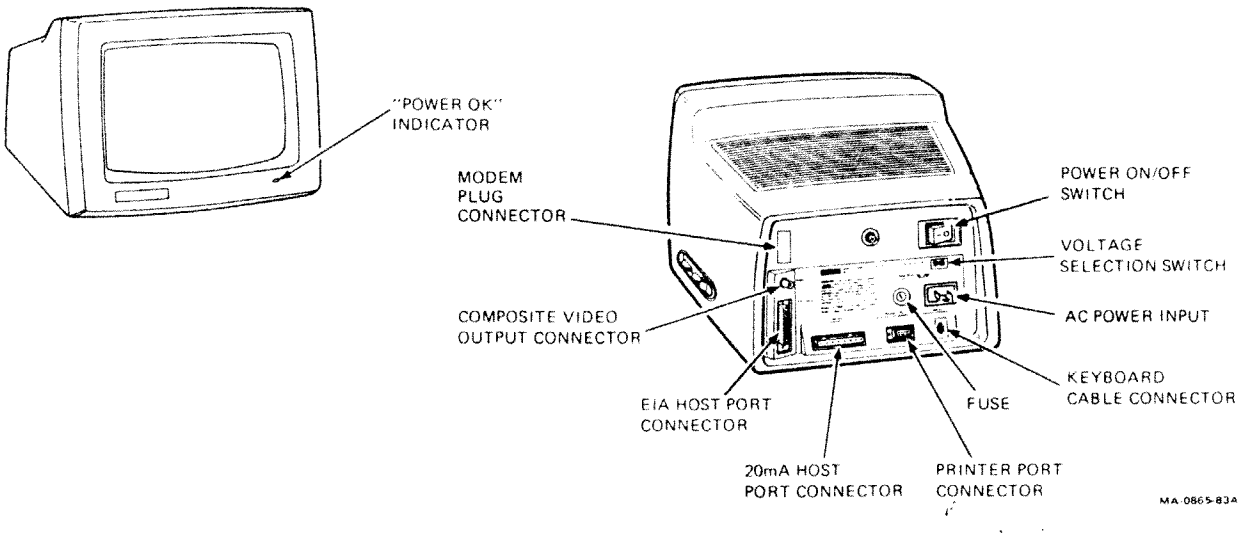


Figure 2-1 Monitor Assembly Controls, Indicators, and Connectors

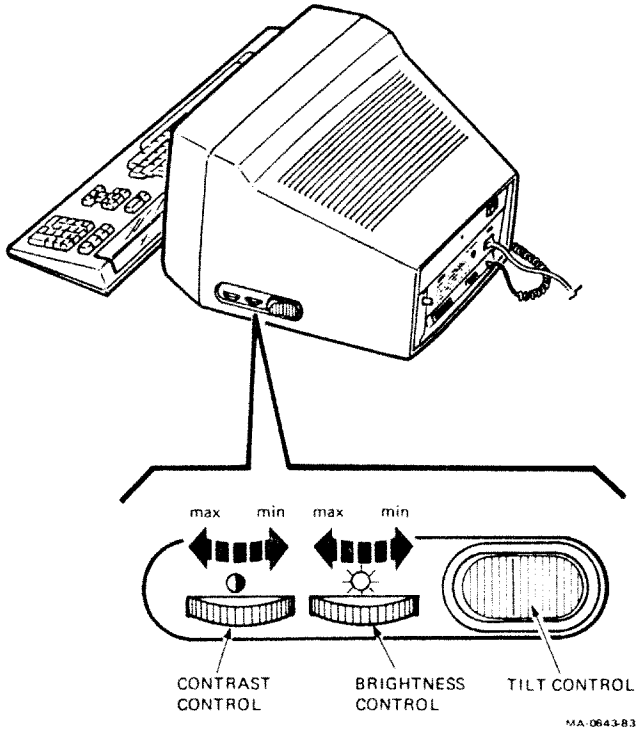


Figure 2-2 Display Controls and Tilt Leg Release Button

- AC power input -- connects the power cord to the monitor assembly.
- Fuse -- protects the monitor assembly from electrical damage.
- Voltage selection switch -- matches the input voltage selected to the voltage supplied by the ac source.

CAUTION

An incorrect setting of the voltage select switch can damage the monitor assembly.

Communication connectors

- EIA host port connector -- connects the terminal to a local host computer, or an external modem for remote host communication.
- 20 mA host port connector -- connects the terminal to a local host computer via a passive only 20 mA loop.
- Composite video output connector -- provides a complete composite video output signal for an additional slave monitor; (composite video output is an RS170-like output using dc coupling not in strict agreement with RS170 specifications).
- 9-pin printer port connector -- connects a printer to the terminal.
- Keyboard cable connector -- connects the keyboard to the monitor assembly.
- Modem plug connector -- connects shorting plug portion of modem connection cable to monitor assembly.

CRT display controls

- Contrast control -- adjusts the degree of contrast on the screen.
- Brightness control -- adjusts the degree of brightness on the screen.
- Tilt control -- releases a tilt leg that drops to provide a -5 to +15 degree tilt range for adjusting the angle of the monitor.

2.3 KEYBOARD (LK201)

The LK201 keyboard (Figure 2-3) consists of the following components.

- Main keypad
- Editing keypad
- Auxiliary keypad
- Top-Row function keys
- Visual indicators
- Audible indicators
- Connector cable

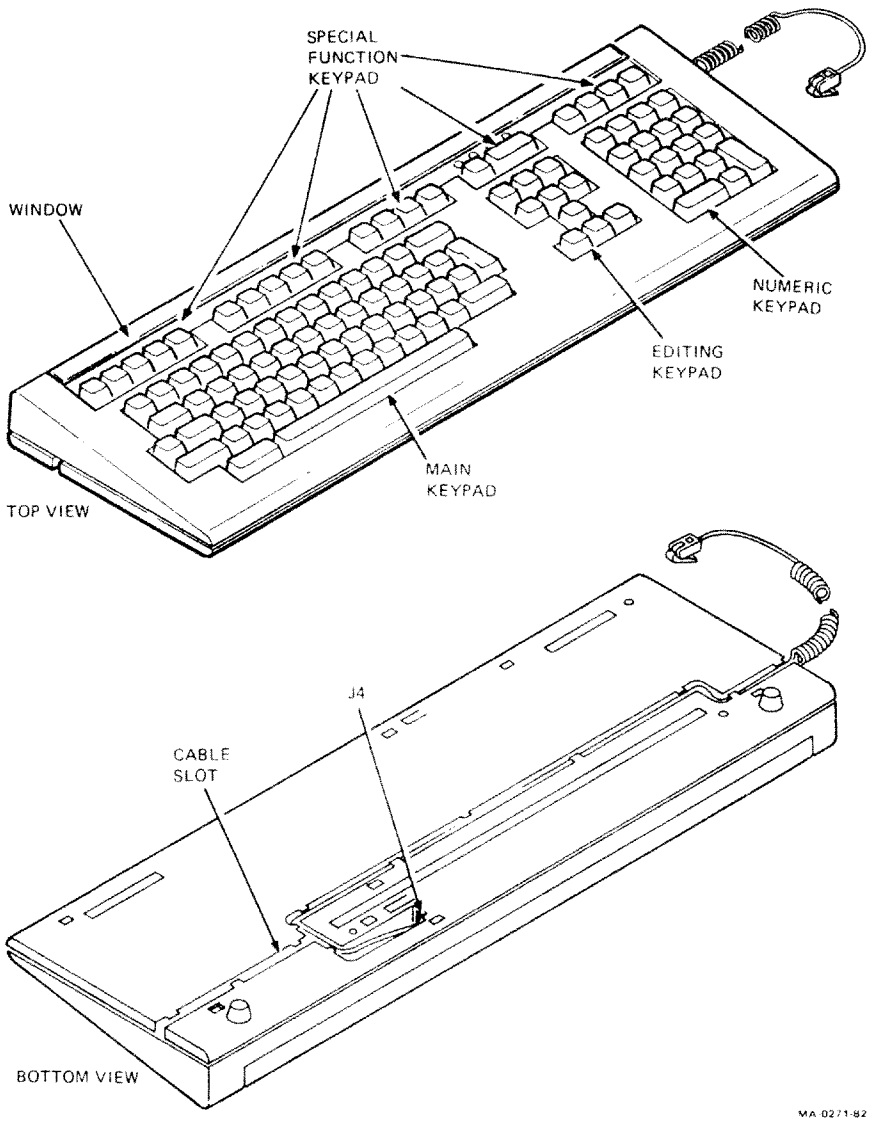


Figure 2-3 LK201 Keyboard Module

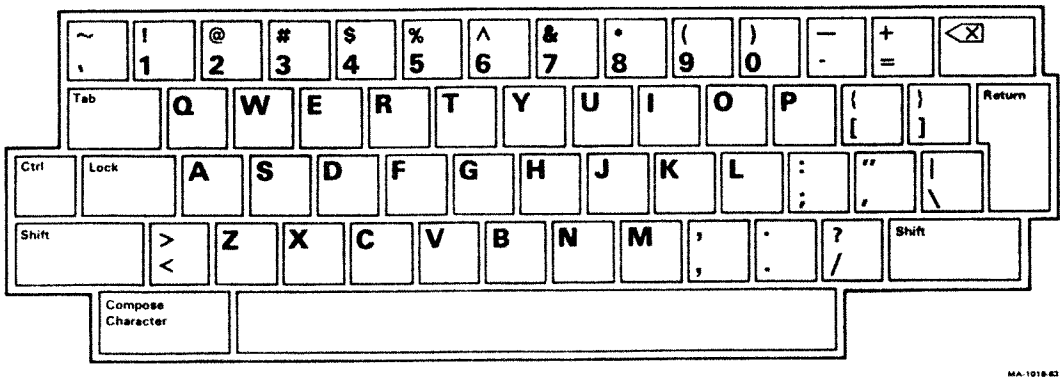


Figure 2-4 Main Keypad

2.3.1 Main Keypad

The main keypad (Figure 2-4) operates like a standard typewriter keyboard. These special function keys are located on the main keypad.

- **TAB** key -- generates a horizontal tab, normally moving the cursor to the next tab stop.

- **CTRL** (Control) key -- when pressed with another key, generates a control code to tell the system to perform a predefined function (such as **CTRL** -- <X, which generates a CANCEL control character).

- **LOCK** key -- function determined by set-up feature so that when pressed, it can serve as either a **SHIFT LOCK** (all keys to generate their shifted value), or a **CAPS LOCK** (alphabetic keys generate uppercase characters), until **LOCK** key is pressed again.

- **SHIFT** key -- when pressed with another key, generates either the key's shifted value (for alphanumeric and two-symbol keys), or, in the case of some function keys, generates a predefined control function.

- **RETURN** key -- generates a CR (or a CR and LF, as selected in General Set-Up), or, in some cases, moves the cursor to the next line when editing text. In other cases, it is a signal to the system that a particular operation is finished.

- <X (Delete) key -- generates a DEL character, normally moving cursor one character to the left and erasing character at the new cursor position.

- **COMPOSE CHARACTER** key -- generates characters that do not exist as standard keys.

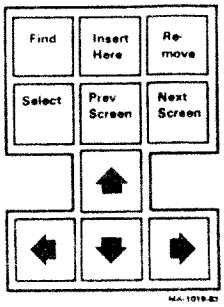


Figure 2-5 Editing Keypad

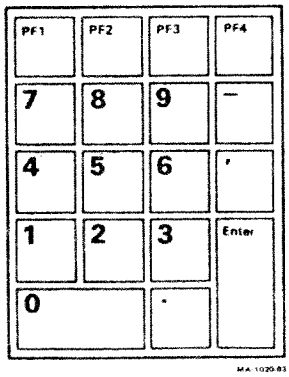


Figure 2-6 Auxiliary Keypad

2.3.2 Editing Keypad

The editing keypad (Figure 2-5) is normally used to control the cursor, and edit data already entered. In a typical editing operation, the four arrow keys move the cursor in the direction indicated by the arrow. The six editing keys can have functions corresponding to their legends, or can be defined for special functions, depending on the application program in effect.

2.3.3 Auxiliary Keypad

The auxiliary keypad (Figure 2-6) is used primarily to enter numeric data. However, some of this keypad's keys (PF1, PF2, PF3, and PF4) can have functions assigned to them by the application software in use. The ENTER key causes a CR (or a CR and LF, as selected in General Set-Up), and is also used while in set-up mode to activate selected features.

2.3.4 Top-Row Function Keys

Most of the top-row function keys (Figure 2-7), have functions assigned to them by the application software in use. The following top-row function keys have predetermined values.

- **HOLD SCREEN** key -- freezes the display and stops new characters from being displayed until pressing **HOLD SCREEN** again returns the terminal to normal operation.
- **PRINT SCREEN** key -- sends the text on the screen to the printer (**CTRL-PRINT SCREEN** sets or resets auto print mode).
- **SET-UP** key -- causes terminal to enter or exit set-up.

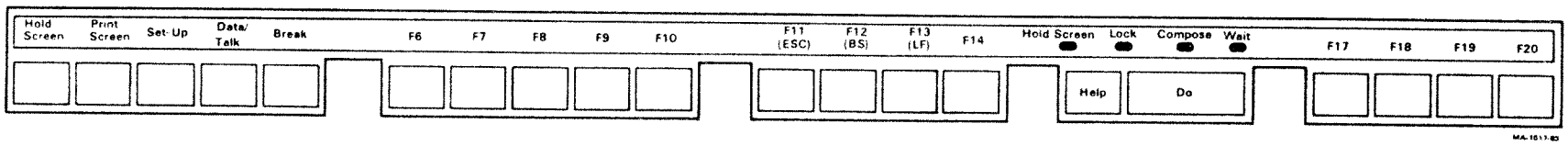


Figure 2-7 Top-Row Function Keys

- DATA/TALK key -- controls use of a switched telephone line when the optional modem is installed.

- BREAK key -- transmits a BREAK control character to the host if BREAK generation is enabled in set-up (SHIFT-BREAK initiates a disconnect, while CTRL-BREAK sends the answerback message to the host).

- F11 (ESC) -- generates an ESC character in either VT100 or VT52 modes (function is determined by application programs in either of the VT200 modes).

- F12 (BS) -- generates a BS character in either VT100 or VT52 modes (function is determined by application programs in either of the VT200 modes).

- F13 (LF) -- generates a LF character in either VT100 or VT52 modes (function is determined by application programs in either of the VT200 modes).

2.3.5 Visual Indicators

The keyboard has four visual indicators to show the present status or operation in progress.

- HOLD SCREEN indicator -- on when display is frozen (refer to HOLD SCREEN key description in section 2.3.4)

- LOCK indicator -- on when keyboard's LOCK key is depressed (see LOCK key description in para. 2.3.1)

- COMPOSE indicator -- on to indicate a compose sequence is in progress

- WAIT indicator -- on when keyboard is prevented from transmitting information (in effect, locked out of the system)

2.3.6 Audible Indicators

The keyboard generates two sounds, both of which can be enabled or disabled in set-up.

- Keyclick
- Bell

2.3.6.1 Audible Keyclick -- sounds each time a key is pressed, with the following exceptions.

- When the **SHIFT** or **CTRL** keys are depressed, because these keys do not generate characters, but only modify characters generated by other keys
- When the **WAIT** indicator is on (characters from the keyboard will be lost)
- When the keyclick is disabled in set-up
- When an inactive key is pressed

2.3.6.2 Bell -- sounds in each of the following cases.

- During the power-up self-test
- When the terminal receives a BEL character from the host
- When a composing error is made
- When the margin is approached (unless bell is disabled in set-up)

2.3.7 Connector Cable

The keyboard module connects to the system via a BCCØ1 cable. Figure 2-8 shows the connector for the BCCØ1 cable.

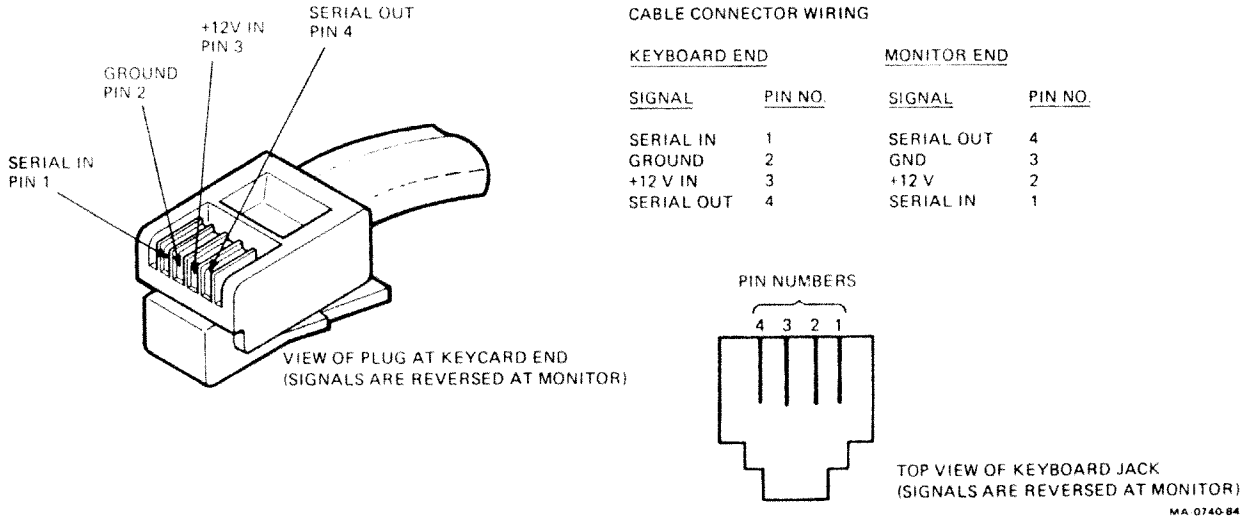


Figure 2-8 BCCØ1 Cable Connector (Keyboard End)

2.4 MODEM OPTION (VT22X-AA)

The VT22X-AA modem controls, indicators, and connectors (Figure 2-9) are as follows.

Front panel controls and indicators

- Test LED -- when lit, provides visual indication of either on-going analog or remote loop test condition.
- Analog loop test button -- puts modem into test of local loop when depressed.
- Remote loop test button -- puts modem into test of remote loop when depressed.

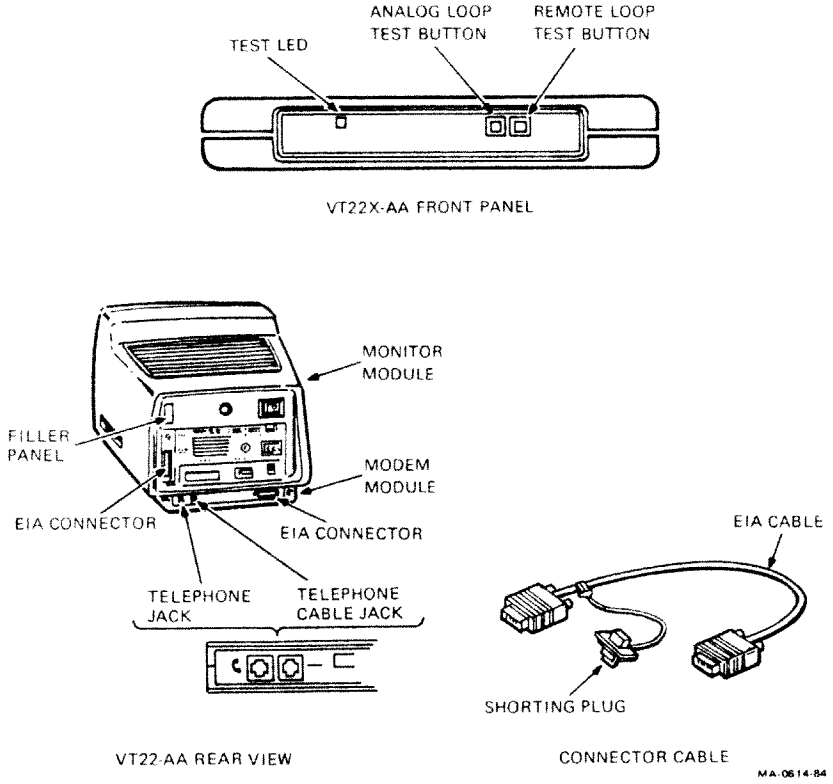


Figure 2-9 Modem Module Controls, Indicators, and Connectors

Rear panel connectors

- Connector cable -- consists of shorting plug (which connects to receptacle covered by filler panel) and EIA cable (which routes host communication between the EIA connectors on the monitor and the modem).

- Filler panel -- is a removable panel covering monitor assembly receptacle for shorting plug of modem connector cable.

- EIA connector -- is a 25-pin connector on both monitor assembly and modem with host communications routed between the two EIA connectors by the connector cable.

- Telephone jack -- connects telephone device to the modem.

- Telephone cable jack -- connects telecommunications line to the modem.

CHAPTER 3
SYSTEM OVERVIEW

3.1 GENERAL

This chapter provides an overview of system interactions during each of the possible operating states of the VT220 Series terminal.

3.2 OPERATING STATES

The terminal functions in any one of three operating states.

- Set-Up
- Local
- On-Line

3.2.1 Set-Up

Set-Up is selectable from the keyboard (SET-UP key) for performing the following functions.

- Examining or changing terminal operating characteristics (such as transmit and receive speeds)
- Transferring from on-line to local, or from local to on-line

While in set-up, the terminal is functionally disconnected from the host. Only the keyboard is enabled as an input device, and only the monitor is enabled for output. Any data received from the host is buffered until the terminal is placed in an on-line operating state.

3.2.2 Local

Local is selectable while in set-up. This operating state disables terminal-to-host communications. Any data received from the host while in local is buffered until the terminal is placed on-line.

While in local, the keyboard serves as an input device, with displayable data input from this device sent to the screen. In addition, information can be output from the terminal (either screen or keyboard data), to the printer (via printer port).

3.2.3 On-Line

On-line is selectable while in set-up. This operating state lets the terminal communicate with a host. This communications link-up can take the following two forms.

- Null modem -- communication is through a direct line link with the host, either through the EIA host port, or the 20 mA port
- External modem -- communication with a remote host, via EIA host port connection with the modem option

When the terminal is on-line, data entered at the keyboard is transmitted to the host. A local-echo feature (selectable in set-up) routes keyboard data to the monitor, as well as to the host.

Both the monitor and the printer can receive information from the host, but not both at the same time. However, data received for the monitor can be subsequently transferred to the printer.

The printer port can be placed in controller mode while on-line (via set-up feature). When the printer port is selected for controller mode, the terminal is essentially a buffer for host to printer communications. In such a case, no output is made to the monitor, and no keyboard input is transferred to the host.

3.3 SYSTEM ARCHITECTURE

Figure 3-1 provides a functional block diagram of the terminal that identifies the terminal's major components or logics.

- CPU logic
- Video logic
- System communication logic
- Modem option
- Power supply
- Keyboard
- Monitor (monitor circuits and CRT)

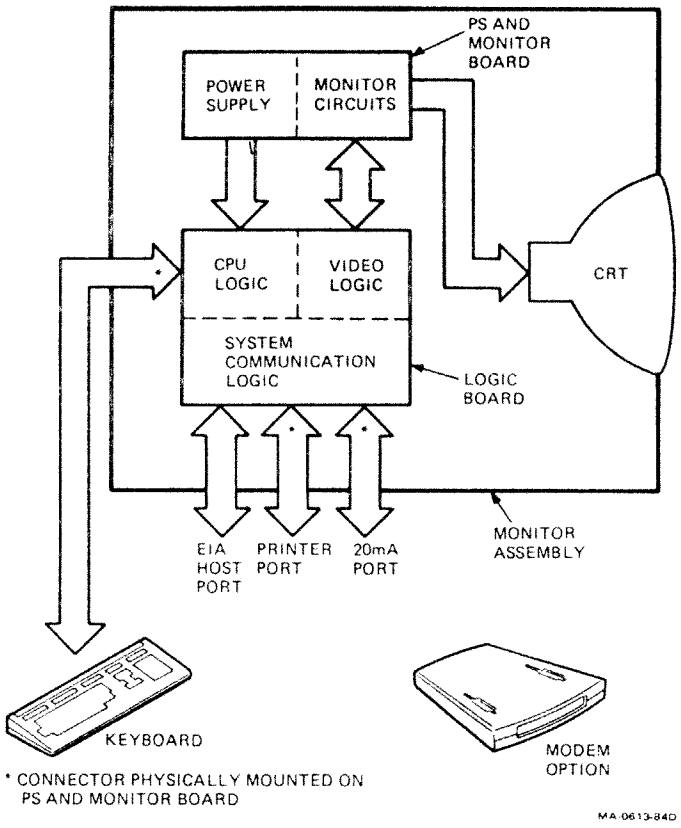


Figure 3-1 VT220 Series Terminal
Functional Block Diagram

3.3.1 CPU Logic

The CPU logic controls the overall operation of the terminal. It interprets host and keyboard input and directs terminal functions. The CPU logic contains the following major components/circuits.

- 8051 microprocessor with internal RAM (128 bytes) and ROM (4K), directly responsible for terminal operation, including direct interface with the keyboard module
- Associated decoding logic
- 256 byte nonvolatile RAM for storing terminal set-up information
- 24K byte of ROM containing firmware for all terminal control functions, such as keyboard handling, screen data handling, set-up, self-test, VT100 and VT52 modes, and printer control

- 8K of volatile screen RAM used for storage of characters to be displayed, as well as for data buffering, and scratch pad operations

- 8K of volatile atribute RAM used for storage of attribute data associated with characters stored in the screen RAM

NOTE

The volatile screen and attribute RAMs are also accessed by the video logic to obtain character and attribute values stored in these RAMs.

3.3.2 Video Logic

The video logic develops the video output signals required to drive the terminal monitor. The video logic consists of the following major components/circuits.

- A 9007 video processor that performs DMA transfers (character and attribute transfers from CPU logic RAMs to the video converting circuit), and generation of basic video timing signals

- A video converting circuit that transforms display data into video output to the monitor circuits, and composite video output to a slave monitor

3.3.3 System Communication Logic

The system communication logic interfaces the terminal with external devices. The system communication logic consists of the following major components/circuits.

- Connectors for physical connection with the printer, host (EIA host port or 20 mA port connectors), and modem option (via EIA host port)

- DUART for control of communication as programmed by the CPU

- Interface components responsible for input and output of data from the various connectors

3.3.4 Modem Option (VT22X-AA)

When installed, the modem interfaces the terminal with a switched or dedicated telephone line for communication with a remote host. The VT22X-AA modem consists of the following major circuits/components.

- Two four-pin telephone jack connectors for interfacing with the telephone line
- EIA connector for interfacing with the monitor assembly
- Handshake circuits to control the communication between the terminal and the remote host

3.3.5 Power Supply

The power supply generates the operational voltages required by the monitor assembly, keyboard, and the modem module option. The power supply contains the following major components/circuits.

- AC input circuits
- +5 V development circuits
- +12 V development circuits
- -12 V development circuits
- Pulse modulation and feedback control circuits
- Overcurrent protect circuit

3.3.6 Keyboard

The keyboard enables operator input to the system. The keyboard consists of the following major components/circuits.

- 8Ø51 microprocessor for control of keyboard operations
- Serial interface for communication with the monitor assembly
- Key matrix scanning circuits for determining when a key is being pressed
- Audio circuits for generating bell tones and key clicks
- LED drivers for enabling the keyboard's visual indicators

3.3.7 Monitor Components

The monitor components convert separate video and sync input signals from the video logic into visual output to the operator. The monitor contains the following major components/circuits.

- CRT device for presenting the visual output
- Monitor circuits for developing drive potentials for the CRT
- BNC connector for composite video output to a slave monitor
- Brightness and contrast controls

3.4 SYSTEM INTERACTION

Figures 3-2 through 3-7 provide an overview of the information flow within the terminal for various system configurations during the different operating states (set-up, local, and on-line).

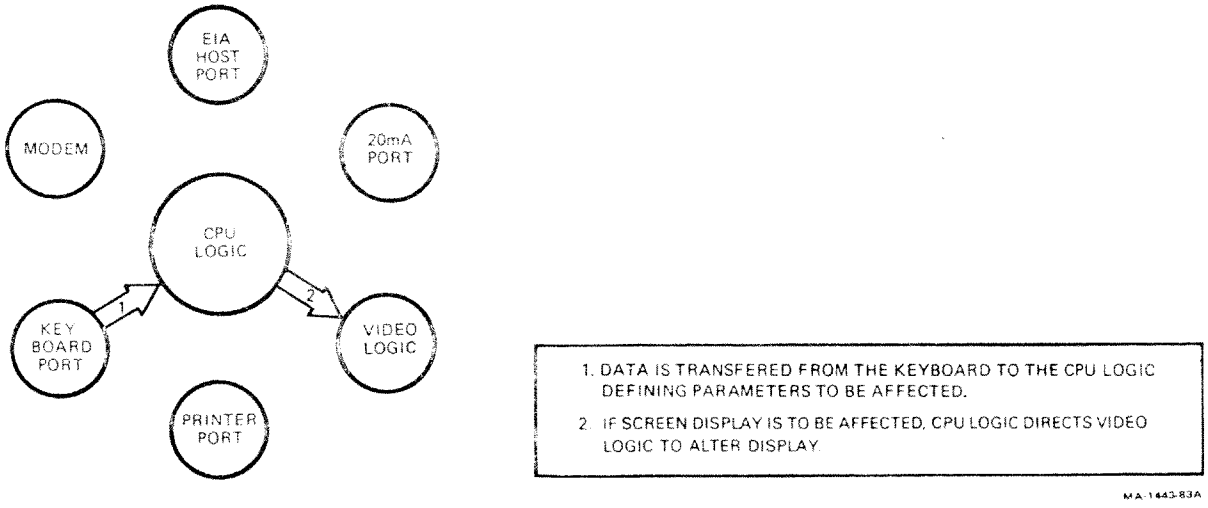


Figure 3-2 System Interaction in Set-Up

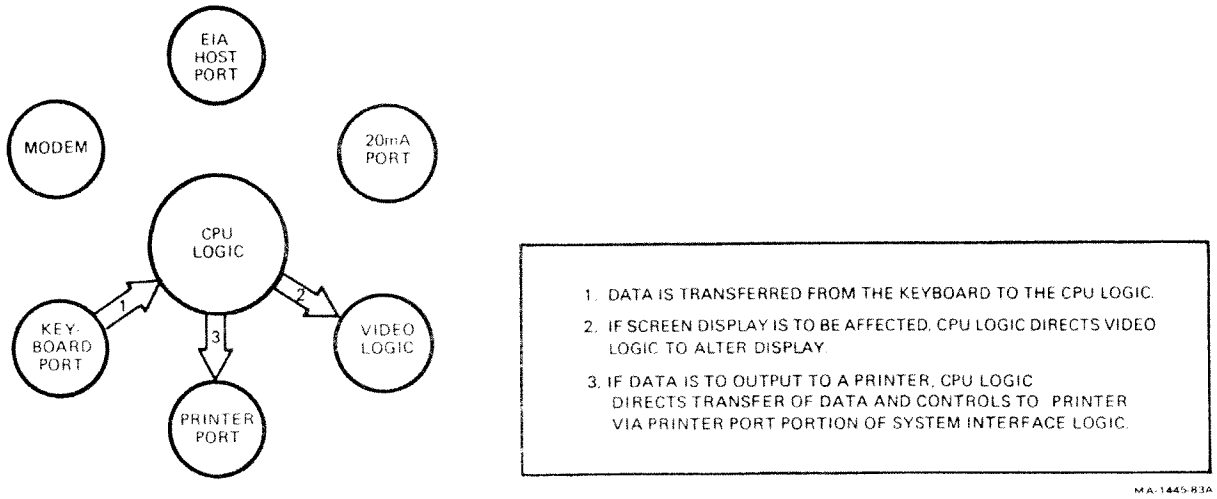


Figure 3-3 System Interaction in Local

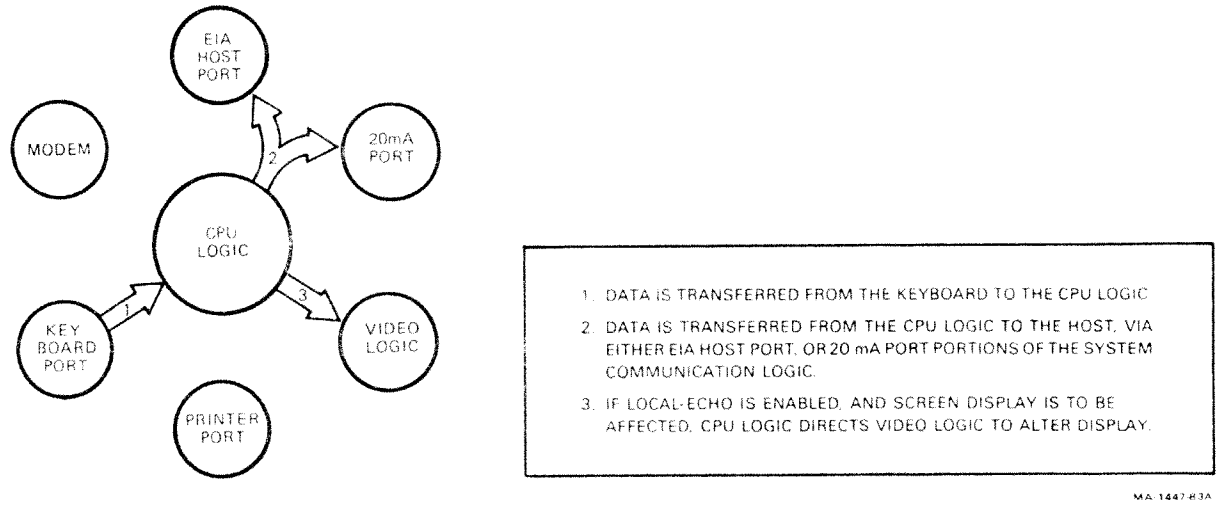
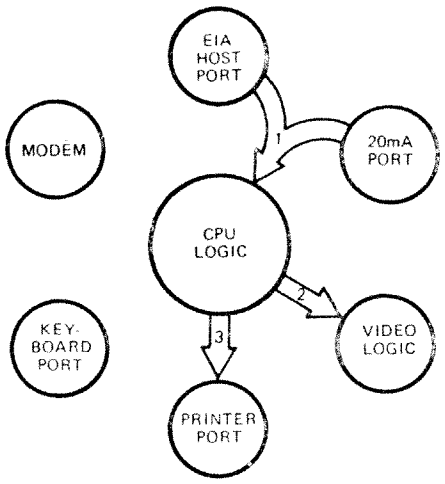


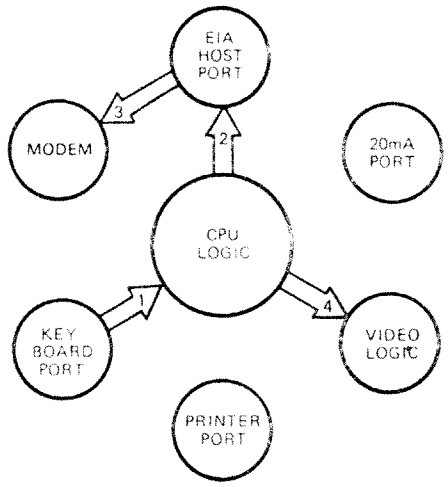
Figure 3-4 System Interaction On-Line: Data to Host (Null-Modem)



1. DATA IS TRANSFERRED TO THE CPU LOGIC FROM THE HOST, VIA EITHER EIA HOST PORT, OR 20 mA PORT PORTIONS OF THE SYSTEM COMMUNICATION LOGIC.
2. IF SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.
3. IF DATA IS TO BE OUTPUT TO THE PRINTER DEVICE, CPU LOGIC DIRECTS TRANSFER OF DATA AND CONTROLS TO PRINTER DEVICE VIA PRINTER PORT PORTION OF SYSTEM COMMUNICATION LOGIC.

MA-1450-83A

Figure 3-5 System Interaction On-Line: Data from Host



1. DATA IS TRANSFERRED FROM THE KEYBOARD TO THE CPU LOGIC.
2. DATA IS TRANSFERRED FROM THE CPU LOGIC TO THE HOST EIA PORT.
3. DATA IS ROUTED FROM EIA HOST PORT TO MODEM OPTION.
4. IF LOCAL-ECHO IS ENABLED, AND SCREEN DISPLAY IS TO BE AFFECTED, CPU LOGIC DIRECTS VIDEO LOGIC TO ALTER DISPLAY.

MA-1452-83A

Figure 3-6 System Interaction On-Line: Data to Host (Modem)

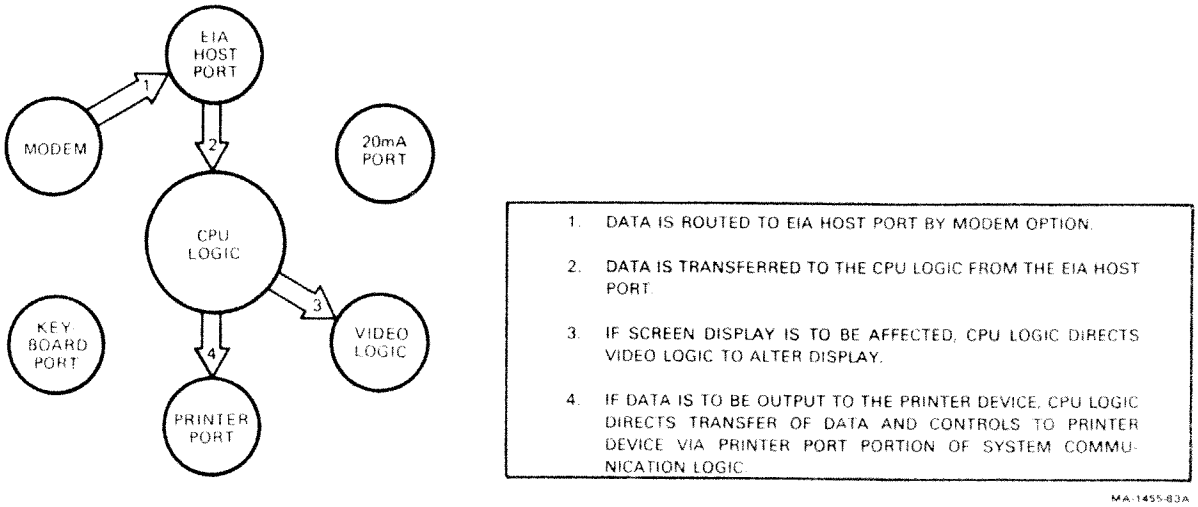


Figure 3-7 System Interaction On-Line: Data from Host (Modem)

CHAPTER 4
CPU LOGIC

4.1 GENERAL

The CPU logic (shaded area in Figure 4-1) directs VT220 activity in response to either operator input (via keyboard), or host input (via system communication logic). In general, the CPU performs the following functions.

- Defines operational parameters for other logic components
- Directs system communication logic, video logic, and keyboard module operation

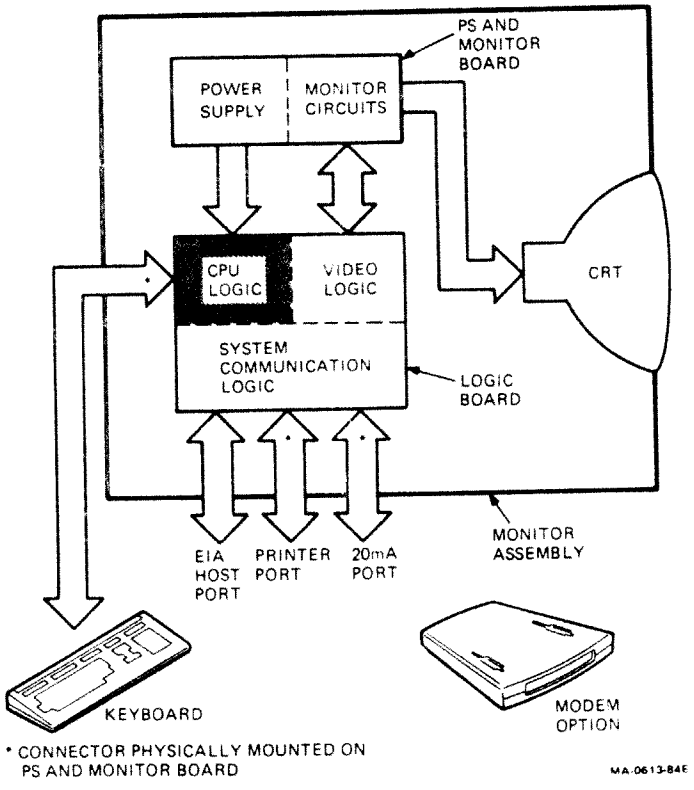


Figure 4-1 VT220 Series Terminal Functional Block Diagram

- Manages screen and attribute RAMs
- Initializes system at power up, and executes self-test programs

4.2 MAJOR CIRCUITS AND COMPONENTS

Figure 4-2 provides a block diagram identifying the major circuits and components that make up the central processing unit (CPU) logic.

- Central processing unit (CPU)
- Address latch
- Program ROM
- Data buffer
- Screen RAM
- Attribute RAM
- Select decoder
- Keyboard I/F
- Nonvolatile RAM (NVR)
- Configuration register

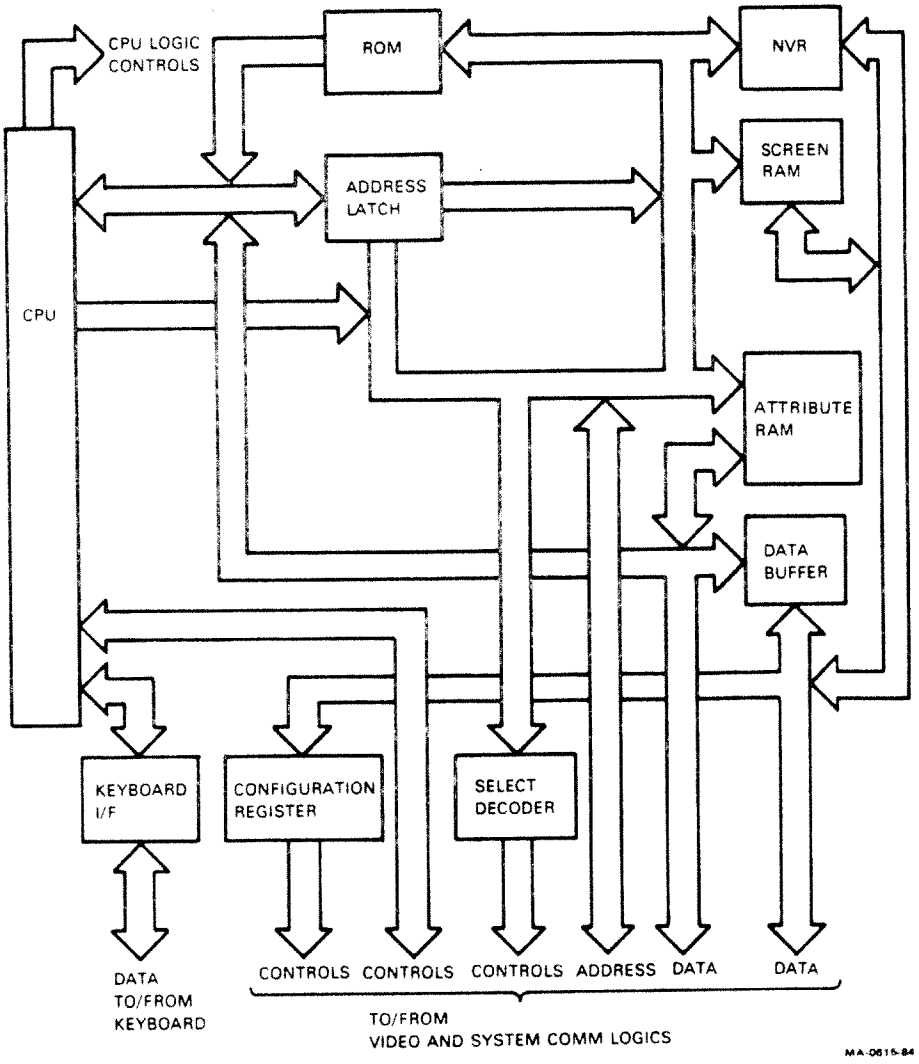


Figure 4-2 CPU Logic Block Diagram

4.2.1 Central Processing Unit (CPU)

The CPU (Figure 4-3) consists of the following components.

- 8051 microprocessor -- services interrupt and DMA requests, interprets host and keyboard data, generates address and read/write controls for system components, and initializes system on power up.

- RD gate -- generates RD L from either CPU RD L, when CPU is attempting to read from an I/O device or RAM, or from DMA L, when character and attribute data is to be transferred out of the RAMs over to the video logic.

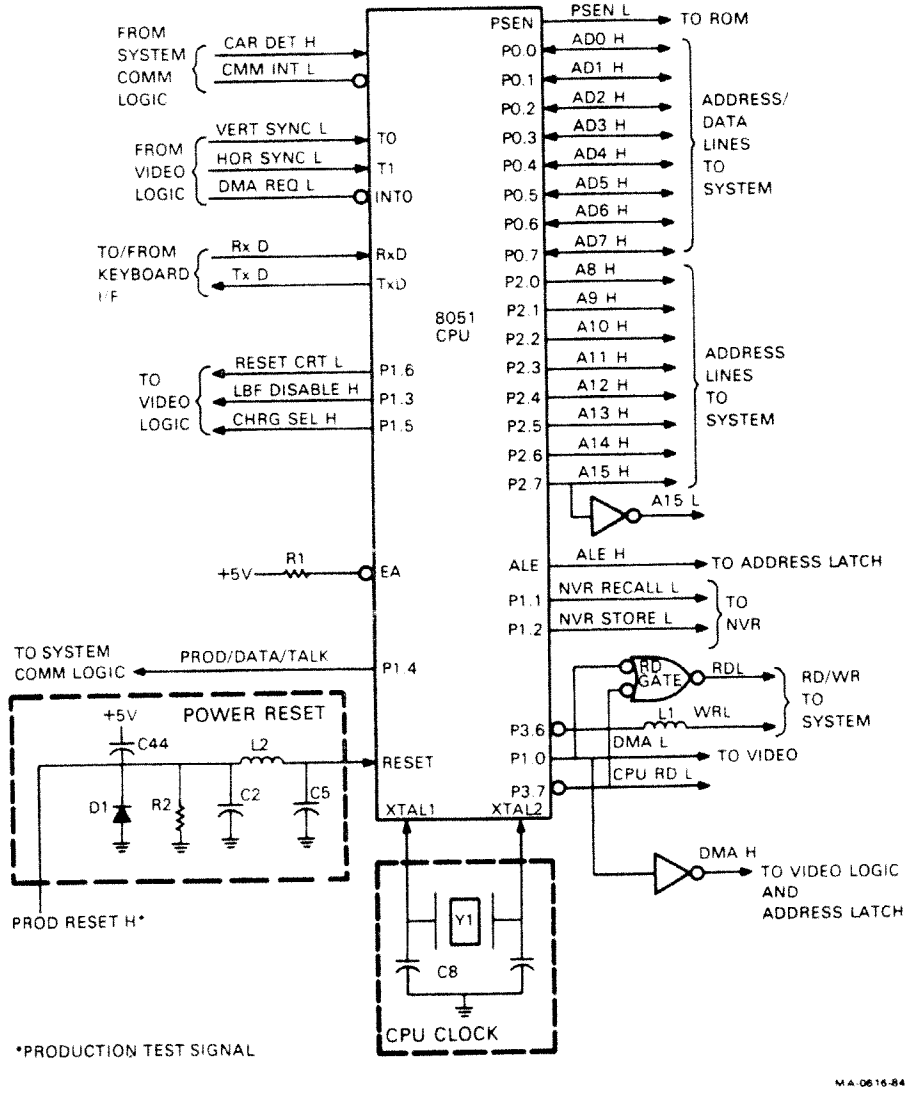


Figure 4-3 CPU Block Diagram

- Power reset -- resets the 8051 on power up.
- CPU clock -- provides 11.0592 MHz input to 8051 CPU for basic timing.

4.2.1.1 8051 CPU Internal Circuits -- Figure 4-4 provides a block diagram showing the major 8051 CPU internal circuits.

- Port 0 -- is eight bidirectional lines used for output of lower byte of address and for input and output of data.
- Port 1 -- is eight quasi-bidirectional lines used for input of status information and output of controls.
- Port 2 -- is eight lines used for output of high byte of address.

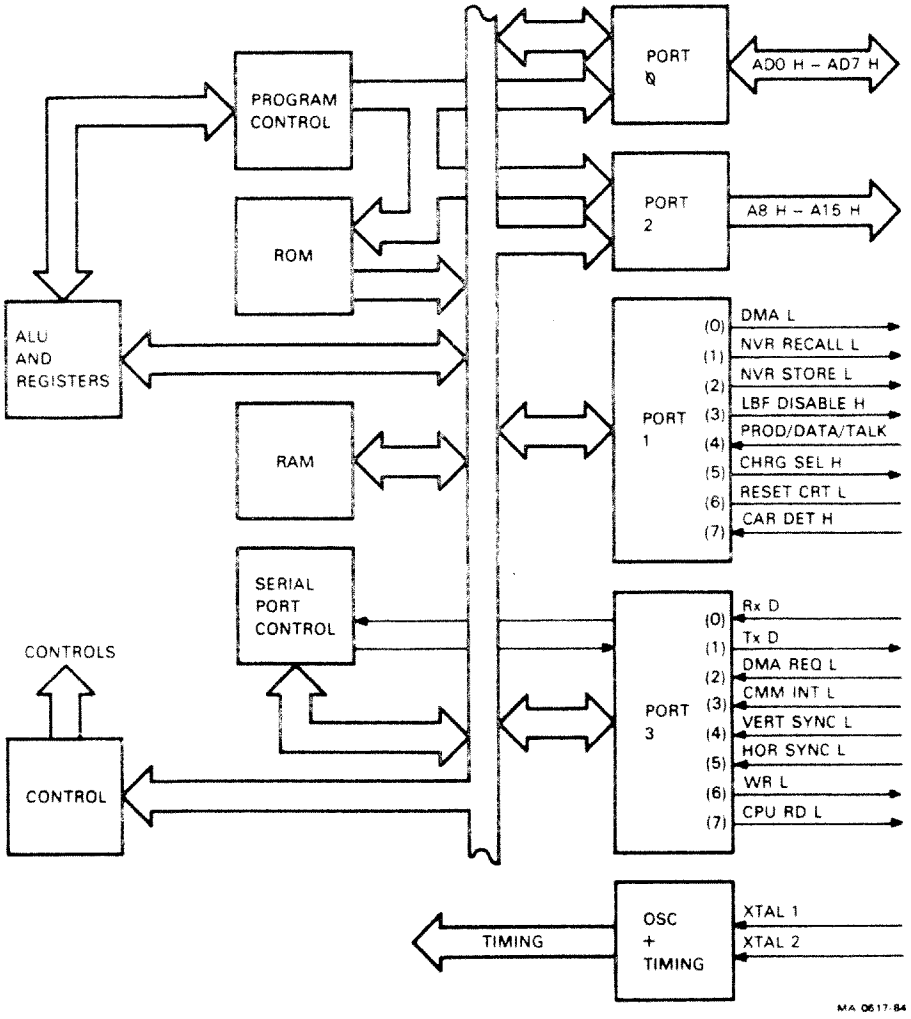


Figure 4-4 8051 CPU Internal Block Diagram

- Port 3 -- is eight lines used for input of status, output of controls, and transfer of serial data between the 8051 and the keyboard I/F.

- Oscillator (OSC) and timing -- generates 8051 timing signals based on 11.0592 MHz input from external CPU clock.

- Program control -- controls sequence of program memory execution (internal ROM and external ROM).

- Control -- interprets instructions and generates controls to 8051 circuits based on that interpretation.

- Serial port control -- provides full-duplex UART functionality for serial data communications with the keyboard.

- ROM -- provides 4K bytes of internally stored programming.

- RAM -- provides 128K bytes of memory for scratch pad and register/stack functions.

- ALU and registers -- provide processing logic, including special function registers.

Later in this chapter, Table 4-2 describes the signals shown in Figures 4-3 and 4-4.

4.2.1.2 **8051 CPU Transactions** -- The 8051 performs the following transactions.

- Instruction fetch -- reads internal or external ROM.

- Read/write transaction -- reads or writes data for system I/O devices, screen RAM, or attribute RAM.

- DMA transaction -- grants control of the data buses to enable video logic access of CPU logic RAMs, for access of character and attribute values.

Figures 4-5 through 4-7 provide timing diagrams for instruction fetch, read, and write transactions. No diagram is provided concerning DMA transactions, as DMA transactions are described in greater detail in the video logic description (refer to the CRT controller description in Chapter 6).

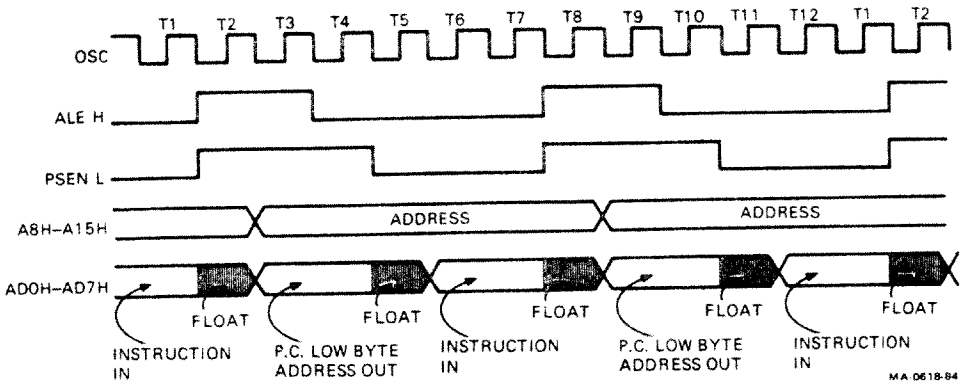


Figure 4-5 8051 CPU Instruction Fetch Timing Diagram

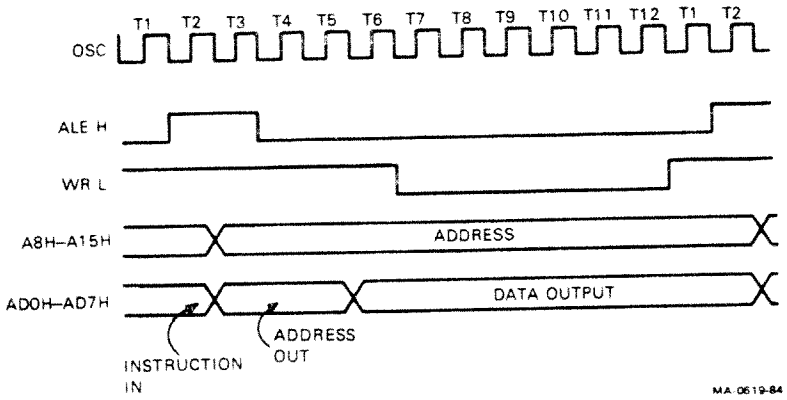


Figure 4-6 8051 CPU Read Transaction Timing Diagram

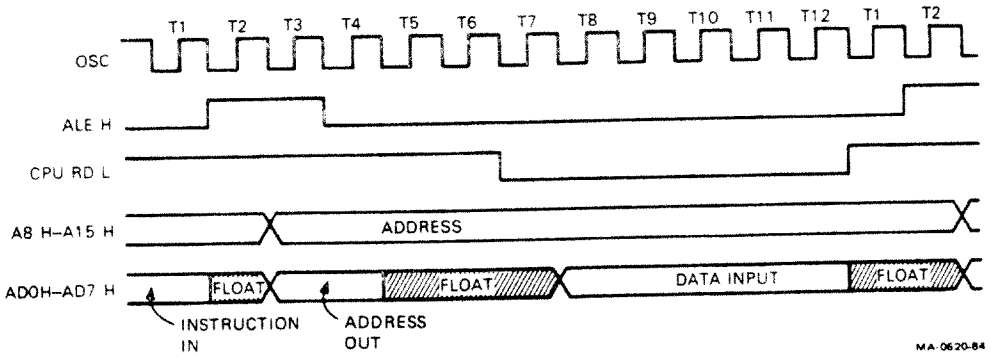


Figure 4-7 8051 CPU Write Transaction Timing Diagram

Figure 4-8 provides an address map for instruction fetch transactions (ROM access). Figure 4-9 provides an external data memory map for system non-ROM read/write transactions. As shown in Figure 4-9, several address ranges are mapped for each specific device or transaction. This is due to a "don't care" condition for some bits when addressing these devices. The addresses actually used are identified in Table 4-1 in conjunction with the select decode description (section 4.2.8).

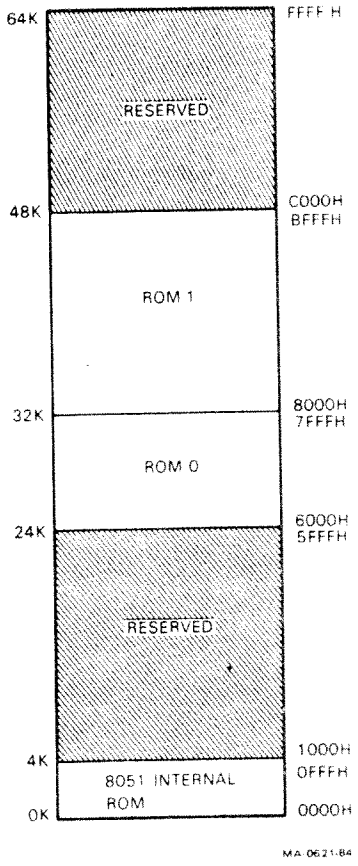


Figure 4-8 8051 CPU Address Map: ROM

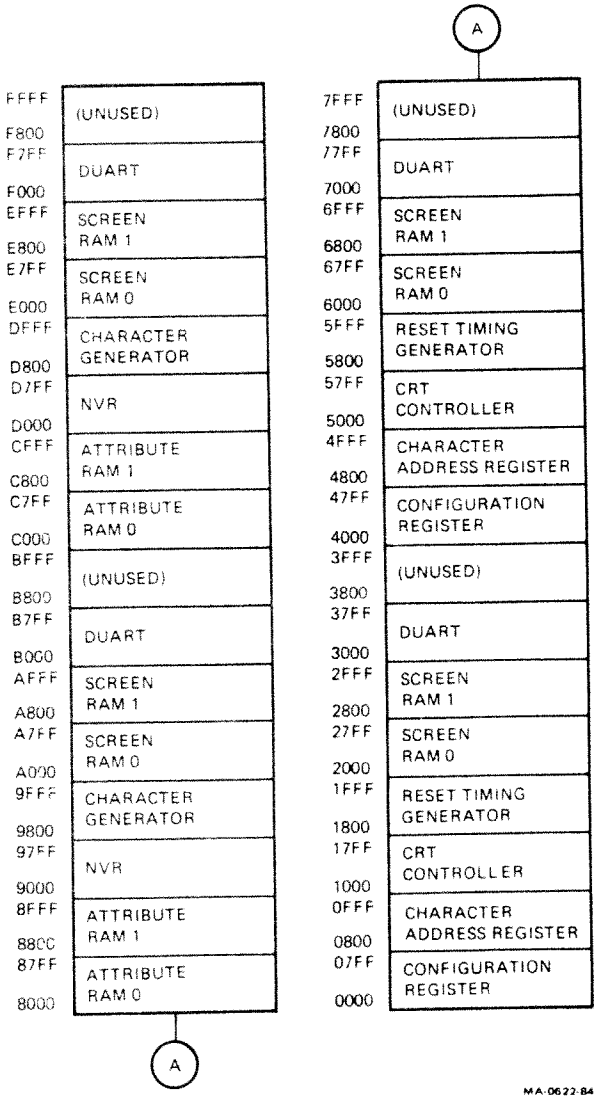


Figure 4-9 8051 CPU Address Map: Non-ROM

4.2.2 Address Latch

The address latch (Figure 4-10), is used by the 8051 for storing the lower byte of address to be used for access of any 8051 addressable component, including external ROM. Address is input to the latch by ALE H and enabled as output as long as DMA H is false. The address latch is inhibited during DMA transactions to prevent any value stored in the latch from affecting the address being generated by the video logic for access of the RAM.

Definitions of the signals identified in Figure 4-10 are provided in Table 4-2.

4.2.3 Read Only Memory (ROM)

ROM provides storage for the firmware required for terminal operation. The ROM (Figure 4-11) consists of two ROM devices, ROM 0, containing 8K bytes of firmware, and ROM 1, containing 16K bytes.

ROM access occurs when PSEN L is true, with ROM 0 enabled for A15 L true, and ROM 1 enabled for A15 H true.

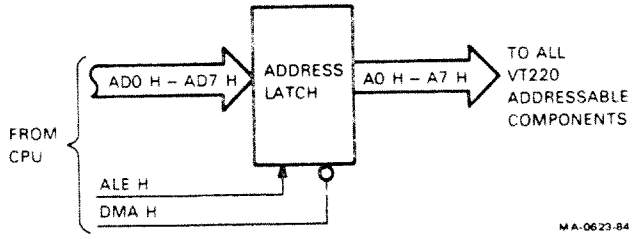


Figure 4-10 Address Latch Block Diagram

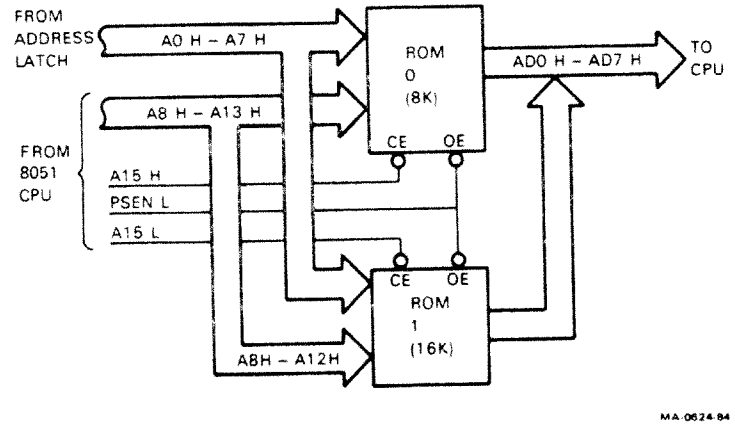


Figure 4-11 ROM Block Diagram

Later in this chapter, Table 4-2 describes the signals shown in Figure 4-11.

4.2.4 Data Buffer

The data buffer provides isolation between the AD0 H-AD7 H lines used by the 8051 CPU for program memory, addressing, and access of either of the two attribute RAMs in the video logic (refer to Chapter 6), and the BAD0 H-BAD7 H lines used for all other read, write, and DMA transactions.

The isolation between the AD0 H-AD7 H bus and the BAD0 H-BAD7 H bus provided by the data buffer enables the video logic to use both buses during DMA transactions. The BAD0 H-BAD7 H lines are used for accessing character address data stored in the screen RAM, while the AD0 H-AD7 H lines are used for accessing attribute data stored in the attribute RAM.

As shown in Figure 4-12, the data buffer is a bidirectional device enabled whenever the attribute RAM is not being accessed (SEL ATR0 L and SEL ATR1 L both false), with the direction of data transfer determined by RD L (out as BAD signals when RD L is false, and in as AD signals when true). The data buffer is disabled either during 8051 CPU access of the attribute RAM, or during DMA transactions, when the video logic is accessing the stored attribute data.

Later in this chapter, Table 4-2 describes the signals shown in Figure 4-12.

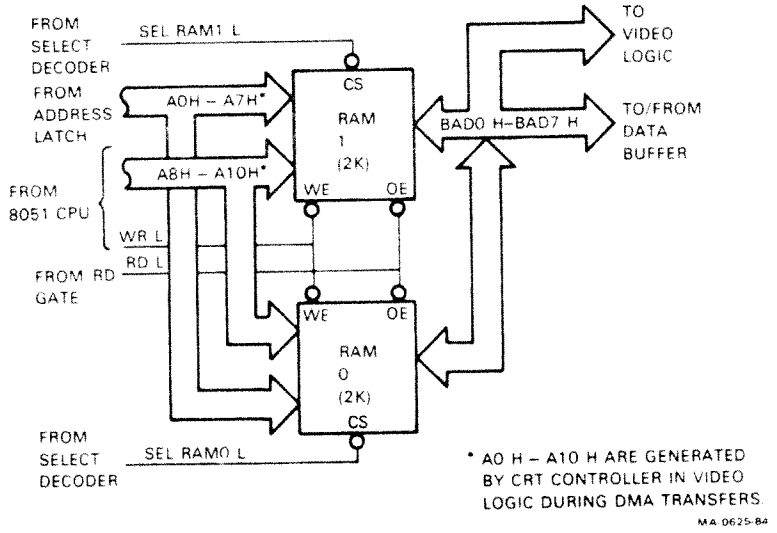


Figure 4-12 Data Buffer Block Diagram

4.2.5 Screen RAM

The 8051 uses the screen RAM to store character address data for output to the video logic and for scratch pad operations. Character address data stored in the screen RAM is transferred to the video logic during DMA transactions (along with attribute values associated with the defined character address, as stored in the attribute RAM). It also defines an address value for a character generator within the video logic, with that address defining the character to be processed for display (refer to the video logic description in Chapter 6).

The screen RAM (Figure 4-13) consists of two static RAM devices, each providing 2K bytes of RAM space. Each is selected by separate select signals (SEL RAM0 L or SEL RAM1 L), and enabled for 8051 write by WR L, or enabled for read output by RD L (with RD L generated either from CPU RD L, for CPU access, or from DMA L, for DMA transfer to the video logic).

Later in this chapter, Table 4-2 describes the signals shown in Figure 4-13.

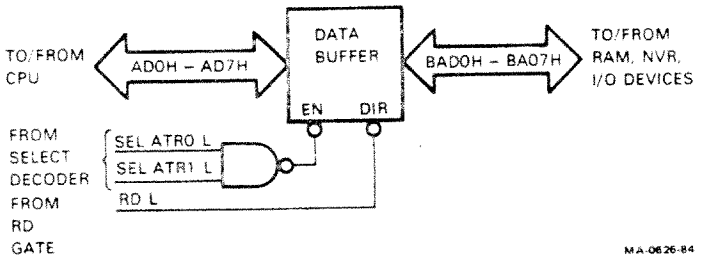


Figure 4-13 Screen RAM Block Diagram

4.2.6 Attribute RAM

The 8051 CPU loads attribute values for specific characters into attribute RAM at addresses directly corresponding to character address values loaded into the screen RAM. Whenever character address values are loaded into the screen RAM, the 8051 CPU will write attribute values associated with those character address values into the attribute RAM.

During DMA transactions, the video logic generates a single address which is applied to both the attribute and screen RAMs. The attribute data is output from attribute RAM and sent to the video logic in conjunction with the character address being output from the screen RAM on the same DMA transaction (attribute value on the AD data lines, and character data on the BAD data lines).

The attribute RAM (Figure 4-14) consists of two static RAM devices, each providing 2K bytes of RAM space. Each is selected by separate select signals (SEL ATR0 L or SEL ATR1 L), and enabled for 8051 write by WR L, or enabled for read output by RD L (with RD L generated either from CPU RD L, for CPU access, or from DMA L, for DMA transfer to the video logic).

Later in this chapter, Table 4-2 describes the signals shown in Figure 4-14.

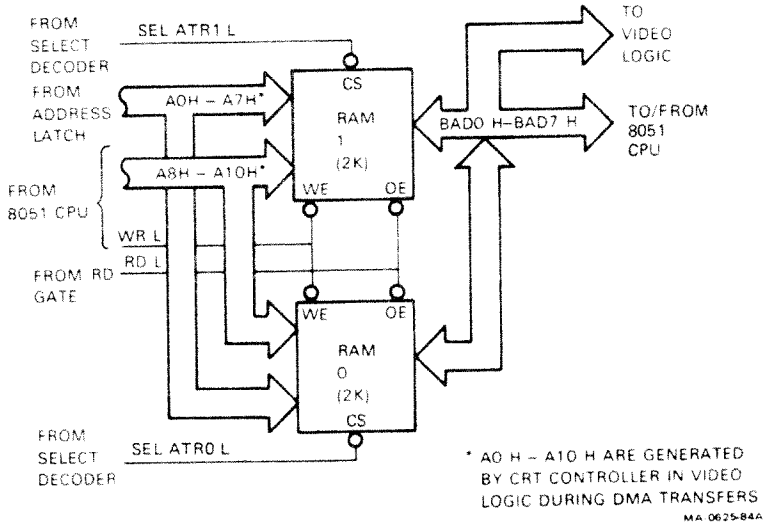


Figure 4-14 Attribute RAM Block Diagram

4.2.7 Select Decoder

The select decoder generates access enables for 8051 CPU read/write transactions, and for video logic DMA transactions. The select decoder (Figure 4-15) consists of the following components.

- RAM/DUART decoder -- is enabled by A13 H true, during 8051CPU read/write transactions to decode A11 H-A12 H address inputs into enable of either the screen RAM (SEL RAM0 L or SEL RAM1 L) or the DUART in system communication logic (SEL DUART); it is also enabled by DMA H true during DMA transactions for selecting screen RAM to be accessed (address input for DUART is not presented during DMA transactions).

- RD/WR decoder -- is enabled by RD L or WR L for 8051 CPU read/write transactions, when A13 H is false, to decode A15 L, A11 H-A12 H into access output to NVR (SEL NVR L), configuration register (SEL CONF REG L), attribute RAM (SEL ATR0 L or SEL ATR1 L), or to various video logic components (EN CHR GEN L, CHR ADDR WR L, SEL CRT L, and RESET TIM L); it is also enabled by RD L, during DMA transactions (A13 H false during DMA, with address value for either of two attribute RAMs presented to decoder).

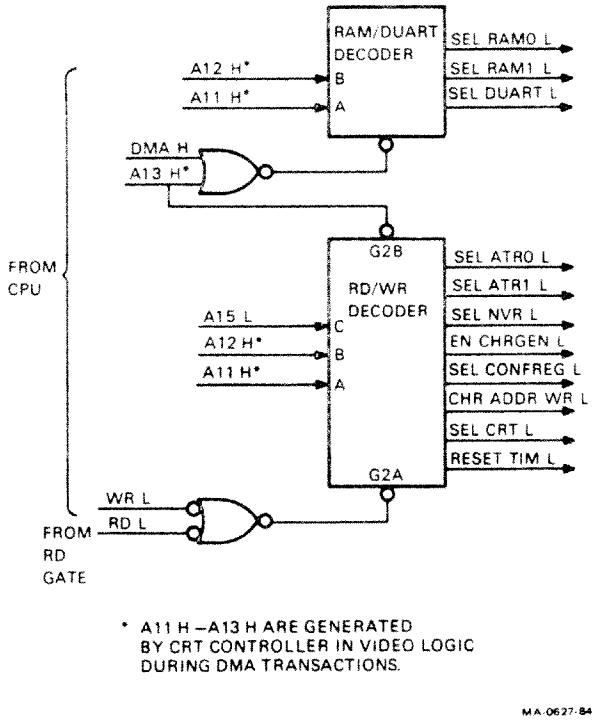


Figure 4-15 Select Decoder Block Diagram

During DMA transactions, the RD/WR decoder and the RAM/DUART decoder will both be enabled for output of corresponding screen RAM and attribute RAM select signals, as these two RAM circuits are read simultaneously by the video logic.

Table 4-1 identifies the address values for all of the access enable signals. Later in this chapter, Table 4-2 describes the signals shown in Figure 4-15.

Table 4-1 8051 CPU Addresses (Non-ROM)

Enable Signal	Hex Address(es)	Device (Logic)
SEL RAM0 L	A000-A7FF	RAM 0 (CPU)
SEL RAM1 L	A800-AFFF	RAM 1 (CPU)
SEL DUART L	B7F0-87FF	DUART (system communication)
SEL ATR0 L	8000-87FF	Attribute RAM 0 (video)
SEL ATR1 L	8800-8FFF	Attribute RAM 1 (video)
SEL NVR L	9700-97FF	NVR
EN CHR GEN L	9FF0-9FFF	Character generator (video)
SEL CONF REG L	07FF	Configuration register (CPU)
CHR ADDR WR L	0FFF	Character address register (video)
SEL CRT L	1700-17FF	CRT controller (video)
RESET TIM L	1FFF	Timing control (video)

4.2.8 Keyboard Interface (I/F)

The keyboard I/F buffers communication between the keyboard module and the 8051 CPU. Serial data is output to the keyboard as KBT (originating at 8051 as TxD), and input to the 8051 as RxD (originating at keyboard as KBR).

Keyboard I/F components are physically located on both of the terminal PCBs. Figure 4-16 provides a breakdown of the keyboard I/F.

- EIA driver and receiver -- interface TTL level logic with EIA level communication lines.
- J1 (logic board)/J2 (PS and monitor board) -- are 26-pin connectors used for routing signals between the two system PCBs.
- Output components -- are ferrite beads tied to keyboard connector pins that are used for radiation suppression.
- J6 -- is a 4-pin telephone plug-type connector that provides direct connection between the keyboard cable and the monitor assembly.

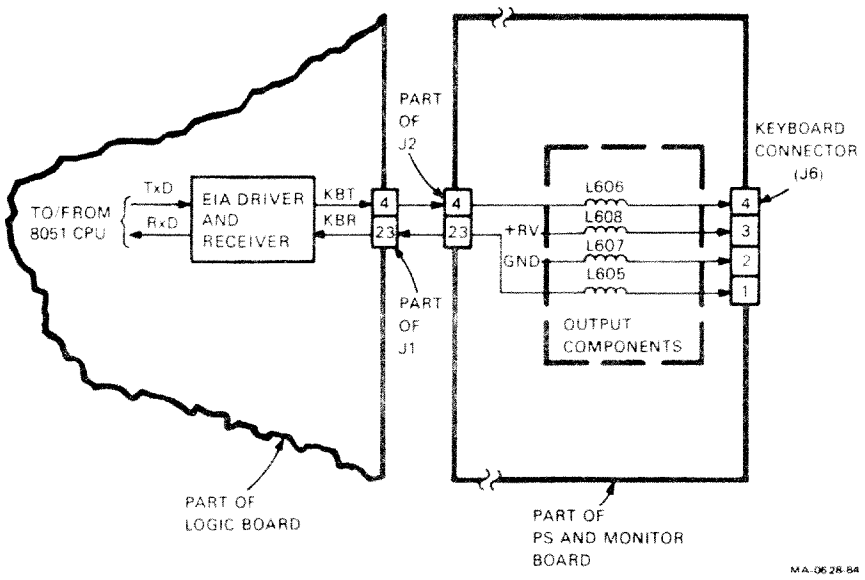


Figure 4-16 Keyboard I/F Block Diagram

Figure 4-16 provides a pin-out for the keyboard connector (J6) and identifies the J1/J2 pins used for keyboard I/F functions. A complete pin-out of J1/J2 is provided in the system communication logic description presented in Chapter 5 (refer to Figure 5-9).

Later in this chapter, Table 4-2 describes the signals shown in Figure 4-16.

4.2.9 Nonvolatile RAM (NVR)

The NVR combines a 256 X 4 bit static RAM with a 256 X 4 bit electrically alterable ROM (EAROM) to provide memory for storing terminal operational parameters, and allowing those parameters to be manipulated by the operator.

During a power-up sequence, data is transferred from the EAROM to the NVR RAM portion (NVR RECALL L), and then to the CPU logic RAM for use in defining terminal parameters. While in the CPU logic RAM, the data stored can be altered. Operator keyboard input defines new parameters, with the 8051 directing a write to alter the data stored in the CPU logic RAM. During a save parameters operation, the data stored in the CPU logic RAM is written to the NVR RAM by the 8051 (SEL NVR L and WR L), and then stored as new parameter values in the NVR EAROM by NVR STORE L from the 8051.

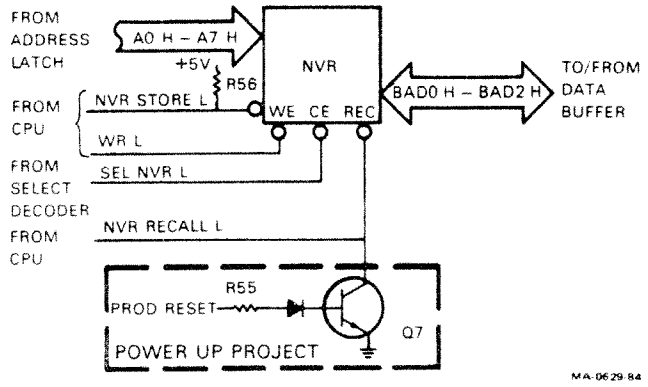


Figure 4-17 NVR Block Diagram

The NVR circuit (Figure 4-17) consists of the following components/circuits.

- NVR device -- contains the RAM and EAROM memories for storing and transferring of parameter values.
- Power up protect -- prevents inadvertant write to NVR device by the 8051 during a power up sequence by forcing NVR RECALL L low until full dc power is applied and all circuits operational (NVR RECALL L places NVR in recall mode and prevents a low at NVR STORE L from being acted on).

Later in this chapter, Table 4-2 describes the signals shown in Figure 4-17.

4.2.10 Configuration Register

The configuration register is programmed by the 8051 with control values to affect system communication and video logic operations. The configuration register (Figure 4-18) consists of two devices, both loaded by SEL CONF REG L: A F/F device for controlling which host communications port is to be enabled (reset for ENA EIA H, set for ENA 20 mA H), and a register for generating miscellaneous video logic controls (NOR FIELD H, LBA CLRS H, EN CHR GEN RW H, ALT SEL H, and LBA CLKS H), as well as a reset to the DUART in the system communications logic (RESET CMM H).

Descriptions of the signals identified in Figure 4-18 follow in Table 4-2.

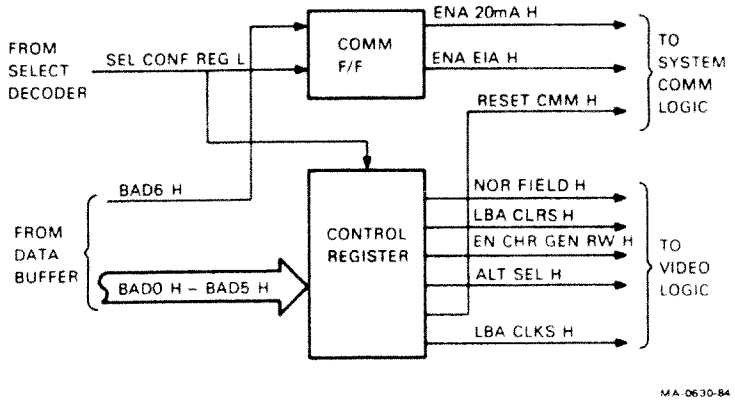


Figure 4-18 Configuration Register Block Diagram

4.3 SIGNAL DESCRIPTIONS

Table 4-2 provides descriptions of all the signals identified in this chapter. These descriptions are provided for reference, and are listed alphabetically by mnemonic, with numeric mnemonics listed last.

4.4 SCHEMATIC REFERENCE INFORMATION

Table 4-3 identifies the logic board component coordinate, and the schematic page and coordinates for each of the CPU logic circuits and components identified in this chapter.

NOTE

The reference information is based on Rev. A of the logic board schematics (CS 5415653-Ø-1), and Rev. A of the PS and monitor board schematics (CS 5415651-Ø-1).

Table 4-2 CPU Logic Signal Descriptions

Mnemonic	Signal	Description
A8 H-A15 H	Address bits 8-15 high	High order byte of address
A15 L	Address bit 15 low	Inverted most significant bit of address used as enable for ROM 1, and for decode input to select decoder
AD0 H-AD7 H	Address/data bits 0-7 high	Bidirectional CPU lines used for output of address, output of data being written, and for input of data being read.
ALE H	Address latch enable high	Enables loading of AD0 H-AD7 H into address latch for low order address value
ALT SEL H	Alternate select high	Enables CPU selection of alternate character generator for read/write when CPU access of video logic is enabled (refer to EN CHR GEN RW H)
BAD0 H-BAD7 H	Buffered data bits 0-7 high	Bidirectional lines for transfer of data between the data buffer and RAM, NVR, video logic, and system communication logic components
CAR DET H	Carrier detect high	Status input to CPU from modem (via EIA host I/F in system communication logic) indicating a good communication line is detected by the modem
CHR ADDR WR L	Character address write low	Enables CPU write of data to attribute latch in video logic when CPU access of video logic is enabled (refer to EN CHR GEN RW H)

Table 4-2 CPU Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
CHRG SEL H	Character generator select high	Defines most significant bit of address to character generator in video logic
CMM INT L	Communication interrupt low	Interrupt to CPU from DUART with value programmable at the DUART
CPU RD L	CPU read low	CPU control for read access of non-ROM system components
DMA H-DMA L	Direct memory access high low	Acknowledgment from CPU relinquishing control of AD0H-AD7H and BAD0H-BAD7H bus lines to the CRT controller in the video logic for access of screen characters and attribute data
DMA REQ L	Direct memory Access Request Low	Interrupt input to CPU from CRT controller in video logic requesting CPU give up buses so CRT controller can access screen character and attribute data
EN CHR GEN L	Enable character generator low	Enables CPU write access of alternate character generator in video logic when CPU access to video logic is enabled (ref. EN CHR GEN RW H), and alternate character generator is selected (refer to ALT SEL H)
EN CHR GEN RW H	Enable character generator read and write low	Enables CPU read/write of video logic components
ENA EIA H	Enable EIA communication high	Defines EIA host port as enabled for communication

Table 4-2 CPU Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
HDR SYNC L	Horizontal sync low	Input to CPU from CRT controller in video logic defining horizontal sync period
KBR	Keyboard receive data	Serial data input from the keyboard to the keyboard I/F for input to CPU (as RxD)
KBT	Keyboard transmit data	Serial data output from the keyboard I/F to the keyboard (originating as TxD at CPU)
LBA CLKS H	Line buffer address clocks high	Clock inputs to line buffer address counter in video logic when CPU access to video logic is enabled (refer to EN CHR GEN RW H)
LBA CLRS H	Line buffer address clears high	Clear input to line buffer address counter in video logic when CPU access to video logic is enabled (refer to EN CHR GEN RW H)
LBF DISABLE H	Line buffer disable high	Disables chip select input to line buffer in video logic
NDR FIELD H	Normal field high	Output to attribute latch in video logic defining background of display as normal
NVR RECALL L	NVR recall low	CPU output defining transfer of stored NVR EAROM data into NVR RAM for definition of terminal operational parameters

Table 4-2 CPU Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
NVR STORE L	NVR store low	CPU output defining transfer of NVR RAM data into NVR EAROM to provide new definition of stored terminal operational parameters
PROD RESET	Production reset	Provides biasing for NVR POWER UP Protect circuit
PSEN L	Program source enable low	CPU output enabling access to ROM
RD L	Read low	Read control generated either in response to CPU RD L, for CPU read transactions, or DMA L, for video access of screen data stored in RAM
RESET COMM H	Reset comm high	Reset signal to DUART in system communication logic to initialize to known start condition
RESET CRT L	Reset CRT low	Reset signal to CRT controller in video logic to initialize to known start condition
RESET TIM L	Reset timing low	Reset signal to timing circuit in video logic to initialize to known start condition
RxD	Receive data	Serial data input to CPU from keyboard I/F (refer to KBR)
SEL ATRØ L	Select attribute RAM Ø low	Enables CPU read/write access or video logic access (during DMA transaction), of attribute RAM Ø

Table 4-2 CPU Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
SEL ATR1 L	Select attribute RAM 1 low	Enables CPU read/write access or video logic access (during DMA transaction), of attribute RAM 1
SEL CONF REG L	Select configuration register low	Enables CPU write access of configuration register
SEL CRT L	Select CRT low	Enables CPU read/write access of CRT controller in video logic
SEL DUART L	Select DUART low	Enables CPU read/write access of DUART in system comm logic
SEL NVR L	Select NVR low	Enables CPU read/write access of NVR
SEL RAMØ L	Select RAM Ø low	Enables CPU read/write access of RAM Ø, during CPU read/write transactions, or video logic read access of RAM Ø during DMA transactions
SEL RAM1 L	Select RAM 1 low	Enables CPU read/write access of RAM 1, during CPU read/write transactions, or video logic read access of RAM Ø during DMA transactions
TxD	Transmit data	Serial data output from CPU to keyboard I/F (refer to KBT)
VERT SYNC L	Vertical sync low	Input to CPU from CRT controller in video logic defining vertical sync period
WR L	Write low	CPU control defining write access of non-ROM system component

Table 4-3 CPU Logic Schematic References

Circuit/ Component	Logic Board Reference No.(s)	Schematic Page	Coordinates
Address Latch	E2	1	B5
Communication F/F	E32	2	B5
Configuration Register	E26	2	B7
CPU	E1,E24,L1,R1	1	B5-B7
CPU clock	Y1,C8,C9	1	B7
Data buffer	E9,E38	1	C1
J1	J1	1	A8
J2*	J2	1	D8
Keyboard connector*	J6	1	C1
KYBD driver, receiver	E54,E55	1	A7-A8
NVR	E17	2	C4
Output components*	L605-L608	1	C1
Power reset	C2,C5,C44,D1,L2,RZ	1	B7
RAM 0	E11	2	C7
RAM 1	E10	2	C5
RAM/DUART decoder	E33,E39	1	B3
RD gate	E31	1	A5
RD/WR decoder	E23,E31	1	A4-A5
ROM 0	E4	1	C5
ROM 1	E3	1	C6

* indicates references are for components physically mounted on PS and monitor board; all other references are for components on logic board.

CHAPTER 5
SYSTEM COMMUNICATION LOGIC

5.1 GENERAL

The system communication logic (shaded area in Figure 5-1) interfaces with the printer, via the printer port, and with the host (via either the EIA host port, or 20 mA host port).

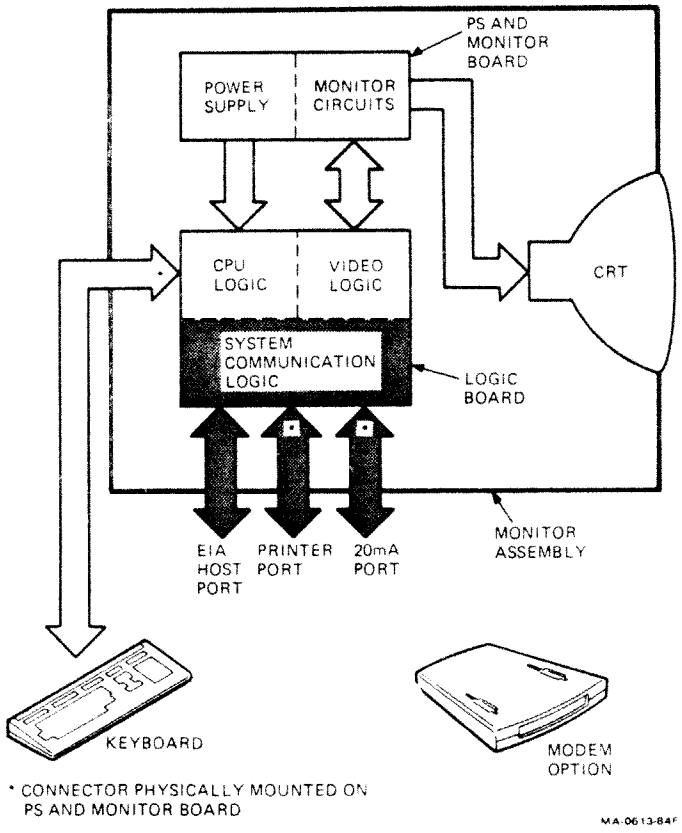


Figure 5-1 VT220 Series Terminal Functional Block Diagram

Printer interfacing is independent of host interfacing. EIA port and 20 mA port interfacing, however, are not independent. When one interface is enabled (EIA host port or 20 mA port), the other is disabled.

NOTE

The enabling and disabling of the host interfaces is primarily a function of firmware response to system configuration data supplied by set-up feature selection.

In addition to communication functions, part of the system communication logic is programmed by the CPU logic to provide control and status report functions for the video logic (refer to the DUART description provided in section 5.2.1).

Operation of the system communication logic is completely under control of the CPU logic. The CPU logic programs operational parameters, reads status, and directs transfer of data to and from the system communication logic.

5.2 MAJOR CIRCUITS AND COMPONENTS

Figure 5-2 provides a block diagram identifying these five major circuits and components that make up the system communication logic.

- Dual asycronous receiver/transmitter (DUART)
- Host data mux
- Printer interface (PRINTER I/F)
- EIA host interface (EIA HOST I/F)
- 20 mA interface (20 mA I/F)

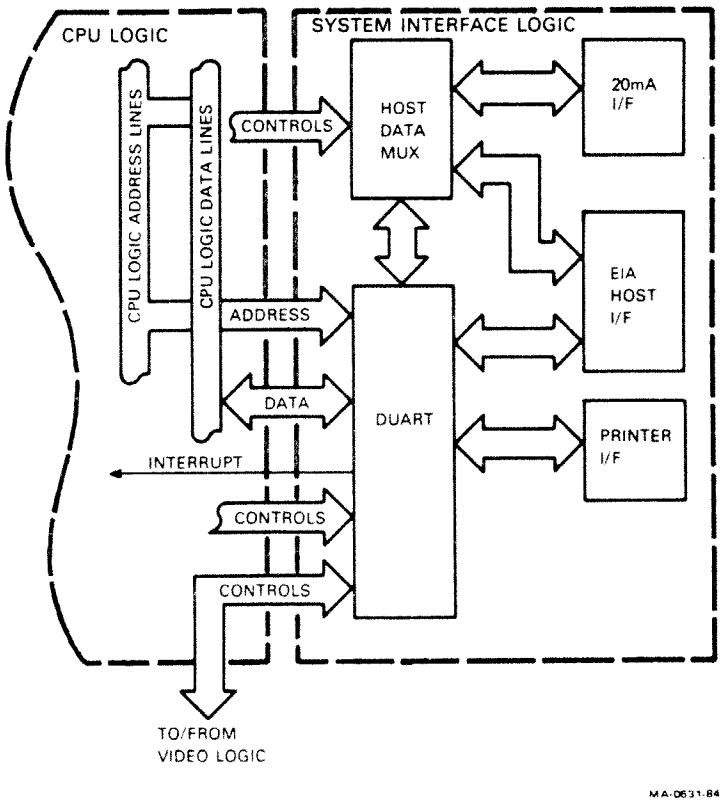


Figure 5-2 System Communications Logic Block Diagram

5.2.1 Dual Asynchronous Receiver/Transmitter (DUART)

The DUART transfers host and printer data between the CPU logic and the following interfaces: EIA host interface, 20 mA interface (with host data transferred between the DUART and the host port via the host data mux), and the printer interface (for printer data).

Figure 5-3 identifies the DUART components.

- 2681 DUART -- is a device that performs the data transfer functions.
- DUART clock -- is a crystal oscillator device that provides 3.6864 MHz input for 2681 DUART timing.

The 2681 DUART device is also used in video logic operations. Some of the 2681 DUART's input and output ports are programmed by the CPU logic for control register (output ports) and status register (input ports) functions.

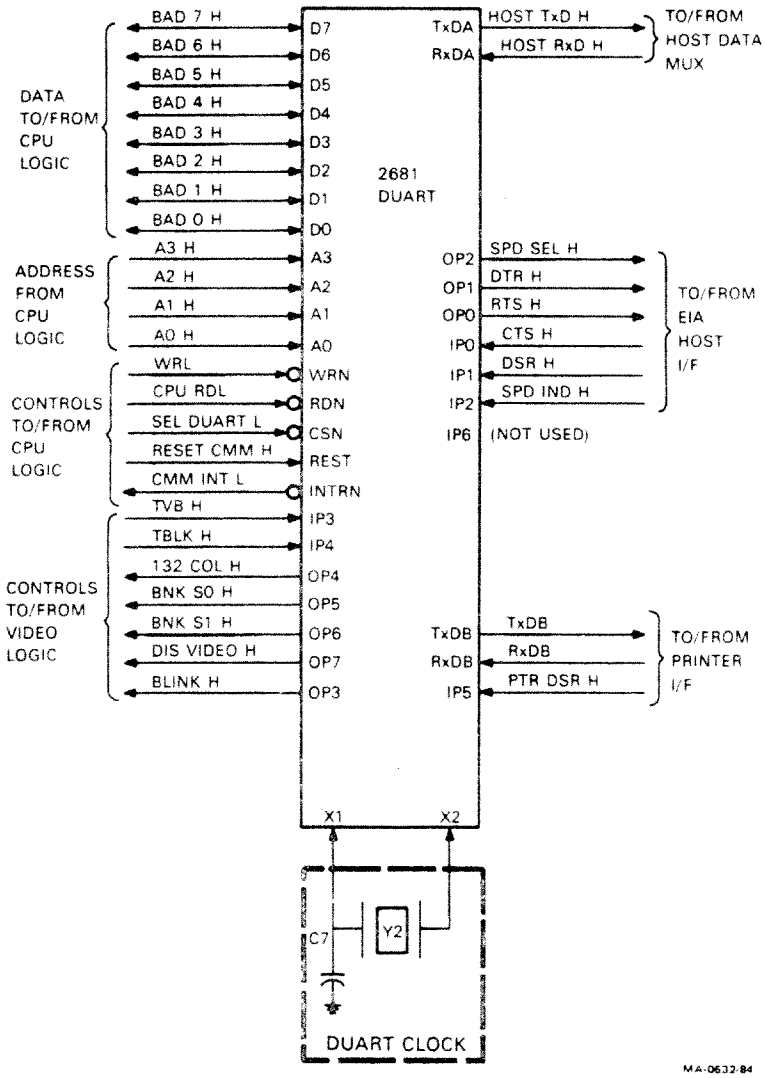


Figure 5-3 DUART Block Diagram

5.2.1.1 2681 DUART Internal Circuits -- Figure 5-4 provides a block diagram showing the major 2681 DUART internal circuits.

- Data bus buffers -- transfer data between the 2681 DUART's internal circuits and the CPU logic data lines.
- Operation control -- decodes read (CPU RD L), write (WR L), address (AØ H-A3 H), and chip enable (SEL DUART L) inputs to enable CPU logic access to control, status, and data registers within the various 2681 DUART circuits.
- Timing -- generates the clock and baud rate signals required for operation.

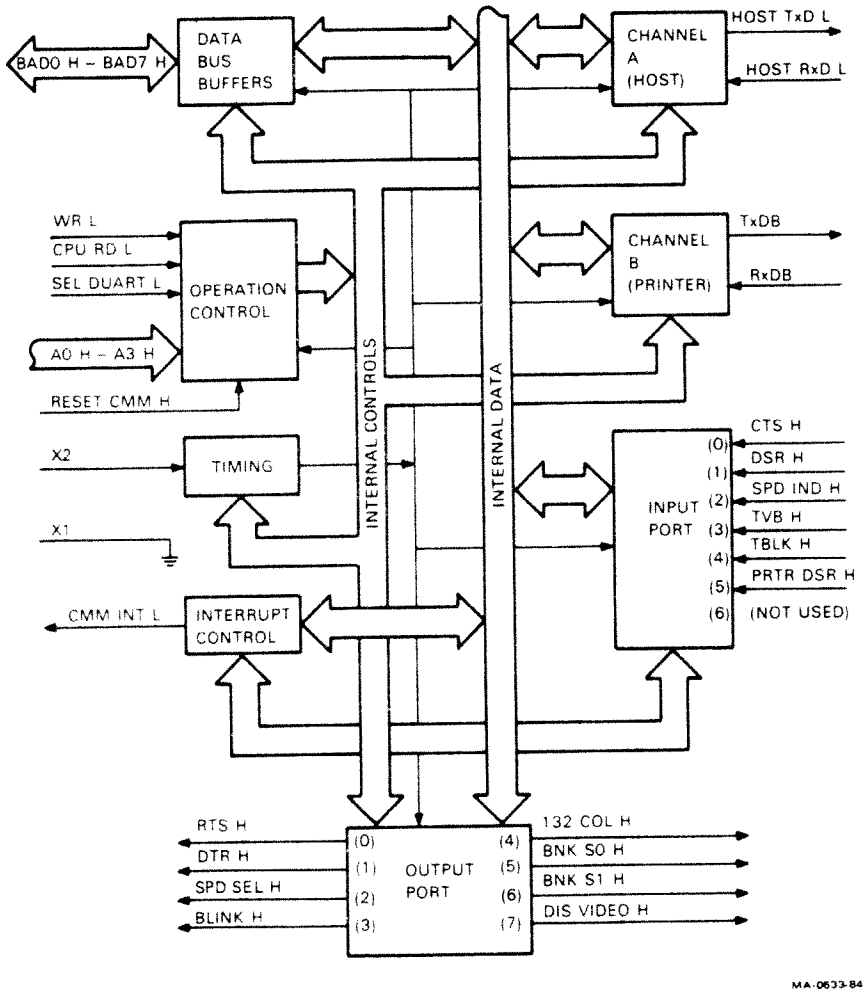


Figure 5-4 2681 DUART Internal Circuits Block Diagram

- Channel A (host) -- converts host transmit data to serial data output (HOST TxD H), and serial host receive data input (HOST RxD H) to parallel data.

- Channel B (printer) -- converts printer port transmit data to serial data output (TxD B), and serial printer port receive data (RxD B) to parallel data.

- Interrupt -- generates a programmable interrupt (CMM INT L) to the CPU logic.

- Output port -- contains eight output ports programmed to provide video logic control register functions (132 COL H, BNKSØ H-BNK S1 H, DIS VIDEO H, AND BLINK H), an EIA host port data terminal ready output (DTR H), and modem handshaking outputs (RTS H and SPD SEL H).

- Input port -- contains state change detection devices and six active input ports (port six is not used) programmed to accept data set ready inputs (PRTR DSR H and DSR H), video logic status register functions (TVB H and TBLK H), and modem handshaking inputs (CTS H and SPD IND H).

Later in this chapter, Table 5-2 describes the signals shown in Figures 5-3 and 5-4.

5.2.1.2 2681 DUART Addresses -- The CPU logic accesses various 2681 DUART internal registers to perform any of the following functions.

- Provides program control for the communication functions
- Provides program control for video logic functions by defining output port values
- Reads communciation function status
- Reads video logic status by reading input port values
- Transfers host and printer data to and from the DUART; CPU logic access is done by addressing a specific device (A0 H-A3 H), defining a read (CPU RD L) or write (WR L) transaction while the DUART is enabled (SEL DUART L).

Table 5-1 defines the registers that can be addressed, with definition provided by address, read/write operation, and the involved circuit (Appendix C provides a complete description of the register bit values).

NOTE

No information is provided in Appendix C for the BF7E (RD or WR) or BF7F (RD or WR). Two of these addresses are used simply to start (BF7E RD) or stop (B7FF RD) the counter, while the other two are used to set (BF7E WR) or reset (BF7F WR) all output register bits.

Table 5-1 2681 DUART Addresses

Address	RD/WR	Circuit	Register
B7FØH	RD	Host channel	Mode (1 & 2) A
B7FØH	WR	Host channel	Mode (1 & 2) A
B7F1H	RD	Host channel	Status A
B7F1H	WR	Host channel	Data clock select A
B7F2H	WR	Host channel	Command A
B7F3H	RD	Host channel	Receive data A
B7F3H	WR	Host channel	Transmit data A
B7F4H	RD	Input port	Input change
B7F4H	WR	Timing	Auxiliary control
B7F5H	RD	Interrupt	Interrupt status
B7F5H	WR	Interrupt	Interrupt mask
B7F6H	RD	Timing	Counter timer (upper)
B7F6H	WR	Timing	Counter timer (upper)
B7F7H	RD	Timing	Counter timer (lower)
B7F7H	WR	Timing	Counter timer (lower)
B7F8H	RD	Printer channel	Mode (1 & 2) B
B7F8H	WR	Printer channel	Mode (1 & 2) B
B7F9H	RD	Printer channel	Status B
B7F9H	WR	Printer channel	Data clock select B
B7FAH	WR	Printer channel	Command B
B7FBH	RD	Printer channel	Receive data B
B7FBH	WR	Printer channel	Transmit data B
B7FDH	RD	Input port	Input port
B7FDH	WR	Output port	Output port configuration
B7FEH	RD	Timing	Start counter command
B7FEH	WR	Output port	Output bits command (set bits)
B7FFH	RD	Timing	Stop counter command
B7FFH	WR	Output port	Output bits command (reset bits)

5.2.1.3 2681 DUART Timing Diagrams -- Figures 5-5 and 5-6 provide timing diagrams for DUART transmit data (Figure 5-5) and receive data (Figure 5-6) activity.

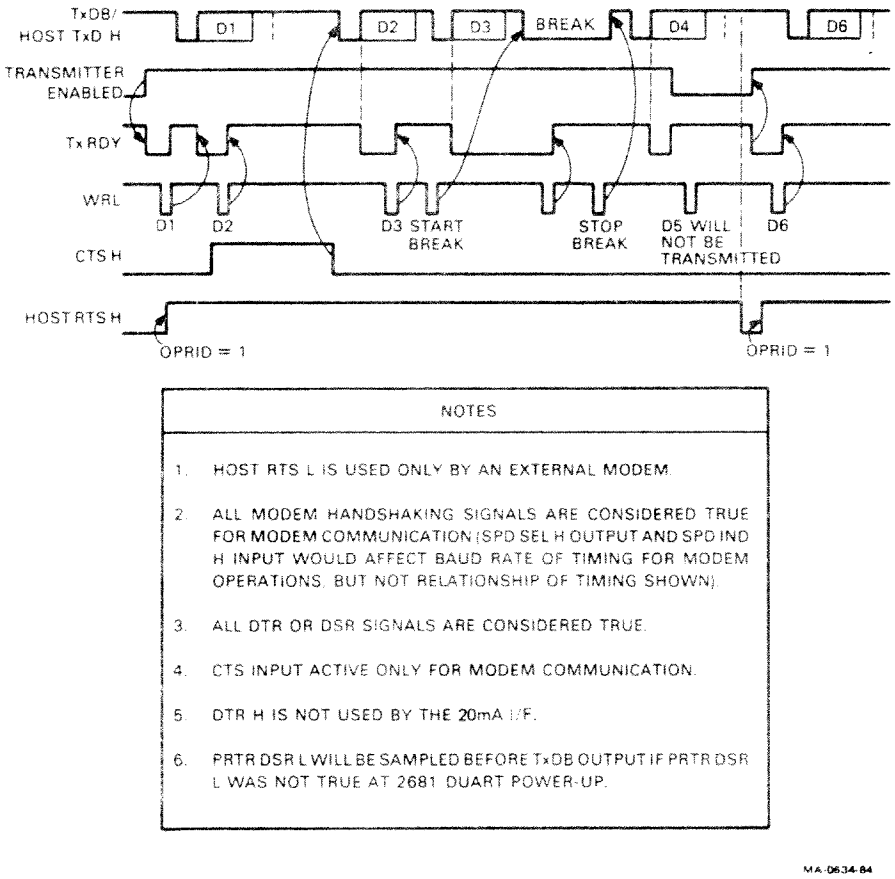


Figure 5-5 2681 DUART: Transmit Data Timing Diagram

5.2.2 Host Data Mux

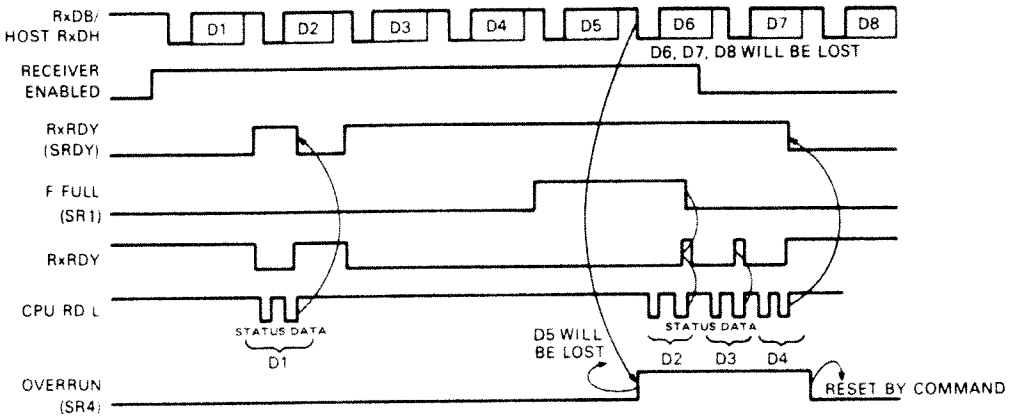
The host data mux routes serial data between the 2681 DUART and either the 20 mA I/F or the EIA host I/F. The I/F selected for data transfer is dependent on control signal inputs from the CPU logic (ENA EIA H or ENA 20 mA H).

The host data (Figure 5-7) mux consists of the following components.

- RxD mux -- gates RxD inputs from the host I/Fs with control inputs from the CPU logic to generate HOST RxD H input to the 2681 DUART (from EIA RxD H when ENA EIA H is true, or from 20 mA receive circuit when ENA 20 mA H is true).

- TxD mux -- routes HOST TxD H input from 2681 DUART out as either 20 mA TxD H (when ENA 20 mA H is true) or as EIA TxD H (when ENA 20 mA H is false).

Later in this chapter, Table 5-2 describes the signals shown in Figure 5-7.

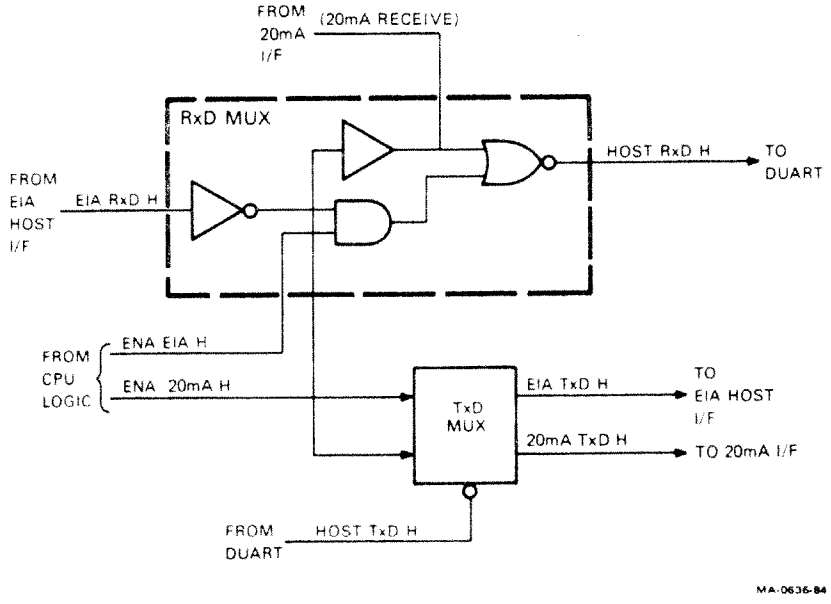


NOTES

1. DTR AND DSR ARE CONSIDERED TRUE.
2. MODEM HANDSHAKING SIGNALS ARE CONSIDERED TRUE FOR MODEM COMMUNICATION.

MA-0635-84

Figure 5-6 2681 DUART: Receive Data Timing Diagram



MA-0636-84

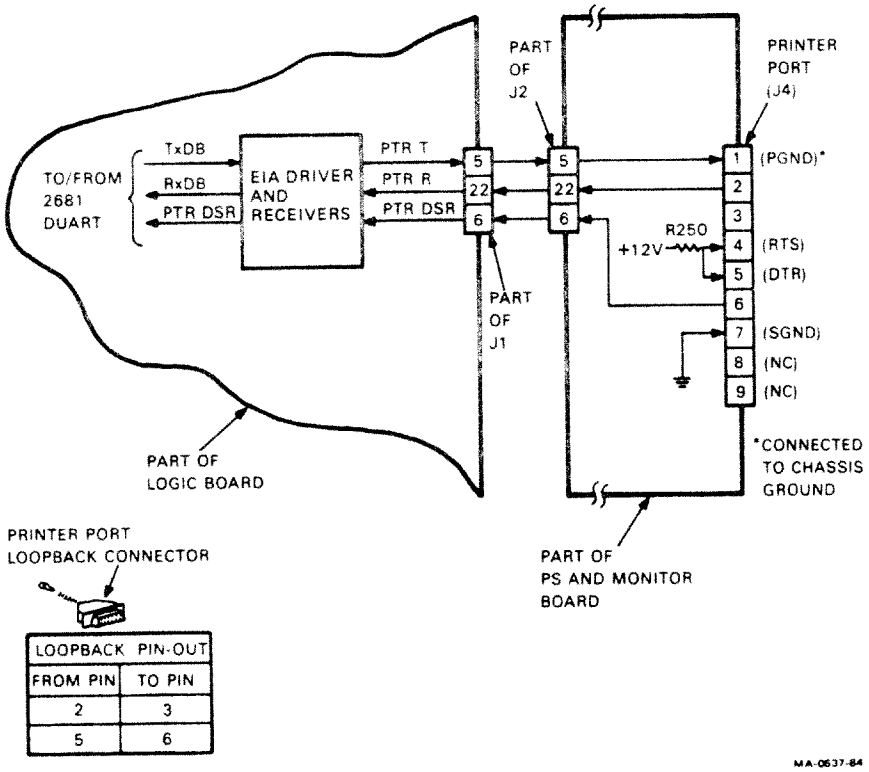
Figure 5-7 Host Data Mux Block Diagram

5.2.3 Printer Interface (I/F)

The printer I/F buffers communication between the terminal and a printer connected to the printer port. Serial control and print data is output to the printer as TxDB, while serial flow control data is input from the printer as RxDB.

Printer I/F components are physically located on both of the terminal PCBs. Figure 5-8 provides a breakdown of the printer interface.

- EIA driver and receivers -- interface TTL logic with EIA level communication lines.
- J1 (logic board)/J2 (PS and monitor board) -- are 25-pin connectors used for routing signals between the two PCBs.
- Printer port (J4) -- is a 9-pin EIA RS232C/RS423 connector, physically mounted on the PS and monitor board; it is used to connect the terminal to the printer.
- Printer port loopback connector -- is used for test purposes; it also routes ready and data signals back into the terminal.



LOOPBACK PIN-OUT	
FROM PIN	TO PIN
2	3
5	6

Figure 5-8 Printer I/F Block Diagram

Figure 5-8 also provides a pin-out for the printer port loopback connector. Figure 5-9 provides a complete pin-out of the interconnection between the logic board and the PS and monitor board. This connection is used for routing signals between the video logic and the monitor circuits, between the power supply and the logic board, between the keyboard connector and the CPU logic, and between the 20 mA I/F components, as well as between the printer I/F components.

Later in this chapter, Table 5-2 describes the signals shown in Figure 5-8.

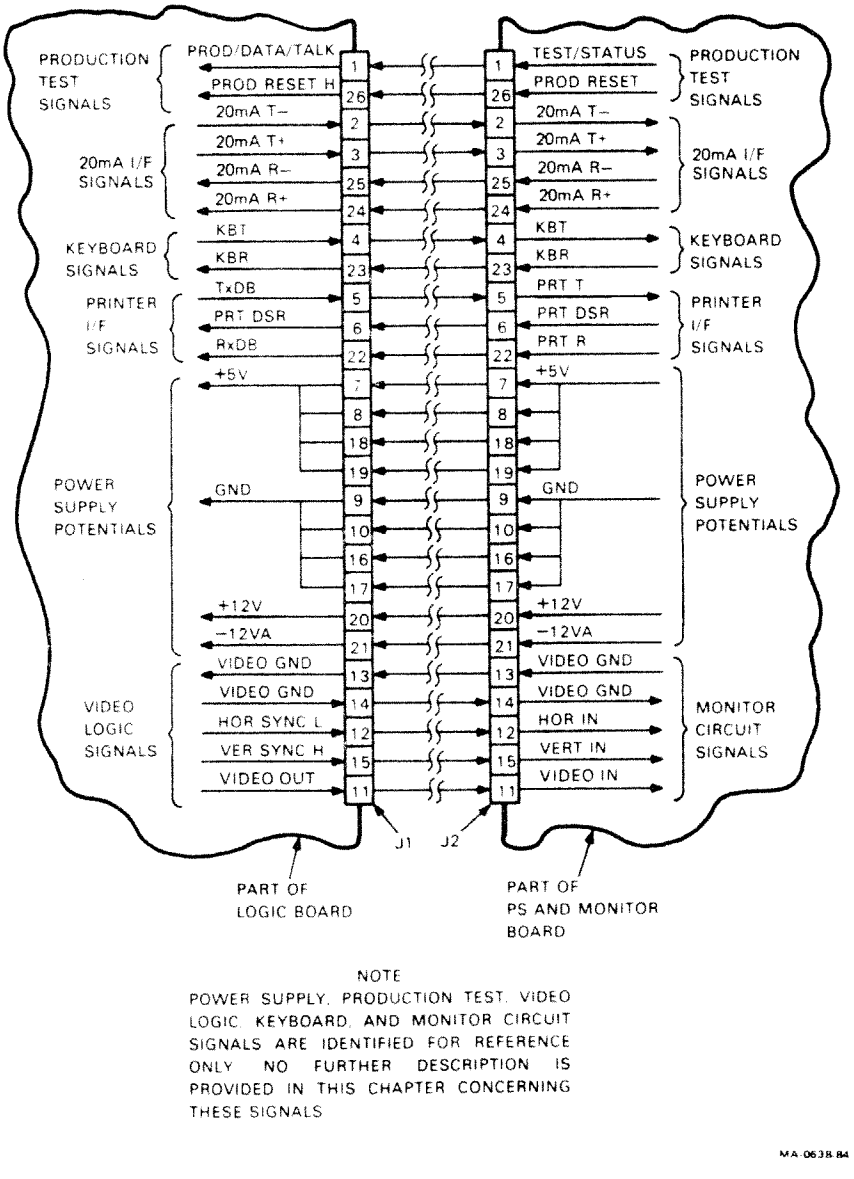


Figure 5-9 Logic Board (J1)/PS and Monitor Board (J2) Interconnection Diagram

5.2.4 EIA Host Interface (I/F)

The EIA host interface buffers communication between the terminal and a host (or modem) connected to the EIA host port.

Figure 5-10 provides a breakdown of the EIA host interface.

- EIA driver and receiver -- interface TTL logic with EIA communication lines.
- J2 -- is a 25-pin EIA RS232C/RS423 connector, physically mounted on the logic board; it is used to connect the terminal to a local or remote host (via modem).
- Data loopback connector -- used for test purposes, routes signals back into terminal.
- J4 -- is a 8-pin connector with jumper plug inserted when VT22X modem option is installed; it provides output of operational voltages and data/talk signal (PROD/DATA/TALK) to the modem (J4 pins are shorted by jumper as shown in Figure 5-10).

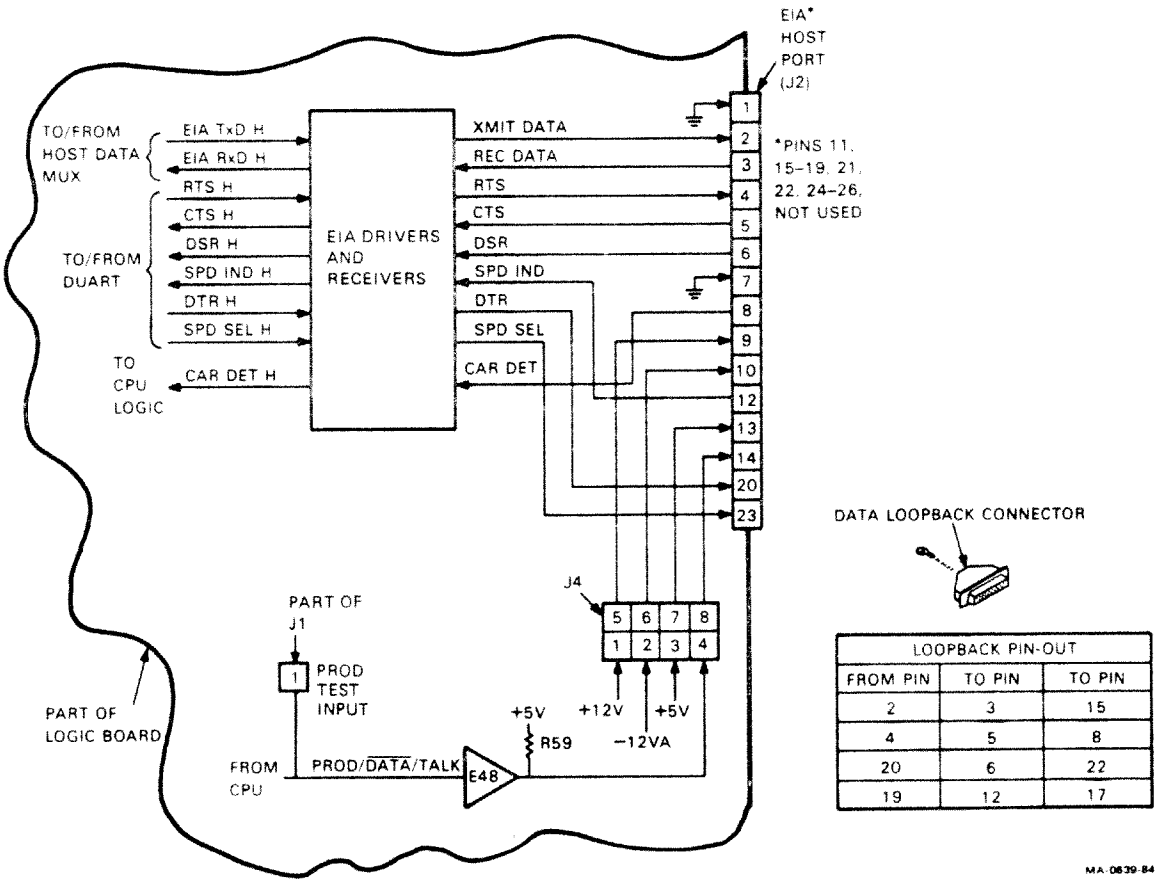


Figure 5-10 EIA Host I/F Block Diagram

Figure 5-10 provides a pin-out for the EIA host port loopback connector. Later in this chapter, Table 5-2 describes the signals shown in Figure 5-10.

5.2.5 20 mA Interface (I/F)

The 20 mA interface buffers communication between the terminal and a local host connected to the 20 mA host port. Serial data is output to the host as 20 mA TxD H, and input from the host as 20 mA RxD H.

20 mA I/F components are physically located on both of the terminal pcbs. The 20 mA interface (Figure 5-11) is composed of the following parts.

- Transmit TTL/20 mA converter -- provides isolation between the TTL level transmit data signal (20 mA TxD H) at the terminal, and 20 mA level signals (T+/T-) on the 20 mA port communication lines.
- Receive 20 mA/TTL converter -- provides isolation between the TTL level receive data signal (20 mA RxD H) at the terminal, and 20 mA level signals (R+/R-) on the 20 mA port communication lines.

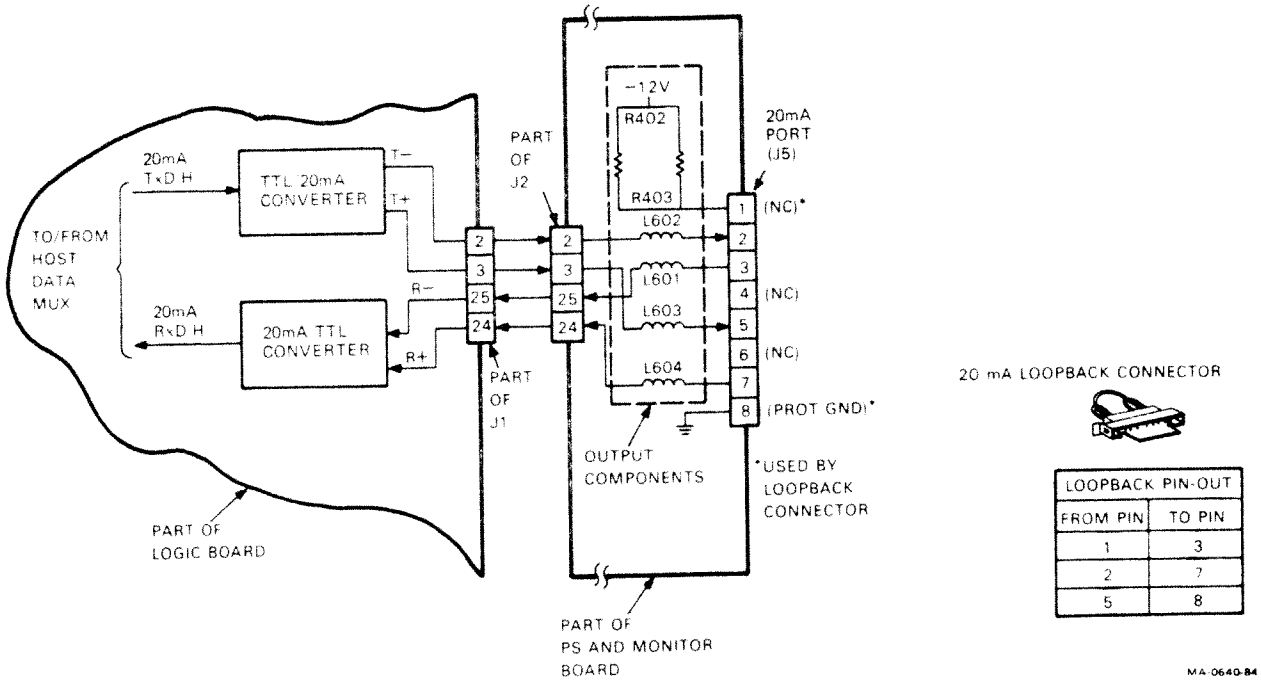


Figure 5-11 20 mA I/F Block Diagram

- J1 (logic board)/J2 (PS and monitor board) -- are 25-pin connectors used for routing signals between the two PCBs.

- Output components -- provide control signals and voltage potentials required for 20 mA loop operation, and lessen radiated high frequency noise.

- 20 mA host port (J5) -- is a 8-pin 20 mA connector, physically mounted on the PS and monitor board, used to connect the terminal to a local host.

- 20 mA loopback connector -- is used for testing, routes signals back into the terminal

Figure 5-11 provides a pin-out for the 20 mA loopback connector. For a complete pin-out of the connection between the logic board and the PS and monitor board, refer to Figure 5-9.

Complete descriptions of the signals shown in Figure 5-11 follow in Table 5-2.

5.3 SIGNAL DESCRIPTIONS

Table 5-2 provides descriptions of all the signals identified in this chapter. These descriptions are provided for reference, and are listed alphabetically by mnemonic, with numeric mnemonics listed last.

Table 5-2 System Communication Logic Signal Descriptions

Mnemonic	Signal	Description
A0-A3 H	Address bits 0-3 high 0-3 high	Input to DUART from CPU logic defining DUART device to be accessed for read (CPU RD L0 or write (WR L) transaction
BAD0-BAD7 H	Buffered data bits 0 through 7 high	Bus lines for transfer of data between DUART and CPU logic
BLINK H	Blink H	Control output from DUART to video logic defining blinking attribute
BNKS0-BNKS1 H	bank select 0-1 high	Control outputs from DUART to video logic providing two most significant bits of address to line buffer memory in that logic

Table 5-2 System Communication Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
CAR DET H	Carrier detect high	Status input from modem, routed to CPU logic by EIA I/F, indicating modem has detected a good communication line
CMM INT L	Communication interrupt low	Programmable interrupt output from DUART
CPU RD L	CPU read low	CPU logic input to DUART defining a read transaction when DUART is selected for access (SEL DUART L)
CTS H	Clear to send high	Handshaking input from modem, routed to DUART via EIA host I/F, indicating modem is ready to receive transmit data (EIA TxD H)
DIS VIDEO H	Disable video high	Control output from DUART to video logic defining disabled video
DSR H	Data set ready high	Handshaking input from modem, routed to DUART via EIA host I/F, indicating modem is ready for communication activity
DTR H	Data terminal ready high	Two outputs, one for printer and one for modem; Handshaking output from DUART to modem, via EIA host I/F, indicating terminal is ready for communication activity; output from printer port developed from +12 V whenever terminal is powered
EIA RxD H	EIA receive data high data high	Serial data input from the EIA Host port (as REC DATA) to the EIA host I/F, from either a local host or modem, and routed to DUART (as HOST RxD H), via host data mux

Table 5-2 System Communication Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
EIA TxD H	EIA transmit data high	Serial data output from the EIA host port (as XMIT DATA) to either a local host or modem, originating at DUART (as HOST TxD H), and routed to EIA host port via host data mux and EIA host I/F
ENA EIA H	Enable EIA high	Control input from the CPU logic enabling host data mux to pass data between the DUART and the EIA host I/F
ENA 20 mA H	Enable 20 mA high	Control input from the CPU logic enabling host data mux to pass data between the DUART and the 20 mA I/F
HOST RxD H	Host receive data high	Serial data input to the DUART from the host data mux (refer to EIA RxD H and 20 mA RxD H)
HOST TxD H	Host transmit data high	Serial data output from the DUART to the host data mux (refer to EIA TxD H and 20 mA TxD H)
PGND	Protective ground	Printer port ground potential output to printer
PROD/DATA/ TALK	Production/data/talk	Modem control signal high for talk mode and low for data mode
PROT GND	Protective ground	20 mA port output used for loopback testing (ties T+ to ground)
PTR DSR	Printer data set ready	High input to DUART from printer I/F when printer is ready for communications activity
PTR R	Printer receive	Serial data input from printer port routed to DUART by printer I/F (as RxDB)

Table 5-2 System Communication Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
PTR T	Printer transmit	Serial data output to printer port from printer I/F originating at DUART (as TxDB)
R-/R+	Receive -/receive +	20 mA loop serial data inputs to the 20 mA I/F sent to host data mux (as 20 mA RxD H) where it is routed to DUART (as HOST RxD H)
REC DATA	Receive data	Serial data input to EIA host port (refer to EIA RxD H)
RESET CMM H	Reset communication high	CPU logic input to DUART resetting DUART to known start condition
RTS H	Request to send high	Two outputs, one for printer and one for modem: Handshaking output to modem from DUART, via EIA host I/F, when DUART has data to be transmitted; Output to printer developed from +12 V whenever terminal is powered
RxDB	Receive data channel B	Serial data to DUART originating at printer port (refer to PTR R)
SEL DUART L	Select DUART low	Enable to DUART from CPU logic for read (CPU RD L) or write (WR L)
SGND	Signal ground	Ground output from printer port
SPD IND H	Speed indicator high	Handshaking input from modem to DUART, via EIA host I/F, defining receive and transmit speeds of 1200 bps, regardless of the speeds selected by set-up feature

Table 5-2 System Communication Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
SPD SEL H	Speed select high	Handshaking output from DUART to modem, via EIA host I/F, when set-up selection of receive speed is greater than 600 bps
T-/T+	Transmit -/transmit +	20 mA serial data outputs from 20 mA I/F originating at DUART (as HOST TxD H), and routed to 20 mA I/F by host data mux (as 20 mA TxD H)
TBLK H	Test blank high	Status input to DUART from video logic indicating video blank circuitry is functional (used only during self-test)
TVB H	Test video bits high	Status input to DUART from video logic indicating video serial steam is functional (used only during self-test)
TxDB	Transmit data	Serial data output from the DUART Channel B for the printer (refer to PRT T)
WR L	Write low	Selects DUART for write transaction when DUART is enabled (SEL DUART L)
X1/X2	Crystal 1/crystal 2	Crystal input to DUART for timing
XMIT DATA	Transmit data	Serial data output from EIA host port (ref. EIA TxD H)
-12 V	-12 Vdc	Voltage potential output from 20 mA port developed across two resistors and used for loopback testing (ties R- to -12 V)
+12 V	+12 Vdc	Voltage potential used to develop RTS and DTR outputs from printer port

Table 5-2 System Communication Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
20 mA RxD H	20 mA receive data high	Serial data input from the 20 mA port (as R-/R+) to the 20 mA I/F from a local host, and routed to DUART (as HOST RxD H), via host data mux
20 mA TxD H	20 mA transmit data high	Serial data output from the 20 mA port (as T-/T+) to a local host, originating at DUART (as HOST TxD H), and routed to 20 mA port via host data mux and 20 mA I/F
132COL H	132 column high	Control output from DUART to video logic defining screen attribute of 132 columns enabled

5.4 SCHEMATIC REFERENCE INFORMATION

Table 5-3 identifies the logic board and PS and monitor board component coordinate, and the schematic page and coordinate for each of the system communication logic components and circuits identifed in this chapter.

NOTE

The reference information provided in Table 5-3 is based on CS 5415653-0-1, Rev. A, for logic board references, and on CS 5415651-0-1, Rev. A, for the PS and monitor board.

Table 5-3 System Communication Logic Schematic References

Circuit/ Component	PCB Name	Board Ref. Numbers	Schematic Page	Loc.
DUART (2681)	Logic	E15	6	D7
DUART clock	Logic	Y2,C7	6	C7
EIA host port	Logic	J2	6	D3
J1	Logic	J1	6	A7,B1, B5,C6
			5	B1
			1	A8
J2	PS/MTR	J2	1	D8
EIA drivers, receivers (EIA)	Logic	E52-E57,R27-R31, R35,R53,C22,C23	6	D6-D2/ C5-C2
EIA drivers, receivers (PRTR)	Logic	E51,E52,R32,R33, C14,C15	6	C6
Output components	PS/MTR	L601-L604,R402, R403	1	C1
Printer port	PS/MTR	J4,R250	1	D1
Rx 20 mA/TTL converter	Logic	E40,C11,D7, R46-R51,Q5,Q6	6	B6
RxD mux	Logic	E24,E31,E39,E48	6	A5
Tx TTL/20 mA converter	Logic	E47,E48,C12,C13, D6,D8,R44,R45, R52,Q3,Q4	6	B6-B8
TxD mux	Logic	E33	2	A4
20 mA port	PS/MTR	J5	1	C1

CHAPTER 6
VIDEO LOGIC

6.1 GENERAL

The video logic (shaded portion of Figure 6-1) generates the outputs needed to drive the monitor circuits and CRT (video and sync signals). It can also drive an optional slave monitor device (composite video output).

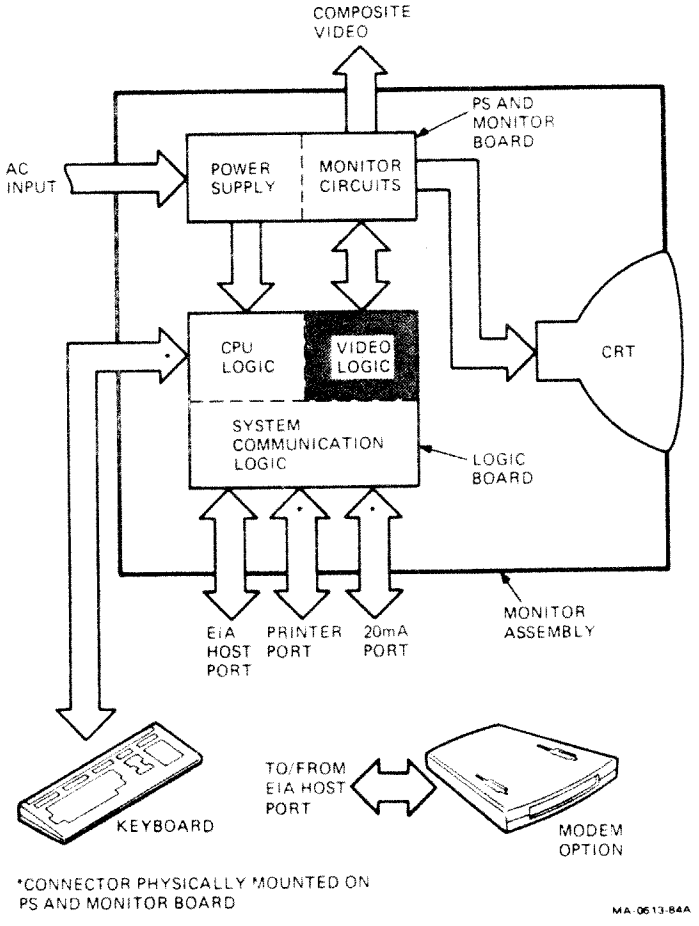


Figure 6-1 VT220 Series Terminal Functional Block Diagram

The video outputs are developed from character address and attribute values stored in a line buffer memory within the video logic. As each scan line of display is processed, the character address values are used to select the characters to be processed for the scan line, while the attribute values define the attributes to be associated with the characters being processed.

Character and attribute data is defined by CPU write transactions. Character address data is stored in the CPU logic screen RAM. Attribute values associated with each character are written into the CPU attribute RAM at an address directly corresponding to the address of the character address value stored in the screen RAM. During DMA transactions, the video logic transfers the character and attribute values to the line buffer memory for processing.

DMA transactions occur during the first scan line of each row of screen data. The data is read out of the screen and attribute RAMs in the CPU logic and transferred to a line buffer in the video logic. At the same time the character address and attribute data is applied to character generator and attribute circuits to get the character dots for the first scan line. The remaining scan lines are processed from the data stored in the line buffer.

6.2 MAJOR CIRCUITS AND COMPONENTS

The video logic (Figure 6-2) consists of the following components/circuits.

- CRT Controller
- Timing generator (TIMING GEN)
- Blank circuits
- Character generator (CHAR GEN)
- Attribute circuits
- Video converter
- Video output

The video logic also uses input and output ports of the system communication logic's 2681 DUART for status reporting (input ports) and control register (output ports) functions (refer to the description of 2681 DUART in section 5.2.1).

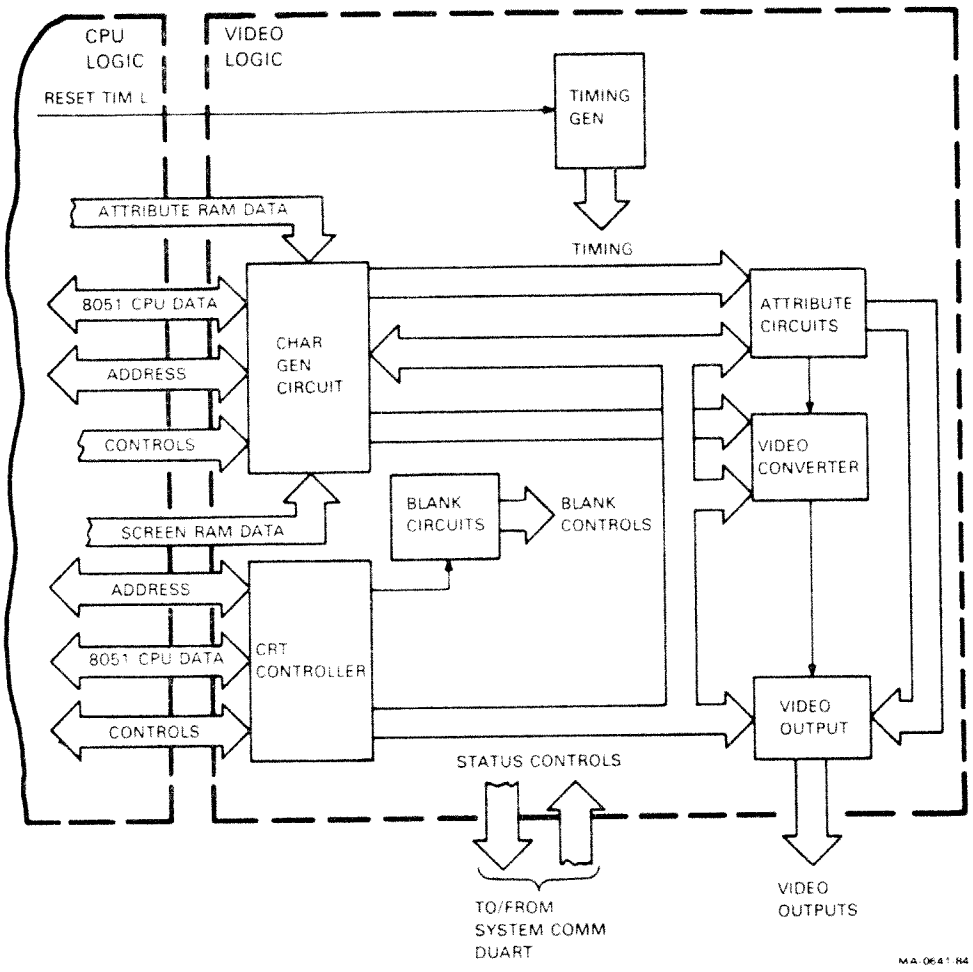


Figure 6-2 Video Logic Block Diagram

6.2.1 CRT Controller

The CRT controller (Figure 6-3) is a 9007 video processor and controller (VPAC) device. The 9007 VPAC generates address and control signals for the following functions.

- Request for DMA transactions
- Address values used during DMA transactions to access character address and attribute data to be transferred to the character generator circuit
- Synchronization controls for defining vertical and horizontal retrace periods
- Address values to define specific scan line of an addressed row of characters to be processed out for video by the character generator
- Controls for screen blanking

The 9007 VPAC is not involved in cursor positioning. In the VT220, cursor positioning is a function of CPU logic firmware.

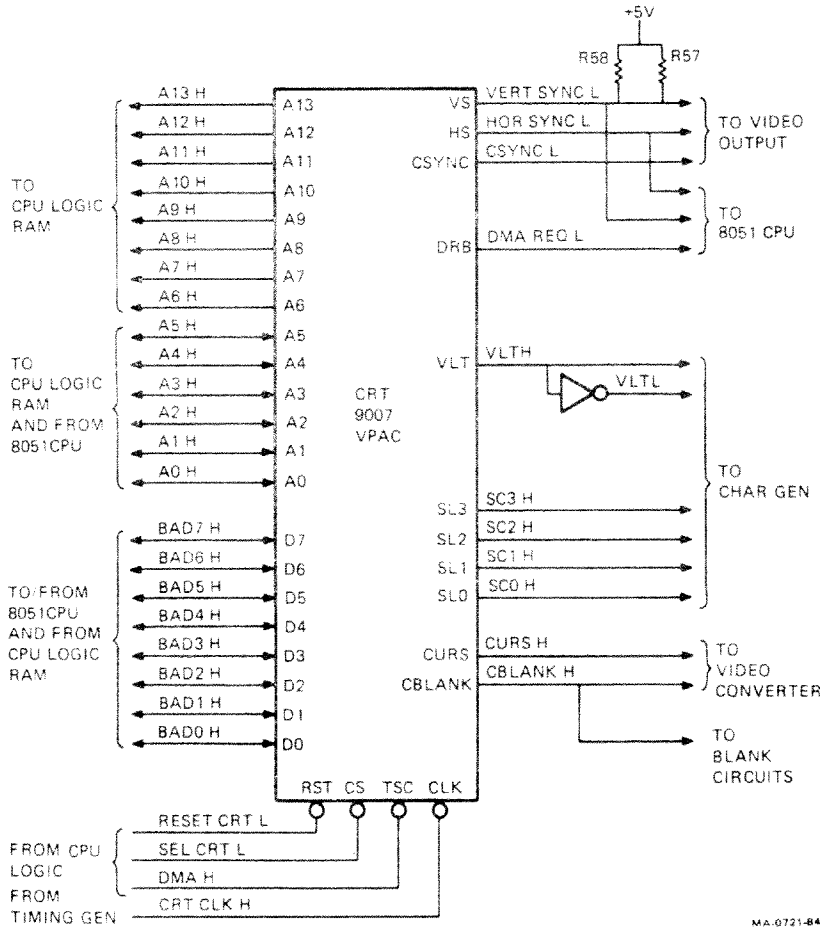


Figure 6-3 CRT Controller Block Diagram

6.2.1.1 9007 VPAC Internal Circuits -- The 9007 VPAC (Figure 6-4), as used in the VT220 series terminal, consists of the following components/circuits.

- Decode -- decodes CPU address inputs to determine type of operation to occur, of register device to be accessed.
- Timing and control -- generates control and address values needed for overall video logic functionality.

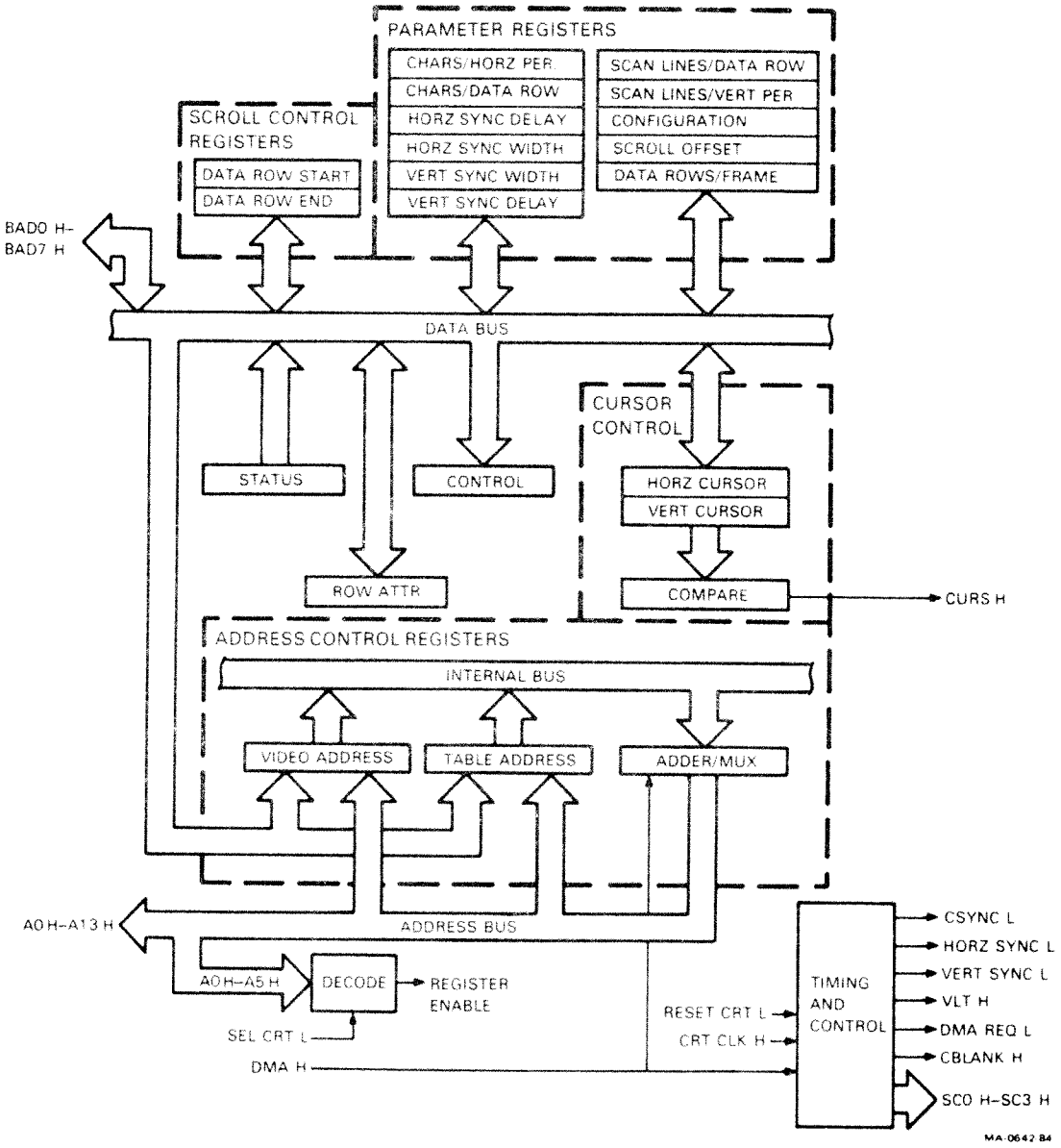


Figure 6-4 9007 VPAC Internal Block Diagram

- Address control registers -- generates address values used to address CPU logic screen and attribute RAMs, including registers containing the starting address of character and attribute values (table address register) and the current address to be accessed (video address register).

- Cursor control registers -- generate CURS H output (used for double height/double width data row function) based on comparison of horizontal and vertical cursor position values in relation to portion of screen display currently being processed.

- Parameters registers -- contain information defining operational parameters concerning video control and format.

- Scroll control registers -- define start and stop display data row values for scroll or screen blanking operations.

- Row attribute register -- is a two-bit register that defines height and width values for data row being processed

- Status register -- contains flags concerned with whether or not vertical retrace is in progress, or whether or not the final table address has been read (all data to be displayed during a given complete scan of the screen has been read out of CPU logic RAM).

- Control register -- defines operational modes for the 9007 VPAC.

Later in this chapter, Table 6-2 describes the signals shown in Figures 6-3 and 6-4.

6.2.1.2 9007 VPAC Addresses -- The CPU uses write transactions to program operational modes, parameters, cursor register values, scroll and screen blanking row values, display memory position, and row width and height values, as well as two commands affecting entire 9007 VPAC operation (start and reset). Read transactions are used by the CPU to obtain status or to verify current cursor register values.

Access to internal 9007 VPAC registers is enabled by a low chip enable input (SEL CRT L) accompanied by a valid address. No read or write enable is used, as the address not only defines the device to be accessed, but also determines whether it is to be accessed for read or write.

Table 6-1 provides a complete listing of the 9007 VPAC addresses, with identification of the addresses which are valid for 9007 VPAC operation, as this device is used in the VT220, and the device or command the address affects.

NOTE

A complete description of the bit values associated with the various 9007 VPAC registers is provided in Appendix C.

Table 6-1 9007 VPAC Internal Addresses

Address (hex)	RD/WR	Device/command
17C0	WR	Characters/horizontal row register
17C1	WR	Characters/data row register
17C2	WR	Horizontal sync delay register
17C3	WR	Horizontal sync width register
17C4	WR	Vertical sync width register
17C5	WR	Vertical sync delay register
17C6	WR	Configuration/skew register
17C7	WR	Data rows/frame register
17C8	WR	Scan lines/data row and scan Lines/vertical period registers
17C9	WR	Scan lines/vertical period register
17ca	--	(not used in VT220)
17CB	WR	Control register
17CC	WR	Table address register (low byte)
17CD	WR	Table address register (high byte)
17CE	--	(not used in VT220)
17CF	WR	Row attribute register
17D0	--	(not used in VT220)
17D1	WR	Data row start register
17D2	WR	Data row end register
17D3-17D4	--	(not used in VT220)
17D5	WR	Start command (see note)
17D6	WR	Reset command (see note)
17D7	WR	Smooth scroll offset register
17D8	WR	Vertical cursor register
17D9	WR	Horizontal cursor register
17DA-17F7	--	(not used in VT220)
17F8	RD	Vertical cursor register
17F9	RD	Horizontal cursor register
17FA	RD	Status register
17FB-17FF	--	(not used in VT220)

NOTE

Start and reset commands are not written to any specific device. They are decoded into start or reset operations by the 9007 VPAC.

6.2.1.3 9007 VPAC Transactions -- The 9007 VPAC is responsible for the basic control of video logic operations, including all of the following functions.

- Requesting access of CPU logic screen and attribute RAM's for DMA transactions using DMA REQ L, with DMA H granting access
- Accessing character address and attribute values using A0 H-A13 H address outputs
- Defining of trace and retrace periods through VLT H, CSYNC L, HORZ SYNC L, and VERT SYNC L outputs
- Controlling screen blanking using CBLANK H output
- Controlling smooth and jump scroll operations
- Defining double width/double height data rows using CURS H output

Smooth and jump scroll operations are controlled by CPU programming of 9007 VPAC registers. During jump scroll, new data lines are displayed as soon as they are received. During smooth scroll, the screen is offset by a specified number of scan lines for each vertical retrace (for example, five retrace periods are required to display a complete new data row when offset is two scan lines per retrace period), resulting in each scroll being done in increments over a longer period of time.

Double height/double width is also controlled by CPU programming of 9007 VPAC registers. The CPU programs the cursor positioning registers with the address of the data row to be double width, and programs the row attribute register for single height/double width or double height/double width functions (refer to Figure C-26 in Appendix C for row attribute register values and functionality associated with those values). The 9007 VPAC will then perform appropriate DMA transactions to process a data row for single or double height, while generating CURS H output during CBLANK H time to define double width operation (refer to Section 6.2.7.1 for description of how CURS H is used by the conversion control portion of the video conversion circuit to control double width).

Figures 6-5 through 6-8 provide transaction and timing diagrams for 9007 VPAC DMA, sync, and blanking operations. Additional timing diagrams concerning video logic operation are provided in the description of the timing generator circuitry (refer to section 6.2.2).

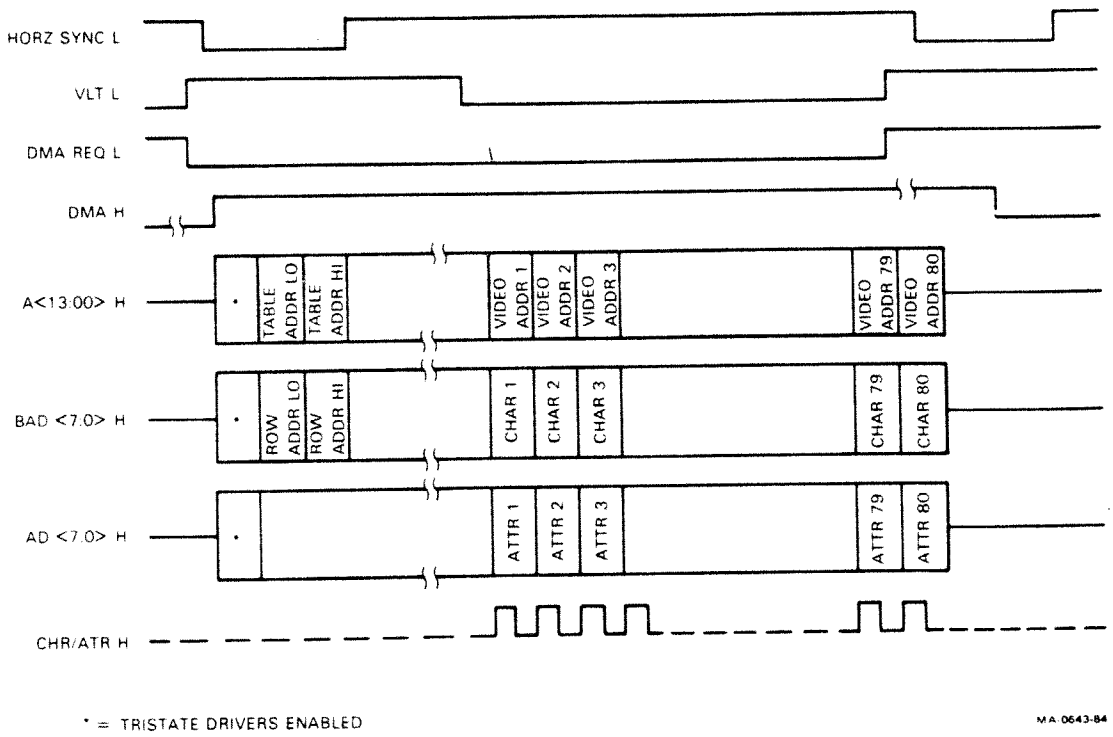


Figure 6-5 9007 VPAC: DMA Transaction Diagram

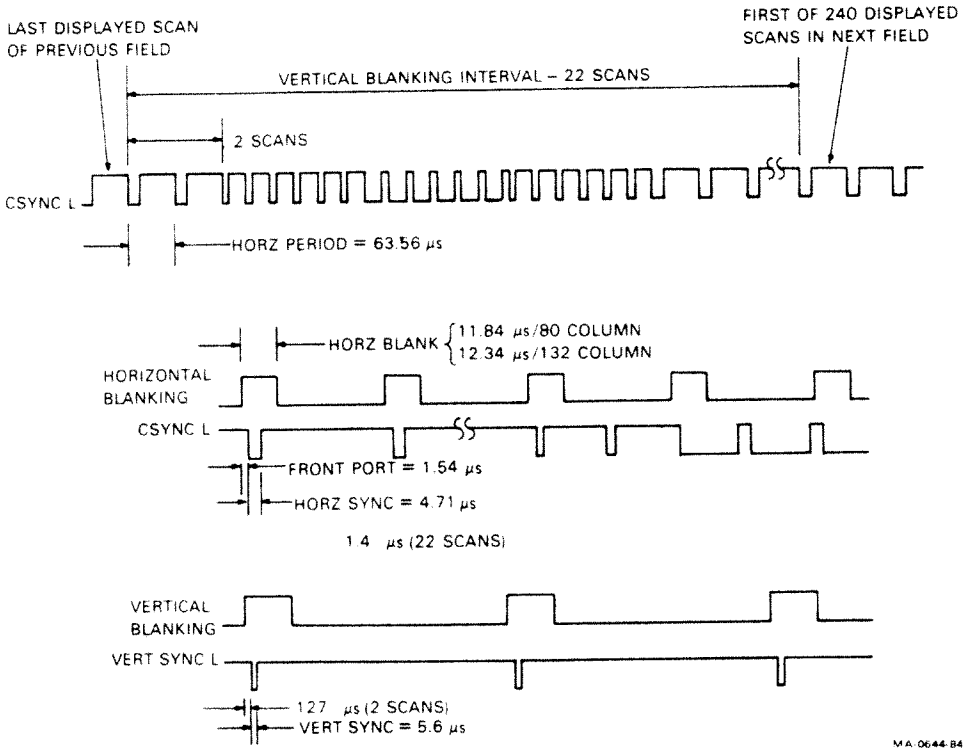
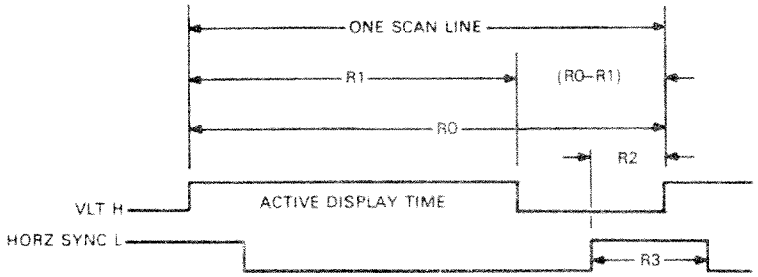


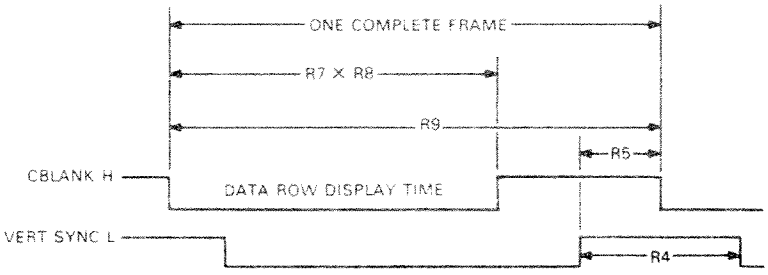
Figure 6-6 9007 VPAC: Composite Sync and Blanking Timing Diagram



NOTES		
R1	–	CHARACTERS PER DATA ROW REGISTER VALUE (80 OR 132)
R0	–	CHARACTERS PER HORIZONTAL PERIOD REGISTER VALUE
R0–R1	–	HORIZONTAL RETRACE DEFINED BY R0 VALUE LESS R1 VALUE
R2	–	HORIZONTAL DELAY REGISTER VALUE
R3	–	HORIZONTAL SYNC WIDTH REGISTER VALUE

MA-0645-84

Figure 6-7 9007 VPAC: Horizontal Timing



NOTES		
R4	–	VERTICAL SYNC WIDTH REGISTER VALUE
R5	–	VERTICAL DELAY REGISTER VALUE
R7×R8	–	VISIBLE DATA ROWS PER FRAME REGISTER VALUE (R7) TIMES SCAN LINES PER ROW REGISTER VALUE (R8)
R9	–	SCAN LINES PER FRAME REGISTER VALUE

MA-0646-84

Figure 6-8 9007 VPAC: Vertical Timing

6.2.2 Timing Generator

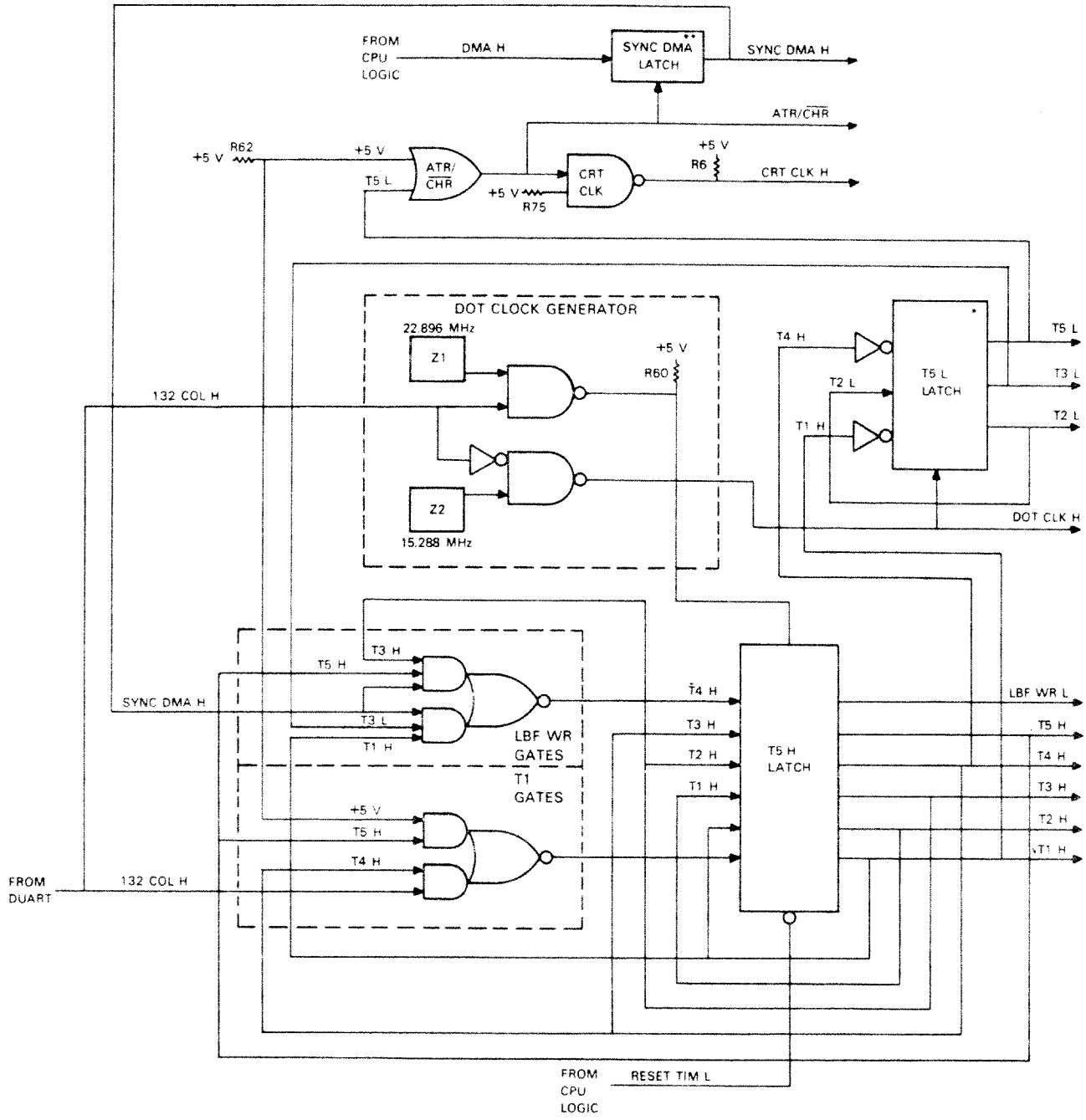
The timing generator provides all timing signals required for video logic operation. Where the 9007 VPAC provides basic control for video logic operation, the timing generator provides the timing required to carry out those operations.

Timing outputs depend on whether the video logic is processing 80 or 132 characters per row display (defined by 132COL H input from 2681 DUART). During 80-column timing, ten dot clocks (DOT CLK H) are used to process a complete character. During 132-column timing, nine dot clocks are used.

Figure 6-9 identifies the components that make up the timing generator.

- Dot clock generator -- generates basic timing (as DOT CLK H) from either 22.896 MHz source (for 132-column) or 15.288 MHz source (for 80-column).
- LBF WR gates -- are enabled during DMA transactions (SYNC DMA H) to provide low input to T5 H latch for LBF WR L generation to load character and attribute data into line buffer memory in character generator.
- T1 gates -- are enabled to generate low input to T5 H latch for T1 H false on either T4 H (for 132-column) or T5 H (for 80-column).
- T5 H latch -- generates active high timing signals and active low line buffer memory load signal (LBF WR L).
- T5 L latch -- generates active low timing signals.
- SYNC DMA latch -- latches value of DMA H input on ATR/CHR going low, synchronizing DMA transaction activity.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-9. Figure 6-10 provides a diagram of DMA and visible line timing for 80-column display. A 132-column display is identical except that all action occurring at the tenth dot clock in 80-column display occurs at the ninth dot clock in 132-column display.



* SHARES SAME PHYSICAL COMPONENT (LS174 LATCH) AS SERIAL AND SIN LATCHES IN VIDEO CONVERTER.
** SHARES SAME PHYSICAL COMPONENT (LS174 LATCH) AS ATTRIBUTE LATCH 2.

MA-0711-84

Figure 6-9 Timing Generator Block Diagram

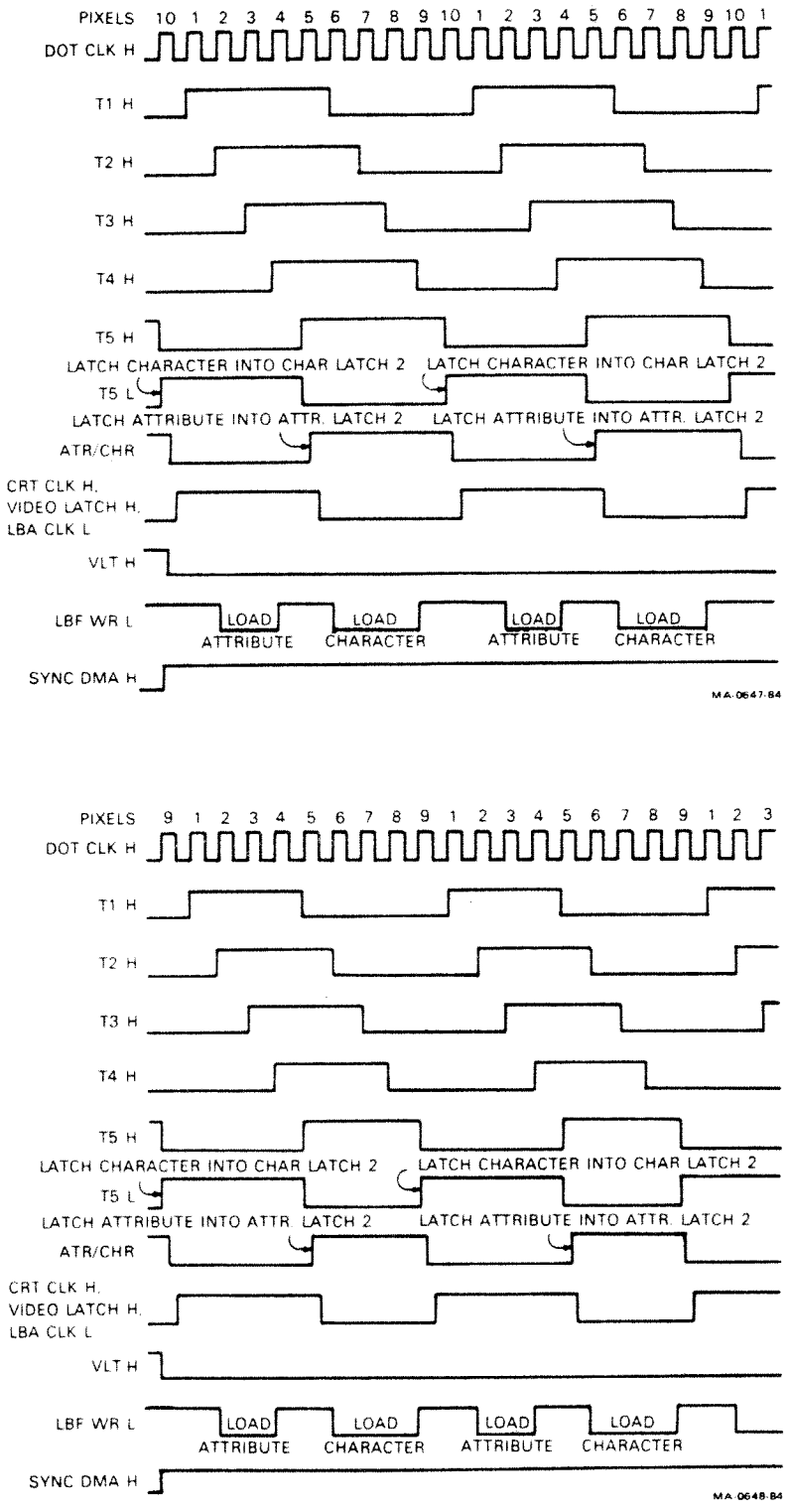
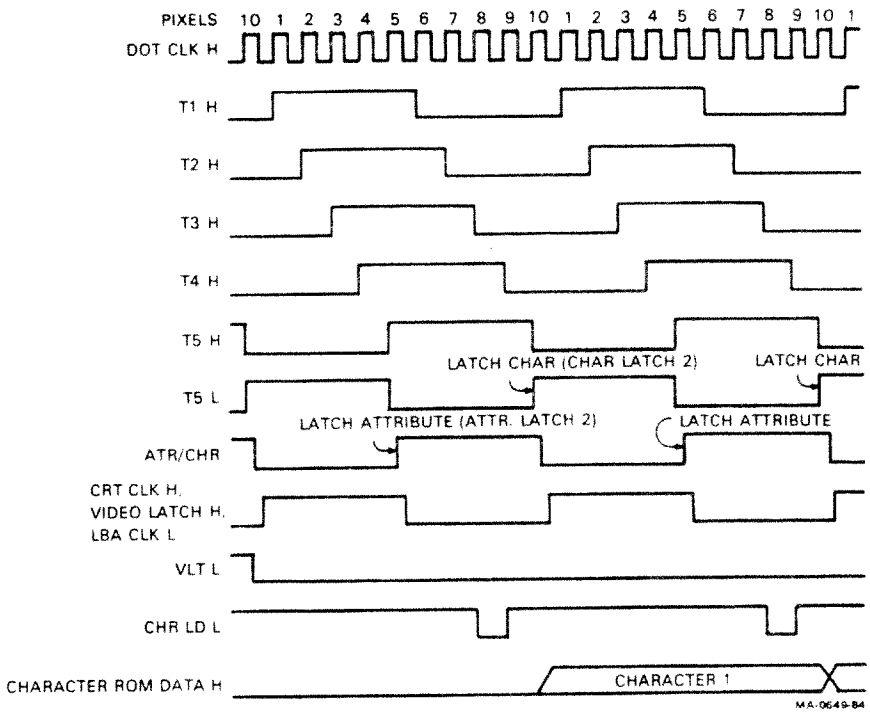


Figure 6-10 DMA and Visible Line Timing Diagram (Sheet 1 of 2)



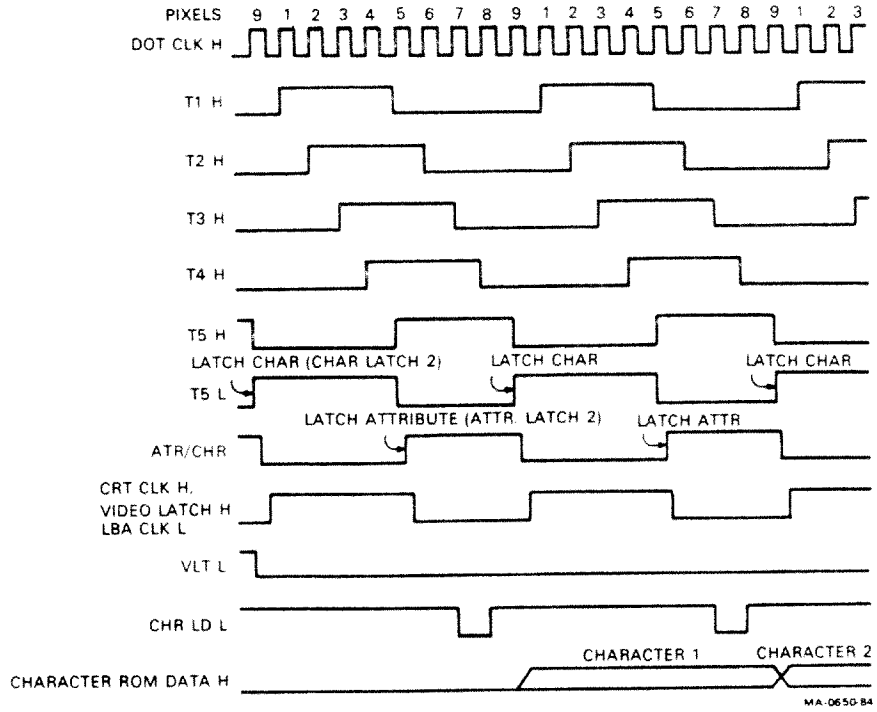


Figure 6-10 DMA and Visible Line Timing Diagram (Sheet 2 of 2)

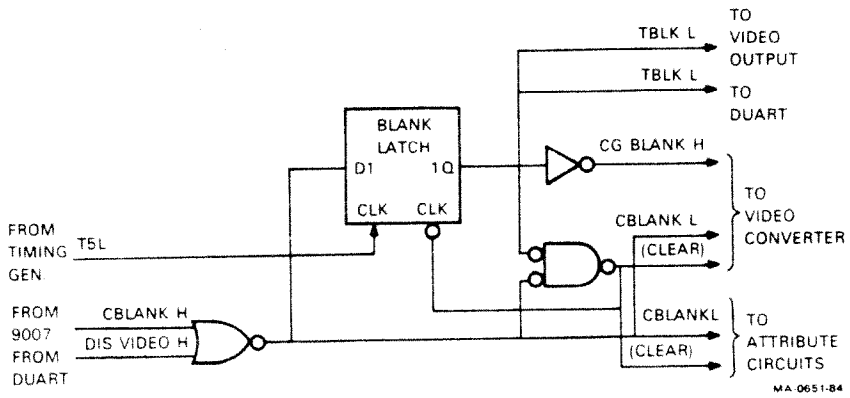


Figure 6-11 Blank Circuits Block Diagram

6.2.3 Blank Circuits

The blank circuits (Figure 6-11), generate blanking control signals in response to blank input from either the 9007 VPAC (CBLANK H) or the 2681 DUART (DIS VIDEO H). In addition, a clear signal is output to attribute and video output circuits to clear those circuits for new processing.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-11.

6.2.4 Character Generator

The character generator processes character dot matrix values to the video conversion circuit based on character address values stored in a line buffer during DMA transactions. This processing is done on a scan line to scan line basis for each row of screen data.

DMA transactions occur at the first scan line of each row of screen data. During DMA transactions, character address values from the screen RAM, and attribute values from the attribute RAM, are input to the character generator.

As each character address and associated attribute value is transferred into the character generator circuit, it is stored in a line buffer RAM. At the same time, character address data is also passed to a character ROM (or alternate character RAM) for output of the dot pattern associated with the first scan line of the character address being stored. The associated attribute value being stored in the line buffer is output from the character generator, at the same time as it is being stored, to provide for attributes affecting the dot pattern being output by the character ROM (or RAM).

This process repeats for all characters being DMA'ed into the line buffer RAM, until the first scan line for all characters in the screen row has been processed (DMA transaction completed). The remaining scan lines of the data row are processed by accessing the character address and attribute values stored in the line buffer RAM during the DMA activity. Once all the scan lines for the screen row have been processed, a new DMA transaction will be used to input the next screen row for display.

The character generator (Figure 6-12) consists of three main circuits.

- Access mux
- Line buffer
- Character (CHAR) output circuit

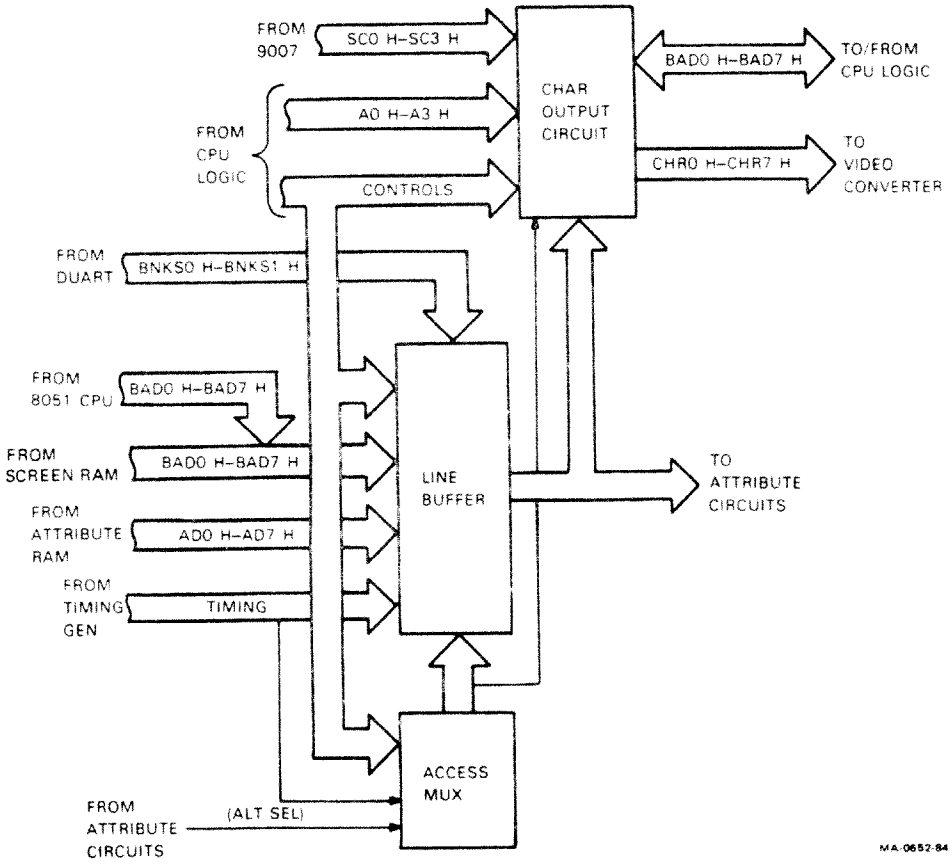


Figure 6-12 Character Generator Block Diagram

6.2.4.1 Access Mux -- The access mux (Figure 6-13) selects outputs based on select input (EN CHR GEN RW H) from the CPU logic. Video logic inputs when select is low and CPU logic inputs when select is high.

The video logic accesses character generator circuits to load character and attribute values during DMA transactions, and to process those values out. The CPU logic accesses the character generator to load alternative character formats into the character output circuit, or to read back previously loaded characters.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-13.

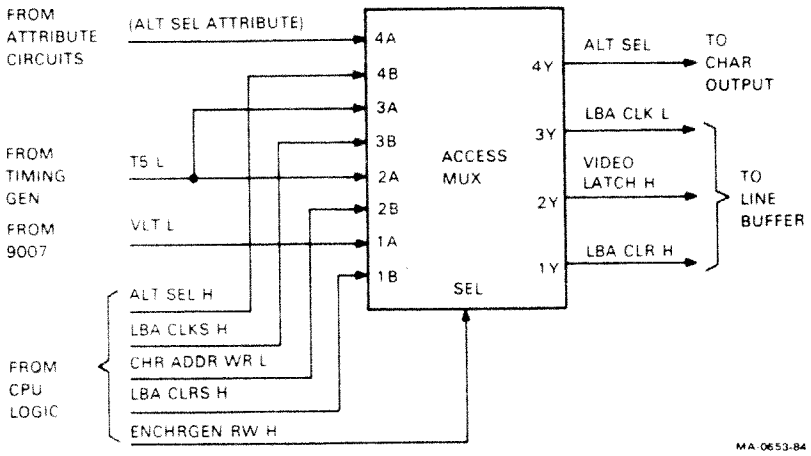


Figure 6-13 Access Mux Block Diagram

6.2.4.2 Line Buffer -- The line buffer circuit is used to store character address and attribute values during DMA transactions, and to process those character address and attribute values out to the character output (character address data) and attribute (attribute data) circuits.

The line buffer circuit (Figure 6-14) consists of the following components.

- Line buffer address counter -- is clocked by LBA CLKS L to generate a sequential address value to address buffer.
- Address buffer -- loads new address value on each T5 L time to provide sequentially incrementing address input to the line buffer RAM.

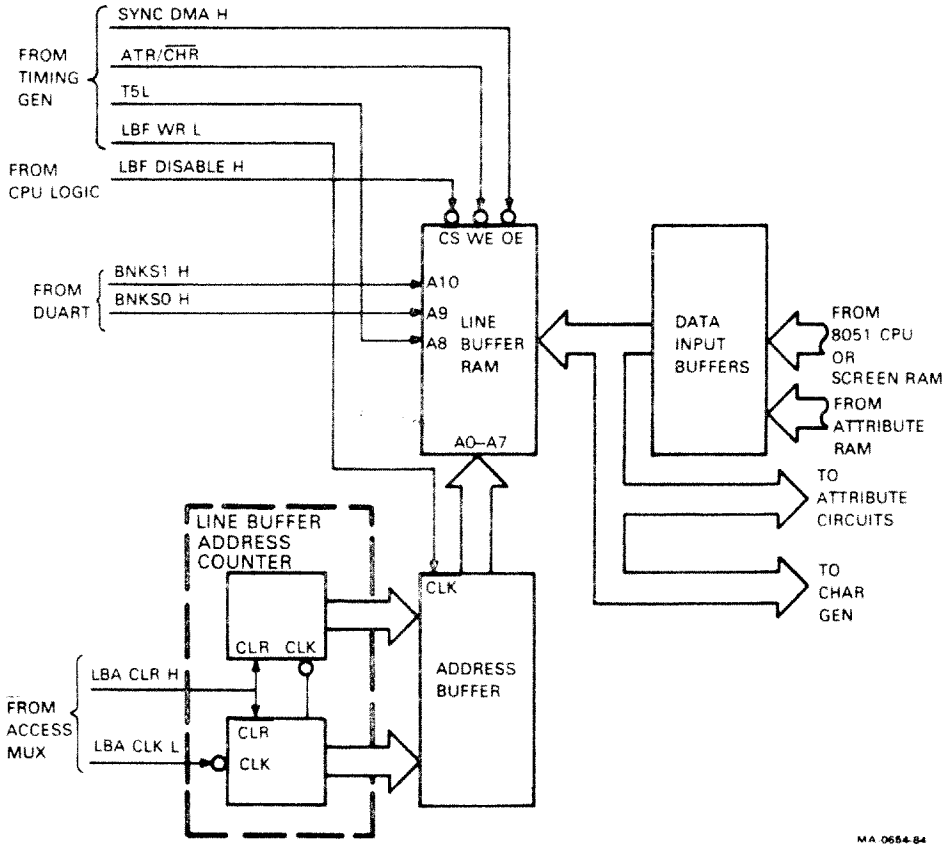


Figure 6-14 Line Buffer Block Diagram

- Line buffer RAM -- is a 2K X 8-bit wide RAM device that provides for storage and processing of the following character address data and attribute values:

  - A0-A7 inputs define the 8-bit position into which character address or attribute data will be loaded;

  - A8 input (ATR/CHR) defines character address data (ATR/CHR high) or attribute value (ATR/CHR low) is being loaded;

  - A9-A10 inputs define one of four banks of memory space, each bank containing 512 bytes of memory space for character address and attribute values (256 bytes for each).

Figure 6-14 also shows the data input buffers which consist of two latch devices.

- Attribute latch -- is used during DMA transactions to transfer attribute values to the line buffer RAM and to provide the attribute values to the attribute circuits for the first scan line of the screen row undergoing DMA.

- Character latch -- is used during DMA transactions to transfer character address data to the line buffer RAM and to provide the character address data to the character output circuit for the first scan line of the screen row undergoing DMA.

Loading character address and attribute values into the line buffer RAM is enabled by SYNC DMA H high, LBF WR L low, and LBF DISABLE H low. During read out of character address and attribute values, SYNC DMA H and LBF DISABLE H are both lows. LBF DISABLE H is only high when the CPU logic is accessing the alternate character generator in the character output circuit.

Figure 6-15 provides a memory map of the line buffer RAM. Figure 6-16 shows the attribute and character latches. Later in this chapter, Table 6-2 describes the signals shown in Figure 6-16.

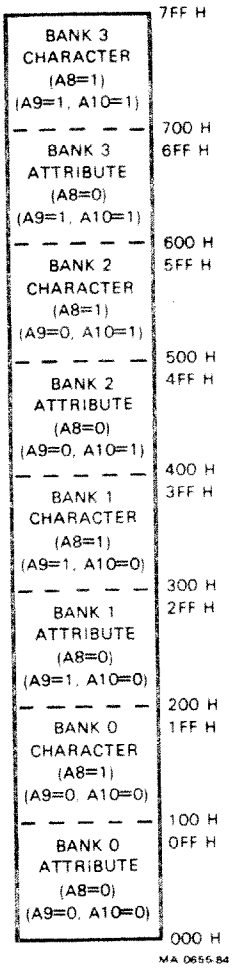


Figure 6-15 Line Buffer RAM Memory Map

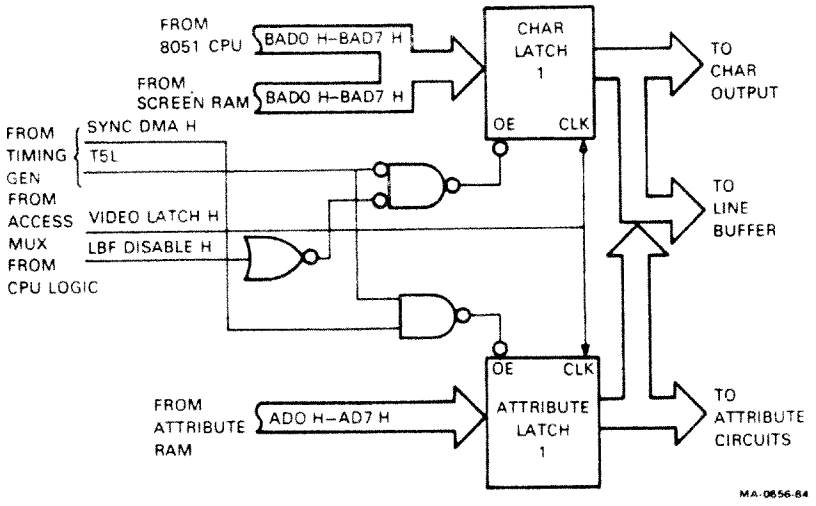


Figure 6-16 Data Input Buffers Block Diagram

6.2.4.3 Character Output Circuit -- The character output circuit generates the dot matrix character pattern used for the display. The character output circuit (Figure 6-17) consists of the following components.

- Character latch 2 -- provides address of character position being accessed by character latch 1 (for processing of the first scan line of a character address being transferred to the line buffer RAM during DMA transaction), line buffer RAM (during processing of second and subsequent scan lines of a stored screen row), or by the CPU logic (for read/write access of character generators).

- Address mux -- provides address of scan line of character being addressed by character latch 2 input, from either the 9007 VPAC input (during scan line processing), or from the CPU logic (during accessing the character generators).

- Read/write buffer -- provides for data transfer between the character generators (ROM and RAM) and the CPU logic.

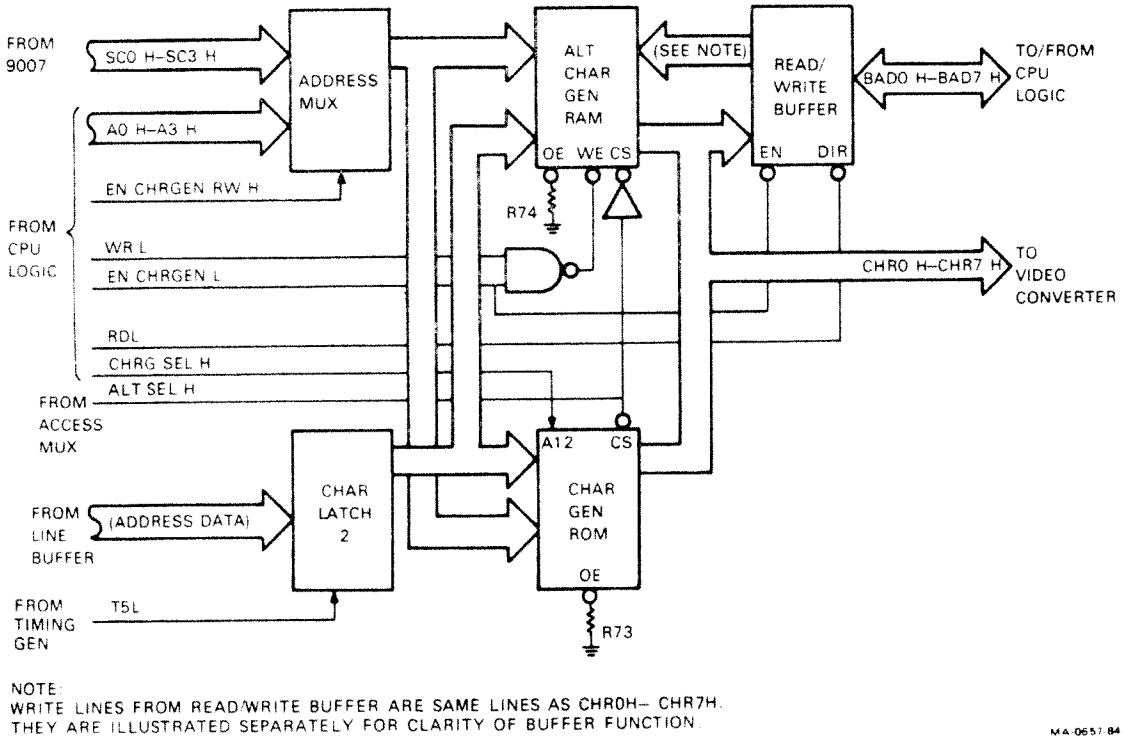


Figure 6-17 Character Output Circuits Block Diagram

- Alternate character generator RAM -- contains "soft" character set (down-line loadable characters), with font storage of up to 94 characters (each character consisting of 10 bytes of data, one byte for each scan line).

- Character generator ROM -- contains "hard" character set.

Which character generator is selected for character data output (CHR0 H-CHR7 H) is determined by the ALT SEL H signal from the access mux, with ALT SEL H developed either from CPU logic input (during CPU logic read/write access of alternate character generator) or from attribute circuits input developed from bit 5 of the attribute associated with the character to be processed.

Character latch 2 provides the base address for characters being accessed from either of the two character generators, while the address mux provides the scan line address.

The character ROM contains two identical pages of character format data, with each page containing 256 rows of data, each data row 16 bits wide (which page is to be accessed is defined by CHARG SEL H input).

Figure 6-18 provides a general map of the character ROM. As shown in this figure, 288 characters are packed into each page of 256 data rows: 256 characters, packed one per data row, and 32

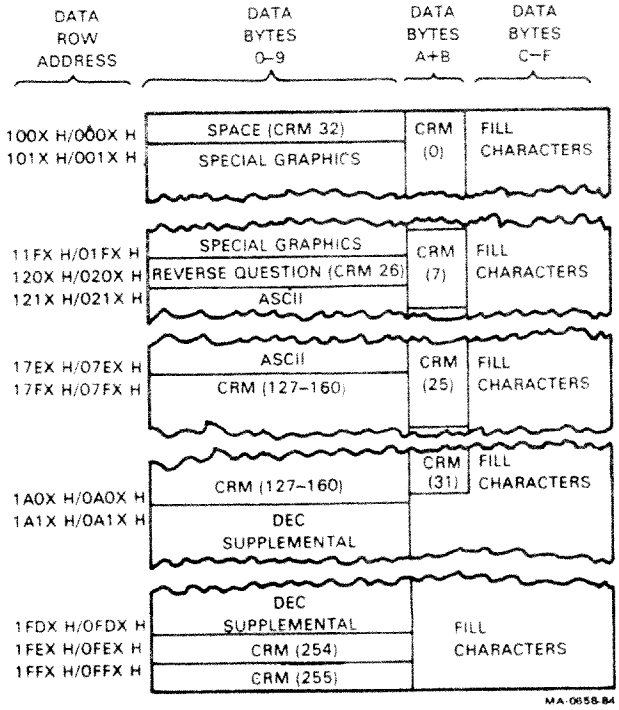


Figure 6-18 Character ROM Map: Overview

characters (CRMØ-CRM31) packed one character per each 5 data rows (ROM space not taken up by character font data is filled with FFH data).

Figure 6-19 shows that each of the 256 characters packed one character per data row consist of 1Ø bytes of data, one byte for each scan line of the character. When addressing one of these characters, a single base address is provided to the character ROM by character latch 2, and each of the 1Ø scan lines is addressed by the address mux input.

However, addressing the remaining 32 characters (CRMØ-CRM31) requires a separate base address input from character latch 2 for every two scan lines of the character to be processed. Figure 6-2Ø shows that each of the 32 characters packed into five different data rows consist of 1Ø bytes of data, one byte for each scan line, but only two bytes per data row.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-17.

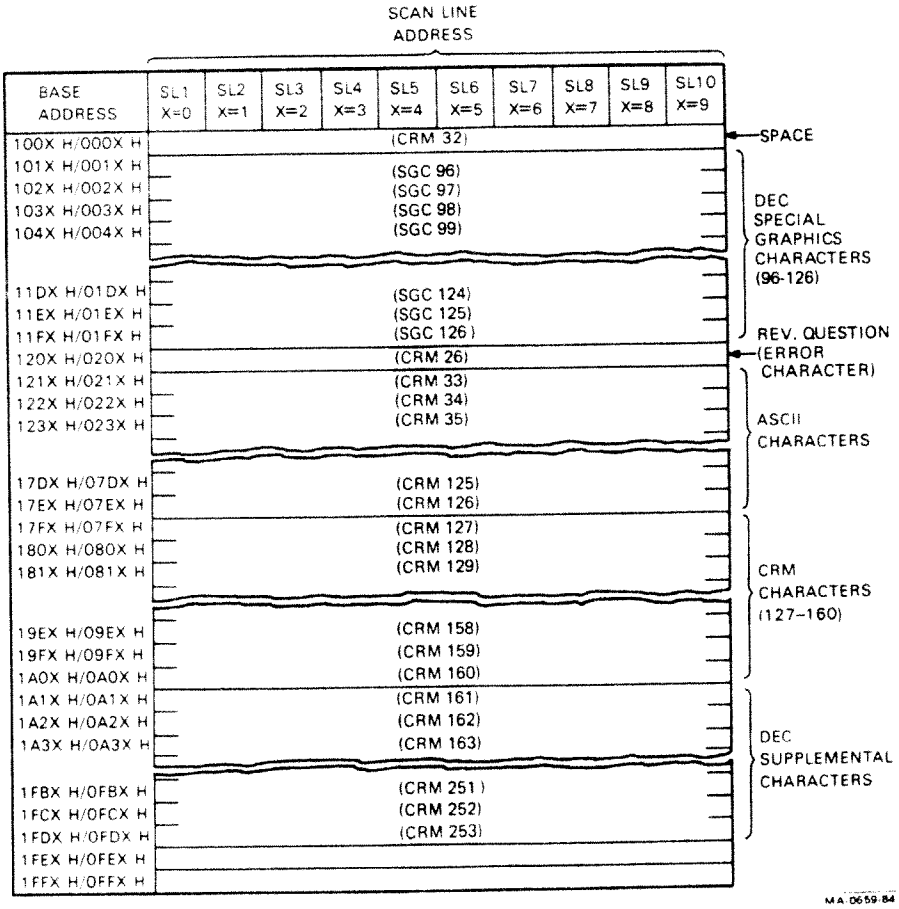


Figure 6-19 Character ROM Map: CRM32-255 and Special Graphics

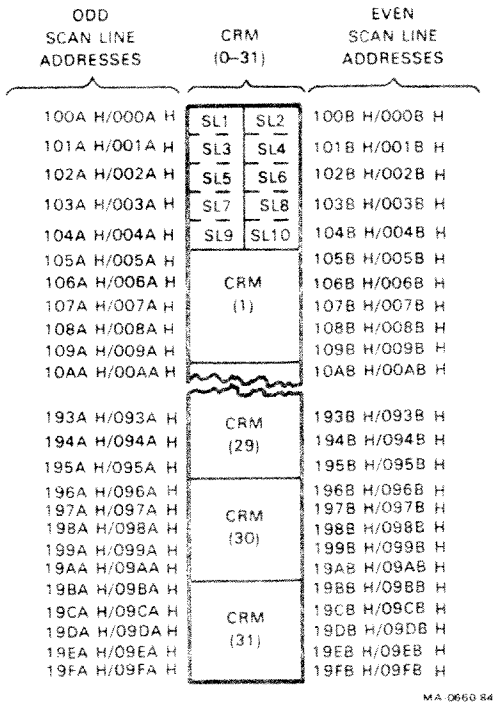


Figure 6-20 Character ROM Map: CRM0-31

6.2.5 Attribute Circuits

The attribute circuits output the attribute control values to be considered in processing each character for display. As each scan line of a character is output from the character generator, attributes associated with that character, as loaded into the attribute circuits by the line buffer RAM in the character generator, are output to video output and video converter circuits.

The attribute circuits (Figure 6-21) consist of the following components.

- Attribute latch 2 -- latches character generator input at ATR/CHR going high to provide attribute value for the next character to be processed to attribute latch 3 for loading.

- Attribute latch 3 -- loads attribute value from attribute latch 2 on leading edge of T5 L (blink attribute input is enabled or disabled by being gated with BLINK H input from 2681 DUART).

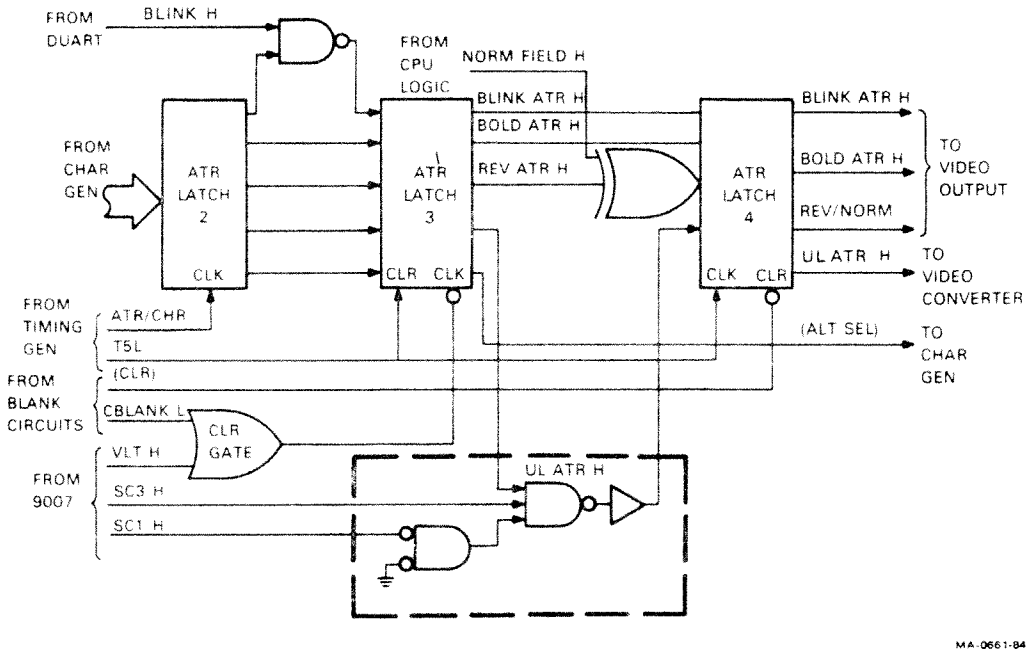


Figure 6-21 Attribute Circuits Block Diagram

- CLR gate -- clears value stored in attribute latch 3 whenever the screen is being blanked (CBLANK L) and active line time (VLT H) is not occuring.

- UL ATR gates -- gates underline attribute with scan line address values input from the 9007 VPAC to define an underline output only during the ninth and tenth scan lines of the character being processed.

- Attribute latch 4 -- is the output stage of attribute circuits, clocked on leading edge of T5 L to latch inputs provided by attribute latch 3 and UL ATR gates, with the reverse attribute input from attribute latch 3 exclusive ORed with NORM FIELD H control input from the CPU logic.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-21.

6.2.6 Video Converter

The video converter transforms parallel character dot matrix data input from the character generator into serial data output to the video output circuit. The video converter (Figure 6-22) consists of the following circuits.

- Conversion control
- Parallel-to-serial (P/S) converter

6.2.6.1 Conversion Control -- The conversion control circuit controls loading of parallel character dot matrix data into the P/S converter. The conversion control circuit (Figure 6-23) consists of the following components.

- INH latch -- is latched at T5 L time, with output alternately enabling and disabling the INH gate.
- Cursor skew F/F -- is set by CURS H during horizontal retrace time, when double width row is to be processed, with high output partially enabling INH gate and set input to INH F/F.
- INH gate -- is used during processing of double width rows to jamset the load F/F, preventing load of a new character until each bit of the current character is processed twice.
- INH F/F -- is used during processing of double width rows to inhibit shift activity at the P/S converter so that each bit of data input from the character generator requires two dot clocks to process instead of one.
- Load F/F -- defines a shift condition (CHR LD L high) or load condition (CHR LD L low) to the P/S converter.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-23.

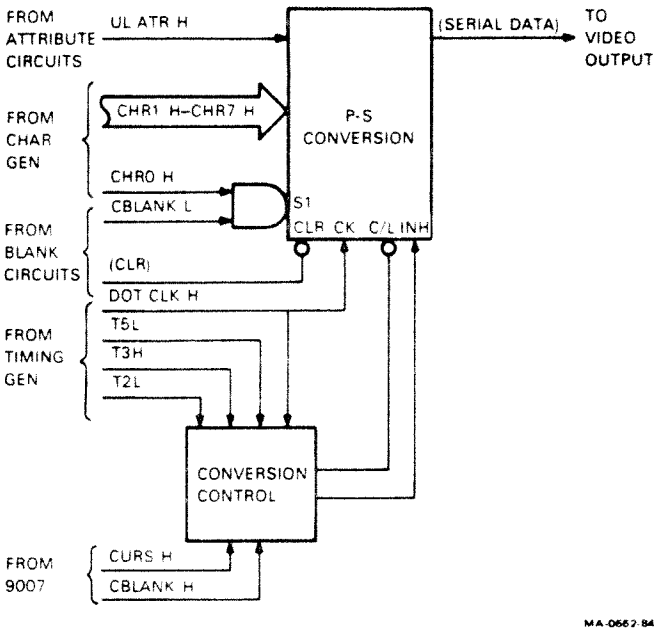


Figure 6-22 Video Converter Block Diagram

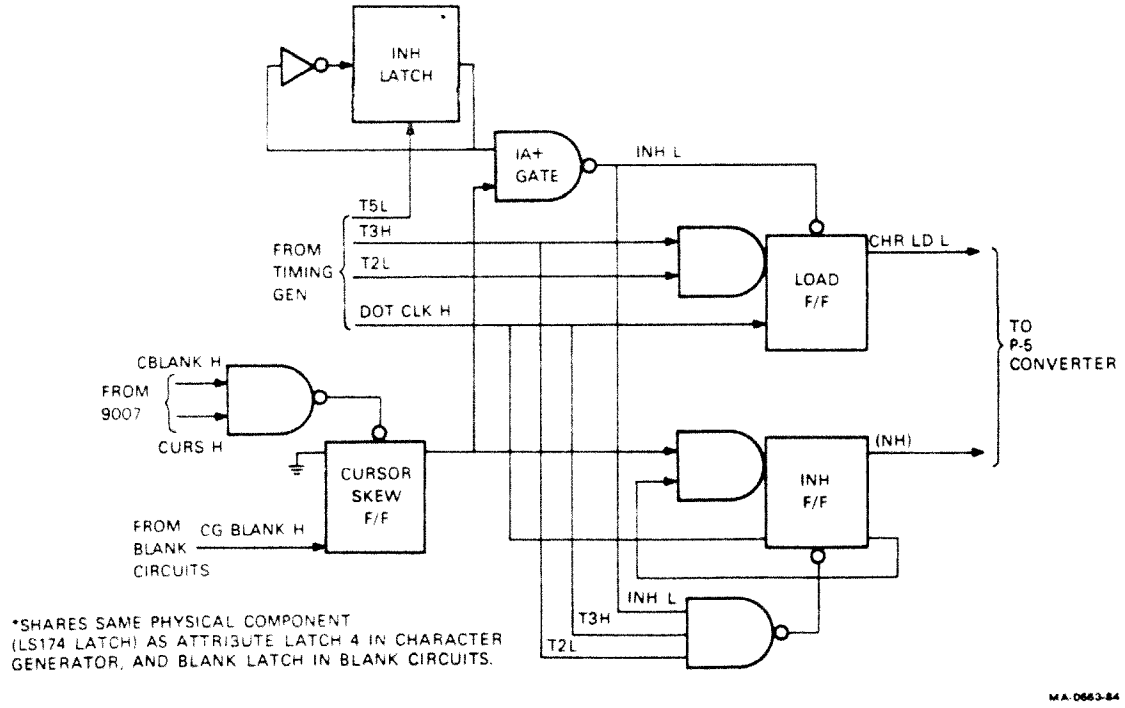


Figure 6-23 Conversion Control Block Diagram

6.2.6.2 Parallel-to-Serial (P/S) Converter -- The P/S converter performs the actual parallel-to-serial conversion of dot matrix data, and in the process performs dot stretching. It converts single "on" dots into two adjacent "on" dots (and, due to construction of the dot stretching circuit, converts the last "on" dot of a sequence into two dots as well).

Dot stretching (Figure 6-24) occurs only on the horizontal plane, and does not increase the number of dots in the vertical plane of a character matrix. It also does not increase the size of the horizontal plane of a character matrix. Dot stretching simply compensates for monitor risetime being too slow to reach maximum brightness for single "on" dots. Figure 6-25 shows that stretching each "on" bit increases the amount of time allowed for the monitor to respond, allowing brightness to achieve its maximum.

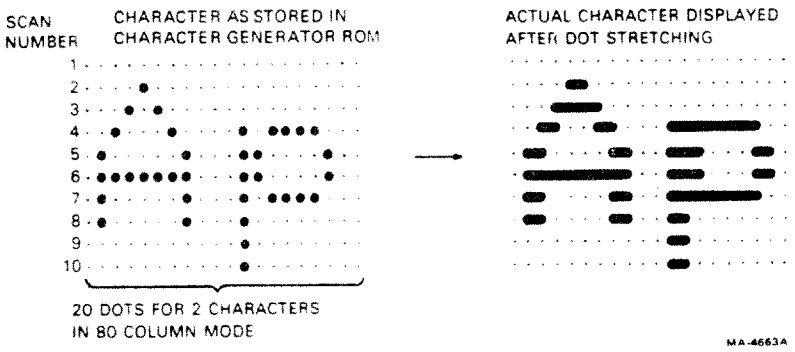


Figure 6-24 Dot Matrix Display and Dot Stretching

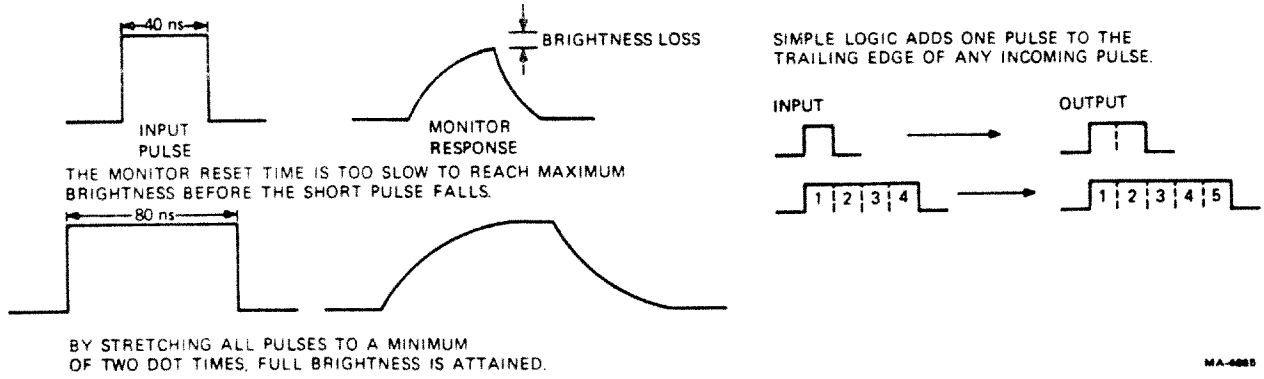


Figure 6-25 Effects of Dot Stretching

The P/S converter (Figure 6-26) circuit consists of the following components.

- Shift register -- loads parallel data on CHR LD L low,and serially shifts data through on each DOT CLK H input, when INH input is low. It also outputs shifted data to serial latch.

- SIN latch -- initiates serial shifting by loading bit Ø of the parallel dot matrix data into the serial input of the P/S converter.

- Serial latch -- performs dot stretching by feeding back the output developed from the shift register input to add a high output to the gate at the trailing edge of each high input (either for a single high input from the shift register, or at the end of a series of high inputs).

The outputs from the serial latch are gated with the underline attribute (UL ATR H) to provide all high output to video output circuit during processing of the ninth scan line of a data row when underline attribute is selected.

Later in this chapter, Table 6-2 describes the signals shown in Figure 6-26.

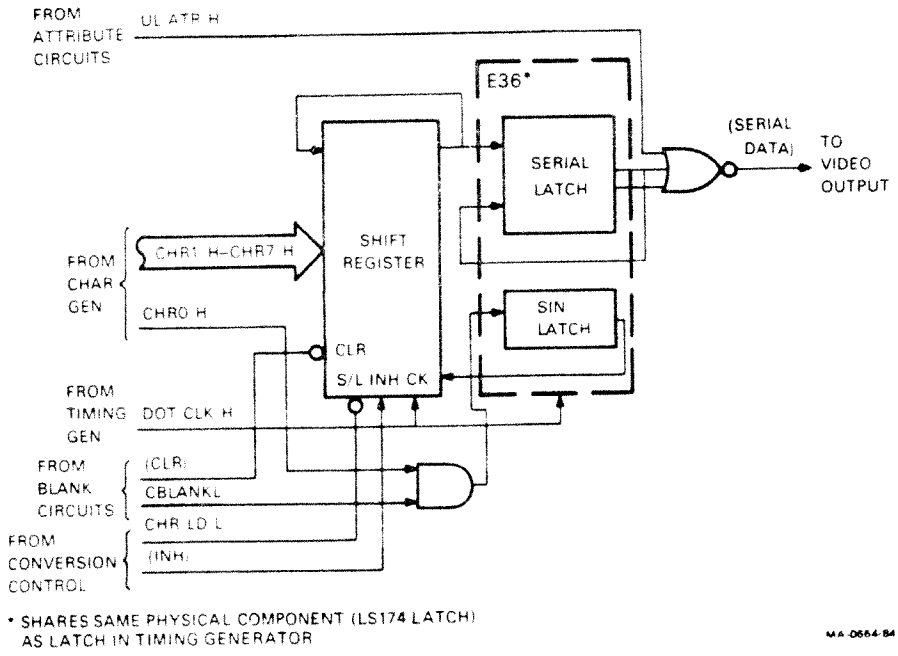


Figure 6-26 P-S Conversion Block Diagram

6.2.7 Video Output

The video output circuit converts serial data input from the video converter into video outputs to the monitor circuits and an optional monitor device.

The video output circuit (Figure 6-27) consists of the following components/circuits.

- Data gate -- is an exclusive OR's serial input from video converter with REV/NORM condition from attribute logic to generate a high output (bit "on" condition) when REV/NORM is low.

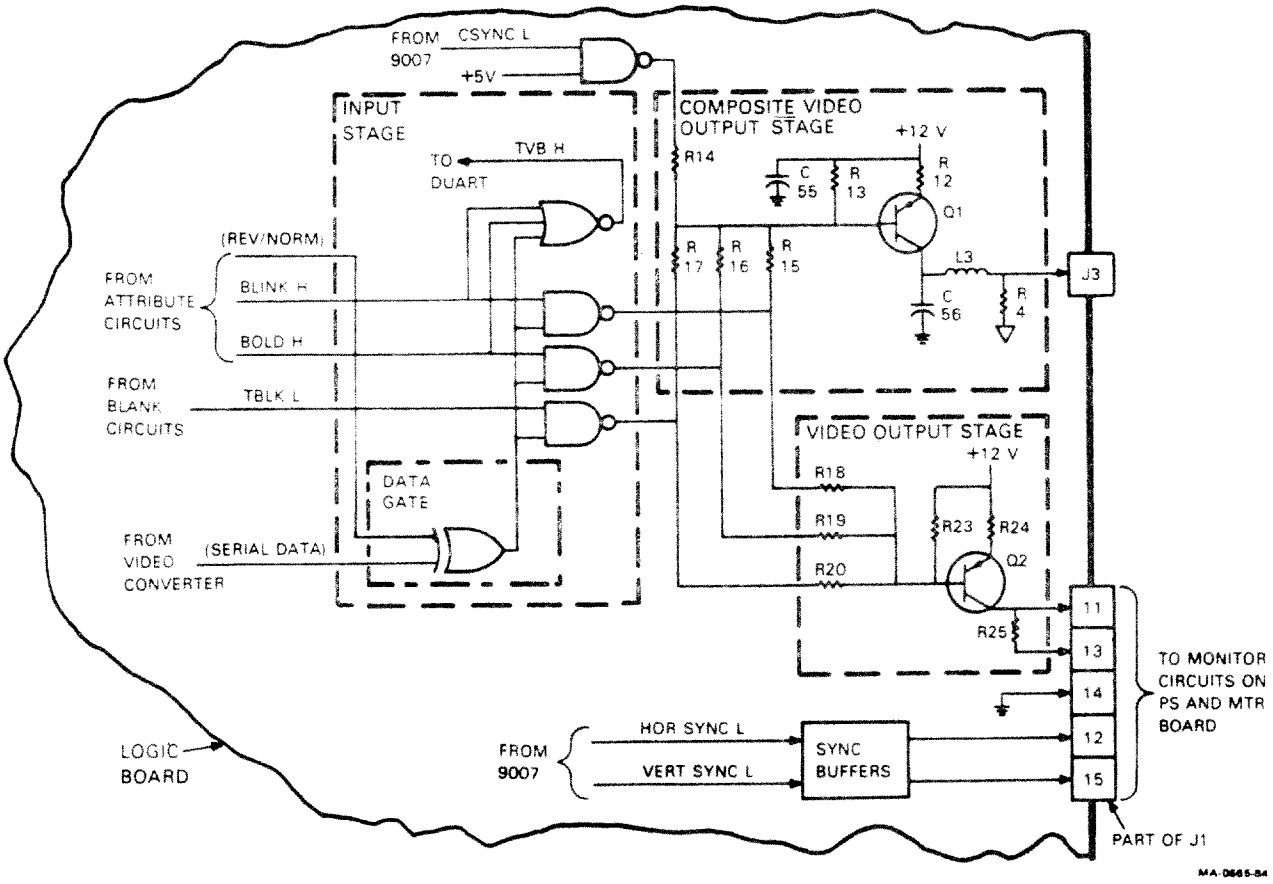


Figure 6-27 Video Output Block Diagram

- Input stage -- gates data gate value with blink, bold, and blank attribute inputs to provide biasing to composite video output and video output stages.

- Composite video output stage -- develops a composite video output to be used by an optional monitor device connected to J3 from input stage biasing and composite sync (C SYNC L) inputs.

- Video output stage -- develops video output to monitor circuits from input stage biasing inputs.

- Sync buffers -- buffer sync outputs to monitor circuits.

- J1 -- provides interconnection between logic board and PS and monitor board.

NOTE

A complete pin-out for J1 is provided in the system communication logic description presented in Chapter 5 (Figure 5-9).

Descriptions of the signals shown in Figure 6-27 follow in Table 6-2.

6.3 SIGNAL DESCRIPTIONS

Table 6-2 provides descriptions of all the signal identifed in this chapter. These descriptions are provided for reference, and are listed alphabetically by mnemonic, with numeric mnemonics listed last.

Table 6-2 Video Logic Signal Descriptions

Mnemonic	Signal	Description
A0--A3 H	Address bits 0-3 high	Input to address mux in character generator from CPU logic defining scan line of alternate character generator RAM to be accessed for read (RD L) or write (WR L) transaction
A0--A5 H	Address bits 0-5 high	Input to 9007 VPAC from CPU logic defining internal register to be accessed (SEL CRT L) for read or write transaction (type of transaction defined by address)
A0--A13 H	Address bits 0-13 high	Address outputs from 9007 VPAC during DMA transactions defining CPU logic RAM and attribute RAM addresses to be accessed for read of character and attribute data
AD0--AD7 H	Address/data bits 0-7 high	Data bus lines used to transfer attribute data from attribute RAM to character generator during DMA transactions
ALT SEL H	Alternate select high	Select signal to character generator ROM (ALT SEL H low) and alternate character generator RAM (ALT SEL H high) developed by character generator access mux from either CPU logic input (when CPU is accessing alternate character generator RAM), or from input defined by attribute of character being processed for output

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
ATR/CHR	Attribute/character	Timing generator output controlling transfer of attribute (ATR/CHR low) and character address values (ATR/CHR high) into line buffer RAM (during DMA transactions) or out of line Buffer RAM to attribute latch 2 and character latch 2 (during active line time)
BAD0--BAD7 H	Buffered data bits 0-7 high	Data bus used by CPU logic to transfer data to and from 9007 VPAC, or to and from the alternate character generator RAM, and by video logic to transfer character address data from the CPU logic RAM to the character generator circuit
BLINK H	Blink high	DUART signal which produces blink rate at screen; BLINK H is gated with blink attribute (BLINK ATR H) at attribute circuits with BLINK H high for blink off at screen and low for blink on
BLINK ATR H	Blink attribute high	Enables blinking display at screen through biasing of video output stage circuit (intensity of video output increased for BLINK ATR H high and decreased for BLINK ATR H low)

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
BNKSØ--BNKS1 H	Bank select Ø-1 high	DUART signals defining the two most significant bits of line buffer RAM address
BOLD H	Bold high	Enables bold display at screen through biasing of video output stage circuit (intensity of video output increased for BOLD ATR H high and decreased for BOLD ATR H low)
CBLANK H	Composite blank high	CRT controller output defining screen blanking during vertical and horizontal retrace periods
CBLANK L	Composite blank low	Control defining screen blanking developed from either CBLANK H, during retrace periods, or from DIS VIDEO H, during self-test
CGBLANK H	Composite gated blank high	Gated from CBLANK L and used as clock to cursor skew F/F in video output circuit to reset double width control at start of each horizontal and vertical retrace period
CHRØ--CHR7 H	Character bits Ø-7 high	Parallel dot matrix data output from character generator to video converter defining dot pattern of display characters on a scan line-to-scan-line basis

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
CHR ADDR WR L	Character address write low	Input to access mux in character generator used to develop VIDEO LATCH H when CPU is supplying address value to character generator to be used to access alternate character generator RAM for read/write transaction
CHR LD L	Character load low	Input to P/S converter enabling load of parallel character dot matrix data (CHRØ-CHR7 H)
CHRG SEL H	Character generator select high	Input to character generator ROM providing MSB of address, with bit defining which character set is to accessed during character processing for screen display (ASCII or DEC multinational)
(CLEAR)	(Clear)	Output from blank circuit (developed from CBLANK L) to clear input of P/S converter and attribute latch 4 at start of each retrace period
CRT CLK H	CRT clock high	Timing generator clock output to CRT controller generated at T5 time
CSYNC L	Composite sync low	CRT controller output to video output circuit to be gated with video data to define vertical and horizontal sync for composite video output to optional slave monitor

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
CURS H	Cursor high	CRT controller output used during horizontal retrace periods to define a double width data row to be processed
DIS VIDEO H	Disable video high	DUART signal used to generate blanking signals during self-test
DMA H	DMA high	Acknowledgement from CPU relinquishing control of AD0-7 H and BAD0-7 H data bus lines to the CRT controller for access of screen character address and attribute values
DMA REQ L	DMA request low	Interrupt to CPU from CRT controller requesting CPU give up data buses for video logic access of screen character address and attribute values
DOT CLK H	Dot clock high	Timing generator signal providing basic timing for video logic with one active clock for each dot of screen display
EN CHR GEN RW H	Enable character generator read/write high	CPU logic signal to access mux character generator selecting for CPU logic inputs during CPU access of character genenerator
EN CHR GEN L	Enable character generator low	CPU logic signal to alternate character generator RAM and read/write buffer in character generator enabling CPU access for read/write transactions

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
HOR SYNC L	Horizontal sync low	CRT controller output defining horizontal sync time
INH L	Inhibit low	Control within video converter conversion control circuit which prevents serial shifting of dot matrix display data during double width row processing
LBA CLK L	Line buffer address clock low	Clock input to line buffer address counter developed from either LBA CLKS L (from CPU logic) or T5 L (from timing generator) by character generator access mux
LBA CLKS H	Line buffer address clocks high	Clock input from CPU logic to character generator access mux used to develop LBA CLK L during CPU access of character generator
LBA CLR L	Line buffer address clear low	Clear input to line buffer address counter developed from either LBA CLRS L (from CPU logic) or VLT L (from CRT controller) by character generator access mux
LBA CLRS H	Line buffer address clears high	Clear input from CPU logic to character generator access mux used to develop LBA CLR L during CPU access of character generator

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
LBF DISABLE H	Line buffer disable high	Control input to character generator enabling character address values being presented to character generator to be passed to alternate character generator RAM without being inadvertently written to line buffer RAM
LBF WR L	Line buffer write low	Timing generator output enabling write of character address and attribute values into line buffer RAM during DMA transactions
NORM FIELD H	Normal field high	Control input from CPU logic defining dark screen background
RD L	Read low	CPU logic input to character generator read/write buffer defining direction of data transfer between CPU and alternate character generator RAM
RESET CRT L	Reset CRT controller low	CPU logic signal resetting CRT controller to known start state
RESET TIM L	Reset timing generator low	CPU logic signal resetting timing generator to known start state
REV ATTR H	Reverse attribute bit high	Defines reverse display at screen for character being processed (character dot matrix "on" dots at same value as screen background)

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
(REV/NORM)	(Reverse/normal)	NORM FIELD H and REV ATTR H exclusive ORed and gated with SERIAL DATA L for display "on" for "on" dots (REV/NORM high) when NORM FIELD H/REV ATTR H are opposing states (reverse on light screen or normal on dark), or for display "on" for "off" dots (REV/NORM low) when NORM FIELD H/REV ATTR H are identical states (reverse on dark screen or normal on light)
SC0-SC3 H	Scan address bits 0-3 high	Address inputs to character generator address mux from CRT controller defining scan line of character to be processed from either character generator ROM or alternate character generator RAM
SEL ATR0 L	Select attribute RAM 0 low	Enable to attribute RAM 0 when CPU logic is accessing the RAM for a write, or when being accessed for DMA transaction
SEL ATR1 L	Select attribute RAM 1 low	Enable to attribute RAM 1 when CPU logic is accessing the RAM for a write, or when being accessed for DMA transaction
SEL CRT L	Select CRT controller low	Enable to CRT controller when CPU is accessing this device for read/write transaction

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
(SERIAL DATA L)	(Serial data stream low)	Bit stretched serial dot matrix data output from P/S converter to video output defining "on" and"off" bits of display
SYNC DMA H	Synchronized DMA high	Timing generator output developed from DMA H synchronized to ATR/CHR time
T1-T5 H,T2 L T3 L, T5 L	Timing signals 1-5 high, 2-3 and 5 low	Timing generator clocking signals outputs to video logic circuits
TBLK L	Test blank low	Blank control to video output circuit developed from CBLANK L (CBLANK L low for either retrace periods, from CBLANK H, or during self-test, from DIS VIDEO H), and preventing video output from turning display on
TVB H	Test video bits high	Status output to DUART from video output circuit used during self-test to sample condition of video data stream
UL ATR H	Underline attribute high	Enables generation of underline at display by being gated with SERIAL DATA L to turn all dots "on" during ninth and tenth scan lines of a processed character
VERT SYNC L	Vertical sync low	CRT controller output defining vertical sync time

Table 6-2 Video Logic Signal Descriptions (Cont)

Mnemonic	Signal	Description
VIDEO LATCH H	Video latch high	Character generator access mux output enabling either CPU access of alternate character generator RAM (VIDEO LATCH H developed from CHR ADDR L) or video logic transfer of character address and attribute values to line buffer RAM (VIDEO LATCH H developed from T5 L)
VLT H/L	Visible line time high low	Control outputs from CRT controller defining screen data processing time (horizontal trace periods)
WR L	Write low	CPU logic input to alternate character generator RAM enabling CPU access for write transaction when that device is selected (EN CHRGEN L)
132 COL H	132 column high	Control input to timing generator from DUART defining number of characters per screen data row

6.4 SCHEMATIC REFERENCE INFORMATION

Table 6-3 identifies the logic board component coordinates and schematic page and coordinate for each of the video logic components and circuits identified in this chapter.

NOTE
The reference information provided in Table 6-3 is based Rev. A of the logic board schematics (CS 5415653-Ø-1).

Table 6-3 Video Logic Schematic References

Circuit/ Component	Board Ref. No.'s	Schematic Page	Loc.
ACCESS MUX	E30	4	B3
ADDRESS BUFFER	E8	4	D6
ADDRESS MUX	E25	4	D4
ALT CHAR GEN RAM	E12,E22,E24,R74	4	D4/C3/B3
ATR/CHAR GATE	E46,R62	3	B4
ATTRIBUTE RAM	E5,E6	1	C3-C2
ATTRIBUTE LATCH 1	E21,E38	4	B7
ATTRIBUTE LATCH 2	E29	4	B6
ATTRIBUTE LATCH 3	E28,E38	4	B4
ATTRIBUTE LATCH 4	E50,E46	5	D7/D6
BLANK CIRCUITS	E22,E39,E44,E50	5	C8-C5
CHAR GEN ROM	E13,R73	4	C3
CHAR LATCH 1	E19,E22,E39	4	C7/A4
CHAR LATCH 2	E20	4	C4
CLR GATE	E22	4	A4
COMPOSITE VIDEO OUTPUT STAGE	E49,C55,C56,L3,Q1, R4,R12-R17	5	D3-D1
CRT 9007 VPAC	E16,E24,R57,R58	2	B2-C2
CRT CLK GATE	E34,R75,R6	3	B3
CURSOR SKEW F/F	E32,E38	5	B8
DATA GATE	E46	5	D4
DOT CLOCK GENERATOR	E24,E34,R60,Y3,Y4	3	B6-B4
INH F/F	E35,E37	5	A6/A7
INH GATE	E37	5	B7
INH LATCH	E50	5	C6
INPUT STAGE	E45,E49	5	D4-C4
J1	J1	5	C1-A1
J3	J3	5	C1
LBF WR GATES	E42	3	D6
LINE BUF ADDRESS COUNTER	E7	4	D7-C7
LINE BUFFER RAM	E14	4	D5
LOAD F/F	E35,E41	5	B7/B6
P/S CONVERTER	E27	5	B5
READ/WRITE BUFFER	E18	4	D2
SERIAL LATCH	E36,E45	5	B4-B3
SIN LATCH	E36,E41	5	B5/B4
SYNC BUFFERS	E44,E48,R9,R10	5	B3
SYNC DMA LATCH	E29	4	B6
T1 GATES	E42	3	C6
T5 H LATCH	E43	3	C4
T5 L LATCH	E36,E44	5	B4
UL ATR GATES	E37,E44,E45	5	C8-C7
VIDEO OUTPUT STAGE	Q2,R18-R20,R23-R25	5	C3-C2

CHAPTER 7
KEYBOARD (LK201)

7.1 INTRODUCTION

The LK201 keyboard module (shaded area in Figure 7-1) is the user's interface to the terminal. The keyboard detects keystrokes, encodes them, and transmits and receives information to and from the CPU logic in the system box.

Communication between the keyboard and the CPU logic is full-duplex, serial, and asynchronous at 4800 bits per second (bps). The communication lines conform to EIA standard RS-423, which applies to imbalanced voltage interfaces.

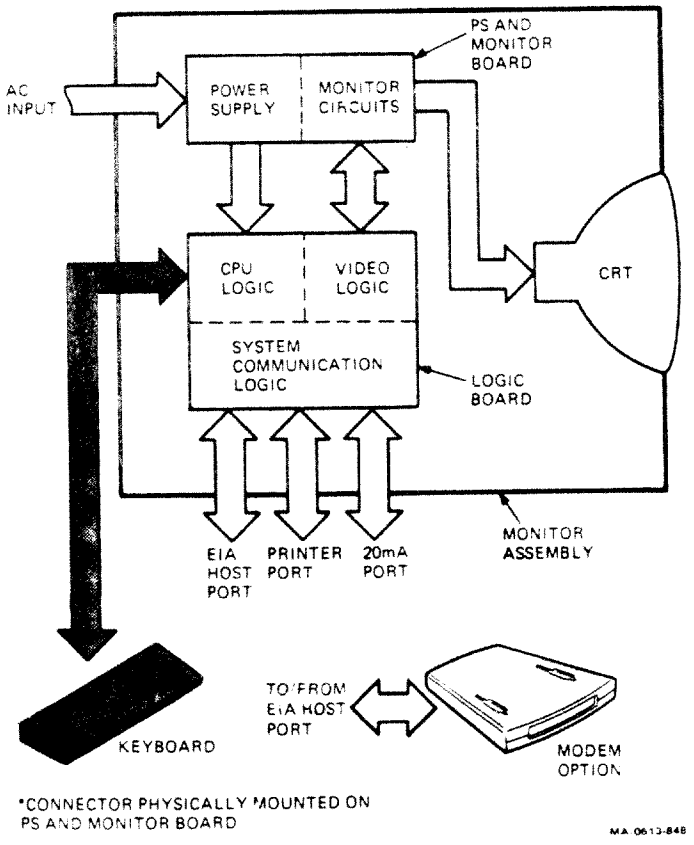


Figure 7-1 VT220 Series Terminal Functional Block Diagram

7.2 PHYSICAL DESCRIPTION

The VT240 Series terminal keyboard (Figure 7-2) has 105 keys arranged in the following four groups.

- Main keypad (57 keys)
- Numeric keypad (18 keys)
- Special function keypad (20 keys)
- Editing keypad (10 keys)

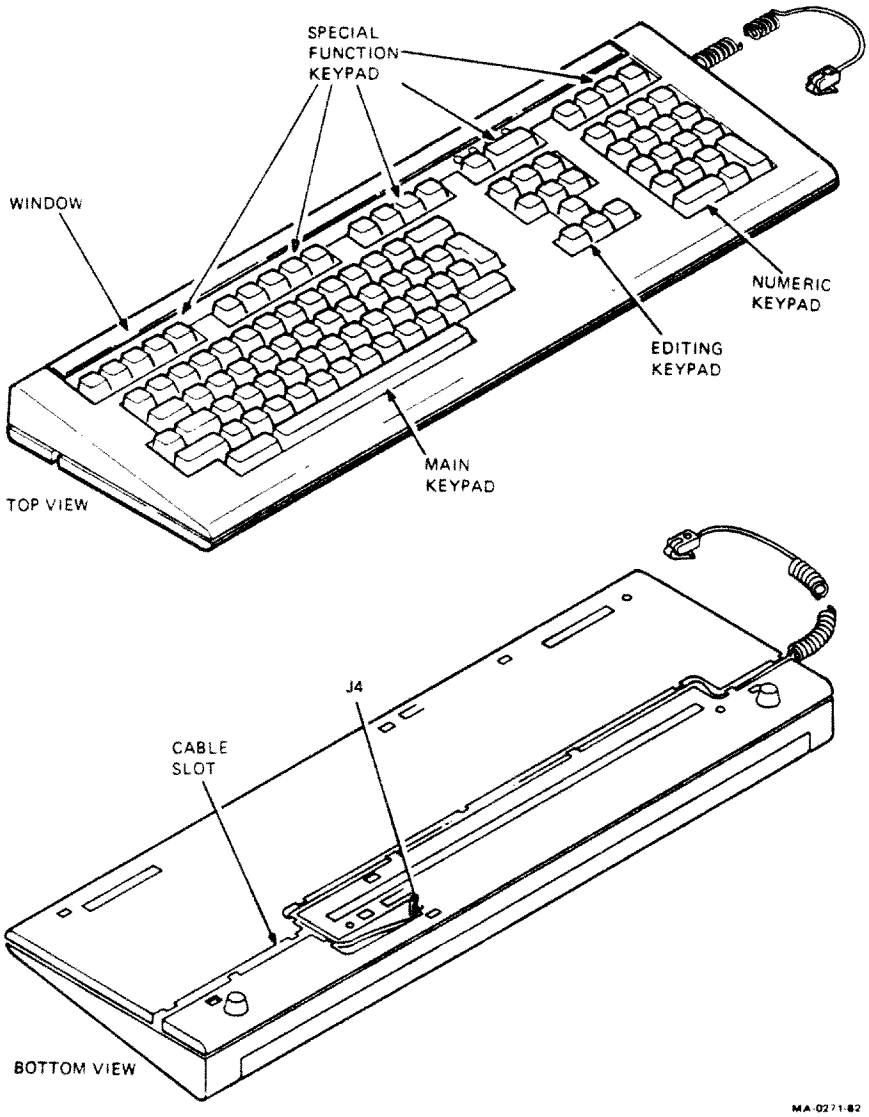


Figure 7-2 LK201 Keyboard

You can install the keycaps manually, but you need a special tool to remove them.

The keyboard circuitry is contained in a low profile cabinet that has a 30 mm nominal height from table top to home row. The keyboard case is made of two plastic shells that you can separate with a screwdriver. Nonslip plastic strips along the bottom prevent the keyboard from sliding on a table top. You can manually insert two feet in holes to raise the back edge of the keyboard.

You can lift a plastic window along the top edge above the special function keys to insert a user function label. The label, a thin paper strip, fits into the indented space and varies according to the application program.

A coiled cable (PN BCC01), with a 4-pin modular connector on each end, connects the keyboard to the video monitor. The keyboard transmits four signals to the monitor, which pass unchanged to the system box via the video cable (Figure 7-3). The four signals are as follows.

- +12 V power to keyboard
- Ground to keyboard
- Serial out (transmit line from keyboard)
- Serial in (receive line to keyboard)

You can place the cable in a channel in the bottom case and the modular type telephone connector fits into jack J4. You can insert the cable in the channel on either side of the keyboard. Section 7.6 provides keyboard specifications.

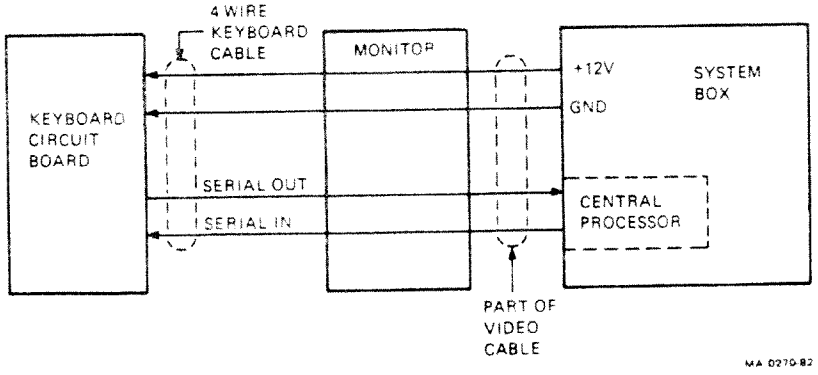


Figure 7-3 Keyboard Cable Connections

7.3 FUNCTIONAL DESCRIPTION

This section provides a functional description of the LK201 keyboard.

7.3.1 Keyboard Operation Overview

Figure 7-4 is a simplified block diagram of the keyboard circuitry. Everything except the block marked KEYBOARD SWITCH MATRIX is on the printed circuit board. This block represents the connections between the keyboard switches and the signals from the 8051 microprocessor.

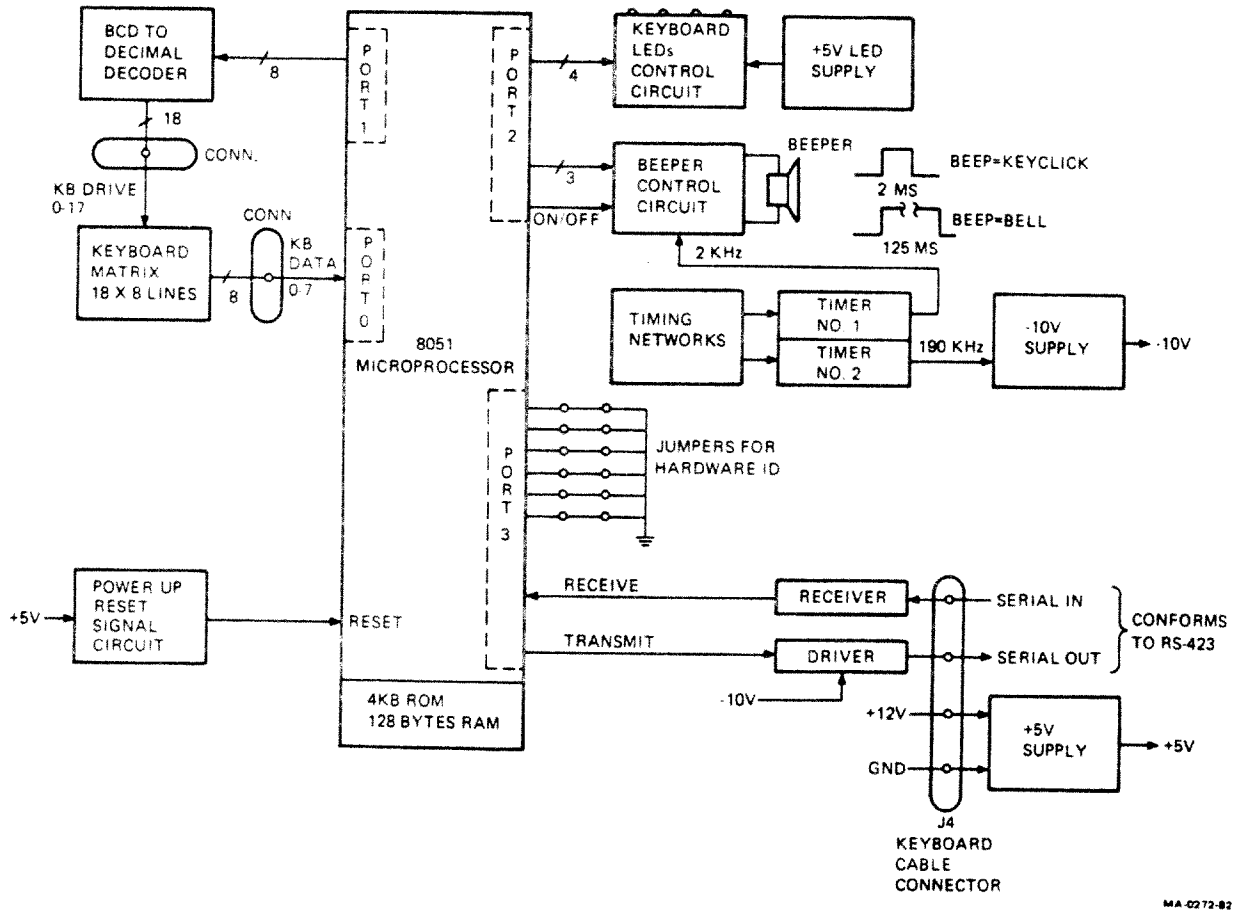


Figure 7-4 LK201 Keyboard Block Diagram

The firmware in the 8051 8-bit microprocessor controls the following three major keyboard operations at the same time.

1. Scans the keyboard to detect changes in the keyboard matrix

2. Transmits results of the keyboard scan to the CPU

3. Receives information from the CPU

7.3.1.1 Keyboard Scanning -- The keyboard switches are connected at the intersections of an 18 X 8 line matrix. This provides a fixed position identifier for each key.

The firmware scans the 18-line axis and detects a pressed or newly released key by reading the 8-line axis. The firmware then verifies the detected keystroke and changes this position information into an 8-bit code that is unique to that key.

7.3.1.2 Control of Audio Transducer and Indicators -- Two circuits control the audio transducer and the indicators. One circuit receives its inputs from the 8051 and controls the transducer (beeper). A long beep represents the bell and a short beep represents the keyclick.

A separate circuit, controlled by a signal from the 8051, controls each of the four indicators. The firmware, responding to commands received from the CPU, turns the indicators on or off.

7.3.2 Keyboard Firmware Functions

This section describes the keyboard firmware functions. The functions are divided into two categories: functions that cannot be changed by CPU instructions and those that can.

7.3.2.1 Functions Not Changed by CPU Instructions -- The following functions cannot be changed by instructions from the CPU.

Power-Up test
Keycodes
Special codes

Power-Up Test

Upon power-up, the firmware performs a self-test in less than 70 ms. The test results are transmitted to the CPU in four bytes.

The keyboard indicators are lit during the self-test. The indicators blink once during the self-test routine. The indicators remain lit if the test is failed, but go off if the test is passed. The system module can also request a self-test at any time.

Keycodes

The keycodes represent fixed positions in the key switch matrix. The key associated with a particular matrix position is always represented by the same keycode.

Special Codes

There are 13 special codes transmitted by the keyboard. Four codes transmit the results of the power-up self-test. The other nine codes are status indicators or command acknowledgements.

7.3.2.2 Functions Changed by CPU Instructions -- The CPU can issue instructions to change some keyboard transmission characteristics and control the keyboard indicators and beeper.

Upon completion of a successful power-up self-test, the firmware sets certain functions to predetermined conditions. These are referred to as default conditions. The conditions can be changed but they always come up to the default condition after a successful power-up self-test.

7.3.2.3 Firmware Functions Changed by CPU Instructions -- Certain firmware functions can be changed by commands (instructions) from the CPU. These commands are categorized as transmission commands and peripheral commands. Transmission commands contain a mode set command and an autorepeat rate set command. Peripheral commands contain a variety of commands. Refer to section 7.5.5.3 for more information on peripheral commands.

7.4 Detailed Keyboard Circuit Description

This section describes the keyboard circuit. Figure 7-4 shows the keyboard block diagram.

7.4.1 Keyboard Matrix Scanning

The key locations are arranged in an 18 X 8 line matrix. Each key switch is connected across a matrix intersection. This gives a fixed position for each key connected in the matrix. This matrix accommodates all 105 keys in the keyboard.

Figure 7-5 is a simplified block diagram of the matrix scanning circuit. Eight lines from PORT 1 of the 8051 microprocessor go to the binary coded decimal (BCD) inputs of two 74LS145 BCD-to-decimal decoders. Ten outputs from one decoder and eight outputs from the other decoder provide the drive lines for the matrix. These 18 lines are called KB DRIVE 0 -- 17.

The other axis of the matrix consists of eight lines tied to +5 V through pull-up resistors. These lines go to PORT 0 of the 8051 microprocessor and are called KB DATA 0 -- 7.

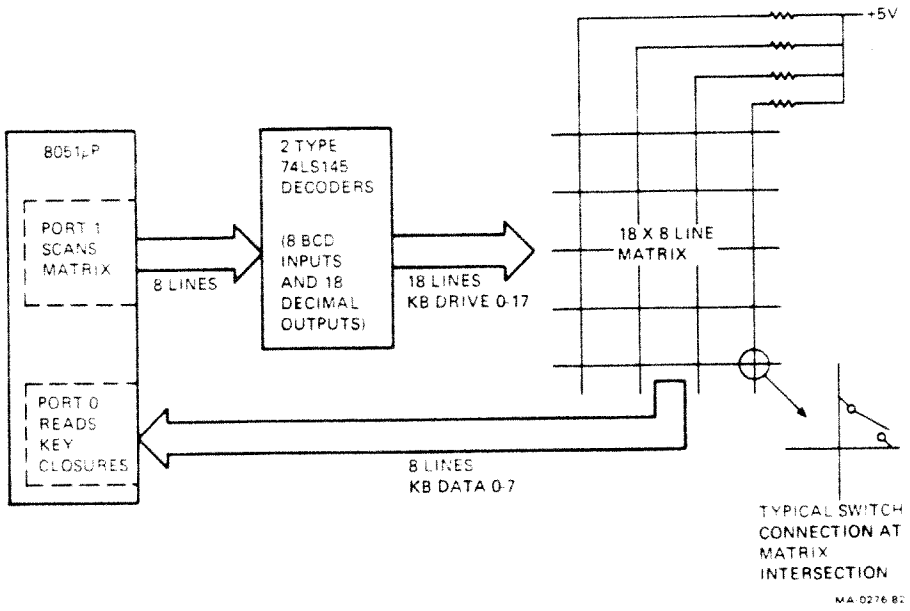


Figure 7-5 Matrix Scanning Block Diagram

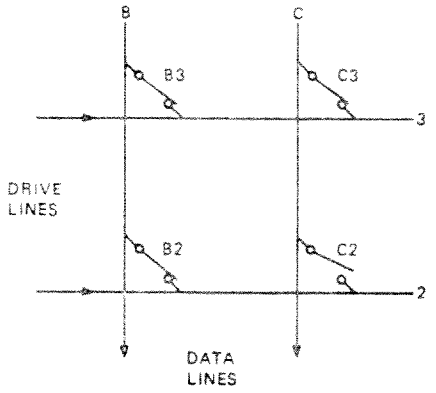
The 8051 scans the 18 drive lines. Key closures are detected by reading the eight data lines. The complete matrix is scanned every 8.33 ms.

When a key closure is detected, it is scanned again to verify that it is really a key closure and not just electrical noise.

Once the key closure is verified, the 8051 firmware translates the position information into a key code and transmits it to the CPU. Transmission is handled by the Universal Asynchronous Receiver Transmitter (UART) in the 8051.

A ghost key indication can occur when three of the four corners of a matrix rectangle are closed (Figure 7-6), causing what is known as a sneak path. The key positions in the matrix are arranged to avoid sneak paths. However, if a sneak path does occur, the firmware prevents the keycode for the key that caused the sneak path to be transmitted until one of the involved keys is released. This prevents transmission of ghost keys entirely.

Table 7-1 shows the keyboard matrix on the LK201-AA (American) keyboard. Keycap designations are listed for reference only; you can compare them to Figure 7-7 (A and B).



1. CONDITIONS ARE: SWITCHES B2, B3, AND C3 CLOSED, SWITCH C2 OPEN; LINE 2 IS BEING DRIVEN AND LINE C IS BEING READ.

2. INTERSECTION C2 IS BEING LOOKED AT. IT SHOULD NOT SHOW A KEY CLOSURE BECAUSE SWITCH C2 IS OPEN.

3. HOWEVER A SNEAK PATH IS PRESENT FROM LINE 2 THROUGH SWITCHES B2, B3, AND C3 TO LINE C. A GHOST KEY IS READ AT INTERSECTION C2.

MA-0273-82

Figure 7-6 Example of Ghost Key Generation

Table 7-1 Keyboard Matrix

Refer to Figure 7 (A and B). It shows the international matrix for the LK201 keyboard. The legends are from the LK201 keyboard and are provided for convenience only.

KB Drive	KB DATA 7	6	5	4	3	2	1	Ø
17	Reserved	F19	Reserved	F20	PF4	N (Note 1)	N,	ENTER
		G22		G23	E23	D23	C23	A23
16	F18	PF3	Reserved	N9	↓	N6	N3	N.
	G21	E22		D22	B17	C22	B22	A22
15	F17	PF2	Reserved	N8	N5	→	N2	NØ (See
	GØ	E21		D21	C21	B18	B21	Note 2
14	PF1	NEXT SCREEN	REMOVE	↑	N7	N4	N1	NØ
	E20	D18	E18	C17	DØ	CØ	BØ	AØ
13	INSERT HERE	-	DØ	PREV SCREEN	{ [	" '	Reserved	Reserved
	E17	E11	G16	D17	D11	C11		

NOTES

1. Note that NØ -- N9, N_, N,, refer to the numeric keypad.

2. NØ of the numeric keypad can be divided into two keys. Normally only the NØ keyswitch is implemented as a double-sized key.

3. The **RETURN** key also can be divided into two keys. The one that is decoded as return is the **RETURN** (C13) key.

Table 7-1 Keyboard Matrix (Cont)

KB Drive	KB DATA 7	6	5	4	3	2	1	Ø
12	FIND	+ =	HELP	SELECT	}]	RETURN	<	\
	E16	E12	G15	D16	D12	C13	B16	C12
11	ADDTNL OPTIONS	X (delete)	Reserved	) Ø	P	See Note 3	: ;	? /
	G14	E13		E10	D10		C10	B10
10	Reserved	F12	Reserved	F13	(9	O	L	. .
		G12		G13	E09	D09	C09	B09
9	Reserved	F11	Reserved	Reserved	* 8	I	K	. .
		G11			E08	D08	C08	B08
8	Reserved	MAIN SCREEN	Reserved	EXIT	& 7	U	J	M
		G08		G09	E07	D07	C07	B07
7	Reserved	CANCEL	Reserved	RESUME	^ 6	Y	H	N
		G07		G06	E06	D06	C06	B06
6	Reserved	Reserved	Reserved	INTER-RUPT	% 5	T	G	B
				G05	E05	D05	C05	B05
5	SETUP	F5	Reserved	$ 4	R	F	V	SPACE
	G02	G03		E04	D04	C04	B04	A01-A09

Table 7-1 Keyboard Matrix (Cont)

KB Drive	KB DATA 7	6	5	4	3	2	1	Ø
4	Reserved	PRINT SCREEN G00	Reserved	BREAK G01	# 3 E03	E D03	D C03	C B03
3	HOLD SCREEN G99	@ 2 E02	Reserved	TAB D00	W D02	S C02	X B02	> < B00
2	Reserved	Reserved	Reserved	~ E00	! 1 E01	Q C01	A B01	Z
1	CTRL C99	LOCK C00	COMPOSE A99	Reserved				
Ø	SHIFT B99,B11							

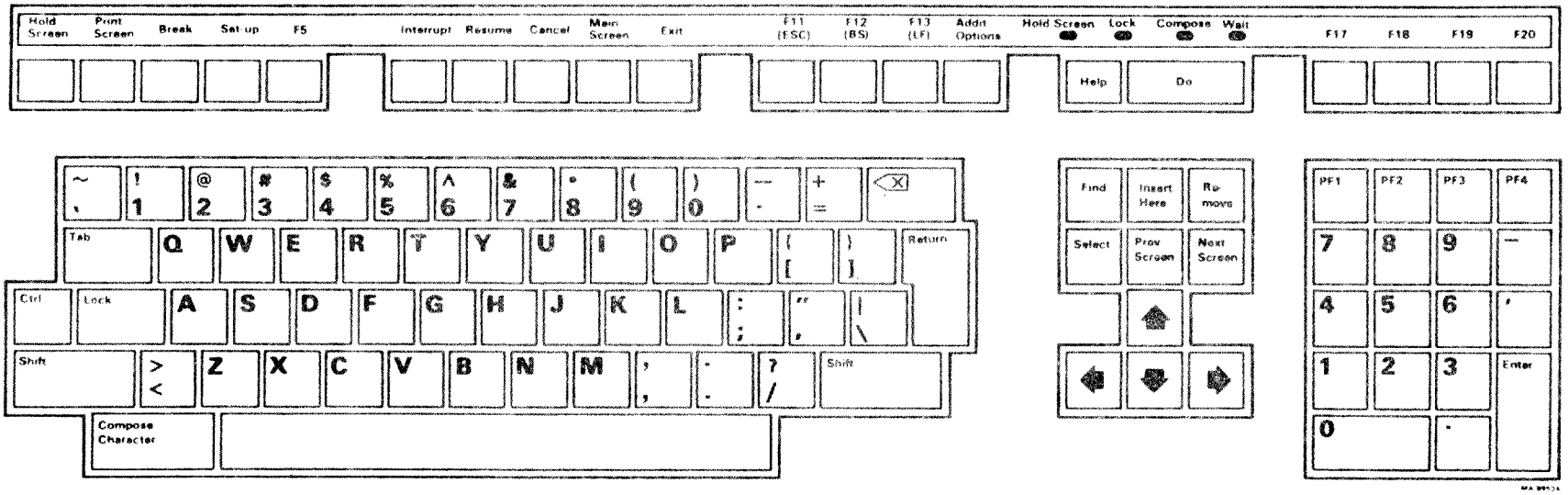
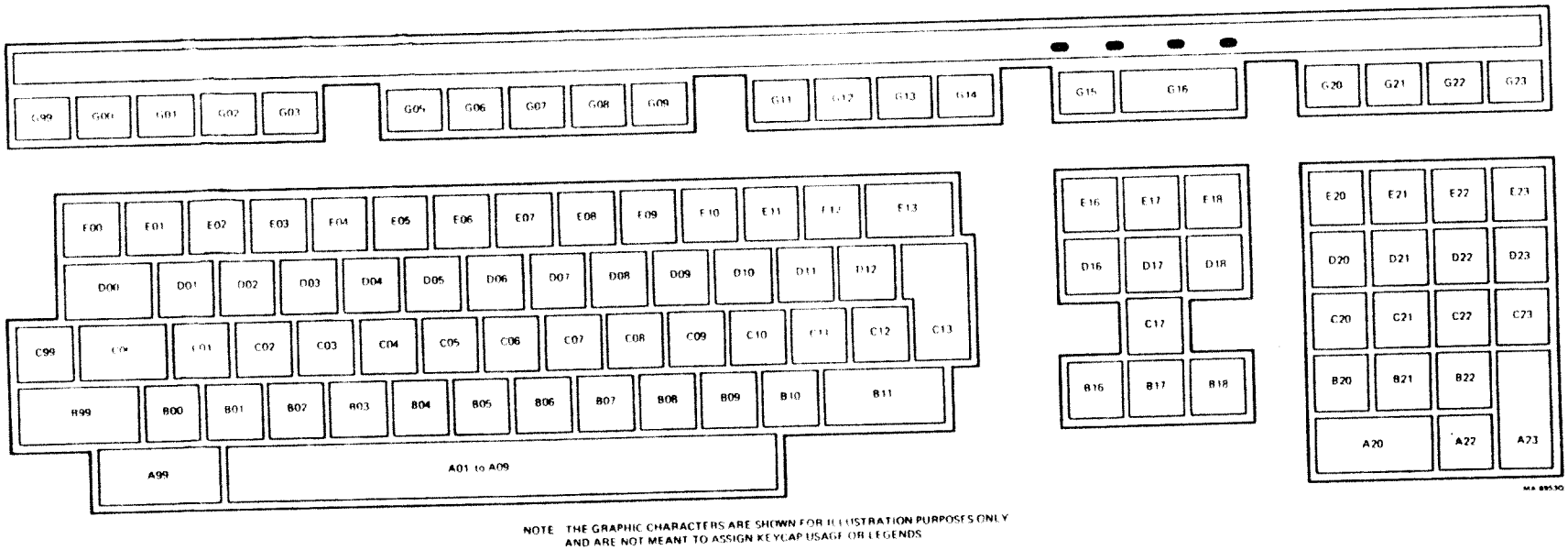


Figure 7-7A LK201-AA Keyboard Layout



NOTE THE GRAPHIC CHARACTERS ARE SHOWN FOR ILLUSTRATION PURPOSES ONLY AND ARE NOT MEANT TO ASSIGN KEYCAP USAGE OR LEGENDS

Figure 7-7B LK201-AA Keyboard Layout

7.4.2 Audio Transducer Control Circuit

Figure 7-8 shows the audio transducer or beeper control circuit. The beeper is driven by a transistor whose base is connected to a 2 KHz square wave from a 556 timer IC. This signal is biased by a network of four type 74LS05 open collector inverters. The 8051 microprocessor controls all four inverters via the firmware. The on/off inverter connects directly to the transistor base. When the 8051 puts a high on the on/off inverter input, its output goes low and removes the 2 KHz square wave from the transistor base. This cuts off the transistor and disables the beeper.

To turn on the beeper, the 8051 puts a low on the on/off inverter input. Its output goes high and allows the 2 KHz signal to reach the transistor base; this turns on the beeper. The firmware generates a keyclick (on for 2 ms) or a bell tone (on for 125 ms). The 8051 sets up the three level control inverters by putting one of eight binary combinations on the inverter inputs. All highs give the softest sound and all lows give the loudest sound.

The firmware controls the keyclick and the bell tone independently. The bell tone is sounded only upon request from the system control processor. The keyclick is sounded (unless disabled) under the following conditions.

- When a key is pressed
- When a metronome code is sent
- When a command to sound the keyclick is received from the system control processor

7.4.3 Indicator (LED) Control Circuit

Figure 7-9 shows the LED indicator control circuit.

The control signal for each LED comes from PORT 2 of the 8051 to the input of a type 74LS05 open collector inverter. The inverter output goes to the LED cathode; its anode is connected to +5 V. A separate +5 V source relieves the LEDs load on the main +5 V supply.

A low signal from the 8051 drives the inverter output high, which cuts off the LED. A high signal from the 8051 drives the inverter output low. This provides a path to ground from the +5 V through the LED. The LED then turns on.

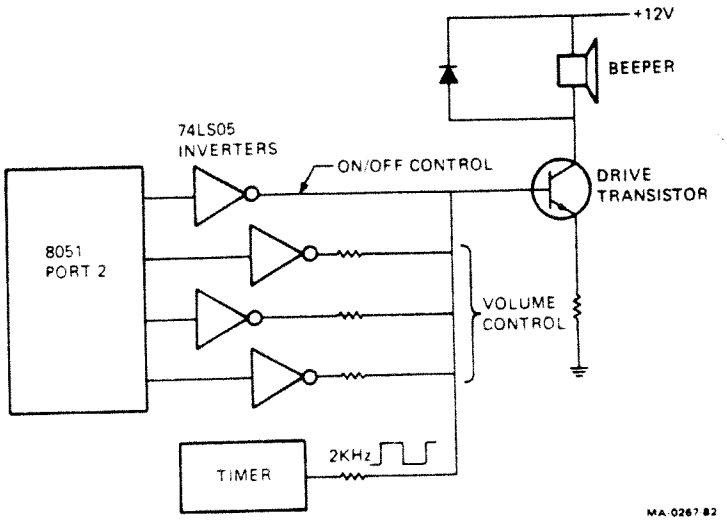


Figure 7-8 Beeper Control Circuit

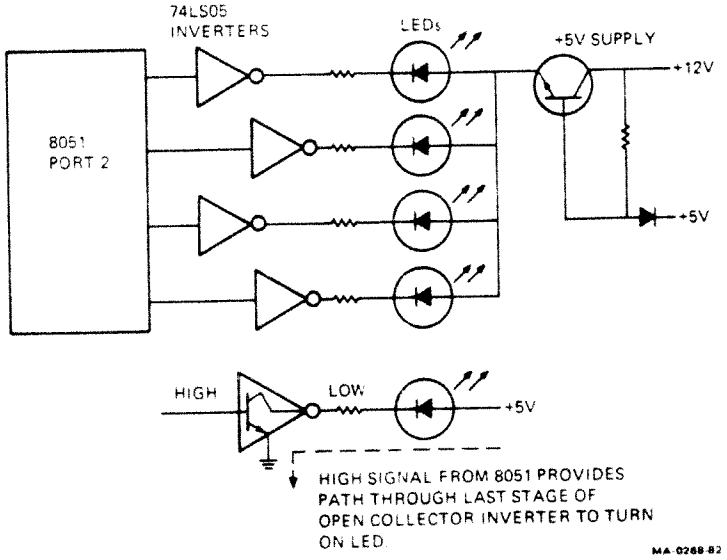


Figure 7-9 Indicator (LED) Control Circuit

7.4.4 Keyboard Communication

This section describe the keyboard communication.

7.4.4.1 Keyboard Transmit Mode -- The keyboard codes and a few other special codes are transmitted via a serial line output in PORT 3 of the 8051. The transmitted signal goes from the 8051 to a driver, through the keyboard cable, monitor, and video cable to the CPU. A UART within the 8051 controls the transmission.

Transmitted characters conform to a specific format. Each character is 10 bits long. The first bit is the start bit. It is always a logical zero (space). The next eight bits represent the encoded data. The last bit is the stop bit. It is always a logical one (mark). Figure 7-10 shows the character format.

7.4.4.2 Keyboard Receive Mode -- The firmware contains features that can be enabled by commands from the CPU. There are two categories of features: one sets keyboard transmission characteristics and the other controls keyboard peripherals. A peripheral command covers indicator control, bell and keyclick loudness, keyboard ID code, and reinstate keyboard. The commands come from the CPU and pass through the video cable, monitor, and keyboard cable to the receiver and into the 8051 via PORT 3. The commands go to the UART in the 8051.

Received characters conform to the same 10-bit format used for transmitted characters. The eight data bits are arranged in a specified protocol, depending on the command type.

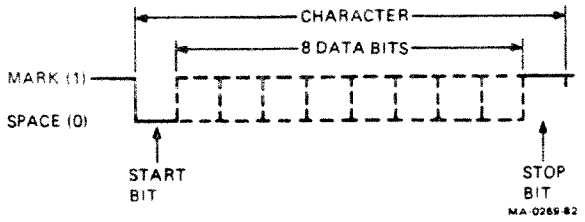


Figure 7-10 Keyboard Transmit and Receive Character Format

7.4.5 Reset Signal for 8051 Microprocessor

Whenever the system is turned on, the 8051 microprocessor in the keyboard must be reset. This allows the 8051 to start operating.

The reset signal generator is active only during powerup. The input is +5 V. The output is connected to the RESET input of the 8051. When power is turned on, the +5 voltage starts to rise from zero. The reset signal circuit output follows it and drops off when a steady state of +5 V is reached. This circuit holds the 8051 RESET input high (+3.5 V to +5 V) long enough to enable the reset action in the 8051. This action occurs only during powerup.

7.4.6 Hardware Keyboard Identification (ID)

At powerup, the keyboard performs a self-test and sends the results to the CPU. One piece of information to be sent is the keyboard hardware ID, which is read from hardwired jumpers.

There are six jumpers. Each jumper line goes from an input in PORT 3 of the 8051 to ground. All jumpers are installed so the keyboard hardware ID is zero.

7.4.7 Voltage Supplies

The only voltage sent to the keyboard is +12 V. However, +5 V and -10 V are also required. These voltages are derived from the +12 V.

There is a +5 V supply that handles most of the requirements for this voltage. The four keyboard LEDs have their own +5 V supply. A -10 V supply provides voltage for the driver in the serial out line.

7.5 KEYBOARD PROGRAMMING

This section describes the functions that the keyboard performs under system central processor control. This section also describes keyboard programming machine language, but does not describe high level user programming.

7.5.1 Keyboard Layout and Key Identification

Each keyboard key has a unique location. Each location is scanned, and when closure or release is detected, the location is verified. This information is then decoded to an 8-bit keycode. Figure 7-7 shows the keyswitch locations. Table 7-2 shows the 14 functional divisions of the keyboard. Table 7-3 shows the divisions, keycaps, and keycodes.

Table 7-2 Keyboard Functional Divisions

Division	Description	Representation
1	48 graphic keys and spacebar	0001
2	Numeric keypad	0010
3	Delete character (E12)	0011
4	Return (C13) Tab (D00)	0100
5	Lock (C00) Compose (A99)	0101
6	Shift (B99 and B11) CTRL (C99)	0110
7	Horizontal cursors (B16 and B18)	0111
8	Vertical cursors (B17 and C17)	1000
9	Six keys directly above the cursor keys (D16 -- D18 and E16 -- E18)	1001
10	Function keys (G99 -- G03)	1010
11	Function keys (G05 -- GO9)	1011
12	Function keys (G11 -- G14)	1100
13	Function keys (G15 -- G16)	1101
14	Function keys (G20 -- G23)	1110

Table 7-3 Keycode Translation Table

Division	Position	Keycap	Keycode Decimal	Keycode Hexadecimal
Function Keys				
10	G99	Hold screen	086	56
	G00	Print screen	087	57
	G01	Break	088	58
	G02	Setup	089	59
	G03	F5	090	5A
	--	Reserved	091--098	5B--62
11		Reserved	099	63
	G05	Interrupt	100	64
	G06	Resume	101	65
	G07	Cancel	102	66
	G08	Main screen	103	67
	G09	Exit	104	68
	--	Reserved	105--110	69--6E
12	--	Reserved	111	6F
	--	Reserved	112	70
	G11	F11 (ESC)	113	71
	G12	F12 (BS)	114	72
	G13	F13 (LF)	115	73
	G14	Additional Options	116	74
		Reserved	117--122	75--7A
13	--	Reserved	123	7B
	G15	Help	124	7C
	G16	D0	125	7D
14	--	Reserved	126--127	7E--7F
	G20	F17	128	80
	G21	F18	129	81
	G22	F19	130	82
	G23	F20	131	83
	--	Reserved	132--135	84--87
6 Basic Editing Keys				
9	--	Reserved	136--137	88--89
	E16	Find	138	8A
	E17	Insert here	139	8B
	E18	Remove	140	8C
	D16	Select	141	8D
	D17	Previous screen	142	8E
	D18	Next screen	143	8F
	--	Reserved	144	90

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexadecimal
Keypad				
2	--	Reserved	145	91
	A20	0	146	92
	--	Reserved	147	93
	A22	.	148	94
	A23	Enter	149	95
	B20	1	150	96
	B21	2	151	97
	B22	3	152	98
	C20	4	153	99
	C21	5	154	9A
	C22	6	155	9B
	C23	,	156	9C
	D20	7	157	9D
	D21	8	158	9E
	D22	9	159	9F
	D23	--	160	A0
	E20	PF1	161	A1
	E21	PF2	162	A2
	E22	PF3	163	A3
	E23	PF4	164	A4
		Reserved	165	A5
Cursor Keys				
7	--	Reserved	166	A6
	B16	Left	167	A7
	B18	Right	168	A8
8	B17	Down	169	A9
	C17	Up	170	AA
	--	Reserved	171--172	AB--AC
Shift, Lock CTRL, A99, and A10				
6	--	Reserved	173	AD
	B99,B11	Shift	174	AE
	C99	CTRL	175	AF
5	C00	Lock	176	B0
	A99	Compose	177	B1
	--	Reserved	178	B2

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexadecimal
Special Codes				
		All ups	179	B3
		Metronome	180	B4
		Output error	181	B5
		Input error	182	B6
		KBD Locked acknowledge	183	B7
		Test mode acknowledge	184	B8
		Prefix to keys down	185	B9
		Mode change acknowledge	186	BA
		Reserved	187	BB
Delete				
3	E13	Delete (X)	188	BC
Return and Tab				
4	C13	Return	189	BD
	D00	Tab	190	BE
48 Graphics Keys and Spacebar				
1	E00	Tilde	191	BF
	E01	!1	192	D0
	D01	Q	193	C1
	C01	A	194	C2
	B01	Z	195	C3
	--	Reserved	196	C4
	E02	@2	197	C5
	D02	W	198	C6
	C02	S	199	C7
	B02	X	200	C8
	B00	><	201	C9
	--	Reserved	202	CA
	E03	#3	203	CB
	D03	E	204	CC
	C03	D	205	CD
	B03	C	206	CE
	--	Reserved	207	CF
	E04	$4	208	D0
	D04	R	209	D1
	C04	F	210	D2
	C04	V	211	D3

Table 7-3 Keycode Translation Table (Cont)

Division	Position	Keycap	Keycode Decimal	Keycode Hexadecimal
	A01--A09	Space	212	D4
	--	Reserved	213	D5
	E05	%5	214	D6
	D05	T	215	D7
	C05	G	216	D8
	B05	B	217	D9
	--	Reserved	218	DA
	E06	^6	219	DB
	D06	Y	220	DC
	C06	H	221	DD
	B06	N	222	DE
1	--	Reserved	223	DF
	E07	&7	224	E0
	D07	U	225	E1
	C07	J	226	E2
	B07	M	227	E3
	--	Reserved	228	E4
	C08	*8	229	E5
	D08	I	230	E6
	C08	K	231	E7
	B08	' '	232	E8
	--	Reserved	233	E9
	E09	(9	234	EA
	D09	0	235	EB
	C09	L	236	EC
	B09	. .	237	ED
	--	Reserved	238	EE
	E10	)0	239	EF
	D10	P	240	F0
	--	Reserved	241	F1
	C10	: ;	242	F2
	B10	? /	243	F3
	--	Reserved	244	F4
	E12	+ =	245	F5
	D12	}]	246	F6
	C12	| \	247	F7
	--	Reserved	248	F8
	E11	_ -	249	F9
	D11	{ [	250	FA
	C11	. ,	251	FB
	--	Reserved	252-255	FC-FF

NOTE
The legends under "keycap" are taken from the keycap legends of the LK201-AA (American).

Keycodes 00 through 64 are reserved. Keycodes 65 through 85 are unused.

7.5.2 Modes

This section describes the function of the keycode transmission modes. The mode set command allows any one of the 14 keyboard divisions to be set to any one of the following three modes. (Refer to section 7.5.7 for division defaults.)

- Down only mode -- The keyboard transmits a keycode when the key is pressed.
- Autorepeat down -- The keyboard transmits a keycode when the key is first pressed. If the key is held down past the specified timeout period (usually 300 to 500 ms), a fixed metronome code is sent at the specified rate until the key is released.
- Down/up -- The keyboard transmits a keycode when the key is pressed and an "up code" when the key is released. If any other DOWN/UP keys are pressed, the "up code" is a repeat of the "down code." If no other DOWN/UP keys are pressed, the keyboard sends an ALL UPS code.

7.5.2.1 Special Considerations Regarding Autorepeat -- The autorepeat rate set command allows the following changes in the autorepeat mode.

- Autorepeat rate buffer association can be changed for the selected keyboard division.
- The timeout and interval values can be changed in any one of the four autorepeat rate buffers.
- If multiple autorepeating keys are held down, metronome codes are still generated. The metronome codes apply to the keycode transmitted most recently. If the last key pressed is released, and any other keys are still down, the keycodes for those keys are retransmitted.

Example 1

The a key is held down. This produces the following transmission.

a metronome metronome

Now the b key is pressed. This produces the following transmission.

a metronome metronome b metronome metronome

Now the b key is released. This produces the following transmission.

a metronome metronome b metronome metronome a metronome met. . .

While metronome codes are being generated for an autorepeating key, a nonautorepeating keycode or special code may be transmitted. The keyboard transmits this special code instead of the next metronome code, and then returns to the autorepeated code. The keycode to be autorepeated is always the last byte transmitted.

Example 2

The a key is held down. This produces the following transmission.

a metronome metronome

Now the SHIFT key is pressed. This produces the following transmission.

a metronome metronome shift a metronome

Now the SHIFT key is released. This produces the following transmission.

a metronome metronome shift a metronome ALL UPS a metronome. . .

- If an autorepeating key is not to autorepeat (**CTRL C** for example), the system module must issue a temporary inhibit autorepeat command. This halts the transmission of any metronome codes or keyclicks for that key only. Metronome codes continue when another key is pressed. The command must be issued after the keycode for the autorepeating key is received.

- Autorepeat can be enabled and disabled independently of the division settings by using the enable/disable autorepeat commands. These commands apply to all keys on the keyboard. When autorepeat is disabled, internally the keyboard continues to autorepeat characters. However, it does not transmit metronome codes or keyclicks. When autorepeat is enabled, the keyboard transmits the metronome codes from the point they were before autorepeat was disabled. This may be within either the timeout or interval period, depending upon the time elapsed since the key was pressed.

- If the keyboard receives a request to change a division mode to autorepeat while a key is pressed, the keyboard makes the change immediately. After the specified timeout period, the keyboard transmits metronome codes for the pressed key. In place of the first metronome code, the keyboard transmits the keycode of the autorepeating key.

All autorepeating division modes can be changed to only down with one command. This and other autorepeat commands are grouped with the peripheral commands (refer to section 6.5.5.3).

7.5.2.2 Special Considerations Regarding Down/Up Mode -- If two DOWN/UP keys are released simultaneously (within the same scan), and there are no other DOWN/UP keys down on the keyboard, only one ALL UPS code is generated.

7.5.2.3 Autorepeat Rates -- There are four buffers in the keyboard to store autorepeat rates. They are numbered zero through three. Each buffer stores the following two values. These values can be changed by the system module.

The timeout value
The interval value

The timeout value is the amount of time between the detection of a down key and the transmission of the first metronome code (defaults range from 300 to 500 ms). The interval value is the number of metronome codes per second (defaults to 30).

Each division is associated with one of the four buffers. Rates are taken from the associated buffer each time the autorepeat timers are loaded. This buffer-to-division association can be changed by the system module, or left to default.

7.5.3 Keyboard Peripherals

This section describes the peripherals available on the keyboard. The keyclick, bell, and LEDs are all considered keyboard peripherals. Refer to section 7.5.5.3 for information on system module control over these peripherals.

7.5.3.1 Audio -- The keyclick is a 2 ms beep and the bell is a 125 ms beep. The bell is sounded only upon request from the system module. The keyclick (if not disabled by the system module) sounds when a key is pressed, when a metronome code is sent, or when the system module receives a sound keyclick command.

If either the B11 or B99 keys (the left and right SHIFT keys on the LK201) or the C99 key (the CTRL key on the LK201) are pressed, the keyclick is not generated. However, if a command is sent from the system module to enable the keyclick on the C99 key, the keyclick is generated (refer to section 7.5.5.3). Figure 7-7 shows the positions of these keys.

The keyclick or bell (or both) may be disabled. When the keyclick or bell is disabled, it does not sound. If the system module requests sound (refer to section 7.5.5.3) the keyclick or the bell does not sound.

Both the keyclick and bell may be independently set to one of the following eight volume levels.

000 -- highest
001
010 -- default
011
100
101
110
111 -- lowest

7.5.3.2 Indicators (LEDs) -- The system module normally transmits indicator control commands. However the following are exceptions.

- Upon powerup, the keyboard turns all LEDs off.
- After receiving the inhibit transmission command, the keyboard turns on the keyboard-locked LED. The LED is turned off after the keyboard receives a resume transmission command.

7.5.4 Keyboard-to-System Module Protocol

This section describes the keyboard-to-system module protocol.

7.5.4.1 Keycode Transmission -- The keyboard transmits single byte keycodes that reflect the keyboard matrix status. The eight-bit codes above 6410 are used for keycodes. Every key is identified by a unique keycode. There are no special codes for shifted or control keys.

Refer to Figure 7-7 and Tables 7-1 and 7-2 for complete keycode matrix translation table information.

7.5.4.2 Special Code Transmission -- There are 13 special codes. Nine codes have values above 6410 and four codes have values below.

The following nine special codes have values above 6410 (keycode value range).

- ALL UPS — Keycode 179 (decimal), B3 (hexadecimal)
- METRONOME CODE — Keycode 180 (decimal), B4 (hexadecimal)
- OUTPUT ERROR — keycode 181 (decimal), B5 (hexadecimal)

- INPUT ERROR — Keycode 182 (decimal), B6 (hexadecimal)
- KBD LOCKED ACK — Keycode 183 (decimal), B7 (hexadecimal)
- TEST MODE ACK — Keycode 184 (decimal), B8 (hexadecimal)
- PREFIX TO KEYS DOWN — Keycode 185 (decimal), B9 (hexadecimal)
- MODE CHANGE ACK — Keycode 186 (decimal), BA (hexadecimal)
- RESERVED — Keycode 127 (decimal), 7F (hexadecimal)

ALL UPS -- indicates to the system module that a **DOWN/UP MODE** key was just released and no other DOWN/UP keys are pressed.

METRONOME CODE -- indicates to the system module that an interval has passed, a keyclick has been generated, and the last key received by the system module is still pressed.

OUTPUT ERROR -- indicates an output buffer overflow to the system module. The overflow occurred after receiving a keyboard inhibit command from the system module, and some keystrokes may be lost.

INPUT ERROR CODE -- indicates to the system module that the keyboard received a meaningless command, too many parameters, or too few parameters.

KEYBOARD LOCKED CONFIRMATION -- indicates to the system module that the keyboard received an inhibit transmission command (refer to section 7.5.5.3).

TEST MODE ACKNOWLEDGE -- indicates that the keyboard has entered test mode. This is a special mode used during the production test. If the system module receives this acknowledgement, it sends 8Ø hexidecimal. This terminates the test mode and jumps to power-up.

PREFIX TO KEYS DOWN -- indicates that the next byte is a keycode for a key already down in a division which has been changed to down/up (refer to section 7.5.5.4).

MODE CHANGE ACKNOWLEDGE -- indicates that the keyboard has received and processed a mode change command (refer to section 7.5.5.4).

RESERVED -- indicates that keycode 7F is reserved for internal use.

• KEYBOARD ID (firmware)	Keycode 01 (decimal), 01 (hexadecimal)
• KEYBOARD ID (hardware)	Keycode 00 (decimal), 00 (hexadecimal)
• KEY DOWN ON POWER-UP ERROR CODE	Keycode 61 (decimal), 3D (hexadecimal)
• POWER-UP SELF-TEST ERROR CODE	Keycode 62 (decimal), 3E (hexadecimal)

KEYBOARD ID -- is a two byte identification code, transmitted after the power-up self-test (refer to section 7.5.4.3). It is also sent on request from the system module (refer to section 7.5.5.3).

KEY DOWN ON POWER-UP ERROR CODE -- indicates that a key was pressed on power-up.

POWER-UP SELF-TEST ERROR CODE -- indicates to the system module that the ROM or RAM self-test of the system module failed (refer to section 7.5.4.3).

7.5.4.3 Power-Up Transmission -- Upon power-up, the keyboard performs a self-test in less than 70 ms, then transmits the self-test results to the system module in 4 bytes.

Byte 1	KBID (firmware) -- This is the keyboard identification (ID) stored in the firmware.
Byte 2	KBID (hardware) -- This is the keyboard ID read from hardware jumpers.
Byte 3	ERROR -- Two error codes indicate either the failure of the ROM or RAM self-test within the processor (3E hexadecimal), or a keydown on powerup (3D hexadecimal). No error is indicated by 00.
Byte 4	KEYCODE -- This byte contains the first keycode detected if there was a key pressed on power-up. No error is indicated by 00.

If the ROM self-test (CHECKSUM) fails and the error is critical, the keyboard is unable to transmit. Noncritical errors let the keyboard continue operating.

If the keyboard finds a key pressed on the first scan, it continues to look for an ALL UPS condition. The keyboard sends the corrected four-byte power-up sequence when the pressed key is released. This avoids a fatal error condition if a key is pressed by mistake while powering up.

The keyboard LEDs are lit during the power-up self-test. If the self-test passes, the keyboard turns the LEDs off. If a bell is selected on powerup, the system module can transmit a sound bell command to the keyboard. However, this should not be done until the system module receives the last byte of the four-byte sequence. The request for self-test tests the serial line and system module connection. The power-up self-test takes 70 ms or less.

The system module can request a jump to powerup at any time. This causes the LEDs on the keyboard to blink on and off (for the power-up self-test).

7.5.5 System Module to Keyboard Protocol

The system module controls both the peripherals associated with the keyboard and the keyboard transmit characteristics. Figure 7-11 shows the protocol for command and parameter transmission from the system module to the keyboard.

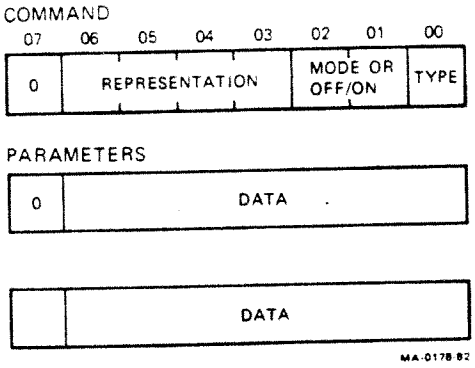


Figure 7-11 System Module to Keyboard Protocol

7.5.5.1 Commands -- There are two kinds of commands, commands that control keyboard transmission characteristics and commands that control keyboard peripherals. The low bit of the command is the TYPE flag. The TYPE flag is clear if the command is a transmission command, and set if the command is a peripheral command.

Transmission Commands	Peripheral Commands
Mode set	Flow control
Autorepeat rate set	Indicator Audio Keyboard ID Reinitiate keyboard Some autorepeat control Jump to test mode Reinstate defaults

The high order bit of every command is the PARAMS flag. If there are any parameters to follow, the PARAMS flag is clear. If there are no parameters to follow, the PARAMS flag is set.

7.5.5.2 Parameters -- The high order bit of every parameter is the PARAMS flag. This flag is clear if there are parameters to follow, and set on the last parameter. The remaining seven bits of the parameter are for data.

7.5.5.3 Peripheral Commands -- The following two commands can turn the data flow from the keyboard off and on.

- Inhibit keyboard transmission -- shuts off or locks the keyboard and turns on the keyboard locked LED. After receiving the inhibit command, the keyboard sends a special command to the system central processor. If the system central processor receives this code without requesting it, this indicates that noise on the line was interpreted as the inhibit command. The central processor then responds immediately with the resume keyboard transmission command.

- Resume keyboard transmission -- turns on or unlocks the keyboard and turns off the keyboard locked LED. If any keystrokes are lost, the keyboard responds with an error code.

Each keyboard LED can be turned on and off.

The following eight commands control the keyclick and bell sounds.

- Disable keyclick
- Enable keyclick and set volume
- Disable CTRL keyclick
- Enable CTRL keyclick
- Sound keyclick
- Disable bell
- Enable bell and set volume
- Sound bell

The following four commands are related to control over the autorepeat mode.

- Temporary autorepeat inhibit -- stops autorepeat for a specific key only. It resumes automatically when another key is pressed.

- Enable autorepeat across the board -- starts transmission of metronome codes without affecting autorepeat timing or keyboard division.

- Disable autorepeat across the board -- stops transmission of metronome codes without affecting autorepeat timing or keyboard division.

- Change all autorepeat to down only -- changes all keyboard autorepeating divisions to down only mode.

The following are three other miscellaneous commands.

- Request keyboard ID -- causes the keyboard to send the two byte ID (firmware and hardware). The keyboard does not jump to the power-up sequence.

- Reinitiate keyboard -- causes the keyboard to jump to the power-up sequence. Transmission to the keyboard should be held until the host processor receives the last byte of the power-up self-test.

- Reinstate defaults -- sets the following functions back to the default settings after a successful power-up self-test.

  Division mode settings
  Autorepeat interval and timeout rates
  Autorepeat buffer selections
  Audio volume
  Control key keyclick

To send a peripheral command, set the TYPE flag (low order bit). Bits six -- three contain a command representation from the chart below. Bits two and one specify on (Ø1), off (ØØ), or sound (11). Bit seven should be set if there are no parameters to follow.

Table 7-4 lists the peripheral commands (in hexadecimal).

Table 7-4 Peripheral Commands in Hexadecimal

Function	Hex	Parameters
Flow control		
Resume keyboard transmission	8B	None
Inhibit keyboard transmission	89	None
Indicators		
Light LEDs	13	Bit pattern
Turn off LEDs	11	Bit pattern
Audio		
Disable keyclick	99	None
Enable click, set volume	1B	Volume
Disable CTRL keyclick	B9	None
Enable CTRL keyclick	BB	None
Sound keyclick	9F	None
Disable bell	A1	None
Enable bell, set volume	23	Volume
Sound bell	A7	None
Autorepeat		
Temporary autorepeat inhibit	C1	None
Enable autorepeat across keyboard	E3	None
Disable autorepeat across keyboard	E1	None
Change all autorepeat to down only	D9	None
Other		
Request keyboard ID	AB	None
Jump to powerup	FD	None
Jump to test mode	CB	None
Reinstate defaults	D3	None

Command	Representation
Flow control	0001
Indicator (LEDs)	0010
Keyclick	0011
Bell	0100
Keyboard ID	0101
Keyclick for CTRL key	0111
Temporarily inhibit autorepeat	1000
Jump to test mode	1001
Change all autorepeat characters to down only	1010
Enable/disable autorepeat	1100

The jump to power-up command is FD hexadecimal.

The following are some of the peripheral commands.

- Flow control -- The system module can lock the keyboard with the inhibit keyboard transmission command. When the keyboard is unlocked, it responds with an error code if any keystrokes were missed (refer to section 7.5.6.2).

- Indicators (LEDs) -- Figure 7-12 shows the LED parameter. Figure 7-13 shows the LED layout on the LK201 keyboard.

- Audio -- Figure 7-14 shows the audio volume parameter.

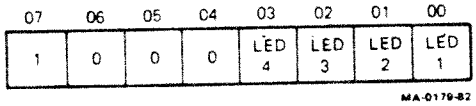


Figure 7-12 Indicator (LED) Parameter

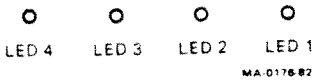


Figure 7-13 Indicator (LED) Layout

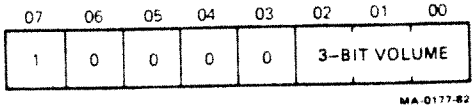


Figure 7-14 Audio Volume Parameter

The audio has the following volume levels.

```
000 -- highest
001
010
011
100
101
110
111 -- lowest
```

Either keyclick or bell (or both) can be disabled. When the keyclick or bell is disabled, it does not sound, even if the system module requests it.

The following are additional peripheral commands.

- Temporary autorepeat inhibit -- stops autorepeat for this key only. Autorepeat automatically continues when another key is pressed.

- Disable/enable autorepeat across keyboard -- stops/starts metronome code transmission without affecting autorepeat timing or division settings.

- Change all autorepeat to down only -- changes division settings for all autorepeating divisions to down only.

- Request keyboard ID -- causes keyboard to send a two-byte keyboard ID. Keyboard does not jump to powerup.

- Reinitiate keyboard -- causes keyboard to jump to its powerup routine. The system module should not try to transmit anything to the keyboard until the last byte of the power-up sequence is received.

- Jump to test mode -- is a special test mode for production test.

- Reinstate defaults -- sets the following functions back to the default settings after a successful power-up self-test.

  Division mode settings
  Autorepeat interval and timeout rates
  Autorepeat buffer selections
  Audio volume
  Control key keyclick

7.5.5.4 Mode Set Commands -- This section describes the mode set commands. It does not provide information about division mode settings. Refer to section 7.5.2 for an explanation of transmission modes and rates.

- Each division on the keyboard has a unique 4-bit representation (refer to section 7.5.1). Table 7-2 describes these representations.

- Each mode has a unique two-bit code.

Modes	Representation
Down only	ØØ
Autorepeat down	Ø1
Down/up	11

To set the key transmission mode on a particular keyboard division, the system module must send the PARAMS flag, then the keyboard division representation with the mode code, and then the TYPE flag (cleared).

Figure 7-15 shows a set main array to down/up.

The PARAMS flag is set to one if there are no parameters. The PARAMS flag is clear if there are parameters.

Autorepeat Rate Buffer Association -- If autorepeat mode is selected, the system module can transmit a parameter to change the buffer association of the selected division. Refer to section 7.5.2.3 for autorepeat rates and section 7.5.7 for default values.

Figure 7-16 shows a set main array to autorepeat, changing buffer association to buffer 3.

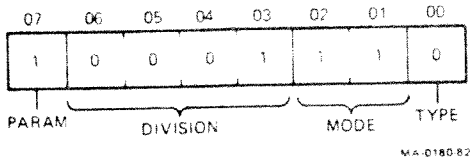


Figure 7-15 Set Main Array to Down/Up Example

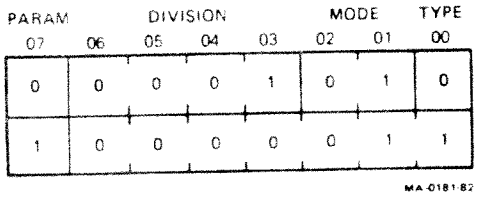


Figure 7-16 Set Main Array to Autorepeat Example

Autorepeat Rate Buffer Values -- At keyboard power-up time, the four autorepeat rate buffers contain default values (refer to section 7.5.2.3 for autorepeat rates and section 7.5.7 for defaults). The system module may change these values.

In the command byte, bit seven (PARAMS flag) should be clear, bits six -- three are 1111 (to indicate that this is a rate set command), bits two and one should be the buffer number (Ø -- 3), and bit zero (TYPE flag) is clear.

There should be two parameters carrying the rate set data.

Figure 7-17 shows change rates in buffer 3.

The first parameter specifies the timeout to the store in the selected buffer. The second parameter specifies the interval. (Refer to section 7.5.2.1 for definitions of these parameters.) For example, to set the autorepeat rate in buffer one, the system module firmware transmits ØØØØØØ11 followed by two bytes of numeric parameters.

The autorepeat timeout is the transmitted number times 5 ms. To specify a rate of 5 ms delay, the first parameter received is ØØØØØØØ1. The maximum allowable time is 630 ms (Ø1111110). The system module must not send 635 (Ø1111111).

NOTE
This code (635) is reserved for internal keyboard use. ØØ is an illegal value.

Autorepeat timeout is implemented as a multiple of 8.33 ms (the keyboard's internal scan rate). Timeout rates can vary ± 4.15 ms.

The autorepeat interval is the number of metronome codes per second. in order to specify a speed of 16 Hz, the second parameter received is 10010000. Note that the high order bit is set because it is the last parameter. The highest value which may be sent is 124 (11111100).

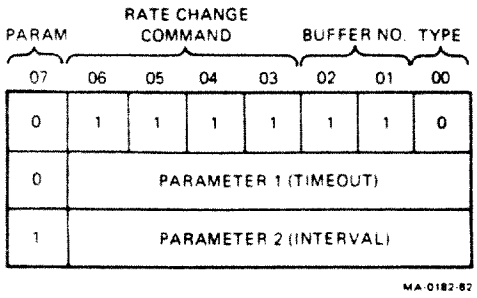


Figure 7-17 Change Rates in Buffer 3 Example

The lowest rate which can be implemented by the keyboard is 12 Hz. Values as low as 1 can be transmitted, but are translated to 12 Hz.

NOTE

The system module must not send 125 (11111101). This code is the power-up command.

7.5.6 Special Considerations

This section describes the special codes and related considerations.

7.5.6.1 Error Handling -- There are four error codes. The first two are sent at power-up if the self-test fails (refer to section 7.5.4.3). The other two codes are the INPUT ERROR code and the OUTPUT ERROR code.

The OUTPUT ERROR (B5 hexadecimal) is sent after the keyboard receives a resume transmission command if the output buffer overflowed while the keyboard was locked.

The INPUT ERROR (B6 hexidecimal) is sent when the keyboard detects noise (unidentified command or parameter) on the line. B6 is also sent if the keyboard detects a delay of more than 100 ms when it expects a parameter.

7.5.6.2 Keyboard Locked Condition -- When the keyboard receives an inhibit transmission command, it lights the LOCKED LED and transmits one more byte. This is a special code that indicates the keyboard is locked (KEYBOARD LOCKED ACKNOWLEDGE). If the system module receives this code without a request, the code indicates that noise on the line was interpreted as an inhibit transmission command. The system module should immediately send the resume transmission command to unlock the keyboard.

The output first in the first out (FIFO) buffer in RAM is four bytes. When the keyboard is locked it attempts to store characters received from the keyboard. The keyboard stops scanning its matrix. When the keyboard is unlocked by the system module, it transmits all four bytes in the output buffer. If any keystrokes have been missed due to buffer overflow, the keyboard transmits an error code as the fifth byte (OUTPUT ERROR). Any keys that were not transmitted and are being pressed when the keyboard is unlocked are processed as new keys. An error code upon unlocking the keyboard indicates a possible loss of keystrokes to the system module.

The keyboard stops scanning its matrix when its buffer is full. However, it processes all incoming commands.

7.5.6.3 Reserved Code -- The number 7F (hexidecimal) is reserved for the internal keyboard input and output buffers that handle routines.

7.5.6.4 Test Mode -- The keyboard jumps into a test mode by command during production test. The keyboard transmits a special code to the system module to confirm the test mode. If the system module receives this code, it should send the byte 80 (hexidecimal) to continue. This causes a jump to power up.

7.5.6.5 Future Expansion -- Some keycodes are reserved for future use as special codes or keycodes. Table 7-5 lists these reserved codes.

7.5.7 Default Conditions

The LK201 has the following default conditions.

- Certain keyboard divisions have specific default modes. Some divisions default to the autorepeat mode. Therefore, they have an associated buffer that contains the default values for timeout and interval. Timeout is the amount of time that the keyboard waits before starting to autorepeat a character. The rate of autorepeating a character is called the interval. Table 7-5 shows the default modes and Table 7-6 shows the default rates in the four keyboard division autorepeat rate buffers.

- The volume levels for the keyclick and bell have an eight-step range. The default volume levels for the keyclick and bell are the third loudest.

- For the LK201 keyboard, the CTRL (control) key defaults to the no keyclick state.

7.5.7.1 Audio Volume -- Both keyclick and bell volumes are two decimals (010 binary) by default. The key in position C99 of the keyboard (the CTRL key in the LK201) does not generate a click unless enabled by the system module. The keys in position B99 and B11 (SHIFT keys on the LK201) never generate a keyclick.

Table 7-5 Keyboard Division Default Modes

Keyboard Division	Mode	AR Buffer
Main array	Autorepeat	Ø
Keypad	Autorepeat	Ø
Delete	Autorepeat	1
Cursor keys	Autorepeat	1
Return and tab	Down only	
Lock and compose	Down only	
Shift and control	Down/up	
Six basic editing keys	Down/up	

Table 7-6 Default Rates in Autorepeat Buffers

Buffer Number	Timeout (ms)	Internal (Hz)
Ø	5ØØ	3Ø
1	3ØØ	3Ø
2	5ØØ	4Ø
3	3ØØ	4Ø

7.6 SPECIFICATIONS

Functional

Electronics	8-bit microprocessor, 4 KB of ROM, 256 bytes of RAM, 4 LEDs, transducer
Cord	1.9 m (6 ft) coiled, 4-pin telephone-type modular connectors, plugs into display monitor (PN BCCØ1)
Keypad	Sculptured key array
Home row key height	3Ø mm (1.16 in) above desk top
Keys	1Ø5 matte textured finish keys
Main keypad	57 keys

Numeric keypad	18 keys
Special function keypad	20 keys, firmware and software driven
Editing keypad	10 keys
Spacing	1.9 cm (0.75 in) center to center (single width keys)
Wobble	Less than 0.5 cm (0.020 in)
Diagnostics	Power-up self-test, generates identification upon passing test

Physical

Height	5 cm (2.0 in) at highest point
Length	53.3 cm (21 in)
Width	17.1 cm (6.75 in)
Weight	2 kg (4.5 lb)

CHAPTER 8
MONITOR CIRCUITS

8.1 GENERAL

The monitor circuits and CRT (shaded areas of Figure 8-1), along with the yoke assembly, are responsible for actual display to the VT220 operator. The monitor circuits, located on the PS and monitor board, develop the drive potentials for both the CRT and the yoke assembly. The CRT generates an electron beam to provide actual visual output; the yoke assembly controls the positioning of the electron beam generated by the CRT.

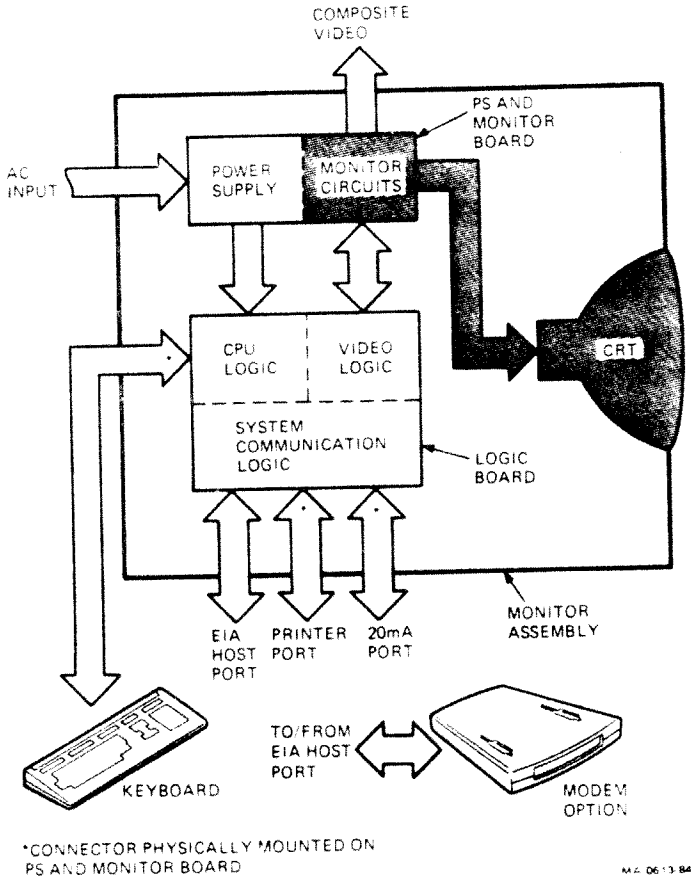


Figure 8-1 VT220 Series Terminal Functional Block Diagram

8.2 MAJOR CIRCUITS AND COMPONENTS

The monitor circuits (Figure 8-2) consist of the following components/circuits.

- Video amp
- Horizontal deflection circuit
- Flyback transformer
- Vertical deflection circuit
- Dynamic focus
- Brightness control
- CRT
- Yoke assembly
- +12 V filter

The yoke assembly is described in conjunction with the horizontal and vertical deflection circuit descriptions. No description is provided concerning the +12 V filter.

NOTE
Circuit illustrations provided are based on REV A of CS 5415651-0-1.

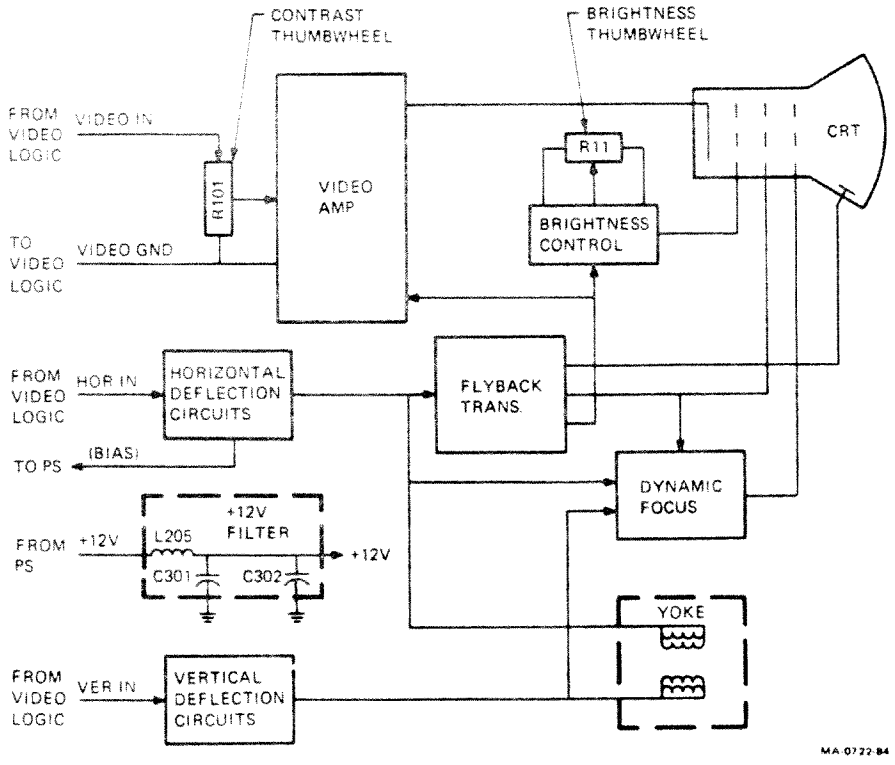


Figure 8-2 Monitor Circuits Block Diagram

8.2.1 Video Amplifier (Amp) Circuit

The video amp is a two-stage circuit converting video input from the video logic on the logic board into an emitter potential at the CRT.

The video amp (Figure 8-3) consists of the following circuits.

- Video input (R101-R103)
- Input stage (Q101 and R105)
- Output stage (Q102, C102, R109, and R108)
- Voltage divider (R106, R107, C150, and C151)
- Frequency compensation (C101 and R104)

Video input (a 2.5 V peak to peak signal, from 0 V to +2.5 V) is supplied to the base of Q101 through the contrast thumbwheel potentiometer (R101). C101 provides for frequency compensation when Q101 and Q102 are conducting. A +60 V input from the flyback transformer to R109 provides the voltage supply for emitter output to the CRT.

With no signal input, Q101 is off, and Q102 has a bias of 7.2 V on its base from R106 and R107. When a video signal is applied to the base of Q101, Q101 is turned on, forward biasing Q102. With Q102 on, the potential developed across R109 is dc coupled to the CRT emitter through R108 (R108 protects Q102 from transients that can occur as a result of high voltage arcing at the CRT anode).

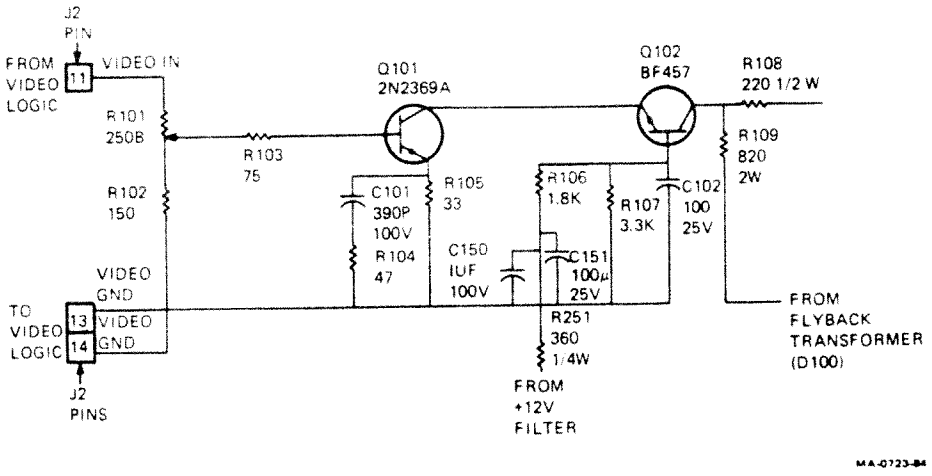


Figure 8-3 Video Amplifier Circuit Diagram

8.2.2 Horizontal Deflection Circuit

The horizontal deflection circuit develops the potentials supplied to the horizontal windings of the yoke assembly. These potentials provide for deflection of the CRT electron beam during horizontal trace and retrace times. Horizontal retrace time is defined by a horizontal sync signal input from the video logic (HOR IN).

The horizontal deflection circuit (Figure 8-4) consists of the following circuits.

- Horizontal processor
- Horizontal driver
- Horizontal output

8.2.2.1 Horizontal Processor Circuit -- The horizontal processor circuit provides the base control for defining trace and retrace periods. It develops a square wave output that is low during the second half of trace time, and high at all other times.

The horizontal processor circuit (Figure 8-5) consists of the following circuits.

- Horizontal processor device (E201)
- Horizontal sync input network (C200, R200, and R202)
- Horizontal hold network (R203, R204, C202, R205, R208, C203, and C204)
- Horizontal centering (phase) network (R215, R211, C208, and C207)
- Voltage divider network (R206, C206, C205, R210, and ZD1)

The horizontal hold network provides for adjustable control (R203) of the base frequency of the processor (E201). The horizontal centering network provides for adjustable control (R211) of the feedback from the horizontal output, which is compared by E201 against the HOR IN from R200, to determine the phase difference between the HOR IN and horizontal output circuit conditions. The voltage divider network defines the output duty cycle of E201 (20 us, $\pm$1us), with this duty cycle reflected as a square wave output from E201, pin 1, to the horizontal driver circuit (the output from E201, pin 1 is also sent to the pulse width modulator in the PS as a sync signal).

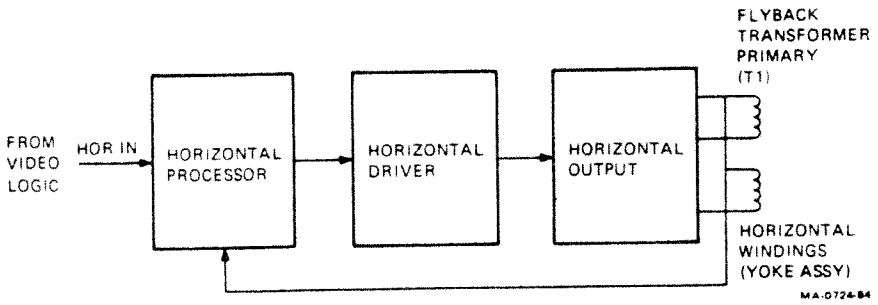


Figure 8-4 Horizontal Deflection Circuit Block Diagram

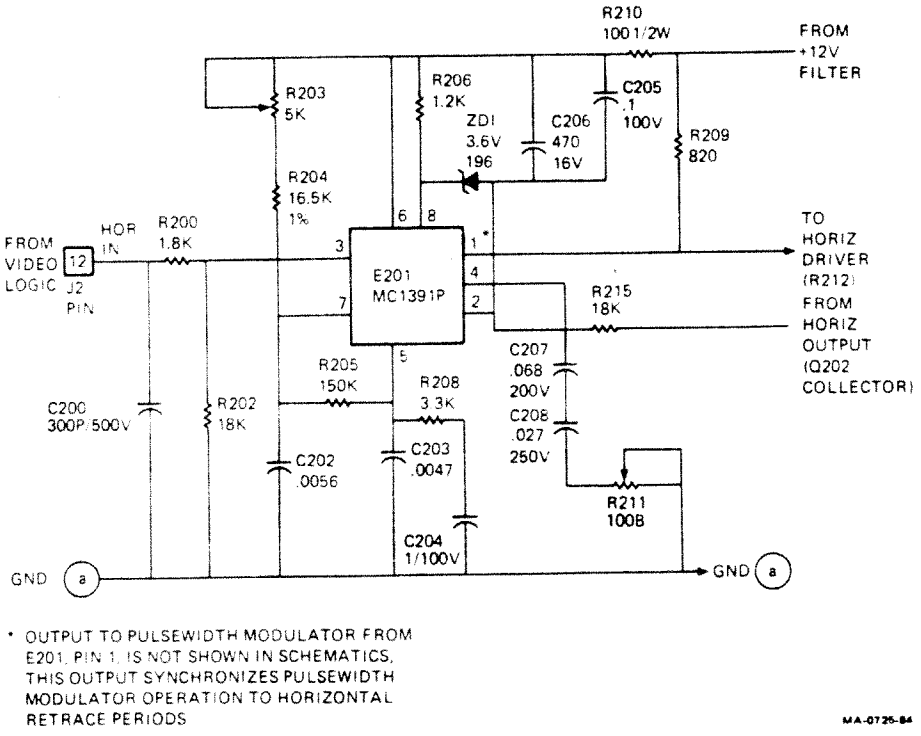


Figure 8-5 Horizontal Processor Circuit Diagram

8.2.2.2 Horizontal Driver Circuit -- The horizontal driver circuit converts the square wave input from the horizontal processor to a bias potential to the horizontal output circuit.

The horizontal driver circuit (Figure 8-6) consists of the following components/circuits.

- Driver (Q201)
- Base bias resistor (R212)
- Power source filter (C210)
- Output network (T201, R213, R214, and C211)

A high input is applied to the base of Q201 for horizontal retrace and first half of trace, a low for second half of trace. A high input forward biases Q201, placing 10 volts across the primary of T201, with the resulting secondary potential turning the horizontal output circuit off. When a low input turns Q201 off, current is reversed at the secondary of T201, turning on the horizontal output circuit.

R213 limits the current through Q201, and R214 and C211 limit voltage across this transistor.

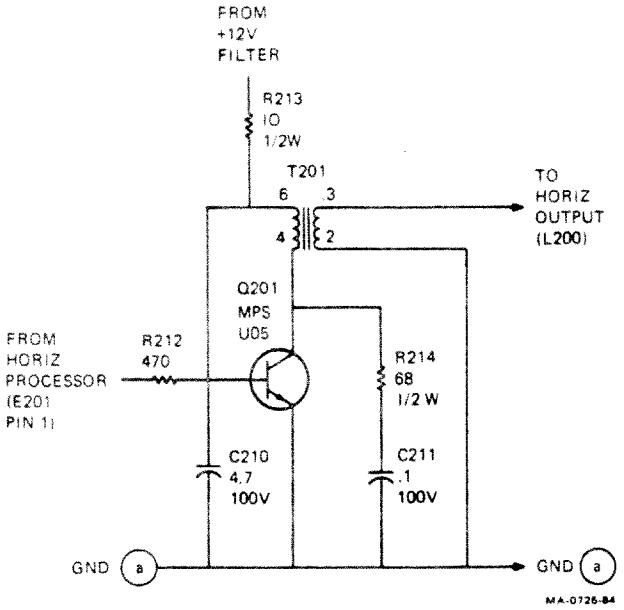


Figure 8-6 Horizontal Driver Circuit Diagram

8.2.2.3 Horizontal Output Circuit -- The horizontal output circuit is turned on and off by the horizontal driver circuit to generate the potential applied to the horizontal windings of the yoke assembly. The horizontal output circuit potential is also used to control flyback transformer activity (refer to description in section 8.2.4).

The horizontal output (Figure 8-7) consists of the following components/circuits.

- Input network (R216 and L200)
- Drive transistor (Q202)
- Collector voltage network (T1 primary, D201, C214, and R218)
- Charge pump circuit (C106, D101, D102, and C105)
- Horizontal linearity (L201, L202, R217, and C212)
- Yoke connector (J1)
- Output components (C216, C213, D200, R231, and C224)

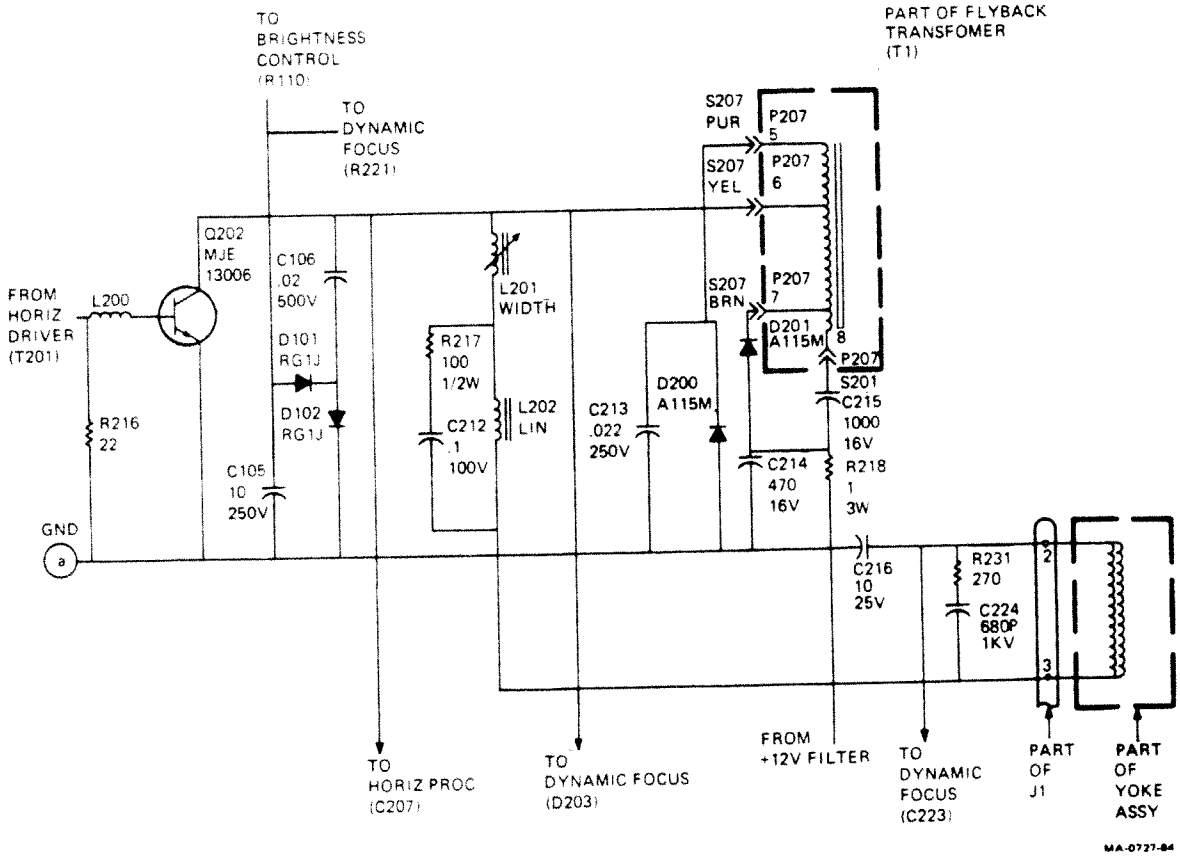


Figure 8-7 Horizontal Output Circuit Diagram

Q202 is turned on and off by current flow through the secondary of T201 in the horizontal driver circuit. During the second half of retrace, Q202 is turned on to saturation. At other times, Q202 is backbiased by T201, quickly turning Q202 off to minimize dissipation.

The Q202 collector voltage is sourced at +12 V and boosted through the collector voltage network to +15.5 V.

The charge pump circuit inverts the large positive voltage swings at the collector of Q202 into -170 V bias used by brightness control and dynamic focus circuits.

The horizontal linearity circuit provides adjustable (L201) control of current flow through the horizontal windings of the yoke assembly during trace and retrace scanning. L201 provides variable inductive reaction for adjusting current flow and varying the trace width. L202 provides nonlinear reactance that varies with changes in yoke current. R217 and C212 provide correction for nonlinearity caused by the decaying exponential rate of current increase in the yoke.

The output components switch yoke current back and forth between C213 and C216.

Figure 8-8 provides an illustration of the waveform developed at the horizontal windings of the yoke assembly during trace and retrace periods. Points T0 through T3 are identified in this figure as references within the waveform. Figures 8-9 through 8-12 provide illustrations and descriptions of the current flow conditions that result in the waveform shown in Figure 8-8.

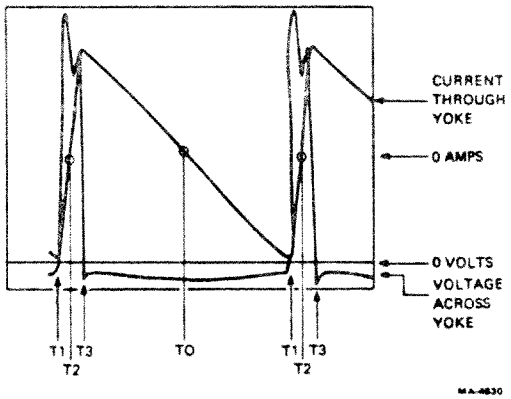
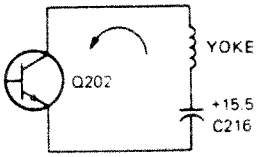


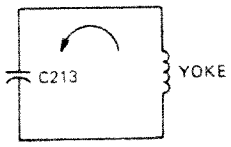
Figure 8-8 Horizontal Deflection Waveform



ACTIVITY DESCRIPTION
INITIAL CONDITION: 1. Q202 OFF; 2. CURRENT THROUGH YOKE AT ZERO; 3. C216 CHARGED TO +15.5V. ACTION: 1. Q202 TURNED ON; 2. CURRENT STARTS FLOWING THROUGH YOKE SUPPLIED BY CONSTANT VOLTAGE AT C216; 3. CURRENT INCREASES IN LINEAR FASHION THROUGH YOKE, DEFLECTING BEAM TO RIGHT OF THE SCREEN; 4. INDUCTIVE ENERGY IS STORED IN YOKE; 5. C213 IS GROUNDED BY SATURATED Q202.

MA-0729-84

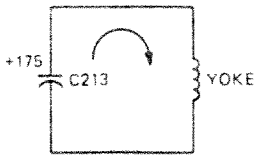
Figure 8-9 Horizontal Trace: Scan from Center to Right Side of Screen (TØ Time)



ACTIVITY DESCRIPTION
INITIAL CONDITION: 1. Q202 SATURATED; 2. CURRENT THROUGH YOKE AT MAXIMUM; 3. C216 CHARGED TO 0V. ACTION: 1. Q202 TURNED OFF; 2. YOKE CURRENT CONTINUES FLOWING DUE TO INDUCTIVE INERTIA AS STORED MAGNETIC FIELD COLLAPSES; 3. C213 QUICKLY CHARGES TO HIGH VOLTAGE; 4. HIGH VOLTAGE AT C213 CAUSES FAST REDUCTION IN CURRENT FLOW THROUGH YOKE; 5. CRT BEAM IS QUICKLY MOVED TO CENTER OF THE SCREEN (T0).

MA-0730-84

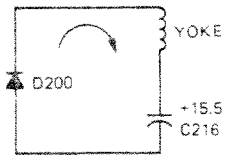
Figure 8-10 Horizontal Retrace: Move to Center from Right Side (T1 Time)



ACTIVITY DESCRIPTION
INITIAL CONDITION: 1. Q202 OFF; 2. CURRENT THROUGH YOKE AT ZERO; 3. C213 CHARGED TO +175V. ACTION: 1. C213 VOLTAGE DISCHARGES THROUGH YOKE; 2. QUICK RISE IN YOKE CURRENT MOVES BEAM TO LEFT SIDE OF SCREEN.

MA-0731-84

Figure 8-11 Horizontal Retrace: Move to Left Side from Center (T2 Time)



ACTIVITY DESCRIPTION
INITIAL CONDITION: 1. Q202 OFF; 2. CURRENT THROUGH YOKE AT MAXIMUM; 3. C213 DISCHARGING; 4. VOLTAGE ACROSS C216 EQUALS 0V. ACTION: 1. INDUCTIVE INERTIA FORCES TOP OF YOKE SLIGHTLY NEGATIVE; 2. NEGATIVE FROM YOKE FORWARD BIASES D200 PROVIDING FOR CURRENT PATH THROUGH C216; 3. YOKE CURRENT GRADUALLY DECREASES AS MAGNETIC FIELD COLLAPSES, DISCHARGING INTO C216; 4. BEAM MOVES IN LINEAR FASHION TO CENTER OF THE SCREEN.

MA-0732-84

Figure 8-12 Horizontal Trace: Scan to Center from Left Side of Screen (T3 Time)

8.2.3 Flyback Transformer Circuit

The flyback transformer circuit provides high voltage anode (12,500 V), cutoff grid (+750 V) and variable focus grid potentials to the CRT, as well as operational voltage (+60 V) for the video amp and brightness control circuits.

The flyback transformer circuit (Figure 8-13) consists of the following components/circuits.

- Flyback transformer (T1)
- +60 V output (D100 and L204)
- Cutoff grid bias network (L203, D202, R219, C219, R224, and C220)
- Focus grid bias network (R220-R221)

The outputs from the flyback transformer are controlled by Q202 in the horizontal output portion of the horizontal deflection circuit. When Q202 cuts off, a 175 V pulse is passed across the primary of T1. This pulse results in the anode, cutoff and focus, and video amp and brightness control voltage outputs.

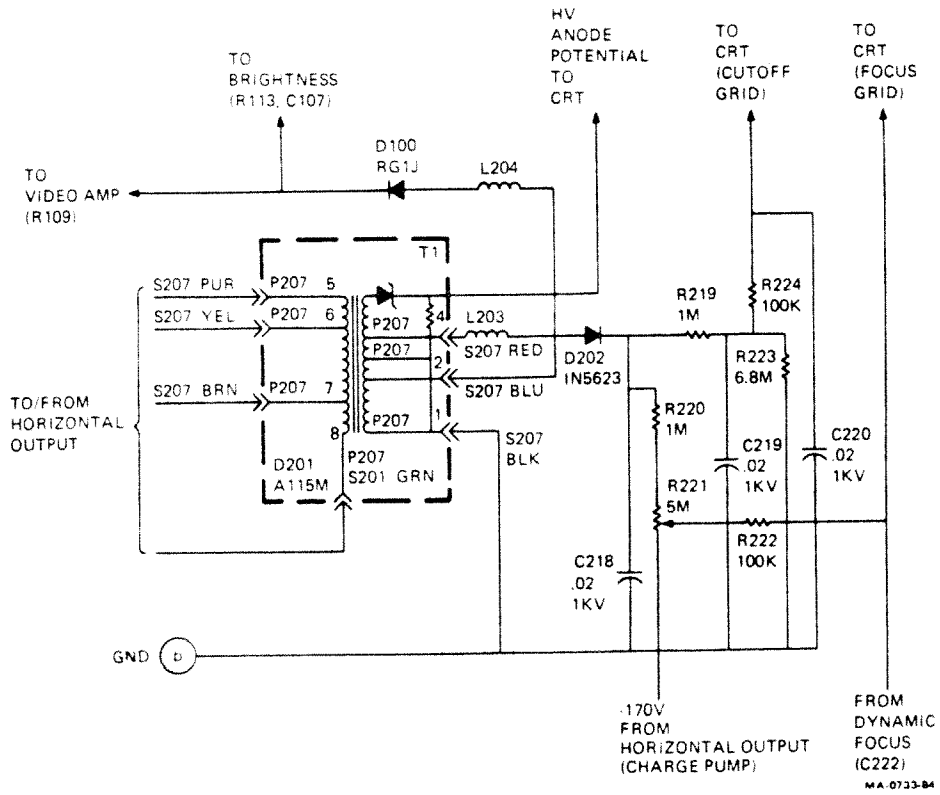


Figure 8-13 Flyback Transformer Circuit Diagram

The anode output is rectified internal to T1, and filtered by graphite coatings at the CRT end of the anode wire, which can connect or disconnect only at the CRT end.

The operational voltage (+60 V) used by the video amp and brightness control circuits is output from pin 2 of T1 and regulated and filtered by D100 and L204.

The cutoff grid potential is taken from pin 4 of T1 and regulated by L203 and D202. The regulated potential (+750 V) is routed to the CRT cutoff grid via a voltage divider network (R219 and R224, filtered by C219 and C220), and to R220 in the dynamic focus circuit.

The focus grid potential is picked off of the focus potentiometer (R221) with a voltage range at R221 from +500 V to -170 V. The positive range is developed from the same T1 output used for the cutoff grid potential, while the negative range is developed from input from the charge pump circuit in the horizontal output circuit. The actual focus grid value sent to the CRT is developed across R222 in conjunction with the value supplied by the dynamic focus circuit (refer to section 8.2.5).

8.2.4 Vertical Deflection Circuit

The vertical deflection circuit develops the potentials supplied to the vertical windings of the yoke assembly. These potentials provide for deflection of the CRT electron beam during vertical trace and retrace times.

Vertical deflection is a linear current rise to the vertical yoke windings during a complete scan of the screen (each scan line of the scan defined by horizontal trace and retrace activity). A complete scan of the screen occurs at a rate of 60 vertical trace periods per second. Vertical retrace time is defined by a vertical sync signal input from the video logic (VER IN). VER IN results in a steep drop in the current supplied to the vertical yoke windings, returning the placement of the CRT beam to the top of the screen.

The vertical deflection circuit (Figure 8-14) consists of the following circuits.

- Vertical processor
- Vertical output

8.2.4.1 Vertical Processor Circuit -- The vertical processor circuit provides the base control for defining trace and retrace periods. It develops a ramping output used by the vertical output to move the CRT beam from the top to the bottom of the screen through linear increase of current flow through the vertical windings of the yoke assembly.

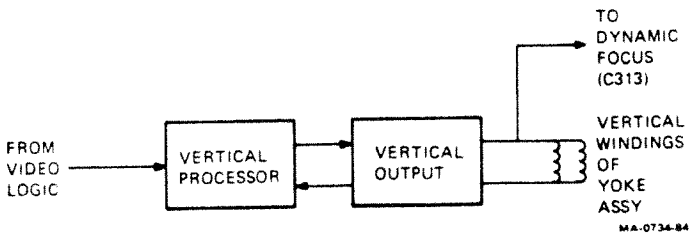


Figure 8-14 Vertical Deflection Circuit Block Diagram

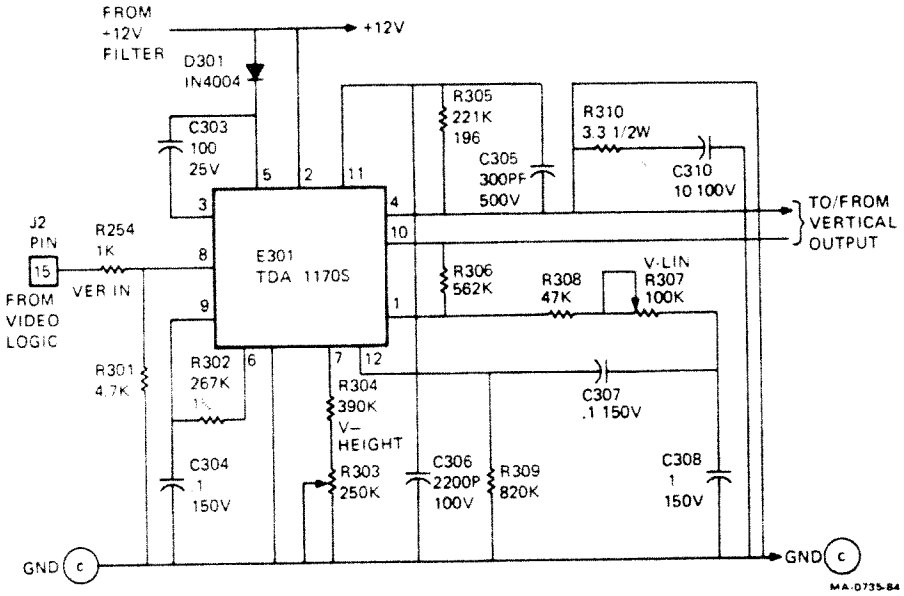


Figure 8-15 Vertical Processor Circuit Diagram

The vertical processor circuit (Figure 8-15) consists of the following components/circuits.

- Vertical processor device (E301)
- Vertical sync input (R254 and R301)
- Voltage regulator (D301 and R301)
- Oscillator synchronizer (R302 and C304)
- Current regulation (R303 and R304)
- Ramp sensor (R306)
- Power amp stabilization network (R305, R310, C305, C306, and C310)
- Vertical linearity control (R308, R307, C307, and C308)

The vertical sync input initiates retrace each time it goes low (60 times per second). However, the E301 is capable of free-running trace and retrace, in the event no retrace sync signal is sensed from the video logic. R302 and C304 define E301 internal free-running oscillation at 60 Hz (±1 Hz).

At the start of a vertical trace, E301 outputs a voltage potential on pin 4. This potential is stabalized and output to the vertical output circuit. Feedback from that circuit is input to E301 at pin 10. This feedback is applied across R306 and compared with the adjustable (R307) vertical linearity value at pin 1 of E301. The feedback at pin 10, and the value at pin 1 are used by E301 to monitor gain and to compensate for any drift in output voltage value.

The output potential at pin 4 of E301 is ramped upward throughout the trace period. At vertical retrace, the output is returned to zero, removing the ramped potential from the vertical output circuit.

Current regulation on the output of E301 is controlled by an adjustable regulator (R303), which can increase or decrease the height of the area of the screen scanned during a vertical trace.

8.2.4.2 Vertical Output Circuit -- The vertical output circuit develops the potentials used to drive current through the vertical windings of the yoke assembly.

The vertical output circuit (Figure 8-16) consists of the following circuits.

- Voltage divider network (R311-R314 and C309)
- Yoke current drive components (C311, C312, R317, and J1)

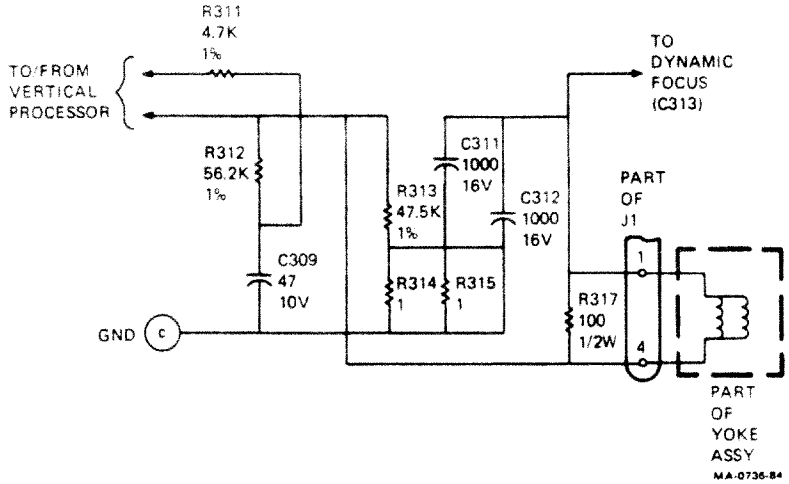


Figure 8-16 Vertical Output Circuit Diagram

Output from the vertical processor circuit is applied to the voltage divider network. The resulting voltage drop caused by current flow through R314 and R315 is reflected back to the vertical processor circuit at R313.

During vertical trace, the output capacitors are incrementally charged, with a resulting incremental flow of current through the vertical windings of the yoke assembly. This moves the CRT beam from top to bottom of the screen during the trace.

At the start of retrace, the input from the vertical processor returns to zero. This results in C311 and C312 discharging through the vertical windings of the yoke assembly. This reverse in current flow quickly moves the CRT beam back to the top of the screen.

8.2.5 Dynamic Focus

The CRT beam travels further when deflected to a corner of the screen than when scanning near the center. The dynamic focus circuit optimizes focus in the corners.

The dynamic focus circuit (Figure 8-17) consists of the following components/circuits.

- Operating voltage network (D203 and C221)
- Horizontal component coupling (C223 and R230)
- Vertical component coupling (C313 and R316)
- Focus transistor (Q203)
- Bias resistors (R225-R229)
- Output coupler (C222)

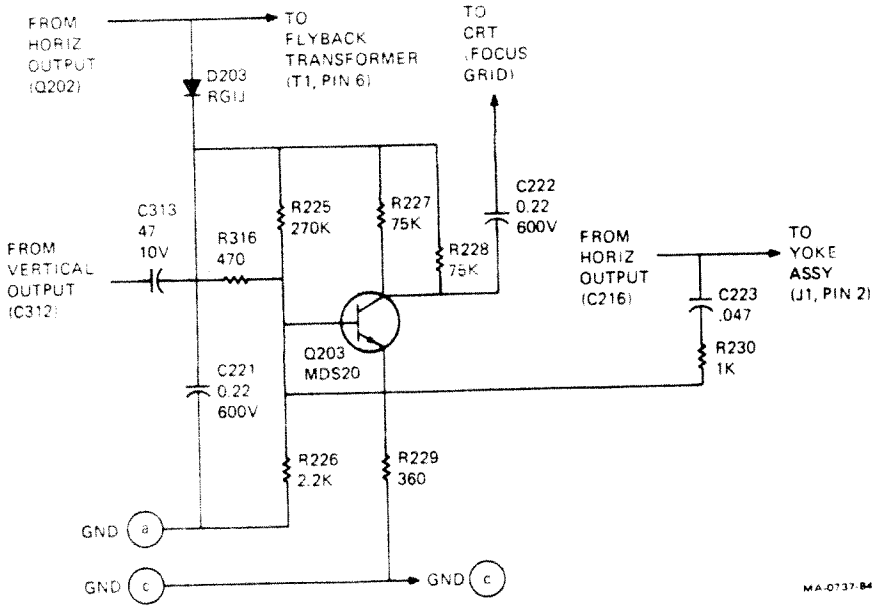


Figure 8-17 Dynamic Focus Circuit Diagram

D203 and C221 rectify and filter an operational voltage input of +160 V supplied to the base and collector of Q203 through the bias resistors.

The horizontal component of the focus value is coupled to the base of Q203 by C223 and R230, and developed from the charge condition of C216 (refer to section 8.2.2.3, and Figures 8-9 through 8-12) during scanning. The vertical component of the focus value is coupled to the base of Q203 by C313, and developed by the charge condition of C311 and C312 during vertical deflection (refer to section 8.2.4). The output resulting from the biasing of Q203 is coupled to the focus grid potential developed by the flyback transformer circuit through C222.

8.2.6 Brightness Control

The brightness control circuit allows the brightness of the display at the CRT to be adjusted by the operator.

The brightness control circuit (Figure 8-18) consists of the following components/circuits.

- Reference voltage network (D103, R113, C104, and C107)
- Voltage divider (R110-R112)
- Bypass capacitor (C103)

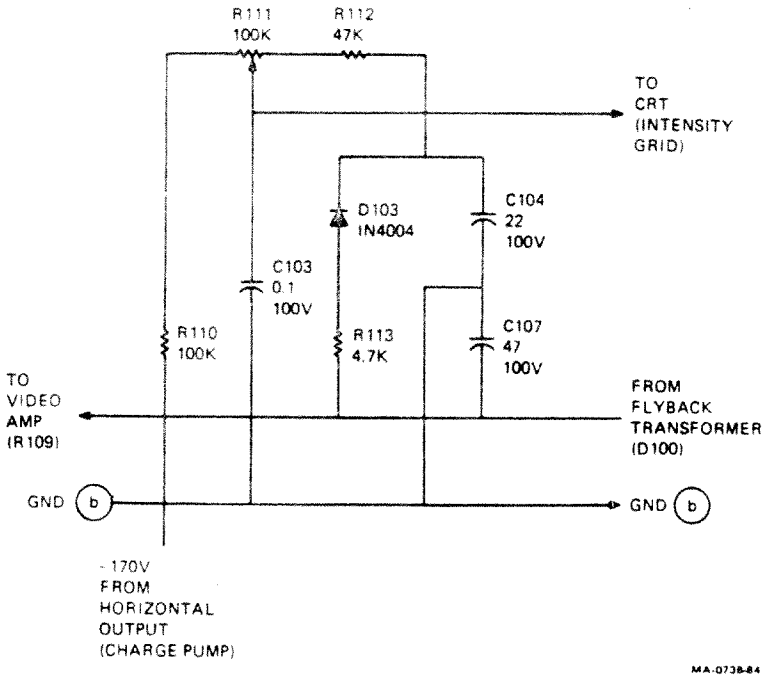


Figure 8-18 Brightness Control Circuit Diagram

The voltage divider network, which includes the brightness thumbwheel (R111), provides for a variable bias (from +9.5 V to -80 V) to the intensity grid of the CRT. The bias is developed from -170 V input from the charge pump in the horizontal output circuit (refer to section 8.2.2.3) and +60 V input to the reference voltage network from the video amp operational voltage developed by the flyback transformer.

C103 provides for bypassing transients that occur as a result of internal CRT arcing, as well as for bypassing video signals from the intensity grid that would interfere with the frequency response of the CRT cathode.

8.2.7 CRT Device

The CRT device (Figure 8-19) provides for actual output to the operator. Video input to the monitor circuits is converted to emitter potential to the CRT emitter. Focus, intensity, and cutoff potentials applied to the three grids of the CRT inhibit (cut off input from flyback transformer circuit), refine (focus input from the focus circuit of the flyback transformer coupled to the value developed by the dynamic focus circuit), and control the brightness (intensity input from brightness control) of the display generated by the CRT beam from the emitter potential provided by the video amp.

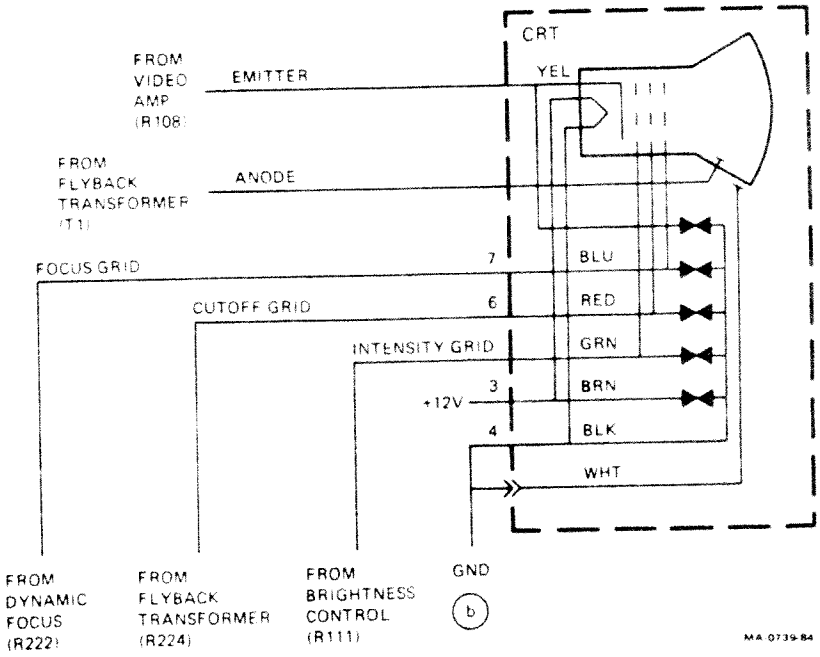


Figure 8-19 CRT Device

CHAPTER 9
POWER SUPPLY

9.1 GENERAL

The power supply (shaded area of Figure 9-1) converts ac input to dc voltages required for VT220 terminal operation.

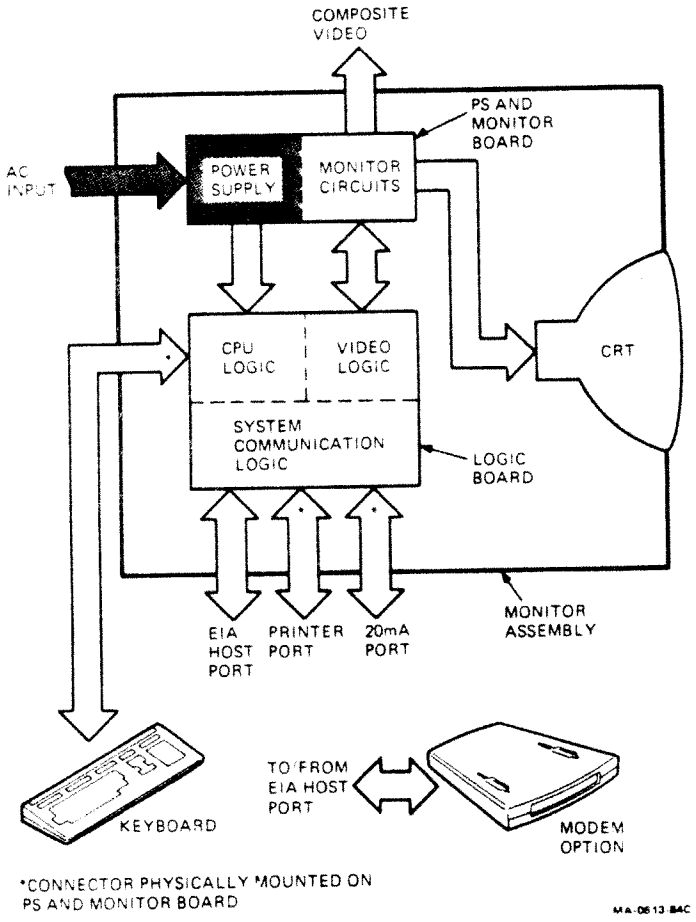


Figure 9-1 VT220 Series Terminal Functional Block Diagram

9.2 MAJOR CIRCUITS AND COMPONENTS

The power supply (Figure 9-2) consists of various components and circuits, including circuits that physically mount on the logic board.

- AC input components
- AC conversion circuits
- Interboard connectors (J1 and J2)
- DC input circuits
- DC power ok

NOTE
Circuit illustrations in this chapter are based on REV A of CS 5415651-Ø-1.

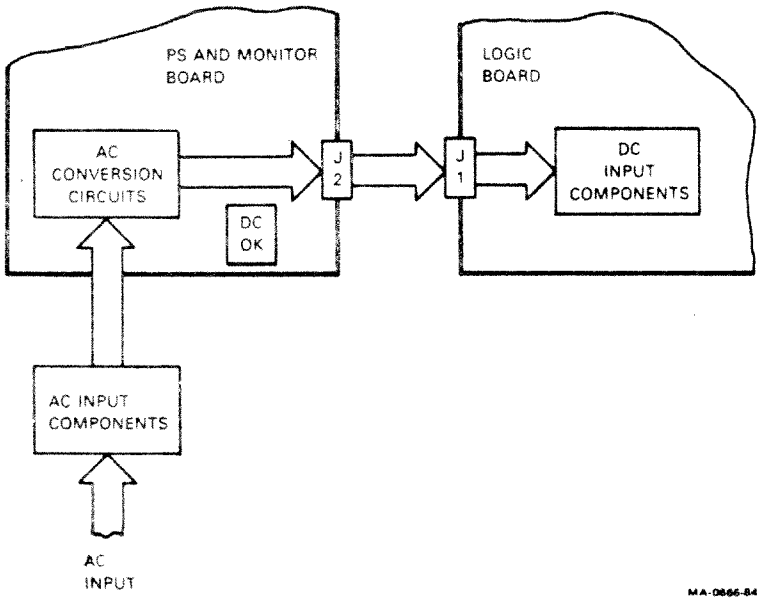


Figure 9-2 Power Supply Block Diagram

9.2.1 AC Input Components

The ac input components provide for ac input, including voltage range (115 Vac or 230 Vac) selection. Figure 9-3 shows the following ac input components.

- EMI filter -- filters ac input which is connected by power cord directly into the EMI filter.
- S1 -- is the power on/off switch (S1 is shown in off position in Figure 9-3).
- S2 -- is the voltage selection switch (S2 is shown at 115 Vac selection in Figure 9-3).
- F1 -- is a 2, 250 Vac input line fuse.
- Chassis ground lug -- provides ground connection of ac input ground from LMI filter.

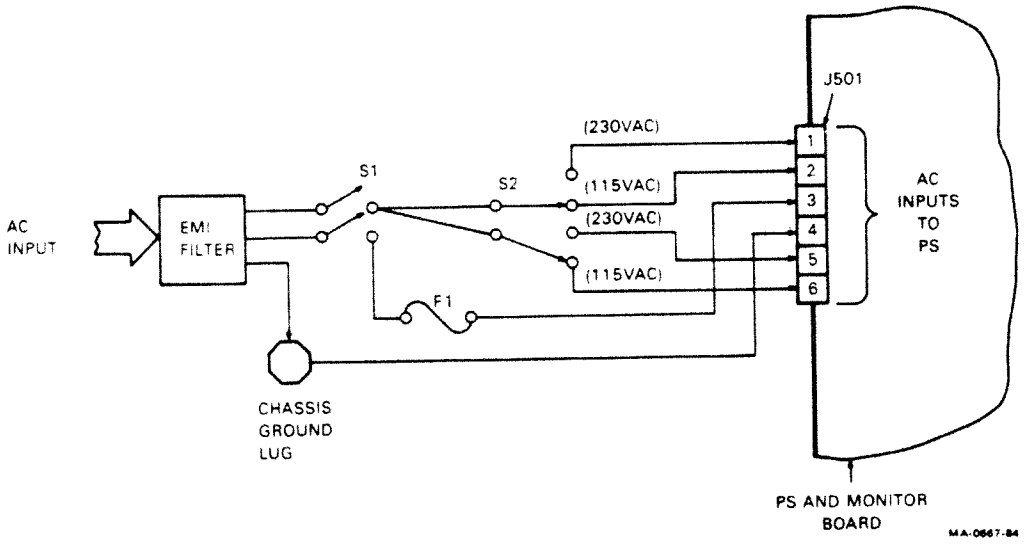


Figure 9-3 AC Input Components Block Diagram

9.2.2 AC Conversion Circuits

The ac conversion circuits convert ac input into three dc voltage outputs: +5 V, +12 V, and -12 V. The ac conversion circuits, (Figure 9-4) which are all located on the PS and monitor board, are as follows.

- J501 -- is the connector for ac input from voltage selectionswitch.
- +12 V start up -- provides operational voltage potential for overcurrent protect circuit, and also provides initial power for pulse width modulator during power up sequence (until +12 V circuit is operational).
- Input rectification -- consists of components responsible for rectification and filtering of ac input into the pulse width modulator controlled switching transistor circuit, which provides ac input to primary of T501.

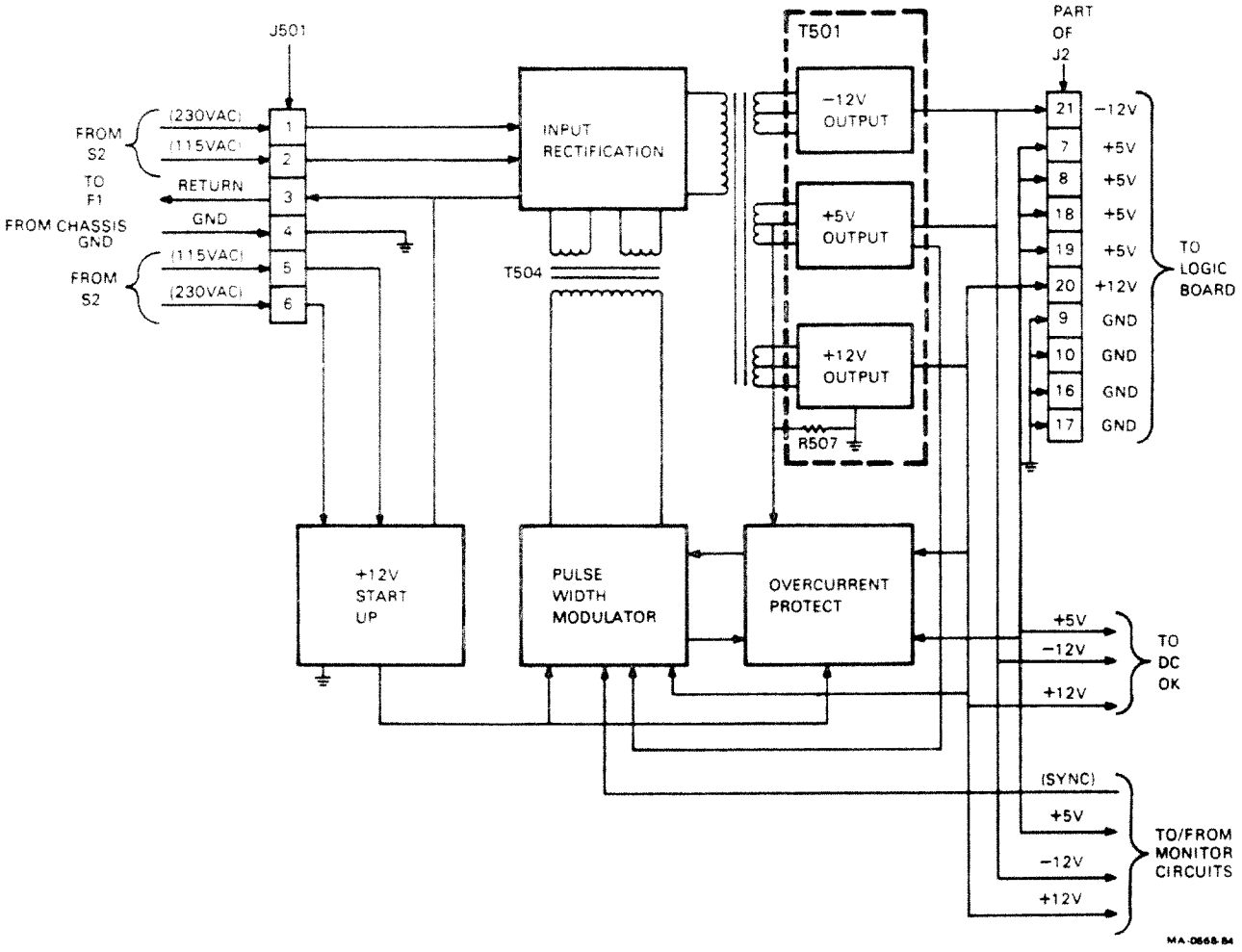


Figure 9-4 AC Conversion Circuits Block Diagram

- T501 -- transforms regulated ac input into secondary voltages used by the dc output circuits to generate the required dc potentials.
- DC output circuits -- generate the dc potential outputs (+12 V, +5 V, and -12 V).
- Part of J2 -- are the pins of interconnection between P/S and monitor board and logic board used for routing of dc.
- Overcurrent protect -- monitors for +5 V/+12 V overcurrent and +5 V overvoltage conditions.
- Pulse width modulator -- monitors overcurrent protect and dc output circuits conditions to control width of ac pulses supplied to T501 by switching transistor network within the input rectification circuit.
- T504 -- provides means for pulse width modulator to control width of rectifed ac pulses supplied to T501.

Table 9-1 provides specifications for the ac inputs. Figure 9-4 shows the pinouts for J501 and J2. Each of the ac conversion circuits are described separately (with the exception of components J501, J2, T501, and T504, which are discussed only as they relate to the other circuits).

Table 9-1 Input Voltage Specifications

Voltage	Specification	Value
115 Vac	Nominal voltage	120 Vac
	Minimum voltage	87 V rms
	Maximum votage	134 V rms
	Input line current	1 A rms (max.)
	Line frequency	47-63 Hz
	Power factor	(watts) -- (rms V X rms A) > 0.55
	Inrush current	Surge current at first application of input voltage may be reached for 1/2 cycle of input line, with repetitive peaks of exponentially decaying amplitude for up to 10 more cycles.
	Peak inrush	25 A (Thermisters cold)
	Input power	60 watts (max.) at full rated dc output load of 40 watts.
	Efficiency	0.65 (min.) output power to input power ratio.
	Undervoltage	Provides minimum of 10 millisecond hold-up at 90 V rms during power outage.
	Overvoltage	150 Vac for 1 second (max.)

Table 9-1 Input Voltage Specifications (Cont)

Voltage	Specification	Value
	Transients	Low energy transient of 300 V peak spike with no more than 0.2 watt-seconds of energy per spike; High energy transient of 1 kV peak spike with no more than 2.5 watt-seconds of energy per spike.
230 Vac	Nominal voltage	220 Vac-240 Vac
	Minimum voltage	174 V rms
	Maximum voltage	268 V rms
	Input line current	0.5A rms (max.)
	Line frequency	47-63 Hz
	Power factor	(watts) -- (rms V X rms A) > 0.55
	Inrush current	Surge current at first application of input voltage may be reached for 1/2 cycle of input line, with repetitive peaks of exponentially decaying amplitude for up to 10 more cycles.
	Peak inrush	25 A (Thermisters cold)
	Input power	120 watts (max.) at full rated dc output load of 77 watts.
	Efficiency	0.65 (min.) output power to input power ratio.
	Undervoltage	Provides minimum of 5 millisecond hold-up at 180 V rms during power outage.
	Overvoltage	300 Vac for 1 second (max.)
	Transients	Low energy transient of 300 V peak spike with no more than 0.2 watt-seconds of energy per spike; High energy transient of 1 kV peak spike with no more than 2.5 watt-seconds of energy per spike.

9.2.2.1 +12 V Start Up Circuit -- The +12 V start up circuit (Figure 9-5) consists of the following components/circuits.

- AC input transformer (T502)
- Rectifier (E501)
- Filter capacitors (C501 and C502)
- +12 V regulator components (E502, D501, and D502)

The +12 V start up potential provides an operational potential for the comparator within the overcurrent protect circuit. The +12 V start up potential is also supplied to the pulse width modulator where it provides initial power for operation of this circuit until the +12 V dc circuit is operational.

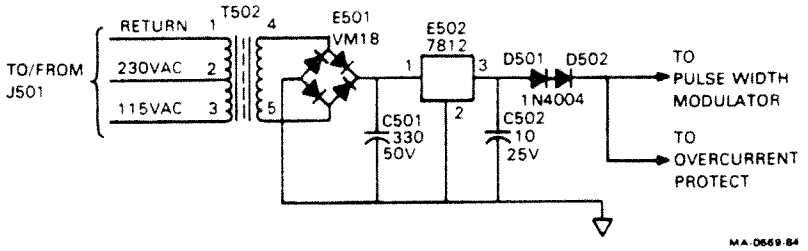


Figure 9-5 +12 V Start Up Circuit Diagram

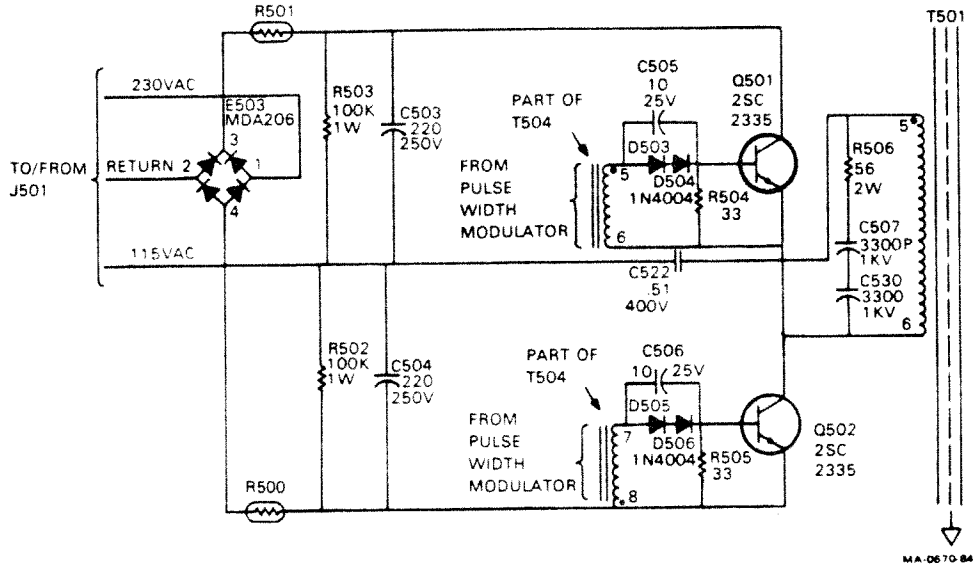


Figure 9-6 Input Rectification Circuit Diagram

9.2.2.2 Input Rectification Circuit -- The input rectification circuit rectifies and filters the ac input to produce positive, negative, and neutral "dc type" signals. These signals are then used as a power supply for two switching transistors. The switching transistors produce an ac signal applied across the primary of T501, with the width of the ac signal controlled by input to the switching transistors from the pulse width modulator.

The input rectification circuit (Figure 9-6) consists of the following components/circuits.

- Rectifier (E503)
- Thermistors (R500 and R501)
- Filter networks (R503 and C503, R502 and C504, and R506, C507, and C530)
- Switching transistor networks (Q501 and Q502, and related components)

Q501 and Q502 are coupled to the pulse width modulator in reverse polarity via T504. Current is induced in T504 by the pulse width modulator, with the effect on the switching transistors determined by the direction of the current flow. When current in T504 is induced from pin 6 to pin 5 and pin 7 to pin 8, back biasing of Q502 occurs, turning this transistor off, which results in Q501 being turned on (with charge of C505 speeding up the transition). When current is the reverse, Q501 is back biased and turned off, with Q502 turned on (with charge of C506 speeding up the transition). The result is an ac signal to the T501 primary controlled by the width of pulses output from E505, the pulse width modulator.

9.2.2.3 DC Output Circuits -- The dc output circuits (Figure 9-7) consists of the following components/circuits.

- -12 V output circuit containing a rectifier (D507 and D508), filter networks (L501 and C508, and C509, R525, and R526), and a voltage regulator (E504).
- +5 V output circuit containing a rectifier (D509), and filter networks (T503 and C510, and L502, C523, and C513).

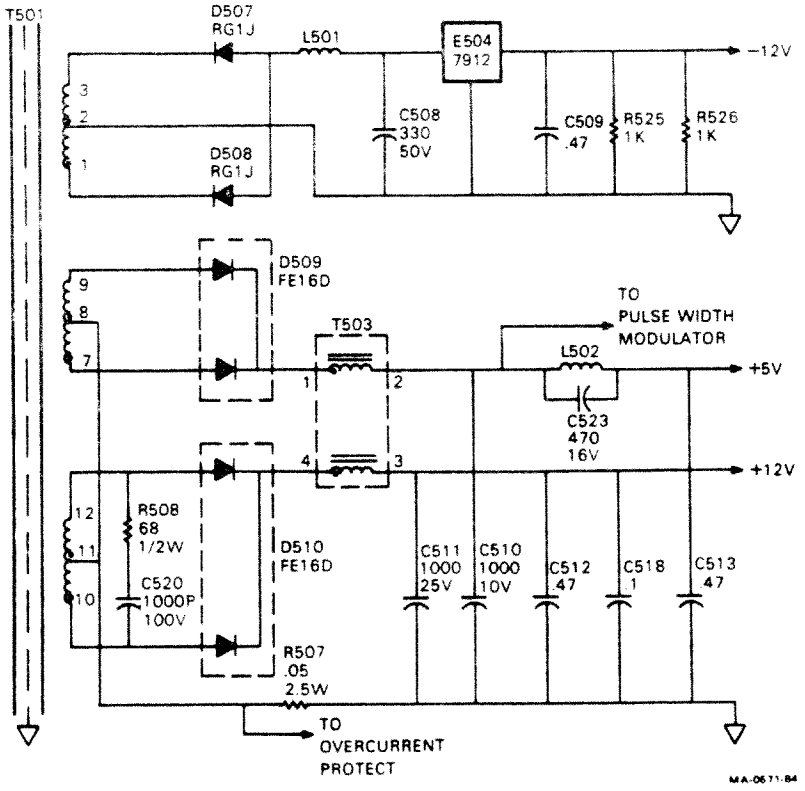


Figure 9-7 DC Output Circuits Diagram

- +12 V output circuit containing a rectifier (D510), and filter networks (R508 and C520, and T503, C511, C512, and C518).

- Sensing resistor (R507).

DC outputs are generated from T501 secondary potentials and output to the logic board (via J2), monitor circuits, and the dc ok circuit. In addition, +12 V, along with an output from the +5 V circuit, is sent to the pulse width modulator, and +5 V, along with the sensing resistor potential, is sent to the overcurrent protect circuit. These outputs are monitored to control the pulse width of the T501 primary potential to compensate for any overvoltage, undervoltage, or overcurrent condition.

Table 9-2 provides specifications for the three dc outputs.

Table 9-2 Output Voltage Specifications

Voltage	Specification	Value
+5 V	Nominal output	+5.0 V
	Minimum load	1 A
	Maximum load	2.2 A
	Ripple	150 MV p-to-p for < 66 KHz (max) (see note 1)
	Noise	1% of peak for > 100 KHz (noise is superimposed on ripple) (see note 1)
	Total regulation	±5.0%
	Static line reg.	±5.0%
	Static load reg.	±5.0%
	Long term stability	0.1%/1000 hr (see note 2)
	Thermal Drift	±0.025% per degree centigrade (see note 2)
	Dynamic load reg.	+2.2% (see note 3)
	Overload protection	Current limit with foldback (limit point of 6.5 A max. and foldback at 3.3 A max.)

NOTES:

1. Ripple and noise must be measured with wide band oscilloscope such as Tektronix P6046 differential probe, with scope set for >100 MHz bandwidth, and specification applies only to repetitive voltage variations occuring while operating with constant input voltage and fixed load.

2. Long term stability and thermal drift specifications apply after five minute warm up and are measured at the dc distribution buses with an averaging meter.

3. Dynamic load regulation is measured in +25% load steps from a starting point of 75% of full load, with measurements made at power suppy terminals.

Table 9-2 Output Voltage Specifications (Cont)

Voltage	Specifications	Value
+12 V	Nominal output	+12 V
	Minimum load	1 A
	Maximum load	2.2 A
	Ripple	240 MV p-to-p for < 66 kHz (max) (see note 1)
	Noise	1% of peak for > 100 kHz (noise is superimposed on ripple) (see note 1
	Total regulation	±5.0%
	Static line reg.	±0.5%
	Static load reg.	±0.2%
	Long term stability	0.1%/1000 hr (see note 2)
	Thermal drift	±0.025% per degree centigrade (see note 2)
	Dynamic load reg.	+2.0% (see note 3)
	Overload protection	Current limit with foldback (limit point of 6.5 A max. and foldback at 3.3 A max.)
-12 V	Nominal output	-12 V
	Minimum load	0.0 A
	Maximum load	0.2 A
	Ripple	240 MV p-to-p for < 66 kHz (max) (see note 1)
	Noise	1% of peak for > 100 kHz (noise is superimposed on ripple) (see note 1)
	Total regulation	±5.0%
	Static line reg.	±0.5%
	Static load reg.	±1.0%
	Long term stability	0.1%/1000 hr (see note 2)
	Thermal drift	±0.025% per degree centigrade (see note 2)
	Dynamic load reg.	±2.0% (see note 3)
	Overload protect	Internal current limit by regulator

9.2.2.4 Overcurrent Protect Circuit -- The overcurrent protect circuit monitors the +5 V dc output to sense an undervoltage condition, and the dc output circuits sensing resistor (R507) potential to sense overcurrent condition resulting from a short in either the +5 V or +12 V output circuits.

The overcurrent protect circuit (Figure 9-8) consists of the following circuits.

- Summing network (R514, R523, and R524)
- Voltage comparator components (E506 and R509)

The sensing resistor potential, +5.1 V reference voltage input from the pulse width modulator, and +5 V input are summed to provide biasing to the plus input of the comparator. This bias is reflected in the output from the comparator, which is sent to the pulse width modulator. If overcurrent or overvoltage conditions exist, the output of the comparator will go low, caused by a negative value present at the comparator's positive input. This will cause the pulse width modulator to output a minimum pulse width, effectively shutting off the power supply to prevent further damage.

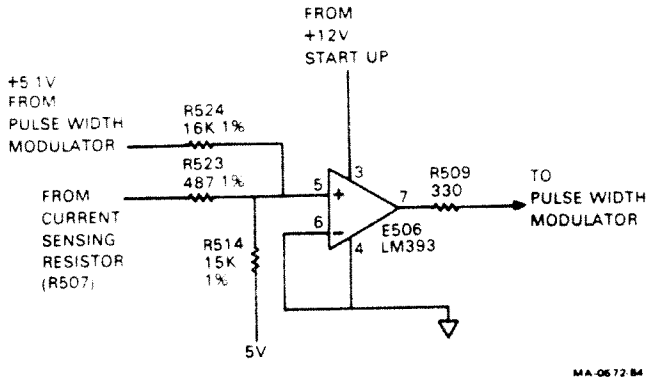


Figure 9-8 Overcurrent Protect Circuit Diagram

9.2.2.5 Pulse Width Modulator Circuit -- The pulse width modulator monitors the +12 V output potential, along with inputs from the +5 V output, overcurrent protect, and horizontal processor in the monitor circuits, to control the width and frequency of pulses passed through the primary of T501 by biasing of the switching transistors in the input rectification circuit (via T504).

The pulse width modulator (Figure 9-9) consists of the following components/circuits.

- Pulse width modulator device (E505)
- Power input components (D511 and C521)
- Summing network (R517-R520)
- Pulse control output network (R510, D512, and D513)
- Oscillator synchronization input network (R54, C54, and D54)
- Oscillator frequency control components (R511, R527, C514-C516)
- Biasing components (R515 and R516)
- Start-up delay capacitor (C517)

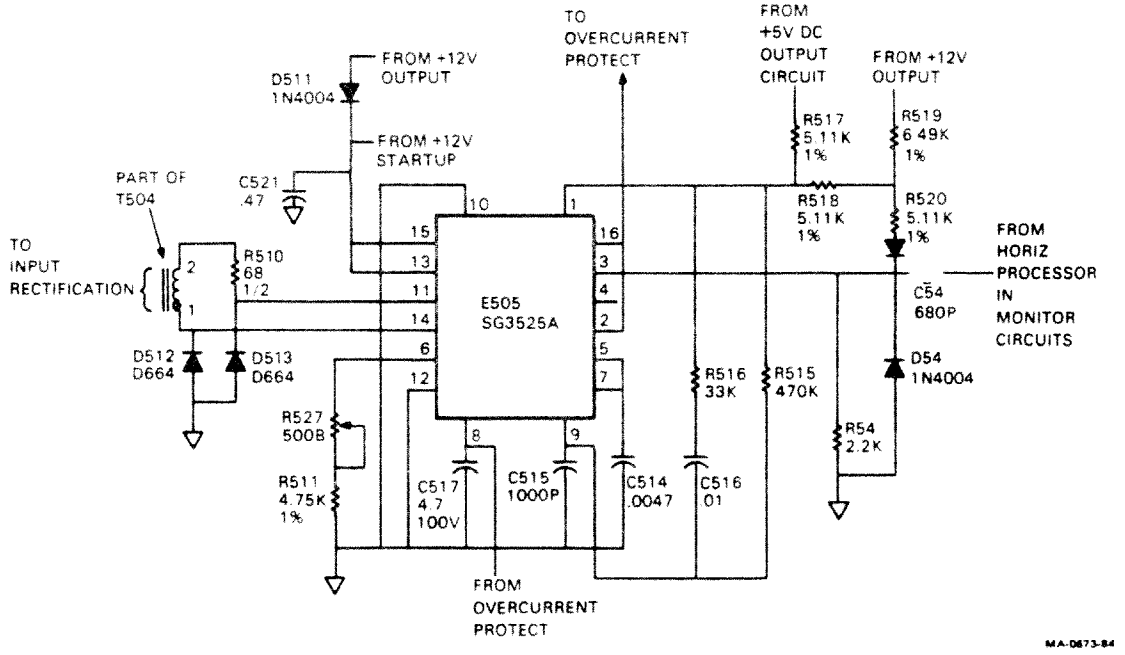


Figure 9-9 Pulse Width Modulator Circuit Diagram

The pulse width modulator circuit generates two outputs: Biasing to the switching transistors in the input rectification circuit (via T504) and +5.1 V reference voltage to the overcurrent protect circuit.

The input to the pulse width modulator from the horizontal processor in the monitor circuits is a sync input to the pulse width modulator's internal oscillator. This input synchronizes modulator operation to horizontal retrace time.

The switching transistor bias output is directly affected by the biasing supplied to the pulse width modulator device by the overcurrent protect circuit (pin 8 input to modulator), summing network input (developed from +12 V potential summed with input from +5 V output circuit), and the power sensing components.

The power sensing components provide for operational voltage input from either the +12 V start up circuit (during power up situations), or from the +12 V dc output circuit (when fully operational following a power up). C517 inhibits operation during the power up sequence by holding pin 8 of E505 low until this capacitor can be charged up. This prevents operation of the pulse width modulator during the time that initial surge conditions may occur.

9.2.3 DC OK Circuit

The dc ok circuit provides visual indication of the presence of dc in the monitor module. The dc ok circuit (Figure 9-10) consists of the following components.

- LED indicator (D400)
- Connector (J7)
- Drive transistor (Q400)
- Biasing components (R400, R401, and D401)

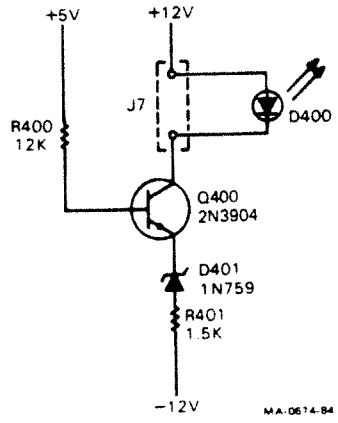


Figure 9-10 DC OK Circuit Diagram

+5 V, +12 V, and -12 V potentials are applied as inputs to the dc ok circuit. When all three inputs are present to turn on Q400, D400, which is mounted on the front panel of the VT220, and connected to Q400's collector via J7, it will light.

9.2.4 DC Input Components

The dc input components located on the logic board provide for additional filtering of dc potentials to be used by the monitor module logic board components, and for the +12 V potential to be output to the LK201 keyboard module. They also develop a fourth dc potential, -6 V, from the -12 V input.

The dc input components (Figure 9-11) consist of the following components.

- +5 V filter capacitors (C41 and C47)
- +12 V filter capacitor (C42)
- -12 V components (D5, C43, and C45)
- -6 V regulation components (R42 and D4)
- Individual IC +5 V decoupling capacitors (C1, C3, C4, C11, C14-C39, and C48-C54)

-12 VA is an unfiltered version of the -12 V input to the logic board.

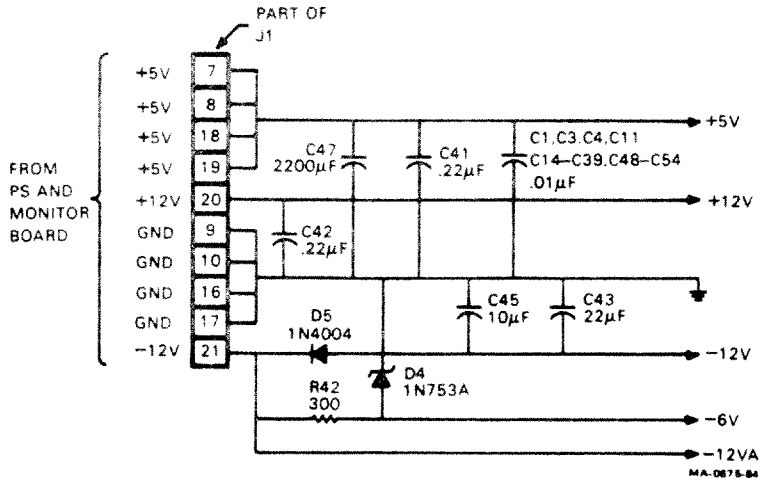


Figure 9-11 DC Input Circuits Diagram

APPENDIX A
SPECIFICATIONS

GENERAL

This appendix lists the specifications of the VT220 terminal.

VT220 SPECIFICATIONS

Physical

Terminal	Height: 28.3 cm (11 1/8 in) Width: 33.3 cm (13 1/8 in) Depth: 38.7 cm (15 1/4 in) Weight: 11.8 kg (26 lbs) Adjustable Tilt: +5 to -15 degrees
Keyboard	Height: 5.1 cm (2.0 in) Width: 53.3 cm (21.0 in) Depth: 17.1 cm (6.75 in) Weight: 2.0 kg (4.5 lbs)

Environmental

Operating Temperature:	10o to 40o C (50o to 104o F) Relative humidity: 10% to 90% Maximum wet bulb: 28o C (82o F) Minimum dew point: 2o C (36o F) Maximum altitude: 2.4 km (8000 ft)
Storage	Temperature: -40o to 66o C -40 to 151o F Relative humidity: 0% to 95% Maximum altitude: 9.1 km (30,000 ft)

Electrical

Line voltage (switch selectable)	90-128 Vac (100-120 rms nominal) single phase, 3-wire
	180-268 Vac (220-240 rms nominal) single phase, 3-wire
Line frequency	47-63 Hz
Line current	0.48 A rms @ 120 Vac rms 0.24 A rms @ 240 Vac rms
Input power	60 W maximum
Power cord	Detachable, 3-conductor, grounded
Power cord receptacle	EIA specified CEE22-6A
BTU	215 Btu/hr, 63 W

Display

CRT	30.5 cm (12 in) diagonal measure monochrome
Active display size	Horizontal: 20.3 cm (8 in) Vertical: 12.7 cm (5 in)
Format	24 lines of 80 or 132 characters
Character	7 X 9 dot matrix with 2 descenders
Character size	80 column mode: 3.35 X 2 mm (0.132 X 0.078 in) 132 column mode: 3.35 X 1.3 mm (0.132 X 0.051 in)
Character sets	ASCII, UK National, DEC Special Graphic, and DEC Supplemental Character Sets (each 94 characters)
Video attributes	Reverse video, underline, bold, and blinking -- selectable individually or in any combination
Cursor type	Blinking block character or blinking underline

Keyboard

General	105 key detachable unit with a 1.8 m (6 ft) coiled cord with a 4-pin telephone-type modular connector. Word processing and data processing versions available in 15 languages
Keypad	Sculptured key array. Matte texture finish keys. Home row key height 30 mm (1.18 in) above desk top
Key size	12.7 mm (0.5 in) square
Key spacing	19 mm (0.75 in) center-to-center (single width keys)
Numeric keypad	18 keys
Function keys	36 keys, firmware and software driven
Visual indicators	4 LED indicators: hold, lock, wait, and compose
Audible signals	
Keyclick:	Audible feedback for each keystroke
Bell:	Sounds when BEL character received, when 8 characters from right margin and for compose errors
Multiple bell:	Sounds on error in set-up, save, or recall operation.

APPENDIX B
VT102/220 DIFFERENCES

This appendix describes the major differences between a VT102 terminal and the VT220 terminal operating in a VT100 mode.

Difference Area	VT102	VT220
LEDs	Programmable	Non-programmable
Alternate character ROM	Socket for OEM supplied character ROM	Down-line loadable character set
Screen freeze	NO SCROLL key	HOLD SCREEN key
Printer port connector	25-pin	9-pin
Screen refresh	50/60 Hz	60 Hz only
Set-up	Display in set-up "bits."	Display in three languages. Different display. Has no effect on software.
RIS function	Performs power-up self test	Does not perform power-up self test
Off-line/local	Off-line mode disconnects modem	Local mode does not disconnect modem
Communication	Full duplex and half duplex	Full duplex only. Does not affect software
	Transmit speed limitation of 60 char/s regardless of baud rate	Optional transmit speed limitation of 150 char/s
	Selectable passive or active 20 mA	Passive 20 mA only

Difference Area	VT102	VT220
Terminal ID	Responds to primary device attributes with: ESC [? 6 c	Responds to primary device attribute with: CSI ? 62;1;2;6;7;8;9 c

NOTE

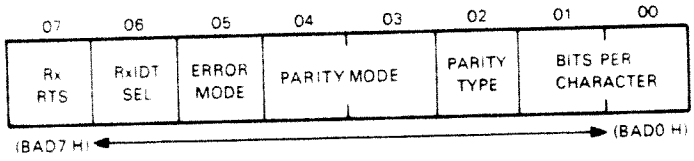
If the terminal is in VT100 mode and an ID other than VT220 ID is selected, then the following primary exchanges apply.

VT220 to host (VT100 ID selected in set-up)	ESC [? 1; 2 c
VT220 to host (VT101 ID selected in set-up)	ESC [? 1; 0 c
VT220 to host (VT102 ID selected in set-up)	ESC [? 6 c
Secondary device attribute not supported	Responds to secondary device attribute with: CSI > 1;Pv; 0 c where Pv is firmware version number

APPENDIX C
REGISTER BIT VALUES

This appendix contains figures illustrating bit values for the various register devices within the system box logic board circuits. The figures are provided for reference only, and are not meant as a guide to programming the VT220 Series terminal.

MR1A ADDRESS B7F0H (RD)/B7F0H (WR)
MR1B ADDRESS B7F8H (RD)/B7F8H (WR)



BIT VALUES		
BIT 7	0	RxRTS DISABLED
	1	RxRTS ENABLED
BIT 6	0	INTERRUPT ON RxRDY
	1	INTERRUPT ON FFULL
BIT 5	0	CHARACTER ERROR MODE
	1	BLOCK ERROR MODE
BIT 3–4	00	WITH PARITY
	01	FORCE PARITY
	10	NO PARITY
	11	SPECIAL MODE
BIT 2	0	EVEN PARITY
	1	ODD PARITY
BIT 0–1	00	5 BITS PER CHARACTER
	01	6 BITS PER CHARACTER
	10	7 BITS PER CHARACTER
	11	8 BITS PER CHARACTER

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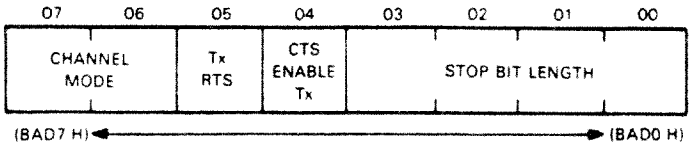
Figure C-1 2681 DUART: Mode Register 1 (MR1) (Channel A and B)

MR2A ADDRESS B7F0H (RD)/B7F0H (WR)
MR2B ADDRESS B7F8H (RD)/B7F8H (WR)



BIT VALUES		
BIT 6–7	00	NORMAL MODE
	01	AUTO ECHO MODE
	10	LOCAL LOOP MODE
	11	REMOTE LOOP MODE
BIT 5	0	Tx RTS DISABLE
	1	Tx RTS DISABLE
BIT 4	0	NO CTS REQUIRED FOR Tx
	1	CTS REQUIRED FOR Tx
BIT 0–3	0000*	0.563 BIT STOP CHARACTER
	0001*	0.625 BIT STOP CHARACTER
	0010*	0.688 BIT STOP CHARACTER
	0011*	0.750 BIT STOP CHARACTER
	0100*	0.813 BIT STOP CHARACTER
	0101*	0.875 BIT STOP CHARACTER
	0110*	0.938 BIT STOP CHARACTER
	0111*	1.000 BIT STOP CHARACTER
	1000	1.563 BIT STOP CHARACTER
	1001	1.625 BIT STOP CHARACTER
	1010	1.688 BIT STOP CHARACTER
	1011	1.750 BIT STOP CHARACTER
	1100	1.813 BIT STOP CHARACTER
	1101	1.875 BIT STOP CHARACTER
	1110	1.938 BIT STOP CHARACTER
	1111	2.000 BIT STOP CHARACTER

* ADD .5 BIT FOR 5 BITS PER CHARACTER OPERATION

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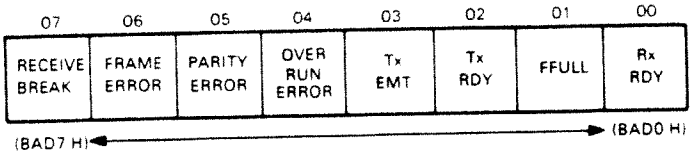
Figure C-2 2681 DUART: Mode Register 2 (MR2) (Channel A and B)

SRA ADDRESS B7F1H (RD)
SRB ADDRESS B7F9H (RD)



BIT VALUES		
BIT 7	0	NO BREAK DETECTED
	1	RECEIVE BREAK DETECTED
BIT 6	0	NO ERROR
	1	FRAMING ERROR
BIT 5	0	NO ERROR
	1	PARITY ERROR
BIT 4	0	NO ERROR
	1	OVERRUN ERROR
BIT 3	0	Tx NOT EMPTY
	1	Tx HOLDING AND SHIFT REGISTERS EMPTY
BIT 2	0	Tx HOLDING REGISTER FULL
	1	Tx HOLDING REGISTER EMPTY
BIT 1	0	Rx FIFO NOT FULL
	1	Rx FIFO FULL
BIT 0	0	NO Rx DATA WAITING
	1	Rx DATA IN FIFO

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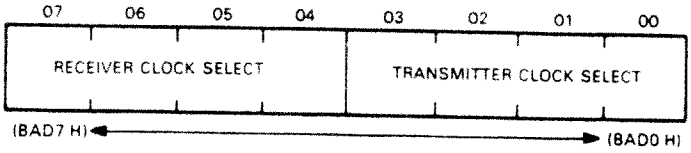
Figure C-3 2681 DUART: Status Register (SR) (Channel A and B)

DCSRA ADDRESS B7F1H (WR)
DCSRB ADDRESS B7F9H (WR)



BIT VALUES

BIT 0–3 OR 4–7	BAUD RATE SET 1	BAUD RATE SET 2
0000	50	75
0001	110	110
0010	134.5	134.5
0011	200	150
0100	300	300
0101	600	600
0110	1200	1200
0111	1050	2000
1000	2400	2400
1001	4800	4800
1010	7200	1800
1011	9600	9600
1101	38.4K	19.2K
1110	IP4–16X(RxCA)	IP4–16X(RxCA)
1110	IP6–16X(RxCB)	IP6–16X(RxCB)
1110	IP3–16X(TxCA)	IP3–16X(TxCA)
1110	IP5–16X(TxCB)	IP5–16X(TxCB)
1111	IP4–1X(RxCA)	IP4–1X(RxCA)
1111	IP6–1X(RxCB)	IP6–1X(RxCB)
1111	IP3–1X(TxCA)	IP3–1X(TxCA)
1111	IP5–1X(TxCB)	IP5–1X(TxCB)

NOTES:
1. RxC AND TxC ARE ALWAYS 16X EXCEPT FOR 1111 CONDITION.
2. SET SELECTION MADE BY ACR BIT 7.

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Figure C-4 2681 DUART: Data Clock Selection Register (DCSR) (Channel A and B)

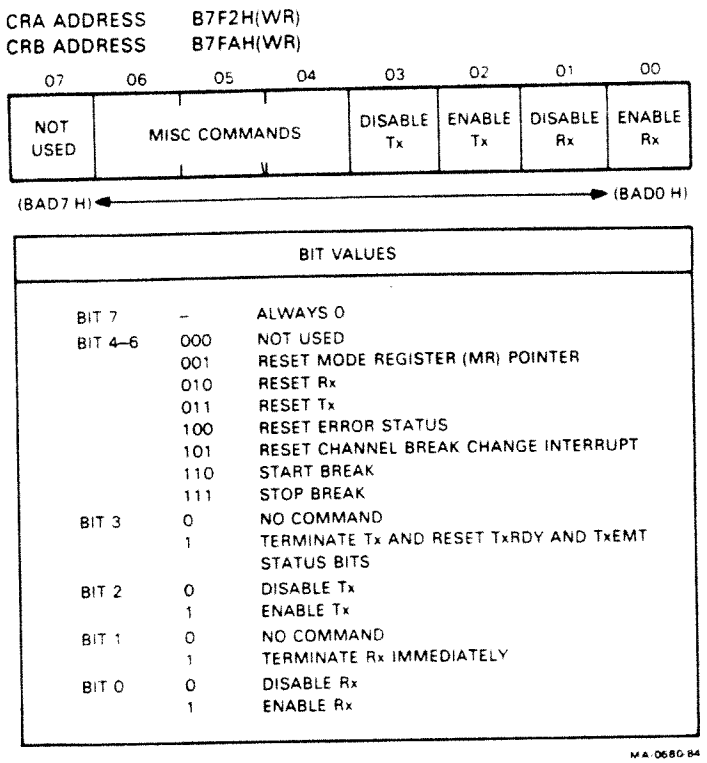

Figure C-5 2681 DUART: Command Register (CR) (Channel A and B)

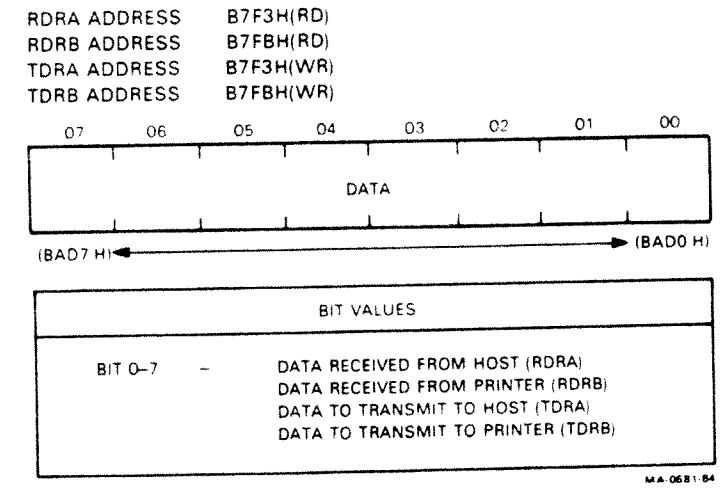

Figure C-6 2681 DUART: Receive/Transmit Data Registers (RDR/TDR) (Channel A and B)

ICR ADDRESS B7F4H(RD)

07	06	05	04	03	02	01	00
DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0

(BAD7 H) ◄——————————————————► (BAD0 H)

BIT VALUES		
BIT 7	0	NO CHANGE OF STATE DETECTED AT IP3
	1	CHANGE OF STATE DETECTED AT IP3
BIT 6	0	NO CHANGE OF STATE DETECTED AT IP2
	1	CHANGE OF STATE DETECTED AT IP2
BIT 5	0	NO CHANGE OF STATE DETECTED AT IP1
	1	CHANGE OF STATE DETECTED AT IP1
BIT 4	0	NO CHANGE OF STATE DETECTED AT IP0
	1	CHANGE OF STATE DETECTED AT IP0
BIT 3	0/1	CURRENT STATE OF IP3 (TVB)
BIT 2	0/1	CURRENT STATE OF IP2 (SPD IND)
BIT 1	0/1	CURRENT STATE OF IP1 (DSR)
BIT 0	0/1	CURRENT STATE OF IP0 (CTS)

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Figure C-7 2681 DUART: Input Change Register (ICR)

ACR ADDRESS B7F4H(WR)

07	06	05	04	03	02	01	00
BAUD SET SEL	COUNTER/TIMER MODE AND SOURCE			DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INIT

(BAD7 H) ◄——————————► (BAD0 H)

BIT VALUES		
BIT 7	0	SELECT BAUD RATE SET 1
	1	SELECT BAUD RATE SET 2
BIT 4–6	000	COUNTER MODE – EXTERNAL (IP2) SOURCE
	001	COUNTER MODE – TxCA AT 1X CLOCK OF CHANNEL A Tx
	010	COUNTER MODE – TxCB AT 1X CLOCK OF CHANNEL B Tx
	011	COUNTER MODE – CRYSTAL OR EXTERNAL CLOCK (CLK) DIVIDED BY 16
	100	TIMER MODE – EXTERNAL (IP2) SOURCE
	101	TIMER MODE – EXTERNAL (IP2) SOURCE DIVIDED BY 16
	110	TIMER MODE – CRYSTAL OR EXTERNAL (CLK) SOURCE
	111	TIMER MODE – CRYSTAL OR EXTERNAL (CLK) SOURCE DIVIDED BY 16
BIT 3	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP3
BIT 2	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP2
BIT 1	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP1
BIT 0	0	NO INTERRUPT ON CHANGE OF STATE
	1	SET ISR BIT 7 ON DETECT OF CHANGE OF STATE AT IP0

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Figure C-8 2681 DUART: Auxiliary Control Register (ACR)

ISR ADDRESS B7F5H (RD)

07	06	05	04	03	02	01	00
INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	CNTR READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA

(BAD7 H) ◄——————————————► (BAD0 H)

BIT VALUES		
BIT 7	0	NO INTERRUPT
	1	INPUT PORT CHANGE OF STATE DETECTED
BIT 6	0	NO INTERRUPT
	1	CHANGE IN BREAK STATE DETECTED (CH. B)
BIT 5	0	NO INTERRUPT
	1	RxRDY/FFULL CONDITION (CH. B)
BIT 4	0	NO INTERRUPT
	1	TxRDY CONDITION (CH. B)
BIT 3	0	NO INTERRUPT
	1	COUNTER READY CONDITION
BIT 2	0	NO INTERRUPT
	1	CHANGE IN BREAK STATE DETECTED (CH. A)
BIT 1	0	NO INTERRUPT
	1	RxRDY/FFULL CONDITION (CH. A)
BIT 0	0	NO INTERRUPT
	1	TxRDY CONDITION (CH. A)

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Figure C-9 2681 DUART: Interrupt Status Register (ISR)

IMR ADDRESS B7F5H (WR)

07	06	05	04	03	02	01	00
INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	CNTR READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYB	TxRDYA

(BAD7 H) ◄——————————————► (BAD0 H)

BIT VALUES		
BIT 7	0	INTERRUPT DISABLED
	1	INPUT PORT CHANGE OF STATE INTERRUPT ENABLED
BIT 6	0	INTERRUPT DISABLED
	1	CHANGE IN BREAK STATE INTERRUPT ENABLED (CH. B)
BIT 5	0	INTERRUPT DISABLED
	1	RxRDY/FFULL INTERRUPT ENABLED (CH. B)
BIT 4	0	INTERRUPT DISABLED
	1	TxRDY INTERRUPT ENABLED (CH. B)
BIT 3	0	INTERRUPT DISABLED
	1	COUNTER READY INTERRUPT ENABLED
BIT 2	0	INTERRUPT DISABLED
	1	CHANGE IN BREAK STATE INTERRUPT ENABLED (CH. A)
BIT 1	0	INTERRUPT DISABLED
	1	RxRDY/FFULL INTERRUPT ENABLED (CH. A)
BIT 0	0	INTERRUPT DISABLED
	1	TxRDY INTERRUPT ENABLED (CH. A)

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Figure C-10 2681 DUART: Interrupt Mask Register (IMR)

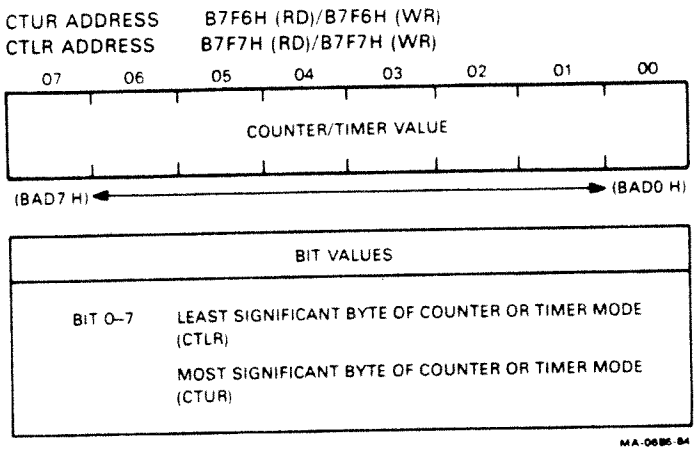


Figure C-11 2681 DUART: Counter Timer/Upper (CTUR) and Lower (CTLR) Registers

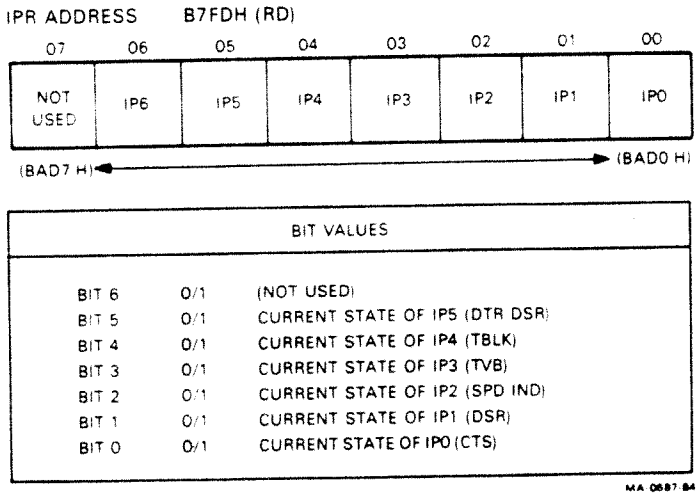


Figure C-12 2681 DUART: Input Port Register (IPR)

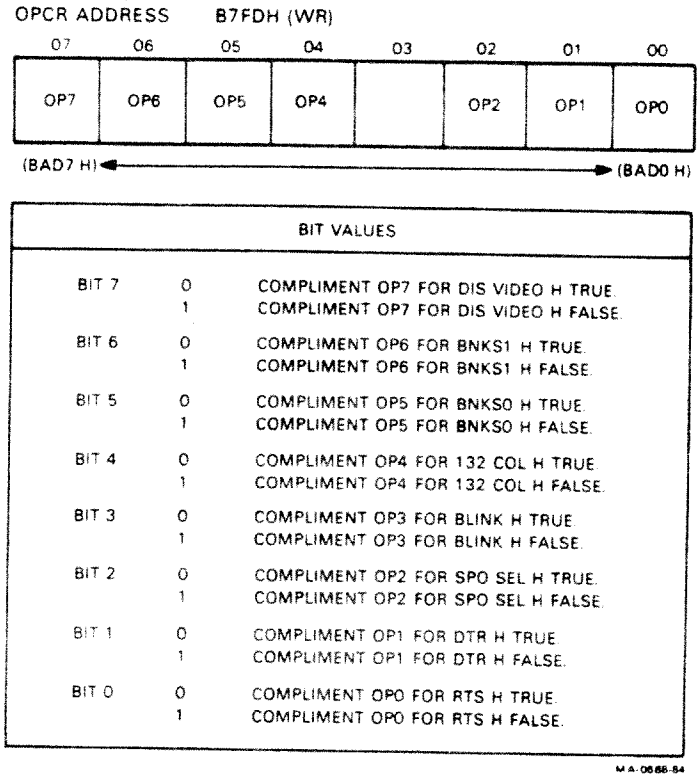


Figure C-13 2681 DUART: Output Port Configuration Register (OPCR)

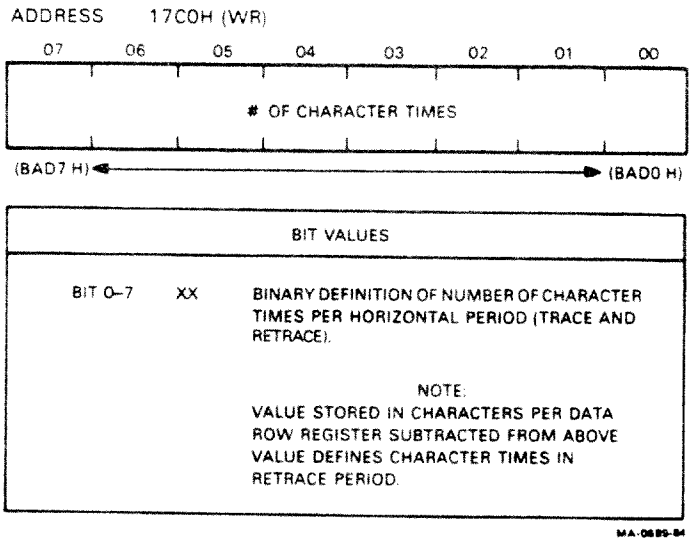


Figure C-14 9007 VPAC: Characters Per Horizontal Period Register

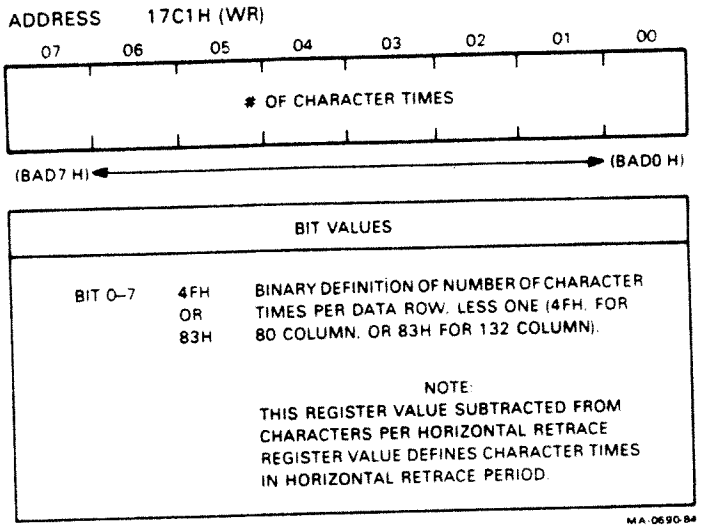


Figure C-15 9007 VPAC: Characters Per Data Row Register

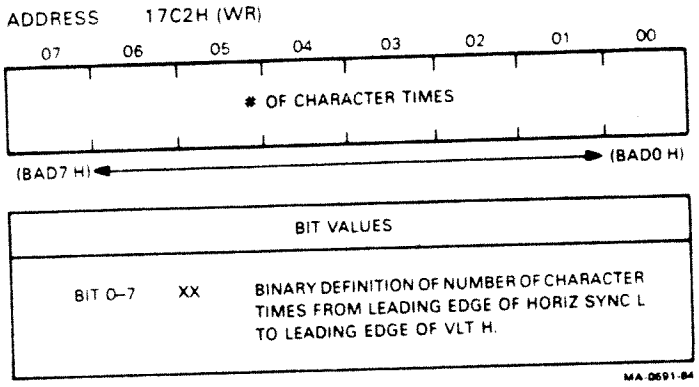


Figure C-16 9007 VPAC: Horizontal Sync Delay Register

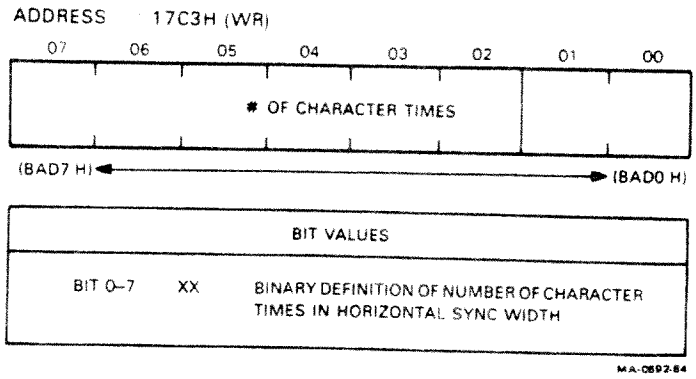


Figure C-17 9007 VPAC: Horizontal Sync Width Register

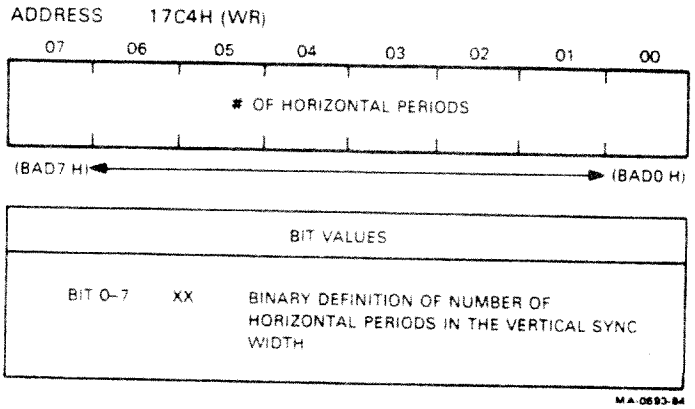


Figure C-18 9007 VPAC: Vertical Sync Width Register

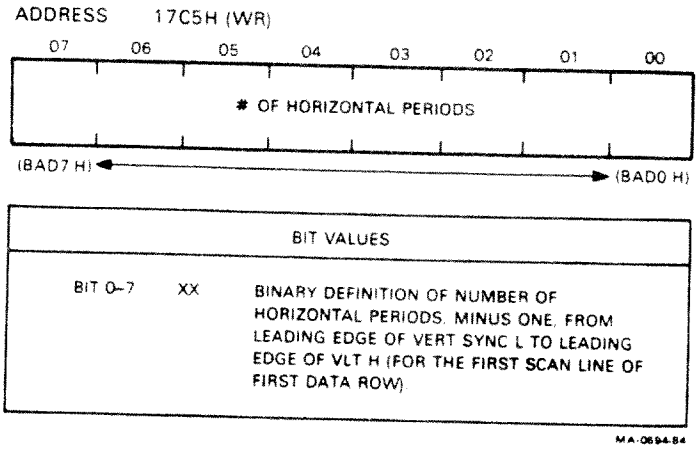


Figure C-19 9007 VPAC: Vertical Sync Delay Register

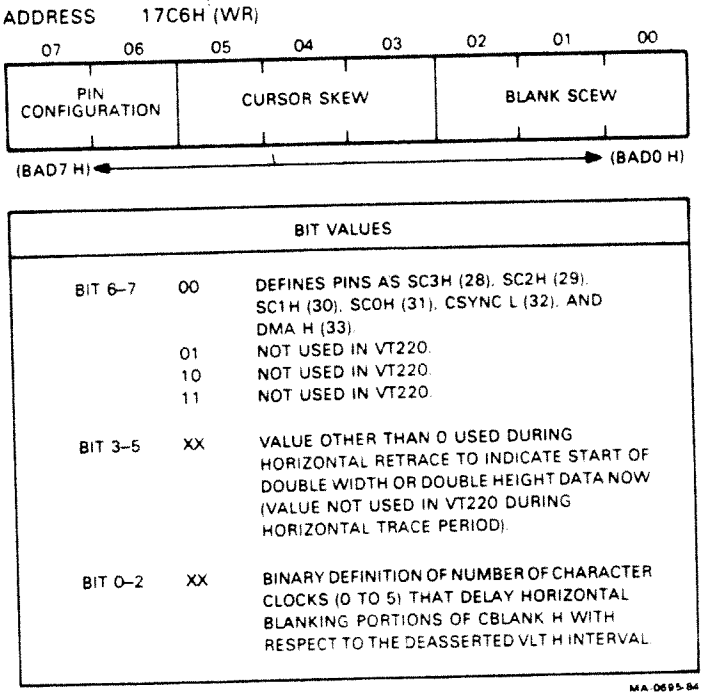


Figure C-20 9007 VPAC: Configuration/Skew Register

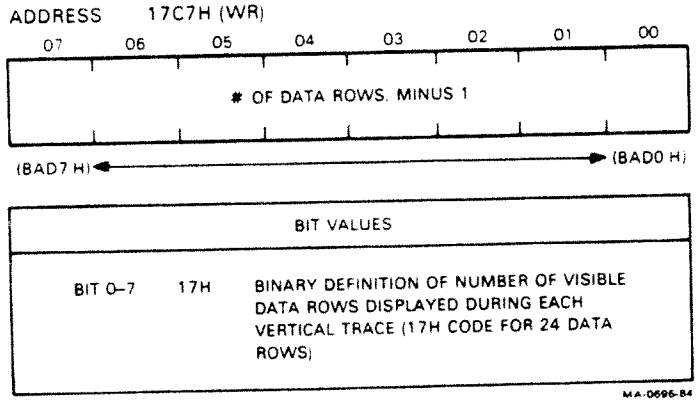


Figure C-21 9007 VPAC: Data Rows Per Frame Register

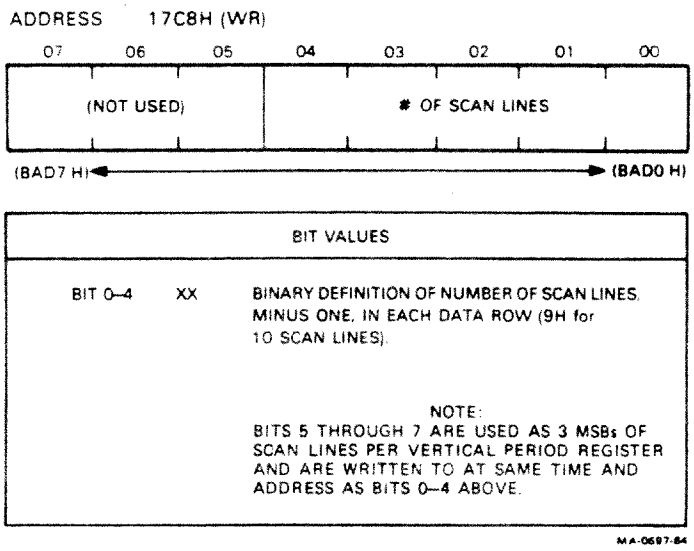


Figure C-22 9007 VPAC: Scan Lines Per Data Row Register

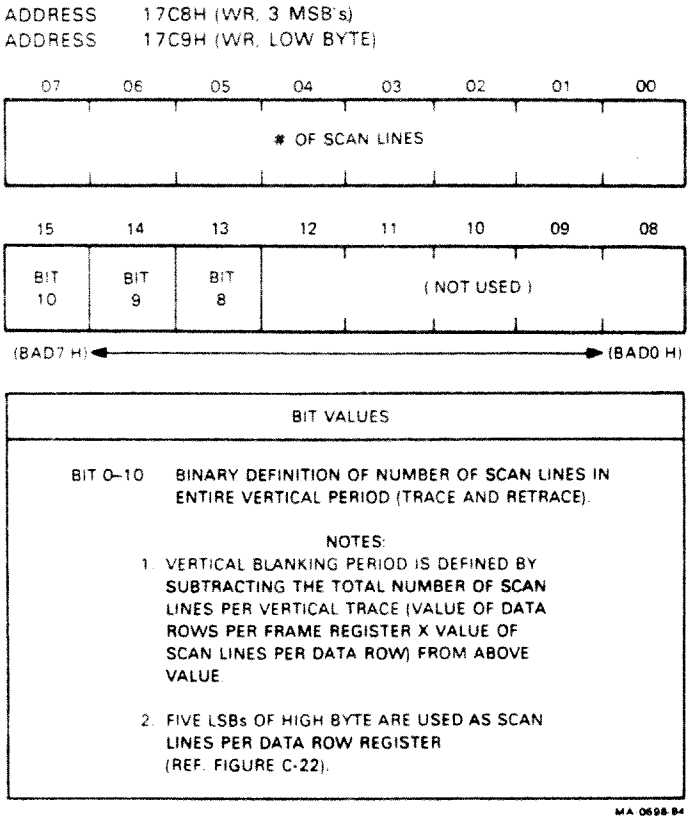


Figure C-23 9007 VPAC: Scan Lines Per Vertical Period Register

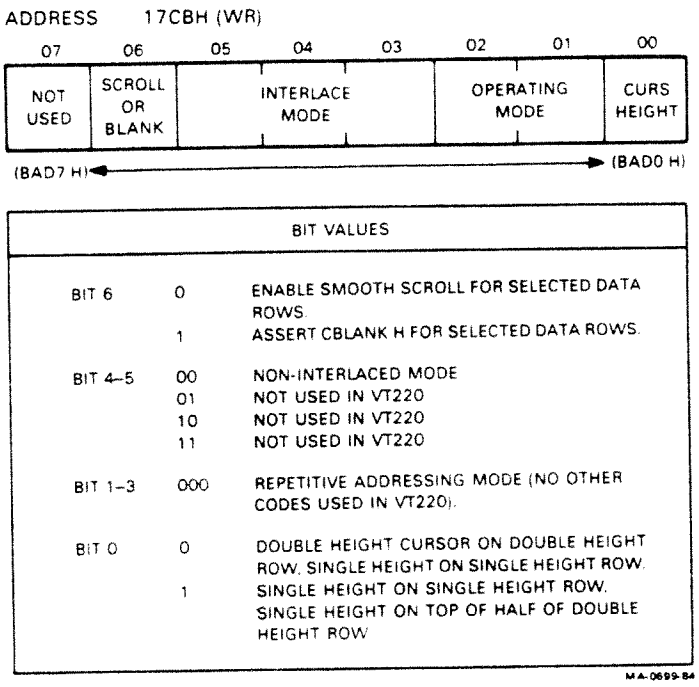


Figure C-24 9007 VPAC: Control Register

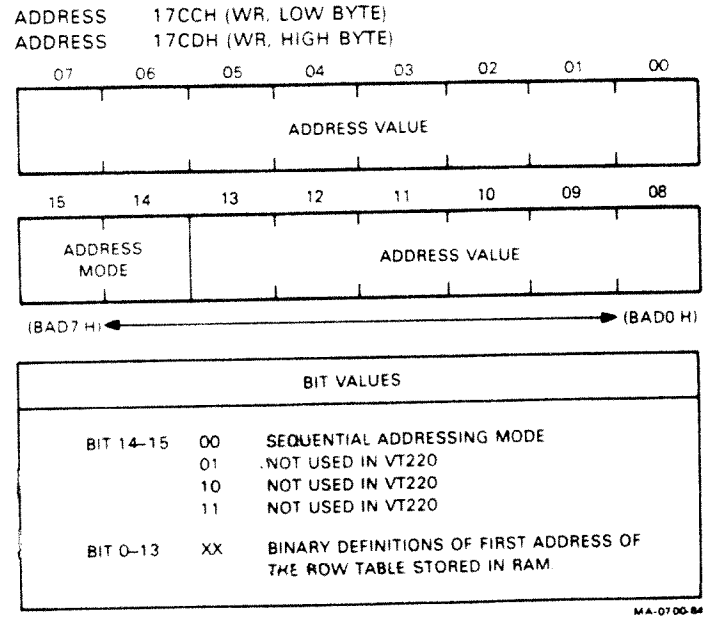


Figure C-25 9007 VPAC: Table Address Register

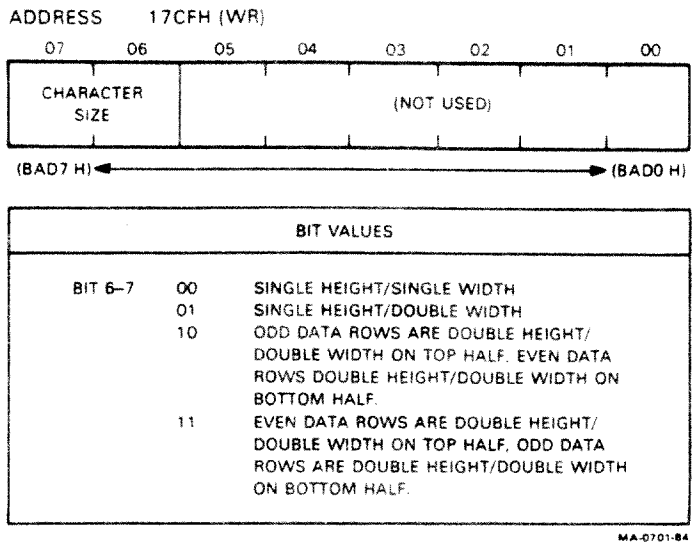


Figure C-26 9007 VPAC: Row Attribute Register

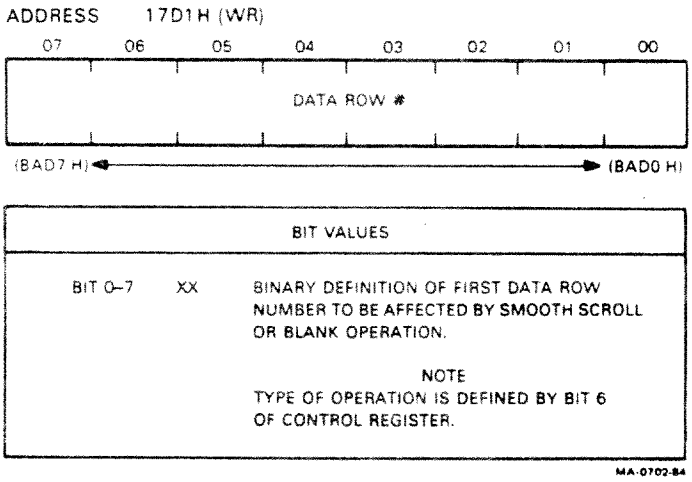


Figure C-27 9007 VPAC: Data Row Start Register

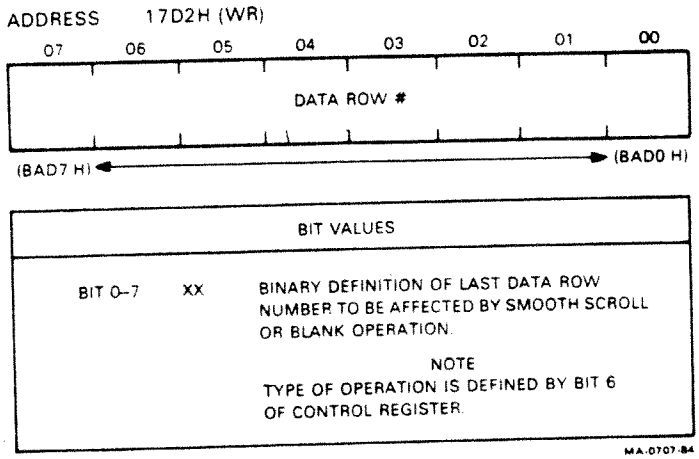


Figure C-28 9007 VPAC: Data Row End Register

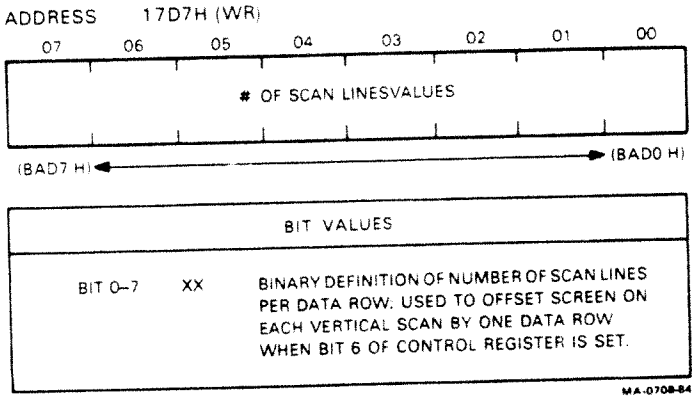
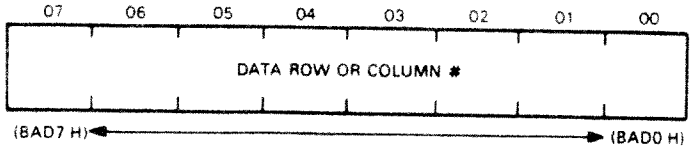


Figure C-29 9007 VPAC: Smooth Scroll Offset Register

ADDRESS 17D8H (WR, VERTICAL)
ADDRESS 17D9H (WR, HORIZONTAL)
ADDRESS 17F8H (RD, VERTICAL)
ADDRESS 17F9H (RD, HORIZONTAL)



BIT VALUES		
BIT 0–7	XX	BINARY DEFINITION OF DATA ROW (VERTICAL CURSOR REGISTER) OR COLUMN NUMBER (HORIZONTAL CURSOR REGISTER) OF THE CURSOR.

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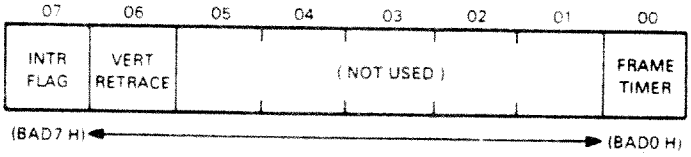
Figure C-30 9007 VPAC: Vertical/Horizontal Cursor Registers

ADDRESS 17FAH (RD)



BIT VALUES		
BIT 7	0	NO OTHER STATUS BIT SET.
	1	OTHER STATUS BIT SET.
BIT 6	0	NO VERTICAL RETRACE IN PROGRESS.
	1	VERTICAL RETRACE IN PROGRESS.
BIT 1–5	–	NOT USED
BIT 0	0	FINAL TABLE ADDRESS NOT READ.
	1	FINAL TABLE ADDRESS READ.

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Figure C-31 9007 VPAC: Status Register