NEW NUMBER = DBKTA

ABSTRACT =

This program incrementally test the basic logic functions of the KT11-D memory management option for the PDP-11/40. It fully tests relocation direct and indirect addressing of the memory management registers, and correct operation of all the bits in the registers. The various aborts are tested, as is proper "locking" and "unlocking" of the error tracking logic.

REQUIREMENTS =

PDP-11/40 with KT11-D option

STORAGE = Program requires memory locations 0 to 17474.

LOADING = Absolute Loader.

EXECUTION TIME = Each pass takes approximately 3 minutes with core memory.

STARTING PROCEDURE = Load address 200.

PRINTOUTS = Yes

SWITCH REGISTER OPTIONS = Yes

SW15 = 1 or Up ... HALT ON ERROR
SW14 = 1 or Up ... SCOPE LOOP
SW13 = 1 or Up ... INHIBIT PRINTOUT
SW11 = 1 or Up ... INHIBIT ITERATIONS
SW10 = 1 or Up ... HALT AT END OF CURRENT TEST WITH NEXT TEST NUMBER IN DATA LIGHTS.