R SERIES LOGIC
CIRCUIT PHILOSOPHY AND SYMBOLOGY

INTRODUCTION

This portion of the discussion will deal with the 2 mc line of R series FLIP CHIP™ logic modules.

Standard logic levels used are ground and −3v. Both pulse and level signals may be used to drive the logic.

In the R series line, the minimum allowable pulse width is 100 nsec, while a voltage is considered a level if it remains constant for a minimum of 400 nsec before changing state. Rise times of 60 nsec maximum for pulses or edges may be used to activate differentiating inputs. When using DEC logic, an important item to remember is that only rising edge triggering (differentiation) is used.

The DEC symbology for standard signals is shown in Figure 1-1.

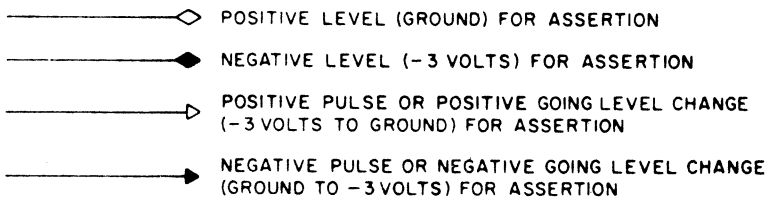

Figure 1-1 DEC Standard Levels and Pulses

In addition, the following standardization of the "1" and "0" terminology is used:

1. If a flip-flop is set to the 1 state, its 1 output is at −3v and its 0 output is at ground.

2. If a flip-flop is set to the 0 state, its 0 output is at −3v and its 1 output is at ground.

Hence, DEC practice is based on negative logic.

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SYMBOLOGY

The inverter, consisting of a saturating PNP transistor, −3v power supply, and clamped load, is the most basic circuit network used in DEC logic. The schematic for this circuit is shown in Figure 1-2.

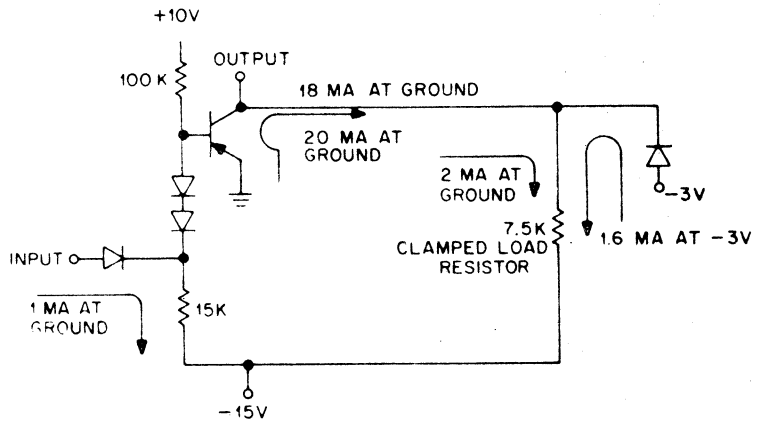


Figure 1-2 Inverter

This circuit will operate from either pulse or level input signals. The circuit operation is as follows. When the input terminal is at ground potential, the transistor is turned off and its collector-emitter terminals are effectively open circuited. The −3v clamping diode is then forward biased and holds the output (collector) terminal at the −3v level. An advantage of this type of configuration is that the inverter has a low output impedance. When the transistor is not conducting, the inverter output impedance is effectively the conducting clamp diode in parallel with the 7.5K load resistor. When the transistor is conducting, the output impedance is that of the transistor itself, about 6 ohms.

A further analysis of the circuit will show that with a grounded input, the input diode is forward biased and 1 ma will flow through the 15K resistor. When the input terminal is held at −3v, or is open circuited, the transistor will saturate and the output terminal will be at nearly ground potential. Under the conditions described here, the transistor is capable of supplying 20 ma through its collector. However, because the −3v clamping diode is now back biased, the transistor must supply a 2-ma internal load through the clamped load resistor. Therefore, the inverter can supply 18 ma of output current at ground. It should also be noted that with the input at −3v, the input diode is back biased and no current will flow through the input leg.

The inverter circuit exhibits good noise immunity because of its DTL configuration. When the transistor is being held on by a −3v signal at its input, any noise spike tending to turn the transistor off must overcome the forward drop of three diodes in series. This amounts to something on the order of 1.2 to 1.5v.

Using the DEC standard of 1 ma equals 1 unit of load, the diode gate requires 1 unit load at its input and can supply 20 units minus 2 units for internal load or 18 unit loads at its output terminal. The logic symbol for the inverter is shown in Figure 1-3.

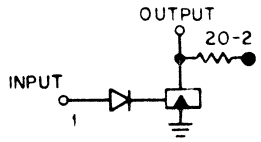
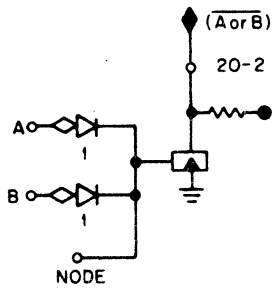


Figure 1-3 Inverter with Loading Requirements

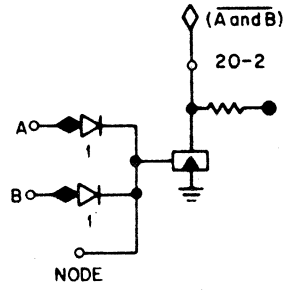
Diode Gate Variations

There are several variations of the basic inverter detailed below. A multiple input diode gate is shown in Figure 1-4. If both inputs A and B are at −3v, the output will be ground. The diode gate is operating as a NAND circuit, in keeping with our earlier definition of negative logic.

For use in positive logic applications, the gate performs a NOR function.



Positive Logic



Negative Logic

Figure 1-4 Multiple Input Diode Gate

It should be noted that these diode gates have a fan in limitation of 6 inches of lead length at the node point. Lead lengths of more than 6 inches connecting the added diodes at the node tend to increase the noise sensitivity of the circuit since the node is connected to the transistor base.

The output terminals of several diode gates can be tied together to perform different types of gating functions. Figure 1-5 shows a parallel connection of diode gates for dependent operation.

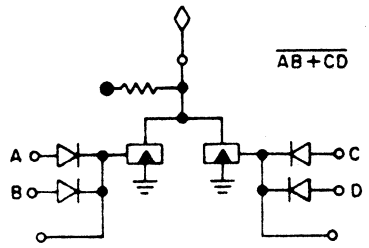


Figure 1-5 Diode Gates in Parallel

Another variation of the basic diode gate is the circuit shown in Figure 1-6.

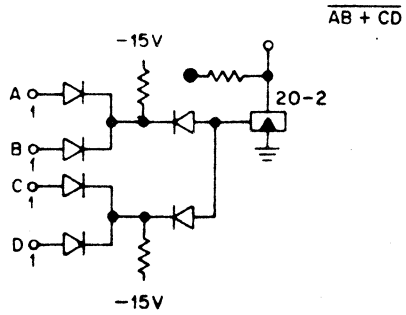


Figure 1-6 Variation of Basic Diode Gate

This circuit performs two levels of gating. As shown in Figure 1-6, this diode gate contains two 2-input networks. The back to back diode circuitry is possible because of a negative bias voltage tied to the input of each second stage diode.

For negative input signals, this diode gate acts as two 2-input AND gates which are NORed together. That is, if both input terminals of any pair of input terminals are at $-3v$, the output of the gate will go to ground.

Flip-Flops

When a pair of two input diode gates are connected so that the output of one diode gate is connected to the input of the second, and vice-versa, the resultant circuit is a flip-flop. Figure 1-7 shows the diode gate interconnections necessary to form a flip-flop.

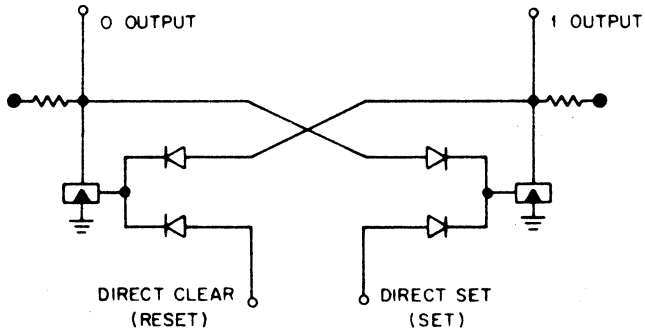


Figure 1-7 Flip-Flop Formed from Diode Gate Interconnections

The circuit shown above is an R-S type flip-flop. In order to set the flip-flop to 0, the direct clear input is held at ground. The flip-flop can be set to a 1 by applying a ground at the direct set input terminal. Of course, once the flip-flop has been set to a given state, it will remain in that state until the input terminal corresponding to the opposite state has been pulsed. The standard DEC symbology for this flip-flop, along with the loading characteristics, is shown in Figure 1-8.

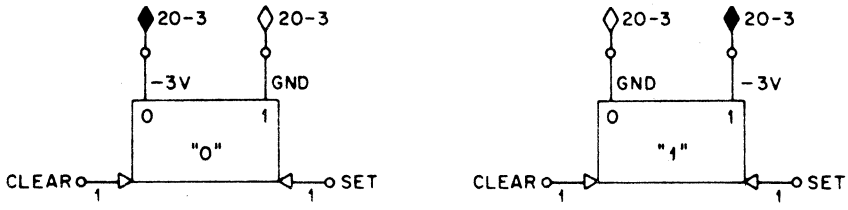


Figure 1-8 DEC Flip-Flop Symbology

The diode-capacitor-diode (DCD) gate represents another gating structure used in DEC logic. This gate is used primarily for flip-flop pulse steering applications. Figure 1-9 shows the basic DCD schematic.

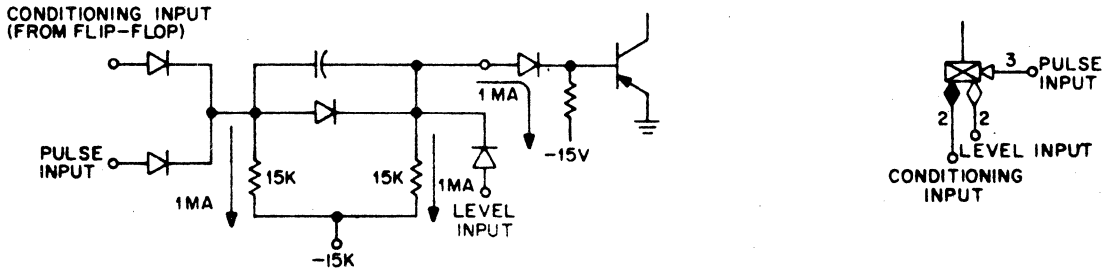


Figure 1-9 DCD Schematic

Before the DCD gate can operate, the level input must be grounded and the pulse input must be held at −3v for 400 nsec minimum in order to charge up the capacitor. The input pulse or level change must be at least 100 nsec long to pass through the gate. After the capacitor has been charged, when a positive pulse or positive going level change is applied to the pulse input terminal, a positive pulse (ground to +3v) of about 150 nsec duration will immediately appear at the output terminal. Since the DCD gate output terminal is always directly connected to the base of one of the transistors in a flip-flop circuit, the positive pulse at the DCD output will shut that transistor off.

It can be said that the DCD gate has a temporary memory due to its built-in RC network. Once the gate has been conditioned, the input pulse will be gated by the level input that existed during the period before the pulse. In addition, because of the long time constant of this circuit, a change in the level input will not be noticed by the gate until approximately 100 nsec after the change has occurred. This delay

feature of the DCD gate allows the flip-flop output to be sampled at the same time its input is changing. The input-output characteristics of the DCD gate are shown in Figure 1-10.

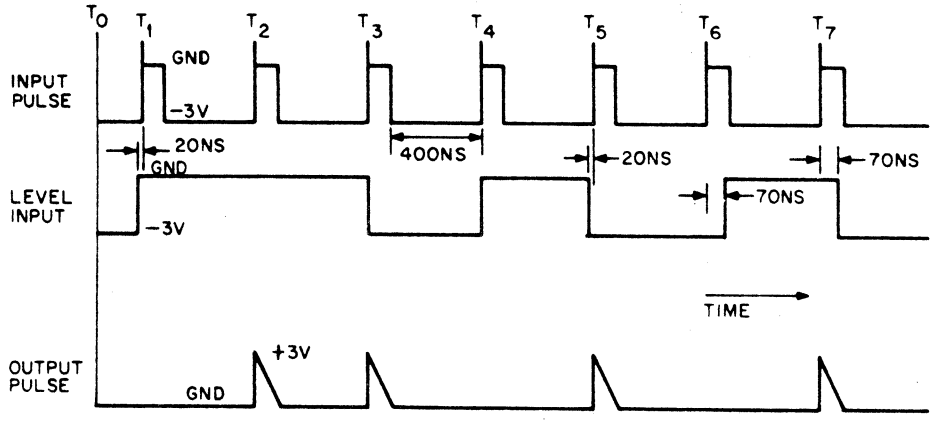


Figure 1-10 DCD Gate Input/Output

Figure 1-11 shows a transition region from 20 to 400 nsec after a level input changes. Any positive transition occurring up to 20 nsec after a level change and after 400 nsec from the level change will be either inhibited or enabled according to the chart. The transition region is one of uncertainty and it is wise to design systems which avoid triggering DCD gates during this period.

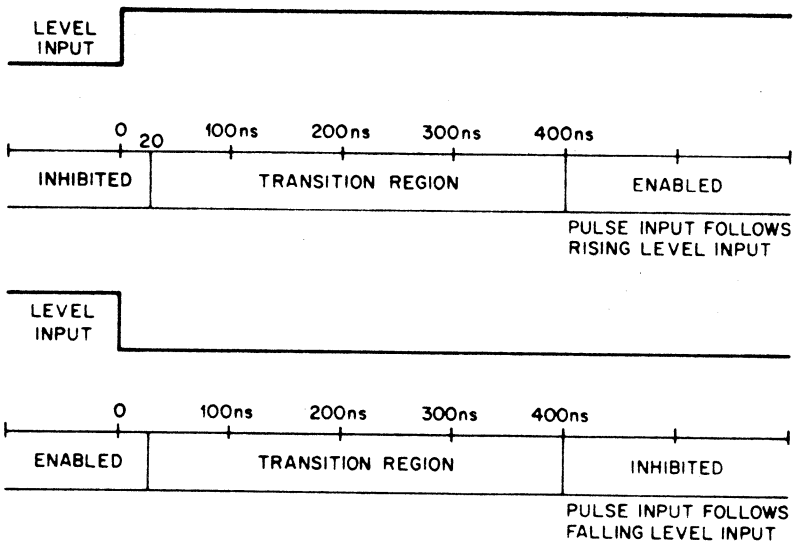


Figure 1-11 DCD Gate Input Timing

For added versatility, DCD gates are connected to the flip-flop inputs. These gates provide sufficient delay so the information may be read out of one flip-flop into another at the same time the first flip-flop receives a command to change state. Figure 1-12 shows the DCD gate to flip-flop connections.

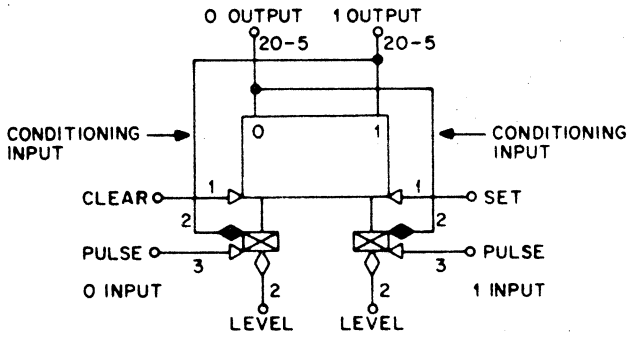


Figure 1-12 DCD Gate and Flip-Flop

When a DCD gate is combined with a flip-flop, as shown in Figure 1-12, the flip-flop output is used to condition the gate. That is, when the flip-flop has been set to a 1, the 0 input gate is conditioned by the −3v level applied in parallel with the pulse input terminal. The 1 input gate has a ground level applied in parallel with its pulse input terminal and this prevents the capacitor from being charged under any conditions.

When the flip-flop is set to 0, only the 1 input DCD gate is conditioned. Both the 0 and 1 conditioning inputs are connected internally on the modules and are not shown on any logic diagrams. However, the function of these conditioning levels should be remembered since it is a very useful tool to use when designing with flip-flops. Figure 1-13 shows a DEC standard flip-flop.

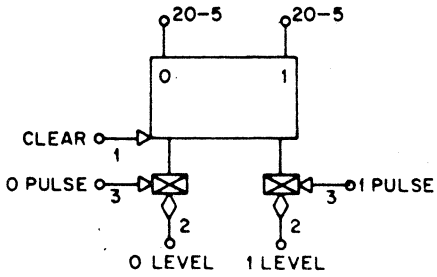


Figure 1-13 DEC Standard Flip-Flop

This flip-flop can perform in any one of the following applications without additional gating:

1. up counter
2. down counter
3. shift register
4. ring counter
5. jam transfer buffer
6. switch tail ring counter

This circuit can be connected for both R-S and J-K operation. Figure 1-14 shows the flip-flop connected for J-K operation by tying the 0 pulse and 1 pulse inputs together.

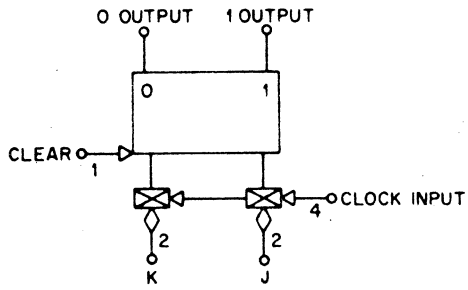


Figure 1-14 J-K Operation

Note that by using a common pulse input, the DCD gate input loading requirements have lessened. The circuit can be complemented by connecting the 0 level and 1 level inputs to ground. When a signal arrives at the common pulse input, the flip-flop will complement.

As shown in Figure 1-14, the flip-flop has no built-in set input. When the need for this type or additional inputs arises, these flip-flops may be collector triggered. That is, when there are not enough DCD gates available, the flip-flop can be set to a 1 by grounding the 0 output terminal from a collector. The flip-flop can be also set to a 0 by simply grounding the 1 output terminal from a collector. Figure 1-15 shows this in schematic form.

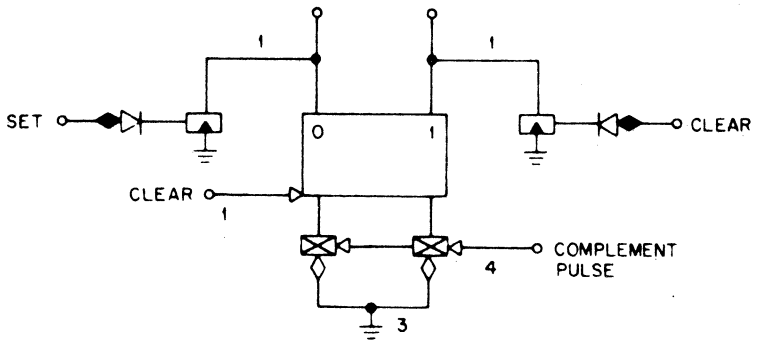


Figure 1-15 Collector Triggering

An expansion of collector triggering techniques is shown below. Figure 1-16 shows a series of basic R-S flip-flops with individual set and clear inputs. When the need arises to clear all flip-flops together, such as from a master clear signal, it can be done as shown.

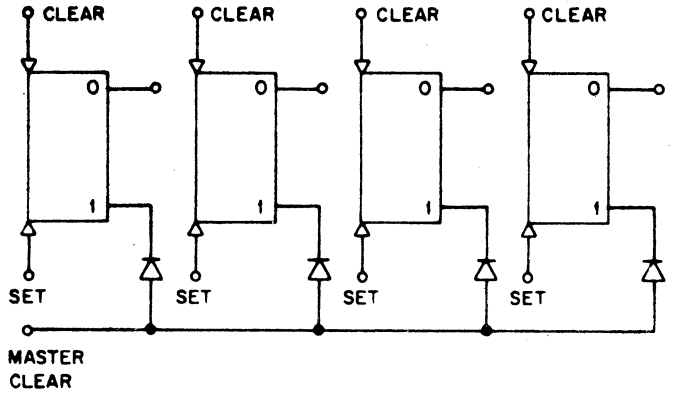
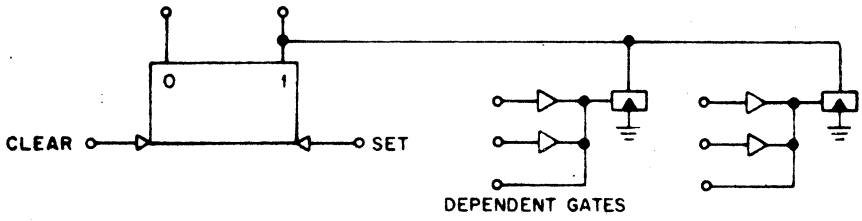
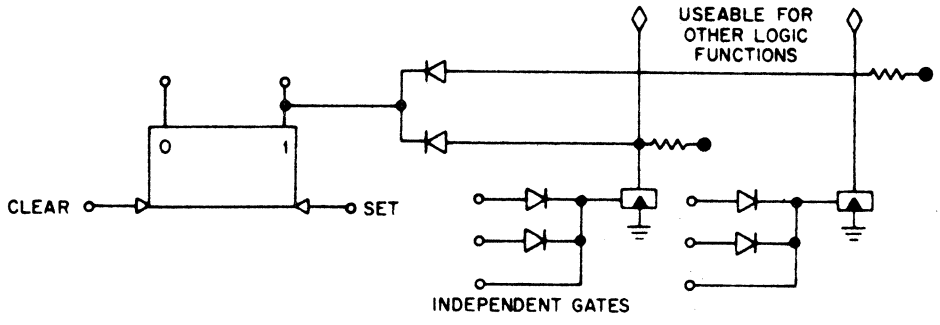


Figure 1-16 RS Flip-Flop Series

Figure 1-17 shows methods used for gated or multiple input set/reset controls.



Dependent Gates



Independent Gates

Figure 1-17 Collector Triggering Techniques for Gated or Multiple Input Controls

THE PRACTICAL SIDE OF LOGIC DESIGN

It must be remembered even though we talk about low speed logic, we are still talking about rates up to 2 mc with pulse widths of 100 nsec and edge speeds of 60 nsec or less. Stray capacity introduced by wiring can, for example, slow an edge down to the point where a flip-flop will fail to regenerate, or a DCD gate will fail to trigger. There are no hard and fast rules for recognizing the problem. Experience with the actual circuits will be the best tool in detecting the problem. There are, however, some rules of thumb remedies for coping with the problems that may arise.

The most prevalent problem by far is that of R-series flip-flops which fail to regenerate when they have long lines connected to their outputs. This is caused by the increased fall time due to the additional capacitance. Discharging the capacitance more quickly will solve the problem and is accomplished by adding clamped loads to the ailing collector. In general, lines up to two feet in length will not affect the fall time appreciably.

On extremely long lines, where it is impossible to add enough clamped loading without using up the full driving capability of the line, a series termination of 100 ohms at the driving end will help to decouple the line capacitance.

Notes:
1. Drive the line in its characteristic Z.
2. Terminate the line in its characteristic Z.
3. Both

$$\text{Char. } Z = \sqrt{\frac{L}{C}}$$

$$\text{Prop. velocity} = V = \frac{1}{\sqrt{\frac{L}{C}}}$$

R. SERIES
LOGIC SYMBOLS

LOGIC LEVELS ARE 0V AND -3V

A LOGIC LEVEL THAT IS ASSERTED HIGH IS DRAWN:

A LOGIC LEVEL THAT IS ASSERTED LOW IS DRAWN:

A HIGH GOING PULSE IS DRAWN:

A LOW GOING PULSE IS DRAWN

ANY SIGNAL LESS THAN 400 NS WIRE IS CONSIDERED A PULSE

A <u>STANDARD</u> PULSE IS 100 NS WIDE

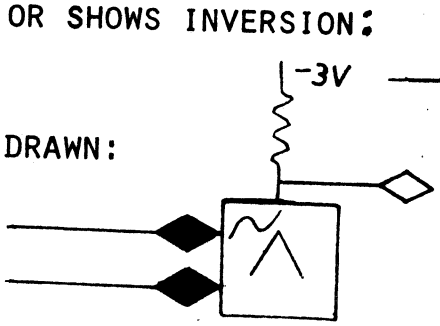
AN INVERTED SIGNAL IS SHOWN WITH THIS SYMBOL:

FOR EXAMPLE: PC ENABLE

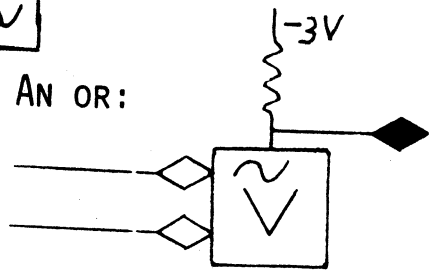
PC ENABLE

THE SAME SYMBOL IN A BOX OR OTHER SYMBOL IS AN INVERTER OR SHOWS INVERSION:

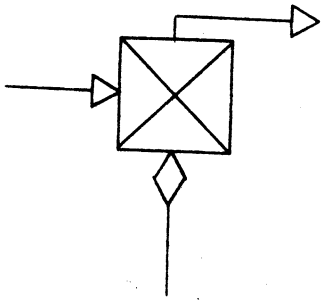
AN AND GATE IS DRAWN:



AN OR:



A DIODE CAPACITOR DIODE GATE (DCD GATE) IS DRAWN:



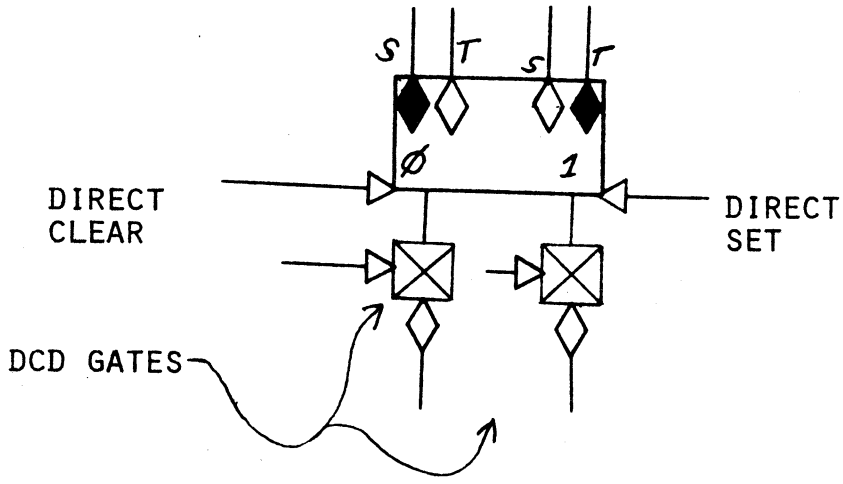
THE LEVEL INPUT MUST BE PRESENT 400 NS BEFORE THE PULSE

AFTER 400 NS THE LEVEL MAY BE REMOVED AND THE GATE CAN STILL BE SATISFIED WITH A PULSE WITHIN THE NEXT 200 NS

REGARDLESS OF INPUT SYMBOLS, THIS GATE REQUIRES HIGH INPUTS

FLIP FLOPS ARE DRAWN:

FF'S HAVE ONLY TWO OUTPUT PINS (S AND T). WHEN THE FE IS CLEARED, S WILL BE -3V; WHEN IT IS SET T WIL BE -3V.



THESE FLIP FLOPS ARE INTERNALLY COMPLEMENTED AND MAY BE COLLECTOR TRIGGERED.