EK-ADV11-OP-002

ADV11-A, KWV11-A, AAV11-A, DRV11 user's manual

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

This manual contains information necessary for the Operation, installation, and maintenance of the family of real-time analog and digital I/O devices which DEC provides as Options for the LSI-11 Processor, i.e., the ADV 11 -A Analog-to-Digital Converter, the KWV11-A Real-Time Clock, the AAVI I-A Digital-to-Analog Converter, and the DRV1 1 Parallel Line Interface. Operating information for each device is provided in a chapter specific to that device which includes functional description, specifications, theory of Operation, and programming background. Installation and maintenance information is provided for all units in Chapter 6.

All members of the LSI-11 real-time I/O family are designed to interface between the processor and analog or digital Signals in the world external to the processor. All devices are configured on one quad or double-height board designed to mount in an LSI-11 backplane or expander box and to receive power from LSI-11 supplies. All communicate with the LSI-11 bus and receive interrupt priority as a function of their location in the backplane. Finally, all have facilities to permit users to assign device addresses, and where appropriate, interrupt vector locations.

A number of recommendations are made in this text regarding specific interfacing configurations and general good practice. However, no specific interfacing claims are made over and above those expressed in the general specifications for each module. The responsibility for connecting DEC modules to external equipment rests ultimately with the user.

1.2 REFERENCES

- *Microcomputer Handbook (EB-06583 76 09/53)*
- *LSI-11 Bus Specification*

CHAPTER 2

ADV11-A ANALOG-TO-DIGITAL CONVERTER

2.1 GENERAL DESCRIPTION

The ADV11-A is a 12-bit successive-approximation analog-to-digital converter with built-in multiplexer and Sample-and-hold for use on the LSI-11 bus. The multiplexer section accommodates 16 Single-ended or 8 quasi-differential inputs, and the converter section utilizes a patented auto-zeroing design that measures the sampled signal with respect to the offset of its own internal circuitry and thus effectively cancels out its own offset error contributions to the measurement.

A/D conversions are initiated either by program command, clock Overflow, or external events as determined by program control of the ADV11-A's Control/Status Register (CSR). The clock Overflow command is supplied by the KWV11-A clock Option. External event inputs may originate directly from user equipment or from the Schmitt trigger output on the KWV11-A clock. Digital A/D conVersion data is routed through a buffer register to the LSI-11 for programmed transfer into memory. This buffering optimizes the throughput rate of the converter by allowing data from one conversion to be transferred to the processor after a subsequent conversion begins.

A vernier offset digital-to-analog converter is included in the ADV11-A's analog circuitry to facilitate very accurate program-controlled trimming of the A/D's offset. Three test signals - two dc levels and one bipolar triangular waveform - are available for use on any channel input. The triangular wave can be used in conjunction with diagnostic Software and the vernier DAC to produce extremely thorough and precise analog testing.

2.2 SPECIFICATIONS

2.2.1 Electrical (@ 25" C unless otherwise specified)

Inputs

Analog Input Protection	Fusible resistor guaranteed to open at ±85 V within 6.25 seconds. Guaranteed not to open from -20 V to +15 V at the input. Overload affects no components other than the fusible resistor on the overloaded channel; no other channels are affected.
Logic Input Protection	Fusible resistor guaranteed to open at ± 25 V within 6.25 seconds. Guaranteed not to open from -3 V to +8 V at the input.
Analog Input Full Scale Range (FSR)	10.24 V bipolar (-5.12 V to +5.12 V)

Inputs (Cont)

Analog Input Dynamic Resistance (/Vin/ ⩽ 5.12 V)	100 MΩ, minimum
Analog Input Bias Current (/Vin/ ⩽ 5.12 V)	50 nA, maximum
Logic Input Voltages	Low = 0.0 to +0.7 V; high = +2 V to +5 V
Logic Input Currents	Low = -6.8 mA at 0 V in.; high = +1.3 mA at i-5 V in
Logic Input Rise/Fall Time	400 ns, maximum

2.2.2 Coding

A/D Converter

Resolution	12 bits, binary weighted
Format	Parallel offset binary, right justified

Input Voltage	Output Code
+FS-1 LSB	7777
0	4000
-FS	0

(FS = 5.12 V; 1 LSB = 2.5 mV)

Vernier D /A

Resolution	8 bits, binary weighted
Format	Offset binary encoded

Input Code	Approximate Offset Voltage
377	+2.5 A/D LSB (+6.4 mV)
200	0
0	-2.5 A/D LSB (-6.4 mV)

2.2.3 Performance

Gain Error	Adjustable to zero
Offset Error	Adjustable to zero
Differential Linearity	No skipped states; no states wider than 2 LSB. 99% of state-widths ± 1/2 LSB
I ntegral Linearity	± 1 LSB, maximum non-linearity (referenced to end points)

Performance (Cont)

Temperature Coefficients	Gain = 6 ppm per degree C Linearity = 2 ppm of full-scale range per degree C Offset = 7.5 ppm of full-scale range per degree C
Noise	Module = 0.4 LSB rms; 2 LSB peak System = 1/2 LSB rms; 2 LSB peak
Warm-Up Time	5 minutes, maximum

2.2.4 Timing

External Start	Low level pulse, 50 ns minimum to 10 μs maximum; conversion starts on leading edge
Synchronization	0 to T
Conversion Time	16T (T = clock period = 2.14 μs ± 6%)
Transition Interval*	9 μs ± 12%
Sample and Hold	Aperture Delay = 200 ns Aperture Uncertainty = 2 ns

2.2.5 Test Signals

The ADV11-A provides three output voltages for test purposes:

1. Positive dc level, +4.4 V (± 15%)
2. Negative dc level, -4.4 V (± 15%)
3. Triangular wave, 15 Hz nominal (± 15%)

2.2.6 Environmental (Ref: DEC STD 102, class B)

2.2.7 Power Requirements

+5 Vdc ±5% @2.0 A, maximum
+12 Vdc ±3% @450 mA, maximum

2.3 FUNCTIONAL DESCRIPTION

The ADV11-A performs its function in seven successive steps:

1. It enables the specified channel.
2. It samples 1 of 16 Single-ended (or 1 of 8 differential) analog input channels specified by the control program long enough to acquire a reliable internal reference equivalent.
3. It accepts a command to perform an A/D conversion.
4. It holds the sampled reference equivalent during 12 successive interrogation intervals.

*Reacquisition interval between end of conversion or channel change and start of new conversion.

5. When the least significant bit has been resolved in the Successive Approximation Register (SAR), the ADV11-A transfers the contents of the now-filled SAR to the DATA Buffer Register (DBR) where that data can be accessed by the processor.

6. It informs the processor that conversion data is available.

7. It reacquires and tracks the programmed channel.

These steps are implemented in the ADV11-A by components that can be grouped together in four functional categories:

1. C hannel selection

2. A/D conversion

3. Processor/ADV11-A interface

4. Control logic that coordinates the above steps with respect to one another and to the needs of the processor.

These categories are discussed below.

2.3.1 Channel Selection

Channel selection is accomplished under program control by two 8-channel multiplexers and is a function of the data asserted in bits 8 through 11 of the Control/Status Register (CSR). Each of the 16 analog input channels is routed to the single output channel through a MOS field-effect transistor which acts as a normally-open switch. During the sample interval, the data pattern in CSR bits 8 through 11 selects one of these transistors and causes it to change from a condition of nearly infinite resistance (1 GΩ or more) to one of very low resistance (1000 Ω or less). Since in the selected state the transistor conducts current within the ±5.12 V limits equally well in both directions, it now functions as a closed switch, effectively routing to the output line whatever analog signal is connected to its input.

2.3.2 A/D Conversion

A/D conversions can be initiated in three ways: under program control, on Overflow from the KWV11-A Real-Time Clock, or on external input. When a conversion is completed or the control program writes a multiplexer address into the CSR, the control logic initiates the Transition Interval – a delay of about 9 μs to allow the multiplexer adequate selection and settling time and to permit a valid representation of the signal level to be established in the sample circuit. If no A/D Start signal has occurred by the time the Transition Interval has elapsed, the sample circuit merely follows the signal transmitted to it through the selected multiplexer channel and waits for an A/D Start Signal. When an A/D Start signal occurs – or at the end of the Transition Interval if A/D Start was previously generated by the writing of the CSR GO bit – the sample and hold circuits are switched to hold, sustaining the sampled level for the next step. The multiplexer output is then set to its hold condition, i.e., to ground if the Single-ended (SE.) input is set low for Single-ended measurement, to the second differential input (return line) if the S.E. input is not set low. Note that if an external or clock start signal occurs during the Transition Interval, conversion starts immediately without waiting for the Transition Interval to be completed. Bit 15 of the CSR (AD ERROR) is set, however, and an interrupt is generated if bit 14 (error interrupt enable) is set – alerting the program that conversions are occurring too fast and are consequently liable to be in error.

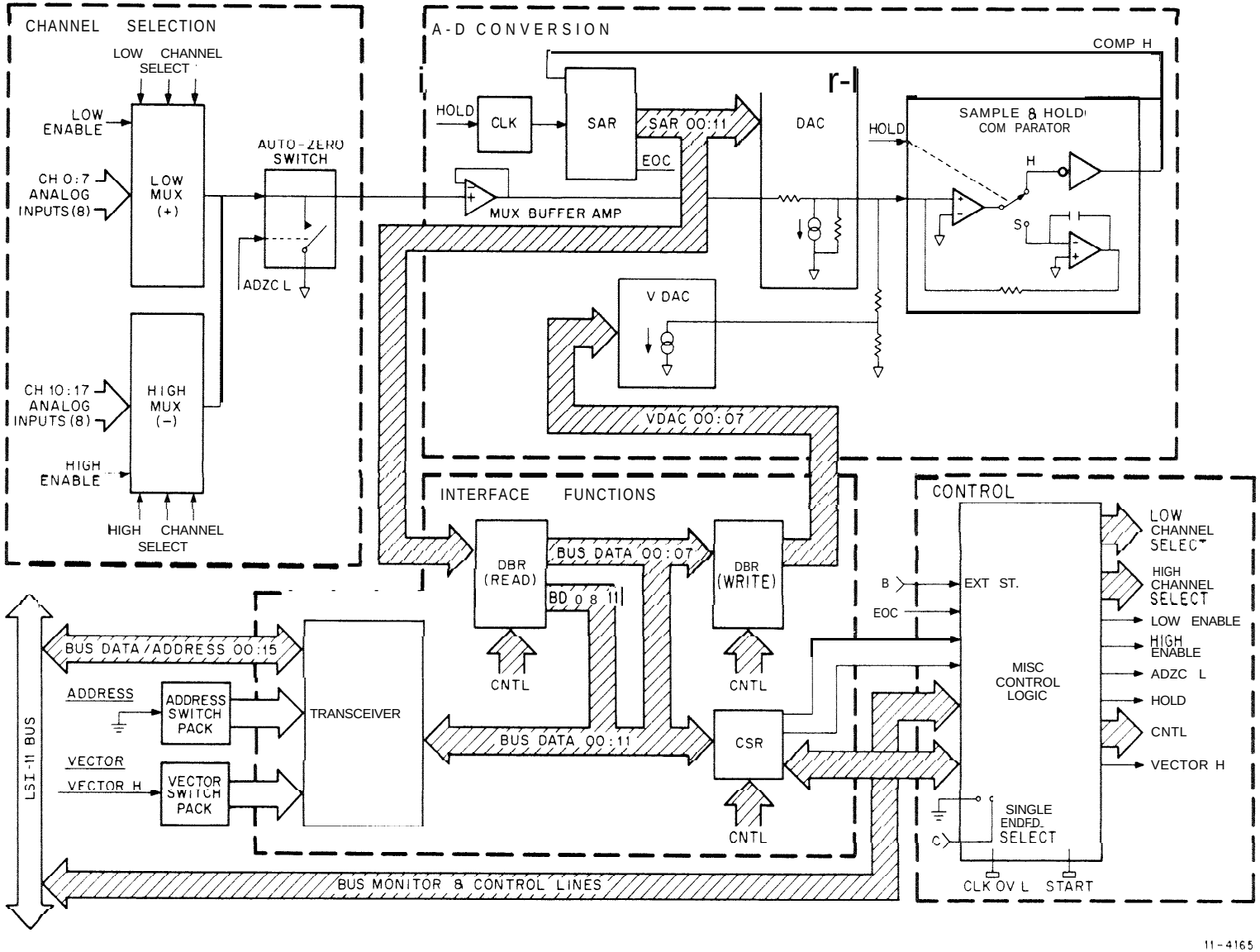


Figure 2-1 ADV11-A Functional Block Diagram

Under normal conditions, it is not until the Transition Interval is complete that the measurement process is begun. The Successive Approximation Register (SAR) is cycled through 13 states by the clock. In the first state its output code involves only the most significant bit (MSB) of the 12-bit SAR word. This output code causes the feedback digital-to-analog converter (DAC) to generate an output equivalent to that produced by the hold circuits in response to a sample voltage of 0. The DAC output is summed with that produced by the hold circuits and with that coming from the grounded multiplexer output (Single-ended mode) or from the second differential input (quasi-differential mode). If the current from the summing node is negative, the first approximation was too low, and the comparator Signals the SAR to maintain the state of bit 11 and repeat the process with bit 10. If the current from the summing node is positive, the first approximation was too high and the SAR changes the state of bit 11 before cycling into the second approximation. This process continues until all 12 bits in the word have been set, tested, and if necessary, changed. The 13th state (end of conversion, or EOC) indicates that the measurement is complete and that the SAR now contains an offset binary equivalent of the sampled voltage and may therefore be transfered to the processor. EOC causes the sample and hold circuits to return to the sample mode and to reset the SAR, preventing further SAR activity until the occurrence of the next hold condition.

Note that because the reference point against which the sample voltage is compared is at the output of the multiplexer itself rather than internal to the sample and hold circuits, all offset voltages generated by the intervening circuits are common to both sample and hold conditions and are therefore cancelled out of any measurement. In Single-ended mode, grounding the multiplexer output (and thereby establishing this reference point) is identified as auto-zeroing the converter.

2.3.3 Interface Functions

In addition to stopping the SAR clock and reestablishing the sample mode, the end-of-conversion signal also initiates the process that causes the SAR data to be transferred to the processor. Since this Operation takes a finite amount of time which would interfere with subsequent measuring operations, the SAR data is first transferred to a holding device, the Data Buffer Register (DBR), where it will remain until the processor can be notified to read the conversion data for processing. In the meantime, the channel selection and A/D conversion circuits can begin the next measurement as dictated by Control/Status Register (CSR) bit conditions controlled by the processor.

Included in the ADV11-A interface is an extension of the DBR designed to accept 8-bit write information from the BUS DATA/ADDRESS lines. This buffer permits programmed setting of the Vernier DAC (see Paragraph 6.2.2.3). Also included are transceivers that connect the bi-directional BUS DATA lines to the LSI-11 Bus DATA/ADDRESS lines. Associated with these transceivers are switches that permit assigning device and vector addresses to any given A DV11-A.

2.3.4 Control

As the above discussion suggests, a large number of Signals must be precisely orchestrated each time the ADV 11-A executes a conversion. The control logic contains an assortment of gates, latches, read-only memories, and timing circuits designed to assure that multiplexer channels are properly selected, sample durations are of adequate length, conversions are not initiated during uncompleted previous conversions, etc. In general, this logic precludes the need for the user to attend to any but the most-elementary details of the conversion process, e.g., making necessary connections to the system and writing control programs that make appropriate use of the CSR.

2.4 USER INTERFACING

2.4.1 Analog Inputs

2.4.1.1 Single-Ended Mode* - Single-ended analog input signals for the ADVV11-A may be of two types, grounded and floating. A grounded input is one whose level is referenced to the ground of the instrument that is producing it, as illustrated in Figure 2-2. Since the instrument may be located at a

*The ADV11-A is factory-set for differential mode. Single-ended mode must be selected as described in Paragraph 2.4.3.3.

distance from the Computer, there may be some voltage difference between the instrument ground and the Computer ground. The voltage seen by the ADV11-A will be the sum of the undesired ground difference voltage and the desired instrument signal voltage. In cases where such differences are encountered, they can be minimized by plugging the instrument into an ac outlet as close as possible to that providing power to the Computer. Do *not* run a wire from user's ground to the ADV11-A analog ground. Such a wire can cause ground loop currents which affect results not only on the input channel in question, but also on other channels.

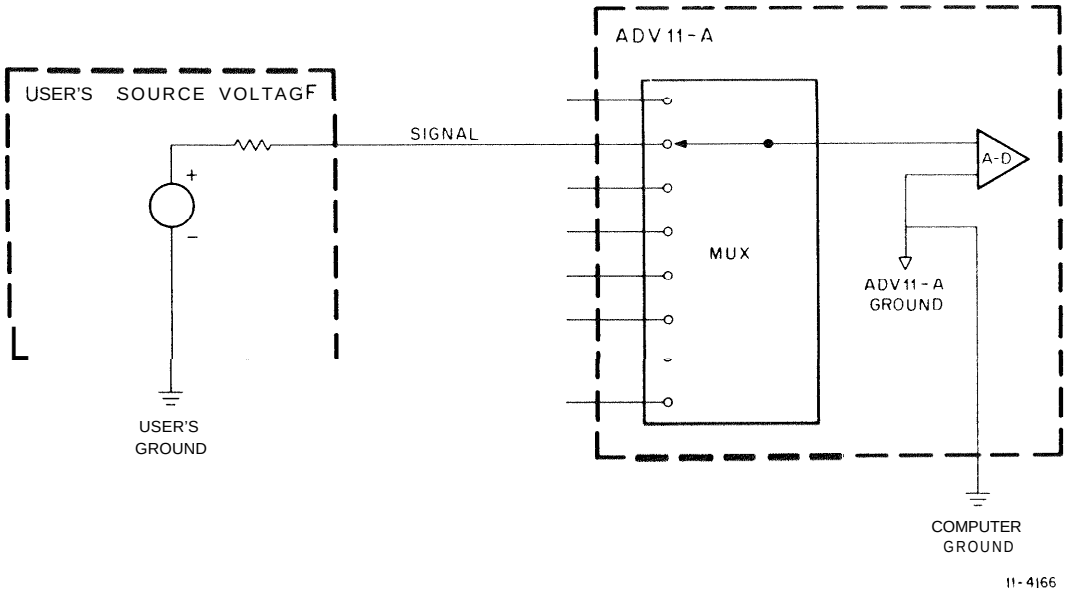


Figure 2-2 Single-Ended Input Referenced to User's Ground

A floating input is one whose signal voltage is developed with respect to a point not connected to ground, as illustrated in Figure 2-3. The identifying characteristic of a floating source is that connecting the signal return to the ADV11-A ground does not result in a current path between the ADV11-A ground and the instrument ground.

Note that the return of a floating input must be connected to one of the ADV11-A's analog ground terminals (see Figure 2-3). Ground points may be shared among channels, as illustrated by the battery-powered sources in Figure 2-3.

2.4.1.2 Quasi-Differential Mode - The "quasi" prefix in "quasi-differential" can best be explained in the context of a preliminary review of true differential Operation. A true differential input involves two signal lines connected to a differential amplifier in such a way that the output of the device is a function of the instantaneous *difference* between the voltages on the two signal lines. One advantage of such a configuration is illustrated in Figure 2-4.

Figure 2-4(a) assumes a Single-ended generating device that produces a signal, V_S, with respect to its ground and is situated sufficiently far from the receiving device for a significant noise voltage, V_n, to be developed in the power distribution ground lines. The result is that, at any given instant, the differential amplifier in the receiving device sees both the signal voltage and the noise voltage. Its output, V_O, is a function of $V_S + V_n$ and is in error with respect to V_S alone.

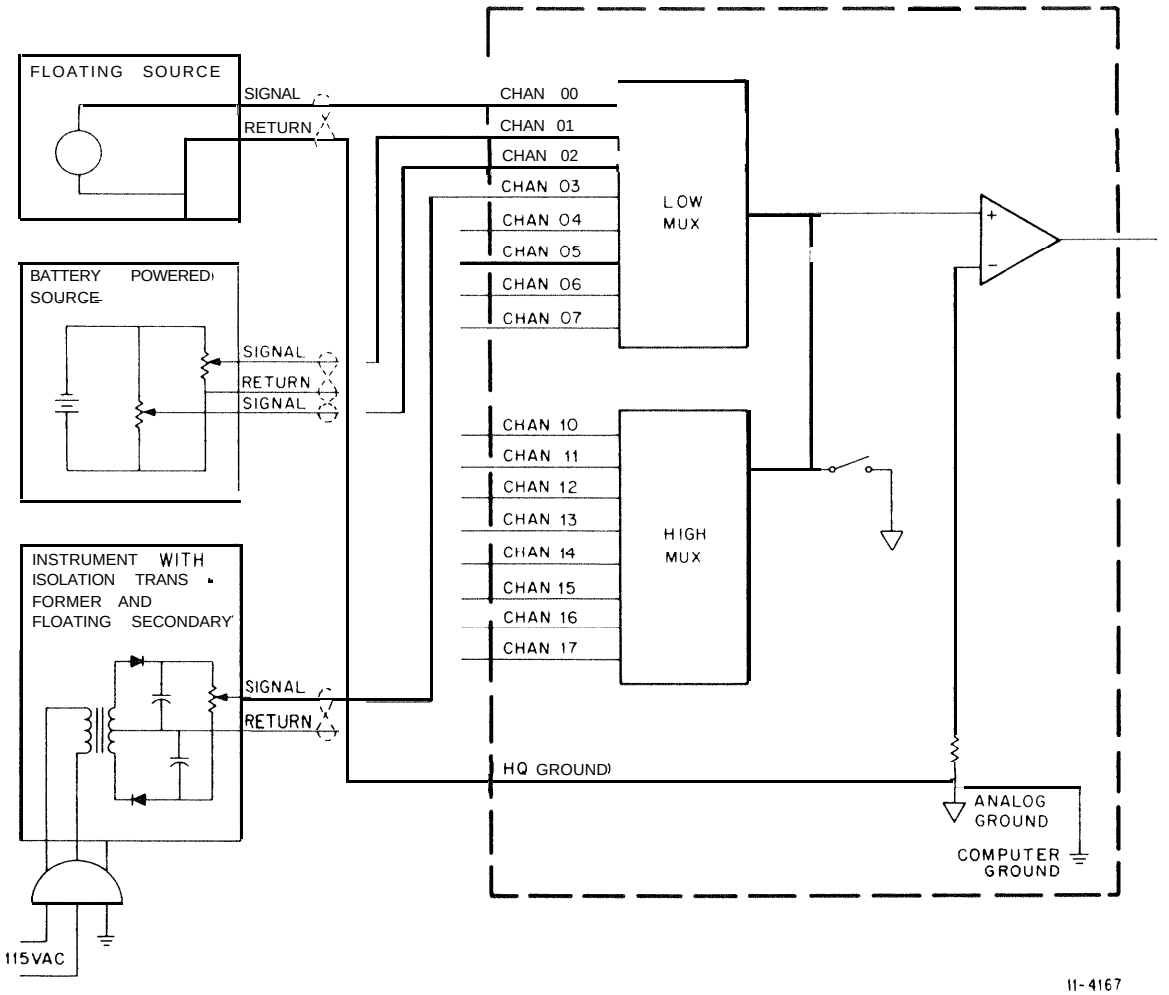


Figure 2-3 Floating ADV11-A Input Signals

Figure 2-4(b) illustrates the same device connected in true differential mode. The same noise voltage exists in the power distribution ground System, but this time the generating device ground is connected directly to the negative input of the receiving differential amplifier. Since the instantaneous noise voltage is common to both the + and the – inputs, it is cancelled out of the final amplifier output. V_o now provides a valid representation of V_s alone.

Figure 2-5 illustrates the ADV1 1-A operating in the quasi-differential mode.

The major contrast between true differential Operation as described above and the Operation of the ADV1 1-A in differential mode is that in the latter, the two sides of the signal are not simultaneously input to a differential amplifier. Rather, their difference is established by a sequential Operation that first samples the voltage at one of the two inputs and then, holding this value fixed, in effect subtracts from it the voltage at the second input. For near dc conditions, this procedure produces a result like that of true differential Operation – that is, the output is a function of the difference between the two input voltages, and common mode voltages are cancelled out. But, since there is a significant time lapse between taking the sample and completing the final approximation, a possibility for error is introduced by the ADV l l-A that increases as a function of common mode signal frequency. The result

is that the common mode rejection ratio, while essentially infinite at dc, rolls off for ac Signals, and is about 40 dB at 60 Hz line frequency. In addition, since the holding action of the Sample-and-hold circuit is only in effect on the first (non-inverting, signal) input but not on the second (inverting, return) input, the voltage rate of change on the second input should be kept below 25 mV/ms. This is the slope that results in a quarter-LSB change during the conversion interval. Such a rate of change corresponds to 125 mV peak-to-peak at 60 Hz line frequency. This dynamic response difference between the two inputs requires us to distinguish the ADV11-A's differential mode from true differential Operation. Hence the term "quasi-differential."

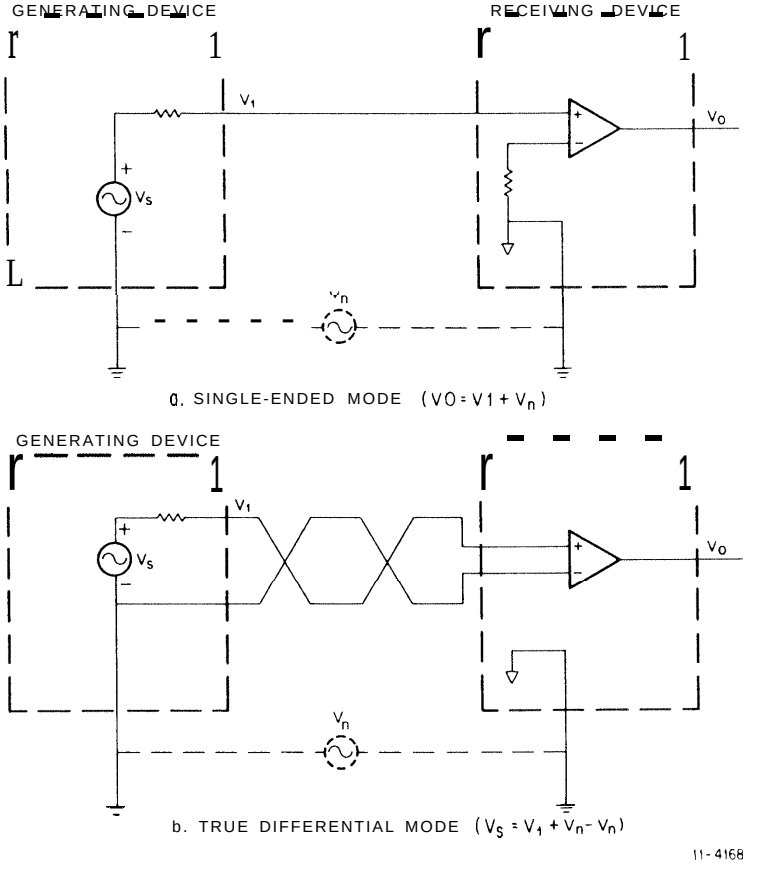
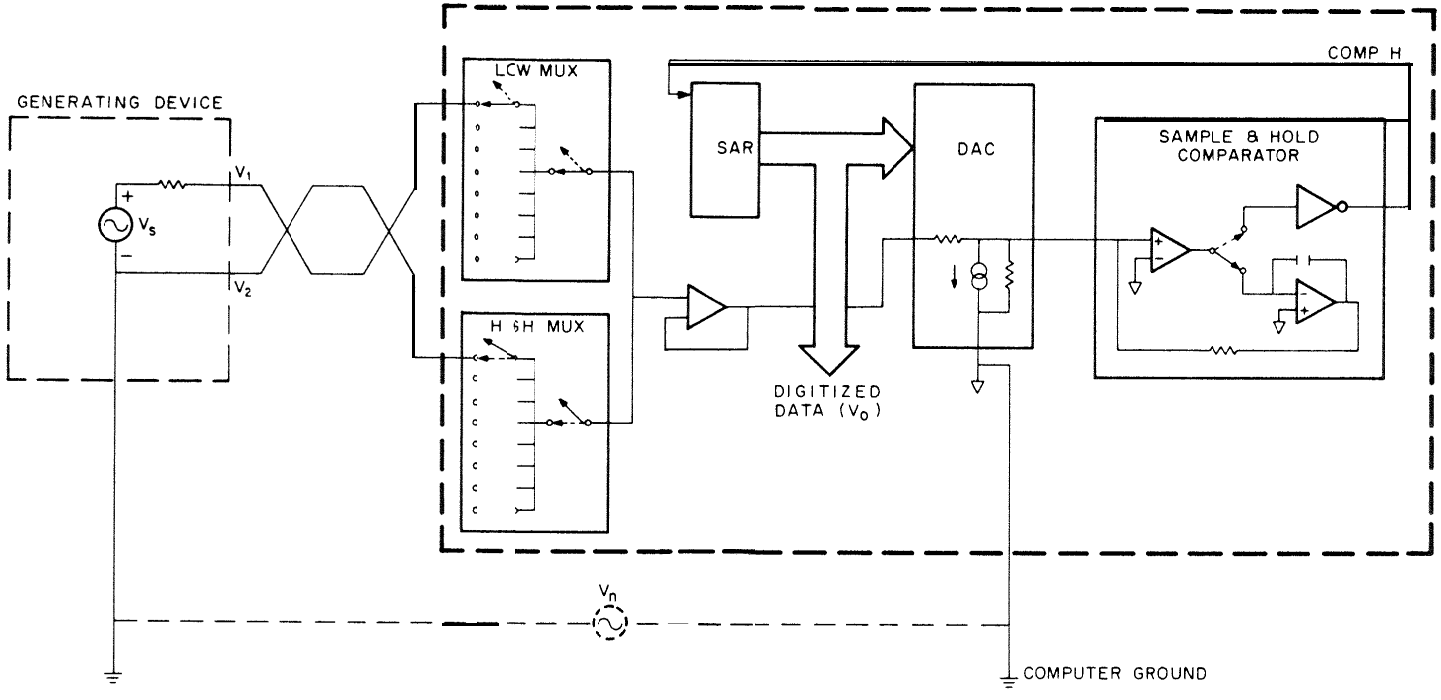


Figure 2-4 Single-Ended Versus True Differential Input Modes

2.4.2 Avoiding Spurious Signals

As a preliminary step, confirm that the Computer power supply ground is connected to power line (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the power supply ground and a convenient point associated with earth ground. (All DECLAB 11/03 systems are provided with this connection at the factory.)

2.4.2.1 Twisted Pair Input Lines - The effects of magnetic coupling on the input signals may be reduced for floating Single-ended or differential inputs by twisting the signal and return lines in the input cable. If the inductive pickup voltages of the two leads match, the net effect seen at the ADV11-A input is zero. Use of twisted pairs has no effect with a Single-ended non-floating signal (referenced to ground at the instrument end).



FOR dc CONDITIONS :

$V_o = V_1 - V_2 = (V_s + V_n) - V_n = V_s$

FOR ac CONDITIONS :

$V_o = V_1(t_1) - V_2(t_2) = V_s(t_1) + [V_n(t_1) - V_n(t_2)]$

NOTE :

Solid switch positions indicate sample state (t_1); dotted positions indicate holdtate (t_2)

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Figure 2-5 ADV11-A Qusi-Differential Mode

2.4.2.2 Shielded Input Lines - The effects of electrostatic coupling on the input Signals may be reduced by shielding the signal wires. This is especially important if the instrument or transducer has high source impedance. To prevent the shield from carrying current and thus developing ground loop voltages within the ADV1 I-A, connect it to ground at the instrument end only.

2.4.2.3 Allowing for Input Settling with High Source Impedance - All solid-state multiplexers inject a small amount of charge into their input lines when changing channels, causing a transient error voltage that is discharged by the input signal's source impedance. The ADV11-A shares this characteristic, and also injects a small charge into the selected input line at the end of each conversion when the auto-zero switch is turned off (see Paragraph 2.3.2). After any channel change and after any conversion, the ADV 1 1-A's control logic allows a 9 μs interval (identified as the Transition Interval) during which conversions cannot start without generating error conditions. Normally, this is sufficient time for the input transient to settle out. However, more time may be needed when the multiplexer is switching into an input channel with high source impedance, particularly when large amounts of shunt capacitance exist in the interconnecting cables. Source impedance/cable shunt capacitance products greater than 1 μs should be avoided whenever conversions are to be made at maximum rate with less than 1/2 LSB error. This means that cable shunt capacitance for a 1000 Ω source should not exceed 1000 pF ($10^3 \times 10^{-9} = 10^{-6}$), that shunt capacitance for a 100 Ω source should not exceed 0.01 μF ($10^2 \times 10^{-8} = 10^{-6}$), etc. Assuming twisted pair cable capacitance of 50 pF/foot, these constraints translate into a maximum run of 20 feet from a 1000-Ω source, 200 feet from a 100-Ω Source, etc. Note that these values are consistent with good practice for avoiding noise pickup in long cable runs. Note also that settling errors can be eliminated by increasing the time between conversions or incorporating a Software delay between channel changes and program start commands.

2.4.3 Connections

Figure 2-6 illustrates the location of user connectors and switches on the component side of the ADV11-A board.

Analog input Signals are input to the ADV1 1-A through the 40-pin connector. Pin assignments for the connector are shown in Figure 2-7. The proper Berg-to-Berg cable is the BC08R; the proper Berg to prepared open-ended cable is the BC04Z. (See Maintenance chapter for further information.)

2.4.3.1 Distribution Panel - Figure 2-8 shows an H322 Distribution Panel that is connected on the rear to the ADV1 1-A Berg connector and on the front provides easily identifiable and conveniently accessible barrier strip connections for user apparatus. Each H322 accommodates two ADV1 l-As or one ADV11-A and one other Single-connector device. The ADV11-A is shipped with decal sets that specifically identify ADV11-A inputs and Outputs. Note that the H323-B Potentiometer Box may *not* be used with the ADV1 1-A. (See Maintenance chapter for appropriate Potentiometer box circuit.)

2.4.3.2 External and Clock Starts - The external start signal line, pin B of the Berg connector or TAB S (see Figures 2-6 and 2-7), is a TTL-compatible input that presents five unit loads (8.0 mA) to any driving output. Conversions start on the high-to-low transitions of this Signal.

In most cases, the external start signal will be produced by a grounded (non-floating) pulse generator or logic circuitry located in a grounded instrument. The return path for the External Start signal will be through the power line ground System. For this reason, ground differences between source and computer should be minimized to prevent spurious start pulses due to ground noise. In no case should a separate return line be run between grounded source and the Computer ground. Only with floating devices should return lines be run between source logic ground and logic ground pins on the ADV11-A Berg connector. External devices that require buffering can be interfaced to the ADV 1l-A through Schmitt Trigger 1 of the KWV11-A clock (ST1). Connection is made by means of a DEC 7010771 type jumper (Figure 2-9) to TAB S (Figure 2-6) of the ADV11-A.

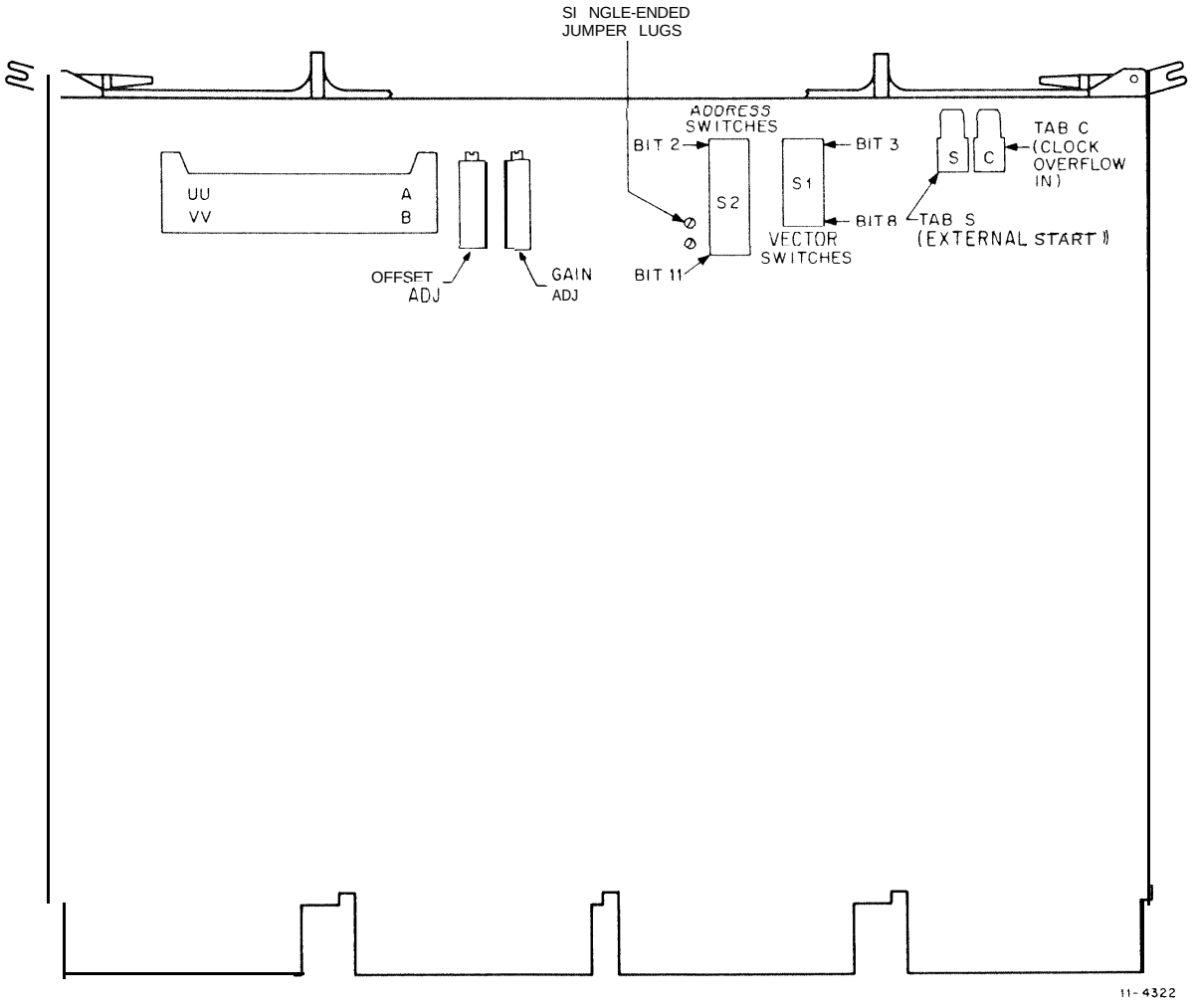


Figure 2-6 ADV 11-A Connectors and Switches

Conversions that must be initiated in consequence of time intervals or on every nth external event may be triggered from the KWV11-A through a DEC 7010771 type jumper connected from the clock output tab (CLK) to the ADV11-A clock Overflow tab (C).

2.4.3.3 Mode Control - The ADV11-A is equipped with jumper lugs (see Figure 2-6) that permit changing operating mode from quasi-differential (no connection) to Single-ended (jumper installed). The Single-ended mode can also be selected by connecting Berg connector pin C to logic ground. This alternative is provided to permit convenient external mode selection in installations that require frequent alternation between one mode and the other.

2.4.4 Vector and Address Selection - Device and vector addresses are assigned to the ADV 11-A by means of two switch packs (S2 and S 1, Figure 2-6). S2 is a pack containing 10 single-pole/single-throw switches, numbered 1- 10, that communicate with data lines BDAL 2-l 1. Assuming BDAL lines 12-15 to be set by the processor to 1, S1 permits assigning any address between 170000 and 177774. The recommended address for the ADV1 1-A Status Register is 170400, set as illustrated in Figure 2-10(a). The Data Buffer Register automatically receives the next even address following that assigned to the CSR.

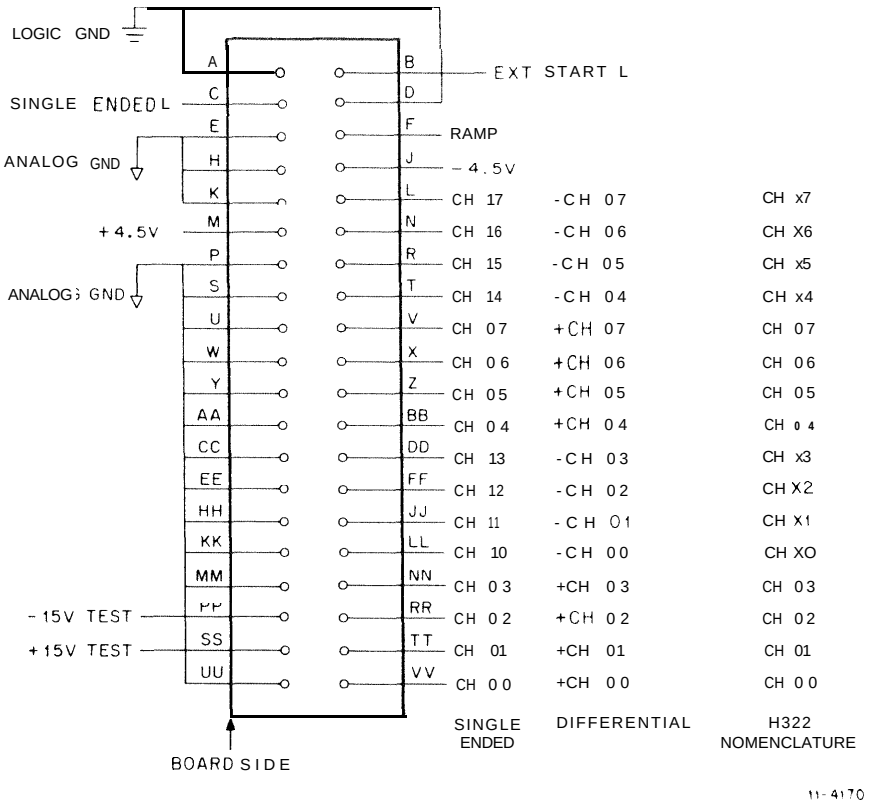


Figure 2-7 ADV1 1-A 40-Pin Connector Pin Assignments

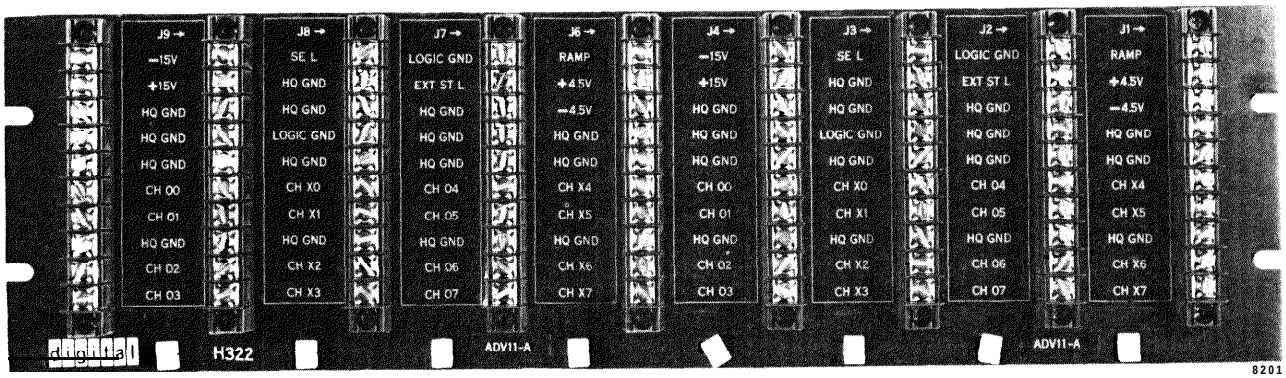


Figure 2-8 H322 Distribution Panel

The A/D done interrupt vector address is set by means of S1, an 8-switch pack of which only six switches are utilized. These switches communicate with BDAL lines 3 through 8 and can be set in increments of 10_8. The error interrupt vector automatically receives an address that is four locations higher than the A/D done interrupt vector whose recommended address is 000400 [see Figure 2-10(b)].

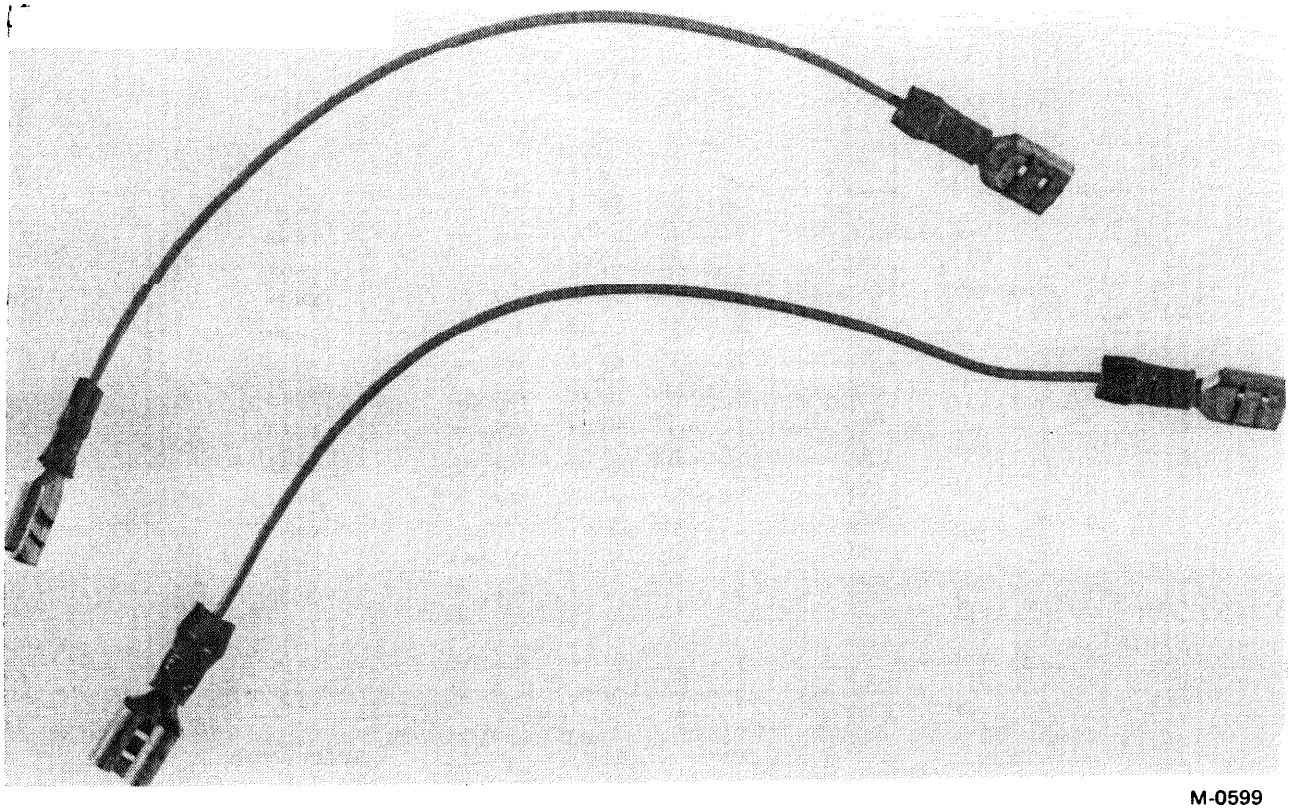


Figure 2-9 Module Jumpers

2.5 PROGRAMMING

2.5.1 Control/Status Register (CSR)

The significance of the CSR bits is defined below:

Bit 15: A/D ERROR (Read/ Write) - The A/D ERROR may be program set or cleared and is cleared by the processor INITIALIZE. It is set by any of the following conditions:

1. Attempting an external or clock start during the transition interval (see Paragraph 2.3.2)
2. Attempting any start during a conversion in progress
3. Failing to read the result of a previous conversion before the end of the current conversion.

Bit 14: ERROR INTERRUPT ENABLE (Read/ Write) - When set, enables a program interrupt upon an error condition (A/D ERROR). Interrupt is generated whenever bits 14 and 15 are set, regardless of which was set first.

Bits 13-12: Not used.

Bits 11-8: MULTIPLEXER ADDRESS (Read/ Write) - Contain the number of the current analog input channel being addressed.

Bit 07: A/ D DONE (Read) - Set at the completion of a conversion when the data buffer is updated. Cleared when the data buffer is read and by the processor INITIALIZE. If enabled interrupts are requested simultaneously by both bits 07 and 15, bit 07 has the higher priority.

Bit 06: DONE INTERRUPT ENABLE (Read/ Write) - When set, enables a program interrupt at the completion of a conversion (A/D DONE). Interrupt is generated when bit 07 and bit 06 are both set, regardless of sequence.

Bit 05: CLOCK STAR T ENA BLE (Read/ Write) - When set, enables conversions to be initiated by an Overflow from the clock Option.

Bit 04: EXTERNAL STA RT ENABLE (Read/ Write) - When set, enables conversions to be initiated by an external signal or through a Schmitt trigger from the clock Option.

Bit 03: ID ENABLE (Read/ Write) - When set, causes bit 12 of the Data Buffer Register to be loaded to a 1 at the end of any conversion.

Bit 02: MAINTENA NCE (Read/ Write) - Loads, when set, all bits of the converted data output equal to Multiplexer Address LSB (bit 08) at the completion of the next conversion. Cleared by the processor INITIALIZE. Used for "all Os" and "all 1s" tests of A/D conversion logic.

Bit 01: Not used.

Bit 00: A/ D STA R T (Read/ Write) - Initiates a conversion when set. Cleared at the completion of the conversion and by the processor INITIALIZE.

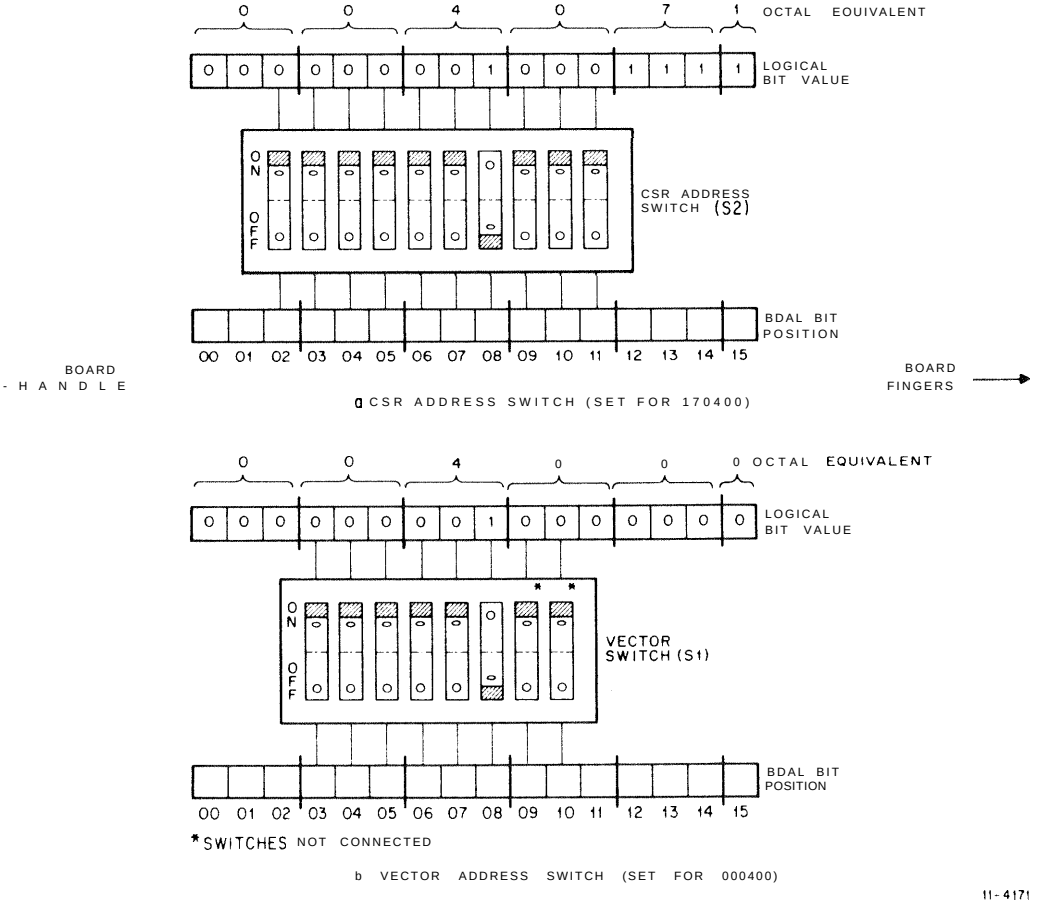


Figure 2- 10 ADV 11-A Address and Vector Switches (Rocker or Slide Switches)

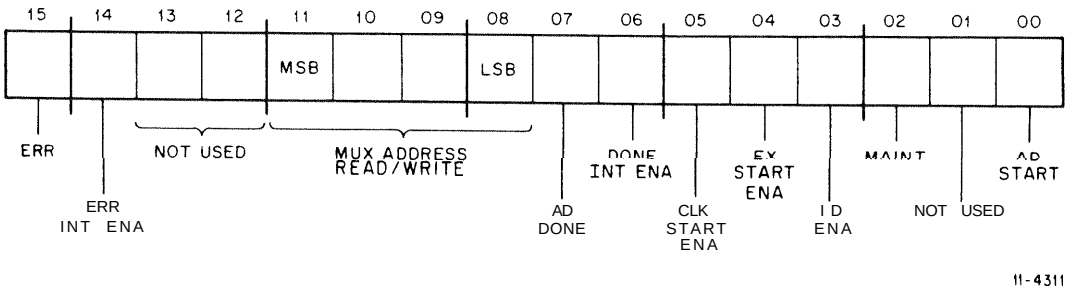


Figure 2- 11 ADV 1 l-A Control/Status Register (CSR)

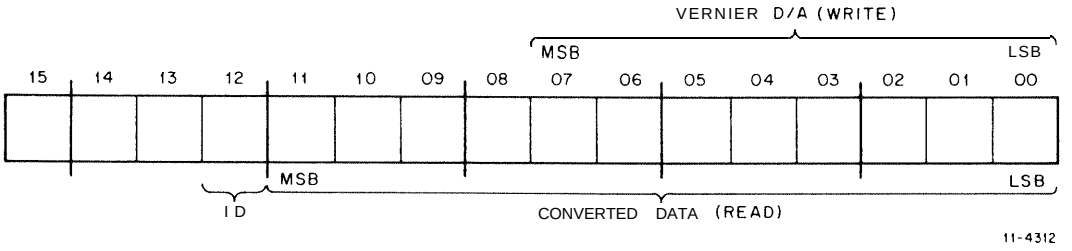


Figure 2- 12 ADV1 1-A Data Buffer Register (DBR)

2.5.2 Data Buffer Register (DBR)

The DBR is actually two separate registers - one read only, the other write only.

Read Only (Cleared at processor initialize)

Bits *15–13*: Not used. Should read as 0.

Bit 12: ID (Read) - When ID ENABLE (bit 03) of the CSR has been set, DBR bit 12 will be loaded to a 1 at the end of conversion.

Bits 1 1–00: CON VERTED DA TA (Read) - These bits contain the results of the last A/D conversion.

Write Only (Set to 200_8 at processor initialize)

Bits 15–08: Not used.

Bits 07–00: VERNIER D/A (Write) - These bits provide a programmed offset to the converted value (scaled 1 D/A LSB = 1/50 A/D LSB). The hardware initializes this value to 200_8 (mid-range). Values greater than 200_8 make the input voltage appear more positive.

2.5.3 Programming Example

Read 100_8 A/D conversions from channel 0 into locations 4000_8–4176_8 and halt.

```
START:  CLR     @ADSR           ;CLEAR A/D STATUS REGISTER
        MOV     #4000,R0        ;SET UP FIRST ADDRESS
        INC     @ADSR           ;START A/D CONVERSION
LOOP:   TSTB    @ADSR           ;CHECK DONE FLAG
        BPL     LOOP            ;WAIT UNTIL FLAG SE:?
        INC     @ADSR           ;START NEXT CONVERSION*
        MOV     @ADBR,(R0)+     ;PLACE CONVEPTEG VALUE
                                ;FROM A/D BUFFER INTO MEMORY
                                ;LOCATION AND SET UP NEXT
                                ;LOCATION FOR TRANSFER*
        CMP     R0,#4200        ;CHECK IF 100 CONVERSIONS
                                ;HAVE BEEN DONE
        BNE     LOOP            ;NO, GE? NEXT CONVERSION
        HALT                    ;DONE
ADSR:   170400                  ;A/D STATUS REGISTER ADDRESS
ADBR:   170402                  ;A/D BUFFER REGISTER ADDRESS
        .END    START
```

*Starting a subsequent conversion before moving data from a previous conversion is to be recommended only with Systems equipped with non-processor memory refresh, as provided in the REV11 Options. Without this capability, data will be lost occasionally by CPU memory refresh intervening between the INC and MOV commands. In general, non-processor memory refresh is essential to realizing the full potential of the ADV11-A.

CHAPTER 3

KWV11-A PROGRAMMABLE REAL-TIME CLOCK

3.1 GENERAL DESCRIPTION

The KWV 11-A is a programmable clock/counter combination that provides a variety of means for determining time intervals or counting events. It can be used to generate interrupts to the LSI-11 processor at predetermined intervals, to synchronize the processor to external events, or to measure time intervals or establish programmed ratios between input and output events. It can also be used to start the ADV11-A Analog-to-Digital Converter either by clock counter Overflow or by the firing of a Schmitt trigger.

The clock counter has a resolution of 16 bits and can be driven from any of five internal crystal-controlled frequencies (100 Hz to 1 MHz), from a line frequency input or from a Schmitt trigger fired by an external input. The KWV11-A can be operated in any of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base.

The KWV 11-A includes two Schmitt triggers, each with integral slope and level controls. The Schmitt triggers permit the user to start the clock, initiate A/D conversions, or generate program interrupts in response to external events.

The physical structure of the KWV11-A is illustrated in Figure 3-1. The unit is contained on one quad size module whose fingers interface to the LSI-11 Bus. User interfacing for the Schmitt triggers and clock Overflow Signals is accomplished by means of a multi-pin connector (J1). FAST ON connectors (CLK, ST1) are provided to permit direct and simple connections of clock Overflow and Schmitt trigger Outputs to corresponding terminals on the ADV11-A A/D Converter. Switch packs permit selecting CSR (Control/Status Register) address, interrupt vector address, and Schmitt trigger slope and level conditions. Screwdriver controls (R 18 and R19) permit setting Schmitt trigger levels. Provision is also made via the multi-pin connector J1 for external user-provided slope switches and level controls.

3.2 SPECIFICATIONS (@ 25" C unless otherwise specified)

3.2.1 Clock

Oscillator Accuracy	0.01%
Range	Base frequency (10 MHz) divided into five selectable rates (1 M Hz, 100 kHz, 10 kHz, 1 kHz, 100 Hz); line frequency; Schmitt trigger 1 input

3.2.2 Input and Output Signals

All inputs and Outputs are TTL compatible unless otherwise specified.

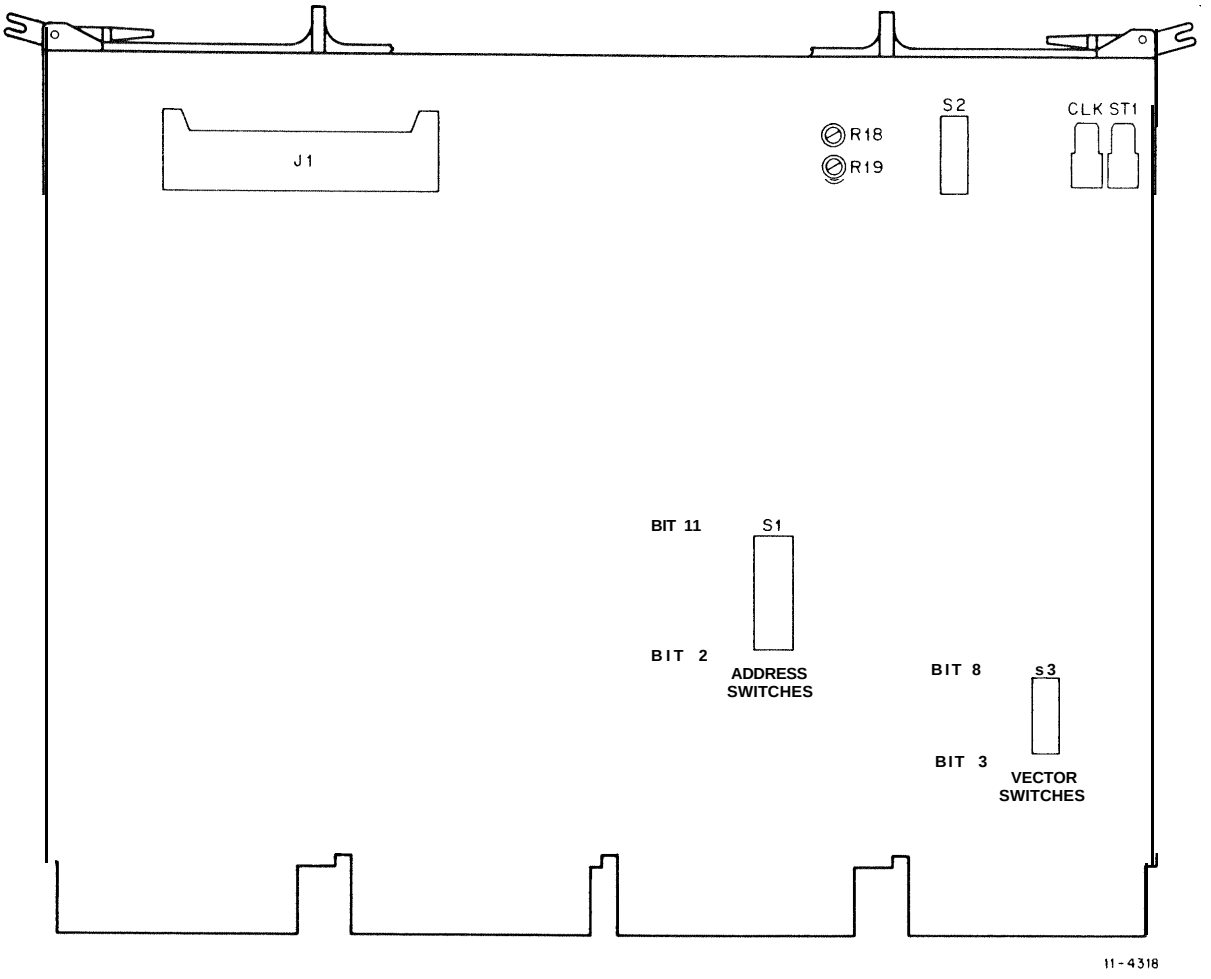


Figure 3-1 KWV11-A Connectors, Switches, and Contrals

3.2.2.1 Input Signals

1. ST1 IN (Schmitt Trigger 1 Input)

Input Range (maximum limits)	**-30 V to +30 V**
Assertion Level	Depends upon position of slope reference selector switch and level control; triggering range, -12 V to + 12 V
Origin	User device
Response Time	Depends upon input waveform and amplitude; typically 600 ns with TTL logic input
Hysteresis	Approximately 0.5 V, positive and negative
Characteristics	Single-ended input; 100 kΩ impedance to ground

2. ST2 IN (Schmitt Trigger 2 Input)

Same description as ST1 **IN**

3.2.2.2 Output Signals

1. CLK OV (Clock Overflow)

Asserted Level	Low
Destination	User device or ADV11-A
Duration	Approximately 500 ns
Characteristics	TTL open-collector driver with 470 Ω pull-up to +5 V
	Maximum source current from output through load to ground when output is high (≥ 2.4 V): 5 mA
	Maximum sink current from external source voltage through load to output when output is low (≤0.8 V): 8 mA

2. ST1 Out (Schmitt Trigger 1 Output)

   Same description as CLK OV

3. ST2 OUT (Schmitt Trigger 2 Output)

   Same description as CLK OV

3.2.2.3 Environmental (ref: DEC STD 102, class C)

3.2.2.4 Power Requirements (from LSI-11 Bus Power Supply)

+5 v	1.75 A typical
+12 v	10 mA typical

3.3 FUNCTIONAL DESCRIPTION

3.3.1 Bus Control

Figure 3-2 illustrates the KWV11-A in block diagram form.

The logic associated with the bus control block maintains proper communications protocol between the processor bus and the KWV11-A. This logic generates and monitors the bus Signals involved during interrupts and data transfers between the processor and the KWV11-A. It permits the KWV11-A to recognize when it is being addressed by the processor (address defined by the Address Switch Pack), to prescribe the location in memory pointing to the starting addresses of interrupt Service routines (by means of the Vector Address Switch Pack), to input control data from the processor, and to output data to the processor.

Interrupts can be enabled for both counter Overflow and Operation of ST2. Since each of these conditions raises a flag bit in the Control/Status Register, and since separate interrupt vectors exist for each condition, the conditions may be distinguished either by vectors or by testing flag bits.

3.3.2 Control/Status Register

The Control/Status Register (CSR) provides a means for the processor to control the Operation of the KWV11-A and to derive information about its operating condition. Bits are provided for enabling interrupts, mode selection, maintenance operations, starting the counter, and Overflow and Schmitt trigger event monitoring. (See Figure 3-9 and Table 3-1 .)

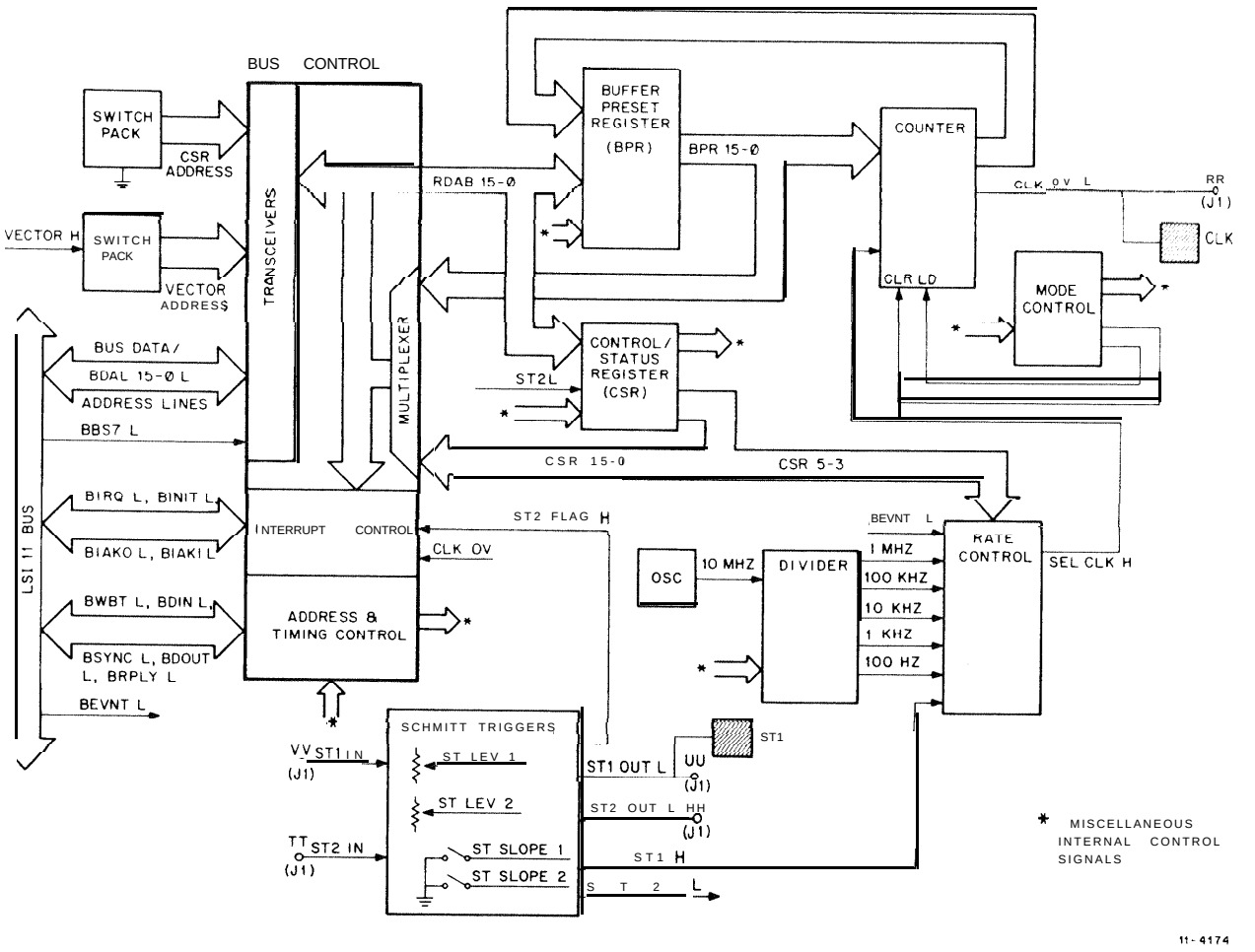


Figure 3-2 KWV 11-A Real-Time Clock Block Diagram

3.3.3 Mode Control

Logic circuitry associated with the mode control block permits KWV11-A Operation in four different modes as specified by bits 2-1 of the CSR.

3.3.3.1 Mode 0 (Single Interval)

When the GO bit is set in this mode either by the processor or by a Schmitt Trigger 2 event, the counter is loaded from the Buffer/Preset Register (which has previously been loaded with the 2's complement of the number of counts desired before Overflow). Once loaded, the counter will increment at the selected rate until it Overflows. Overflow clears the GO bit, sets the Overflow Flag, and interrupts the processor if that function has been enabled. If interrupt has not been enabled, the KWV11-A waits for processor intervention.

3.3.3.2 Mode 1 (Repeated Interval)

When the GO bit is set in this mode, the counter is loaded from the Buffer/Preset Register (BPR) and is then incremented to Overflow as for Mode 0. In Mode 1, however, Overflow does not clear the GO bit; instead, it causes the counter to be reloaded from the BPR, raises the Overflow Flag, initiates an interrupt sequence if the CSR Interrupt on Overflow bit is set, and causes the count to be continued with no loss of data.

3.3.3.3 Mode 2 (External Event Timing)

When the GO bit is set in this mode, the counter is set to 0 and then incremented at the selected rate as long as the GO bit remains set. An external signal to Schmitt Trigger 2 (ST2) causes the current contents of the counter to be loaded into the BPR while the counter continues to run. At the same time the ST2 Flag is set and, if Interrupt 2 is enabled, an interrupt is generated, thus permitting the program to read the value held in the BPR.

The counter continues to run after the ST2 event and also continues to run after Overflow. Interrupt on Overflow may be enabled to alert the program to the Overflow condition.

3.3.3.4 Mode 3 (External Event Timing from Zero Base)

Operation in Mode 3 is identical to that in Mode 2 except that the counter is zeroed each time an ST2 event loads its contents into the BPR.

3.3.3.5 Flag Overrun

In all modes, if a second Overflow occurs before the Overflow Flag is reset (i.e., before a prior event is serviced by the processor), or if ST 2 fires when the ST 2 flag is already set, the Flag Overrun bit is set.

3.3.4 Oscillator, Divider, Rate Control Chain

The circuitry associated with these blocks provides the time base that is fed to the counter. The KWV 11-A permits eight clock conditions to be specified by bits 5-3 of the CSR: STOP, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, an external time base applied to ST1, and line frequency (50 or 60 Hz) picked up from bus line BEVNT. External periodic or aperiodic pulses may be applied to ST1 and counted, provided they meet the criteria in Paragraphs 3.2 and 3.3.6.

3.3.5 Buffer/Preset and Counter Registers

The Buffer/Preset Register is a word-oriented, 16-bit read/write register that can be loaded either under program control or from the counter. In Modes 2 and 3, the firing of ST2 causes the BPR to be loaded with the contents of the counter. The BPR cannot be loaded by the program in these modes as long as the GO bit is set.

The counter is a 16-bit internal register accessible only by way of the BPR; in Modes 2 and 3 it can be read indirectly through the BPR.

3.3.6 Schmitt Triggers

Both Schmitt triggers are equipped with switches to permit selecting slope direction (+ or -) and threshold reference level (TTL or -12V to +12V continuously variable). Each Schmitt trigger is also equipped with a screwdriver-operated Potentiometer to permit setting the variable threshold level. Switch-pack and Potentiometer terminals are all brought to multiple connector J1 to permit attachment of external user-provided slope and level controls. (See Figure 3-3.)

The two Schmitt triggers are used in somewhat different ways:

ST1 - Performs as an external time base input or external input for aperiodic signals to be counted. Outputs both to ST1 FAST ON connector to provide external start signals to ADV11-A and, through rate control circuitry, to permit selection as input to the counter. Maximum frequency varies as a function of input waveform.

ST2 - When the ST2 GO ENABLE bit is set, firing ST2 in any mode sets the GO bit and initiates counter action, causes the ST2 Flag to be asserted, and generates an interrupt if that function is enabled. When the GO bit is set in Modes 2 and 3, firing ST2 causes the Buffer/Preset Register to be loaded from the counter, the ST2 Flag to be set, and an interrupt to be generated if enabled.

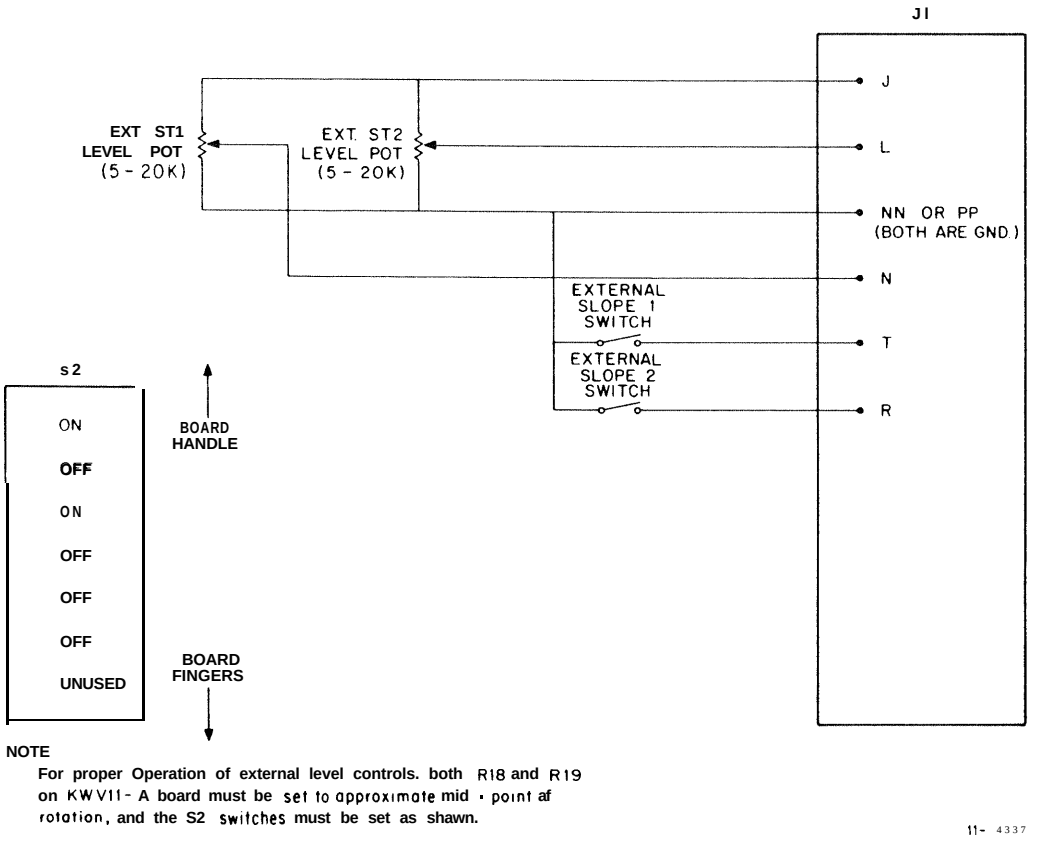


Figure 3-3 Connecting External User-Supplied Slope and Level Controls

3.4 CONNECTORS, SWITCHES, AND CONTROLS

Figure 3- 1 illustrates the location of user connectors, switches, and controls on the component side of the KWV1 I-A board.

3.4.1 40-Pin Connector

Figure 3-4 illustrates the 40-pin connector pin assignments for user inputs and Outputs. These pins may be connected to the optional H322 Distribution Panel* (see Paragraph 2.4.3.1) for convenient external user access. The proper Berg-to-Berg cable is the BC08R. The proper Berg to prepared open-ended cable is the BC04Z.

3.4.2 FAST ON Connectors (Clock Overflow and ST1 Outputs)

Two FAST ON connector tabs labeled CLK and ST1 are situated in the upper-right corner of the K WV I I-A board (see Figure 3-l). These tabs are electrically in parallel with pins RR (CLK OV L) and UU (ST 1 OUT L) on the 40-pin connector and are intended to facilitate connections by means of module jumpers (shown in Figure 2-9) to the clock Overflow and external start inputs on the ADV11-A (see Paragrapgh 2.4.3).

3.4.3 Selector Switches (Address, Vector, and Slope/Reference Level)

Figure 3-1 identifies three switch packs (S1, S2, and S3) that the KWV1 1-A provides to facilitate the selection of CSR address, vector address, and slope/reference level conditions for Schmitt Triggers 1 and 2.

*T he KWV 11 -A is shipped with decals which permit permanent identification of signal lines associated with H322 terminals.

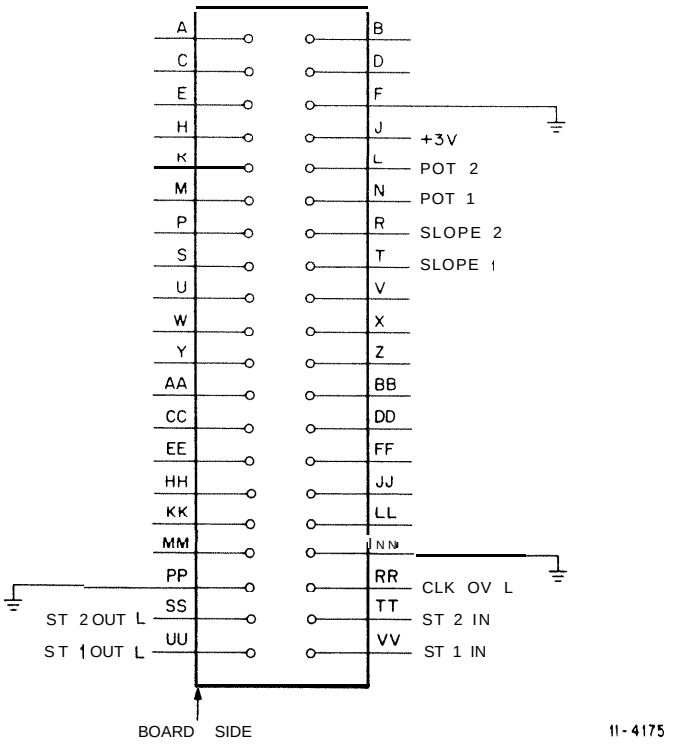


Figure 3-4 40-Pin Connector Pin Assignments

3.4.3.1 Address Selection - Switch Pack S1 contains 10 Single-pole/single-throw switches that communicate with data lines BDAL 1 l-2. The KWV11-A reads the BDAL lines only in response to BBS7 which the processor asserts only for an address of 160000 or higher. For this reason, and because the KWV 1 1-A transceivers are hard wired to respond only when BDAL bit 12 is set to 1, S1 permits assigning the CSR any address ending in 0 or 4 between 170000_8 and 1777748. The recommended address for the KWV1 1-A CSR is 170420, set as illustrated in Figure 3-5. The BPR automatically receives the next even address following that assigned to the CSR.

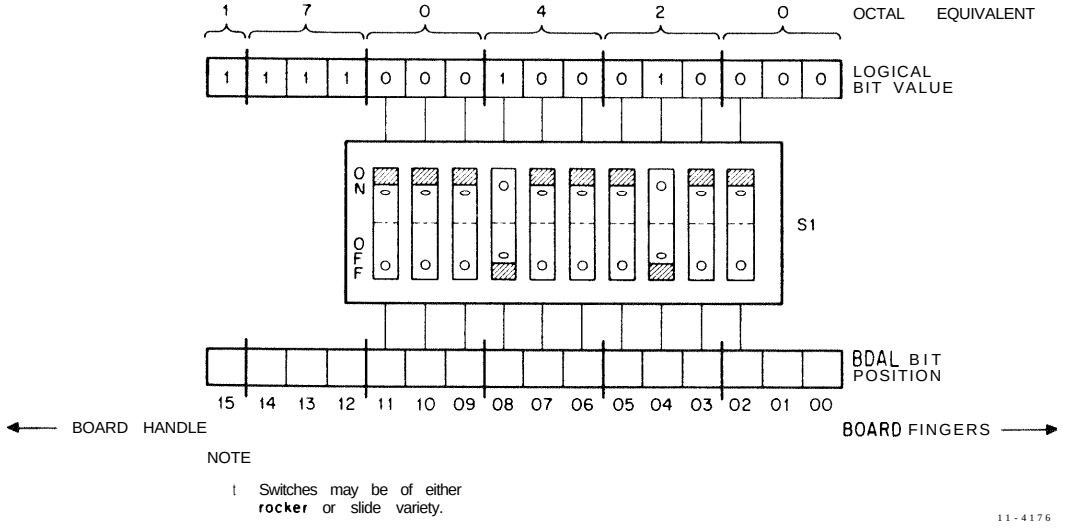


Figure 3-5 KWV11-A CSR Address Switches (Set for 170420)

3.4.3.2 Vector Selection - The clock overflow interrupt vector address is set by means of S3, a 7-switch pack of which oniy six switches are utilized. These switches communicate with BDAL lines 8-3 and can be set in increments of 10_8. The ST2 interrupt vector automatically receives an address that is four locations higher than the clock Overflow interrupt vector whose recommended address is 0000440 (see Figure 3-6).

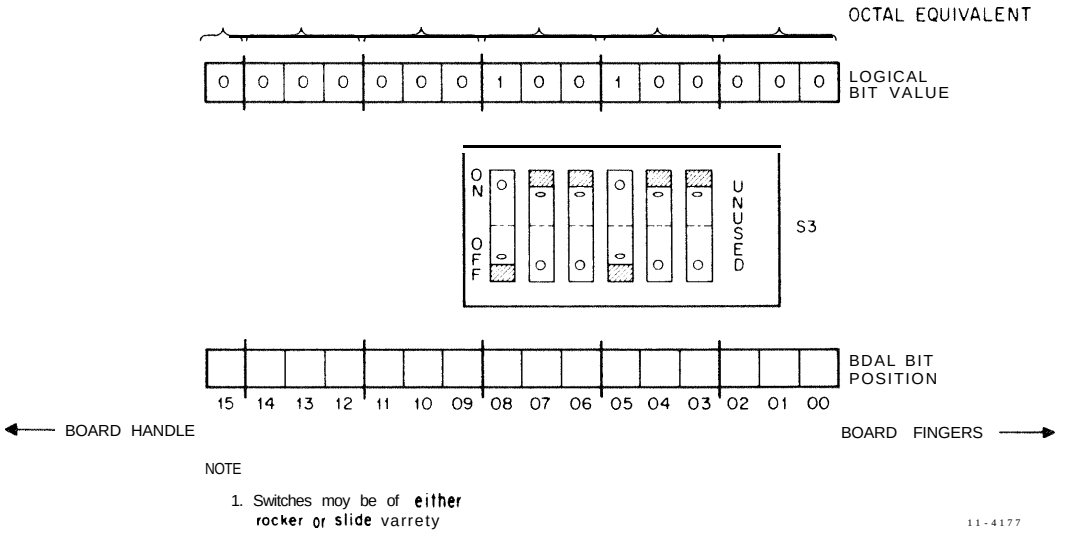


Figure 3-6 KWV 11-A Vector Address Switches (Set for 000440)

3.4.3.3 Slope and Reference Level Selector Switches and Controls (See Figure 3-7) - Slope and reference level selection for ST1 and ST2 are accomplished by means of S2, a 7-switch pack of which only switches 1-6 are used. Two reference modes are selectable for each Schmitt trigger - one that picks a fixed level appropriate to TTL logic, and one that picks a variable level that permits setting the ST threshold to any point between -12 and +12 V.

NOTE

User should take care that both TTL and variable switches for either Schmitt trigger are not on simultaneously. This condition will do no darnage to components, but produces unpredictable reference levels. Note also that if no signal is connected to a Schmitt trigger input, both threshold switches for that ST should be open for noise immunity. Alternatively, ST1 IN and ST2 IN can be grounded externally.

Slope selection is accomplished by separate switches for ST1 and ST2, respectively. When the related switch is on, the firing point effectively occurs on the positive slope of the input waveform. When the switch is off, the firing point occurs on the negative slope. (See Figure 3-8.)

3.5 PROGRAMMING

3.51 CSR Bit Assignments

CSR bit assignments are identified in Figure 3-9 and defined in Table 3-1.

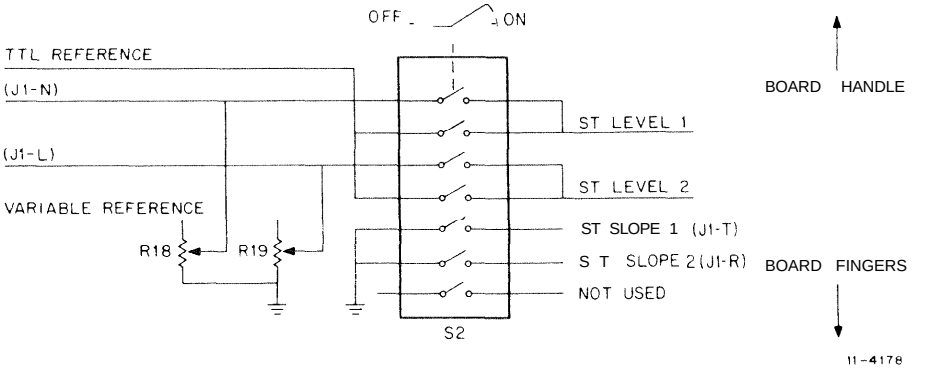


Figure 3-7 KWV11-A Slope/Reference Level Selector Switches and Controls

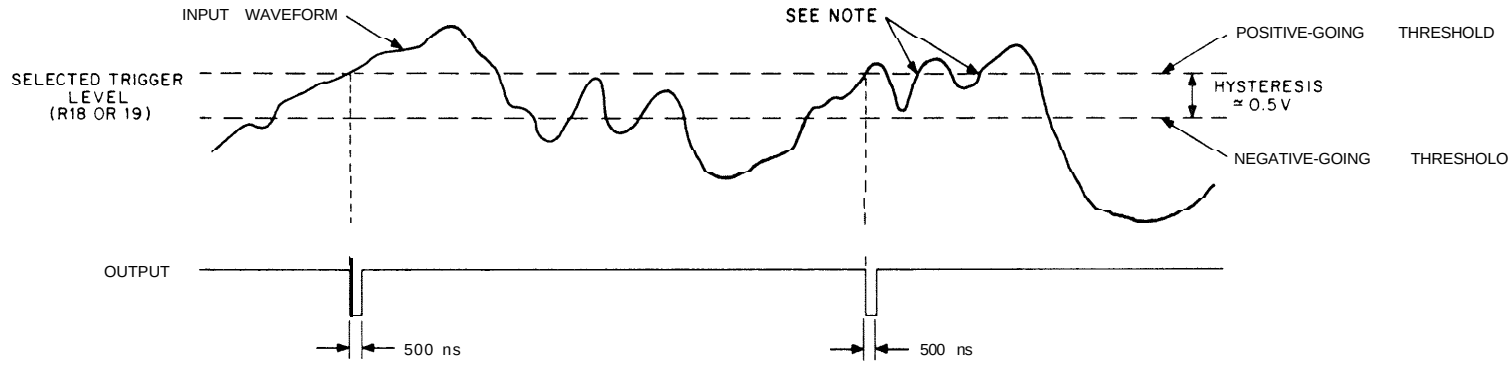
3.5.2 Buffer/Preset Register (BPR)

The BPR is a 16-bit, word-oriented, read/write register. Any attempt to write a byte into this register will result in a whole word being written. In Modes 0 and 1 the program may load it with the 2's complement of the number of counts desired before overflow. In Modes 2 and 3 it permits indirect reading of the clock counter.

3.5.3 Normal Control Sequences

3.5.3.1 Mode G (Single Interval) - Control code for Operation in Mode 0 must support the following sequence:

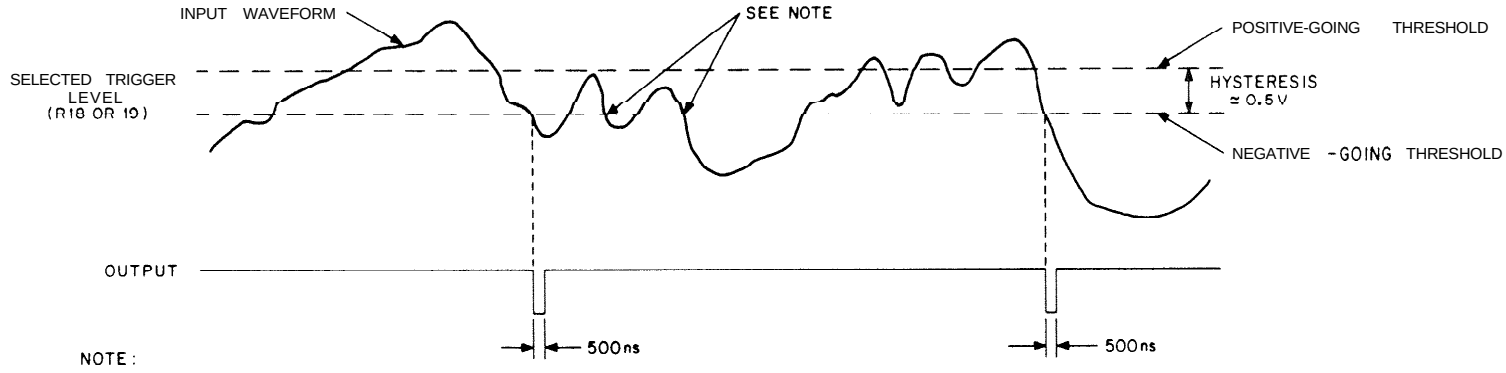
1. Control program writes desired count (2's complement) into BPR (see Paragraph 3.3.5).
2. Program writes control code into Control/Status Register as indicated in Table 3-2.
3. If GO bit is set high, KWV11-A responds by loading the 16-bit counter (see Paragraph 3.3.5) from the BPR and enabling the counter; if GO bit is set low and ST2 GO ENABLE bit is set high, KWV11-A waits for ST2 event, then sets the GO bit and loads and enables the counter.
4. Counter increments until Overflow, then halts (GO bit is cleared)
5. KWV 11-A raises Overflow Flag and issues interrupt if the CSR INT OV bit is set; if interrupt is not enabled, KWVI 1-A waits for program intervention.
6. Program responds to interrupt or intervenes in consequence of other criteria (e.g., testing the Overflow Flag or the A/D Done Flag if overflow was used to start an A/D conversion). Program reads the CSR, clears the Overflow Flag, and if no counting or mode changes are required, sets the GO bit or the ST2 GO ENABLE bit to reenter the sequence at step 3.



NOTE.

ST is retriggered **only** after Input woveform has moved beyond **opposite** threshold and then **again** passed selected threshold

(a) SLOPE SELECTION : SLOPE **switch** ON (Positive **Slope**)



NOTE :

ST **is retriggered** only **after input** waveform has maved beyond opposite threshald and then again passed selected threshold.

(b) SLOPE SELECTION: SLOPE **switch** OFF (Negative **Slope**)

11-4549

Figure 3-8 **KWV11-A** Slope **Selection**

Table 3-1 KWV11-A CSR Bit Definitions

Bit	Set By/Cleared By	Remarks
15 ST2 Flag Read/Write to 0	Set by the firing of Schmitt Trigger 2 or the setting of the MAINT ST2 bit in any mode while the GO bit or the ST2 GO ENABLE bit is set. Cleared under program control. Also cleared at the "1"-going transition of the GO bit unless the ST2 GO ENABLE bit has previously been set.	Must be cleared after servicing an ST2 interrupt to enable further interrupts. When cleared, any pending ST2 interrupt request will be cancelled. If enabled interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority.
14 INT 2 (INTERR UPT ON ST2) Read/W rite	Set and cleared under program control.	When set, the assertion of ST2 Flag will cause an interrupt. If set while ST2 Flag is set, an interrupt is initiated. When cleared, any pending ST2 interrupt request will be cancelled.
13 ST2 GO ENABLE Read/W rite	Set and cleared under program control. Also cleared at the "1"-going transition of the GO bit.	When set, the assertion of ST2 Flag will set the GO bit and clear the ST2 GO ENABLE bit.
12 FOR (FLAG OVERRUN) Read/W rite	Set when an Overflow occurs and the Overflow Flag is still set from a previous occurrence, or when ST2 fires and the ST2 Flag is already set. Cleared under program control and at the "1"-going transition of the GO bit.	This bit provides the programmer with an indication that the hardware is being asked to operate at a speed higher than is compatible with the Software.
11 DIO (DISABLE INTERNAL OSCILLATOR) Read/W rite	Set and cleared under program control.	For maintenance purposes, this bit inhibits the internal crystal oscillator from incrementing the clock counter. Used in conjunction with bit 10 below.
10 MAINT OSC Write Only	Set under program control. Clearing is not required. Always read as a "0."	For maintenance purposes, setting this bit high simulates one cycle of the internal 10 MHz crystal oscillator used to increment the clock counter.
9 MAINT ST2 Write Only	Set under program control. Clearing is not required. Always read as a "0."	Setting this bit simulates the firing of Schmitt Trigger 2. All functions initiated by ST2 can be exercised under program control by using this bit.

Table 3-1 KWV11-A CSR Bit Definitions (Cont)

Bit	Set By/Cleared By	Remarks
8 MAINT ST1 Write Only	Set under program control. Clearing is not required. Always read as a "0."	Setting this bit simulates the firing of ST1. All functions initiated by ST1 can be exercised under program control by using this bit.
7 OVFLO FLAG Read/Write to 0	Set each time the counter overflows. Cleared under program control and at the "1"-going transition of the GO bit.	If bit 6 is set, bit 7 set will initiate an interrupt. Bit 7 must be cleared after the interrupt has been serviced to enable further Overflow interrupts. If cleared while an Overflow interrupt request to the processor is pending, the request is cancelled. If enabled interrupts are requested at the same time by bits 07 and 15, bit 07 has the higher priority.
6 INTOV (INTERRUPT ON OVERFLOW) Read/Write	Set and cleared under program control.	When this bit is set, the assertion of OVFLO Flag will generate an interrupt. Interrupt is also generated if bit 6 is set while OVFLO Flag is set. If cleared while an Overflow interrupt request to the processor is pending the request is cancelled.
5:3 RATE Read/Write	Set and cleared under program control.	These bits select clock counting rate or Source. **5 4 3 Rate** 0 0 0 STOP 0 0 1 1MHz 0 1 0 100 kHz 0 1 1 10 kHz 1 0 0 1 kHz 1 0 1 100 Hz 1 1 0 ST1 1 1 1 Line (50/60 Hz)
2:1 MODE Read/Write	Set and cleared under program control.	2 **1** Mode 0: 0 0 Mode 1: 0 1 Mode 2: 1 0 Mode 3: 1 1
0 GO Read/Write	Set and cleared under program control. Also cleared when the counter Overflows in Mode 0.	Setting this bit initiates counter action as determined by the rate and mode bits. In Modes 1, 2, and 3 it remains set until cleared. In Mode 0 it clears itself when counter Overflow occurs. Clearing bit 0 zeroes and inhibits the counter.

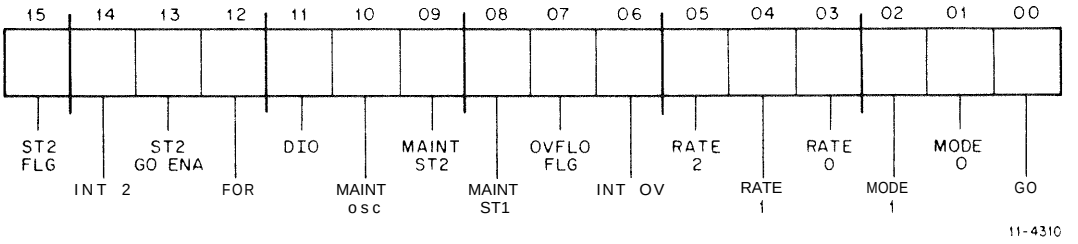


Figure 3-9 CSR Bit Assignments

3.5.3.2 Mode 1 (Repeated Interval) - Control code for Operation in Mode 1 must support the following sequence:

1. Control program writes desired count (2's complement) into the BPR.
2. Program writes control code into CSR as indicated in Table 3-3.
3. If GO bit is set high, KWV1 1-A responds by loading the 16-bit counter from the BPR and enabling the counter; if GO bit is set low and ST2 GO ENABLE bit is set high, KWV1 1-A waits for ST2 event, then sets the GO bit and loads and enables the counter.
4. Counter increments until Overflow.
5. KWV 11 -A reloads counter from the BPR, reenables the counter, raises the Overflow Flag in the CSR, and issues interrupt to the processor if interrupt is enabled.
6. If second Overflow occurs before first is serviced (i.e., if Overflow Flag is still high when next Overflow occurs), KWV11-A Flag Overrun (FOR) bit in the CSR is set high to alert program that data has been lost.
7. Program responds to interrupt or intervenes in consequence of other criteria. Program reads CSR, clears the Overflow Flag, and if no counting or mode changes are required, sets the GO bit or the ST2 GO ENABLE bit to reenter the sequence at step 3.

3.5.3.3 Mode 2 (External Event Timing) Control code for Operation in Mode 2 must support the following sequence:

1. Program writes control code into CSR as indicated in Table 3-4.
2. KWV 1 1-A responds by incrementing the counter (zeroed when the GO bit was cleared) at the selected rate until the GO bit is set to 0.
3. ST2 pulse loads current counter contents into BPR, sets the ST2 Flag, and generates interrupt if INT 2 is enabled.
4. Overflow sets OVFLO FLG high and, if INT OV bit is high, generates interrupt.
5. Counter continues to increment until processor sets GO bit to 0.

Normally, program enables INT 2 and/or INT OV bits, permitting the processor to synchronize its operations with the external ST2 events and prevent loss of data by reinitializing the process after step 4.

Table 3-2 CSR Bit Settings for Mode 0, Single Interval

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	Will be set to 1 by counter Overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter Overflow.
5	RATE 2	x	
4	RATE 1	x	See Table 3- 1.
3	RATE 0	x	
2	MODE 1	0	Set by program to 0.
1	MODE 0	0	Set by program to 0.
0	GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter Overflows.

x = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

Table 3-3 CSR Bit Settings for Mode 1, Repeated Interval

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	Will be set to 1 by counter Overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter Overflow.
5	RATE 2	x	
4	RATE 1	x	See Table 3-l.
3	RATE 0	x	
2	MODE 1	0	Set by program to 1_8.
1	MODE 0	1	
0	GO	x	Same as for Mode 0, except that bit is not cleared when counter Overflows.

x = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

Table 3-4 CSR Bit Settings for Mode 2, External Event Timing

Bit No.	CSR Name	Bit Condition as Written by Processor	Remarks
15	ST2 FLG	0	Will be set to 1 on ST2 event. Cleared by leading edge of GO bit assertion except when ST2 GO ENA has previously been set.
14	INT 2	x	Set to 1 by program if interrupt on ST2 event is desired.
13	ST2 GO ENA	x	Set to 1 by program if GO is to be set by external signal to ST2. Cleared by leading edge of GO bit assertion.
12	FOR	(0)	
11	DIO	0	
10	MAINT OSC	0	
9	MAINT ST2	0	
8	MAINT ST1	0	
7	OVFLO FLG	(0)	Will be set to 1 by counter Overflow. Always cleared by leading edge of GO bit assertion.
6	INT OV	x	Set to 1 by program for interrupt on counter Overflow.
5	RATE 2	x	
4	RATE 1	x	See Table 3-l.
3	RATE 0	x	
2	MODE 1	1	Set by program to 2_8.
1	MODE 0	0	
0	GO	x	Set by program to 1 unless ST2 GO ENA is set; remains 1 until written to 0 by program. Cleared when counter Overflows.

x = 0 or 1, depending on user requirements.
(0) = Automatically cleared by GO bit assertion.

3.5.3.4 Mode 3 (External Event Timing from Zero Base) - Operation is identical to that in Mode 2 except that counter is zeroed after ST2 pulse. Counter continues to increment until GO bit is set to 0.

Note that the interval between two ST2 events may be measured directly in Mode 2 or 3 with processor assistance if the CSR ST2 GO ENABLE and Interrupt 2 bits are set before the first event and the GO bit is left clear. Under these conditions, the first ST2 event will set the GO bit (and thus start the counting process) and simultaneously issue an interrupt. If the interrupt service routine now clears the ST2 Flag bit, the next ST2 event will cause the BPR to be loaded from the counter in the normal Mode 2 fashion. The choice of Mode 2 or Mode 3 for such measurements will depend on whether or not an ongoing accumulation of time after the second event is required by the application. If such an accumulation is necessary, Mode 2 is appropriate since the counter is not zeroed after ST2 events.

3.5.4 Programming Example

Record point in double-precision timeframe for each ST2 event following GO. Program makes use of a 32-bit counter, the low order bits of which are taken directly from the KWV11-A (KWBPR) and the high order bits of which are taken from a Software counter (HICNT) that is incremented with each KWBPR Overflow.

```
                MTPS    #0                  ;CLEAR PSW
                MOV     #ST2SRV, @ST2VEC    ;LOAD ST2 VECTOP
                                            ;ADDR
                MOV     #200,@ST2PSW        ;SET UP PSW FOR ST2
                                            ;INTERRUPT (DISABLE
                                            ;ALL SUBSEQUENT
                                            ;INTERRUPTS)
                MOV     #OVSRV, @OVVEC      ;LOAD O V VECTOR
                                            ;ADDR
                MOV     #200,@OVPSW         ;SET UP PSW FOR OV
                                            ;INTERRUPT (DISABLE
                                            ;ALL SUBSEQUENT
                                            ;INTERRUPTS)
                 .
                 .
                MOV     #BUFFER,P O         ;SET UP POINTER TO
                                            ;BEGINNING OF
                                            ;BUFFER AREA
CLKGO:          MOV     #40115,@KWCSR       ;DEPOSIT 1MHZ, MODE 2 ,
                                            ;INTOVEN, INT ST2 EN,
                                            ;AND GO INTO KWCSH
COUNT:          WAIT                        ;FOR INTERRUPT
                                            ;BY OVFLO OR ST2
                BIT     #10000,@KWCSR       ;IS FOR BIT SET?
                BEQ     COUNT               ;NO, CONTINUE
                JMP     FORSRV              JYES, SERVICE FLAG
                                            ;OVERRUN CONDITION
OVSRV:          BIT     #100000,@KWCSR      ;IS ST2 FLAG SET?
                BEQ     2$                  ;NO, CONTINUE
                TST     @KWBPR              ;DID ST2 OCCUR BEFORE UV?
                BPL     2$                  ;NO, BRANCH
                MOV     HICNT,(R0)+         ;YES, SERVICE ST2 FIRST
                MOV     @KWBPR,(P0)+
                BIC     #100000,@KWCSR      ; ACKNOWLEDGE ST2
                                            ;OCCURRENCE
```

(example continued on next page)

```
2$:         INC     HICNT           ;INCREASE MSB BY
                                    ;1 COUNT
            BEQ     ENDSRV          ;BRANCH IF INCREASE
                                    ;CAUSES OVERFLOW
            BIC     #200,@KWCSR     ;ACKNOWLEDGE OV
                                    ;CLEAR OV BIT
            RTI                     ;AND RETURN TO MAIN
                                    ;PROGRAM
ST2SRV:     MOV     HICNT,(R0)+     ;GET MSB FROM SOFT COUNT
            MOV     @KWBPR,(R0)+    ;GET LSB FROM HARD COUNT
            BIC     #100000,@KWCSR  ;ACKNOWLEDGE ST2
            RTI                     ;AND RETURN TO MAIN
                                    ;PROGRAM
FORSRV:     .                       ;EVENTS OCCURRING
                                    ;TOO FAST FOR CURRENT
                                    ;SERVICE
            .
            .
ENDSRV:     .                       ;32 BIT OVERFLOW
                                    ;OCCURRED
            .
            .
            .
KWCSR:      170420
KWBPR:      170422
OVFVEC:     440
ST2VEC:     444
HICNT:      0
BUFFER:     .BLKW   XXXX            ;XXXX=LENGTH OF RESULT
                                    ;BUFFER
```

CHAPTER 4

AAV11-A DIGITAL-TO-ANALOG CONVERTER

4.1 GENERAL DESCRIPTION

The AAV 11-A is a 4-channel digital-to-analog converter module for use on the bus of the LSI- 11 processor. The unit is made up of control and interfacing circuitry, four D/A converters, a dc-dc converter to provide power to the analog circuits, and a voltage reference. Each channel provides 12 bits of resolution. Each has its own holding register which can be separately addressed and can be written and read in either word or byte format. In addition, bits O-3 of the fourth holding register are brought to the I/O connector for use as a 4-bit digital output register.

Jumpers permit manual selection of voltage range and operating mode (bipolar or unipolar).

4.2 SPECIFICATIONS (@ 25° C unless otherwise specified)

Number of D/A Converters	4
Digital Input	12 bits (binary encoded for unipolar mode, offset binary encoded for bipolar mode)
Digital Storage	Read-write, word or byte operable, single buffered
Analog Output Voltage Range (jumper selected)	±2.56 V, ±5.12 V, ± 10.24 V bipolar; 0 V to +5.12 V, 0 V to + 10.24 V unipolar
Digital Output Characteristics (DAC 3 Holding Register Bits 3:0)	Source: 5.2 mA @ 2.4 V Sink: 16 mA @ 0.4 V
Resolution	1 part in 4096
Warm-Up Time	5 minutes minimum
Gain Accuracy	Adjustable (factory-set for bipolar ±5.12 V; selection of other ranges may require recalibration)
Gain Temperature Coefficient	10 ppm per degree C, maximum
Offset Temperature Coefficient	20 ppm of full scale range per degree C, maximum
Linearity	± 1/2 LSB maximum non-linearity
Differential Linearity	± 1/2 LSB, monotonic
Output Impedance	1 Ω maximum at DAC output; 4 Ω maximum at end of BC08R 8 ft cable

Drive Capability	± 5 mA maximum per converter
Slewing Speed	5 V/μs
Rise and Settling Time (to 0.1% of final value)	4 μs; 8 μs with 5000 pF load in parallel with lk Ω
Power Consumption (from LSI-11 bus power supply)	5 V ±5% @ 1.5 A, 12 V @ 0.4 A
Environmental	Ref: DEC STD 102, class C
Packaging	One quad module
Bus Loading	1 bus load

4.3 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the AAV11-A in block diagram form.

4.3.1 Bus Control

The logic associated with the bus control section maintains proper communications protocol between the processor LST-11 bus and the AAV11-A. This logic generates and monitors the bus signals involved during data transfers between the processor and the AAV11-A, permitting the AAV11-A to recognize when it is being addressed by the processor (address defined by setting on the Address Switch Pack), to accept input data from the processor, and to output data to the processor.

4.3.2 Control Logic

The AAV11-A has no Control/Status Register. The four digital-to-analog converters continually generate voltages at their Outputs that reflect whatever digital values have most recently been written into their respective holding registers. The role of the control logic is to make the necessary discriminations between requests to change the state of the holding registers (i.e., to *write* into the holding registers), and requests to put the holding register contents onto the BD lines where they can be picked up through the transceivers by the processor.

4.3.3 DACs 0, 1, and 2

Digital-to-analog conversion functions are performed in each of the four AAV11-A channels by identical circuits:

- A holding register which stores the digital value output by the processor
- A digital-to-analog converter (DAC) proper which generates a current that is a function of the holding register value and of the mode/level jumper conditions
- An amplifier that translates the current into a proportional voltage, provides a low output impedance for the channel, and permits adjustment of signal offset.

4.3.4 DAC 3

DAC 3 is identical to DACs 0, 1, and 2 except that Holding Register bits O-3 are routed to the I/O connector as well as to the DAC. This arrangement permits these bits to be routed to external equipment that requires binary control signals at programmable intervals. Control data in these bit positions affects any 12-bit D/A conversion that they coincide with, but since they involve the least significant bits of the word, the worst-case error is less than 0.5%. Consequently, DAC 3 can be used as a 12-bit DAC or as an 8-bit DAC plus four output bits for CRT Intensify, Store, Non-Store, Erase, etc.

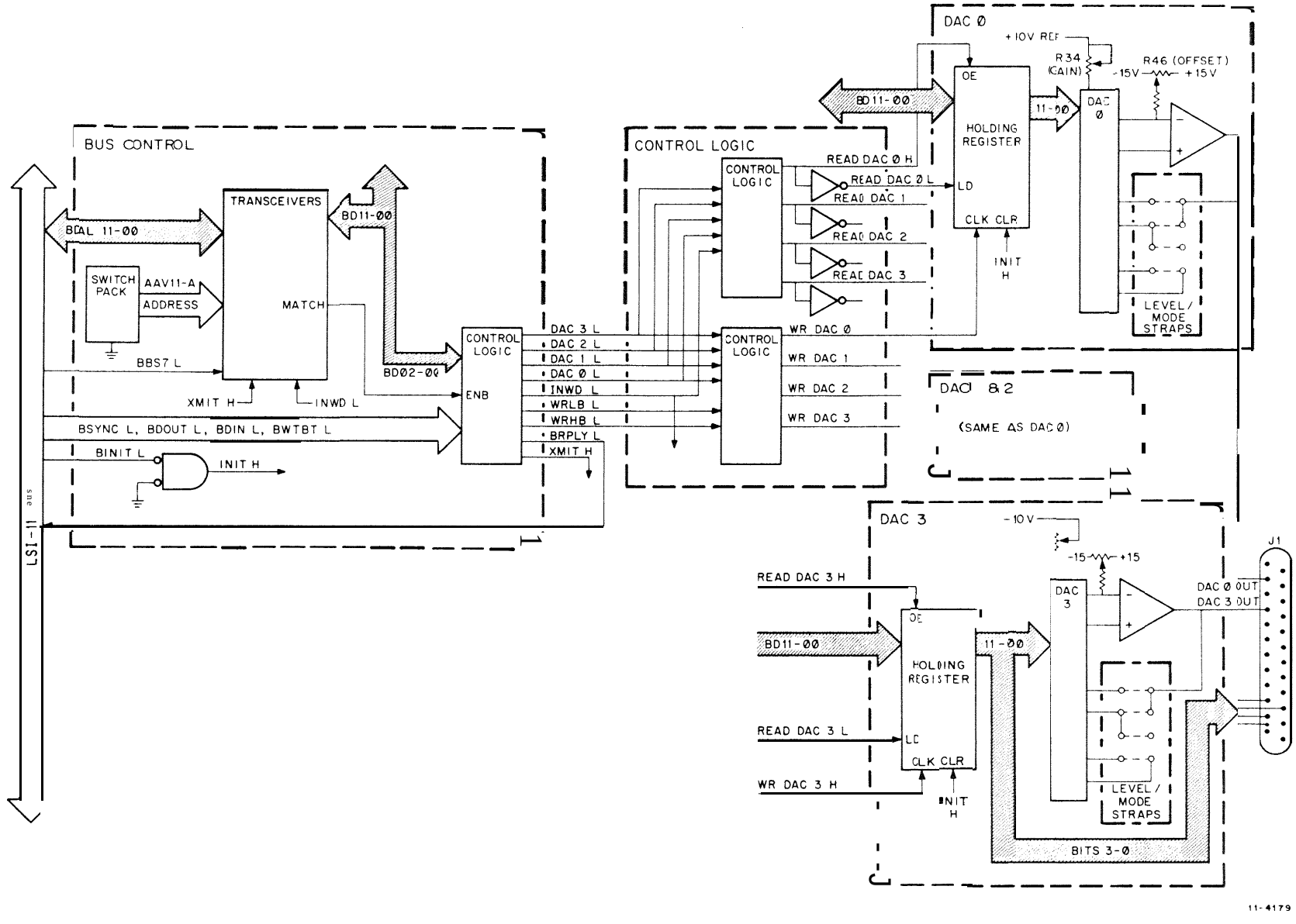


Figure 4-1 AAV11-A Block Diagram

4.4 CONNECTORS, SWITCHES, AND CONTROLS

Figure 4-2 illustrates the location of user connectors, switches, and controls located on the component side of the AAV l l-A board.

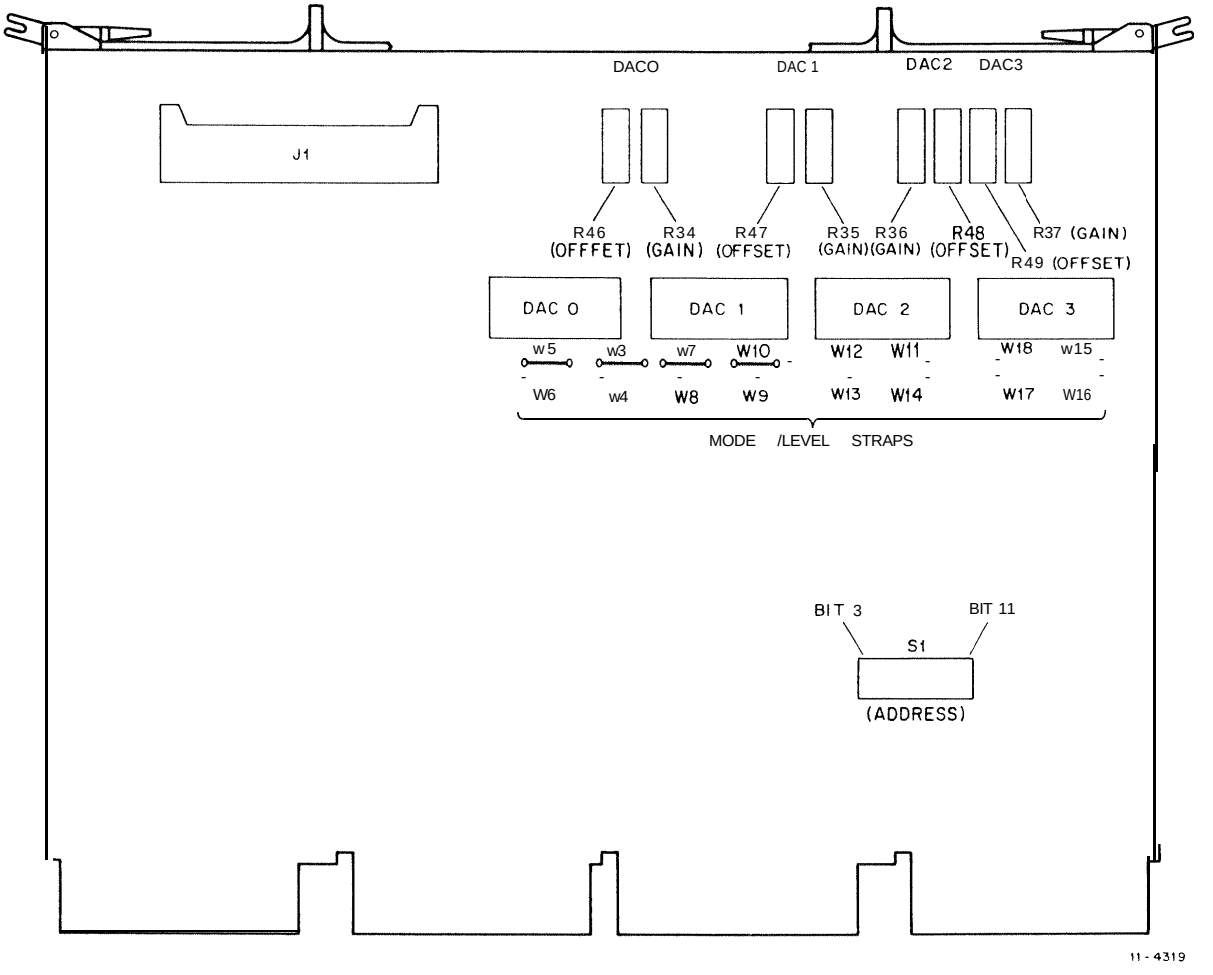


Figure 4-2 AAV1 1-A Connectors, Switches, and Controls

4.4.1 40-Pin Connector

Figure 4-3 illustrates the 40-pin connector pin assignments for user Outputs. These pins may be connected to the optional H322 Distribution Panel* (see Paragraph 2.4.3.1) for convenient external user access. The proper cable for this purpose is the BC08R. Also available is a Berg to prepared open-ended cable, the BC04Z.

Either a VR14 or VR17 CRT may be interfaced to the H322 via a user-created cable terminating in a 24-pin Amphenol, or equivalent, male plug (DEC #12-03466-00). A user-created cable may be connected to other types of CRT systems using a 25-pin connector such as a male DB25P type plug (DK # 12-05886-00).

* The AAVI 1-A is shipped with decals which permit permanent identification of signal lines associated with H322 terminals.

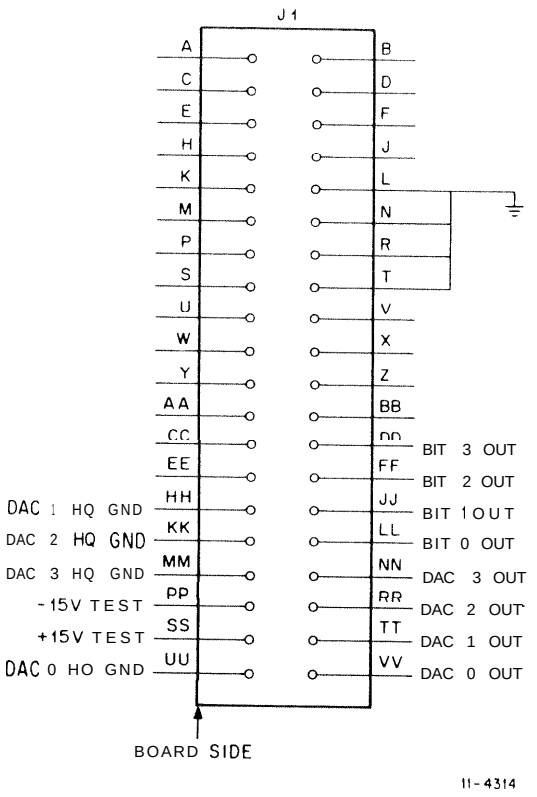


Figure 4-3 40-Pin Connector Pin Assignments

The BC04Z signal lines may be connected to user-selected pins on a male or female connector. A female 25 pin connector of the DB25S type (DEC #12-09326-00) may be used for general purposes. A male 25-pin connector of the DB25P type (DEC #12-05886-00) will interface several popular CRT systems to the AAV11. Either a VR14 or VR17 CRT may be interfaced by means of a 24-pin Amphenol, or equivalent, male plug (DEC #12-03466-00) to the BC04Z. Both the AAV11 and selected CRT must be set up and adjusted for electrical compatibility. The CRT manual should define appropriate connector pins for each AAV11 signal line. Appropriate Software will be necessary to control a CRT.

4.4.2 Address Switches

Figure 4-2 identifies the location of S 1, a switch pack containing 10 Single-pole Single-throw switches (1 unused) which, when set, transmit 0 logic levels to the compare inputs of the transceivers. Whenever the AAV11-A sees BBS7 transmit a logical 1 (indicating that the processor has placed an I/O device address on the bus), the transceivers compare the pattern created by the switches with that appearing on Bus Data/Address (BDAL) lines 3-l 1. If the patterns match, the processor is addressing the AAV 11-A, and the latter prepares to load the DAC holding register identified by decoding bits 1 and 2 of the address word as defined in Figure 4-4.

Since the AAV11-A makes the comparison only in response to BBS7 (which the processor sets to 1 only in response to an address of 160000 or higher) when address line BD 12 = 1, S1 permits assigning the four DACs any contiguous set of four even word addresses between 170000 and 177770. The recommended setting for S1 on the first AAV11-A is 170440, illustrated in Figure 4-5. Since LSI-11 bus address assignments for the AAV11-A extend from 170440 to 170476, up to four AAV11-As can be accommodated on the same processor.

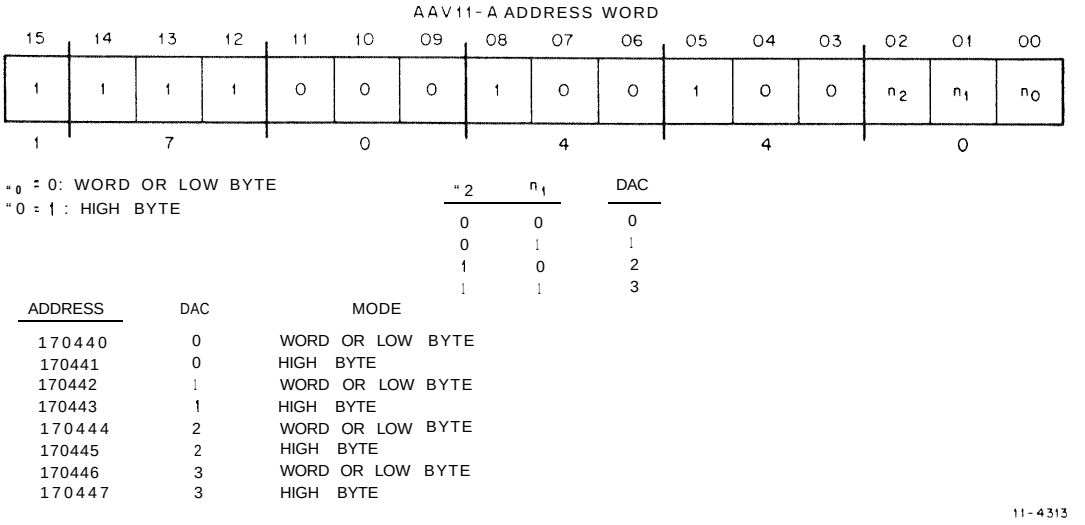


Figure 4-4 AAV 11-A Address Decoding

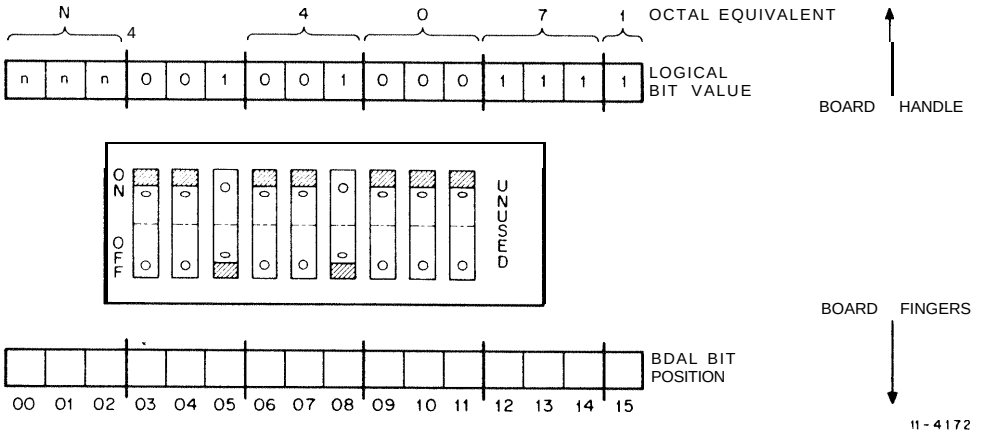


Figure 4-5 AAV1 1-A Address Switches (set for 17044n)

4.4.3 Mode/Level Selector Jumpers

As shipped from the factory, the AAV11-A is set for bipolar Operation between -5.12 and +5.12 V. Unipolar Operation and Operation with other voltage ranges can be achieved by proper changes in the mode/level jumpers (illustrated in Figure 4-2). See AAV11-A Installation and Service chapter for details.

4.5 INTERFACING TO OUTPUT DEVICES

4.5.1 Ground Connections

Analog output devices such as oscilloscopes may be either grounded or floating. If the oscilloscope is grounded, either through its power plug or through contact between its Chassis and a grounded cabinet, the oscilloscope ground should not be connected to any of the AAV11-A ground pins. Doing so may result in a ground loop which will adversely affect scope control results as well as any ADV11-A operations. If the oscilloscope is floating, its ground should be connected to the AAV11-A logic ground, pins L, N, R, or T of the Berg connector. Note that the foregoing assumes that the Computer power supply ground is connected to power line (earth) ground. If continuity checks reveal no such connection, attach a length of 12-gauge wire between the power supply ground and a convenient point associated with earth ground.

Oscilloscope X and Y inputs may be either differential or Single-ended. Differential inputs should be driven as in Figure 4-6.

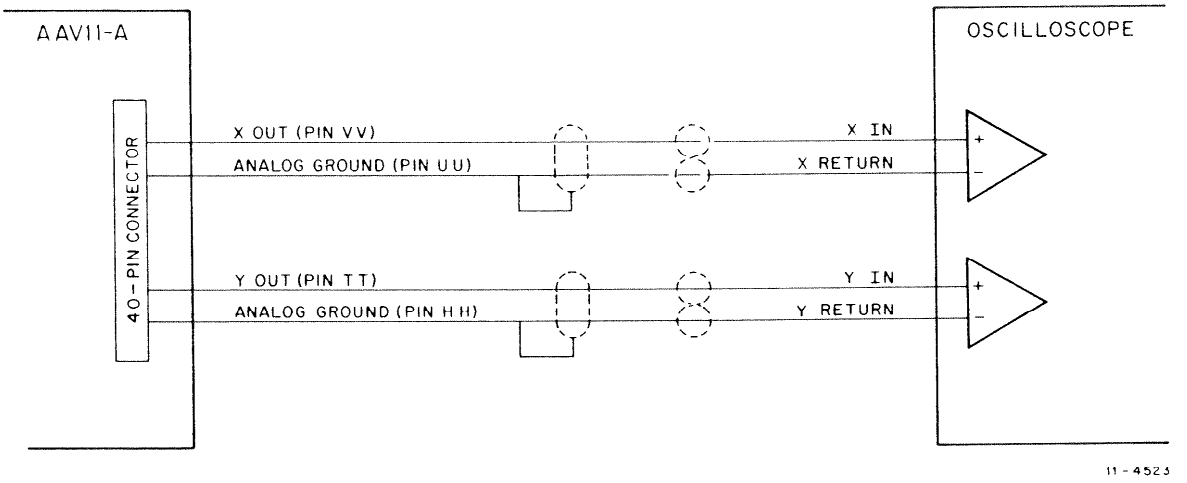


Figure 4-6 Connection to Oscilloscope with Differential Input

When oscilloscopes with Single-ended inputs are involved, the AAV11-A analog grounds (pins UU and HH) are not used. Return path for X and Y signal currents is through ground for a grounded oscilloscope or through logic ground (pins L, N, R, or T) for a floating oscilloscope. Since the grounded, Single-ended oscilloscope sees an input voltage which is the sum of the AAV11-A output and the ground difference voltage between the oscilloscope and the AAV1 l-A, noise and line frequency errors may be minimized by plugging the scope into an ac socket as close as possible to the computer. Running Single-ended scopes in a floating configuration will eliminate noise and line frequency errors which are due to ground voltage differences.

4.5.2 Twisting

The effect of magnetic coupling into the scope input lines can be minimized for a differential-input scope by running the AAV 11 -A output and its return line in a twisted pair. No benefit is derived from a twisted pair with a Single-ended scope input.

4.5.3 Shielding

The effect of electrostatic coupling into the scope input lines can be minimized by shielding the input lines from AAV1 1-A to the scope. The shield should be connected to ground at one end only. Grounding the shield at both ends may result in a ground loop which will adversely affect scope control results and any ADV11-A A/D operations.

4.5.4 Drive Capability

Careful selection of cabling is essential. The D/A Outputs are capable of driving a maximum of 5000 pF. Output impedance is 1 ohm. Output current limit is 5 mA.

4.6 PROCRAMMING

All four DAC holding registers are automatically set to zero on system initialization. This produces -5.12 V at the DAC Outputs when the mode/level jumpers are connected as delivered from the factory. Any holding register value remains in effect until changed by the processor in response to a program instruction. Coding to the D/A converters is offset binary for bipolar Operation and straight binary for unipolar Operation. Offset binary defines 0 as maximum negative voltage, mid-point (i.e., 4000_8 for the 12-bit AAV 1 1-A) as 0 V, and all ls (7777_8) as maximum positive voltage. These relationships are illustrated in Table 4- 1.

Table 4-l AAV11-A Digital-to-Analog Conversions*

1 nput Code (octal)	Bipolar ±2.56 V (volts)	Bipolar ±5.12 v (volts)	Bipolar ± 10.24 V (volts)	Unipolar 0 v to +5.12 v (volts)	Unipolar 0 V to +10.24 V (volts)
0000	-2.56	-5.12	-10.24	+0.0	+o.o
0001	-2.55875	-5.1175	-10.235	+0.00125	+0.025
3777	-0.00125	-0.0025	-0.005	+2.55875	+5.1175
4000	0.0	**0.0**	**0.0**	+2.56	+5.12
4001	+0.00125	+0.0025	+0.005	+2.56125	+5.1225
7777†	+2.55875	+5.1175	+10.235	+5.11875	+10.2375

* Offset binary for bipolar, straight binary for unipolar operating modes. Conversions may be made between 2's complement signed binary and offset binary numbers by subtracting 4000_8 from the 2's complement number (or adding 4000_8 to the offset binary number) and using only the low order 12 bits of the result.

† Note that in all ranges, actual maximum positive voltage output is 1 LSB less than nominal maximum positive output.

CHAPTER 5

DRV11 PARALLEL LINE UNIT

5.1 GENERAL DESCRIPTION

The DRV11 is a general-purpose interface unit used for connecting parallel-line TTL or DTL devices to the LSI-11 bus over up to 25 feet of cable. It permits program-controlled data transfers at rates up to 44K words per second (with optimized programming) and provides LSI-11 bus interface and control logic for interrupt processing and vector generation. Data is handled by 16 diode-clamped input lines and 16 latched output lines. Device address is user-assigned and Control/Status Registers (CSR) and Data Registers are compatible with 'PDP-11 Software routines.

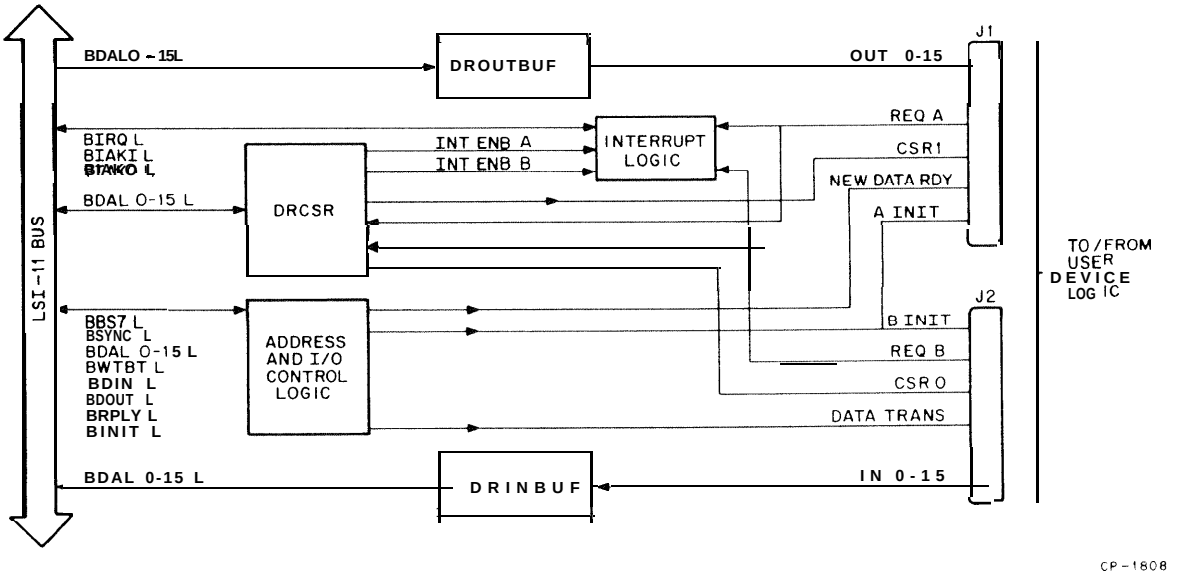


Figure 5-1 DRV11 Parallel Line Unit

5.2 JUMPER-SELECTED ADDRESSING AND VECTORS

5.2.1 Locations

Jumpers for device address and vector selection are provided on the DRV11 as shown in Figure 5-2. Jumpers are installed at the factory for address 167770 (DRCSR) and vectors 300 (interrupt A) and 304 (interrupt B). These can be cut or removed by the user to program the module for his system application, as described in the following Paragraphs.

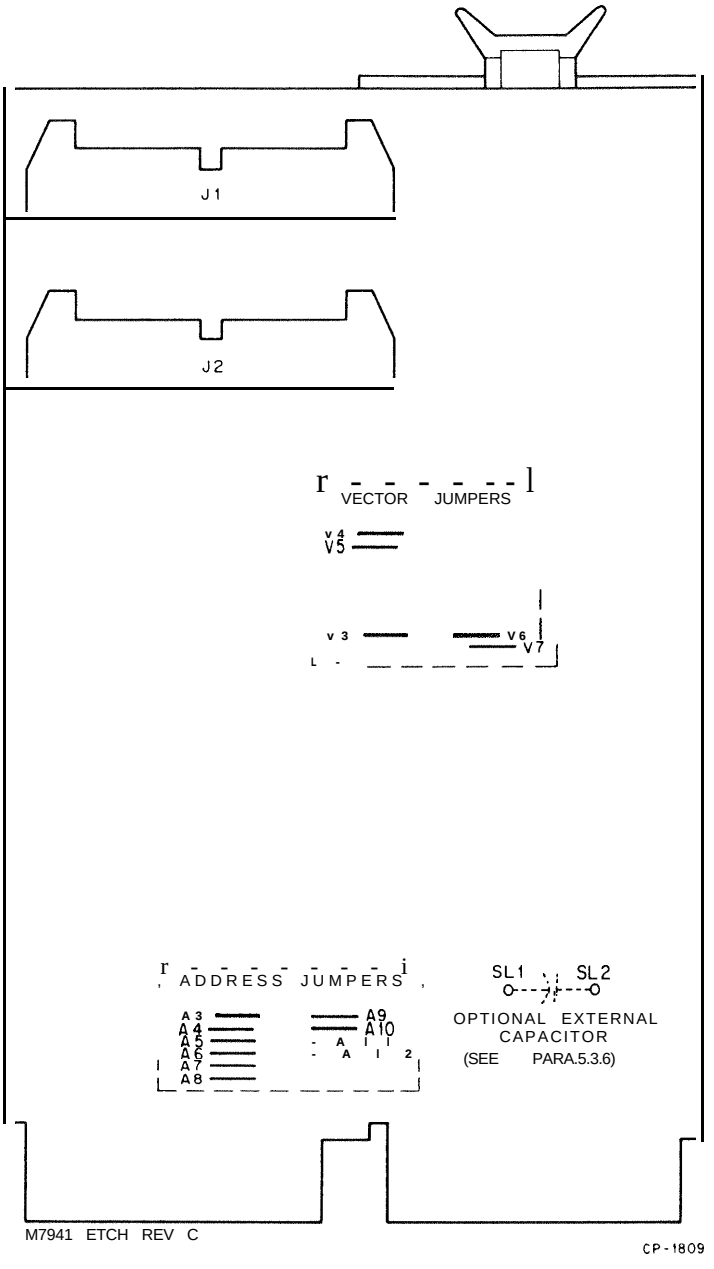


Figure 5-2 DRV11 Jumper Locations

5.2.2 Addressing

Jumpers involved with addressing include A3 through A12. Only address bits 03 through 12 are programmed by jumpers for DRV11 addressing, producing the M-bit address word shown in Figure 5-3. The appropriate jumpers are removed to produce logical 1 bits; jumpers are installed to produce logical 0 bits.

5.2.3 Vectors

Jumpers involved with vector addressing include V3 through V7. Only vector bits 03 through 07 are programmed by the jumpers for DRV11 vector addressing, producing the 16-bit word shown in Figure 5-4. The appropriate jumpers are removed to produce logical 1 bits; jumpers are installed to produce logical 0 bits.

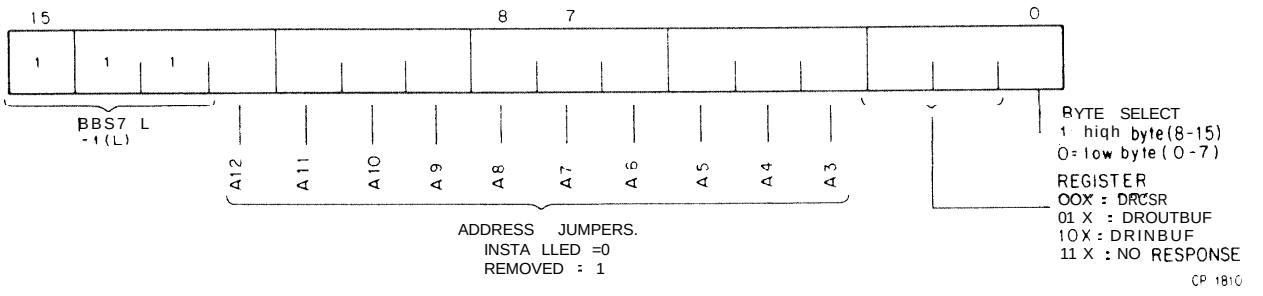


Figure 5-3 DRV11 Device Address

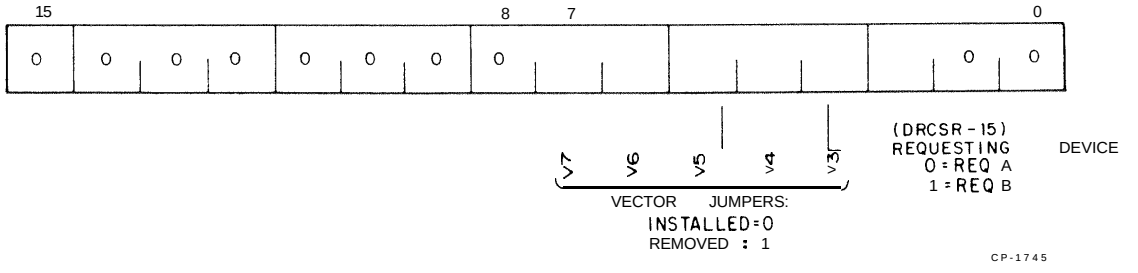


Figure 5-4 DRV11 Vector Address

5.3 INTERFACING TO THE USER'S DEVICE

5.3.1 General

Interfacing the DRV11 to the user's device is via the two board-mounted H854 40-pin male connectors. Pins are located as shown in Figure 5-5. Signal pin assignments for input interface J2 (connector no. 2) and output interface Jl (connector no. 1) are listed in Table 5-l. The proper Berg-to-Berg cable is a BC08R. The proper Berg to open-ended cable is a BC04Z. Connection to the DRV11 can be made through the H322 Distribution Panel (see Figure 2-8). This unit is provided with decals, which when applied according to instructions on the decal sheet, identify the H322 screw terminals with respect to the associated pins on the DRV11 Berg connectors (A, B, UU, VV, etc.). Space is provided on the decal for specific user identification. Note that DRV11/H322 terminal relationships assumed by the decal sheet rest on connection of the BC08R cable so that stamped labels on female cable ends match embossed labels on male connectors - A/B to A/B, UU/VV to UU/VV. This normally means that any "this side up" labels face away from the board on which the male connector is mounted.

Each BC04Z cable from a DRV11 may be terminated in a female 25-pin connector such as a DB25S type (DEC #12-09326-00) socket. The user may assign the signal and ground lines from the BC04Z to specific connector pins. User apparatus may be connected into the socket by means of a male 25-pin connector such as a DB25P type plug (DEC #12-05886-00).

5.3.2 Output Data Interface

The output interface is the 16-bit buffer DROUTBUF. It can be either loaded or read under program control. When DROUTBUF is loaded by the CPU, the NEW DATA READY H 300 ns pulse is generated to inform the user's device of the data transfer. In order to allow data to settle on the interface cable, the trailing edge of this positive-going pulse should be used to strobe the data into the user's device. The system initialize signal (BINIT L) clears DROUTBUF. When an output line is set to logical 1, the TTL output is high ($\geq$ 2.7 V); when an output is set to logical 0, the TTL output is low ($\leq$ 0.5 V).

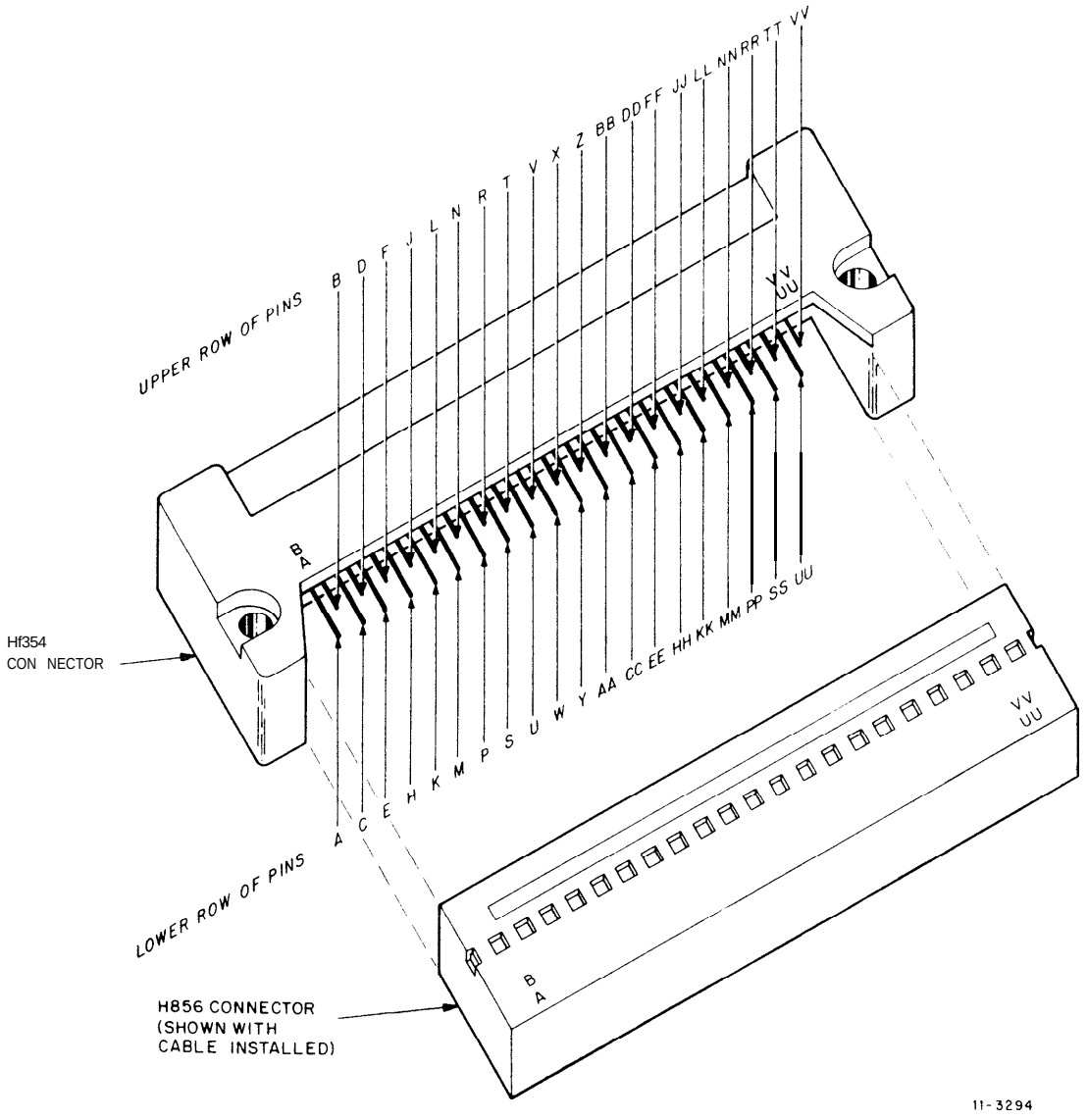


Figure 5-5 J1 or J2 Connector Pin Locations

All output Signals are TTL levels capable of driving five unit loads (8 mA sink** @ 0.5 V, 400 μA Source*** @ 2.7 V) except for the following:

NEW DATA READY = 10 unit loads	= 16 mA sink** @ 0.4 V, 400 μA Source*** @ 2.4 V
INIT (Initialize)* = 10 unit loads/connector	
DATA TRANSMITTED = 30 unit loads	= 48 mA sink** @ 0.4 V, 5 mA Source*** @ 2.7 V

*Common signal on both connectors.
** Sink refers to current from external +5 V supply through load to output line when output is low.
***Source refers to current from output line through load to ground when output is high.

Table 5-1 DRV11 Input and Output Signal Pins*

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	J2	TT	OUT00	J1	C
IN01	J2	LL	OUT01	J1	K
IN02	J2	H, E	OUT02	J1	NN
IN03	J2	BB	OUT03	J1	U
IN04	J2	KK	OUT04	J1	L
IN05	J2	HH	OUT05	J1	N
IN06	J2	EE	OUT06	J1	R
IN07	J2	c c	OUT07	J1	T
IN08	J2	Z	OUT08	J1	W
IN09	J2	Y	OUT09	J1	X
IN10	J2	w	OUT10	J1	Z
IN11	J2	V	OUT1 1	J1	AA
IN12	J2	U	OUT12	J1	BB
IN13	J2	P	OUT13	J1	FF
IN14	J2	N	OUT14	J1	HH
IN15	J2	M	OUT15	J1	JJ
REQ A	J1	LL	NEW DATA RDY*	J1	v v
REQ B	J2	S	DATA TRANS*	J2	C
			CSRO	J2	K
			CSR1	J1	DD
			INIT	J1	P
			INIT	J2	RR, NN

*Pulse Signals, approximately 300-ns wide. Width can be changed by user.

5.3.3 Input Data Interface

The input interface is the 16-bit DRINBUF read-only register, comprising gated bus drivers that transfer data from the user's device onto the LSI-11 bus under program control. DRINBUF is not capable of storing data; hence the user must keep input data on the IN lines until read by the LSI- 11 microprocessor. When it has read the data, the DRV11 generates a positive-going 300-ns DATA TRANSMITTED H pulse which informs the user's device that the data has been accepted. The trailing edge of the pulse indicates that the input transfer has been completed.

All input and request Signals are one Standard TTL unit load; inputs are protected by diode clamps to ground and +5 V. A +2.7 V to +5 V input is read as logical 1; 0 V to 0.5 V as logical 0.

5.3.4 Request Flags

Two signal lines (REQ A H and REQ B H) can be asserted by the user's device as flags in the DRCSR word. REQ B is available via connector no. 2 and can be read in DRCSR bit 15. REQ A is available via connector no. 1; it can be read in DRCSR bit 7. Two DRCSR interrupt enable bits, INT ENB A (bit 6) and INT ENB B (bit 5), allow automatic generation of an interrupt request when their respective REQ A or REQ B Signals are asserted. Once the user's request signal has been asserted (logical 0 to logical 1 transition), it must remain asserted until the CPU completes interrupt processing. At this time, DATA TRANSMITTED or NEW DATA READY Signals (see Paragraphs 5.3.2 and 5.3.3) can be used to cancel the request. Note that Request A has a higher priority than Request B, and that each of the interrupt enable bits can be set or reset under program control.

* Ground pins for connector J1: J, M, S, V, Y, CC, EE, KK, MM, PP, SS, UU. Connector J2: J, L, R, T, X, AA, DD, JJ, MM, PP, SS, UU.

5.3.5 Initialkation

The BINIT L processor-generated initialize signal is applied to DRV1 1 circuits for interface logic initialization. It is also available to the user's circuits via connectors J1 and J2 as follows:

Connector/Pin	Signal
J1/P	AINIT H
J2/RR	BINIT H
J2/NN	BINIT H

An active BINIT L signal will clear the following: DROUTBUF data; DRCSR bits 6, 5, 1, 0; bits 16 and 7 (when the maintenance cable is connected); and Interrupt Request and Interrupt Acknowledge flip-flops.

5.3.6 NEW DATA READY and DATA TRANSMITTED Pulse Width Modification

An optional capacitor can be added by the user to the DRVll module to extend the pulse width of both the NEW DATA READY and DATA TRANSMITTED pulses. The module without external capacitance (as shipped) will produce 300 ns pulses. The capacitor can be added in the location shown in Figure 5-2 to produce the approximate pulse widths listed below.

Optional External Capacitance (pF)	Approximate Pulse Width (ns)
None	300
1200	500
1800	600
6000	1200

5.4 PROGRAMMING

5.4.1 Addressing

Addresses for the DRV1 1 can range from 160000 through $17777X_8$. The least significant three bits address the desired DRV1 1 register as follows:

Address*	Device Register
1 xxxxo	DRCSR
1 xxxx2	DROUTBUF
1XXXX4	DRINBUF

Addresses 177560– 177566 are reserved for the console device and should not be used for DRV1 1 addressing. The following address assignments are normally used:

First DRVll
DRCSR = 167770
DROUTBUF = 167772
DRINBUF = 167774

Second DRV11
167760 to 167764

Third DRVll
167750 to 167754

*Address 1XXXX6 will not produce a response from the DRV1 1.

Second DRV11
167760 to 167764

Third DRV11
167750 to 167754

5.4.2 Interrupt Vectors

Two interrupt vectors are jumper-selected in the range of 0 through $37X_8$. The least significant three bits identify the interrupting function.

000xx0	Interrupt A
oooxx4	Interrupt B

Vectors 60 and 64 are reserved for the console device and should not be used for DRV11 vectors.

5.4.3 Word Formats

The three word formats associated with the DRV11 are shown in Figure 5-6 and are described in Table 5-2.

5.4.4 I/O Timing

I/O transfers through the DRV11 occur as illustrated in Figure 5-7.

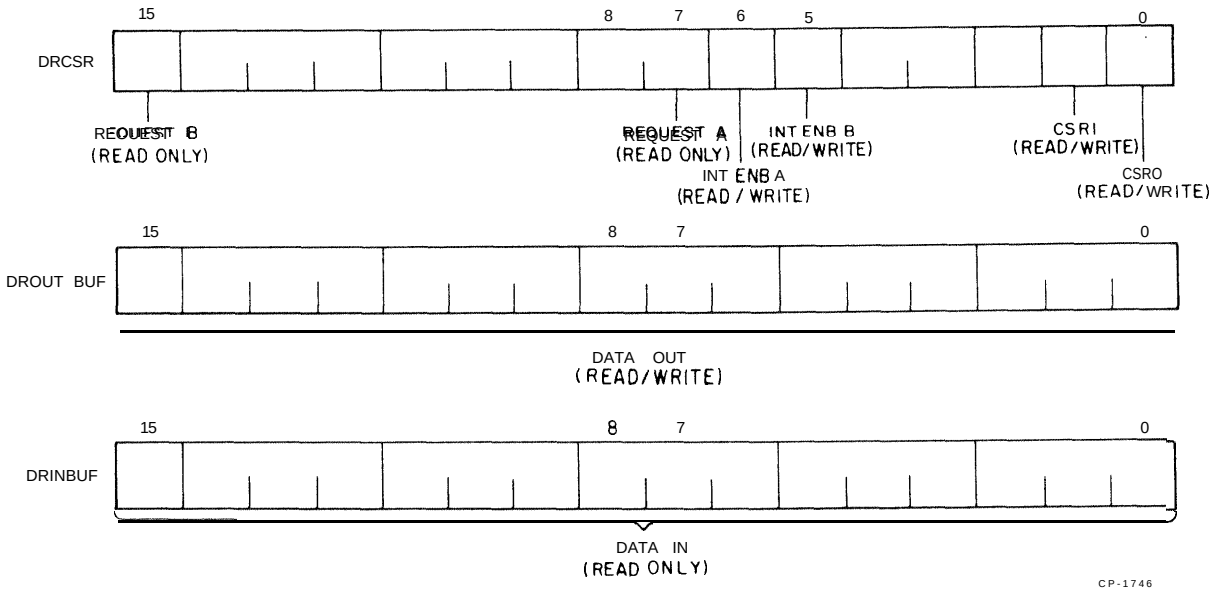


Figure 5-6 DRV11 Word Formats

Table 5-2 Word Formats

Word	Bit(s)	Function
DRCSR	15	REQUEST B — This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is asserted by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface Operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-Only bit. Cleared by INIT when in maintenance mode.
	14-08	Not used . Read as 0.
	07	REQUEST A — Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSRO (bit 00). Read-Only bit. Cleared by INIT when in maintenance mode.
	06	INT ENB A — Interrupt enable bit. When set, allows an interrupt request to be generated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by BINIT.
	05	INT ENB B — Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set.
	04-02	Not used. Read as 0. Can be loaded or read by the program (read/write bit). Cleared by INIT.

Table 5-2 Word Formats (Cont)

Word	Bit(s)	Function
DRCSR	01	CSR1 — This bit can be loaded or read (under program control) and can be used for a user-defined command to the device (appears only on Connector No. 1). When themaintenancecable is used, setting or Clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking Operation of bit 15 which cannot be loaded by the program. Can be loaded or read by the program (read/write bit). Cleared by INIT.
	00	CSRO- Performs the same functions as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.
DROUTBUF	15-00	Output Data Buffer - Contains a full 16-bit word or one or two 8-bit bytes: High Byte = 15-8; Low Byte = 7-o. Loading is accomplished under a program-controlled DATO or DATOB bus cycle. It can be read under a program-controlled DATI cycle.
DRINBUF	15-00	Input Data Buffer — Contains a full 16-bit word or one or two 8-bit bytes. The entire 16-bit word is read under a program-controlled DATI bus cycle.

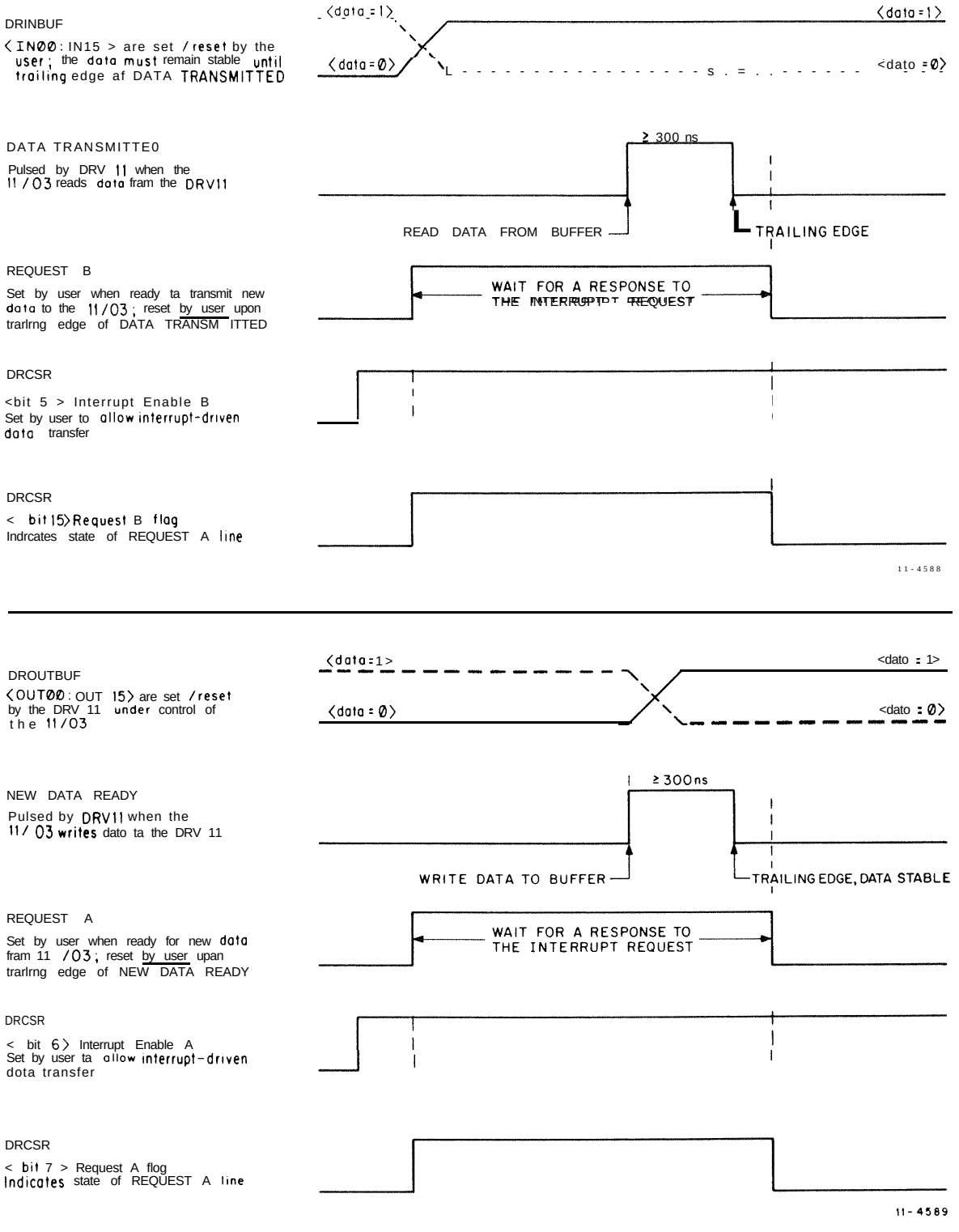


Figure 5-7 DRV1 1 Interface Signal Sequence

CHAPTER 6

ADV11-A, KWV11-A, and AAV11-A MAINTENANCE

6.1 MAINTENANCE PHILOSOPHY

Digital logic circuitry in the ADV11-A, KWV11-A, AAV11-A, and DRV11 is to be repaired in the normal manner. Analog circuitry, however, is to be repaired only at the factory. If any analog failures occur in the field, modules are to be board-swapped and returned to the factory for repair. Installations performed by DEC include installation of DEC-supplied equipment only. The customer is responsible for wiring from his equipment to the H322 Distribution Panel or to the end of the DEC-supplied cable.

6.2 ADV11-A ANALOG-TO-DIGITAL CONVERTER

6.2.1 Installation

6.2.1.1 Location - The ADV11-A is a Single-module option which interfaces to an LSI-11 or PDP-11/03 through one of the quad locations in the LSI-11 backplane or in an expander box. Within the constraints imposed by the LSI-11 bus structure (refer to the *LSI-11, Microcomputer Handbook - EB-06583 76 09/53*) the unit may be mounted in any available location and will operate within specifications, regardless of proximity to the processor, memory, or other DEC Options. Where circumstances permit, however, analog Performance may be improved beyond specification levels by installing the unit away from the processor, memory modules, or other noise-producing Options. Note that priority transfer requires that no empty unstrapped locations exist in the backplane between the processor and any device that communicates with it.

6.2.1.2 Address and Vector Selection - Select and set CSR and Vector addresses as indicated in Paragraph 2.4.3.4. Note that where more than one ADV11-A is involved, CSR addresses must be four locations apart (e.g., 170400, 170404, 170410, etc.). Vector addresses must be 10_8 locations apart (e.g., 000400, 000410, 000420, etc.). Remember to reinstall any covers removed from switch packs S1 and S2.

6.2.1.3 Board Insertion Select a quad location, and making sure that the keyed edge connector matches the physical configuration of the terminal block, apply firm pressure alternately to the extractor handles near the opposite corners of the board until it is squarely and fully seated in the connector.

6.2.1.4 Test Connector - Do not insert I/O cables into the Berg connector at this point. Instead, insert the 7012894 test connector, which establishes the conditions required by the ADV11 Wraparound Test - that is, all channel inputs are grounded except 1, 2, 3, and 17, with internally-generated +4.5 V signal on channel 1, -4.5 V signal on channel 2, ramp signal on channel 3, and Provision for external reference voltage on channel 17.

6.2.1.5 Shields - Install the 1700021-02 electromagnetic shields on both sides of the ADV11-A. Shields are insulated on both sides and physically separate the ADV11-A from adjacent modules but are not electrically connected to the System.

6.2.1.6 Acceptance - Conduct an acceptance test as specified in A-SP-ADV11A.

6.2.1.7 Final Connections

Cables
Remove the 7012894 test connector and install the BC08R cable (ADV11-A to H322 Distribution Panel) or the BC04Z cable (ADV11-A to user devices) in the ADV11-A Berg connector. Connect BC08R at both ends so that the stamped labels on the female cable ends match the embossed labels on the male connectors - A/B to A/B, UU/VV to UU/VV. This normally means that any "this side up" labels face away from the board on which the male connector is mounted.

NOTE

The BC08R cable is symmetrically wired but for several reasons is unsymmetrically labeled. That is, wires identified as A and B on one end are identified as UU and VV on the other end.

To simplify system relationships, the H322 PC board compensates for this inversion on the PC board that distributes Berg connector Signals to front panel screw terminals. For this reason, the user can connect both ends of the BC08R according to the labels, A/B to A/B and UU/VV to UU/VV. So connected, signals from the ADV11-A will properly appear at front panel terminals which have been labeled according to the instructions on the ADV11-A decal sheet. Each BC04Z cable from an ADV11-A may be terminated in a female 25-pin connector such as a DB25S type (DEC 12-09326-00) socket. The user may assign the signal and ground lines from the BC04Z to specific connector pins. User apparatus may be connected to the socket by means of a male 25-pin connector such as a DB25P type plug (DEC 12-05886-00).

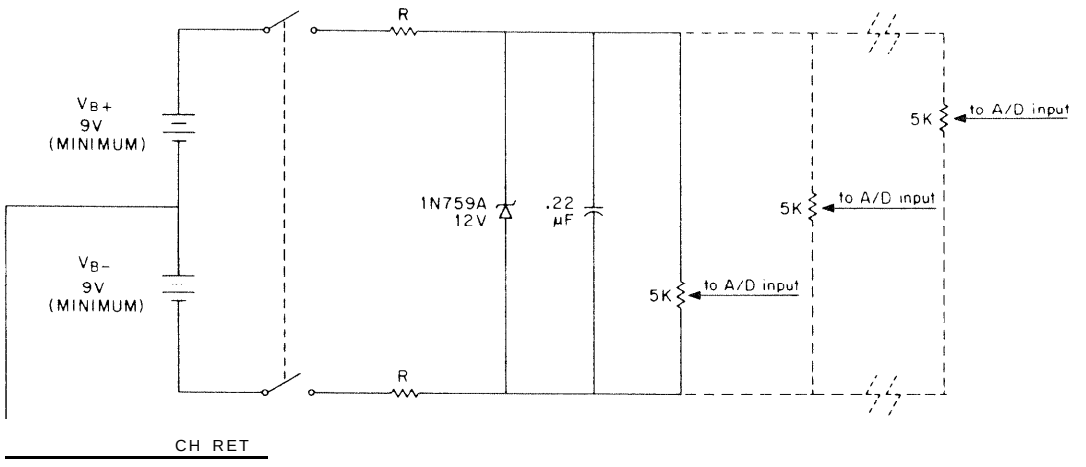
If KWV11-A is present, connect Faston terminals, as described in Paragraph 2.4.3.2.

Manual Voltage Control
Applications which require variable dc voltages to be applied to one or more channels of the ADV11-A can be implemented by the circuit illustrated in Figure 6-1. Note that the H323-B Potentiometer Box may *not* be used with the ADV11-A.

6.2.2 ADV 11-A Circuitry
The digital interface and control logic of the ADV11-A conforms in general to standard DEC practices and should be understandable to qualified technicians who have access to ADV11-A print sets and are familiar with Overall ADV11-A functions as described in Chapter 2. Since the analog power supply and the A/D conversion sections involve some nonstandard circuits, they are discussed below.

6.2.2.1 ADV11-A Analog Power Supply

General
The ±15 V power for the analog circuits is derived from a dc-dc converter which consists of three basic sections: a 12 V power switch, positive and negative voltage doubler diode-capacitor banks, and a dual tracking voltage regulator. Output jumpers (W1 and W2) are provided to permit removing the load for troubleshooting purposes.



NOTE

Value of R in kilohms can be calculated as follows

$$R = \frac{V_B - 6}{2.5\ (N+2)}\ K\Omega \qquad (1)$$

Where N = Number of channel pots

Current drain from battery in milliamps when R is selected with equation (1) can be calculated as follows:

$$I_{bat} = 2.5\ (N+2)\ mA \qquad (2)$$

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Figure 6-1 Battery-Operated Potentiometer Box for ADV11-A A/D Converter

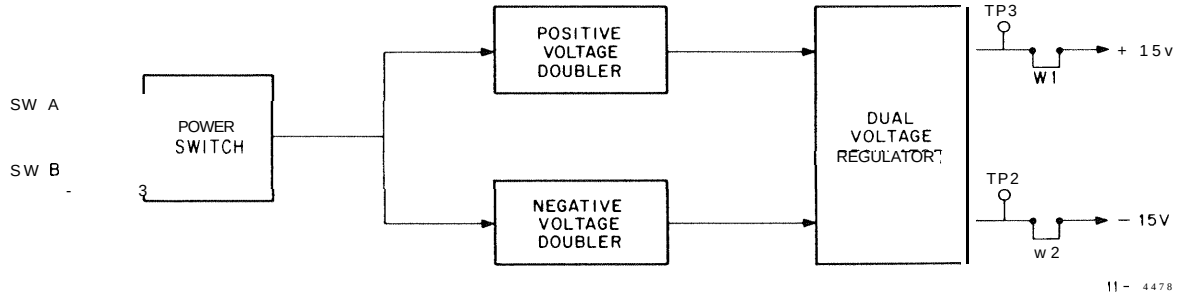


Figure 6-2 Analog Power Supply Block Diagram

Power Switch

Transistors Q15 and Q 16 constitute the output stage of the 12 V power switch and provide a 0 V to + 12 V switching Signal, which is derived from the SW A and SW B Signals, and which drives the voltage doubler diode-capacitor banks. Since saturated transistor switches turn on faster than they turn off, an idle is included (see Figure 6-3) to ensure that Q15 and Q16 are never on at the same time.

Voltage Doublers

The basic voltage doubler consists of a charge transfer stage (D_A and C_A in Figure 6-4) and a charge storage stage (D_B and C_B in Figure 6-3). When the power switch output is at 0 V, C_A charges to $V_{IN} - V_{DA}$ (+11.3 V). When the power switch output goes to + 12 V, D_A is reverse-biased and charge is transferred from C_A to C_B. The power switch output then returns to 0 V, reverse-biasing D_B and recharging C_A - DA. The voltage on C_B builds up to approximately + 12 V - V_{DA} + 12 V - V_{DB}.

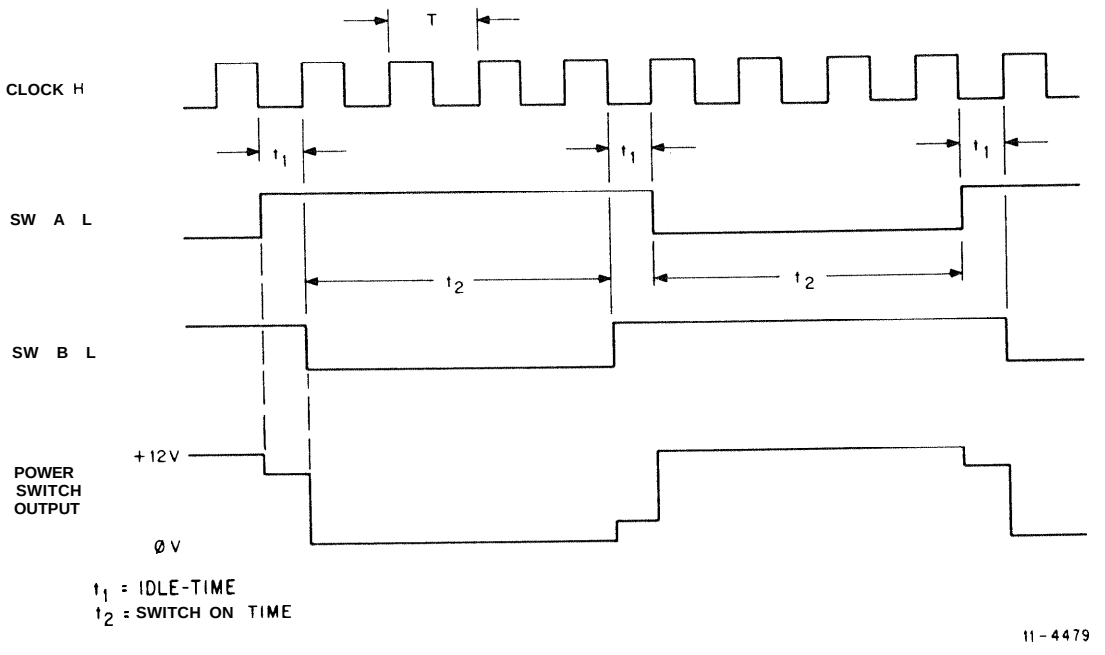


Figure 6-3 DC-DC Converter Signals

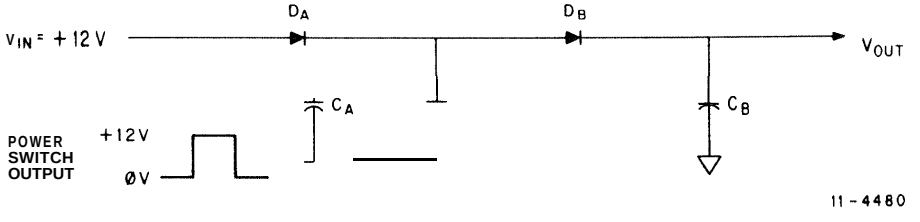


Figure 6-4 Basic Positive Voltage Doubler

The negative voltage doubler operates in a similar manner and consists of two basic doubler circuits in cascade with an additional input negative voltage generating stage (D26 and C47).

Dual Voltage Regulator

The dual voltage regulator comprises an LM325N (E50) tracking regulator and power boosters (Q17 and Q18). Output current limit sensing is provided by R60 and R61. This stage regulates the Outputs from the doubler circuits to provide the ± 15 V of analog power required by the various analog circuits.

6.2.2.2 ADV11-A A/D Conversion Circuit - The ADV11-A A/D converter circuit utilizes a patented auto-zeroing, successive approximation technique. The basic components of this circuit are illustrated in Figure 6-5.

Analog Multiplexer

The analog multiplexer consists of two 8-channel, Single-ended multiplexer ICs (E47 and E48) whose Outputs are connected together, thus forming a 16-channel multiplexer. During Sample, when no conversion is in process, the addressed multiplexer channel is on. During hold, two conditions are possible. If Single-ended (SE) mode is picked, all channels of the multiplexer are off and the auto-zero switch is on. If SE mode is not picked, the negative side of the selected quasi-differential pair is selected.

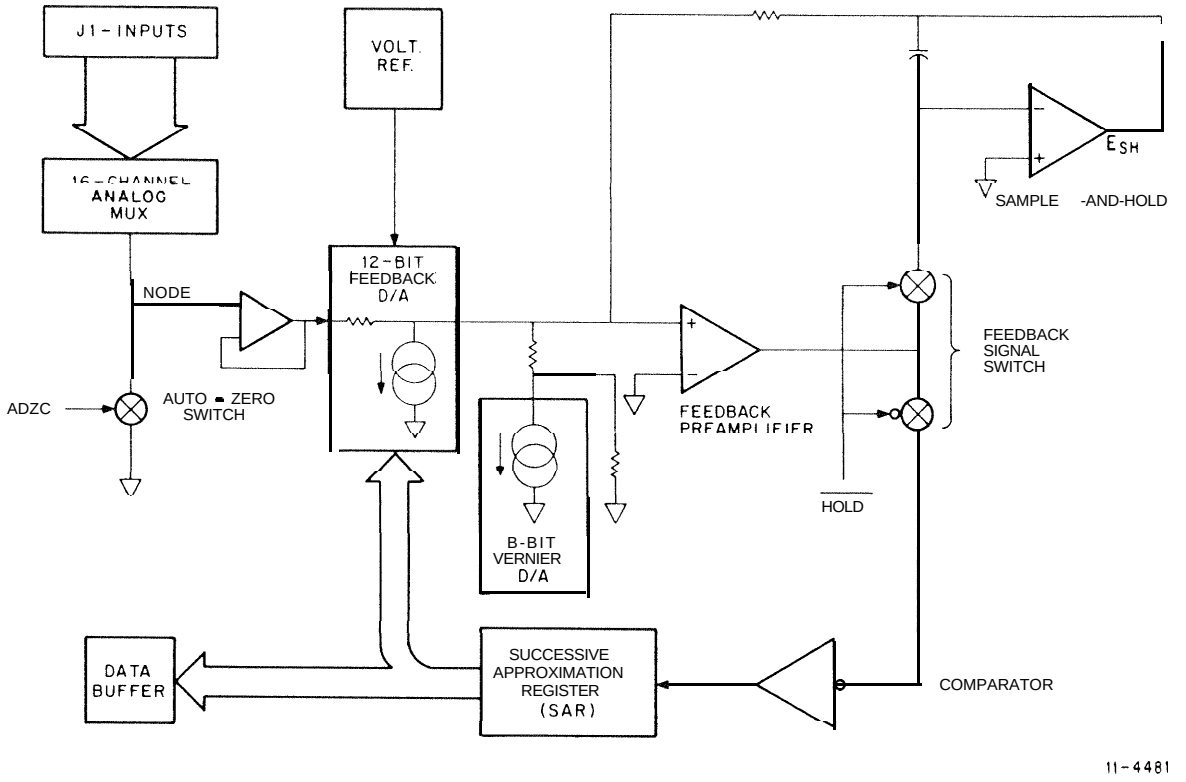


Figure 6-5 ADV1 1-A A/D Conversion Circuit Block Diagram

Auto-Zero

During Sample, the feedback signal switch (QS, Q6, Q8, Q9, Q10, and Q1 1) connects the output of the feedback preamplifier (Q2 - Q4) to the input of the Sample-and-hold (Q13, E5 1, C67), thus completing the amplifier feedback path and allowing the Sample-and-hold to track the analog input (see Figure 6-6).

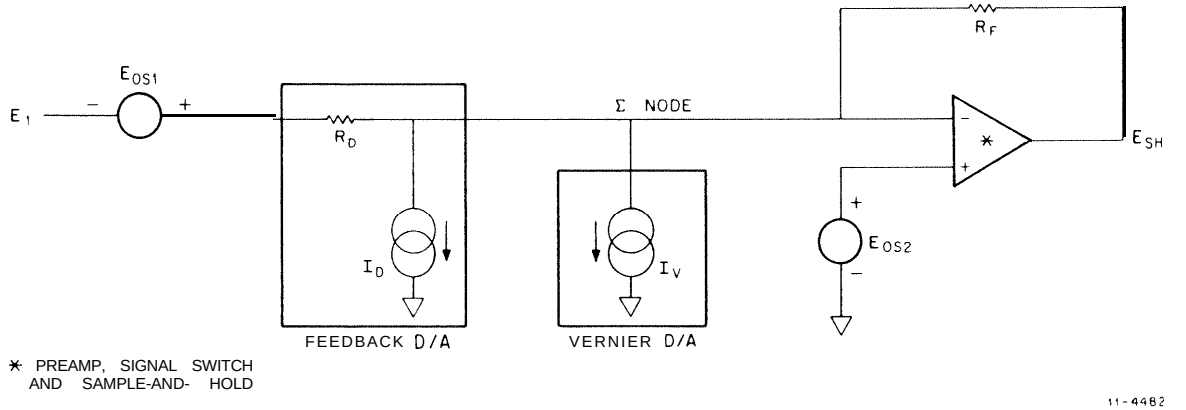


Figure 6-6 A/D During Sample

Summing currents into the $\sum$ node:

$$I_D = \frac{E_1 + E_{OS1} - E_{OS2}}{R_D} + \frac{E_{SH} - E_{OS2}}{R_F} - I_V \qquad (1)$$

E_{OS1} is the offset of the input buffer amplifier (E49) and E_{OS2} is the offset of the feedback preamplifier.

When a conversion is initiated, the feedback signal switch disconnects the output of the feedback preamplifier from the input of the Sample-and-hold, thus storing the signal, and connects the pre-amplifier output to the comparator (Q7 and 412) input. Next, the A/D input, E_1, is either switched to the negative channel or is grounded through the auto-zero switch, E44, depending upon whether or not Single-ended Operation was selected.

At the completion of the conversion, the $\sum$ node is ideally equal to E_{OS2}' (see Figure 6-7).

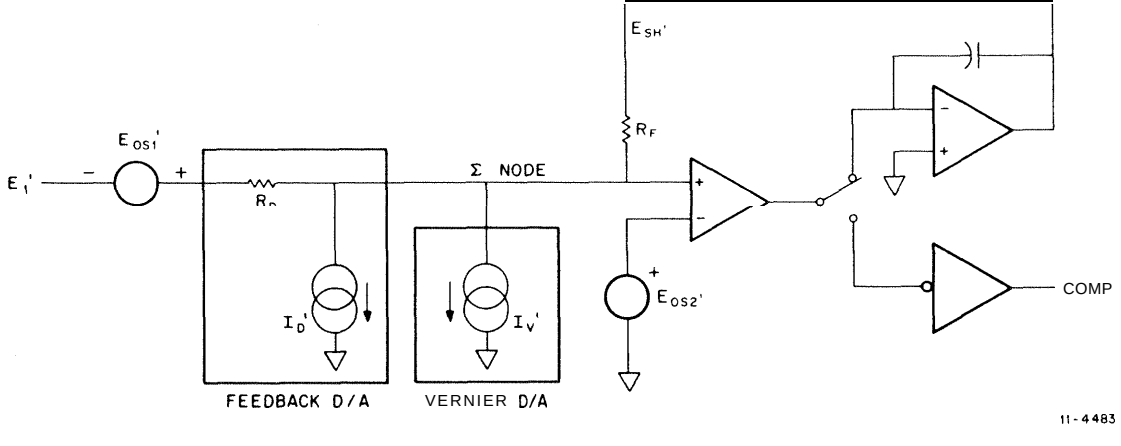


Figure 6-7 A/D During Conversion

Again summing currents into the $\sum$ node:

$$1,' = \frac{E_1' + E_{OS1}' - E_{OS2}'}{R_D} + \frac{E_{SH}' - E_{OS2}}{R_F} - 1,' \qquad (2)$$

Where I_D' is the feedback D/A cwrent at the completion of the LSB interrogation.

Subtracting equation (2) from equation (1):

$$I_D - I_D' = \frac{E_1 - E,'}{R_D} - (I_V - I_V') + \frac{E_{OS1} - E_{OS1}'}{R_D} - \frac{E_{OS2} - E_{OS2}'}{R_F // R_D} + \frac{E_{SH} - E_{SH}'}{R_F} \qquad (3)$$

Note that since the offset due to the input buffer is the same in both cases,

$$\frac{E_{OS1} - E_{OS1}' = E_{OS1} - E_{OS1}}{R_D \qquad R_D} = 0$$

$E_{OS2} - E_{OS2'}$ is controlled by R 15 by forcing an offset shift in the feedback preamplifier and is used to null the offset caused by the Sample-and-hold pedestal ($E_{SH} - E_{SH'}$). Note also that the conversion is not dependent upon the magnitude of E_{OS2}, but upon the forced shift. Therefore:

$$I_D - I_D' = \frac{E_1 - E_1'}{R_D} - (I_V - I_V')$$

If no vernier offset is programmed, $I_V = I_V'$,

and:

$$I_D - I_D' = \frac{E_1 - E_1'}{R_D} \qquad (4)$$

A / D Conversion

The 12-bit feedback D/A (E46) is initialized to 4000_8.

$$I_D = 1/2\ I_{FSR} - I_{LSB} \qquad (5)$$

During conversion, each bit of the feedback D/A is interrogated in sequence by the SAR (E39), starting with the MSB. At the end of each interrogation interval, the decision of the comparator to accept or reject that bit is clocked into the SAR where this decision is held. A positive voltage on the Σ node will cause the comparator to reject a bit. Because of the Overall negative feedback, this process will cause the Σ node to work its way toward null (Figure 6-8). After the LSB interrogation, the contents of the SAR are transferred to the Data Buffer register.

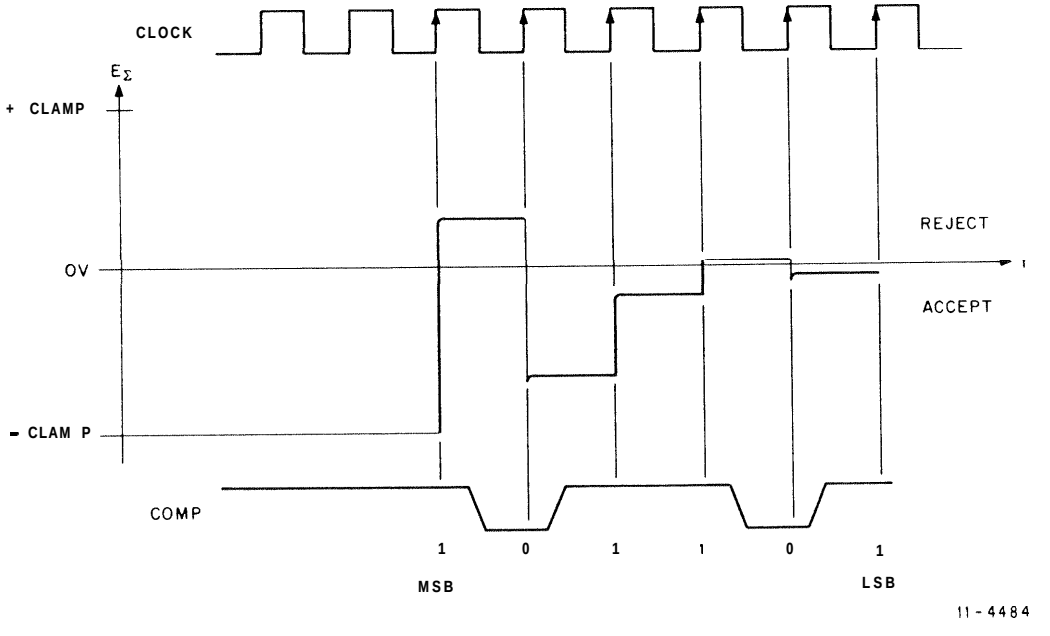


Figure 6-8 Σ Node During Conversion

Since

I_D' min = 0 (@ code = 7777)

and

I_D' max = $I_{FSR} - I_{LSB}$ (@ code = 0000),

equations (4) and (5) permit voltage/current conversions to be derived as illustrated in Table 6-l.

Table 6-1 ADV11-A Voltage/Current/Bit Relationships

I_D'	Code	I_D-1, '	$E_1 - E_1'$
0	7777	$1/2 (I_{FSR} - I_{LSB})$	$1/2 (E_{FSR} - E_{LSB})$
$1/2 (I_{FSR})$	3777	-1_{LSB}	$-E_{LSB}$
$I_{FSR} - 1_{LSB}$	0000	$-1/2 (I_{FSR})$	$-1/2 (E_{FSR})$

6.2.2.3 The Vernier DAC - The Vernier DAC is a digital-to-analog converter packaged in a single chip serving to provide programmable small increment offsets to the summing node of the A/D converter. It has been included in the ADV1 1-A circuit primarily to facilitate automatic testing of the module and is used by the diagnostic routines in the measurement of noise, offset error, and interchannel settling error. The Vernier DAC is controlled through bits 07:00 of the Data Buffer register (write-only), accepting 8-bit offset binary code to produce positive and negative full scale offsets of 2.5 A/D LSBs.

6.2.3 ADV11-A Performance Test (MAINDEC-1 1-DVADA-A)

This diagnostic package permits complete testing of all functional aspects of the ADV11-A. It is divided into four major routines which are described below. Refer to diagnostic listing MAINDEC-1 1-DVADA-A for run instructions.

1. Wraparound Routine - consists of four subtests which can be run individually or consecutively:

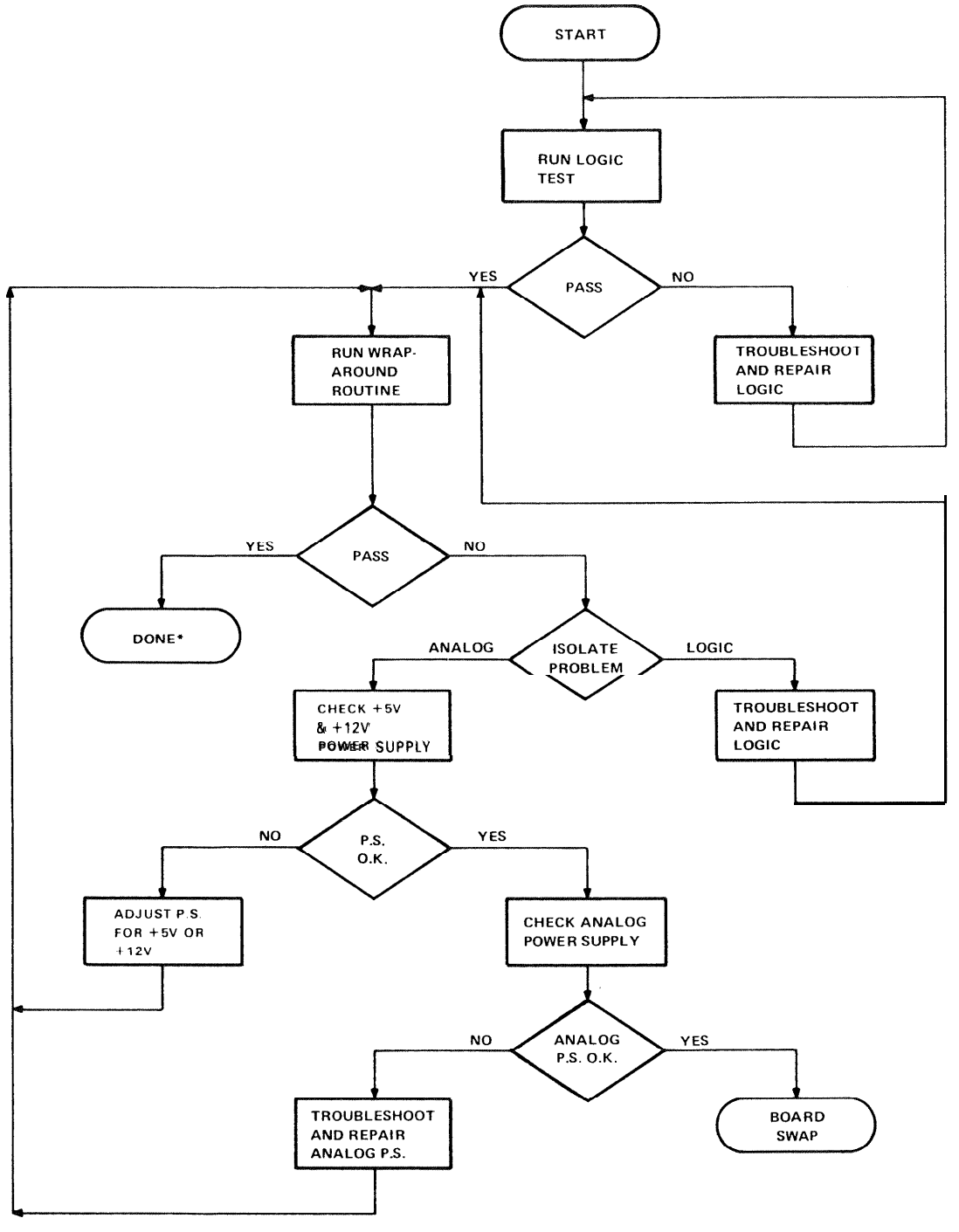
   a. Analog Test - checks all channels and their Outputs to ascertain whether or not multiplexing and gross conversion functions are working.

   b. Noise Test - determines whether or not the amount and distribution of short-term noise within the A/D converter is within limits.

   c. Interchannel Settling Test - Determines whether or not the A/D converter can recover from measurements at opposite extremes within specified times (switches alternately between channels 1 and 2 - i.e., between +4.5 V and -4.5 V).

   d. Differential Linearity and Relative Accuracy Test - makes multiple randomized measurements of ramp signal on channel 2 to determine, within 0.01 LSB, the width of the voltage band corresponding to each of the 4094 finite width states.

2. Calibration Routine - works interactively with Operator to facilitate precise calibration of A/D. Requires precision voltage Source.



● Calibration routine can be run at this point if precision voltage source (EDC VS-1 1 N or equivalent) is available.

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Figure 6-9 ADV1 1-A Troubleshooting Procedure

3. Print Values routine - works interactively with Operator to execute, and if desired, print out results of conversions on selected channels.

4. Logic Test Routine - consists of 23 subtests that run sequentially without Operator intervention and check status register read/write Operation, initialize conditions, A/D done flag setting and Clearing, error flag setting, interrupt functions, etc.

6.2.4 Maintenance

In general, both routine maintenance and specific troubleshooting efforts will follow the flow defined in Figure 6-9. Preventive maintenance will consist of removing airborne dust accumulations, checking the power supply levels whenever new devices are added to the system, and running diagnostics whenever Performance confirmation is desired.

6.2.5 Calibration (Requires Precision Voltage Source - EDC VS-l 1N or Equivalent)

With test connector installed in ADV1 1-A Berg socket, connect the *floating* reference voltage to the two clip-terminated leads (channel 17). Then, run the Calibration Routine and follow the step-by-step instructions it issues. The program will specify reference voltage settings and indicate when offset and gain potentiometers (identified in Figure 2-6) should be adjusted.

6.3 KWV11-A REAL TIME CLOCK

6.3.1 Installation

6.3.1.1 Location - The K WV1 1-A is a Single-module option which interfaces to an LSI-11 through one of the quad locations in the LSI-11 backplane or in an expander box. Within the constraints imposed by the LSI-11 bus structure (refer to the *Microcomputer Handbook* - ***EB-06.583 76*** *09/53*), the unit may be mounted in any available location. Note that LSI-11 priority transfer requires that no empty unstrapped locations exist between the processor and the last device connected to the LSI-11 bus.

6.3.1.2 Address and Vector Selection - Select and set CSR and Vector Addresses as indicated in Paragraphs 3.4.3.1 and 3.4.3.2. Note that where more than one KWV11-A is connected to the same bus, CSR addresses must be four locations apart (e.g., 170420, 170424, 170430, etc.). Vector addresses for multiple KWV1 l-As must be 10_8 locations apart (e.g., 000440, 000450, 000460, etc.). Remember to reinstall any covers on switch packs S1 and S3.

6.3.1.3 Board Insertion - Select a quad location, and making sure that the KWV1 1-A board is oriented so that the keyed edge connector matches the physical configuration of the terminal block, apply firm pressure alternately to the extractor handles near the opposite corners of the board until it is squarely and fully seated in the connector.

6.3.1.4 Test Connections - Do not connect user equipment to Berg connector J1 at this time. Diagnostic I/0 signal tests will require jumpers between specified pins on J1.

6.3.1.5 Acceptance - Conduct an acceptance test as specified in A-SP-KWV1 l-A-3.

6.3.2 Final Connections

Install FAST ON connectors between CLK/ST1 tabs and ADV11-A tabs as required. Install the BC08R cable (KWVI 1-A to H322 Distribution Panel) or BC04Z cable (KWV11-A to user devices) between the Berg connector (J1) and the appropriate terminus. Connect the BCO8R at both ends so that the stamped labels on the female cable ends match the embossed labels on the male connectors - A/B to A/B, UU/VV to UU/VV. This normally means that any "this side up" labels face away from the board on which the male connector is mounted. (See Note in Paragraph 6.2.1.7.)

6.3.3 KWV 11-A Circuitry

The digital logic of the KWV1 1-A conforms in general to Standard DEC practices and should be understandable to qualified technicians who have access to KWV1 **1-A** print sets and are familiar with KWV 1 1-A functions as described in Chapter 3.

6.3.4 KWV11-A Diagnostic (MAINDEC-1 l-DVKWA-A-D)

The KWV1 I-A diagnostic is divided into two main routines, the first designed to test logic functions on up to four KWV1 1-A modules, the second to test selected module I/O functions, ST1, ST2, and clock Overflow. Refer to diagnostic listing MAINDEC- 11 -DVKWA-A-D for run instructions.

6.3.5 Maintenance

Preventive maintenance consists of removing airborne dust accumulations, checking that power supply levels remain within specifications whenever new devices are added to a system, and running diagnostics whenever Performance confirmation is desired.

6.4 AAV11-A DIGITAL-TO-ANALOG CONVERTER

6.4.1 Installation

6.4.1.1 Location - The **AAV** l l-A is a Single-module option which interfaces to an LSI-11 or PDP-1 1/03 through one of the quad locations in the LSI-11 backplane or in an expander box. Within the constraints imposed by the LSI-11 bus structure (refer to the *Microcomputer* ***Handbook - EB-06.583 76*** *09/53*) the unit may be mounted in any available location and will operate within specifications, regardless of proximity to the processor, memory, or other DEC Options. Where circumstances permit, however, analog Performance may be improved beyond specification levels by installing the unit away from the processor, memory modules, or other noise-producing Options. Note that priority transfer requires that no empty unstrapped locations exist in the backplane between the processor and any device that communicates with it.

6.4.1.2 Address Selection - Select and set address as indicated in Paragraph 4.4.2. Note that the least significant three bits of the address word are reserved for Software addressing of the four digital-to-analog converters (DACs) and are therefore not selectable on the switch pack. For this reason, if several AAV 1 1 -As are installed on a System, they must be assigned addresses that are 10_8 locations apart.

6.4.1.3 Board Insertion - Select a quad location on the connector block, and making sure that the AAV 1 I-A board is oriented so that the keyed edge connector matches the physical configuration of the connector block, apply firm pressure alternately to the extractor handles near the opposite corners of the board until it is squarely and fully seated in the connector block.

6.4.1.4 Test Connectors - If **AAV** 11-A signals are to be routed to the H322 Distribution Panel, connection may be made to that unit at this time (see Paragraph 6.4.2). Otherwise, leave the Berg connector empty to allow for monitoring AAV1 1-A output Signals in the next step.

6.4.1.5 Acceptance Test - Conduct an acceptance test as described in the AAV1 1-A Manufacturing and Field Acceptance Procedure (A-SP-AAV 1 l-A-3).

6.4.2 Final Connections

Install the BC08R cable (AAV 1 l-A to H322 Distribution Panel) or BC04Z cable (AAV 1 l-A to user devices) between Berg connector (J1) and the appropriate terminus. Connect BC08R at both ends so that the stamped labels on the female connectors match the embossed labels on the male connectors - A/B to A/B, UU/VV to UU/VV. This normally means that any "this side up" labels face away from the board on which the male connector is mounted. (See Note in Paragraph 6.2.1.7.)

6.4.3 Mode/Level Selection

As shipped from the factory, the AAV11-A is set for bipolar Operation between -5.12 V and +5.12 V. Unipolar Operation and Operation in other voltage ranges can be achieved by proper changes in mode/level jumpers (illustrated in Figure 4-2). Table 6-2 indicates jumper configurations for all bipolar voltage ranges; Table 6-3 indicates those for all unipolar ranges. Note that each of the four DACs on any given AAV11-A may be set for a different mode/level condition. Note also that any change from the factory settings may require recalibration of the DAC involved (see Paragraph 6.4.7).

Table 6-2 Jumper Configurations for Bipolar Operation

	f2.56 V	f5.12 V	± 10.24 V
DAC 1			
W3	IN	IN	OUT
w4	OUT	OUT	IN
W5	IN	OUT	OUT
W6	IN	IN	IN
DAC 2			
w7	IN	IN	OUT
W8	OUT	OUT	IN
w9	IN	OUT	OUT
W10	IN	IN	IN
DAC 3			
W11	IN	IN	OUT
w12	OUT	OUT	IN
w13	IN	OUT	OUT
w14	IN	IN	IN
DAC4			
w15	IN	IN	OUT
W16	OUT	OUT	IN
w17	IN	OUT	OUT
W18	IN	IN	IN

6.4.4 AAV l l-A Circuitry

The digital interface and control logic of the AAV11-A conforms in general to Standard DEC practices and should be understandable to qualified technicians who have access to AAV11-A print sets and are familiar with Overall AAV1 1-A functions as described in Chapter 4. The analog power supply and the digital-to-analog circuitry, however, make use of techniques and components with which DEC technicians may not be familiar. Since the analog power supply and the D/A conversion sections involve some non-standard circuits, they are discussed below.

6.4.4.1 AAV1 1-A Analog Power Supply

General (see Figure 6-l)

The ± 15 V power for the analog circuits is derived from a dc-dc converter which consists of three basic sections: a 12 V power switch, positive and negative voltage doubler diode-capacitor banks, and a dual tracking voltage regulator-

Table 6-3 Jumper Configurations for Unipolar Operation

	0 V – +5.12 V	0 V – +10.24 V
DAC 1		
w3	IN	**IN**
W4	OUT	OUT
W5	IN	OUT
W6	OUT	OUT
DAC 2		
W7	IN	IN
W8	OUT	OUT
w9	IN	OUT
W10	OUT	OUT
DAC 3		
W11	**IN**	IN
W12	OUT	OUT
w13	IN	OUT
W14	OUT	OUT
DAC 4		
w15	IN	**IN**
W16	OUT	OUT
w17	IN	OUT
W18	OUT	OUT

Table 6-4 AAV11-A Input Code/Output Voltage Relationships

Input Code	Unipolar	Bipolar
0000	0 V	– FS
4000	1/2 FS	o v
7777	+FS – 1/2 LSB	+FS – 1/2 LSB

Power Switch

Transistors Q2 and Q3 constitute the output stage of the 12 V power switch and provide a 0 V to + 12 V switching signal, which is derived from the SW A and SW B signals, and which drives the voltage doubler diode-capacitor banks. Since saturated transistor switches turn on faster than they turn off, an idle time is included (see Figure 6-2) to ensure that Q2 and Q3 are never on at the same time.

Voltage Doublers

The basic voltage doubler consists of a charge transfer stage (D_A and C_A in Figure 6-3) and a charge storage stage (D_B and C_B in Figure 6-3). When the power switch output is at 0 V, C_A charges to $V_{IN} - V_{DA}$ (+ 11.3 V) through DA. When the power switch output goes to + 12 V, D_A is reverse-biased and charge is transferred from C_A to C_B through D_B. The power switch output then returns to 0 V, reverse-biasing D_B and recharging C_A through DA. The voltage on C_B builds up to approximately + 12 V – V_{DA} + 12 V – V_{DB} (+22 V).

The negative voltage doubler operates in a similar manner and consists of two basic doubler circuits in cascade with an additional input negative voltage generating stage (D21/22 and C42/43).

Dual **Voltage** Regulator
The dual voltage regulator comprises an LM325N (E38) tracking regulator and power boosters (Q4 and Q5). Output current limit sensing is provided by R57 and R58. This stage regulates the Outputs from the doubler circuits to provide the ± 15V of analog power required by the various analog circuits.

6.4.4.2 Digital-to-Analog Circuits - The analog sections of the AAV11-A consist of four 12-bit D/A converters (each contained on one 24-pin chip), four 2505 operational amplifiers. and a + 10 V precision reference Source.

Each D/A converter (DAC) contains the necesary circuits to generate a O-2 mA output current and to modify that current as a function of the 12 input data bits. A 1-LSB change in the data register corresponds to a change of 1 part in 4096 of the full scale output, approximately 1/2 μA.

The output of the DAC is fed into a 2505 operational amplifier which converts the drive current into a voltage output. The feedback from the output of the amplifier is passed through the selected feedback resistors. The interconnections between these resistors, determined by the mode/range straps illustrated in Figure 4-2, determine the operating mode (unipolar or bipolar) and voltage range of the DAC in question.

Gain and offset of each DAC are controlled through the externally-adjustable potentiometers (see Figure 4-2).

6.4.5 AAV11-A Diagnostic Test (MAINDEC-11-DVAAA-A)
The AAVI 1-A Diagnostic Test is divided into four routines. Each is briefly described below.

1. Logic Tests (starting address: 200) - exercises and monitors behavior of interface and control logic of all DACs on all AAV1 l-As in a System. Checks that DAC holding registers can be loaded, cleared, and modified without error.

2. Ramp Loop (starting address: 204) - reiteratively increments the holding register for each DAC to produce full-scale ramp voltages successively at the output of each DAC. Permits confirmation by oscilloscope of DAC linearity, settling time, and channel isolation.

3. Static Calibration Loop (starting address: 210) - permits Operator to input control data to all DACs and monitor resulting output conditions. Run with a precision DVM as output monitor-, the Static Calibration Loop permits calibration of gain and offset of each DAC.

4. Dynamic Calibration Loop (starting address: 214) - reiteratively switches each DAC between maximum and minimum output conditions. Facilitates checking DAC response and recovery characteristics as well as amplifier slew rates.

6.4.6 Maintenance
In general, both routine maintenance and specific troubleshooting efforts will follow the flow defined in Figure 6- 10. Since the diagnostic program has no way of evaluating AAV 11 -A analog Performance, pass or failure of all but the logic tests depends on the judgment of the Operator. Refer to the AAV1 l-A Manufacturing and Field Acceptance Procedure (A-SP-AAV1 l-A-3) for applicable criteria.

Preventive maintenance consists of removing airborne dust accumulations, checking that power supply levels remain within specifications whenever new devices are added to a System, and running diagnositics whenever Performance confirmation is desired.

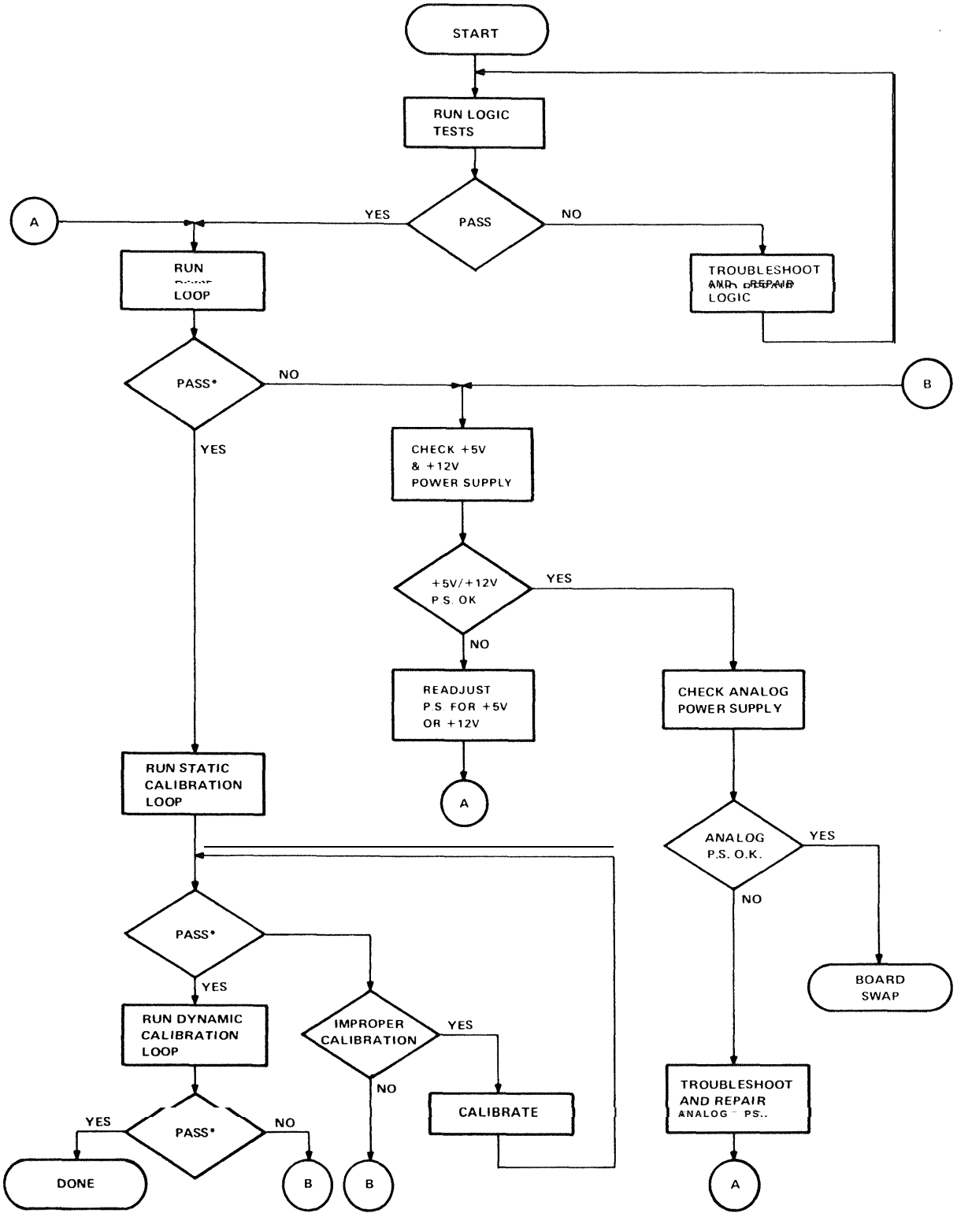


Figure 6- 10 AAV 11 -A Troubleshooting Procedure

6.4.7 Calibration

Prepare the system to permit access to signal line(s) and calibration potentiometers of DAC(s) to be calibrated. Connect DVM of appropriate precision (note that 1 LSB on ±2.56 V bipolar or 0 -5.12 V unipolar = 1.25 mV) to output of DAC to be measured. Float the DVM as illustrated in Figure 6-l 1. Take care to connect DVM common lead to HQ ground associated with the DAC in question. Then proceed as follows:

1. Load DAC holding register with 0000.
2. Adjust offset Potentiometer (see Figure 4-2) for DVM reading appropriate to selected mode/level condition (see Table 4-l).
3. Load DAC holding register with 7777.
4. Adjust gain Potentiometer for DVM reading appropriate to selected mode/level condition (see Table 4-l).
5. Load DAC holding register with 4000.
6. Check DVM for reading appropriate to selected mode/level condition (see Table 4-l).

Step 6 should produce a reading accurate to 1-1/2 LSB.

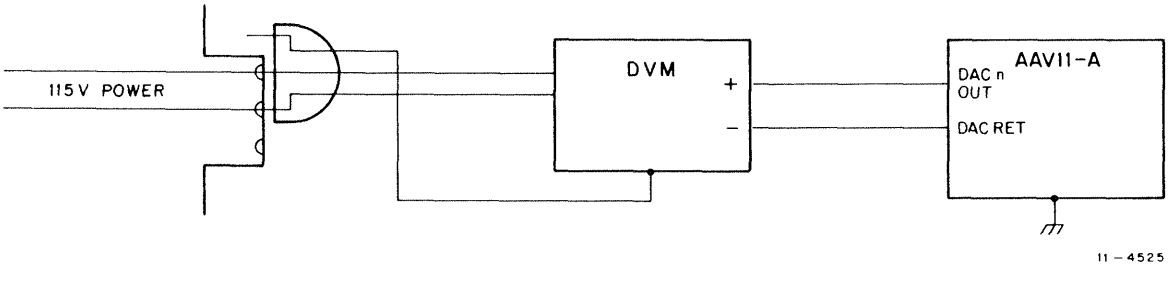


Figure 6- 11 Floating the DVM

6.5 DRV11 PARALLEL LINE INTERFACE

Refer to the *Microcomputer* ***Handbook (EB-06583 76*** *09/53*).

GLOSSARY OF A/D TERMS

Absolute Accuracy
The analog error. expressed as a percentage of full scale, referenced to the National Bureau of Standards volt.

Acquisition Time
The time duration betueen the giving of the sample command and the point when the output remains within a specified error band around the input value.

Aperture Delay Time
The time elapsed between the hold command and the point at which the sampling switch is completely open.

Aperture Uncertainty
The variation in aperture delay time for a particular Sample-and-hold.

Common Mode Rejection (CMR)
The ability of a differential amplifier to reject noise common to both inputs. Common mode rejection is expressed as a ratio, the Common Mode Rejection Ratio (CMRR). A differential amplifier with a CMRR of 80 dB (10,000: 1) would have an output voltage of 0.5 mV if both inputs were 5 V (5 V/80 dB).

Crosstalk
The amount of signal coupled to the output as a percentage of input signal applied to all off channels.

Differential Inputs (True)
Two external signals applied to the input circuitry of an A/D system whereby the first is subtracted from the second. The difference is applied to the A/D system. This is generally used with twisted pair wiring to reduce noise pickup.

Example

$$V_O = (V+) - (V-)$$

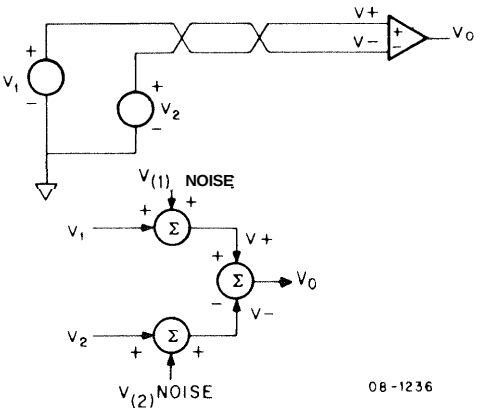
$$= [V_1 + V_{(1)}\ \text{noise}] - [V_2 + V_{(2)}\ \text{noise}]$$

$$= [V_1 - V_2] + [V_{(1)}\ \text{noise} - V_{(2)}\ \text{noise}]$$

For twisted pair wiring:

$$V_{(1)}\ \text{noise} \doteq V_{(2)}\ \text{noise}$$

$$\therefore V_0 \doteq V_1 - V_2$$



Differential Inputs (Psuedo)
This method of inputting is similar to true differen tial inputting except that the negative input to the A D system is common to the other inputs.

Differential Linearity
The maximum deviation of an actual stated width from its theoretical value for any code over the full range of the converter. A differential linearity of ± 1, 2 LSB means that the width of each code over the range of the converter is 1 LSB ± 1 2 LSB. Missing codes in an A, D converter occur when the output code skips a digit. This happens w hen the differential linearity is worse than ± 1 LSB.

Drift
Drift is a function of the temperature coefficients of the components. It is the major contributor to gain and offset error.

Gain Error
The error, expressed as a percentage, by w hich the actual full scale range differs from the theoretical full scale range. This error is adjustable to zero.

Gain Temperature Coefficient
This is the amount of gain that changes with a change in temperature. This may be expressed in ppm /° C or ° C/LSB at full scale. If an A/D has a gain temperature coefficient of 20" C/LSB at F.S., the A/D converted value will be off by 1 LSB at full scale if the temperature rises 20" C above 25° C.

Input Bia s Current
The amount of current that flows into the selected A /D channel from the source.

Input Impedance (dc)
The resistance seen at the input to an A/D system.

Linearity
Linearity is defined as the maximum deviation from a straight line drawn between the end points of the converter transfer function. Linearity may be expressed as a percentage of full scale or as a fraction of an LSB.

Multiplexer
The multiplexer is a set of suitches that permits analog data from different sources (channels) to he supplied to the Sample-and-hold (or A /D converter) individually.

Multiplex er Settling Time
The maximum time required to reach a specified error band around the input value when switching channels.

Offset Error
The error by which the transfer function fails to pass through the origin. This is usually adjustable to zero

Quantization Error
Quantization error is defined as the basic uncertainty associated with digitizing an analog signal, due to the finite resolution of an A/D converter. An ideal converter has a maximum quantiration error of ± 1/2 LSB.

Quasi-Differential
Like true differential Operation (see Differential Inputs) in that measurement is made of the difference between an input and a return line. Unlike true differential, however, in that measurement is not made at one instant in time, but rather throughout the Variation of the conversion.

Relative Accuracy
This is defined us the input to output error as a fraction of full scale with gain and offset errors adjusted to zero. Relative accuracy is dependent on linearity.

Resolution

The resolution of an A/D converter is defined as the smallest analog change that can be dis tinguished. Resolution is the analog value of the least significant bit.

$$\text{Resolution} = \frac{\text{Full scale}}{\text{Least significan t bit}}$$

For example. if a system requires a weight measurement range of 2540 Ib, measured to the nearest 3 lb.

$$\text{Resolution} = \frac{2540}{3} = 847 \text{ code combinations}$$

The closest Standard A/D converter resolution available is IO-bits binary. A binary resolution of IO-bits selected. The new resolution for this channel is recalculated for 10 bits.

$$1 \text{ LSB (least significant bit)} = \frac{\text{Full scale range}}{2^n} \frac{2540}{1024} = 2.5 \text{ lb}$$

Sample-and- Hold

In order to ensure that input voltage does not change during a conversion, a sample-and-hold is required. If the change during a conversion cycle is less than 1/2 LSB, then a Sample-and-hold circuit is not required.

Example

Conversion Speed = 20 μs
Full Scale Input Range (FSR), where $\omega_{max} = 2\pi$ (BW)
Converter Resolution = 10 bits
LSB Value = .01 V/bit
1/2 LSB = 0.005 V

Maximum slew = 0.005 V/20 μsec = 250 μV/μsec = 250 V/sec
(Rate required for no Sample-and-hold)

for ein = 1/2 (FSR) sin ω t

then de/dt = (1/2)ω (FSR) cos ω t

$\therefore$ |de/dt max = (1/2)ω_{max} (FSR) = (BW) (FSR), where $\omega_{max} = 2\pi$ (BW)

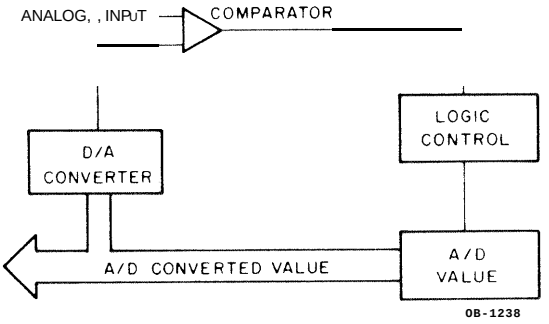
or 250 V/sec = π (BW) (FSR)

BW = 250 V/sec /π (10.24 V) $\doteq$ 7.77 Hz

Slew Rate

The capability of the output of an analog circuit to change its voltage in a given period of time. If the slew rate is 7 V/μsec, the analog circuit output will change seven volts in one μsec.

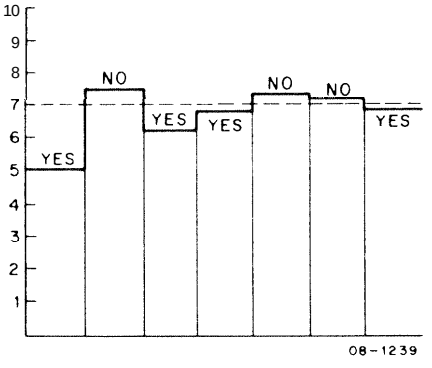
Successive Approximation
A method that is used to transform the analog signal to a digital number.



An analog signal is compared to a logic generated signal. The logic always supplies a half range signal initially. For example, the full scale input to an A/D converter system is 10 V and the input to the system is 7 V.

Try*	New Logic Voltage	Is the Input Greater Than New Voitage	A/D Buffer Bits	Decision	A/D Register Value
5 V	5 V	Yes	6	Add +5 = +5	*1000000*
2.5 v	5 + 2.5 V	NO	5	Do nothing	*1000000*
1.25 v	5 + 1.25 v	Yes	4	Add 1.25 = 6.25	1010000
.625 v	6.25 + .625 V	Yes	3	Add .625 = 6.875	1011000
.3125 v	6.875 + .3125 V	NO	2	Do nothing	1011000
.15625 V	6.875 + .1562 V	NO	1	Do nothing	1011000
.078125 v	6.875 + .078125 V	Yes	0	Add .078175	1011001

*This is a 7-bit A/D
1011001 ≈ 7 V in 10 V full scale range.



Throughput Speed

The Nyquist sampling theorem states that a minimum of tuo samples per cycle are required to completely recover continuous Signals in a noiseless environment. In typical instrumentation systems noise does exist and from 5–10 samples per cycle are required.

For appiications with dc and very low frequency signals, sample rate is usually a sub-multiple of the powerline frequency to provide essentially infinite rejection of these frequencies.

The minimum sampling speed required is the number of samples per cycle multiplied by the highest frequency component of the data. For time multiplexed Systems. the speed requirement of the A/D converter is dependent on system throughput speed. System conversion speed is determined from data bandwidth, the number of channels, and the sampling factor by:

System throughput = (N) (n) (B.W.) samples/second
n = number of channels

where N = number of samples/cycle (sampling factor)
B.W. = largest bandwidth of any channel

Example

Channel 1 bandwidth 100 Hz
Channel 2 bandwidth 200 Hz
Channel 3 bandwidth '250 Hz

throughput = 10 **X** 3 (250) = 7500 sample/second

N = IO
n = 3
BW = 250 Hz

The A/D throughput is comprised of the following:

Multiplexer settling time
Sample & Hold settling time
A /D conversion speed
A/D recovery time
Computer acquisition time (Software)

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ADV11-A, KWV11-A, AAV11-A,
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