PART 8

DISKS

CHAPTER 11
RK8-E DISK DRIVE CONTROLLER

SECTION 1 INTRODUCTION

11.1 PURPOSE

The RK8-E (Figure 11-1) provides the interface between the PDP-8/E OMNIBUS and the RK05 Disk Drive. As a part of this function the RK8-E

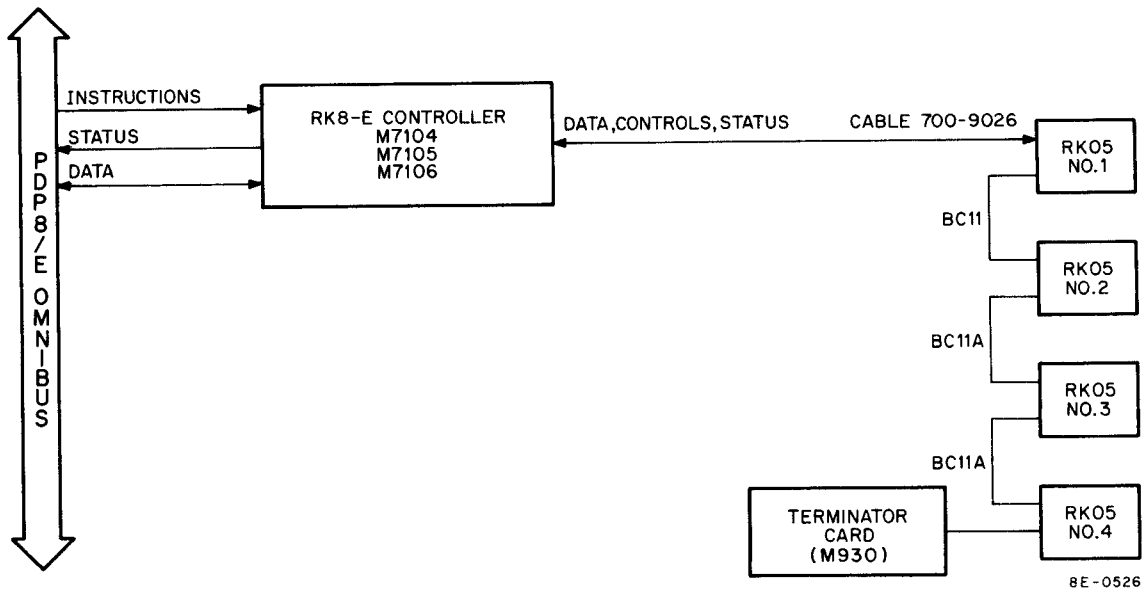

Figure 11-1 RK8-E Controller and RK05 Disk Drive System Block Diagram

a. Decodes programmed IOT instructions.

b. Accepts and stores current address, command, and extended memory address words.

c. Selects the designated RK05 and starts the designated operation.

d. Jointly (with the selected RK05) locates the disk address (track, sector, and surface).

e. Generates interrupts and skips for status checking operations.

f. Generates break requests to initiate single cycle data breaks (data transfers to or from memory).

g. Buffers the input/output data and performs related conversions (serial to parallel and parallel to serial).

h. Performs housekeeping chores for single cycle data break data transfers (i.e., increments Current Address Register and provides sequential memory addresses).

i. Counts bits and words in a transfer to determine when to end a data transfer.

j. Generates and checks CRC (parity) for each sector.

k. Provides flags to indicate current conditions and error status.

l. Provides logic to aid in the maintenance of the RK8-E and RK05.

11.2 PHYSICAL DESCRIPTION

The RK8-E consists of the following quad modules, which are inserted into the OMNIBUS and used to control up to 4 (maximum) RK05 Disk Drives.

- M7104, RK8-E Data Buffer Register and Status Module
- M7105, RK8-E Major Registers Module
- M7106, RK8-E Control Module

The RK8-E modules are inserted into the OMNIBUS and connected together with H851 Top Connectors. The RK8-E is connected to the RK05 Disk Drives by a 7009026 cable.

11.2.1 RK05 Disk Drive

The RK05 Disk Drive contains the drive electronics and mechanism for accepting and releasing the disk, positioning the read/write heads, and reading and writing data from the RK8-E control. The drive contains a removable disk cartridge, control logic, and a power supply. No power is supplied to the RK05 by the RK8-E, and the RK05 supplies no power to the RK8-E. Table 11-1 lists the RK05 Disk Drive specifications.

NOTE

The specifications in Table 11-1 apply to the RK05 when it is used with the RK8-E and a 16-sector cartridge. The RK05 may be used in other systems with other controllers and sector formats.

11.3 RECORDING METHODS AND FORMATS

This section describes the recording methods and the format used to write data on and read data from the RK05 Disk Drives.

Table 11-1

RK05 Disk Drive Specifications

Characteristic	Specification
Cylinder, Track, and Sector	
Cylinder Density	200 CPI
Cylinders/Drive	203
Tracks/Cylinder	2
Sectors/Track	16
Sectors/Cylinder	32
Bit Density and Storage	
Bit Density	2200 BPI
Bits/Cylinder	120,000
Bits/Sector	3750
Bits/Drive	24 million
Data Word Storage	
Words/Sector	400_8 or 256_{10}
Words/Track	$10{,}000_8$ or 4096_{10}
Words/Cylinder	20,000 or 8192_{10}
Words/Disk	1616K
Transfer Rate	
Word Transfer	8.32 usec
Bit Transfer Rate	1440 kHz
Recording Method	Double Frequency

11.3.1 Double Frequency Recording Method

The RK8-E uses the double frequency recording method. During a write operation, the RK8-E control generates timing pulses called Write Data Clock pulses (Figure 11-2). The time between the pulses is called a bit cell (space for writing data). A pulse within the bit cell represents a data 1 and the absence of a pulse represents a data 0. The clock pulse and data (0 or 1) are sent to the drive as Write Data and Clock pulses. Each pulse is recorded on the disk as a flux transition. A pulse representing a data 1 and the clock pulses cause a change in direction of current flow through the write heads and thus a change in the magnetic flux on the surface of the disk. Zero data bits do not cause a change in current flow through the write head; thus, there is no change in the magnetic flux on the surface of the disk.

During a read operation, the drive electronics separates the bit cell flux transitions and the data flux transitions. The bit cell flux transitions are sent to the RK8-E as Read Data Clock pulses and the data transitions are sent as Read Data pulses (serial bits of data).

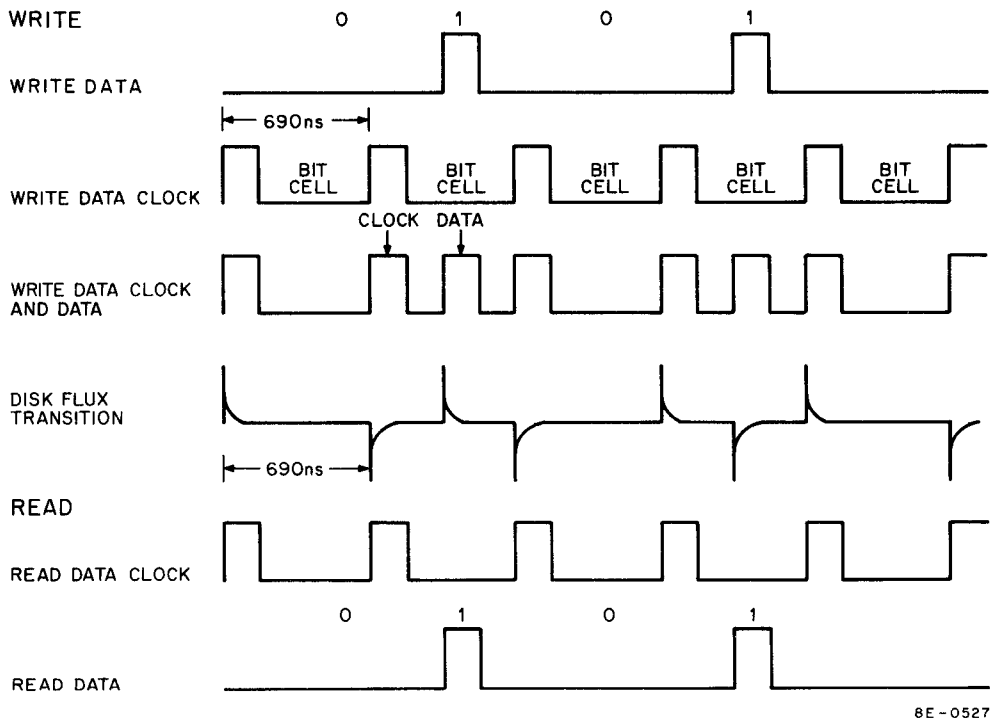

Figure 11-2 Double Frequency Recording Method

11.3.2 Disk Addressing

The surfaces of the RK05 Disk Cartridge are divided into 203 tracks and 16 sectors (Figure 11-3). Each surface has one read/write head.

A drive can be commanded to seek one of 203 cylinder addresses. The drive generates a signal and supplies it to the RK8-E when it is on the correct cylinder address. When the drive completes a seek, it is advisable to check the cylinder address to ensure the heads are positioned correctly.

The RK8-E can be commanded to read the cylinder address (HEADER) from the first cylinder it finds and check this against the cylinder address it previously sent to the disk drive. If the two addresses agree, the controller starts a data transfer; if they do not agree, an ERROR flag is set. The program must determine what to do about the ERROR flag.

A drive performing a seek can be deselected and another drive selected and commanded to seek; thus, overlapped seeks are possible.

11.3.3 Sector Format

The sector format (Figure 11-3) consists of a 140 μs PREAMBLE of zero data bits (time pulses only), a SYNC bit (data bit = 1), a 16-bit HEADER word containing the cylinder address, 256 12-bit data words, a 16-bit Cyclic Redundancy Check (CRC) character, and a 25 μs POSTAMBLE (erase delay zone).

11.3.3.1 HEADER Word – The HEADER is a 16-bit word containing 5 zero bits and a 8-bit cylinder address followed by 3 zero bits.

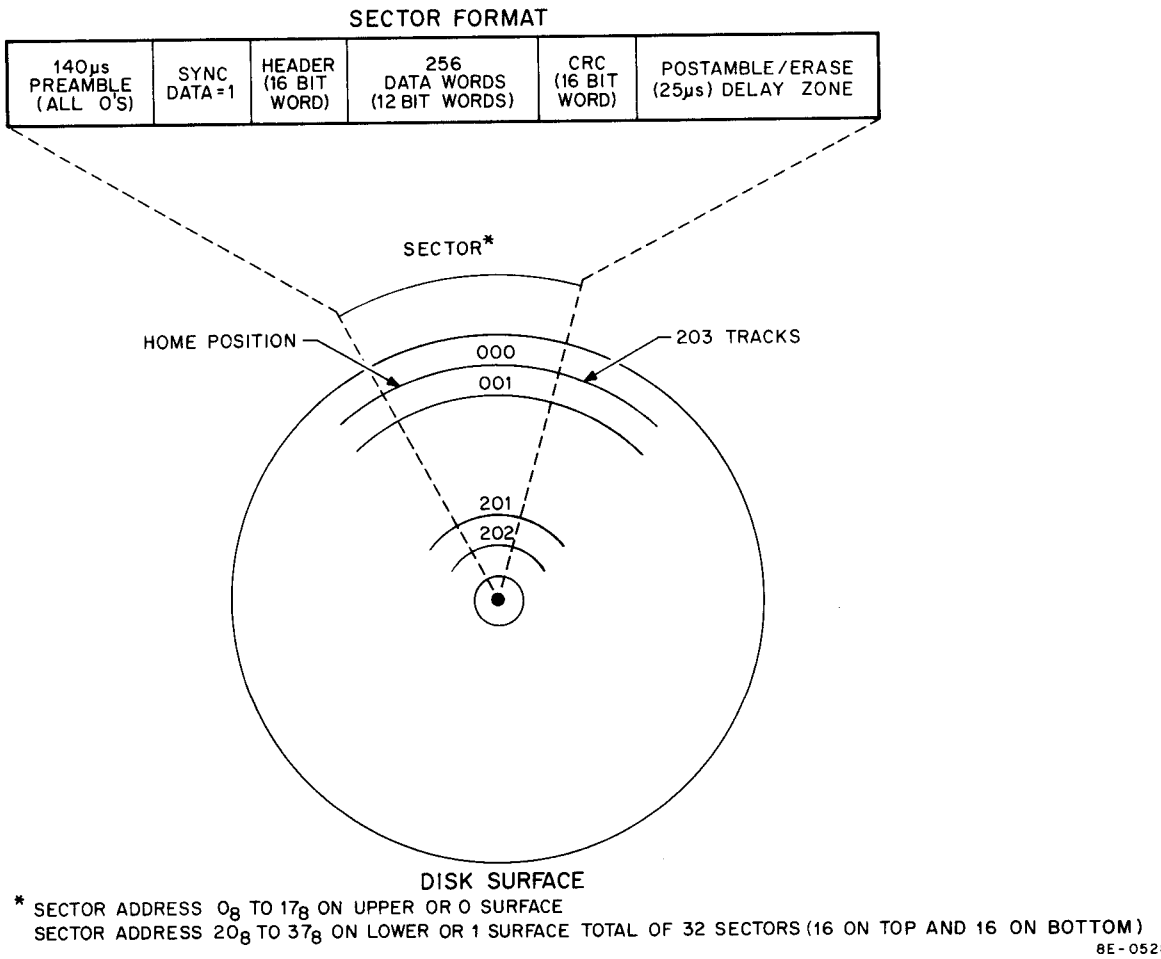

Figure 11-3 Disk Format

11.3.3.2 CRC Character – Data is recorded on the RK05 in blocks of 256 12-bit words (serial data); thus, each block contains 3072 bits of data recorded in a single string, with no separations to indicate word boundaries or record error checking bits.

A long string of data bits is susceptible to single bit errors caused by dropins, dropouts, or burst errors. Burst errors are caused by unwanted physical motion of the read/write heads. The RK8-E generates a Cyclic Redundancy Check (CRC) character to check for these errors. The CRC is a block check character that is calculated by the RK8-E during a read or write operation. The CRC character calculated during a write operation is written immediately following the data (Figure 11-3) and becomes part of the data string. The process used to calculate the block check word is such that if no errors occur, the CRC word calculated while reading data is identical to that calculated during a write operation.

To calculate a CRC word, the data block is treated as a number 3072 bits long which is divided by a polynominal ($X^{16} + X^{15} + X^2 + 1$). The hardware required to do this is a shift register with Exclusive OR gating (division being shift and subtract).

A maintenance instruction allows the program to read the CRC character written on the disk or the CRC character read from the disk.

11.3.3.3 Formatting A Cartridge – A disk cartridge is "formatted" when the cylinder address of a sector is written in the HEADER word of each sector. A special bit in the Command Register allows the program to write HEADER words in each sector (format). The program need only set the bit and write something in each sector. The RK8-E control writes the cylinder address automatically in the HEADER area (Figure 11-3) of each sector. The formatting program writes coded information in the data region of each sector and reads it back to verify that the disk is formatted correctly.

During a normal read or write operation, the disk seeks a cylinder specified by the RK8-E and reads the HEADER word of the first sector it finds after the seek is complete. This HEADER word is compared with the cylinder address specified by the RK8-E to ensure the correct cylinder has been found. The control then waits until the sector containing the address specified by the program passes under the read/write heads before reading or writing data.

11.3.3.4 Write Protect – WRITE PROTECT is turned on at the RK05 Disk Drive or by a bit in the Command Register when it is loaded by the program. WRITE PROTECT must be turned off by pressing a manual control (WT PROT) on each disk drive. If the program attempts to write on a disk that is write protected, the write operation is inhibited and an error condition is produced. WRITE PROTECT may be turned on manually at the RK05 by pressing the WT PROT switch.

11.4 MAJOR REGISTERS

The major registers of the RK8-E are in two broad categories: those that are loaded or read by user software and those that are transparent to user software. The first category includes the Command Register, Current Address Register, Disk Address Register and Status Register. The second category includes the 4-word Data Buffer Register, the CRC Register, Major State Register, Modulo 12- and Modulo 16-bit counters, and the Modulo 128- or 256-Word Count Register.

The major registers must be loaded from the AC by IOT instructions in the correct sequence before they perform any control function. The individual flip-flops in the registers are set by a 1 (true) and cleared by a 0 (false) bit from the AC. Refer to Section 3 for a list of IOT instructions and a detailed discussion of the contents of each major register.

11.4.1 Command Register

The Command Register (Figure 11-4) is loaded from the AC by IOT 6746. This IOT also clears the AC and the Status Register.

11.4.2 Current Address Register

The Current Address Register is a 12-bit register loaded from the AC with IOT 6744, which also clears the AC. This register and 3 bits of the Command Register (Figure 11-4) are combined to make up a 15-bit Memory Address Register. The contents of the CA Register and the 3 bits in the Command Register are applied to the OMNIBUS to select a memory location during a data transfer. The CA Register is incremented before each data transfer to select the next sequential memory location. The EMA bits in the Command Register are not incremented, and these bits must be changed by the program to select new memory fields. If the CA Register is incremented past the last memory location in a field, it will wrap around in the same field. The data is stored in location 000 and starts incrementing through the field again.

11.4.3 Disk Address Register

The Disk Address Register is loaded from the AC by IOT 6743, which also clears the AC and enables the contents of the Command Register to be applied to the control logic.

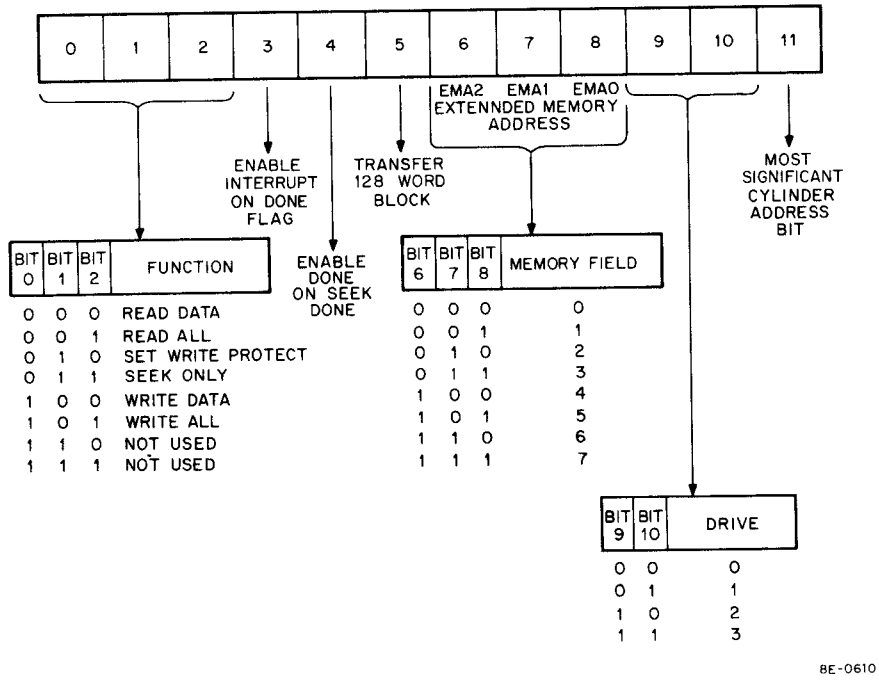

Figure 11-4 Contents of Command Register

The Disk Address Register selects a sector to be used in a data transfer. To select an individual sector, the following must be selected (Figure 11-5).

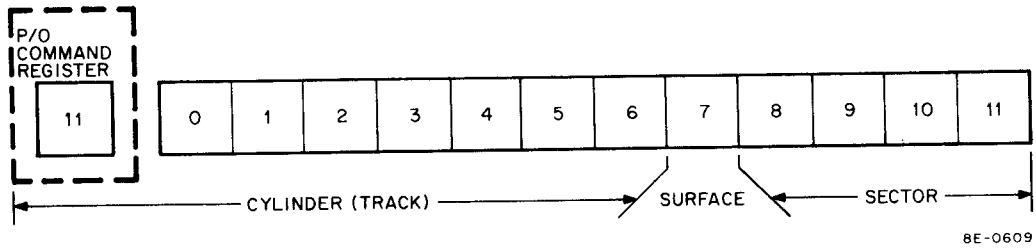

Figure 11-5 Disk Address Register

a. 1 of 203 cylinders

b. 1 of 2 surfaces

c. 1 of 16 sectors

The Disk Address Register and bit 11 in the Command Register (Figure 11-4) are combined to select a cylinder, surface, and sector. The largest valid address is 14537_8 (cylinder address 202_{10}).

11.4.4 Status Register

The Status Register (Figure 11-6) contains all the information needed for the program to evaluate the operation of the RK8-E and RK05.

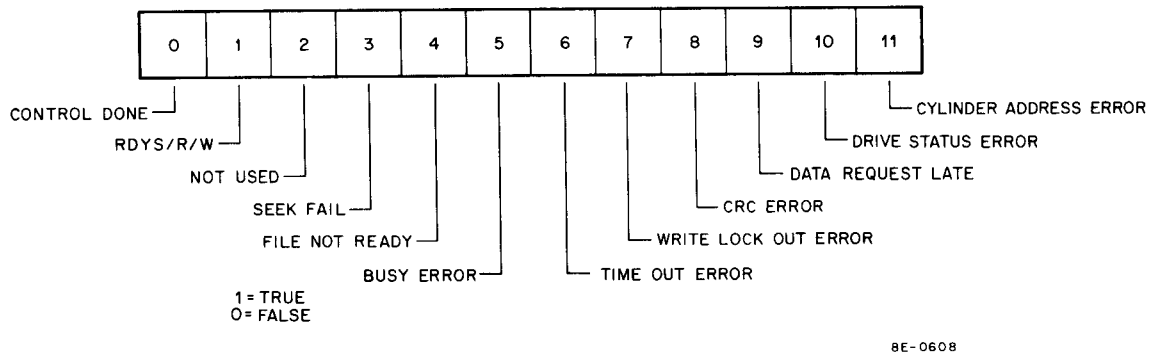

Figure 11-6 Contents of Status Register

11.4.5 Data Buffer Register

All data transfers between memory and a drive pass through the 4-word Data Buffer Register (DB1 through DB4). This 4-word register increases the latency of the RK8-E control from 6.2 μs with a single serial register and one data buffer to 22.5 μs with 4 Data Buffer Registers. Latency is defined as the maximum time the RK8-E control waits for access to the computer memory before data is lost. The numbers given above are for a memory cycle time of 1.2 μs.

During a read operation, Data Buffer 1 accepts the serial data from the drive and transfers a complete word to the last unused buffer, which is eventually removed from Data Buffer 4 and transferred to computer memory. On a write, data from computer memory enters Data Buffer 1 in parallel mode, transfers to the last unused buffer, and is shifted out to the drive as a 12-bit serial word from Data Buffer 4.

During maintenance operations, the contents of the CRC Register, Command Register, and the Surface/Sector Register (disk address) are shifted into Data Buffer 4 by the maintenance IOT for transfer to the AC or memory.

11.4.6 CRC Register

The CRC Register is a 16-bit register used to calculate the CRC character that is written onto the disk after the last data word. During a read, it calculates the CRC of the read data and does a bit-by-bit comparison with the CRC word read from the disk. It also contains the cylinder address loaded from the AC by the Load Address and GO instructions. The CRC Register does a bit-by-bit comparison of the HEADER word to confirm that the selected drive has found the correct cylinder address.

NOTE

The CRC Register and the Disk Address Register are physically the same logic with multipurposes.

11.4.7 Major State Register

The Major State Register (Table 11-2 and Figure 11-7) is the control sequencer of the RK8-E; with its associated gating, this register performs the major portion of the control functions of the RK8-E. The Major State Register is incremented from one state to another, and its decoded outputs gate signals to or from the disk and perform housekeeping tasks such as determining whether the control is in the HEADER region, data region or CRC region of the disk format.

Table 11-2

Major States

Major State	Function	Operation				
		Seek	Seek Check Read	Seek Check Write	Seek Read	Seek Write
IDLE	Control is not busy until the GO Command (DLAG) is issued and the contents of the AC are loaded into the CRC. The CRC Register contains the Cylinder/Surface Address (Disk Address)	X	X	X	X	X
STROBE	Strobe the Cylinder Address from the CRC Register to the Disk Drive and wait for the Disk Drive ADDRESS ACKNOWLEDGE signal.	X	X	X	X	X
DRIVE SEEKING	Wait for DISK READY to SEEK, READ, or WRITE from the Disk Drive to indicate the heads are positioned over the Cylinder Address.		X	X	X	X
HEADER A	Wait for the first Sector Mark, then start READ DELAY.		X	X		
HEADER B	At the end of READ DELAY turn the READ flip-flop on. Zeros are read until the SYNC bit is read at the beginning of a block of data.		X	X		
HEADER C	Read the 16-bit HEADER word and compare it with the cylinder address in the CRC Register.		X	X		
SECTOR SEEK	If the HEADER word does not equal the cylinder address set CYLINDER ADDRESS ERROR and go to IDLE state. At each sector mark compare the sector address with the Disk Sector Address lines If the addresses are equal go to the next state. If this is a write operation transfer data from the processor to the Data Buffer Register.		X	X	X	X

Table 11-2 (Cont)

Major States

Major State	Function	Operation				
		Seek	Seek Check Read	Seek Check Write	Seek Read	Seek Write
HEADER D (Read)	At the beginning of the sector start READ DELAY (85 μs). At the end of READ DELAY set the READ flip-flop. Note zeros are read until the SYNC bit is read.		X		X	
HEADER D (Write)	At the beginning of the sector start SYNC DELAY. Zeros are written during SYNC DELAY time and after SYNC DELAY times OUT (140 μs) a one SYNC bit is written.			X		X
HEADER E (Read)	Count and ignore the first 16 bits.		X		X	
HEADER E (Write)	Write the HEADER word contained in the CRC Register.			X		X
DATA STATE (Read)	Read 256 12-bit data words and a 16-bit CRC character from the Disk and compute a CRC. The 12 bit data words are transferred to the Data Buffer Register and the controller tries to keep the Data Buffer Register empty by transferring data to the processor via the single cycle data break.		X		X	
DATA STATE (Write)	Write 256 data words on the Disk Drive. The Data words are transferred.from the processor via the Single Cycle Data Break.			X		X
CRC STATE (Read)	Read the CRC from the Disk Drive and compare it with the CRC computed by the controller.		X		X	
CRC STATE (Write)	Write the computed CRC on the disk after 256 data words have been written.			X		X

Table 11-2 (Cont)

Major States

Major State	Function	Operation				
		Seek	Seek Check Read	Seek Check Write	Seek Read	Seek Write
END STATE (Read)	If the CRC character read from the Disk Drive does not equal the computed CRC, set the CRC ERROR flag and clear Read. When the Data Buffer Registers are transferred into processor memory, set the DONE flag and go to the IDLE state.		X		X	
END STATE (Write)	Start ERASE DELAY and Write zeros. At the end of ERASE DELAY (25 μs) clear WRITE, set the DONE flag and go to the IDLE state.			X		X

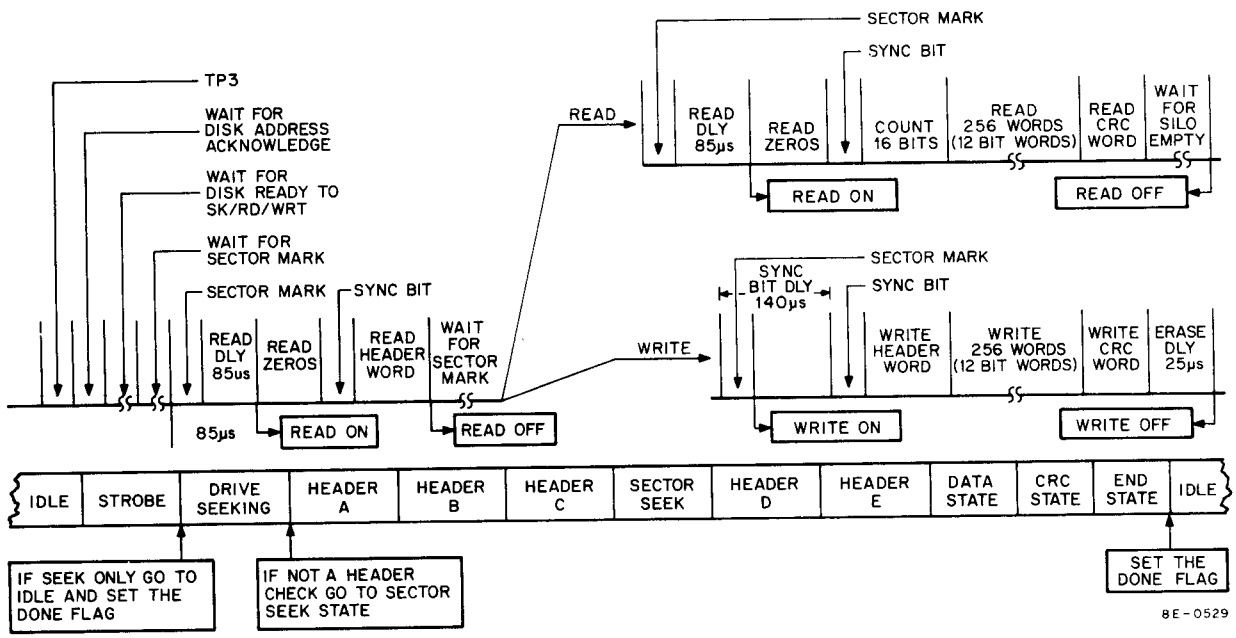

Figure 11-7 Read and Write Flow Diagram

11.4.8 Bit Counters

The Modulo 12-bit counter determines PDP-8/E data word boundaries. The Modulo 16-bit counter determines where the HEADER and CRC character are, so that the control knows when to check the HEADER and CRC characters.

11.4.9 128- or 256-Word Counter

This register counts the output of the 12-bit counter to determine when the correct number of data words (normally 256 words) have been transferred to or from the disk. When the half block bit is set in the Command Register, the 128th word stops the data transfer instead of the usual 256th word.

11.5 COMPANION DOCUMENTS

The following is a list of companion documents needed to operate and maintain the RK8-E.

a. PDP-8/E, PDP-8/F, and PDP-8/M Small Computer Handbook – DEC 1973.

b. PDP-8/E Maintenance Manual, Volumes I and II.

c. Introduction to Programming – DEC 1973 Volumes I and II.

d. DEC Engineering Drawings, M7104-0-1, M7105-0-1, and M7106-0-1.

e. RK05 Disk Drive Maintenance Manual (DEC-00-RK05-DA).

11.5.1 Software

The following programs and associated documents are used in the maintenance of the RK8-E.

a. RK8-E Diskless Control Diagnostic, MAINDEC-08-DHRKA-A-PB or D

b. RK8-E Drive Control Diagnostic, MAINDEC-08-DHRKB-A-PB or D

c. RK8-E Disk Formatter, MAINDEC-08-DHRKD-A-PB or D

d. RK8-E Data Reliability Test, MAINDEC-08-DHRKC-A-PB or D

NOTE

The MAINDEC number is followed by PB for papertape and D for Document, i.e., MAINDEC-08-DHRKA-A-PB for binary tape and MAINDEC-08-DHRKA-A-D for the diagnostic document. The latest revision of these documents and programs should be used to run RK8-E diagnostics.

SECTION 2 SITE PREPARATION, INSTALLATION, AND ACCEPTANCE TEST

The RK8-E is installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, install, checkout, or service the equipment.

11.6 SITE PREPARATION

Adequate site planning and preparation simplifies the installation process and results in a more efficient and more reliable RK8-E installation. DEC Sales Engineers or Field Service Engineers are available for counseling and consultation with the user regarding the installation.

Site planning should include a list of the actual components to be used in the installation. This list should include such items as storage cabinets, Teletype supplies, work tables, etc.

Primary requirements for installation of the RK8-E are:

a. A Teletype, Programmer's Console, and at least 4K of read/write memory must be available to run the RK8-E diagnostics.

b. Adequate space and power must be supplied for the RK05 Disk Drives (refer to Chapter 10 of the *RK05 Disk Drive Maintenance Manual* for power and space requirements).

NOTE
The RK8-E receives +5V, 3A of power from the OMNIBUS.

c. RK8-E diagnostics and documents must be available to checkout the RK8-E and RK05 (Paragraph 11.5).

d. Software to format RK05 disk cartridges must be available (Paragraph 11.5).

11.7 INSTALLATION

Perform the following steps to install the RK8-E:

Step	Procedure
1	Unpack and inspect RK05, using the *RK05 Disk Drive Maintenance Manual,* Volume 2, Paragraph 2.1, RK05 Field Installation and Acceptance Procedure.
2	Using the inventory list shipped with the equipment, verify all items have been received.
3	Ensure that PDP-8/E power is turned off.
4	Ensure correct jumpers are installed to select the device code assigned to this RK8-E. The M7104 is normally shipped with the 674X device code selected, but 675X through 677X device codes may be used (Table 11-3).
5	Install jumpers to select priority assigned to this RK8-E (Table 11-4).
6	Connect the 7009026 cable to the Berg connector on the M7106 module.
7	Insert the RK8-E modules into the OMNIBUS (Figure 11-8). Refer to Table 11-5 in Volume I of the *PDP-8/E Maintenance Manual* for module installation priority.
8	Install H851 Top Connectors between the modules (Figure 11-8).

11.8 ACCEPTANCE TEST

The following diagnostics must be run in the order shown and the specified number of passes to check the RK8-E. (Refer to the diagnostic document for instructions to run the diagnostic).

a. RK8-E Diskless Control Diagnostic, MAINDEC-08-DHRKA-A-PB (2 passes)

b. RK8-E Drive Control Diagnostic, MAINDEC-08-DHRKB-A-PB (1 pass)

c. RK8-E Formatter, MAINDEC-08-DHRKD-A-PB (1 pass)

d. RK8-E Data Reliability Test, MAINDEC-08-DHRKC-A-PB (1 pass)

Table 11-3

Device Select Jumper Installation

Octal Code	Install following Jumpers on M7104 Module
674X	W2
	W4
	W6
675X	W2
	W4
	W3
676X	W2
	W1
	W6
677X	W2
	W1
	W3

Table 11-4

RK8-E Priority Selection

Priority	Install Jumpers
Priority 0 (highest)	W1 and W4
Priority 1	W2, W3, and W5

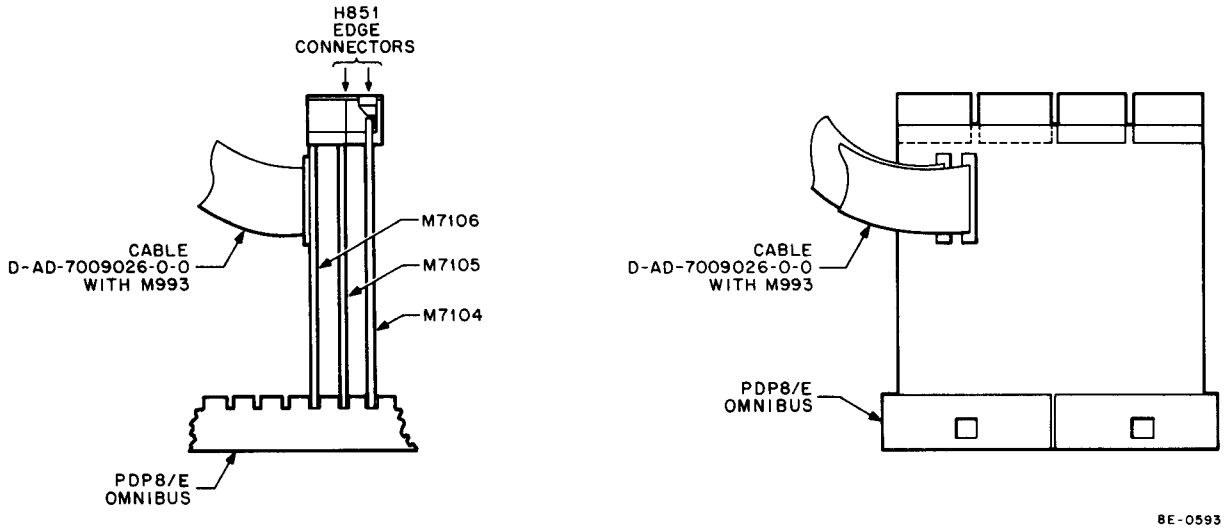

Figure 11-8 RK8-E Module Installation

11.9 RK8-E INTERFACE

One 7009026 cable is used to connect the RK8-E controller to the first RK05 Disk Drive (four maximum). Note that the RK8-E is connected to only one drive and the input to and output from the RK05 are daisy-chained to the other three disks (the connectors on all four disk drives are connected in parallel by BC11A cables). The 7009026 cable is connected from two Berg connectors on the M7106 module to slot A07, A08, B07, or B08 on RK05 Disk Drive located closest to the RK8-E (Tables 11-5 and 11-6). The RK8-E modules on the OMNIBUS are tied together by H851 Top Connectors. The signals of the pins of the top connectors are shown in Tables 11-7 through 11-10. These tables give the origin of signals on the top connectors for troubleshooting and signal monitoring.

An M930 Terminator Card must be installed in the unused interface slot of the last RK05 Disk Drive.

Table 11-5
RK8-E–RK05 Interface Cable (P2)

Connector J2 on RK8-E Pin No.	Signal	Description
A	GND	
B		
C	DSK CAP EX L	The address sent to the selected disk drive was greater than 312_8. (low=true)
E	DSK SEEK FAIL	Disk failed to seek the address specified
F	GND	
H	DSK ACKNOWLEDGE L	Disk has received and acknowledged the disk address
J	GND	
K	DSK SEC 2 L	Disk sector address bit 1 (low=1)
L	GND	
M	DSK DRIVE 3 L	Select disk drive 3 (low=true)
N	GND	
P	DSK RESTORE L	Recalibrate the selected disk drive (low=true)
R	GND	
S	DSK DRIVE 2 L	Select disk drive 2 (low=true)
T	GND	
U	DSK CYL ADD 4 L	Disk cylinder address bit 2 (low=1)
V	GND	

Table 11-5 (Cont)
RK8-E–RK05 Interface Cable (P2)

Connector J2 on RK8-E Pin No.	Signal	Description
W	DSK DRIVE 1 L	Select disk drive 1 (low=true)
X	GND	
Y	DSK CYL ADD 1 L	Disk cylinder address bit 0 (low=1)
Z	GND	
AA	DSK DRIVE 0 L	Select disk drive 0 (low=true)
BB	GND	
CC	DSK CYL ADD 32 L	Disk cylinder address bit 5 (low=1)
DD	GND	
EE	DSK RDY S/R/W L	Selected disk drive ready to read, write, or seek
FF	GND	
HH	DSK CYL ADD 128 L	Disk cylinder address bit 7 (low=1)
JJ	GND	
KK	DSK WRT CLK DATA L	Disk write clock data (low=true)
LL	GND	
MM	DSK CYL ADD 16 L	Disk cylinder address bit 4 (low=1)
NN	GND	
PP	DSK CYL ADD 64 L	Disk cylinder address 6 (low=1)
RR	GND	
SS	DSK CYL ADD 2 L	Disk cylinder address bit 1 (low=1)
TT	GND	
UU	DSK CYL ADD 8 L	Disk cylinder address bit 3 (low=1)
VV	GND	

Table 11-6
RK8-E–RK05 Interface Cable (P1)

Connector J1 on RK8-E Pin No.	Signal	Description
A	Not used	
B	Not used	
C	GND	
D	DSK DATA IN L	Serial Data from the disk drive
E	GND	
F	DSK RD CLK L	Clock pulses from the selected disk drive during a read operation
H	GND	
J	DSK WRT PROTECT L	Disk write protect (low=true). The selected disk drive does not write if this signal is true
K	GND	
L	DSK READ L	Disk read (low=true) causes the selected disk drive to read
M	GND	
N	Not used	
P	GND	
R	DSK WRT STATUS L	Disk Write Status L (low=true, Disk OK)
S	GND	
T	DSK SECTOR MK L	Disk sector mark (low=true) from the selected disk drive
U	GND	
V	DISK FILE RDY L	The selected disk drive is ready to read or write data (low=true)
W	GND	
X	DSK HEAD SEL 1	Disk head select bit; when this bit is a 1, the lower or 1 surface of the disk cartridge is selected

Table 11-6 (Cont)
RK8-E—RK05 Interface Cable (P1)

Connector J1 on RK8-E Pin No.	Signal	Description
Y	GND	
Z	DSK INDEX MK L	Disk index mark (low=true) from the selected disk drive
AA	GND	
BB	DSK WRT ERASE GATE L	Disk write erase gate (low=true)
CC	GND	
DD	DSK SEC 1 L	Disk sector address bit 0 (low=1) from the selected disk drive
EE	GND	
FF	DSK SEC 4 L	Disk address bit 2 (low=1) from the selected disk drive
HH	GND	
JJ	Not used	
KK	GND	
LL	DSK SEC 8 L	Disk sector address bit 3 (low=1) from the selected disk drive
MM	GND	
NN	Not used	
PP	GND	
RR	DSK STROBE L	Disk strobe enables the disk to receive disk address
SS	GND	
TT	Not used	
UU	GND	
VV	Not used	

Table 11-7
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	HM1	M7106	Output of the divide by 12 counter each time 12 bits are read or written
6RK3 OK H	HS1	M7104	6RK3 (DLAG) load disk address and go if RK8-E is in the IDLE state
6RK3 OK L	HS2	M7104	Same as 6RK3 H except low is true
6RK4 L	JS2	M7104	6RK4 (DLCA) load Current Address Register
6RK6 H	HR1	M7104	6RK6 (DLDC) load Command Register
6RK7 H	JC1	M7104	6RK7 (DMAN) maintenance instruction
6RK7 OK H	HN2	M7104	6RK7 (DMAN) OK asserted only at TP3 time
WRT BRK L	HH1	M7105	Write break request (use DB1 for data transfer)
READ BRK L	HL2	M7105	Read break request (use DB4 for data transfer)
B DATA 10 H	JA2	M7104	Buffered data bus bit 10 (high=true) (1)
B DATA 10 L	JP2	M7104	Buffered data bus bit 10 (low=true) (1)
B DATA 11 H	JR1	M7104	Buffered data bus bit 11 (low=true) (1)
B DATA 11 L	JH1	M7104	Buffered data bus bit 11 (low=true) (1)
BRK DIR (0) H	HP2	M7105	Controls state of MD DIR L on the OMNIBUS
BTP3 OK H	HK1	M7104	Asserted at TP3 time if the RK8-E is in the IDLE state for timing
CLR DRV CMD L	JC2	M7104	Clear commands to the selected disk drive (see DCLR instruction and Table 11-11)
CLR ALL H	HD1	M7104	Clear all logic (see DCLR instruction and Table 11-11)
CLR ALL L	JU2	M7104	Same as CLR ALL H except low=true
DRV REVO H	JD2	RK05	Disk has read an index mark
DSK CAPACITY EX L	JK1	RK05	Disk capacity exceeded, a cylinder address greater than 312_8 was sent to the disk drive
DSK FILE RDY L	HE1	RK05	Selected disk drive is ready

Table 11-7 (Cont)
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
DSK WRT STATUS	JD2	RK05	Selected disk drive is in a write status
SET IDLE PL L	JJ1	M7104	Set the IDLE state flip-flop
ENAB INT H	JB1	M7105	Enable the interrupt logic (see Table 3-2)
ENAB SEEK DONE H	JS1	M7105	Enable seek done if bit 3 in the Command Register is set
END STATE (0) H	JJ2	M7106	The RK8-E is in the END state
ERROR CLR L	JD1	M7104	Clear the ERROR flip-flop
HI RD CLK H	JM1	M7105	Maintenance clock or clock from the disk during a read
HI DATA IN H	JR2	M7105	Maintenance data or data from the disk during a read
IDLE (0) H	JN1	M7106	RK8-E is not in IDLE state when this signal is 0 (high)
IDLE (1) H	JL2	M7106	RK8-E is in IDLE state when this signal is 1 (high)
LAST WORD PL H	JN2	M7106	Output of the word counter each time 256 words are read or written
LD CMD REG H	JP1	M7105	Load Command Register asserted by 6RK6 (DLDC at TP3 time)
LO MAIN DATA H	HV2	M7105	Load main data
LO MAIN SHFT L	HP1	M7105	Shift main data
MAIN (0) H	JE1	M7105	Clear side of MAIN enable flip-flop. This signal is true when the MAIN flip-flop is cleared (normal operations)
MAIN (1) H	HA2	M7105	Set side of MAIN flip-flop. This signal is true when the MAIN flip-flop is set to enable maintenance operations
B DATA 01 H	HT2	M7104	Buffered data bus bit 1
NOT EQUAL (0) H	JF2	M7105	The cylinder address sent to the disk and the cylinder address read after seek is complete are not equal

Table 11-7 (Cont)
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
RDY S/R/W L	HU1	RK05	Selected disk drive ready to seek, read, or write
B TP2 H	HC2	M7104	Buffered time pulse 2
SECTOR SEEK (0) H	JF1	M7106	RK8-E is in sector seek state if sector seek (0) is true high
SEEK FAIL H	HU2	RK05	Selected disk drive failed to seek
MAIN PL H	HT1	M7105	See maintenance instruction and Table 11-14
DATA ENABLE (1) H	HN1	M7105	Enable gate to apply MA and EMA bits to the OMNIBUS
DATA STATE (0) H	JM2	M7106	The RK8-E is not in data state when this signal is high (0)
B DATA STATE (1) H	HL1	M7106	The RK8-E is in the data state when this signal is high (1)
DB CONT 1 (0) H	HV1	M7106	Data buffer 1 control
DB CONT 4 (1) H	HE2	M7104	Data buffer 4 control
DEVICE RK H	JA1	M7104	If device RK is high (true), the RK8-E is selected for this operation
B TP3 H	JT1	M7104	Buffered time pulse 3
DRIVE STATUS BAD H	JH2	RK05	Selected disk drive not operational (Table 11-12)
WRITE (1) H	HM2	M7106	WRITE function is (1) high when a write operation is selected
WRT CMD L	JE2	M7106	WRT command to the disk during a write operation
WT BUFF TO DATA L	HD2	M7104	Transfer DB4 to the data lines (used during maintenance operations to transfer contents of DB4 to the AC)
RK DATA 11 H	HF1	M7104	Disk data bit 11
LD DISK ADDRESS H	JB2	M7106	Load Disk Address Register when asserted by 6RK3
SHFT WRT BUFF L	HR2	M7106	Shift write buffer (DB4)
AC7 (0) H	HB1	M7104	Bit 7 from the AC

Table 11-7 (Cont)
M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
RDY S/R/W SLO H	JL1	RK05	Selected disk drive ready to seek, read, or write
BRK RQ H	HA1	M7105	Break request
B BRK RQ H	HB2	M7104	Buffered break request
MAK (0) H	HJ1	M7105	Data BRK RQST accepted (RK8-E has priority)
DATA CLK OK H	HC1	M7106	Data clock OK

Table 11-8
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	HM1	M7106	Output of divide by 12 counter each time 12 bits are read or written
6RK3 OK H	HS1	M7104	6RK3 (DLAG) load disk address and go if RK8-E is in the IDLE state
6RK3 OK L	HS2	M7104	Same as 6RK3 H except low=true
6RK4 L	JS2	M7104	6RK4 (DLCA) Load Current Address Register
6RK6 H	HR1	M7104	6RK6 (DLDC) load command address
6RK7 H	JC1	M7104	6RK7 (DMAN) maintenance
6RK7 OK H	HN2	M7104	Same as 6RK7 except it is enabled at TP3 time
WRT BRK L	HH1	M7105	Write break request (use DB1 for data transfer)
READ BRK L	HL2	M7105	Read break request (use DB4 for data transfer)
B DATA 10 H	JA2	M7104	Buffered data bus bit 10 (high=true)
B DATA 10 L	JP2	M7104	Buffered data bus bit 10 (low=true)
B DATA 11 H	JR1	M7104	Buffered data bus bit 11 (high=true)
B DATA 11 L	JH1	M7104	Buffered data bus bit 11 (low=true)
BRK DIR (0) H	HP2	M7105	Controls MD DIR L on the OMNIBUS
B TP3 OK H	HK1	M7104	Buffered time pulse 3
CLR DRIVE CMD L	JC2	M7104	Clear selected disk drive (DCLD)
CLR ALL H	HD1	M7104	Clear all logic (see DCLR instruction and Table 11-11)
CLR ALL L	JU2	M7105	Same as clear all H except low=true
ENABLE DATA (1) H	HN1	M7105	Enable gates to apply MA and EMA bits to the OMNIBUS
DATA STATE (0) H	JM2	M7106	The RK8-E is in the DATA state (data transfers are enabled)
B DATA STATE (1) H	HL1	M7106	Buffered DATA state

Table 11-8 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
DB CONT 1 (0) H	HV1	M7104	Data buffer 1 control
DB CONT 4 (1) H	HE2	M7104	Data buffer 4 control
DEVICE RK H	JA1	M7104	If device RK is high (true), the RK8-E is selected for this operation
B TP3 H	JT1	M7104	Buffered time pulse 3
DRIVE STATUS BAD H	JH2	M7105	The selected disk drive is not ready (Table 11-12 bit 10)
WRITE (1) H	HM2	M7106	The write function is selected
WRT CMD L	JE2	M7106	Write command to selected disk drive
WT BUFF TO DATA L	HD2	M7104	Transfer contents of write buffer (DB4) to the Data lines
RK DATA 11 H	HF1	M7104	Disk data bit 11 (serial data to disk)
LD DISK ADDRESS H	JB2	M7106	Load Disk Address Register when asserted by 6RK3
SHFT WRT BUFF L	HR2	M7106	Shift the Write Buffer out to the disk drive
AC7 (0) H	HB1	M7104	Bit 7 from the AC
RDY S/R/W H	JL1	M7105	Selected disk drive ready to seek, read, or write
BRK RQ H	HA1	M7105	Break request
B BRK RQ H	HB2	M7105	Buffered break request
MAK (0) H	HJ1	M7105	Data BRK RQST has been accepted (RK8-E has highest priority)
DATA CLK OK H	HC1	M7106	DATA clock OK
DRV REVO H	JK2	M7106	Disk index mark is applied to RK8-E during IDLE state
DSK CAPACITY EX L	JK1	RK05	Disk capacity exceeded, address greater than 312_8 sent to the disk drive
DSK FILE RDY L	HE1	RK05	Selected disk drive is ready (on-line)
DSK WRT STATUS L	JD2	RK05	Disk drive write status (low=true)

Table 11-8 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
SET IDLE PL L	JJ1	M7104	Set IDLE state flip-flop
ENAB INT H	JB1	M7105	Enable interrupt logic (Table 11-12)
ENAB SEEK DONE H	JS1	M7105	Enable seek done if bit 3 in Command Register is set
END STATE (0) H	JJ2	M7106	RK8-E in the END state when asserted
ERROR CLR L	JD1	M7104	Clear the ERROR flip-flop
HI RD CLK H	JM1	M7105	Main clock OR clock from the disk during a read
HI DATA IN H	JR2	M7105	Serial DATA from the disk drive during a read
IDLE (0) H	JN1	M7106	RK8-E is not in the IDLE state when this signal is high
IDLE (1) H	JL2	M7106	RK8-E is in the IDLE state when this signal is 1 (high)
LAST WORD PL H	JN2	M7106	Output of word counter each time 256 words are read or written
LD CMD REG H	JP1	M7106	Load Command Register (DLDC)
LO MAIN DATA H	HV2	M7105	Maintenance data (Table 11-14)
LO MAIN SHFT L	HP1	M7105	Maintenance shift pulse (Table 11-14)
MAIN (0) H	JE1	M7105	Maintenance command (DMAN instruction)
MAIN (1) H	HA2	M7105	Maintenance command (DMAN instruction)
B DATA 01 H	HT2	M7104	Buffered data bit 2
NOT EQUAL (0) H	JF2	M7105	The cylinder address sent to the disk and the cylinder address read after seek is complete are not equal
RDY S/R/W L	HU1	RK05	Selected disk drive ready to seek, read, or write
B TP2 H	HC2	M7104	Buffered time pulse 2
SECTOR SEEK (0) H	JF1	M7106	RK8-E is in sector seek state if sector seek (0) is true high
SEEK FAIL H	HU2	RK05	Selected disk drive failed to seek
MAIN PL H	HT1	M7105	See maintenance instruction and Table 11-14

Table 11-9
M7105 to M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	FA1	M7106	Output of divide by 12 counter each time 12 bits are read or written
6RK3 OK H	FA2	M7104	6RK3 (DLAG) load disk address and go if RK8-E is in IDLE state
B DATA 7 H	ER2	M7104	Buffered data bit 7 (high=true) (1)
B DATA 10 H	EK1	M7104	Buffered data bit 10 (high=true) (1)
B DATA 11 H	EJ1	M7104	Buffered data bit 11 (high=true) (1)
CLR DRIVE CMD L	FB2	M7104	Clear commands to the selected drive
CLR ALL L	EH1	M7104	Clear all logic (see the DCLR instruction and Table 11-11)
DATA STATE (0) H	FP1	M7106	Data state (read or write data)
B TP3 H	FJ1	M7104	Buffered time pulse 3
DRV REVO H	FC2	M7106	Disk index mark is applied to the RK8-E during IDLE state
DSK FILE RDY L	FB1	RK05	Selected disk drive is operational
DSK WRT STATUS L	FD2	RK05	Selected disk drive is in a write status (low=true)
SET IDLE PL L	FK1	M7104	Set the IDLE state flip-flop
END STATE (0) H	FD1	M7106	END state (true=0)
ERROR CLR L	FE2	M7104	Clear the ERROR flip-flop
IDLE (0) H	FR2	M7106	The RK8-E is not in the IDLE state when this signal is (0) high
IDLE (1) H	EC1	M7106	The RK8-E is in the IDLE state when this signal is (1) high
LAST WORD PL H	FE1	M7106	LAST WORD is asserted when 256 words are read or written
MAIN (0) H	FP2	M7105	Clear side of MAIN flip-flop. This signal is true when the RK8-E is not in the maintenance mode
RDY S/R/W H	ED1	M7105	Selected disk drive is ready to seek, read, or write

Table 11-9 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
DATA ENABLE (1) H	EU1	M7105	Enable gates to apply MA and EMA bits to the OMNIBUS
SECTOR SEEK (0) H	FF2	M7106	The RK8-E is in the sector seek state if SECTOR SEEK is true (high)
LAST BRK (1) H	FN2	M7105	Last break (1=true) ends data transfer operations
WRITE (1) H	FF1	M7106	The write function is selected by the program
WRT CMD L	FV2	M7106	Write command to the RK05
B TP2 H	FH2	M7104	Buffered time pulse 2
B DATA 8 H	EM1	M7104	Buffered data bus bit 8
B DATA 9 H	EL1	M7104	Buffered data bus bit 9
BRK ENABLE CLK H	FK2	M7106	Break enable clock pulse
BRK IN CLK H	FU2	M7106	Break in clock pulse
CLR CNTRS L	FS1	M7106	Clear counters asserted by CLR ALL, DATA CLR, or HEADER E during STATE ENABLE
CLR SECTOR AD L	EF1	M7105	Clear Sector Address Register
CRC 16 (1) H	EN2	M7105	CRC Register bit 16
CRC DATA H	EA1	M7106	Serial CRC data
DATA IN (0) H	FR1	M7106	Serial data from the disk during a read
RD CLK (1) H	EB1	M7105	Read clock from the disk during a read
RD SHFT DB L	FS2	M7106	Shift Data Buffer during read operations
SECTOR ADDR 01 H	EP2	M7105	Sector address bit 0 high
SHFT SURF SEC H	FU1	M7105	Shift Surface Sector Register
ENAB DATA L	EV1	M7105	Enable data to the buffers
SHFT CRC L	FN1	M7106	Shift CRC out to the disk drive
FILE RDY H	EE1	RK05	Selected disk drive is READY

Table 11-9 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
STROBE (1) H	EF2	M7106	Asserted when file is ready and GO bit is set (1)
FUNCTION 00 H	EU2	M7106	Function bit 00)
FUNCTION 01 H	EV2	M7106	) Select disk drive Function bit 01) operation, i.e., read)
FUNCTION 02 H	ET2	M7106	Function bit 02)
HALF BLOCK H	ES2	M7105	Transfer 128 words instead of 256
DATA CLK OK H	FM1	M7106	Data clock OK
LO MAIN SHFT L	FL1	M7106	Maintenance shift
DSK DRIVE 2 L	EP1	M7105	Select disk drive 2 when low (true)
DSK DRIVE 3 L	EN1	M7105	Select disk drive 3 (low=true)
DSK CYL AD 128 L	EE2	M7106	Disk cylinder address bit 7 (MSB)
DSK CYL AD 64 L	EB2	M7106	Disk cylinder address bit 6
DSK CYL AD 32 L	EJ2	M7106	Disk cylinder address bit 5
DSK CYL AD 16 L	EC2	M7106	Disk cylinder address bit 4
DSK CYL AD 8 L	ET1	M7106	Disk cylinder address bit 3
DSK CYL AD 4 L	EH2	M7106	Disk cylinder address bit 2
DSK CYL AD 2 L	EK2	M7106	Disk cylinder address bit 1
DSK CYL AD 1 L	ES1	M7106	Disk cylinder address bit 0 (LSB)
DSK CAPACITY EX L	FC1	RK05	Disk capacity exceeded, address sent to the disk greater than 312_8
HI MAIN SHIFT L	FT2	M7106	Maintenance shift pulse
B LAST BRK H	FL2	M7106	Buffered last break
LD DSK ADDRS H	EM2	M7106	Load Disk Address Register when asserted by 6RK3
RK DATA 11 H	FH1	M7105	Disk data bit 11
B TP3 OK H	FM2	M7104	Asserted during TP3 time of the IDLE state only for timing and execution of instructions

Table 11-9 (Cont)
M7105 to M7104 Top Connector Signal List

Signal	Pin No.	Origin	Description
SHFT WRT BUFF L	FJ2	M7104	Shift write buffer (DB4)
STATE ENABLE B H	FV1	M7106	Buffered STATE ENABLE
DSK RDY S/R/W L	EL2	RK05	Selected disk drive ready to seek, read, or write
DSK SEEK FAIL L	EA2	RK05	The seek operation on the selected disk drive failed
DSK DRIVE 0 L	ED2	M7105	Select disk drive 0 when low (true)
DSK DRIVE 1 L	ER1	M7105	Select disk drive 1 when low (true)

Table 11-10
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
12TH BIT OK H	FA1	M7106	Output of divide by 12 counter each time 12 bits are read or written
6RK3 OK H	FA2	M7104	6RK3 (DLAG) load disk address and go
B DATA 7 H	ER2	M7104	Buffered data bus bit 7 (high=true)
B DATA 10 H	EK1	M7104	Buffered data bus bit 10 (high=true)
B DATA 11 H	EJ1	M7104	Buffered data bus bit 11 (high=true)
CLR DRIVE CMD L	FB2	M7104	Clear commands to the selected disk drive clear all logic (see the DCLR instruction and Table 11-11)
CLR ALL L	EH1	M7104	Clear all logic on the RK8-E
DATA STATE (0) H	FP1	M7106	Data state (read or write data)
B TP3 H	FJ1	M7104	Buffered time pulse 3
DRV REVO H	FC2	M7106	Disk INDEX MARK is applied to the RK8-E during the IDLE state
DSK FILE RDY L	FB1	RK05	Selected disk drive is operational
DSK WRT STATUS L	FD2	RK05	Selected disk drive is in a write status (low=true)
SET IDLE PL L	FK1	M7104	Set the IDLE state flip-flop
END STATE (0) H	FD1	M7106	The RK8-E is in the END state
ERROR CLR L	FE2	M7104	Clear the ERROR flip-flops
IDLE (0) H	FR2	M7106	RK8-E is not in the IDLE state when this signal is high
IDLE (1) H	EC1	M7106	RK8-E is in the IDLE state when this signal is high
LAST WORD PL H	FE1	M7106	Output of the word counter each time 256 words are read and written
MAIN (0) H	FP2	M7105	Clear side of MAIN flip-flop. The RK8-E is not in the maintenance mode when this signal is high
RDY S/R/W H	ED1	RK05	Selected disk drive ready to seek, read, or write
DATE ENABLE (1) H	EU1	M7105	Enables MA and EMA bits to be applied to the OMNIBUS during a data break

Table 11-10 (Cont)
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
SECTOR SEEK (0) H	FF2	M7106	Sector seek state
LAST BRK (1)	FN2	M7105	Last break
WRITE (1) H	FF1	M7106	The Write function is selected
WRT CMD L	FV2	M7106	Write command
HI MAIN SHFT L	FT2	M7105	Maintenance shift (DMAN pulse)
B LAST BRK H	FL2	M7106	Buffered last break
LD DISK ADDRS H	EM2	M7106	Load disk address
RK DATA 11 H	FH1	M7104	Data bit 11 from the disk
B TP3 OK	FM2	M7104	Buffered time pulse 3 OK
SHFT WRT BUFF L	FJ2	M7104	Shift Write Buffer (DB4)
STATE ENAB B H	FV1	M7106	State enable
DSK RDY S/R/W L	EL2	RK05	Selected disk drive ready to seek, read, or write
DISK SEEK FAIL L	EA2	RK05	The selected disk did not complete a seek operation (Table 11-12)
DSK DRIVE 0 L	ED2	M7105	Select disk drive 0 when low (true)
DSK DRIVE 1 L	ER1	M7105	Select disk drive 1 when low (true)
DSK DRIVE 2 L	EP1	M7105	Select disk drive 2 when low (true)
DSK DRIVE 3 L	EN1	M7105	Select disk drive 3 when low (true)
DSK CYL AD 128 L	EE2	M7106	Disk cylinder address bit 7
DSK CYL AD 64 L	EB2	M7106	Disk cylinder address bit 6
DSK CYL AD 32 L	EJ2	M7106	Disk cylinder address bit 5
DSK CYL AD 16 L	EC2	M7106	Disk cylinder address bit 4
DSK CYL AD 8 L	ET1	M7106	Disk cylinder address bit 3
DSK CYL AD 4 L	EH2	M7106	Disk cylinder address bit 2

Table 11-10 (Cont)
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
DSK CYL AD 2 L	EK2	M7106	Disk cylinder address bit 1
DSK CYL AD 1 L	ES1	M7106	Disk cylinder address bit 0
DSK CAPACITY EX L	FC1	RK05	Disk capacity exceeded, cylinder address greater than 312_8
DATA CLK OK H	FM1	M7106	Data clock OK during DATA state only
LO MAIN SHIFT L	FL1	M7105	Main shift (DMAN pulse)
B TP2 H	FH2	OMNIBUS	Buffered time pulse 2
B DATA 8 H	EM1	M7104	Buffered data bus bit 8
B DATA 9 H	EL1	M7104	Buffered data bus bit 9
BRK ENABLE CLK H	FK2	M7106	Break enable clock
BRK IN CLK H	FU2	M7106	BREAK IN clock
CLR CNTRS L	FS1	M7106	Clear counters asserted by CLR ALL, DATA CLR, or HEADER E during STATE ENABLE
CLR SECTOR AD L	EF1	M7105	Clear Sector Address Register
CRC 16 (1) H	EN2	M7105	CRC Register bit 16
CRC DATA H	EA1	M7106	Serial CRC DATA
DATA IN (0) H	FR1	M7106	DATA IN from the disk
RD CLK (1) H	EB1	M7105	Read clock from the disk
RD SHFT DB L	FS2	M7106	Shift Read Data Buffer (DL1)
SECTOR ADDR 01 H	EP2	M7105	Sector address bit 0
SHFT SURF SEC H	FU1	M7105	Shift Surface Sector Register
ENAB DATA L	EV1	M7105	Enable data to the buffers
SHFT CRC L	FN1	M7106	Shift CRC Register
FILE RDY H	EE1	RK05	Selected disk drive is READY

Table 11-10 (Cont)
M7106 Top Connector Signal List

Signal	Pin No.	Origin	Description
STROBE (1) H	EF2	M7106	Asserted when file is ready and GO bit is set (1)
FUNCTION 00 H	EU2	M7106	Function bit 00)) Select disk drive
FUNCTION 01 H	EV2	M7106	Function bit 01) operation, i.e., read
FUNCTION 02 H	ET2	M7106	Function bit 02))
HALF BLOCK H	FS2	M7106	Transfer 128 words instead of 256

11.10 SINGLE CYCLE DATA BREAK DESCRIPTION

All data transfers between the RK8-E and memory are via the single cycle data break interface. The concepts of data transfers and interrelationships of the data break interface and peripherals are explained in Chapter 10 of the *Small Computer Handbook 1973.* A detailed description of the data break interface (KD8-E) is explained in Chapter 10, Volume II of the *PDP-8/E Maintenance Manual.* The data break interface option operation is identical to the single cycle data break control logic used in the RK8-E.

11.11 INSTRUCTIONS AND STATUS BITS

The following are used to program the RK8-E.

Skip on Disk DONE or ERROR flag (DSKP)

Octal Code: 6741

Operation: Skip the next instruction if the TRANSFER DONE or ERROR flag is set.

Clear All (DCLR)

Octal Code: 6742

Operation: Transfer bits 10 and 11 from the AC to the clear logic in the RK8-E (see Table 11-11) and clear the AC.

Table 11-11
Clear Operations Using the DCLR Instruction

AC Bit 10	AC Bit 11	Operation
0	0	DCLS; clear tha AC and Status Register. This bit combination is normally used to clear program interrupts.
0	1	DCLC; clears the AC and all RK8-E control logic but does not clear the selected RK05 control logic. This bit combination is used only to simulate a power clear or if the controller does not respond to normal commands. Note this instruction stops the control even if it is rewriting a HEADER word; it should be used with care. The Status Register contains all zeroes after the DCLR instruction is executed with this bit combination in the AC.
1	0	DCLD; clears the AC and recalibrates the selected drive by forcing it to cylinder 000 (home position). This bit combination is used to recover from cylinder address errors and select errors.
1	1	Accomplishes same operation as 0 0.

CAUTION

The following programming sequence should be used to recalibrate the selected disk drive with a DCLR instruction.

a.	DCLR with AC 0000	Clears Status Register and AC
b.	STL	Set AC LINK bit to 1
c.	RTL	Rotate AC and LINK left two. One in the LINK goes to AC bit 10 position
d.	DCLR with AC 0010	The selected drive is recalibrated as explained in Table 11-11
e.	DSKP	The program skips an instruction when the TRANSFER DONE flag is set when the read/write heads are at the cylinder 000
f.	JMP-1	
g.	DCLR with AC 0000	Clears Status Register and the AC
h.	DSKP	Skip on TRANSFER DONE
i.	JMP-1	
j.		Recalibrate procedure is finished. Read/write heads are at cylinder 000 (home position) and the AC is cleared

Load Address and GO (DLAG)

Octal Code: 6743

Operation: Transfer the contents of the AC to the Disk Address Register, clear the AC, and enable the command in the Command Register to be executed. The Disk Address Register specifies one of 16 sectors, one of 2 surfaces, and one of 203 cylinders. The AC must be loaded with the disk address before this instruction is executed. In a normal read or write operation, the following occurs:

a. The selected drive seeks the track specified by AC bits 0 through 6 and bit 11 in the Command Register.

b. When the selected drive signals it has completed a SEEK, the HEADER word is checked on the first sector to pass under the read/write heads.

c. If the track specified checks with the HEADER word (read/write heads are on the right cylinder), the control waits for the next sector pulse.

d. The control reads the sector address of each sector passing under the read/write heads and when the correct sector is found a read or write operation is performed.

Load Current Address (DLCA)

Octal Code: 6744

Operation: Transfer the contents of the AC to the Current Address Register and clear the AC. The contents of the Current Address Register along with the EMA bits in the Command Register are applied to the OMNIBUS MA and EMA lines to select a location in memory for a data transfer. Note that the AC must be loaded with the address of the first memory location used in a data transfer.

Read Status Register (DRST)

Octal Code: 6745

Operation: Clear the AC and transfer the contents of the Status Register to the AC (Table 11-12).

Table 11-12
Contents of Status Register

Bit	Indication
0	TRANSFER DONE is set (1). a. At the end of a data transfer b. When an ERROR occurs while the controller is executing an operation c. When the selected drive completes a seek only operation d. When the selected drive completes a recalibrate operation if bit 4 in the Command Register is set **NOTE** **The TRANSFER DONE flag causes a program to interrupt if bit 3 in the Command Register is set.**
1	RDYS/R/W indicates the selected disk drive heads are in motion and the selected drive is RDY to SK, RD, or WR.
2	Not used.
3	SEEK FAIL is set (1) to indicate the selected drive failed to seek a cylinder address specified by the program. This bit is set by DSK SEEK FAIL L from the selected drive. The recalibrate operation must be performed to clear bit 3. If the DLAG instruction is executed by the program and bit 3 is set (1) the ERROR flag sets.
4	FILE NOT READY indicates the selected drive is not ready or inoperative. This bit is set (1) if DSK FILE DRY L from the selected drive is high. If the DLAG instruction is executed by the program, the ERROR flag sets if bit 4 is set (1). To clear bit 4, some action must be taken by the operator, i.e., power up the selected disk drive.

Table 11-12 (Cont)
Contents of Status Register

Bit	Indication
5	CONTROL BUSY ERROR is set (1) if the program executes the DLAG, DLCA, or DLDC instructions while the control is BUSY (IDLE is cleared). If a CONTROL BUSY ERROR occurs, the current operation is completed and the TRANSFER DONE flag sets at the end of the operation. This error occurs most often when programs are debugged, and requires rewriting of the program to eliminate the error. **CAUTION** **IOT DCLR with AC bit 11 should not be used to clear a CONTROL BUSY ERROR. If the DCLR instruction is issued by the program, the operation is aborted even if the program is writing a HEADER word.**
6	TIME OUT ERROR is set (1) if the control has been busy for more than 280 ms. If TIME OUT ERROR sets, the TRANSFER DONE flag sets. TIME OUT ERROR indicates a hardware problem and can be cleared by the DCLR instruction.
7	WRITE LOCK ERROR indicates the program tried to write on a write-protected disk drive. To write on a disk drive that has been write protected, the operator must manually clear the write lock protect by pressing the WT PROT switch on the drive which produced the error.
8	CRC ERROR is set (1) if the CRC character read from the disk does not agree with the CRC character calculated by the RK8-E as data is read from the disk. CRC ERROR sets the TRANSFER DONE flag immediately and the operation is stopped. If a CRC ERROR occurs, a new read operation must be initiated to reread the data; if this is not successful, the data must be rewritten.
9	DATA REQUEST LATE is set (1) if the processor does not respond to a break request within 22.5 μs. The 4-word Data Buffer Register is filled within 22.5 μs, and if one of the registers is not freed within this time period, a DATA REQUEST LATE ERROR occurs. DATA REQUEST LATE sets the TRANSFER DONE FLAG and stops the operation. A new operation must be initiated to transfer the same data. Note that if the Data Buffer Register is full during a read operation, the processor must grant a BRK RQST within 6.5 μs after the register is filled; or if the Data Buffer Register is empty during a write operation, the processor must grant a BRK RQST within 6.5 μs after the register is emptied. Either one of these conditions causes a DATA REQUEST LATE error. If the register is half-filled or half-empty, the latency would be 13 μs.
10	DRIVE STATUS ERROR is set (1) when the DLAG instruction is executed by the program if: a. The DRIVE NOT READY for one of the following reasons: 1. Power is not turned on 2. The drive does not exist (incorrect address) 3. The selected drive does not have a cartridge installed 4. The door on the selected drive is not closed (interlock open)

Table 11-12 (Cont)
Contents of Status Register

Bit	Indication
	5. Disk is not up to speed (disk rotation less than 1500 rpm) 6. Load switch on the selected disk drive is in the RUN position. The TRANSFER DONE flag is not set as a result of DRIVE NOT READY b. The WRITE CHECK ERROR is set to indicate the drive has one of the following error conditions. 1. Erase or write current without a WRITE GATE 2. The head position transducer lamp is inoperative. If WRITE CHECK ERROR is set, the WT PROT switch on the selected drive must be depressed to remove the error. WRITE CHECK ERROR does not set the TRANSFER DONE flag. 3. If disk capacity is exceeded (cylinder address greater than 312_8 was sent to the selected drive), the program must select a new disk address that is less than 312_8. The TRANSFER DONE flag is set if the disk capacity is exceeded. 4. If a SEEK FAILURE occurs in the drive, this indicates a seek was not completed because of some disk drive malfunction. If the control is busy at the time a SEEK FAILURE occurs, the TRANSFER DONE flag is set and the disk drive must be recalibrated using the recalibrate IOT DCLR with AC = 10.
11	CYLINDER ADDRESS ERROR is set (1) if the HEADER word of a sector does not agree with the cylinder address sent to the drive (either the HEADER word was read wrong or the read/write heads were positioned to the wrong address). The TRANSFER DONE flag is set and the HEADER word is retained in the CRC Register. The selected drive should be recalibrated using the DCLR instruction (AC = 0010), and the disk drive should be addressed again using the DLAG instruction. The cylinder address in the CRC Register is transferred to the AC by the maintenance instruction for the program to compare the disk address with the cylinder address requested by the program (refer to the 6747 maintenance IOT).

Load Command Register (DLDC)

Octal Code: 6746

Operation: Transfer the contents of the AC to the Command Register and clear the AC and Status Register. Note the AC must be loaded with information to be transferred to the Command Register (Table 11-13 and Figure 11-4) before this instruction is executed. Each of the functions selected by the Command Register are discussed in detail in Paragraph 11.11.1.

Table 11-13
Command Functions

Bit	Function
0,1,2	Bits 0, 1, and 2 of the Command Register are decoded and used to select disk operations as follows:

Bit 0	Bit 1	Bit 2	
0	0	0	Read Data – Seek disk address, check the HEADER, and read one sector.
0	0	1	Read All – Seek disk address, do not check the HEADER, and read one sector.
0	1	0	Write protect the selected drive.
0	1	1	Seek disk address, and if bit 4 is 1, set the TRANSFER DONE flag when seek is completed.
1	0	0	Write Data – Seek disk address, check HEADER, and write one sector.
1	0	1	Write all, seek disk address, do not check the HEADER, and write one sector.
1	1	0	Not used
1	1	1	Not used

3	If bit 3 is a 1, enable interrupt on ERROR flag or TRANSFER DONE.
4	If bit 4 is 1, set TRANSFER DONE flag when seek is complete.
5	If bit 5 is a 1, the controller writes or reads 128 words in a sector instead of 256. The TRANSFER DONE flag is set at the end of a sector and the last 128 words of the sector contains all zeroes.
6,7,8	Bits 6, 7, and 8 are used to address extended memory as follows:

Bit 6 (EMA2)	Bit 7 (EMA1)	Bit 8 (EMA0)	
0	0	0	Field 0
0	0	1	Field 1
0	1	0	Field 2
0	1	1	Field 3
1	0	0	Field 4
1	0	1	Field 5
1	1	0	Field 6
1	1	1	Field 7

Table 11-13 (Cont)
Command Functions

Bit	Function
	These bits are *not* incremented and the program must reload the Command Register to select a new memory field when the Current Address Register overflows (reads all zeroes).
9,10	Bits 9 and 10 are used to select a disk drive as follows: **Bit 9** **Bit 10** 0 0 Drive 0 0 1 Drive 1 1 0 Drive 2 1 1 Drive 3
11	Bit 11 is the extended cylinder address bit (Figure 11-15). It is added to the 7-bit Cylinder Address Register to allow the program to address cylinders 00_8 to 312_8. Note an address greater than 312_8 causes an ADDRESS ERROR.

Maintenance IOT (DMAN)

Octal Code: 6747

Operation: Transfers the contents of the AC to the RK8-E maintenance control logic. The maintenance operation performed is determined by contents of the AC (Table 11-14); therefore, the AC must be loaded before this instruction is executed. Table 11-14 gives the purpose of each bit, and the operations are discussed in detail in Paragraph 11.11.2.

11.11.1 Command Functions

When the Command Register is loaded by a DLDC instruction, the operation to be performed by the RK8-E is determined by bits 0, 1, and 2 from the AC. The following paragraphs explain each of these functions. A flow diagram illustrating all RK8-E operations is shown in Paragraph 11.15, Figure 11-15.

11.11.1.1 Read Data – A normal read operation (Table 11-13) is initiated when all zeroes (000) are transferred from AC0–AC2 to the Command Register by a DLDC instruction. The RK8-E and RK05 must interact to SEEK (find the correct cylinder), check the HEADER (find the correct surface), and read serial data from the disk drive. The serial data from the disk drive is read into Data Buffer 1 and transferred to the last empty buffer as a 12-bit parallel word. The parallel words are eventually moved into Data Buffer 4 and transferred to memory via the single cycle data break.

The RK8-E tries to keep the Data Buffer Register empty, by initiating single cycle data breaks, so that a register will be empty when each new word is received from the disk drive. If data is read from the disk drive while the Data Buffer Register is full, the DATA REQUEST LATE flag is set and the sector must be read again.

A read operation continues until 256 words have been read from the disk drive and the TRANSFER DONE flag sets. If the half block bit is set, 256 words are read, but only the first 128 words are data words. The second 128 words are all zeroes and are not transferred to memory.

Table 11-14
Maintenance Functions

Bit	Function
0	Enables maintenance logic and disables IOT DLAG (GO).
1	Enable a shift to lower buffer (DB4) by setting the DB4 control flip-flop.
2	Check CRC Register
3	Check Command Register
4	Check Surface and Sector Register
5	Check Data Buffer
6	Check Data Break Request
7	Transfer contents of Data Buffer 4 to the AC
8	Not used
9	Not used
10	Maintenance data bit
11	Not used

11.11.1.2 Read All – Read All is initiated when 001 is transferred from AC0–AC2 to the Command Register by the DLDC instruction. Read All is identical to a normal read operation except the HEADERs are not checked. This allows a disk cartridge that has been formatted to be checked by the program to verify the HEADERs have been written on the cartridge correctly.

11.11.1.3 Write Data – Write Data (Table 11-13) is initiated when a 100 is transferred from AC0–AC2 to the Command Register by a DLDC instruction. The RK8-E and RK05 must interact to SEEK (find the correct cylinder), check the HEADER (find the correct sector), and write data transferred from memory to Data Buffer 1 as a 12-bit parallel word via the single cycle data break. The 12-bit word is transferred from Data Buffer 1 to the last empty buffer. The 12-bit word is eventually transferred into Data Buffer 4 where it is shifted out to the disk drive as a 12-bit serial word to be written on the disk cartridge.

The RK8-E tries to keep the Data Buffer Register full during a write operation so that there will always be a word available when the drive is ready to write. If the disk drive calls for data when the Data Buffer Register is empty, the DATA REQUEST LATE flag is set and the sector must be rewritten.

The write operation continues until 256 words have been written on the cartridge and the TRANSFER DONE flag sets. If the half block bit is set, 128 words of data from memory are written on the disk cartridge and 128 words of all zeroes are written on the remainder of the sector.

11.11.1.4 Write All – Write All (Table 11-13) is initiated when a 101 is transferred from AC0–AC2 to the Command Register by the DLDC instruction. This function is identical to the write function except the HEADERS are not checked by the RK8-E. Write All is used to format a new disk cartridge. To format a disk cartridge, a HEADER word must be written at the beginning of each sector. The word to be written is determined by the program (Paragraph 11.12.1).

11.11.1.5 Write Protect – A 010 transferred from AC0–AC2 to the Command Register by a DLDC instruction turns on the WRITE PROTECT for the selected disk drive. If the program attempts to write on a disk drive that has WRITE PROTECT set, a WRITE LOCK ERROR occurs and stops the write operation. The only way to enable writing on a disk drive that has been write protected is to push OFF the WRT PROT OFF switch on the drive that was write protected.

11.11.1.6 Seek Only – When a 011 is transferred from AC0–AC2 to the Command Register by a DLDC instruction, the selected disk drive seeks the cylinder contained in the Cylinder Address Register but does not check the HEADER or start a read or write operation. Cylinder (2 tracks) seek electronics are self-contained in each disk drive so once the seek operation has been started a new disk drive can be selected. Thus, more than one disk drive can be doing a seek operation and the control can select another disk drive for a read or write operation. If seek only is specified and the DLAG instruction is executed by the program (this instruction starts all disk operations), the TRANSFER DONE flag is set after IOT DLAG is executed. TRANSFER DONE is set again when the seek is complete if bit 4 in the Command Register is set (1).

11.11.1.7 Interrupt Enable – The program interrupt system is enabled if bit 3 in the Command Register is set. When this bit is set (1), program interrupt is initiated if the TRANSFER DONE or ERROR flags are set.

11.11.1.8 TRANSFER DONE on SEEK COMPLETE – If bit 4 in the Command Register is set (1), the TRANSFER DONE flags set when the selected drive has completed a seek operation.

NOTE

Programming precautions must be taken when using this bit because it is possible to select another drive just as the drive that was previously selected completes a seek. If this happens, the unsophisticated program thinks there is a SEEK COMPLETE on the newly selected drive (see Paragraph 11.12.5 for information on programming around this hazard).

11.11.1.9 Read or Write Half Block (128 Words) – If bit 5 in the Command Register is set, a half block (128 words) of data is specified for a data transfer instead of the usual 256 words contained in one sector. When writing, the first 128 words of a sector come from memory and the second 128 words are all zeroes. The TRANSFER DONE flag is set after a complete sector (256 words) is written. When reading, the first 128 words read from the disk cartridge are transferred to memory. The TRANSFER DONE flag is set at the end of the sector when 256 words have been read. The delay before setting the TRANSFER DONE flag during a read or write half block operation is to allow the generation and checking of a CRC character at the end of the sector.

11.11.1.10 Extended Memory Addressing – Bits 6, 7, and 8 of the Command Register are used to address extended memory (Table 11-13). The extended memory address bits (EMA0–EMA2) are not incremented; thus, the Command Register must be reloaded to select a new memory field. If the Current Address Register overflows, the data is wrapped around in the same field. During a write operation, if data has already been written in those locations it will be written over; also the data read from memory during a write operation is duplicated (reread).

11.11.1.11 Unit Select – Bits 9 and 10 of the Command Register are decoded to select one of four disk drives (Table 11-13). Signals to and from a disk drive are inhibited except when the drive is selected.

11.11.1.12 Extended Cylinder Address – Bit 11 of the Command Register is an extension of the 7-bit Cylinder/Surface/Sector Address Register (Figure 11-4). The maximum number of usable cylinders is decimal 203, designated as 00_{10} to 202_{10} or 00_8 to 312_8. When the program specifies a cylinder address greater than 312_8, the CYLINDER ADDRESS ERROR flip-flop is set.

11.11.2 Maintenance Functions

The maintenance IOT 6747 (DMAN) ANDed with the contents of the AC allows program access to the major registers in the RK8-E. The maintenance instruction transfers data to the major registers (i.e., Data Buffer Register) or reads the contents of the registers into the AC or memory. Data can also be transferred to or from memory using the maintenance IOT. A DCLC instruction (clear control) must be used when changing from read to write or write to read.

The major registers are described in Paragraph 11.4. Note that the CRC Register is a multipurpose register that contains the cylinder address loaded from the AC and the cylinder address that is written or read as a HEADER word. This register also calculates the CRC character. The CRC Register also contains the CRC character read from the disk drive to be compared with the CRC that has been calculated. When the CRC Register is used as the Cylinder Address Register, bits 1–3 and 12–16 are zeroes and bits 4–11 contains the cylinder address.

The contents of the CRC, Command, and Surface/Sector Register must be shifted into Data Buffer 4 before they can be transferred to the AC or memory. These operations are explained in the following paragraphs.

11.11.2.1 Maintenance Mode – If the DMAN instruction is executed and AC00 is a 1, the controller is in the maintenance mode, the maintenance functions are enabled, and the DLAG (GO) IOT is disabled. The maintenance control bit is cleared by the clear control IOT (DCLC).

NOTE
Maintenance functions cannot be microprogrammed.

11.11.2.2 Shift Enable – If AC bit 01 is set when IOT DMAN is executed by the program, the lower Data Buffer (DB4) control flip-flop sets to enable a shift to the lower buffer.

11.11.2.3 Check CRC Register – When AC bit 02 is a 1 and the DMAN IOT is executed by the program, AC bit 10, the CRC Register, and Data Buffer 4 are logically connected as a 29-bit shift register that is shifted one position with each DMAN IOT. AC bit 10 shifts into the CRC and the CRC shifts into Data Buffer 4.

The program must count the bits shifted to determine when to read Data Buffer 4. AC bit 02 does not set a control bit so a clear is not necessary.

11.11.2.4 Check Command Register – When AC bit 03 is set and the DMAN IOT is executed by the program, the Command Register and Data Buffer 4 are logically connected as a 24-bit shift register that is shifted one position with each DMAN IOT. The program must count the bits shifted to determine when to read Data Buffer 4. AC bit 03 does not set a control bit so a clear is not necessary.

11.11.2.5 Check Surface/Sector Register – When AC bit 04 is 1 and the DMAN IOT is executed by the program, the surface bit, the Sector Register, and Data Buffer 4 are logically connected as a 17-bit shift register that is shifted one position with each DMAN IOT. The surface bit shifts into the Sector Register and the Sector Register shifts into Data Buffer 4.

The program must count the bits shifted to determine when to read the lower Data Buffer. AC bit 04 does not set a control bit so a clear is not necessary.

11.11.2.6 Check Data Buffer – When AC bit 05 is a 1 and the DMAN IOT is executed by the program, AC bit 10 and Data Buffer 1 are connected logically as a 13-bit shift register that is shifted one position with each DMAN IOT. In addition, the bit counter and word counter are incremented. The word counter is incremented by the overflow of the 12-bit counter.

After 12 shifts, the 12-bit counter overflows setting a control bit indicating that the upper Data Buffer 1 is full. The contents of Data Buffer 1 transfers to Data Buffer 4 which is read into memory. After 4 words if Data Buffer 4 is not read, and another bit is shifted into Data Buffer 1, the DATA REQUEST LATE ERROR flag is set. If Data Buffer 4 is read either into the AC or memory, information transfers into the buffer filling Data Buffer 4 and emptying Data Buffer 1. When the word counter overflows after 256 transfers, the TRANSFER DONE flag sets.

AC bit 05 does not directly set a control bit but its results do. A DCLC IOT should be issued before and after a sequence using AC bit 05.

11.11.2.7 Check Data Break Request – When AC bit 06 is a 1, and IOT DMAN is executed by the program, a single cycle data break request is initiated. The direction of transfer is controlled by the function bits in the Control Register. If a read is specified, the contents of Data Buffer 4 is transferred into the memory location specified by the Current Address Register and the Extended Memory Address Register. A write transfers data into Data Buffer 1. The data transfers into the buffer and the Data Buffer fills after four data break requests unless it is emptied by a read into the AC. It cannot be emptied by a read into memory if the DCLC is executed before switching from read to write or write to read. IOT DCLC clears the Data Buffer control bits so the buffer appears to be empty. AC bit 06 does set a control bit, but it is automatically cleared after the data break is completed.

11.11.2.8 Check Lower Data Buffer – When AC bit 07 is a 1 and IOT DMAN is executed by the program, the contents of Data Buffer 4 are read into the AC. AC bit 07 does not set a control bit so a clear is not necessary.

11.11.2.9 Maintenance Data – AC bit 10 is used in conjunction with other AC bits as data when the DMAN IOT is executed by the program.

11.12 PROGRAMMING SEQUENCES

11.12.1 Format A New Disk Cartridge

The RK8-E control contains the logic required to format a disk cartridge. All the program must do is address every sector on the disk and write on every sector using the Write All mode. The track address (cylinder and surface when DLAG was issued) is automatically written on the particular sector HEADER word selected by the control. The data written is not important except that the data should contain addressing information so a check can be made to determine if the RK8-E and drive found the correct sector on the correct surface and cylinder.

To write a new disk, the Command Register function bits (bits 0, 1, 2) should contain octal 5 (Write All). To read a newly formatted disk, the function bits should contain octal 1 (Read All). These function bits prevent the RK8-E from reading HEADER words and reporting HEADER errors that exist on an unformatted disk.

Sequence of instructions to format a disk:

1. Set up Current Address Register.
2. Set up Command Register 5000 for Write All, 1000 for Read All.
3. Set up first disk address and GO.
4. Wait for TRANSFER DONE flag, check for errors.
5. Set up current address again.
6. Set up second disk address and GO, etc.

11.12.2 Normal Read/Write

The programming sequence for a Write Data or Read Data mode is very similar to the sequence to format a disk. The sequence is:

1. Set up current address.
2. Set up Command Register 0000 for Read Data, 4000 for Write Data.
3. Set up required disk address and GO.
4. Wait for TRANSFER DONE flag and check for errors.

11.12.3 Bootstrap Loader

Many computers of the PDP-8 family include a clear with key start. On those machines, the clear of step 1 is not required.

1. Clear Control.
2. Load the Command Register with AC = 0000. This also clears the Status Register.
3. Load disk address and GO.
4. JMP.

Most bootstrap loaders for the RK8-E are in sector 0, surface 0, and cylinder 0; thus, with the control cleared, a two instruction bootstrap loader is all that is required.

11.12.4 Seek Only

The sequence for Seek Only (Command Register function bits equal 011) is different from Write All, Read All, Write Data or Read Data. It is necessary to put two skip or interrupt sequences in the program.

The programming sequence is:

1. Set up Command Register, 3000 for Seek Only and desired unit number.
2. Load disk address and GO.
3. Wait for TRANSFER DONE flag. TRANSFER DONE is set during a Seek Only when DISK ADDRESS ACKNOWLEDGE is received from the drive.
4. Clear Status Register DONE flag.
5. Drive is not seeking but if the TRANSFER DONE flag is to be set when the seek is complete, bit 4 of the Command Register must be a 1, issue a load Command DLDC instruction with selected drive number in AC 10—11 and AC bit 4=1.
6. Wait for TRANSFER DONE.

The alternative to steps 5 and 6 above is to check the condition of Status Register bit 1, which is 0 when the seek is complete.

11.12.5 Overlapped Seeks

Overlapped seeks make use of the seek only feature. The program starts multiple drives seeking and then periodically selects a different drive to determine if it has completed seeking. A different drive may be selected after Paragraph 11.12.4 step 3, but in general, programs operating with other program interrupt devices could be confused as to which drive actually completed a seek. For example, if bit 4 of the Command Register is a 1 (allowing seek complete to set the TRANSFER DONE flag) and multiple drives are seeking, it is possible to select a different drive just as one previously selected completes its seek. The TRANSFER DONE flag sets but the unsophisticated program incorrectly thinks the newly selected drive has completed a seek.

A program has two methods of getting around this problem.

a. Before selecting a new drive, the program changes the Command Register to make bit 4 a 0 without changing the drive number. It then changes the drive number with bit 4 equal to 1. If the new drive has completed a seek, there is no confusion as to which drive set the TRANSFER DONE flag.

b. Leave bit 4 of the Command Register set and check bit 1 of the Status Register to determine if the drive selected or the drive previously selected set the TRANSFER DONE flag. Bit 1 of the Status Register is 0 if the selected drive has completed the seek.

11.12.6 Recalibrate Selected Drive

The programming sequence for recalibrating a selected drive to cylinder 000 is similar to the sequence for Seek Only. The sequence follows:

1. Issue IOT 6742 with the AC equal to 0002.

2. Wait for TRANSFER DONE flag.

3. Clear status.

4. Drive is now seeking cylinder 000. If the TRANSFER DONE flag is to be set when the seek is complete, bit 4 of the Command Register must be set, i.e., issue DLDC instruction with AC 10—11 set to the selected drive and AC bit 4=1.

5. Wait for TRANSFER DONE.

The alternative to steps 4 and 5 is to check bit 1 of the Status Register. Bit 1 is 0 when the recalibrate seek is complete.

11.12.7 Data Transfers on Consecutive Sectors

Octal 1 or octal 4 (Read All or Write All) in the function portion of the Command Register allows a program to format a new disk cartridge by disabling the checking of headers. This feature is also used to transfer data on consecutive sectors. Assume a program is required to transfer 512 words of data on two consecutive sectors. The program should use Read Data and Write Data (octal 0 and 4 in the function portion of the Command Register) for the transfer of the first 256 words of data. When the first 256 words have been transferred and the TRANSFER DONE flag is set, there is a minimum of 100 μs for the program to set up the control for transfer to the next consecutive sector. The function portion of the Command Register should be changed to octal 1 or octal 5 (Read All or Write All), the Status Register cleared, and the next sector specified along with surface and cylinder when issuing DLAG. The control does check the header of the next sector but transfers 256 words of data. It is not necessary to change the Current Address Register, if a 512-word buffer is available in memory.

11.13 PROGRAMMING EXAMPLES

The following paragraphs provide examples to be used in programming the RK8-E Controller and the RK05 Disk Drive.

11.13.1 Write All

The programming sequence that follows could be used to write information on a disk sector in the Write All mode.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD CURENT         / desired current address AC0–11
     DLCA               / IOT 6744 load current address
     TAD DRIVE          / get drive number in AC9–11
     TAD WRTALL         / get Write All function in AC
     TAD FIELD          / get field in AC6–8
     TAD EXBIT          / get extended cylinder address bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load disk address and GO
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
     TAD K4000          / compare to expected value
     SZA CLA            / skip if status OK
ERROR, HLT              / ERROR, disk status
     JMP DONE           / to other seek, read, or write routines.

FIELD, 0000             / desired field in AC6–8
TRACK, 0000             / desired cylinder, surface, and sector
K4000, 4000             / expected status
CURENT, 0000            / any desired current address
WRTALL, 5000            / write all function AC0–2
```

11.13.2 Recalibrate

The programming sequence that follows could be used to "recalibrate" (return the read/write heads to cylinder 0) a disk drive.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD DRIVE          / get drive number in AC9–10
     DLDC               / IOT 6746 load Command Register
     CLA CLL CML RTL    / enable recalibrate AC10=1 AC11=0
     DCLR               / IOT 6742 recalibrate
     DSKP               / 6741 IOT skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     TAD K0200          / get enable set DONE bit in AC4
     TAD DRIVE          / get drive number in AC9–10
     DLDC               / IOT 6746 load Command Register
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
```

```
        TAD K4000       / compare to expected value
        SZA CLA         / skip if status OK
ERROR, HLT              / ERROR, disk status
        JMP DONE        / read routines, to other seek, write

DRIVE, 0000             / desired drive in AC9–10
K0200, 0200             / enable set DONE AC4
K4000, 4000             / expected status only DONE flag.
```

11.13.3 Seek Only

The programming sequence that follows could be used for a Seek Only operation.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
        DCLR            / IOT 6742 clear control
        TAD DRIVE       / get drive number in AC9–10
        TAD SEEK        / get seek function in AC0–2
        TAD EXBIT       / get extended cylinder address bit in AC11
        DLDC            / IOT 6746 load Command Register
        TAD TRACK       / get desired track in AC0–11
        DLAG            / IOT 6743 load disk address and GO.
        DSKP            / IOT 6741 skip on DONE or ERROR flag
        JMP .-1         / wait for flag
        TAD K0200       / get enable set DONE on seek complete in AC4
        TAD DRIVE       / get drive number in AC09 and AC10
        DLDC            / IOT 6746 load Command Register
        DSKP            / IOT 6741 skip on DONE or ERROR flag
        JMP .-1         / wait for flag
        DRST            / IOT 6745 read Status Register
        CIA             / change AC for testing
        TAD K4000       / compare to expected value
        SZA CLA         / skip if OK
ERROR, HLT              / ERROR, disk status
        JMP DONE        / seek complete, now to read or write routine
                        / or another seek routine

K0200, 0200             / enable set DONE bit (AC bit 4)
K4000, 4000             / known good or expected status
DRIVE, 0000             / desired drive in AC bits 9–10
SEEK, 3000              / seek only function in AC bits 0–2
EXBIT, 0000             / extended cylinder bit in AC bit 11
TRACK, 0000             / any desired cylinder, surface, and sector.
```

11.13.4 Overlap Seek

The programming sequence that follows could be used for an Overlap Seek operation with multiple drives (Note: four (4) drives are assumed).

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     DCA DRIVE          / start with drive 0
     TAD M4             / 4 drive counter constant
     DCA CNTRL          / set up the counter
OUT, TAD DRIVE          / get drive number pointer
     CLL RAL            / put AC10–11 in AC9–10
     AND K0006          / mask 9–10
     DLDC               / IOT 6746 load Command Register
     TAD DRIVE          / get drive number pointer
     CLL RAL            / put AC10–11 in AC9–10
     AND K0006          / mask 9–10
     TAD SEEK           / get seek function in AC0–2
     TAD EXBIT          / get extended cylinder address bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load disk address and GO.
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     ISZ DRIVE          / update drive number pointer
     JMP CNTRL          / count drives
     JMP OUT            / send next drive out
     JMP WAIT           / to drive wait routine to wait for drives

DRIVE, 0000             / drive number pointer
SEEK, 3000              / seek only function in AC0–2
EXBIT, 0000             / extended cylinder bit in AC11
K0006, 0006             / mask 9–10
M4, 7774                / minus 4 constant
CNTRL, 0                / counter
```

Routine to wait for drives doing an Overlap Seek.

```
WAIT, CLA CLL IAC       / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     DCA DRIVE          / start with drive 0
     TAD M4             / 4 drive counter constant
     DCA CNTRL          / setup drive counter
IN, TAD DRIVE           / get drive number pointer
     CLL RAL            / put AC10–11 in AC9–10
     AND K0006          / mask 9–10
     DLDC               / IOT 6746 load Command Register
```

```
RDSTA, DRST          / IOT 6745 read Status Register
     CLL RAL         / transfer AC01 to AC00
     SZA CLA         / skip if drive not busy
     JMP RDSTA       / drive still busy AC bit 1
     ISZ DRIVE       / drive completed seek
     ISZ CNTRL       / update drive counter
     JMP IN          / wait for next drive
     JMP DONE        / all drives complete. To other read, write, or
                     /seek routines

DRIVE, 0000          / drive number pointer
K0006, 0006          / mask
M4, 7774             / drive counter constant
CNTRL, 0             / counter
```

11.13.5 Write Data

The programming sequence that follows could be used to write information on a disk sector in the Write Data mode.

Example

```
BGN, CLA CLL IAC     / enable clear control AC10=0 AC11=1
     DCLR            / IOT 6742 clear control
     TAD CURENT      / desired current address AC0–11
     DLCA            / IOT 6744 load Current Address
     TAD DRIVE       / get drive number in AC9–11
     TAD WRTDAT      / get Write Data function in AC
     TAD FIELD       / get field in AC6–8
     TAD EXBIT       / get extended cylinder address bit in AC11
     DLDC            / IOT 6746 load Command Register
     TAD TRACK       / get desired track in AC0–11
     DLAG            / IOT 6743 load Disk Address and GO.
     DSKP            / IOT 6741 skip on DONE or ERROR flag
     JMP .-1         / wait for flag
     DRST            / IOT 6745 read Status Register
     CIA             / change AC for testing
     TAD K4000       / compare to expected value
     SZA CLA         / skip if status OK
ERROR, HLT           / ERROR, disk status
     JMP DONE        / to other seek, read, or write routines

FIELD, 0000          / desired field in AC6–8
TRACK, 0000          / desired cylinder, surface, and sector
K4000, 4000          / expected status
CURENT, 0000         / any desired current address
WRTDAT, 4000         / write data function AC0–2
```

11.13.6 Read All

The programming sequence that follows could be used to read information from a disk sector in the Read All mode.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD CURENT         / desired current address AC0–11
     DLCA               / IOT 6744 load current address
     TAD DRIVE          / get drive number in AC9–10
     TAD REDALL         / get Read All function in AC
     TAD FIELD          / get field in AC6–8
     TAD EXBIT          / get extended cylinder bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load disk address and GO.
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
     TAD K4000          / compare to expected value
     SZA CLA            / skip if status OK
ERROR, HLT              / ERROR, disk status
     JMP DONE           / to other seek, read, or write routines.

FIELD, 0000             / desired field in AC6–8
TRACK, 0000             / desired cylinder, surface, and sector
K4000, 4000             / expected status
CURENT, 0000            / any desired current address
REDALL, 1000            / Read All function AC0–2
```

11.13.7 Read Data

The following is an example of a programming sequence that could be used to read information from a disk sector in the Read Data mode.

Example

```
BGN, CLA CLL IAC        / enable clear control AC10=0 AC11=1
     DCLR               / IOT 6742 clear control
     TAD CURENT         / desired current address AC0–11
     DLCA               / IOT 6744 load current address
     TAD DRIVE          / get drive number in AC9–11
     TAD REDDAT         / get Read Data function in AC
     TAD FIELD          / get field in AC6–8
     TAD EXBIT          / get extended cylinder bit in AC11
     DLDC               / IOT 6746 load Command Register
     TAD TRACK          / get desired track in AC0–11
     DLAG               / IOT 6743 load Command Register
     DSKP               / IOT 6741 skip on DONE or ERROR flag
     JMP .-1            / wait for flag
     DRST               / IOT 6745 read Status Register
     CIA                / change AC for testing
```

```
        TAD K4000       / compare to expected value
        SZA CLA         / skip if status OK
ERROR,  HLT             / ERROR, disk status
        JMP DONE        / to other seek, read, or write routines.

FIELD,  0000            / desired field in AC6–8
TRACK,  0000            / desired cylinder, surface, and sector
K4000,  4000            / expected status
CURENT, 0000            / any desired current address
REDDAT, 0000            / read data function AC0–2
```

SECTION 4 THEORY OF OPERATION

This chapter contains a block diagram description (functional level) and a detailed description of the RK8-E logic. Figure 11-9 shows the signal flow between the functional groups of logic.

11.14 BLOCK DIAGRAM DESCRIPTION

The RK8-E consists of 8 major groups of logic:

- I/O Bus Interface
- Command Register
- Status Register
- Data Break Control
- Data Buffer Registers
- CRC Register
- Control Sequencer (Major States Register and Counters)
- Maintenance Logic

11.14.1 I/O Bus Interface

The I/O bus interface (Figure 11-9) provides the following:

a. A buffer for MD00–MD11 from the OMNIBUS

b. IOT decoder

c. Timing pulses for the execution of instructions and maintenance operations.

MD00–MD11 are decoded by the IOT decoder when instructions are executed by the program and generate signals to load the RK8-E registers, execute skips and interrupts, and generate timing pulses for maintenance operations. The outputs of the IOT decoder are used as control signals in other sections of the RK8-E. During the data break of a write operation, the buffered memory data bits (MD00–MD11) are applied to the Data Buffer Register for transfer to the selected disk drive. This block of logic also contains bus drivers for signals to the OMNIBUS (i.e., BRK RQST, INT RQST, SKIP, and INT I/O L) and provides a buffer for signals from the OMNIBUS (i.e., I/O PAUSE and the time pulses).

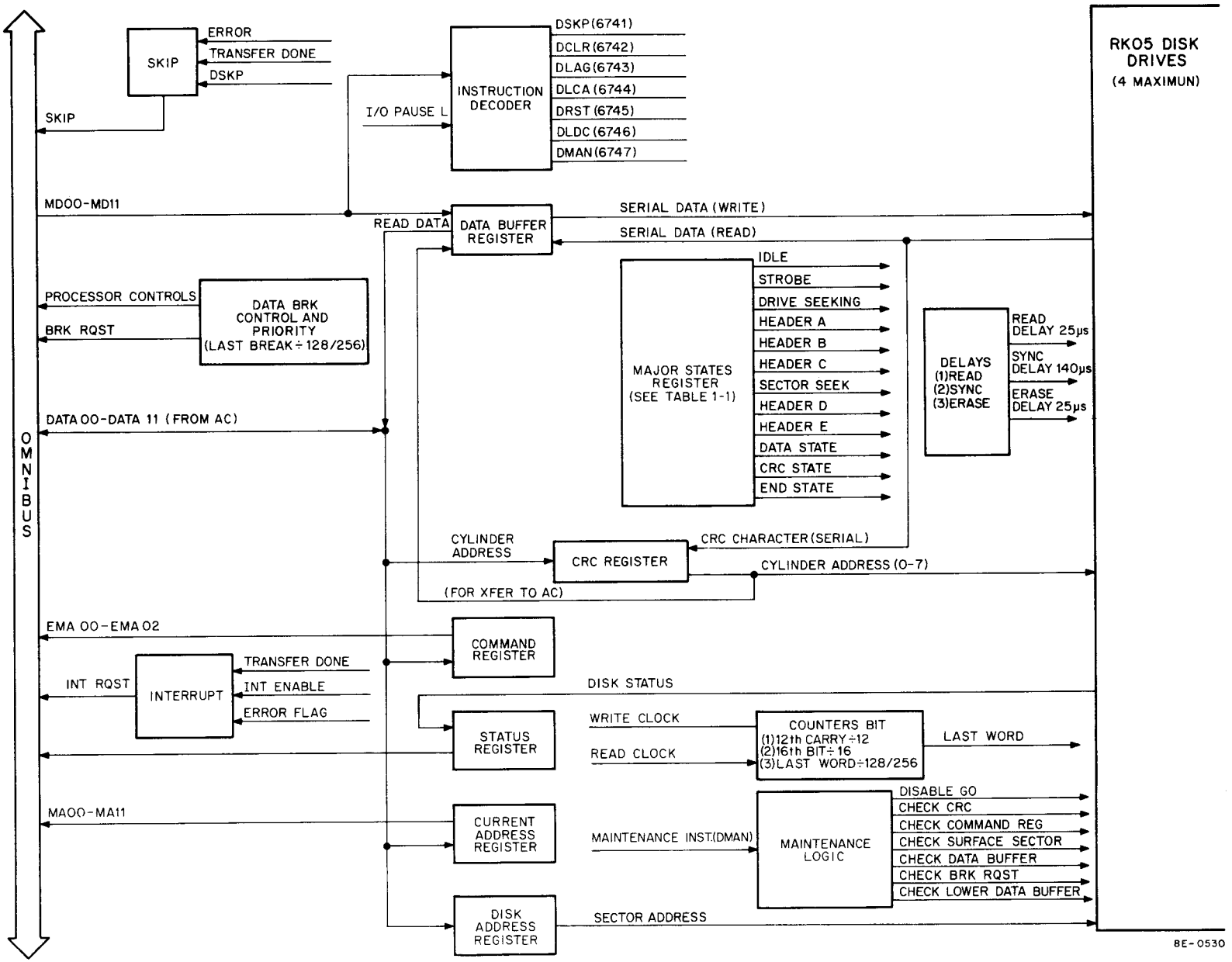

Figure 11-9 RK8-E Block Diagram

11.14.2 Command Register

The Command Register (Table 11-13) enables all disk drive operations, i.e., read, write and seek, selects a disk drive unit, selects a memory field for data transfers, enables interrupts, provides the most significant cylinder address bit, and determines the number of words to be transferred (128 or 256). The Command Register (Figure 11-9) is loaded from the AC by a DLDC instruction with DATA 0—DATA 11. Note that the contents of the Command Register are decoded and used after the program executes the DLAG instruction (load disk address and GO).

During maintenance operations, the contents of the Command Register are transferred to the AC using the DMAN instruction (Table 11-14).

11.14.3 Status Register

The Status Register (Figure 11-9) contains the current status of the selected disk drive (Table 11-12). The program determines the status of the RK8-E and disk drive by transferring the contents of the Status Register to the AC using a DRST instruction. The Status Register receives its input from the RK05 Disk Drive and the data break control logic. The DONE and ERROR flags are applied to the I/O bus interface to generate skips and interrupts if the skip or interrupt logic is enabled. Note that bit 3 in the Command Register must be set (1) to enable an interrupt when the DONE or ERROR flag sets.

11.14.4 Data Break Control Logic

The data break control logic (Figure 11-10) determines the break priority of the RK8-E, controls direction of data transfer (to or from memory), and selects a location in memory for the data transfer.

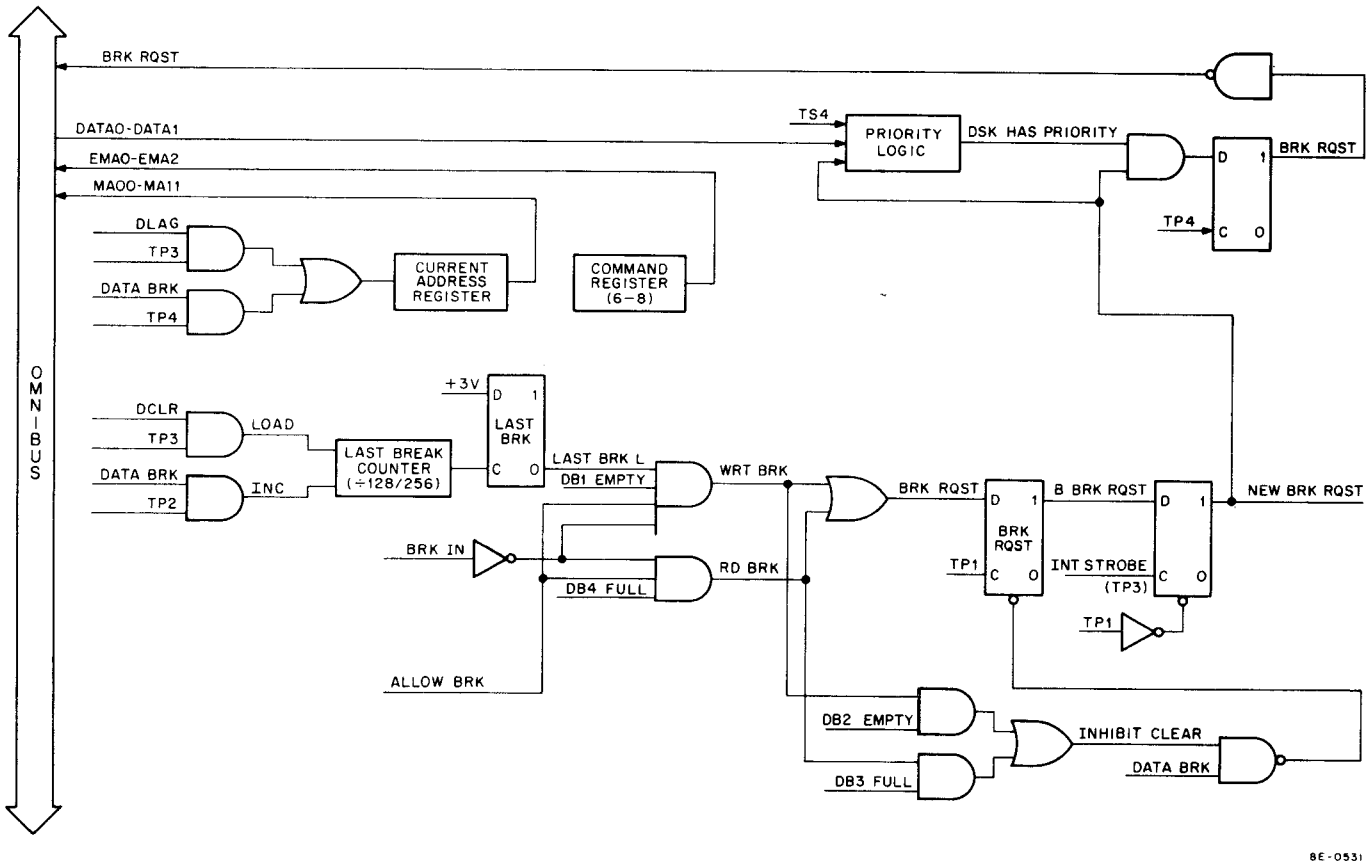

Figure 11-10 Data Break Control

The Current Address Register is loaded from the AC by a DLCA instruction with the initial address to be used in a data transfer. The Current Address Register is incremented after each data break and applied to the MA lines (MA00–MA11) to sequentially select memory locations for data transfers. Note that the memory field is selected by bits in the Command Register (Table 11-13) and not incremented when the CA Register is incremented. The direction of data transfer is determined by the decoded function bits in the Command Register, i.e., during a read operation, data is transferred from the Data Buffer Register to memory via the data bus. Time pulses from the OMNIBUS and control signals from the Data Buffer Register determine the timing of the single cycle data break. The data break control also generates signals to stall the processor and stop the execution of instructions during a data transfer.

The data break priority is returned to the OMNIBUS as DATA 0 (priority 0) or DATA 1 (priority 1) to indicate the priority of the RK8-E. Data break control provides a DATA LATE signal to the Status Register if the processor does not respond to a BRK RQST within 22.5 μs. The last break counter counts the words in a data transfer and sets the LAST BRK flip-flop when 128 (half block) or 256 words have been transferred.

11.14.5 Data Buffer Register

The Data Buffer Register (Figure 11-11) provides four Data Buffer Registers (DB1–DB4) for temporary storage of data that is being transferred between memory and the disk drive. The four registers increase the data break latency of the RK8-E control from 5.6 μs to 22.5 μs. Latency is defined as the maximum time the RK8-E can wait for a BRK RQST to be accepted by the processor. During a write operation, parallel bits of data (MD00–MD11) are received from the OMNIBUS and applied to DB1. The parallel data is dropped into DB4 and shifted out of DB4 on RK DATA 11 as serial data to the selected disk drive. During a read operation, serial data from the disk is shifted into DB1 and dropped into DB4. The parallel bits out of DB4 are transferred to the data bus for transfer to memory during a single cycle data break. The control logic associated with the Data Buffer Register controls the registers and generates signals that are applied to the data break control logic. During maintenance operations, the contents of the CRC Register, Command Register, and Surface/Sector Register can be shifted into DB4 and transferred to the AC or memory by the DMAN instruction. The shifting of data in these registers is accomplished by the MAIN pulse, which is generated by the DMAN instruction.

11.14.6 CRC Register

The CRC Register (Figure 11-12) is a 16-bit multipurpose register with the following functions:

a. The CRC Register receives a cylinder address from the AC when the DLAG (GO) instruction is executed by the program and transfers the cylinder address to the selected disk drive.

b. Makes a bit-by-bit comparison of the cylinder address specified by the program and the cylinder address from the disk drive to determine if disk has found the correct cylinder.

c. During a write operation, a 16-bit CRC character is computed, transferred to the disk, and written at the end of the record.

d. During a read operation, a 16-bit CRC character is computed and compared with the CRC character written at the end of the record. If the two characters are different, NOT EQUAL is asserted to set the CRC ERROR flag. A CRC ERROR is produced if bits are lost or added during the read or write operation.

The disk address is transferred from the AC as a 12-bit parallel word and bit 11 from the Command Register is added to the 7 most significant bits of the CRC Register to form the 8-bit cylinder address (Figure 11-5) transferred to the selected disk drive. Bits 12 through 16 are not used for the disk address. The disk address is transferred to the disk drive on parallel lines during the STROBE major state.

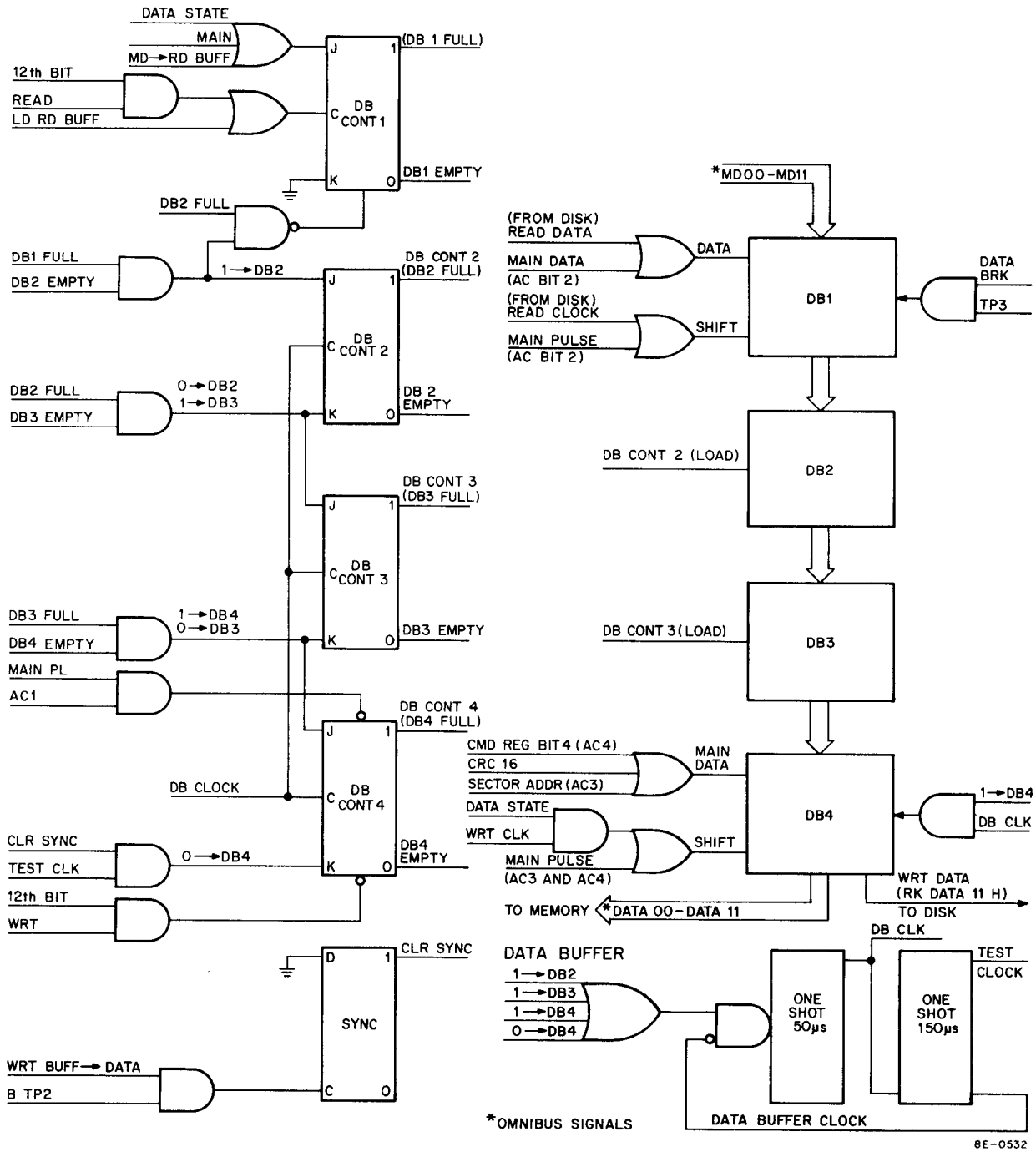

Figure 11-11 Data Buffer Register

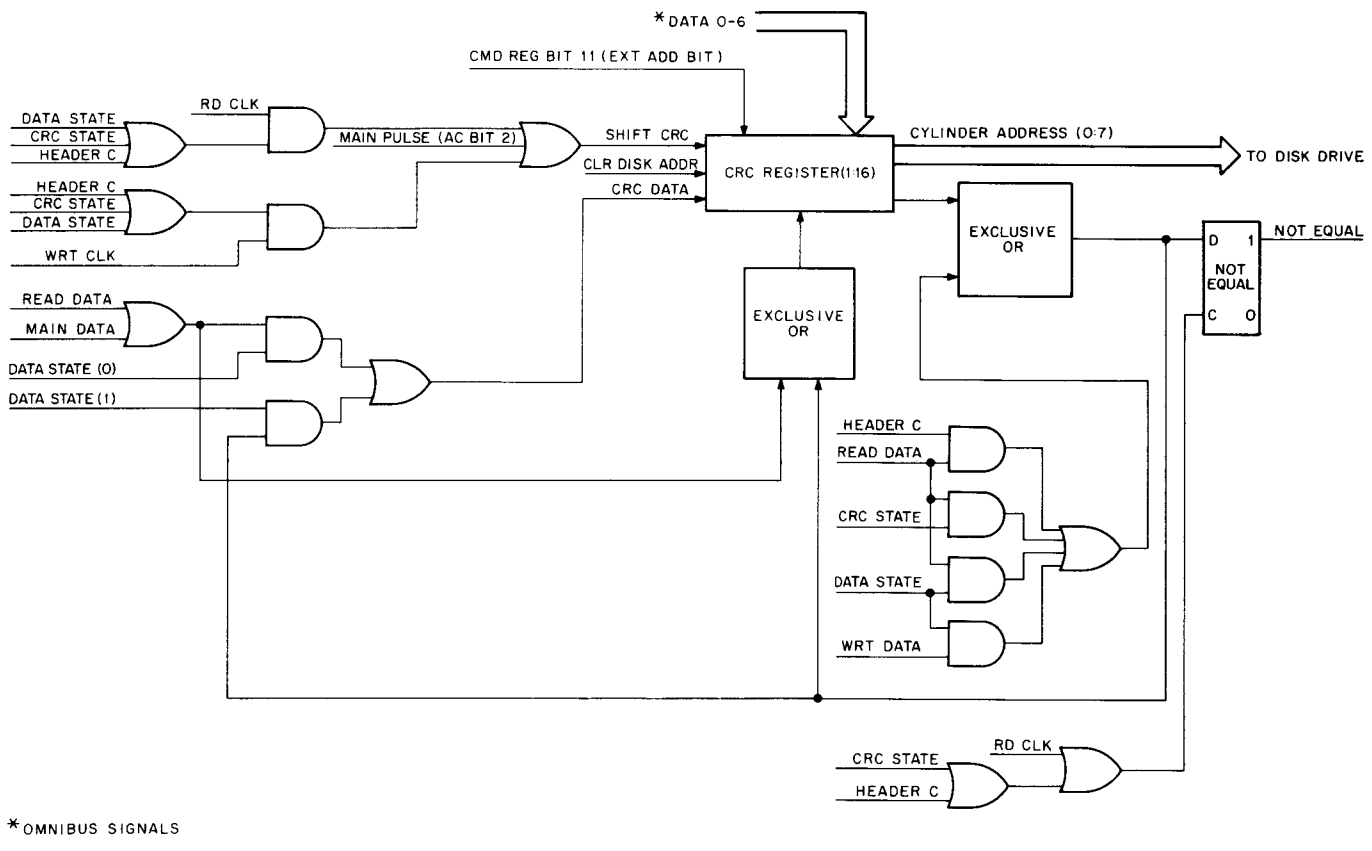

Figure 11-12 CRC Register

When the RK8-E moves into the DATA state, the CRC Register is cleared and the computation of a CRC character is started.

During write operations, the CRC character is transferred to the disk drive during the CRC state as a 16-bit serial word. The serial bits are shifted out of the CRC Register to the disk drive and written at the end of the data.

During read operations, the CRC character is computed from the data read from the disk and compared with the CRC character that was written at the end of the data. The CRC Register makes a bit-by-bit comparison of the two CRC characters, and if they are different, NOT EQUAL is asserted to set the CRC ERROR flag.

The contents of the CRC Register are checked using the maintenance instruction. The bits in the CRC Register are shifted into Data Buffer 4 and transferred to the AC (Table 11-14).

11.14.7 Control Sequencer

The control sequencer (Figures 11-13 and 11-14) comprises the Major States Register, word counter (128 or 256 words), and the bit counter. The word counter and bit counter keep track of the number of words transferred to or from the disk drive. The bit counter counts 12 bits from the disk drive and increments the word counter each time a word (12 bits) is read from the disk. After 256 words are read, the data transfer is stopped and the CRC character is written on the disk during a write, or read from the disk during a read. If bit 5 in the Command Register is set (1), the data transfer is stopped after 128 words are read or written, but the disk drive continues to write all zeroes during a write operation or read all zeroes during a read operation until 256 words have been written or read. This allows the RK8-E to process the CRC character, which is always written at the end of the data (Figure 11-7).

The Major States Register determines the format of the disk, i.e., PREAMBLE, HEADER, DATA, CRC, and POSTAMBLE.

11.14.7.1 Major States – The Major States Register (Figures 11-13 and 11-14) controls each step the RK8-E control progresses through to perform a seek, read, or write operation. Each major state causes specific operations to be performed (Table 11-2 and Figure 11-7).

The Major States Register is a shift register that shifts a binary 1 starting at the IDLE state and ending with the END states as shown in Figure 11-7 unless an error occurs (i.e., an ADDRS ERROR) or the function does not require all major states (i.e., sector, seek, and recalibrate).

11.14.7.2 IDLE State – The RK8-E must be in the IDLE state (Figure 11-13) to allow initiation of a disk function and returns to the IDLE state after an operation is completed. The IDLE state indicates that the control is not busy and that it is capable of accepting IOT instructions from the processor (Figure 11-14). The IDLE flip-flop is cleared when the program executes a DLAG instruction (load disk address and GO) or the CLR drive (DCLD) instruction. The DCLD instruction initiates a special state called RESTORE, which is discussed in Paragraph 11.15.3.

The IDLE state flip-flop is set by any of the following conditions to return the control to the IDLE state to wait for RK8-E instructions.

a. At the end of ERASE DELAY during a write function.

b. During last break of a read operation (after Data Buffer Register is empty).

c. When the selected disk drive asserts ACKNOWLEDGE during a seek only operation.

d. When the ERROR flag is set (Table 11-12).

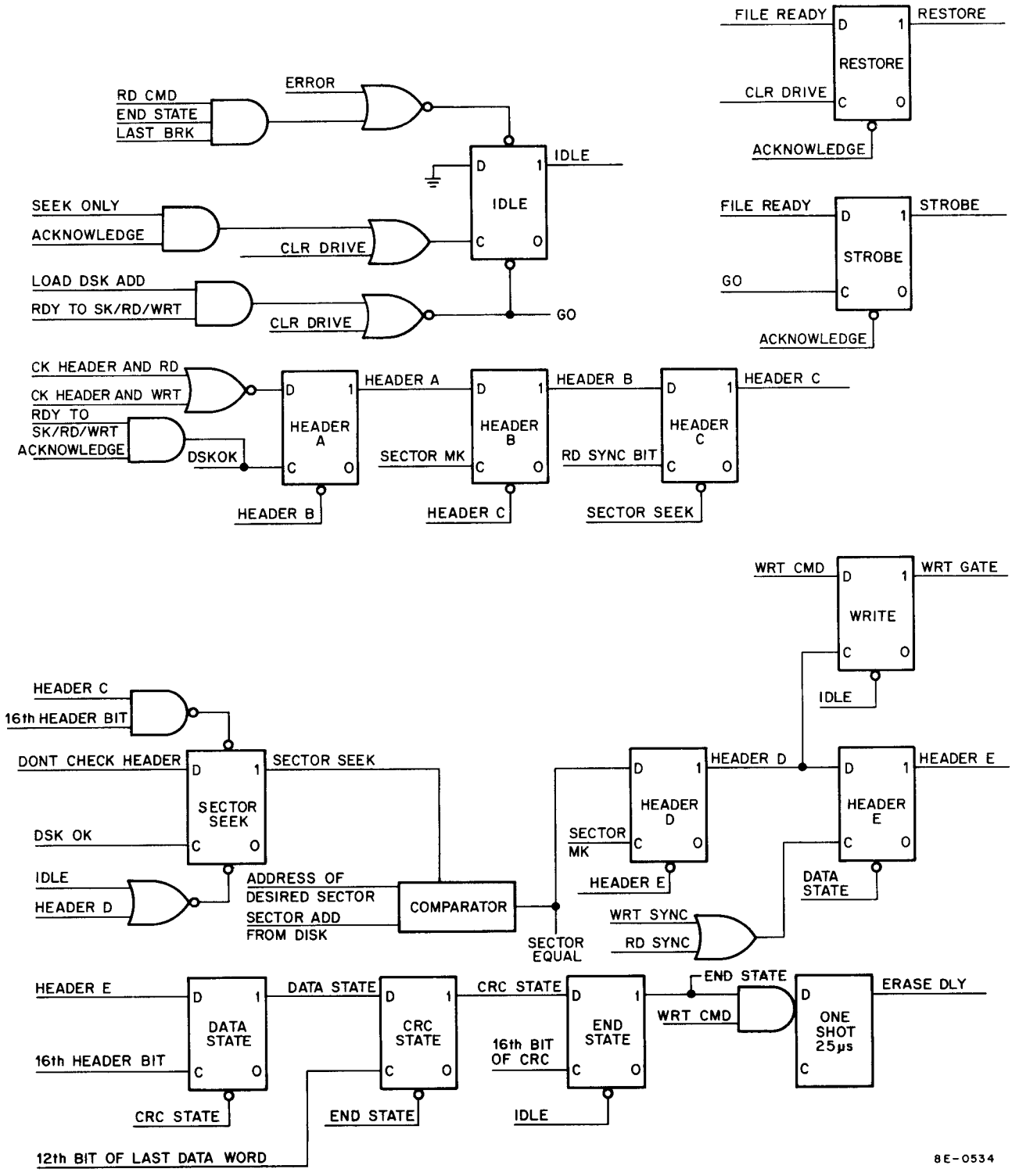

Figure 11-13 Major States Register

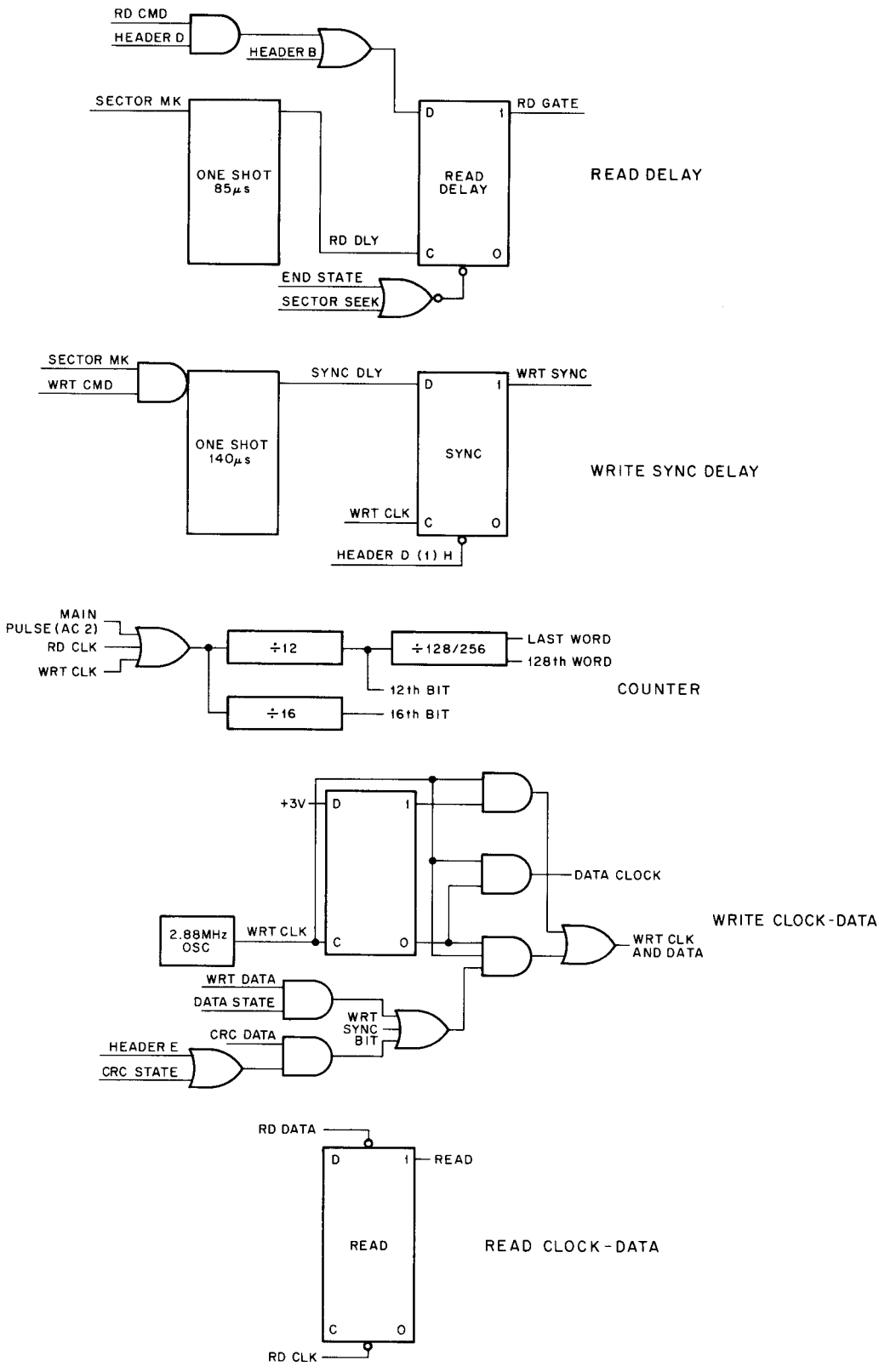

Figure 11-14 Read/Write Delays and Counters

11.14.7.3 RESTORE State – The RESTORE state is a special state (Figure 11-13) used to clear SELECT ERRORS and CYLINDER ADDRESS ERRORS. RESTORE is set by FILE READY and the CLR DRIVE command, generated by the DCLD instruction. When the selected disk asserts ACKNOWLEDGE, the RESTORE flip-flop is cleared and the Major States Register goes back to the IDLE state to wait for RK8-E instructions. Thus, the RK8-E uses only one state for the clear operation and the control is released (made not busy) while the disk drive returns to the home position.

11.14.7.4 STROBE State – The STROBE state (Figure 11-13) is used to transfer the cylinder address from the CRC Register to the disk drive and wait for the selected drive to ACKNOWLEDGE the cylinder address. The STROBE flip-flop is set by GO when the DLAG instruction is executed by the program if the selected disk drive is ready (FILE READY asserted). STROBE is cleared when ACKNOWLEDGE is received from the selected drive and the Major States Register moves to the HEADER A state or SECTOR SEEK state (Figure 11-7) when the selected drive is ready to seek, read or write (Figure 11-14).

11.14.7.5 HEADER A State – The HEADER A state (Figure 11-13) is used to start a read delay (Figure 11-15) and wait for a sector mark during read and write functions. When a sector mark is obtained from the disk drive, the HEADER B state is entered and the HEADER A state is cleared by HEADER B.

11.14.7.6 HEADER B State – The HEADER B state (Figure 11-14) is used to turn READ on at the end of READ DELAY (Figure 11-12) and read zeroes until a SYNC pulse is encountered. The SYNC pulse indicates the beginning of the HEADER area of the disk format.

During a write operation, the write sync delay is triggered when a sector mark is received from the disk (Figure 11-14). After a 140 μs (write sync delay), a one bit (SYNC pulse) is written on the disk to indicate where the HEADER area starts. When the SYNC pulse is read or written, the RK8-E advances to the HEADER C state and HEADER B is cleared.

11.14.7.7 HEADER C State – The HEADER C state (Figure 11-14) is used to read the 16-bit HEADER word and compare it bit-by-bit with the disk address in the CRC Register. HEADER C is cleared when the divide-by-16 counter (Figure 11-15) asserts 16th bit to indicate the 16th bit of the HEADER word has been read from the disk drive. When HEADER C clears, it sets SECTOR SEEK (Figure 11-14) and starts the SECTOR SEEK major state.

11.14.7.8 SECTOR SEEK State – When the control enters the SECTOR SEEK state, cylinder address ERROR is set if the cylinder address does not equal the HEADER word read from the disk during the HEADER C state (Figure 11-12). During the SECTOR SEEK state, the sector address lines from the RK05 are compared with the Surface/Sector Register.

11.14.7.9 HEADER D State – The HEADER D state is used to wait for the completion of READ DLY (85 μs) during a read function or the completion of SYNC DLY during a write operation. If this is a read function, the controller reads all zeroes until a SYNC bit is read. When the sync bit is read, the control advances to the HEADER E state. If this is a write function, the control writes zeroes and waits for SYNC DLY, then writes the SYNC bit (a data 1). When the SYNC bit is written, the RK8-E moves to the HEADER E state and clears the HEADER D flip-flop.

11.14.7.10 HEADER E State – The HEADER E state is used to read, but ignores 16 bits of data during a read operation. During a write operation, the 16-bit HEADER word in the CRC Register is written. When the 16-bit HEADER word has been read or written, the Major States Register advances to the DATA state.

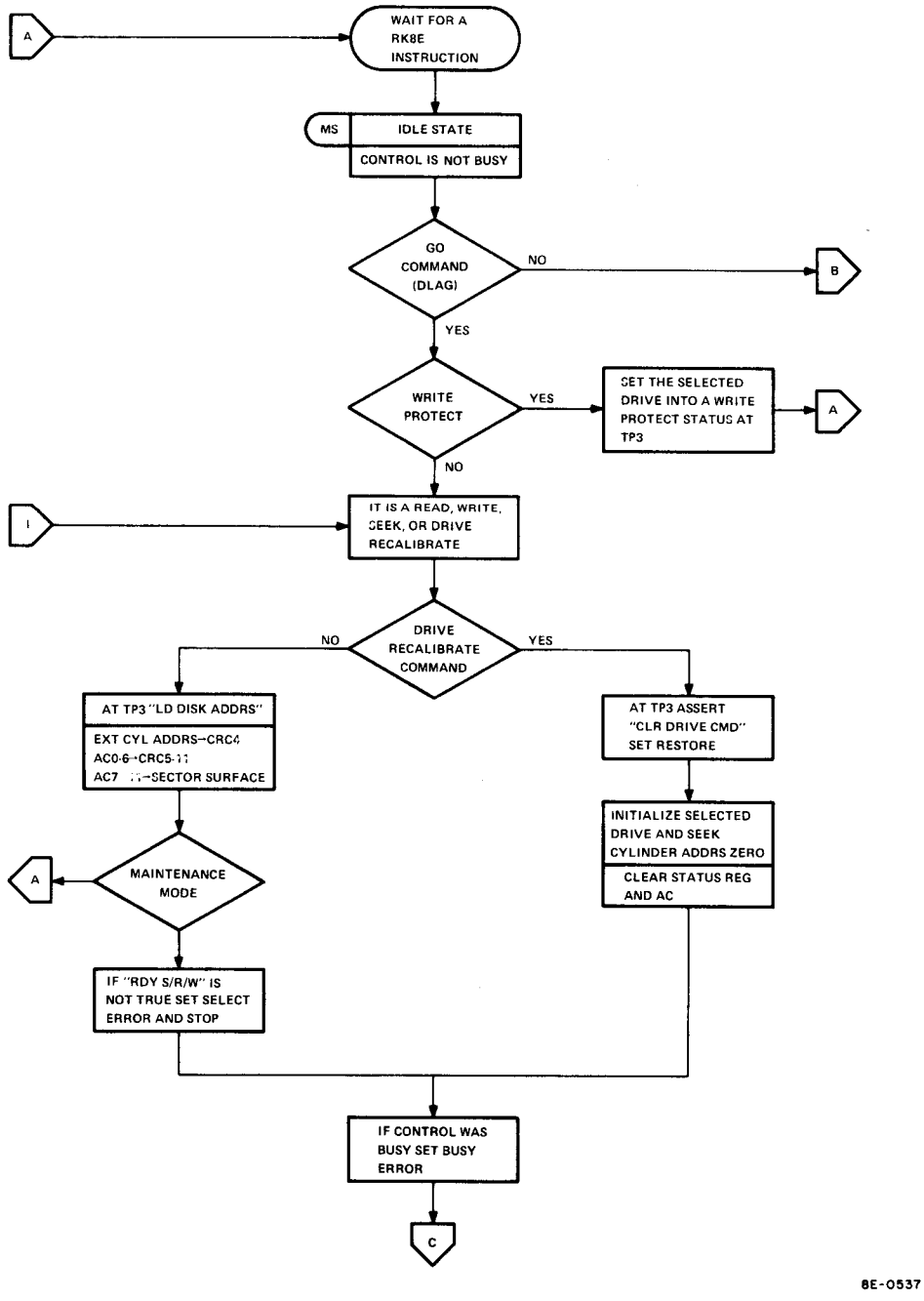

Figure 11-15 RK8-E Flow Diagram (sheet 1)

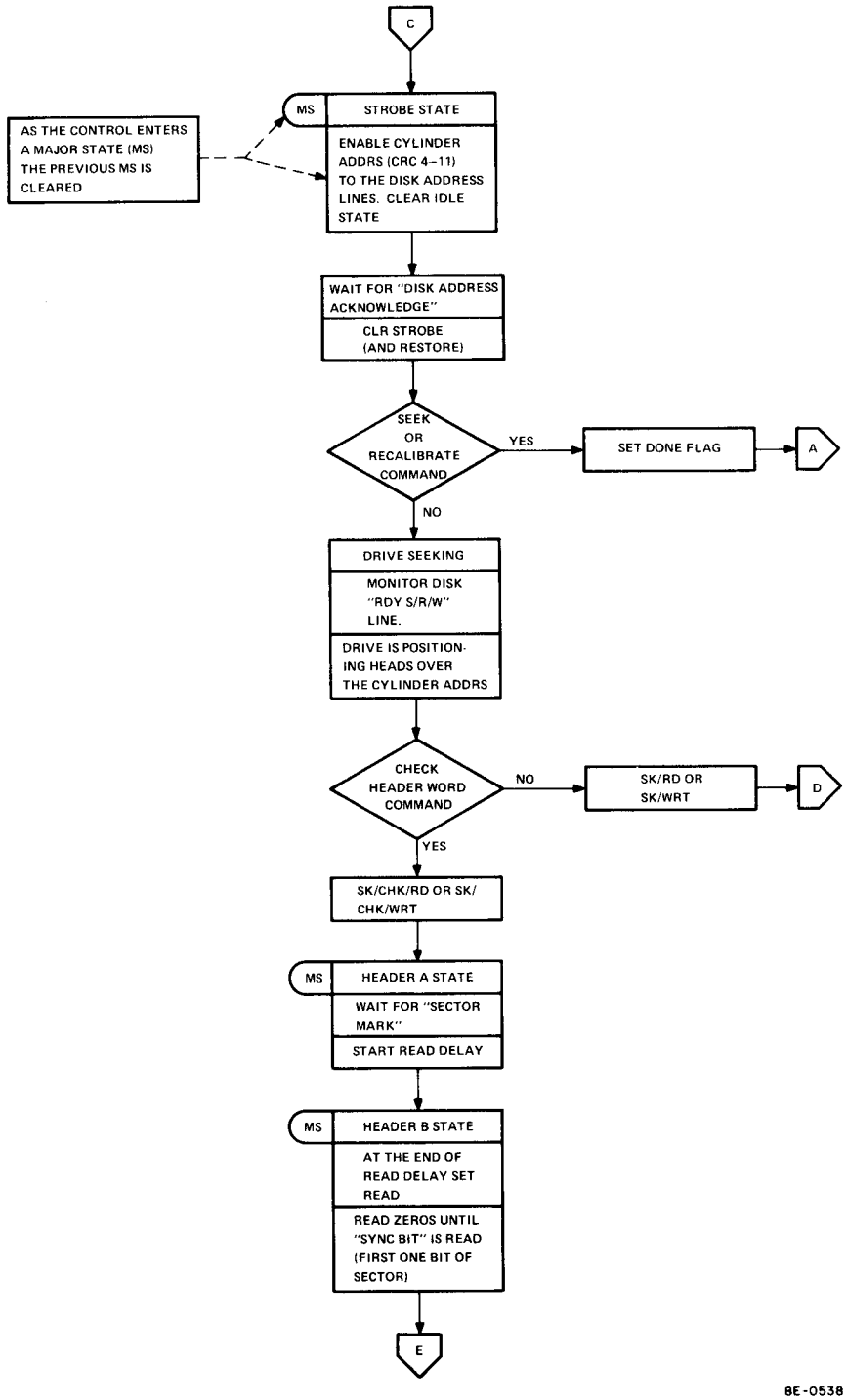

Figure 11-15 RK8-E Flow Diagram (sheet 2)

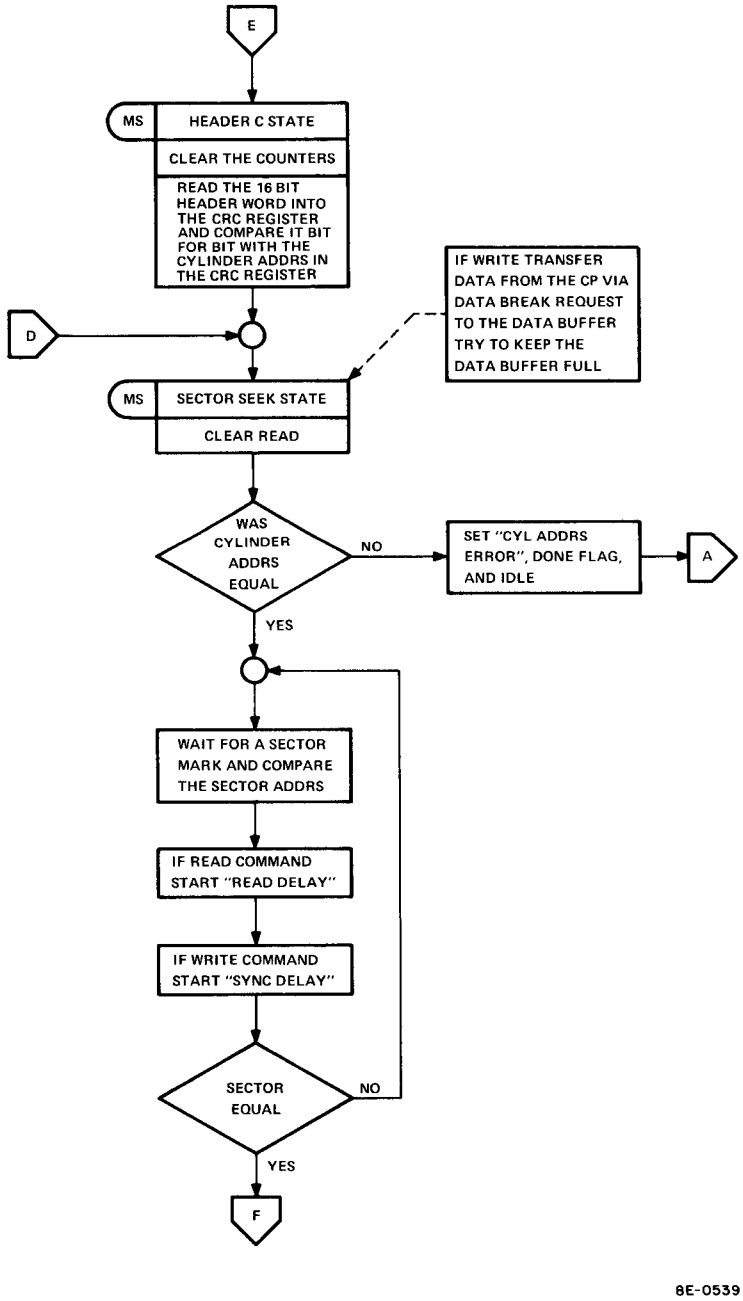

Figure 11-15 RK8-E Flow Diagram (sheet 3)

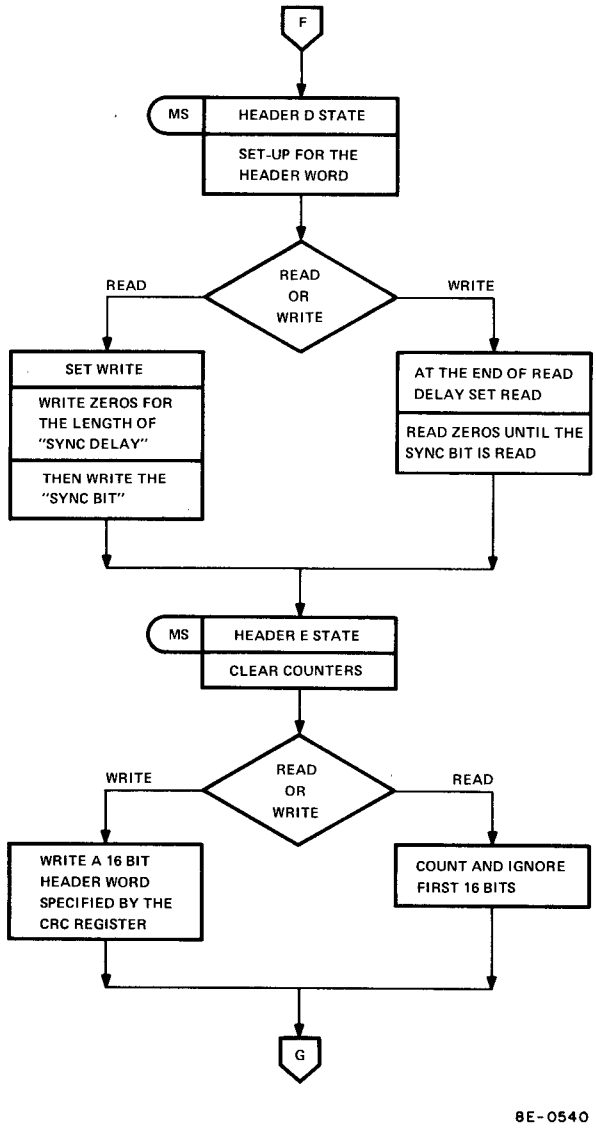

Figure 11-15 RK8-E Flow Diagram (sheet 4)

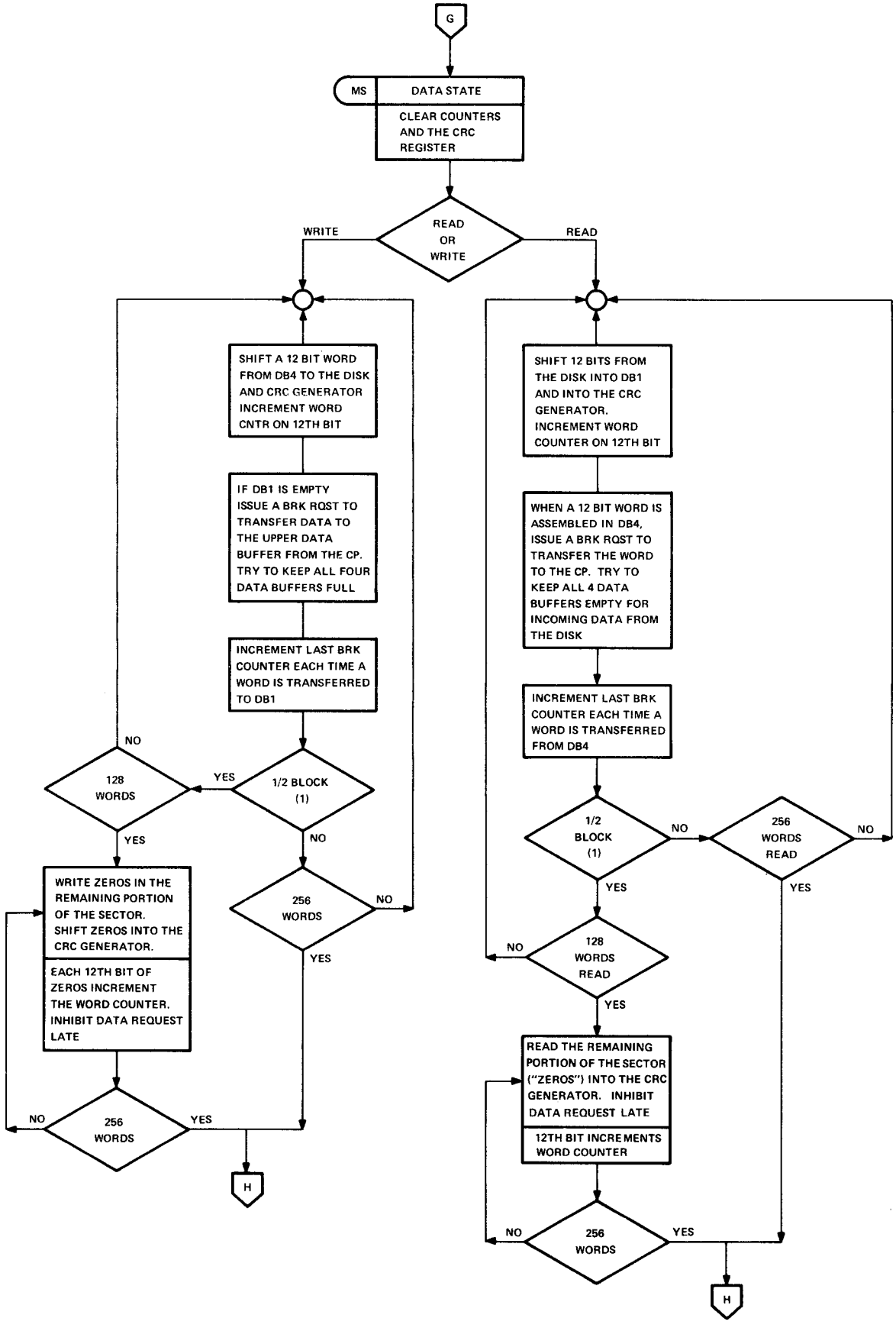

Figure 11-15 RK8-E Flow Diagram (sheet 5)

8E-0541

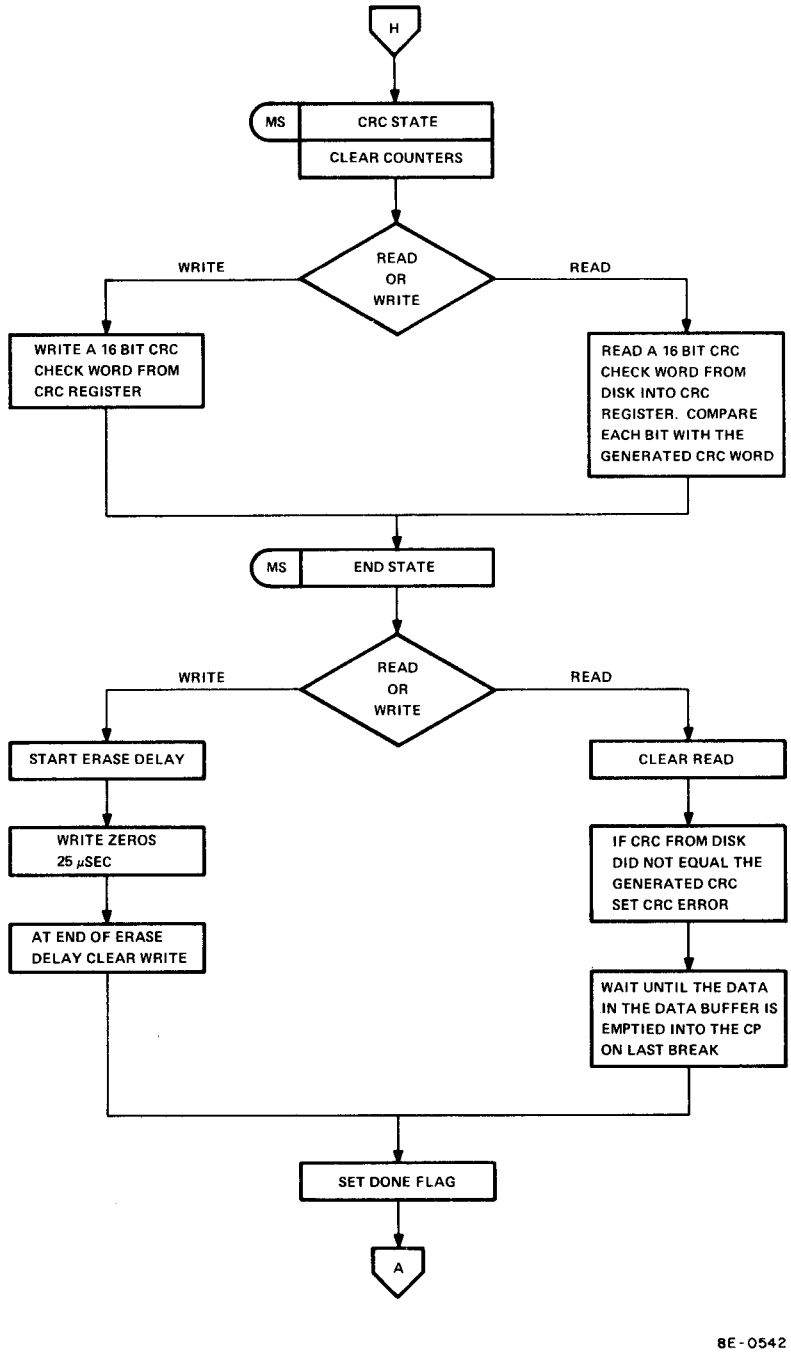

Figure 11-15 RK8-E Flow Diagram (sheet 6)

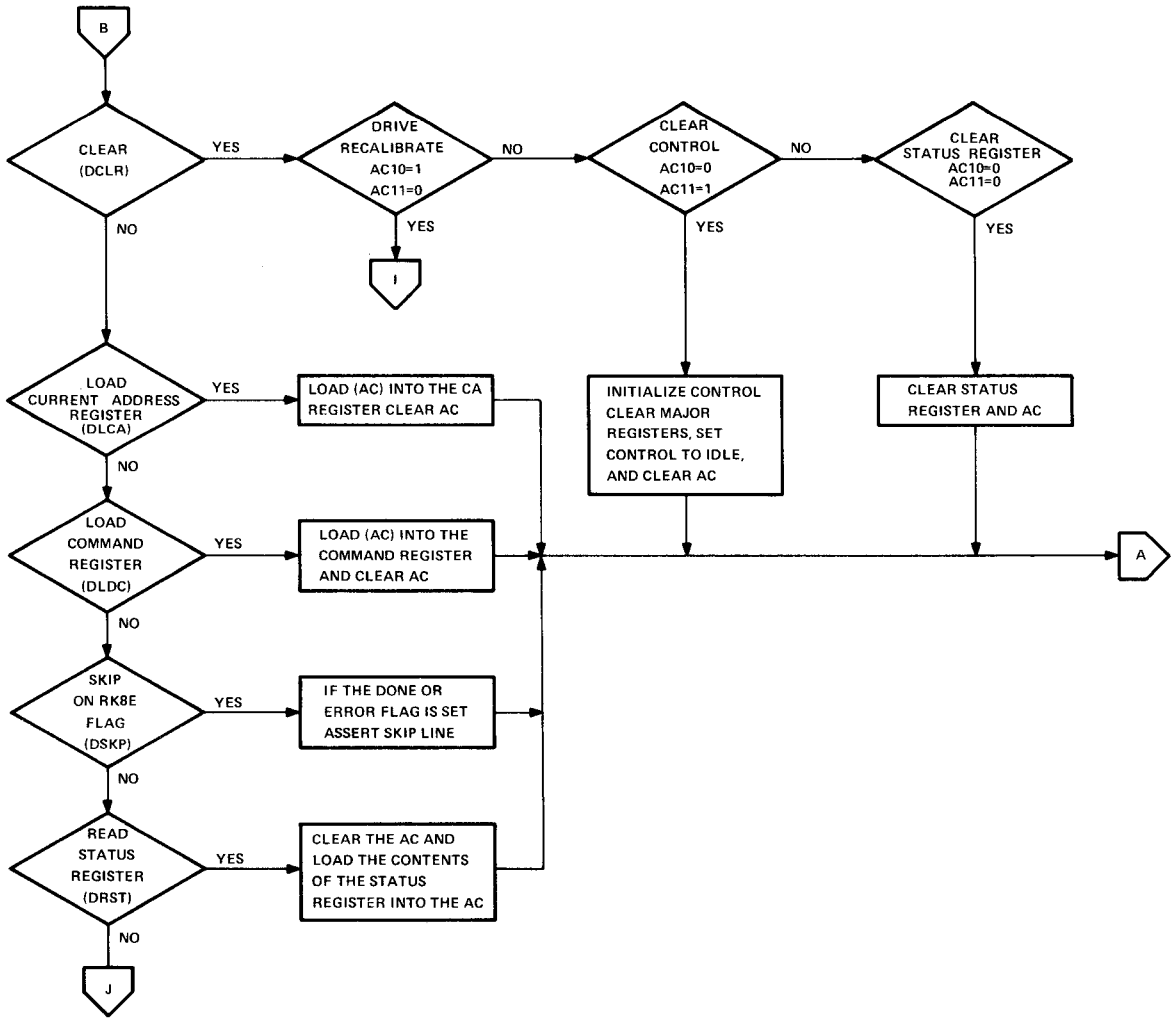

Figure 11-15 RK8-E Flow Diagram (sheet 7)

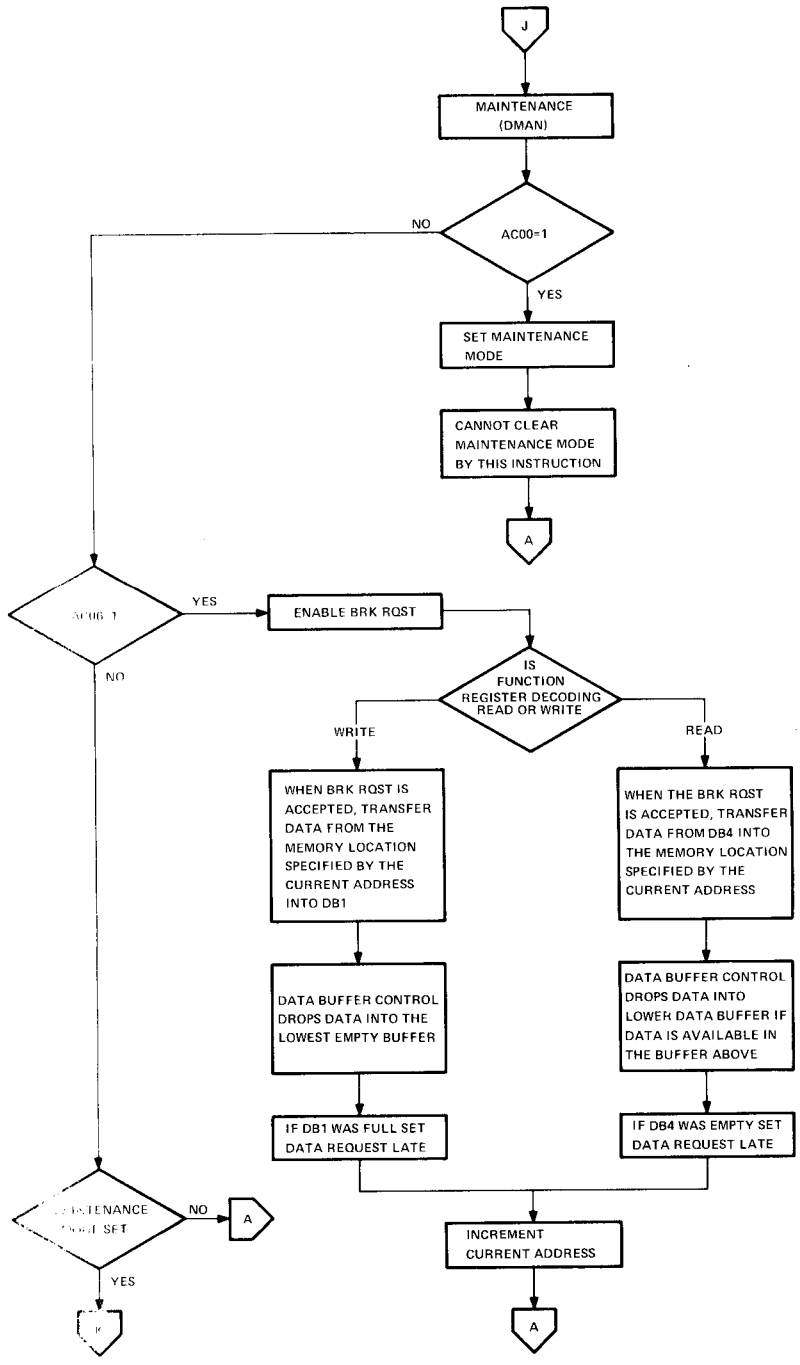

Figure 11-15 RK8-E Flow Diagram (sheet 8)

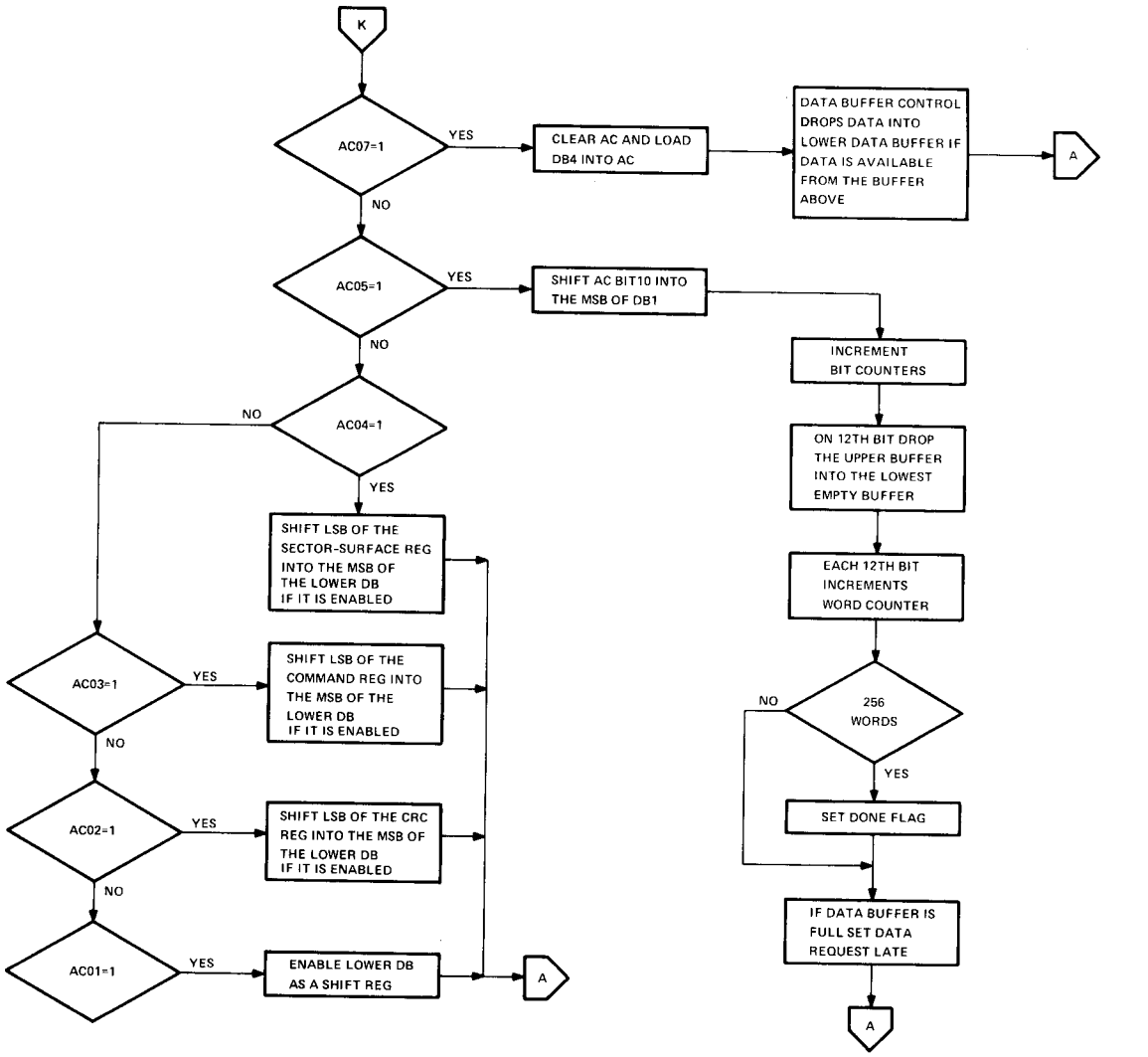

Figure 11-15 RK8-E Flow Diagram (sheet 9)

11.14.7.11 DATA State – The DATA state is used to transfer 256 data words from PDP-8/E memory to the disk drive during a write operation, or transfer 256 words of data from the disk drive to memory during a read operation. The data break control logic tries to keep the Data Buffer full during a write operation and tries to keep the Data Buffer empty during a read operation (the block diagram of the Data Buffer Register is discussed in Paragraph 11.14.5 and the block diagram of the Data Break control logic is discussed in Paragraph 11.14.4). The DATA state ends when 256 words have been transferred and the word counter asserts LAST WORD. If the RK8-E has been instructed to write 128 words, 128th word is asserted after 128 words (half block) have been transferred. The 128th word ends data transfer operations and the disk reads or writes zeroes until the full block of data (256 words) has been read or written. When LAST WORD is asserted, the RK8-E advances to the CRC state and clears the DATA state flip-flop.

11.14.7.12 CRC State – The CRC state (Figure 11-13) is used to write the CRC character, computed by the CRC Register (Figure 11-12) on the disk at the end of a sector during write operation. During read operations, the CRC character computed by the CRC Register during the data transfer is compared with the CRC character read from the disk. An Exclusive OR circuit on the CRC Register makes a bit-by-bit comparison of the CRC character read from the disk and the CRC character shifted out of the CRC Register. If the two characters are not equal, the CRC ERROR flag is set to indicate a CRC ERROR occurred during the data transfer. The program must check the Status Register to determine if the CRC ERROR set the ERROR flag. The Major States Register advances to the END state and clears the CRC state flip-flop when 16th BIT L is asserted.

11.14.7.13 END State – The END state is used by the read operation to allow the Data Buffer Register to be emptied by the single cycle data break, set the CRC ERROR flag if the CRC characters were not equal, clear READ, set the DONE flag, and return the RK8-E to the IDLE state (not busy). During a write operation, the controller starts ERASE DLY (Figure 11-13) and after 25 μs, WRITE is cleared, the DONE flag is set and the RK8-E is returned to the IDLE state. Note that there is no CRC character comparison during a write operation and no CRC ERROR should be detected.

11.14.8 Read/Write Delays, Clocks, and Counters

The read/write delays, clocks, and counters generate signals to assist the Major States Register in the control of disk operations and help to develop the disk format.

11.14.8.1 Write Data Clock – The write data clock (Figure 11-14) is a 2.88 MHz oscillator that is used to generate the WRT CLK pulses (Figure 11-2) during a write operation. The time between WRT CLK pulses (690 ns) is referred to as a bit cell, which is used to write data. The WRT DATA CLK and a SYNC bit, CRC DATA bit, or a DATA bit are written on the disk cartridge.

11.14.8.2 Write Sync Delay – Write sync delay (Figure 11-14) is a 140 μs delay that is started when a SECTOR MARK from the disk drive is detected during write operations. After 140 μs, WRT SYNC is asserted and the SYNC bit is written on the disk drive.

11.14.8.3 Read Delay – The read delay (Figure 11-14) is an 85 μs delay that is started when the SECTOR MK from the disk drive is detected, if the RK8-E is in the HEADER D state of a read operation. The 85 μs delay allows the control to wait for a SYNC bit before advancing to the HEADER E state. RD DLY asserts the RD gate to allow the RK05 to read.

11.14.8.4 Read Clock Data – The READ flip-flop (Figure 11-14) is set by RD DATA from the RK05 and cleared by RD CLK to generate the READ signal. The READ signal is used to enable READ data pulses to be applied to the Data Buffer Register. The READ data pulses are clocked into the Data Buffer Register by the RD CLK signal.

11.14.8.5 Counters – The RK8-E contains 4 counters (Figure 11-14) a divide-by-12-bit counter, a divide-by-16-bit counter, a divide-by-128- or 256-word counter and a break counter. The divide-by-12 counter counts the bits of data as they are read from the disk drive. Each time 12 bits (one word) are read, the word counter is incremented by 1. After 256 words are read, LAST WORD L is asserted to end a data transfer. If the HALF BLOCK bit (bit 5) in the Command Register is set, the 128th WORD signal is asserted after 128 words are read or written. This causes the RK8-E to stop data transfers between memory and the disk drive, but the disk drive continues to read or write all zeroes until LAST WORD L is asserted (256 words have been read or written). When LAST WORD is asserted, the data transfer is complete. The 16-bit counter asserts 16th bit when 16 bits are read from the disk or written on the disk. This is used when the PREAMBLE and CRC are read or written to count 16 bits instead of 12.

The break counter is incremented during TP2 time of a break cycle to count the single cycle data breaks. LAST BRK H is asserted after 128 or 256 words have been transferred to or from memory. There are 128 break cycles when the HALF BLOCK bit (bit 5) in the Command Register is a 1. Note that LAST BRK does not stop a read or write operation because 256 words must be read or written to end an operation. If HALF BLOCK is set (1), the last 128 words are all zeroes and not used.

11.14.9 Maintenance Logic

The maintenance logic (Figure 11-16) allows the program (software) to check the RK8-E operation. The program can transfer the contents of the Data Buffer Register, CRC Register, Command Register, and Surface/Sector Register to the AC or memory if the program executes the DMAN instruction. The operation performed when the DMAN instruction is executed by the program is determined by the contents of the AC (Table 11-14 and Figure 11-15). The maintenance logic allows the program to shift the contents of the CRC Register, Command Register, or Surface/Sector Register into the Data Buffer Register for transfer to the AC by a DMAN instruction or to memory by a data break. The shifting of registers is accomplished by the MAIN pulse, which is generated each time a DMAN instruction is executed. The program must keep track of the number of shifts and determine when to transfer the data to the AC or memory.

The maintenance logic checks all counters in the RK8-E control and allows data to be transferred from the AC to the Data Buffer Register.

The maintenance logic provides timing pulses to the major registers, data break control, and control sequencer to check these groups of logic. Note that the DMAN instruction disables the DLAG (GO) IOT and a clear operation must be performed to allow the program to continue after maintenance operations are executed by the program.

11.15 DETAILED LOGIC DESCRIPTION

The logic in the RK8-E is divided into functional groups for discussion purposes. The block diagram, Figure 11-9, and the flow diagram, Figure 11-15, should be used to understand the interaction of the logic, the signal flow within the RK8-E, and the input or output signals.

11.15.1 I/O Bus Interface

The I/O bus interface consists of the MD receivers, IOT decoder, interrupt and skip logic, and timing and control logic.

11.15.1.1 MD Receivers – The MD receivers allow data on the MD lines to be applied to the device select logic and I/O decoder when an RK8-E I/O instruction is executed by the program. The MD receivers also allow data on the MD lines to be applied to the Data Buffer Register during a write operation (MD → RD BUFF L and MD → RK L are asserted).

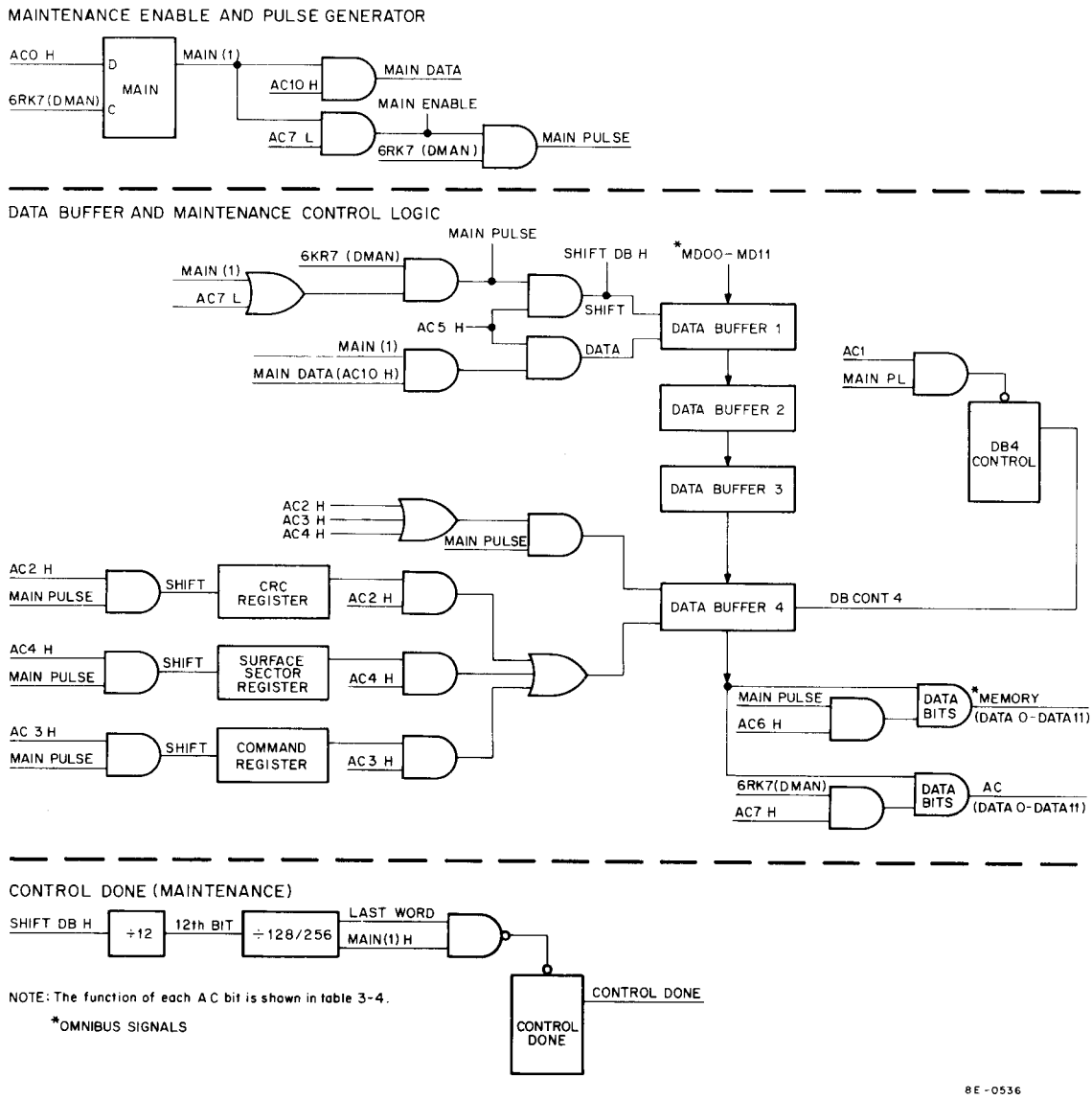

Figure 11-16 Maintenance Logic

11.15.1.2 IOT Decoder Logic – The IOT decoder (Figure 11-17) decodes MD bits (instructions) from the Memory Data Bus and generates signals to control the operation of the RK8-E. Bits MD3–11 are gated by MD → RK L when I/O PAUSE L is asserted by the processor. I/O PAUSE L is asserted anytime an IOT instruction is executed by the program. MD3–8 generates a signal DEVICE RK H and enables bits MD9–11 to be applied to the IOT decoder (an 8251 IC). The 8251 IC is a BCD to decimal decoder (see Volume I, Appendix A for truth table, logic diagram, and pin locations) that produces a low on one output line to indicate which instruction has been executed by the program. For example, MD9 low, MD10 and 11 high (100) produce a low on pin 9, which indicates a DLCA (6744) instruction was executed by the program. The jumpers on MD6–8 are used to select the device code for the RK8-E when multiple systems are installed (see Table 11-3 for jumpers to select the device codes). Internal I/O L is asserted by the DEVICE RK signal to prevent the processor from executing other IOT instructions while the RK8-E is executing an IOT instruction.

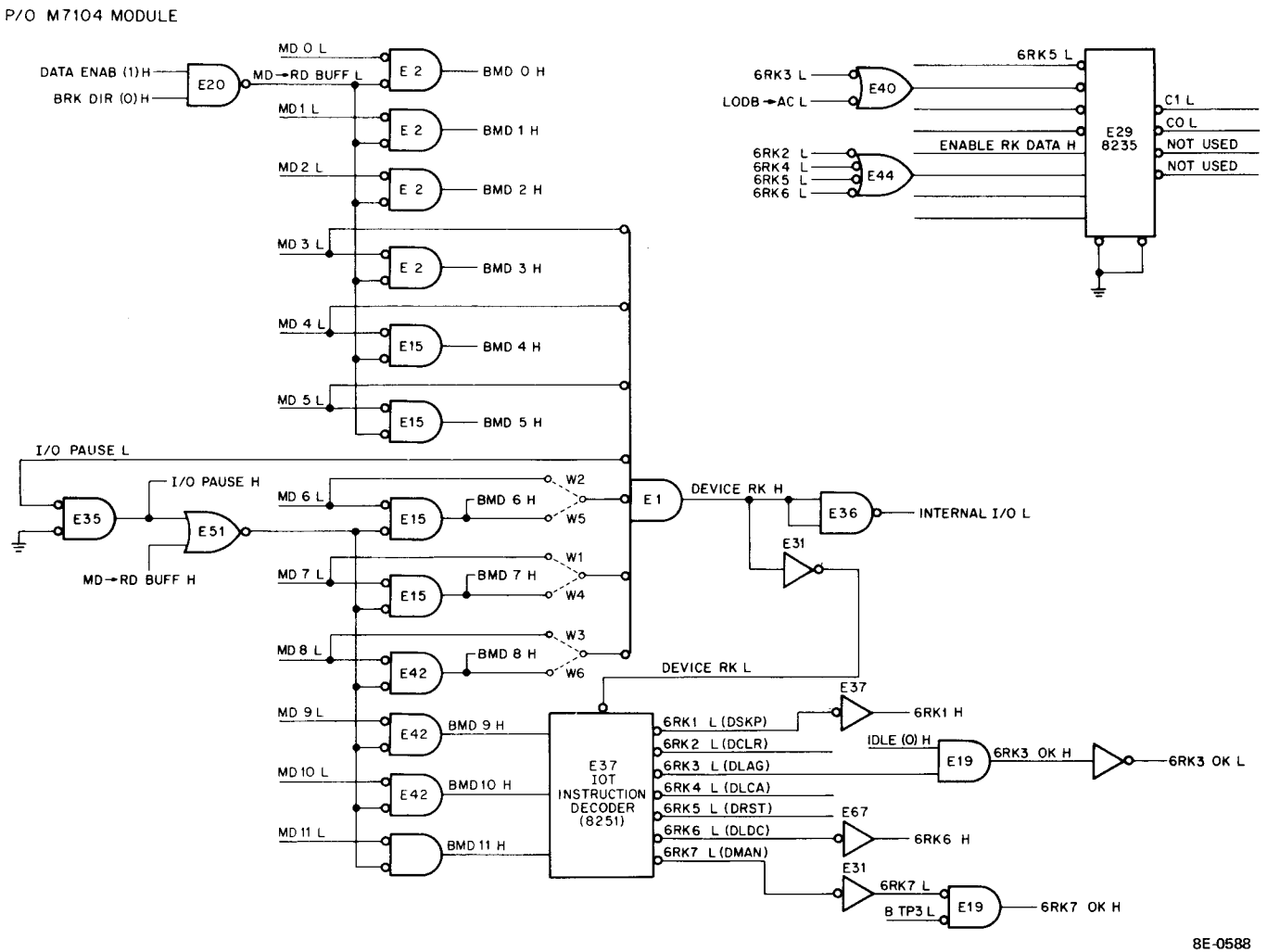

Figure 11-17 MD Receivers and IOT Decoder

11.15.2 Control Logic

11.15.2.1 C Line Select Logic – The C line select logic (Figure 11-17) controls the direction of data flow between the Data Bus and the AC and determines whether the AC is cleared or not. Table 11-15 shows the status of C0 and C1 to transfer data between the Data Bus and the AC using the RK8-E IOT instructions.

Table 11-15
C-Line Select Levels and Transfer Operations

Instruction	C0	C1	Transfer Operation
DCLR	Low	High	AC→ Data Bus, 0→ AC
DLAG	Low	High	AC→ Data Bus, 0→ AC
DLCA	Low	High	AC→ Data Bus, 0→ AC
DRST	Low	Low	Data Bus→ AC
DLDC	Low	High	AC→ Data Bus 0→ AC
DMAN	Low	High	AC→ Data Bus, 0→ AC

11.15.2.2 Time Pulse 3 (TP3) Logic – TP3 (Figure 11-18) is used throughout the RK8-E modules to enable gates for the execution of instructions. SHORT TP3 is used in the detection of a BUSY ERROR (Paragraph 11.15.4).

11.15.2.3 IDLE – The IDLE state indicates that the control is not busy; the control must be in the IDLE state to enable the execution of the 6RK2 (Figure 11-17), 6RK3, 6RK4, 6RK6, and 6RK7 (Figure 11-18) instructions.

11.15.2.4 Clear Logic – The logic of the RK8-E and/or the RK05 Disk Drives is cleared as follows:

a. By INITIALIZE during power up or if the CLEAR key is depressed on the PDP-8/E console.

b. The RK8-E logic is cleared by CLR ALL L if the 6RK2 (DCLR) instruction is executed by the program and AC bits 10 and 11 equal 01 (Table 11-11).

c. By CLR ALL L and CLR DRV CMD L if the 6RK2 (DCLR) instruction is executed by the program and AC bits 10 and 11 equal 10 (Table 11-11).

d. If a power failure is experienced and POWER OK H from the CPU goes low (Figure 11-18).

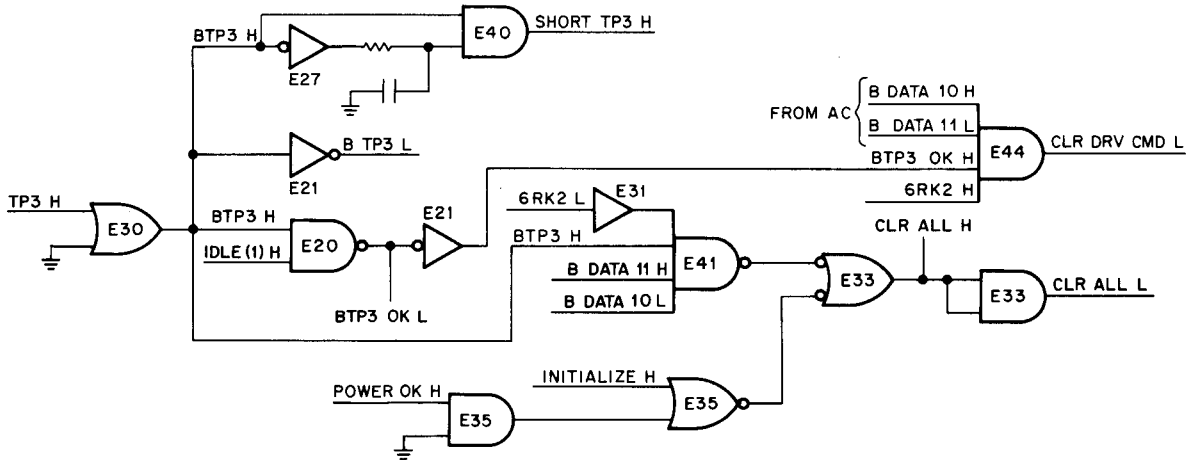

Figure 11-18 INITIALIZE, CLEAR ALL and Time Pulse 3 Logic

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11.15.2.5 Interrupt Logic – INT RQST L (Figure 11-19) is asserted to interrupt the program if ENABLE INT H is asserted (bit 3 in the Command Register must be 1) and the ERROR or DONE flags are set.

11.15.2.6 Skip Logic – The SKIP line is grounded if the ERROR flag or the DONE flag is set and the DSKP instruction is executed by the program (Figure 11-19).

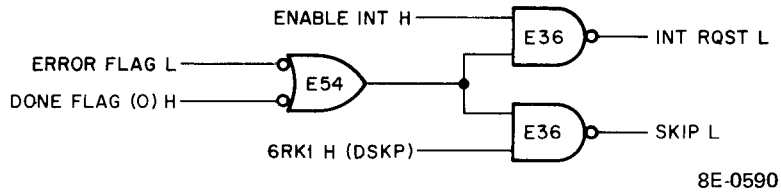


Figure 11-19 Interrupt and Skip Logic

11.15.3 Command Register

The Command Register (Figure 11-20) is loaded from the AC by a 6RK6 (DLDC) instruction. The Command Register (Table 11-13) is used to select a disk function, enable interrupts, read or write 128 words instead of 256, address extended memory, select a unit, and provide a bit (EXT CYL ADDRS) for cylinder addressing. The Command Register consists of three 8271 ICs (see Volume I, Appendix A for truth table, logic, and timing diagram) that contain 12-flip-flops, which are set or cleared by bits from the AC. The inputs to the flip-flops are enabled by DEVICE RK H, which asserts DATA ENAB L when the 6RK6 instruction is executed by the program to load the Command Register. The outputs of the Command Register are applied to a function decoder, unit select decoder, and the RK8-E control logic. Note that bit 11 is applied to the CRC Register to be used in cylinder addressing.

The contents of the Command Register can be shifted into Data Buffer 4 if the 6RK7 (DMAN) instruction is executed by the program and AC bit 3 is set. The MAIN PL H signal shifts the contents of the Command Register one bit position each time the DMAN instruction is executed by the program. The contents of the Command Register becomes a 12-bit serial word that is applied to DB4 in the Data Buffer Register as EXT CYL ADDRS H (Figure 11-25).

The Command Register is cleared anytime CLR ALL L is asserted (Paragraph 11.15.1.2).

11.15.3.1 Function Decoder – The function decoder (Figure 11-20) is an 74155 IC that decodes function bits 00–02 and determines what function is to be performed by the RK8-E and the selected RK05. The 74155 IC (see Section 7 for the truth table, pin locator, and logic diagram) is a 3-line to 8-line decoder that generates a low on one output line to select one of the RK8-E functions (Table 11-13). As an example, if F00 is high and F01 and F02 are low, the function is to seek a cylinder, check the HEADER, and write data on the specified sector.

11.15.3.2 Unit Select Decoder – The unit select decoder (Figure 11-20) decodes the unit select bits (UNIT SEL 0 and UNIT SEL 1) from the Command Register to select one of the RK05 Disk Drives. The unit select decoder is a 74155 IC that decodes the two unit select bits and grounds one of the unit select lines. The 74155 IC (see Section 7 for truth table, pin locator, and logic) is used as 2-line to 4-line decoder that grounds one of the unit select lines and selects one of the RK05 Disk Drives. As an example, if both unit select bits are high (11), pin 4 on the 74155 IC is grounded and drive 3 is selected for an operation.

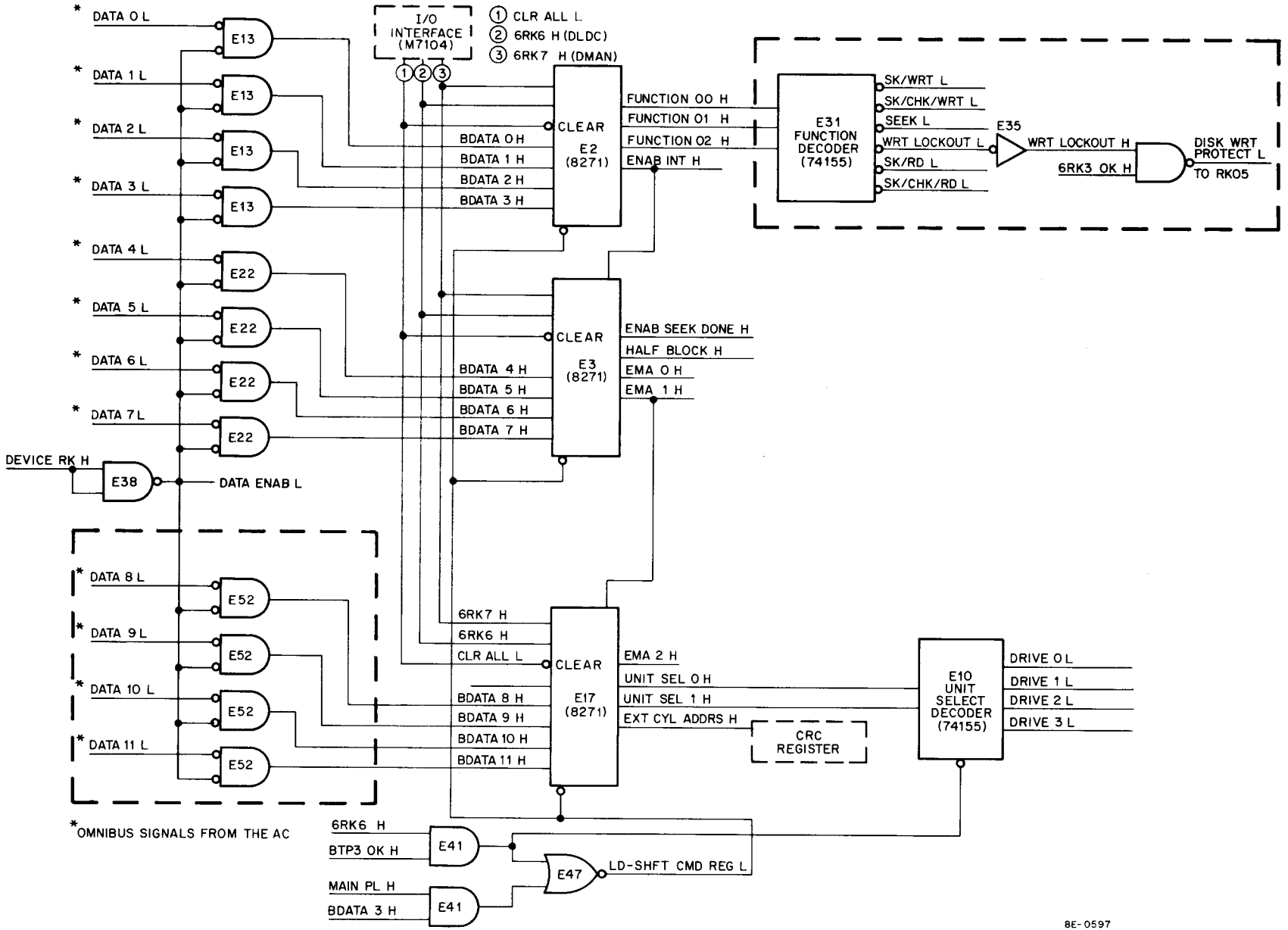


Figure 11-20 Command Register

11.15.4 Status Register

The Status Register (Figure 11-21) provides current status of the RK8-E and the selected RK05 Disk Drive to the program. The contents of the Status Register are transferred to the AC for evaluation by the program if the 6RK5 (DRST) instruction is executed by the program (Figure 11-27). The flip-flops that make up the Status Register supply inputs to the output data multiplexer (Figure 11-27) and are transferred to the AC via the Data Bus by the 6RK2 instruction. The flip-flops in the Status Register provide 1s (set) or 0s (cleared) to indicate error conditions.

11.15.4.1 TRANSFER DONE – The TRANSFER DONE flag (AC0) is set (Figure 11-21) during maintenance operations as follows:

a. By the LAST WORD PL H signal at the end of a data transfer operation. LAST WORD PL H is asserted after 256 words have been transferred. Note, if a half block or 128 words are transferred, the TRANSFER DONE flag is not set until 256 words have been read or written.

b. By IDLE (1) H if the IDLE flip-flop is set by the detection of an error during an operation or at the completion of an operation.

c. By IDLE (1) H and RDY S/R/W if bit 4 (ENABLE SEEK DONE) is set.

11.15.4.2 HEADS IN MOTION – HEADS IN MOTION H (AC1) is asserted when the read/write heads on the selected drive are in motion (Figure 11-21).

11.15.4.3 SEEK FAIL – SEEK FAIL (AC3) is set (1) when the DSK FAIL L signal from the RK05 is asserted (Figure 11-21). DSK FAIL is asserted by the selected disk drive if it fails to seek the cylinder address specified by program. A recalibrate operation must be executed by the program to clear this error condition.

11.15.4.4 DRIVE STATUS ERROR – The DRIVE STATUS ERR (AC6) is set when the selected disk drive is not ready (i.e., not turned on) by FILE READY L from the RK05 (Figure 11-21). Some action must be taken by the operator to clear this bit, i.e., power up the affected RK05.

11.15.4.5 CONTROL BUSY ERROR – CONTROL BUSY ERROR is set (1) if the program tries to do a DLAG, DCLR with AC=10, DLDC, or DLCA instruction while the IDLE flip-flop is cleared (Figure 11-21). Note that the control is busy unless the IDLE flip-flop in the Major States Register is set. This error occurs most often when new programs are debugged, a rewrite of the program or routine that caused the error should eliminate the problem.

11.15.4.6 TIME OUT ERROR – TIME OUT ERROR is set (1) if the control has been busy for more than 280 ms (Figure 11-21) or more than 7 revolutions of the disk cartridge. The DSK INDEX MK L signal is asserted once for each revolution of the disk and applied as the clock input to the 74193 IC (see Section 7 for pin locations and logic diagram). The 74193 IC is a 3-bit binary counter that sets the TIME OUT ERR bit in the Status Register if the Major States Register remains in some state other than IDLE for 280 ms. The binary counter is cleared each time the Major States Register goes to the IDLE state and starts a new countdown each time the IDLE flip-flop is cleared.

11.15.4.7 WRITE LOCK ERROR – WRITE LOCK ERROR (AC7) is set if the program tries to do a write operation on a disk drive that has been write protected (Figure 11-21). If the selected disk drive has been write protected, DSK WRT STATUS L from the write protected disk drive is high and the WRT LOCK ERR flip-flop sets when the WRT CMD is issued by the program. The WRT LOCK ERR flip-flop in the RK8-E is cleared by LD DISK ADDRS H if the affected disk drive is deselected. The WRT PROT switch of the affected disk drive must be depressed to allow data to be written on any drive that has been write protected. Note that a disk drive is write protected by programming the write protect function or by depressing WRT PROT switch on the RK05 (Table 11-13).

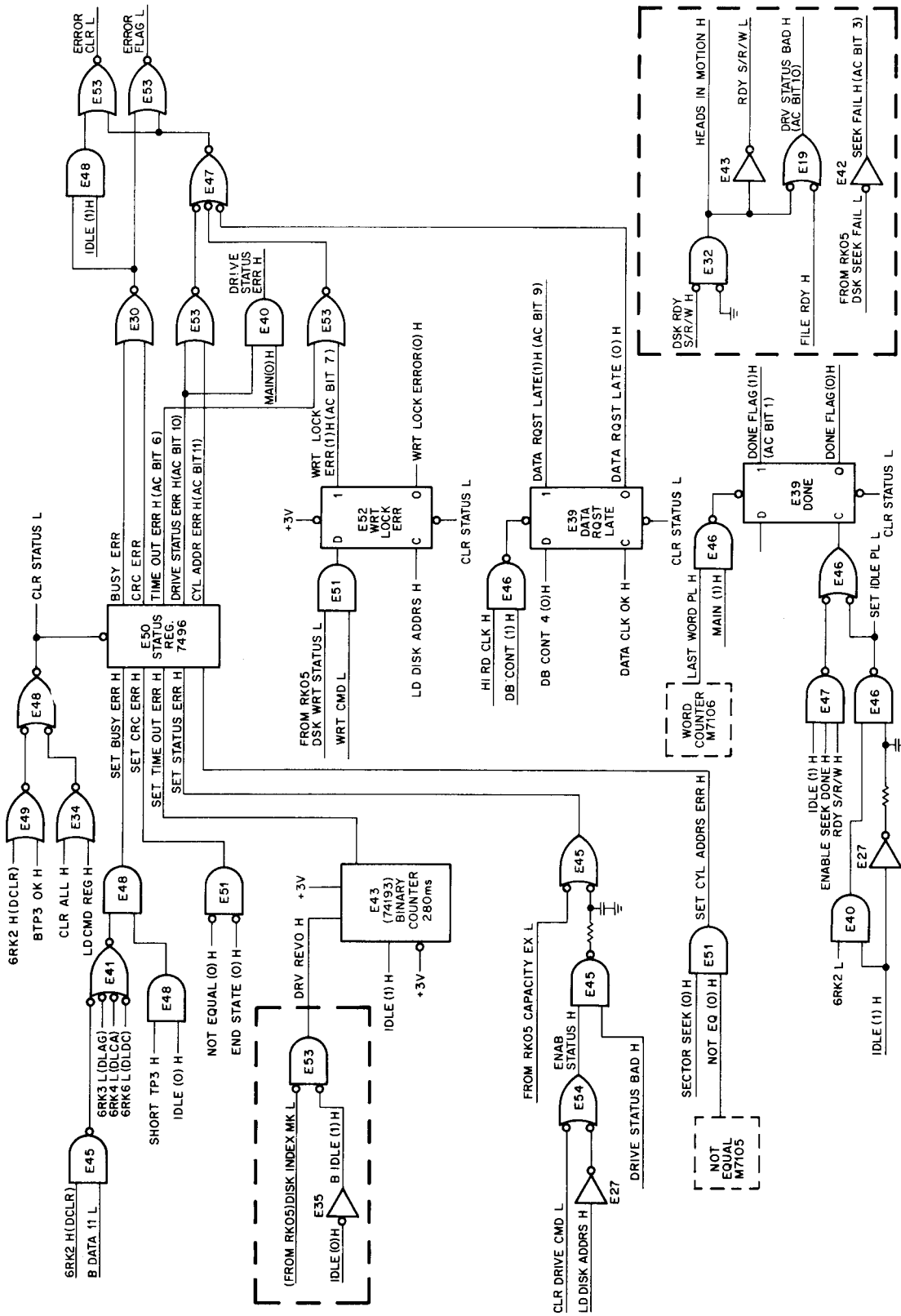


Figure 11-21 Status Register

11.15.4.8 CRC ERROR – The CRC ERROR (AC8) bit is set if the CRC character read from the disk drive does not equal the CRC computed by the CRC Register during a read operation. The CRC character read from the disk during the CRC state is compared bit-by-bit with the CRC character computed by the RK8-E (Figure 11-12). If the CRC characters are not equal, NOT EQUAL (0) H is asserted low and when the Major States Register enters the END state the CRC ERROR bit is set.

11.15.4.9 DATA REQUEST LATE – DATA REQUEST LATE (AC9) is set if the processor does not respond to a BRK RQST within 22.5 μs. If the processor does not respond in time, the Data Buffer Register is emptied during a write operation or filled during a read operation. This causes one or more data words to be lost. The DATA RQST LATE flip-flop (Figure 11-21) is set by one of the following:

a. HI RD CLK and DB CONT 1 (H) during a read operation. This condition indicates the Data Buffer Register is full and there is no room for new data.

b. DATA CLK OK H and DB CONT 4 (0) H during a write operation. This condition indicates the Data Buffer Register is empty and there is no data to be written on the disk cartridge.

11.15.4.10 DRIVE STATUS ERROR – DRIVE STATUS ERROR (AC10) is set if DRIVE STATUS BAD H is asserted and the program initiates a load disk address (DLAG), attempts a clear drive command operation, or if the disk capacity is exceeded (disk address greater than 312_8). The conditions that cause DRIVE STATUS BAD H to be asserted are given in Table 11-12, bit 10.

11.15.4.11 CYLINDER ADDRESS ERROR – CYLINDER ADDRESS ERROR (AC11) is set if the HEADER word of a sector does not agree with the cylinder address sent to the disk drive. The HEADER word is read from a sector during the HEADER C major state and compared with the cylinder address in the CRC Register. If the HEADER word and the cylinder address in the CRC Register (Figure 11-12) are NOT EQUAL, CYLINDER ADDRS ERR is set and the TRANSFER DONE flag sets.

11.15.5 ERROR Flag

The ERROR flag is asserted by any of the following errors, which also set bits in the Status Register.

a. BUSY ERR
b. CRC ERR
c. TIME OUT ERR
d. DRIVE STATUS ERR
e. CYL ADDRS ERR

If the ERROR flag is set and the DSKP instruction is executed by the program, the SKIP line is grounded. This causes the program to skip an instruction (Figure 11-19). If the INTERRUPT ENABLE bit in the Command Register (bits) is a 1 and the ERROR flag is set, the program will be interrupted by an INT RQST (Figure 11-19).

11.15.6 Sector Address Comparator

The sector address comparator (Figure 11-22) compares the address in the Surface Sector Register with the sector address read from the selected disk drive during the HEADER C major state. The comparator is a 7485 IC (see Section 7 for truth table, pin locator, and logic diagram) that asserts SECTOR EQ H when the two 4-bit inputs are equal.

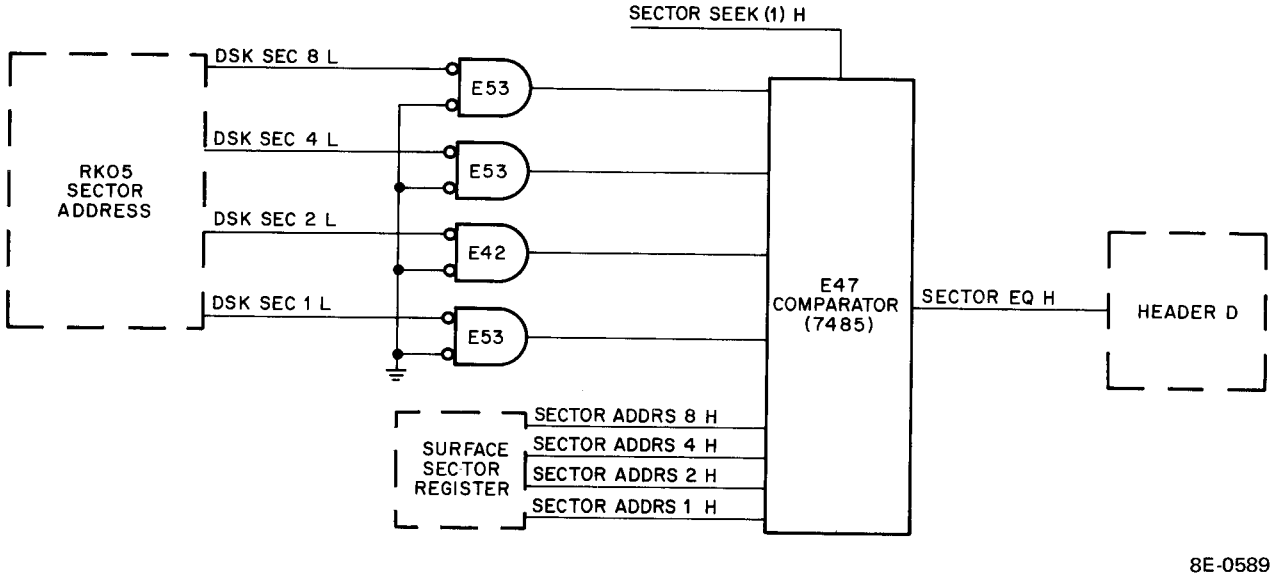


Figure 11-22 Sector Address Comparator

11.15.7 Data Break Control Logic

The data break control logic (Figure 11-23 and 11-24) enables the RK8-E to assume control of the CPU Major Register gating and directly address via the Current Address Register, memory locations associated with a data transfer. The priority network compares the priority of the RK8-E with other peripherals making BRK RQST at the same time. If the RK8-E has the highest priority, the controller asserts signals indicating the RK8-E has accepted the request at INT STROBE time. When the RK8-E asserts BREAK, the single cycle data break is started, a data word is transferred to or from the address indicated by the Current Address Register. If the transfer is from the RK05 to memory, the data is applied to the Data Bus (DATA0–DATA11) by the transfer control logic. Data transfers from memory to the RK05 are taken from the MD lines (MD00–MD11) and transferred to the RK05 via the Data Buffer Register.

11.15.7.1 Current Address Register – The Current Address Register (Figure 11-23) and the EMA bits (EMA0–EMA2) are used to select a location in memory to be used in a data transfer. The Current Address Register is loaded with the address of the first memory location to be used in a data transfer when the 6RK4 (DLCA) instruction is executed by the program. The RK8-E must be in the IDLE state (control not busy) when the CA Register is loaded. DATA ENABLE (1) H (Figure 11-24) is asserted at TP4 time to increment the CA Register and sequentially select locations in memory for data transfers. The contents of the CA Register are applied to the OMNIBUS when MAK (1) H is asserted during a data break.

The CA Register consists of three DEC 74161 ICs (see Section 7 for timing diagram, logic diagram, and pin locations). The DEC 74161 IC is a presetable binary counter with clock input for incrementing. Note that the clock input and the control input (load) must be asserted to load the CA Register.

The EMA bits (EMA0–EMA2) from bits 6 through 8 of the Command Register are applied to the OMNIBUS when DATA ENAB (1) H is asserted by the control logic (Figure 11-24) to select a memory field (0–7). The EMA bits are not incremented and the Command Register must be changed by the program to change memory fields.

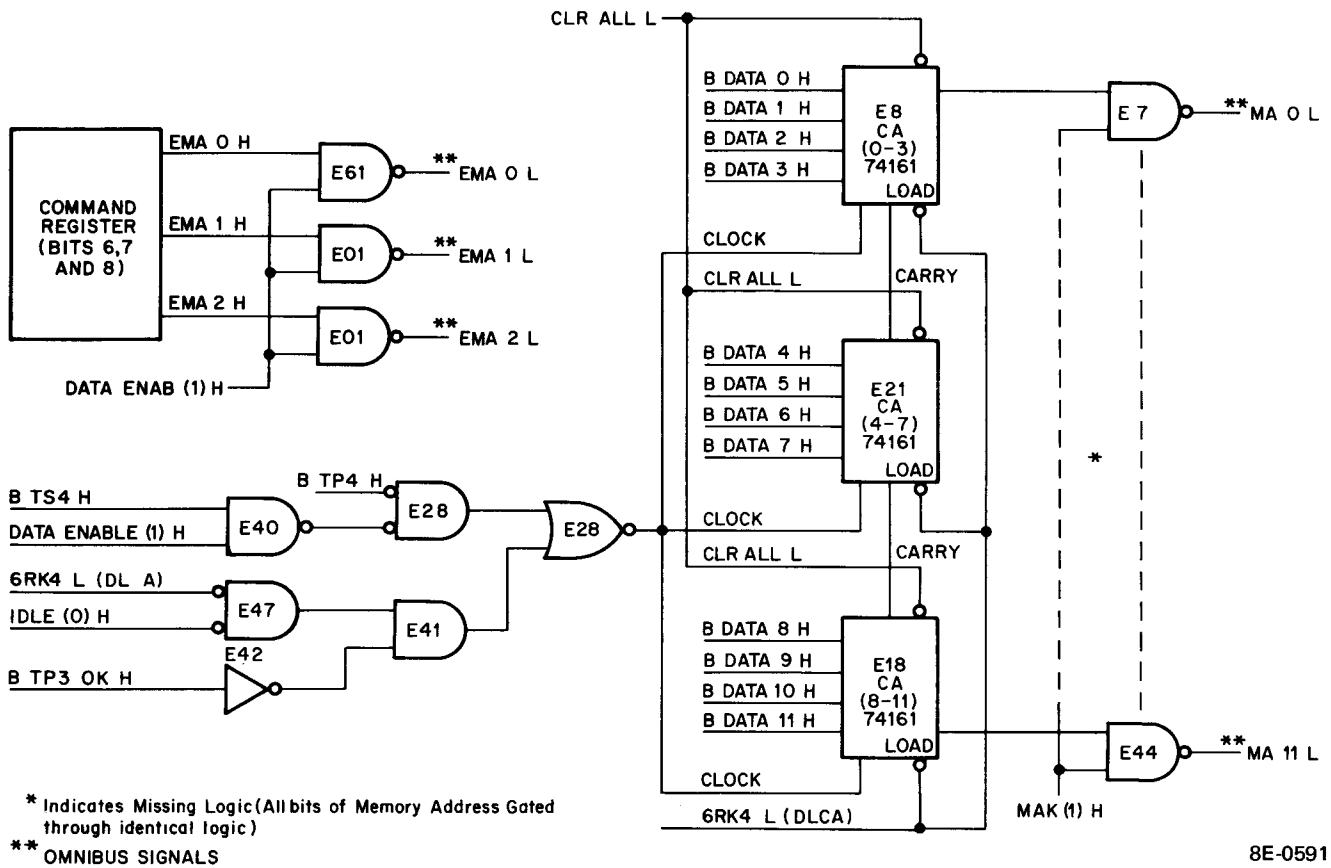


Figure 11-23 Current Address Register

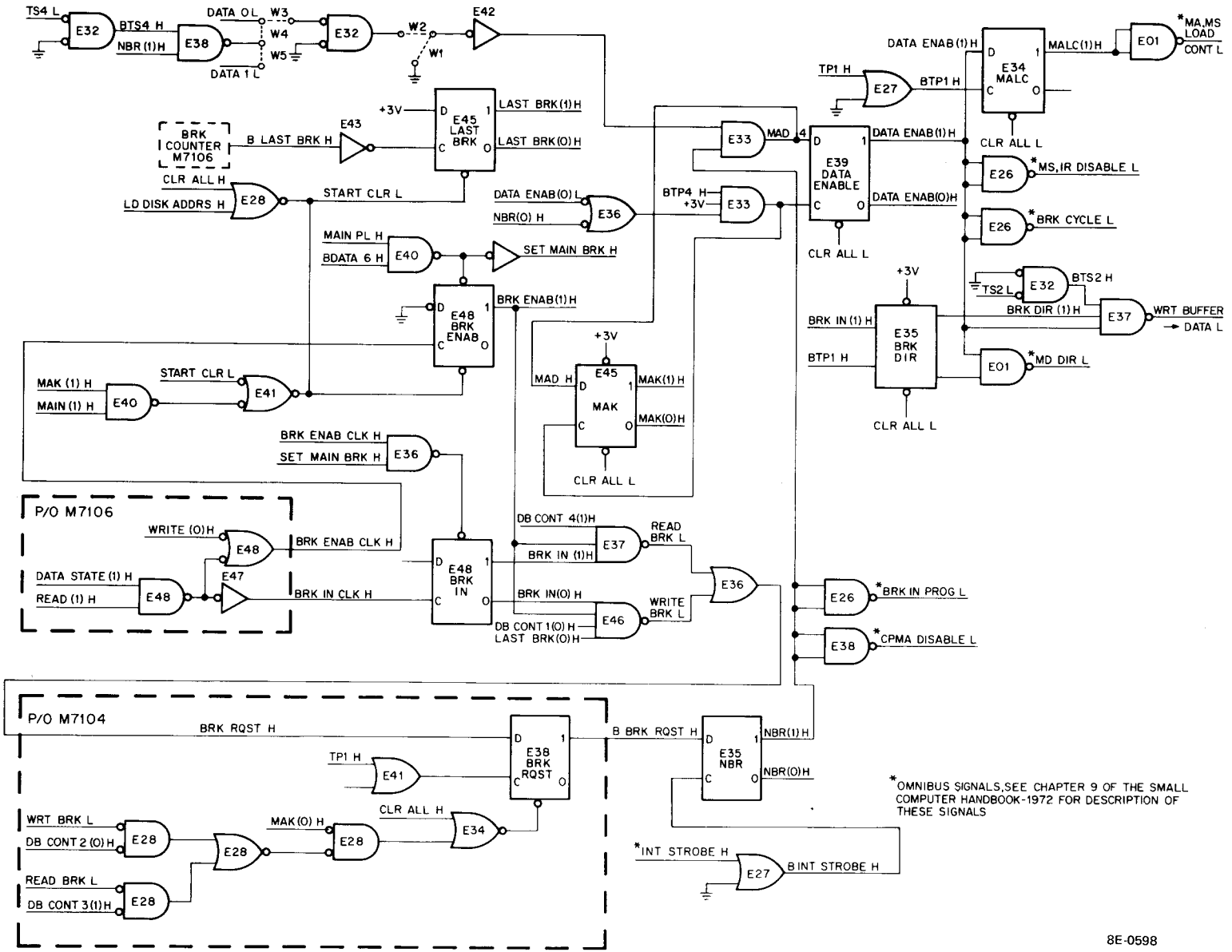


Figure 11-24 Single Cycle Data Break Control Logic

11.15.7.2 Data Transfer Control Logic – The data transfer control logic (Figure 11-24) determines the direction and type of data transfer. The BRK ENAB flip-flop is set immediately if a write operation is initiated or when the Major States Register enters the DATA state during read operations. BRK ENAB (1) H supplies an input to E37 and E46 to allow a BRK RQST if other conditions are met. BRK IN is set during read operations and cleared during write operation to enable either E37 during read breaks or E46 during write breaks. During read operations, E37 is enabled by DB CONT4 (1) H and BRK IN (1) H to assert READ BRK L and initiate a BRK RQST at TP1 time. DB CONT4 (1) H is asserted (high) when DB4 in the Data Buffer Register is full. A new BRK RQST is made each time DB4 is filled until the data transfer is complete. BRK RQST is cleared during a read break when MAK (0) H is low if DB3 in Data Buffer Register is empty. Note that DB CONT3 (1) H is low when DB3 is empty which enables E28 and allows BRK RQST to clear at TP4 time if the MAK flip-flop is set. If DB3 is full, BRK RQST is not cleared and a new break cycle is started to transfer new data. The data in DB3 is transferred to DB4 as soon as DB4 is empty; thus, the data in DB3 is in DB4 when the next break cycle starts.

During write operations, E46 is enabled to assert WRT BRK L if BRK IN is cleared, BRK EN is set, LAST BRK (0) H is asserted, and DB1 in the Data Buffer Register is empty. DB CONT1 (0) H is true to enable E46 and make a BRK RQST at TP1 time when DB1 is empty. BRK RQST is cleared at TP4 time if MAK is set to negate MAK (0) H (low) and DB2 is full. If DB2 is empty, DB CONT2 (0) H disables E28 and the BRK RQST flip-flop is not cleared. If DB2 is empty, the data in DB1 is transferred immediately to DB2 and a new break cycle is started to fill DB1 if the RK8-E has the highest priority.

The data transfer control logic tries to keep the Data Buffer Register full during a write operation and empty during a read operation via the single cycle data break.

11.15.7.3 Priority Logic – The RK8-E must have the highest priority to allow a break cycle when a BRK RQST is made. DISK PRIORITY H (Figure 11-24) is asserted by a ground (W1 installed) on the input of E42 if the RK8-E is assigned the highest priority (0). DATA 0 L (highest priority) or DATA 1 L are asserted by the output of E38 when the NBR flip-flop is set to prevent other peripherals from doing a break cycle when the RK8-E has priority. If priority 1 is selected for the RK8-E, jumper W3 is installed. When a peripheral with priority 0 makes a BRK RQST, E32 is enabled to supply a high to the input of E42. A high on E42 negates PRIORITY H and the RK8-E must wait until DATA 0 L is negated by the peripheral with the highest priority.

Thus, when DISK PRIORITY H is asserted and a BRK RQST is made (NBR is set), a break cycle is started. NBR is set at INT STROBE time if BRK RQST is set. When NBR sets, CPMA DISABLE L and BRK IN PROG L are asserted on the OMNIBUS to start a break cycle. The OMNIBUS signals are explained in Chapter 10 of the *Small Computer Handbook – 1973.*

11.15.7.4 CPU Control Logic – The CPU control signals are asserted by the RK8-E at TP4 time if DISK PRIORITY H is asserted. DATA ENABLE is set at TP4 time to assert BRK CYCLE L and MSIR DISABLE L (see Chapter 10 of the *Small Computer Handbook – 1973* for description of signals). BRK DIR is set during read breaks by BRK IN (1) H to assert MD DIR L. MD DIR L is asserted to allow data to be transferred from memory to the RK8-E (write) and is negated to transfer data from the RK8-E to memory.

The next TP1 pulse after DATA ENABLE is set causes the MAK flip-flop to set and assert MA, MS LOAD CONT L. This inhibits loading of the MA, MS Registers by the processor and allows the contents of the CA Register applied to the MA lines to select a location in memory for this data transfer.

MAK is set at the same time as DATA ENABLE. The clear side of MAK is used to clear BRK RQST at the end of a BRK cycle if DB2 is full during write operations or DB3 is empty during read operations.

The LAST BRK flip-flop is set and B LAST BRK H from the break counter is asserted when the data transfer is completed. The zero side of LAST BRK disables E46 and removes WRITE BRK L from the BRK RQST flip-flop to stop write breaks. READ BRK L is negated when E37 is disabled by the loss of DB CONT4 (1) H to stop read breaks.

The data break control logic is cleared when the load disk address (DLAG) instruction is executed by the program or by CLR ALL L which is asserted when the DCLR instruction is executed.

11.15.8 Data Buffer Register and Control Logic

The Data Buffer Register (Figure 11-25) and its associated control logic (Figure 11-26) has the following functions:

a. During read operations, serial data is shifted into DB1 by the RD CLK pulses and transferred to DB4 via DB2 and DB3 as 12-bit parallel words. The 12-bit words are then transferred to memory by the single cycle data break. The single cycle data break control logic tries to keep the Data Buffer Register empty so that there is space for temporary storage of data transferred from the disk.

b. During write operations, a 12-bit parallel word is transferred from memory to DB1. The 12-bit word is transferred to DB4 via DB2 and DB3. The 12-bit word is shifted out of DB4 by the WRT BUFF SHFT L signal. The output of DB4 is supplied to the write control logic as 12 bits of serial data to be written on the disk between clock pulses (Figure 11-2).

c. During maintenance operations, the contents of CRC Register, Command Register, or the Surface/Sector Register are shifted into DB4 by the LO MAIN SHFT L pulse. The DMAN instruction is used to generate the LO MAIN SHFT L signal (Table 11-14). The contents of DB4 are transferred to the AC via the Data Bus by the DMAN instruction. Thus, the program can read and evaluate the contents of the Command Register, CRC Register, and Surface/Sector Register during maintenance operations or error check routines. The flow diagram in Figure 11-15 illustrates these maintenance operations, and Table 11-14 gives the AC bit requirements to accomplish the maintenance operations.

11.15.8.1 Data Buffer Register Control Logic – The Data Buffer Register control logic (Figure 11-26) provides control signals to the Data Buffer Register (Figure 11-25). The DB control logic consists of a Control Register and a DB clock with gating logic to aid in the control operations. The Control Register consists of four J-K master slave flip-flops with clock inputs. The unique features of these flip-flops are: 1) a clock pulse will not cause any transition in the flip-flop if neither the J or K inputs are enabled during the clock pulse and 2) if both the J and K inputs are enabled during the clock pulse, the flip-flop will complement (change states). The J or K inputs are enabled only when the input is of a state different from the present condition of the flip-flop, i.e., if DB1 is in a 1 state only a 0 state input will cause the flip-flop to change state. When the flip-flops are in a 1 state, the Data Buffer Register associated with that flip-flop is considered to be full, i.e., if DB1 control is in a 1 state, DB1 is full. When the flip-flops are in the 0 state, the registers are considered to be empty.

The DB clock is made up of one 74123 IC (see Volume I, Appendix A for logic diagram and pin locations). This IC is a dual one-shot multivibrator that outputs a pulse of a specified duration each time the input is enabled. The duration of the output pulse is determined by an external capacitor and resistor, i.e., R7 and C38.

DB CLK H out of the first 74123 IC is a 50 ns pulse that is asserted when one of the inputs to E6 are enabled to cause the input to make a high-to-low transition. One of the inputs to E6 is enabled when one of the Data Buffer Control flip-flops is to be loaded. The pulse out of the first 74123 triggers the second 74123 IC and disables the input to the first IC, also disabling the 0 → DB4 signal for 150 ns. This allows the completion of a data transfer before a new DB CLK pulse is generated. Without this delay, the Control Register would attempt to load a register before the output of a register has been transferred into another register (i.e., DB2 → DB3) or to the Data Bus (i.e., DB4 → Data Bus). Note that the clock pulse is initiated only when the correct conditions exist to load one of the Data Buffer Registers and is disabled by the clear side of the second IC to allow time for a data transfer (register-to-register or register-to-disk or processor).

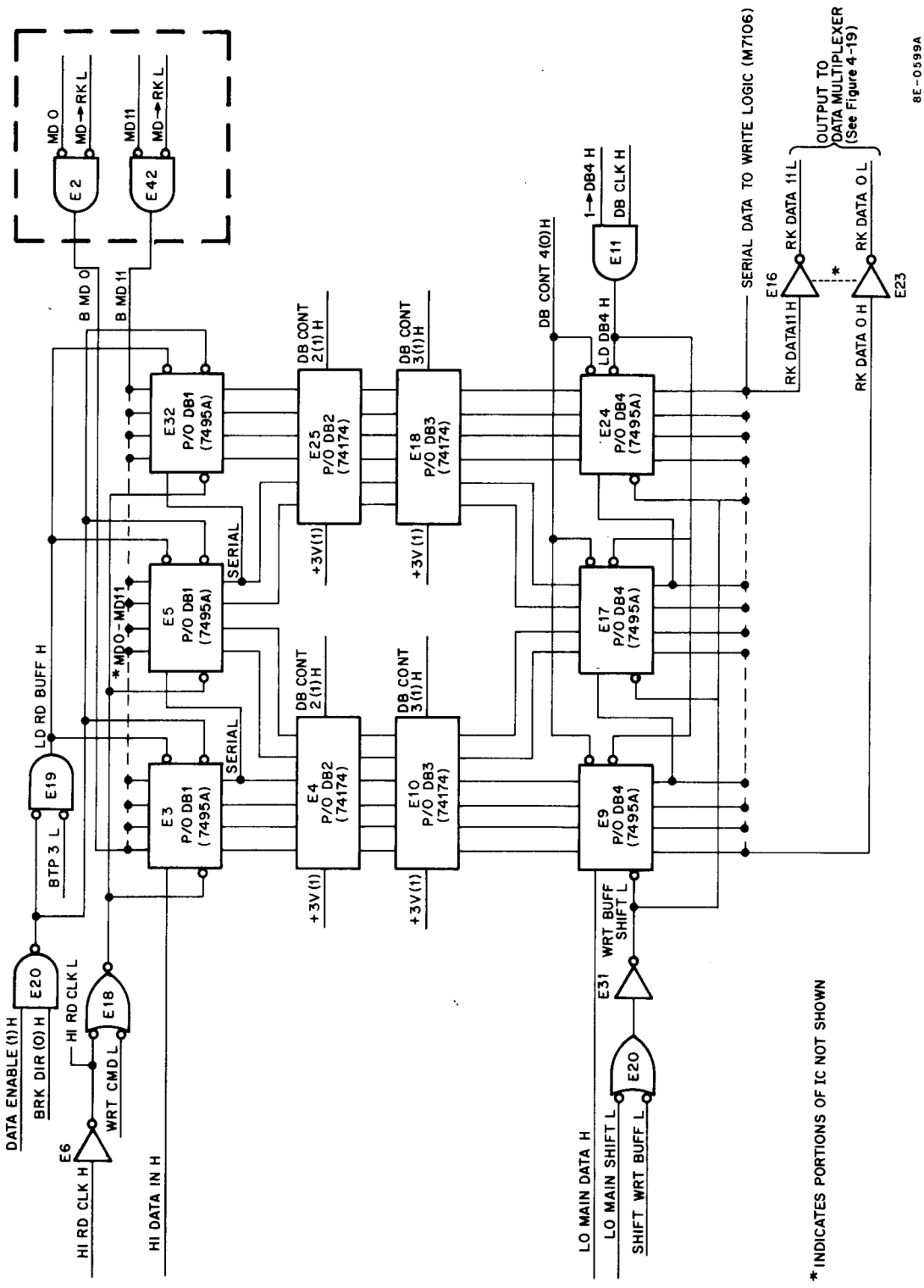


Figure 11-25 Data Buffer Register (sheet 1)

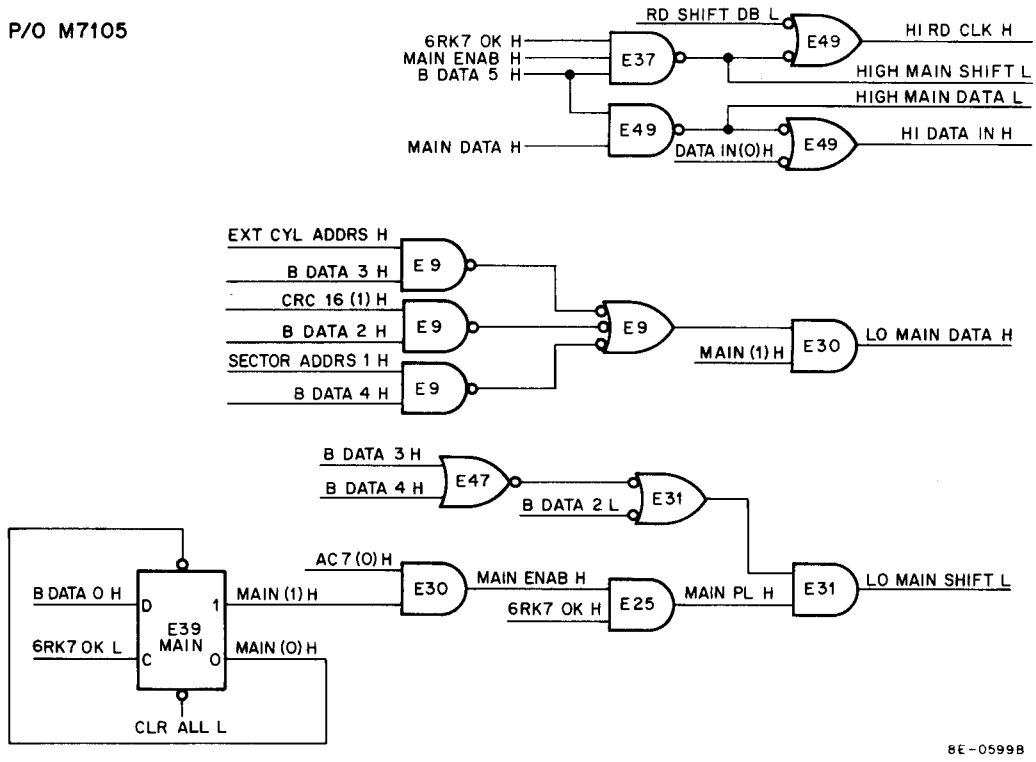


Figure 11-25 Data Buffer Register (sheet 2)

11.15.8.2 Data Buffer Control 1 and Data Buffer 1 – Data Buffer control 1 is used to control Data Buffer Register 1 (Figures 11-25 and 11-26). DB CONT1 is set to a 1 state when DB1 is loaded and remains in a 1 state until the data is transferred to DB2. DB1 is loaded (DB CONT1 goes to a 1 state) during write breaks by data from memory when LD RD BUFFER H is asserted by BRK DIR (0) H and DATA ENABLE (1) H (Figure 11-25). During read operations, DB1 is loaded with serial data so the input to DB CONT1 is not clocked in until 12 bits are read from the disk cartridge. When 12 bits are read and shifted into DB1 by the read clock, 12th BIT OK H is asserted and DB CONT1 goes to a 1 state (DB1 is full).

Note that during maintenance operations MAIN DATA can be shifted into DB1 by the 6RK7 (DMAN) instruction if bit 5 in the AC is a 1. This allows the program to check the Data Buffer Register and control logic.

Data Buffer Register 1 consists of three 7495A ICs (see Volume I, Appendix A for logic diagrams, pin locations, and truth table) connected in series to form a 12-bit register. During read operations, this register is loaded with 12 bits of serial data from the disk cartridge. The output of DB1 is a 12-bit parallel word that is transferred to DB2. DB1 is also loaded with a 12-bit parallel word from memory (write operations) that is transferred to DB2 when DB2 is empty.

11.15.8.3 Data Buffer Control 2 and Data Buffer Register 2 – DB CONT2 is set to a 1 state when DB CONT1 (1) H (DB1 full) and DB CONT2 (0) H (DB2 empty) are asserted. The output of NAND gate E13 (1 → DB2) triggers the 74123 IC and generates a 50 ns clock pulse, which clocks 1 → DB2 H into DB CONT2. Note that DB1 is not transferred to DB2 unless 1 → DB2 is asserted to cause a clock pulse to be generated. This stops a transfer from DB1 to DB2 unless DB2 is empty.

Data Buffer Register 2 consists of two 74174 ICs (see Volume I, Appendix A for logic diagram, truth table, and pin locations) that are connected in series to form a 12-bit register. This register is parallel loaded with 12 bits from DB1 when DB CONT2 is set to a 1 state. The parallel output of DB2 is transferred to DB3 when DB3 is empty.

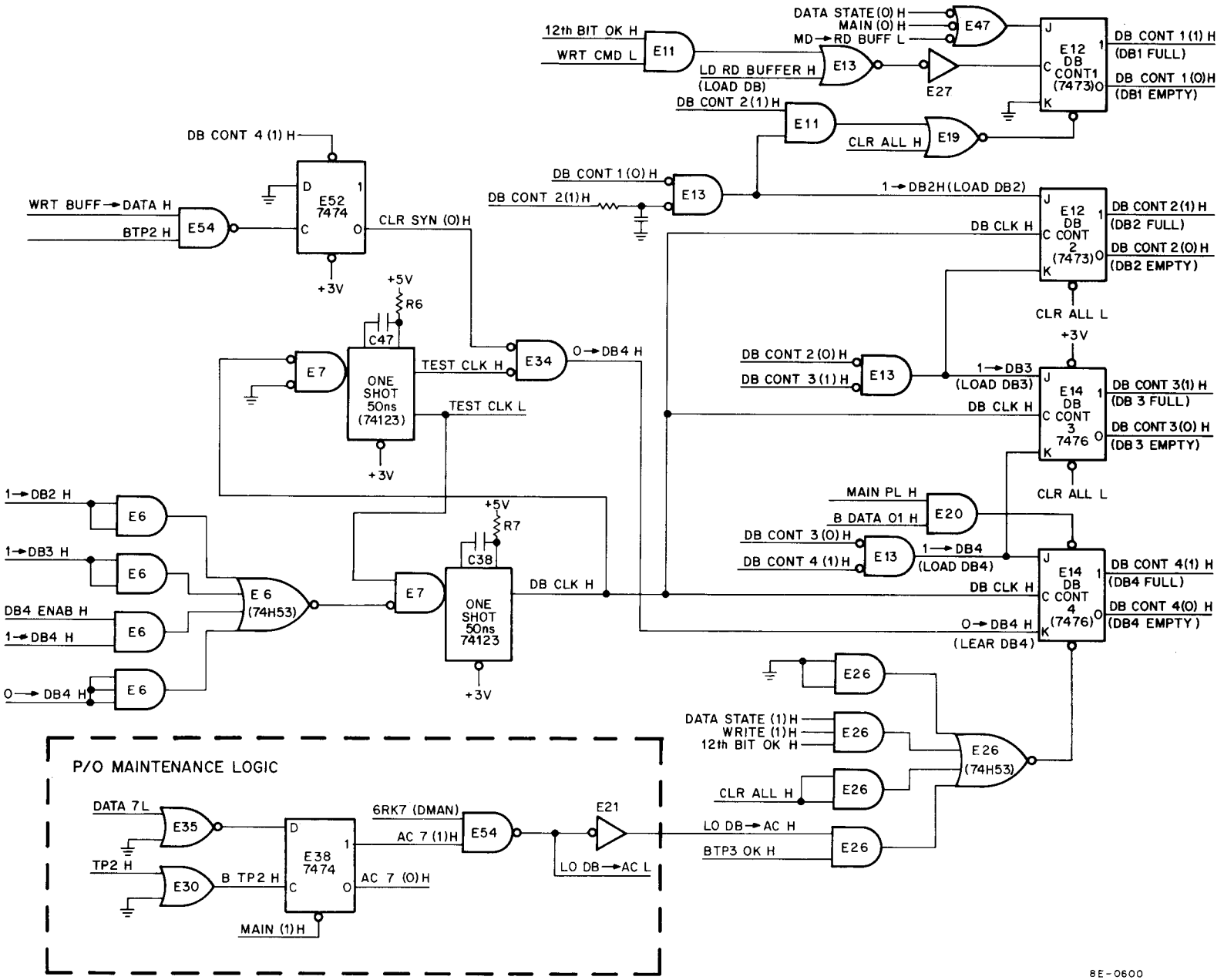


Figure 11-26 Data Buffer Register Control Logic

11.15.8.4 Data Buffer Control 3 and Data Buffer Register 3 – Operation of Data Buffer Control 3 and Data Buffer Register 3 is identical to DB2 CONT and DB2, except that DB3 H is qualified by DB3 (0) and DB2 (1). DB3 is loaded from DB2 when DB2 is full and DB3 is empty. The output of DB3 is transferred to DB4 when DB4 is empty (DB CONT4 in a 0 state) and DB3 is full (DB3 in a 1 state).

11.15.8.5 Data Buffer Control 4 and Data Buffer Register 4 – Data Buffer Control 4 (Figure 11-26) is used to control Data Buffer Register 4 (Figure 11-25). DB4 is loaded with the contents of DB3 if DB CONT3 (1) H (DB3 full) and DB CONT4 (0) H (DB4 empty) are negated to assert 1 → DB4 H. This causes DB CLK H to be asserted and DB4 goes to the 1 state (full).

During write operations, the contents of Data Buffer Register 4 are shifted out to the disk via the write logic (Figure 11-28) on the RK DATA11 line as serial data. WRT BUFF SHFT L is generated by the WRT CLK pulses (Figure 11-28), and shifts the data once for each clock pulse. When 12 bits of data have been shifted out to the disk, E26 is enabled and DB4 ENAB H is negated. This clears DB4 to the 0 state and DB4 can be loaded again from DB3.

During read operations, DB4 receives a 12-bit parallel word from DB3 for transfer to memory via the Data Bus. When WRT BUFF → DATA H is asserted to transfer the contents of DB4 to the Data Bus (DATA0–DATA11), CLR SYN (0) H is asserted to enable NAND gate E34. Signal 0 → DB4 H is asserted if the TEST CLK H pulse out of the 74123 IC is negated and 0 → DB4 returns DB CONT4 to the 0 state when the next DB CLK H pulse occurs. When DB CONT4 goes back to the 0 state, it is ready for new data to be transferred from DB3.

Data Buffer Register 4 consists of 3 7495A ICs (see Volume I, Appendix A for truth table, logic diagram, and pin locations) that are connected in series to form a 12-bit register. The register is loaded with 12 parallel bits from DB3 when DB4 is empty and DB3 is full. During write operations, the 12 bits are shifted out to the disk as serial data. During read operations, a 12-bit parallel word is transferred to memory via the Data Bus.

During maintenance operations, the contents of the Command Register, the CRC Register, and the Surface/Sector Register may be shifted into DB4 of the Data Buffer Register, for transfer to the AC. To accomplish this, the MAIN flip-flop must be set by transferring a 1 from the AC in bit position 1 using the DMAN instruction. This enables the maintenance logic (Figure 11-25) and allows bits from the AC to shift data into DB4. Signals MAIN PL H and B DATA 01 H are used to set DB CONT4 (Figure 11-26) and keep it in the 1 state, which disables transfers from DB3 while maintenance operations are underway. An input to DB4 is supplied by NOR gate E9 and NAND gate E30 as LO MAIN DATA H. When a DMAN instruction is executed by the program, the following events can occur:

a. If bit 3 in the AC is a 1 when the DMAN instruction is executed, bit 11 from the Command Register (EXT CYL ADDRS H) is applied to DB4. Each time the DMAN instruction is executed by the program, if bit 3 in the AC is set, a bit is shifted out of the Command Register and into DB4. When the contents of the Command Register are in DB4 (12 shifts), if the DMAN instruction is executed and bit 7 in the AC is a 1, LO DB → AC L is asserted to transfer the contents of DB4 to the AC via the Data Bus.

b. If bit 2 in the AC is a 1 and the DMAN instruction is executed, the contents of the CRC Register are shifted into DB4. This operation is the same as that listed above for the Command Register. Note that the program must keep track of the number of shifts required to shift all of the bits into DB4. The CRC Register is transferred to the AC with the same instruction and AC bit used for the Command Register.

c. If bit 4 in the AC is a 1 and the DMAN instruction is executed, the contents of the Sector/Surface Register are applied to DB4. This shift and transfer operation is the same as the other maintenance operations.

The MAIN flip-flop must be cleared using the DCLR instruction after maintenance operations are completed.

11.15.9 Output Data Multiplexer

The output data multiplexer (Figure 11-27) selects either the contents of the Status Register or DB4 to be applied to the Data Bus. The output data multiplexer consists of three 8235 ICs (see Volume I, Appendix A for truth table, logic diagram and pin locations) that are controlled by the 6RK5 (DRST) instruction and enable RK DATA L. If LO DB → AC is asserted during maintenance operations or WRT BUFF DATA L is asserted during read operations, RK DATA 0 L through RK DATA 11 L from DB4 are applied to the Data Bus. If the 6RK5 (DRST) instruction is executed by the program, the contents of the Status Register are applied to the Data Bus for transfer to the AC.

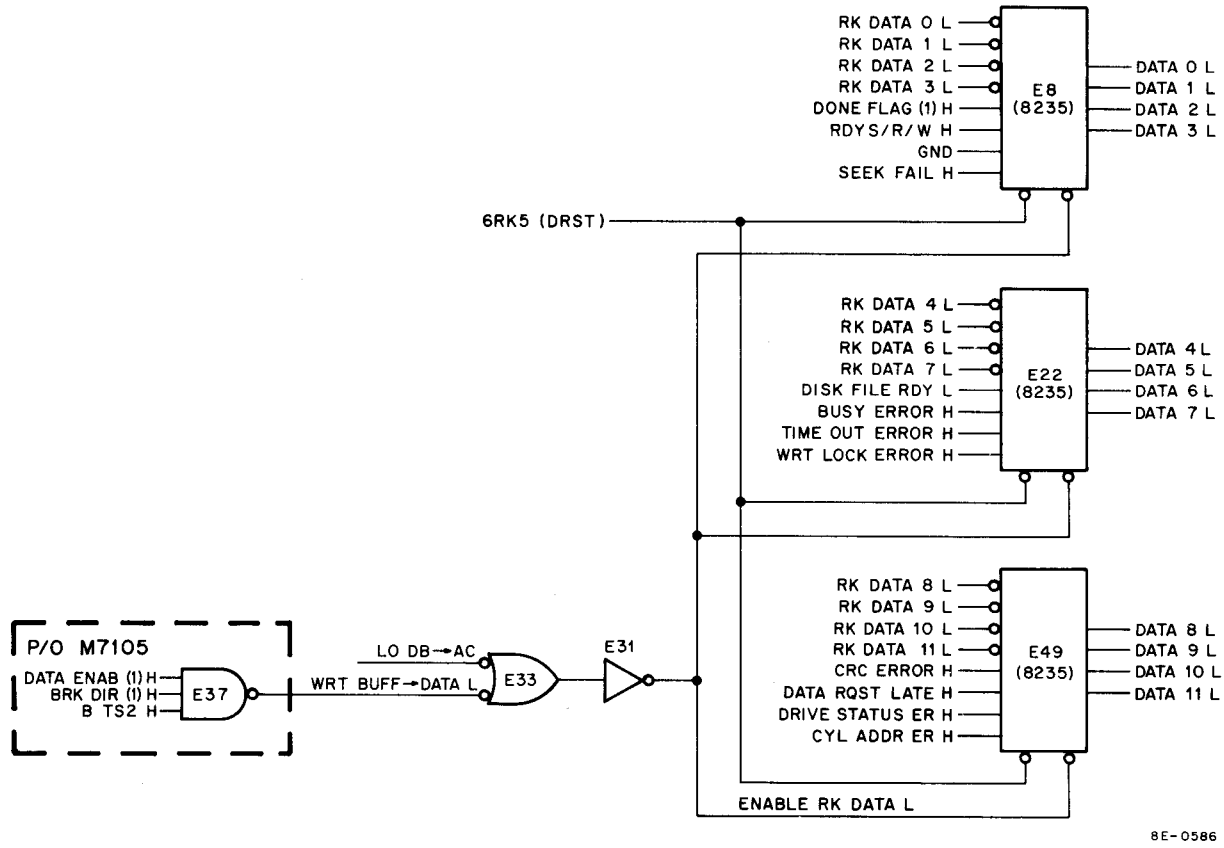


Figure 11-27 Output Data Multiplexer

11.15.10 Read/Write Logic

The read/write (Figure 11-28) logic provides a clock for generation of clock and data pulses to be written on the disk cartridge, the READ DLY logic, and logic to separate RD CLK pulses and READ DATA.

11.15.10.1 Write Clock – The write clock is a 2.88 MHz crystal-controlled oscillator that generates the WRT CLK pulses. When the WRITE flip-flop is set during SK/CHK/WRT or SK/WRT operations, the output of the write clock is enabled to clock E41. The set side of the E41 flip-flop is tied to the data input so that E41 is set and cleared on alternate clock pulses. This enables a NAND gate for WRT CLK pulses when E41 is set and a NAND gate for WRT DATA pulses when E41 is cleared. Thus, WRT CLK pulses and WRT DATA pulses are applied as an output to the RK05 from NOR gate E27. Note that the data pulses occur between clock pulses and a bit cell (Figure 11-2), and are written on the disk cartridge in this manner. The CRC bits (CRC 16 (1) H) from the CRC Register (during CRC state) and the SYNC bit (at end of write delay) are applied to E27 as data pulses to be written on the RK05 between WRT CLK pulses.

During the DATA state, the WRT CLK pulses are used to generate WRT SHFT CRC H, which is used to compute the CRC character (Paragraph 11.15.11).

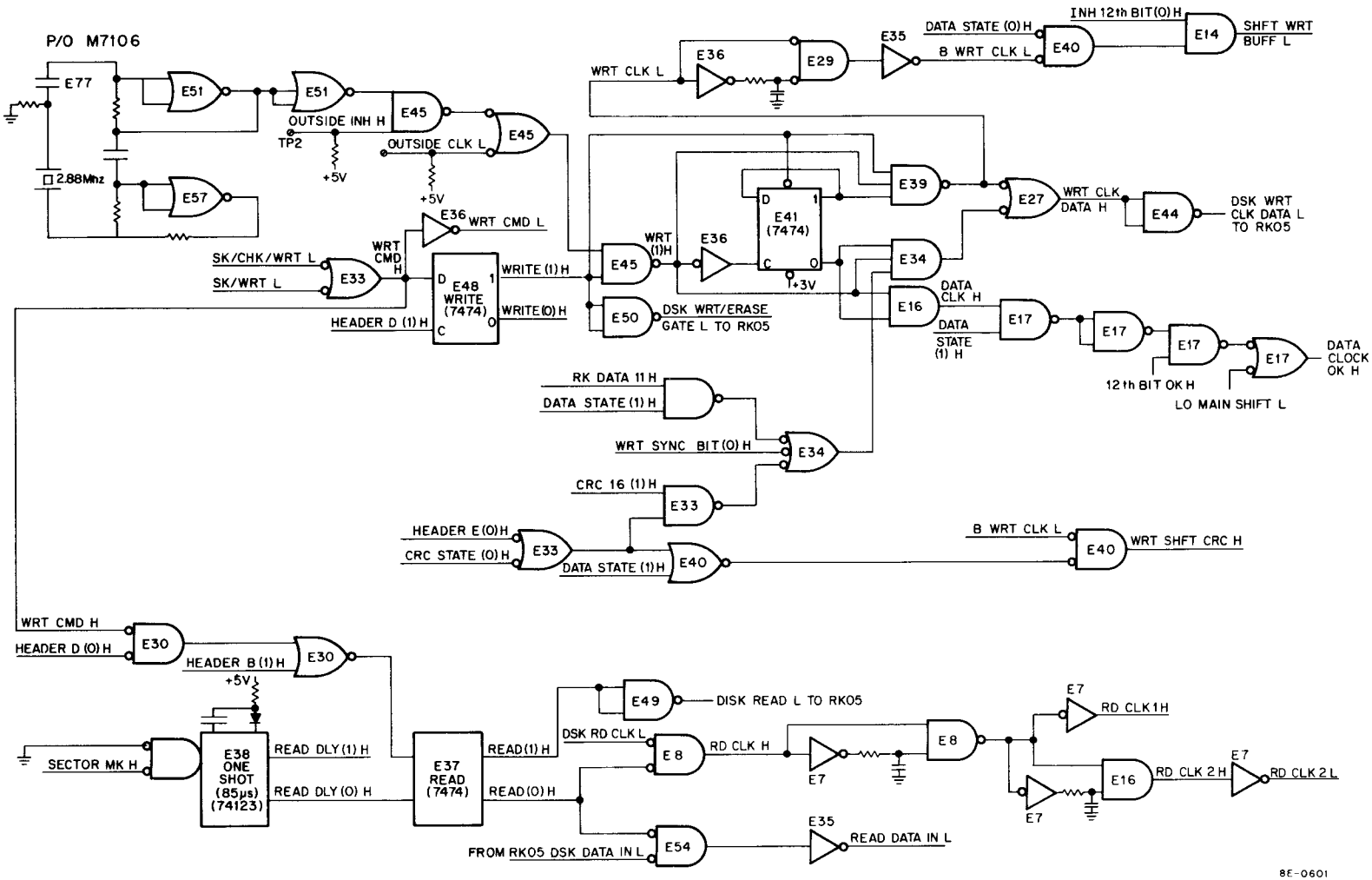


Figure 11-28 Read/Write Logic

11.15.10.2 Read Delay – The READ DLY is a 74123 IC that delays the setting of the READ flip-flop, and the read operation for 85 μs. This allows the controller to wait for the SYNC bit before the Major States Register advances to the HEADER E major state.

The 74123 is a one-shot multivibrator that is triggered when SECTOR MK H makes a low to high transition and outputs of 85 μs READ DLY pulse. After 85 μs, the READ flip-flop is set; after the SYNC bit is read, a read operation is started. The set side of READ is applied to the RK05 as DSK READ L to cause the RK05 to read data. The clear side of READ enables gates to allow RD CLK H and READ DATA IN L pulses to be applied to the RK8-E Data Buffer Register and control logic.

11.15.11 CRC Register

The CRC Register (Figure 11-29) is used to store the disk address and compute a CRC character during read and write operations. The CRC character is computed during write operations and written on the disk cartridge at the end of the data. During read operations, a CRC character is computed and compared with the CRC character that was written at the end of the data. If the two CRC characters are not equal, the CRC ERROR flag is set.

11.15.11.1 Disk Address – The CRC Register (Figure 11-29) is loaded with the 8-bit disk address when the DLDC instruction is executed by the program to assert LD DISK ADDRS H. The two 7496 ICs receive 7 bits (DATA0–DATA6) from the AC and one bit from Bit 11 (EXT CYL ADDRS H) of the Command Register. The disk address bits are applied to the RK05 Disk Drive during the STROBE major state (Figure 11-31) to select a cylinder and surface on the selected disk drive.

The CRC Register stores the disk address until the Major States Register enters the DATA state. At this time, the CRC Register is cleared by DATA STATE (0) H, which is negated (low). The CRC Register is also cleared by the 6RK3 (DCLR) instruction if it is executed by the program.

Note that the Load Disk Address instruction loads the Surface/Sector Register (Figure 11-29) at the same time the CRC Register is loaded.

During the HEADER C major state, the HEADER word is read from the selected drive as DATA IN H and applied to Exclusive-OR gate E24 (Figure 11-29). RD CLK 1 L asserts SHFT CRC H and shifts the contents of the CRC Register out to E24. Thus, the contents of the CRC Register (specified disk address) and the HEADER word read from the disk are compared bit-by-bit. If any bits are different, NOT EQUAL is set by the output of the Exclusive-OR (E24) and the CYLINDER ADDRESS ERROR flag is set (Figure 11-21).

The CRC Register contains the disk address specified by the program until the Major States Register moves to the DATA state. If CYLINDER ADDRESS ERROR is set, the TRANSFER DONE flag sets and the drive that produced the error must be recalibrated.

The disk address may be transferred to the AC for evaluation by the program using the DMAN instruction. When the disk address is transferred, the contents of the CRC Register are shifted out on CRC 16 (1) H to DB4 of the Data Buffer Register (Figure 11-25). Signal MAIN PL is asserted each time the DMAN instruction is executed by the program to shift the CRC Register one position and transfer one bit of the CRC Register to DB4. Note that AC bit 02 must be a 1 to enable the MAIN PL and assert CRC MAIN SHFT L. The program must keep track of the number of shifts and determine when to transfer DB4 to the AC.

Note that when the control is in any state except the DATA state, the Exclusive-OR gates for CRC 2 and CRC 15 have a ground on one input. The ground causes these gates to have an output that is the same as the input, which allows the contents of the CRC Register to be shifted and compared with the CRC DATA H input.

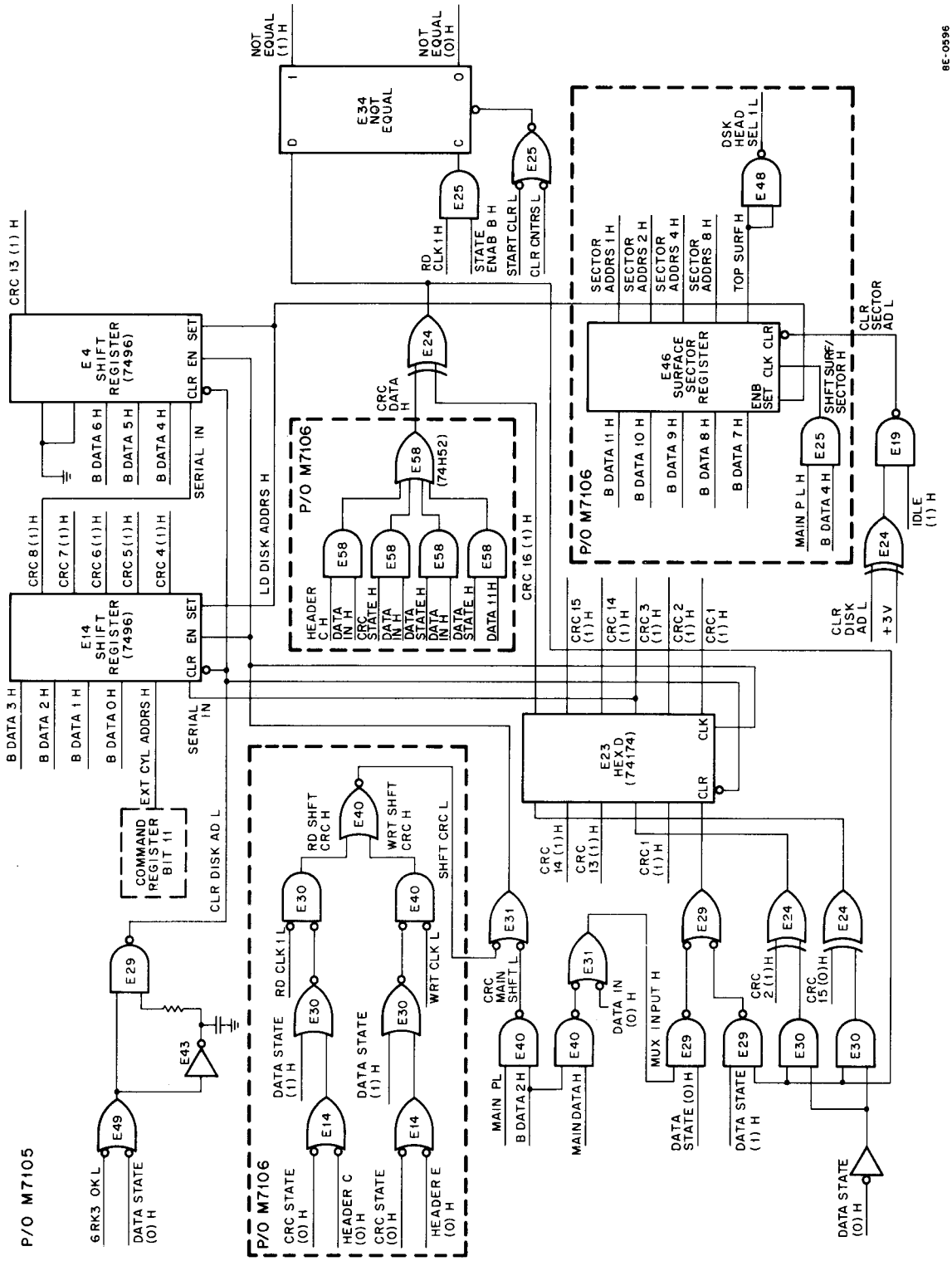


Figure 11-29 CRC and Surface Sector Register

The Exclusive-OR gates for CRC 2 and CRC 15 are used in the computation of the CRC character (Paragraph 11.15.11.2).

11.15.11.2 CRC Character Computation – To generate a CRC word, the block of data is treated as a number 3072 bits long which is divided (modulo 2) by a polynominal $X^{16} + X^{15} + X^2 + 1$. This division being shift and subtract (modulo 2) is accomplished by shifting the CRC Register and Exclusively ORing CRC 2, CRC 15, and CRC 16 (Figure 11-30) as follows:

a. The CRC Register is cleared at the beginning of the DATA state.

b. The CRC Register is shifted one bit position each time a bit is read or written by WRT CLK L or RD DLK 1 L.

c. The bit, which is read or written, is compared with CRC 16 (Exclusively ORed) and the result is Exclusively ORed with CRC 2 and CRC 15.

Using this method, a CRC character is generated for each block of data (256 words) that is written on or read from tape.

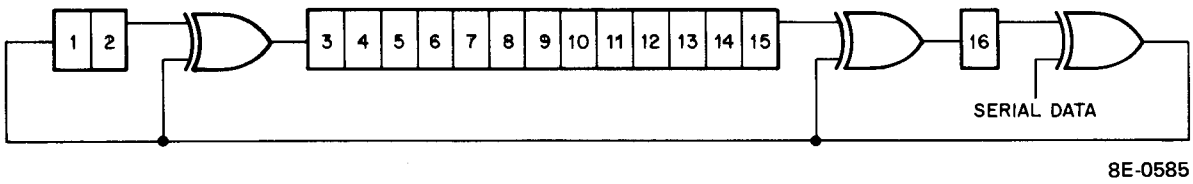


Figure 11-30 CRC Computation Block Diagram

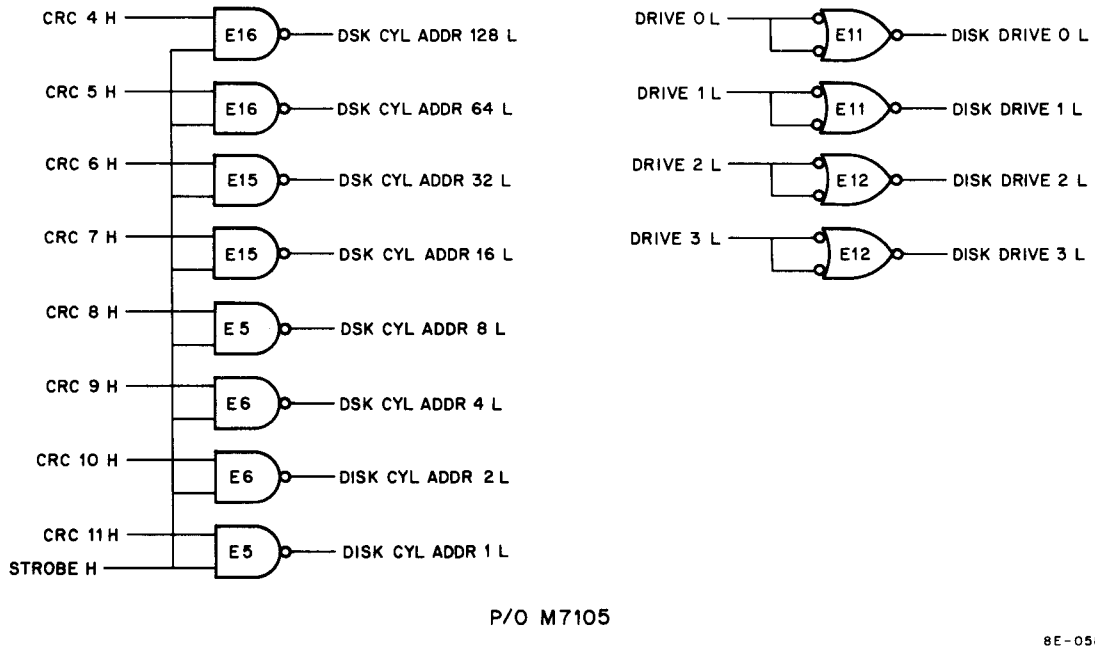


Figure 11-31 Disk Address Output Buffers

11.15.11.3 CRC Character Check – The CRC character that is computed for each block of data during a write operation is written on the disk cartridge after the data during the CRC state. This is accomplished by shifting the contents of the CRC Register out to the disk drive via the read/write logic (Figure 11-28). During the CRC state, the WRT CLK pulse is used to shift the contents of the CRC Register.

During read operations, a CRC is computed as explained above and when the control moves to the CRC major state, the CRC character written on the disk is read. DATA IN H is enabled by CRC STATE H (Figure 11-29) and applied to E24 Exclusive-OR gate. As the CRC character is read from the disk the CRC Register is shifted by RD CLK 1 H and a bit-by-bit comparison is made of the two CRC characters.

If any of the bits are different the output of the Exclusive-OR (E24) sets the NOT EQUAL flip-flop. If NOT EQUAL is set, the CRC ERROR flag sets during the END state (Figure 11-21).

The CRC character can be checked by the program using the DMAN instruction the same way the disk address was checked (Paragraph 11.15.11.1).

11.15.12 Major States

The operation of the Major States Register (Figure 11-32) and the determination of the disk format is discussed in Paragraph 11.14.7. The detailed logic is shown so that the reader can see all the signals required to enter each major state.

11.15.13 RK8-E Counters

The RK8-E counters (Figure 11-33) are used to count the bits and words in a data transfer and keep track of the number of data break cycles.

11.15.13.1 12-Bit Counter – The 12-bit counter (Figure 11-33) consists of 74161 IC (see Section 7 for truth table, timing diagram, and pin locations) used as a binary counter. The 12-bit counter is incremented by RD CLK 2 L (read) or WRT CLK L each time a bit is read or written. When 12 bits have been read or written, 12TH CARRY H is asserted to indicate a 12-bit word has been read or written. Signal 12TH CARRY H increments the word counter each time 12 bits are read or written until 256 or 128 words have been transferred. If HALF BLOCK H is asserted, 12th BIT OK H is negated after 128 words are read or written.

During maintenance operations, HI MAIN SHFT L is asserted if the program executes the DMAN instruction and AC bits 2, 3, or 4 are 1. This allows the program to check the counters and control logic.

The counters are cleared by CLR ALL L or CLR CNTRS L. Signal DATA CLR L is asserted each time the Major States Register advances to the DATA state by a pulse out of the 74123 IC. The 74123 IC (see Volume I, Appendix A for truth table, logic diagram, and pin locations) is a one-shot multivibrator that outputs a pulse each time the DATA state flip-flop sets. The counters are also cleared each time the Major States Register enters the HEADER E major state or when STATE ENAB B H is asserted when the Major States Register enters the CRC or HEADER C major state.

11.15.13.2 Word Counter – The word counter (Figure 11-33) consists of two 74161 ICs (see Section 7 for truth table, timing diagram, and pin locations) that are used as divide by 128 or 256 counters. The word counter is incremented by 12TH CARRY L each time 12 bits of data are read or written. LAST WORD H is asserted after 256 words have been read or written. Signal 128TH WORD H is asserted after 128 words are read or written, and if HALF BLOCK H is asserted (bit 5 in the Command Register must be a 1), the data transfer stops after 128 words. Note that the disk drive continues to read or write zeroes until 256 words are read or written, but this data is not transferred to memory. The TRANSFER DONE flag is not set until LAST WORD H is asserted after 256 words are read or written.

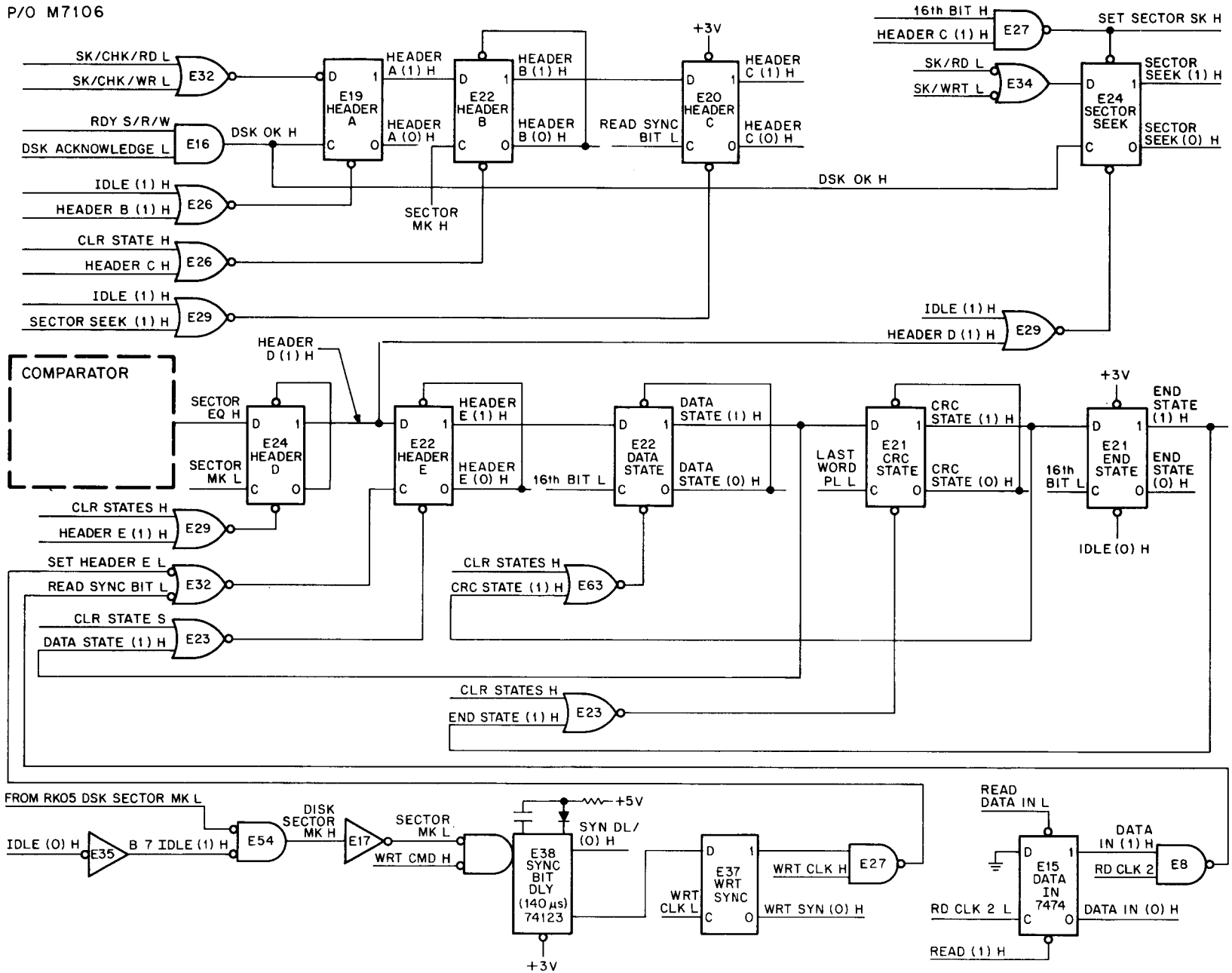


Figure 11-32 Major States Register (sheet 1)

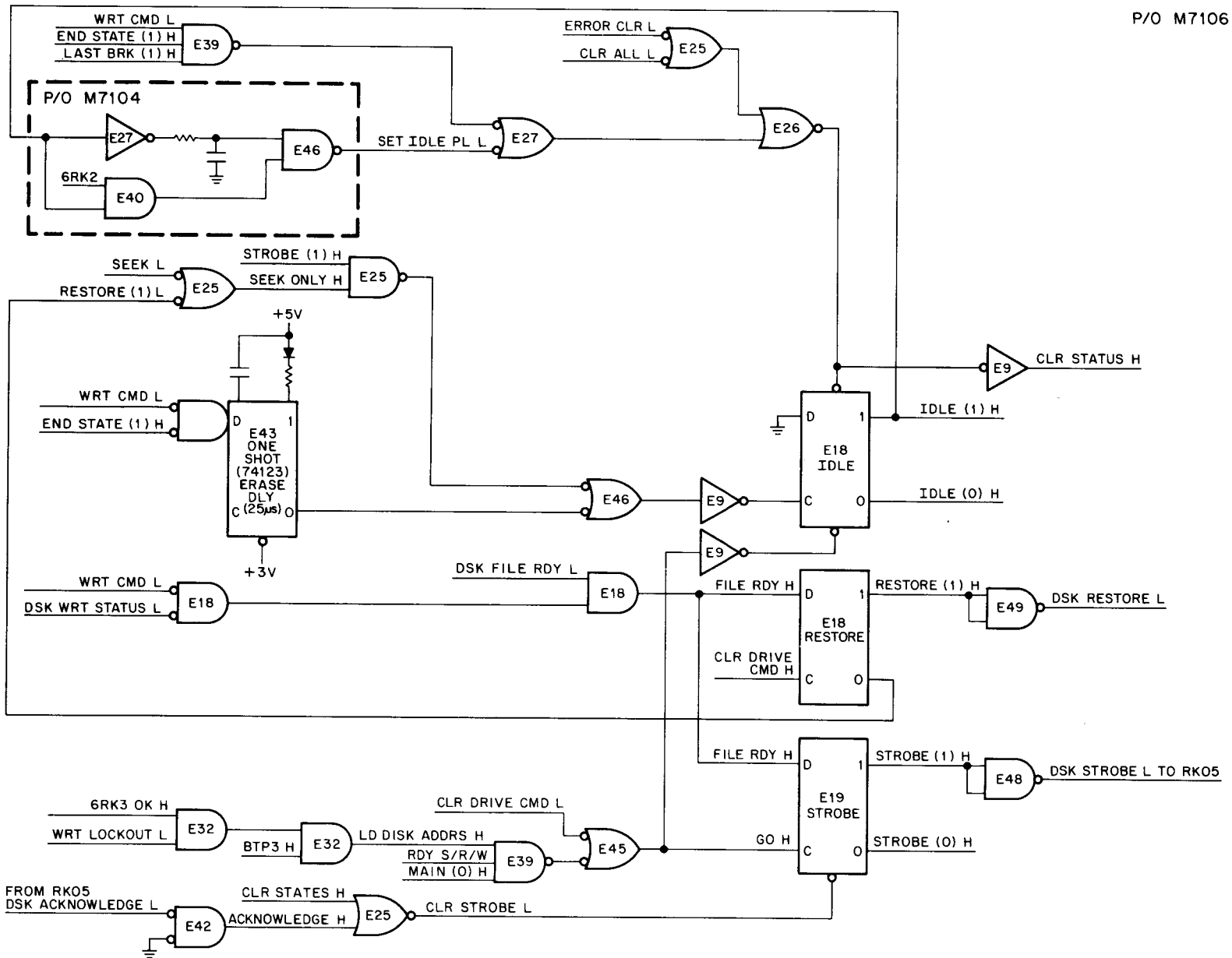


Figure 11-32 Major States Register (sheet 2)

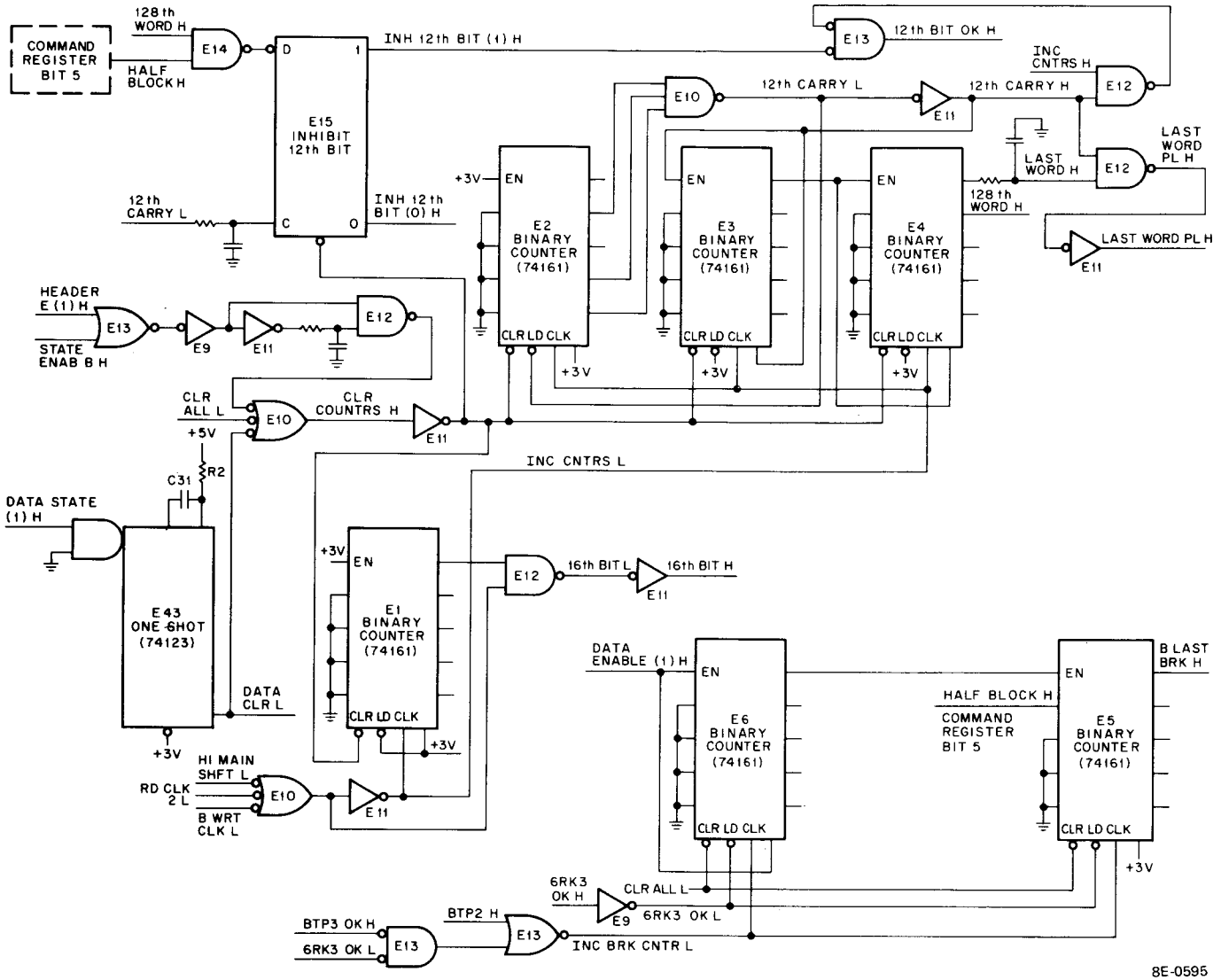


Figure 11-33 RK8-E Counters

11.15.13.3 16-Bit Counter – The 16-bit counter consists of a 74161 IC (see Section 7 for truth table, logic diagram, and pin location) that is used as a binary counter. The 16-bit counter counts the bits in a HEADER word or CRC character as they are read or written. The 16-bit counter is incremented by RD CLK 2 or the WRT CLK, which asserts INC CNTRS H. After 16 bits are read or written, 16TH BIT H is asserted and applied to the control logic.

During maintenance operations, the 16-bit counter is incremented by HI MAIN SHFT L when the DMAN instruction is executed by the program. This allows the program to check the 16-bit counter and associated logic.

11.15.13.4 Break Counter – The break counter (Figure 11-33) consists of two 74161 ICs (see Section 7 for truth table, logic diagram, and pin locations) that are used as a binary counter. The word counter is incremented at TP2 time of a break cycle (DATA ENABLE is set) to count the number of single cycle data breaks. B LAST BRK H is asserted after 256 words have been transferred to or from memory. If HALF BLOCK H is asserted (bit 5 in the Command Register must be a 1), data transfers stop after 128 words have been transferred. Signal B LAST BRK H sets the LAST BRK flip-flop (Figure 11-27) and stops data transfer operations.

SECTION 5 MAINTENANCE

11.16 PREVENTIVE MAINTENANCE

The recommended preventive maintenance should be scheduled on a regular basis to maintain the performance and reliability of the RK8-E and the RK05 Disk Drive system. Preventive maintenance schedules are found in the *RK05 Disk Drive Maintenance Manual* (DEC-00-RK05-DA). RK8-E diagnostics (Paragraph 11.5.1) are provided to test and troubleshoot the RK8-E controller. These diagnostics should be run at regular intervals to verify the operation of the RK8-E.

11.17 CORRECTIVE MAINTENANCE

The following programs may be loaded into memory from the Switch Register and used to monitor RK8-E signals during troubleshooting operations.

NOTE

The program to check the data buffers in Paragraph 11.17.1 should be run first.

11.17.1 Check Data Buffers

This program provides a scope loop to check the Data Buffers by shifting 12 bits of data (1s or 0s) from AC10 into DB1. When DB1 is full, a parallel transfer is made from DB1 to DB2, DB2 to DB3, DB3 to DB4. When DB4 is full, it is read into the AC with the maintenance IOT and stored in memory.

1. Clear disk control logic
2. Enable maintenance logic
3. Enable shift to data buffer 1
4. Set AC10 to equal data
5. Issue maintenance IOT 12 times
6. Read data buffer 4

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA CLL IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	1230	TAD -12	/ DESIRED SHIFT COUNT
7603	3231	DCA COUNT	/ SET UP COUNTER
7604	7330	CML RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7605	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7606	7012	RTR	/
7607	7012	RTR	/
7610	7012	RTR	/ ENABLE CHECK DATA BUFFER (AC05=1)
7611	1232	TAD AC 10 DATA	/ GET DATA TO BE SHIFTED INTO DB1
7612	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7613	2231	ISZ COUNT	/ SHIFTED ONE WORD YET?
7614	5212	JMP -2	/ NO, SHIFT ANOTHER BIT.
7615	7200	CLA	/ YES, CLEAR AC
7616	1233	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7617	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7620	3234	DCA BUF REG	/ STORE DATA WORD
7621	7402	JMP START	/ (DEPOSIT A HLT TO MAKE ONE PASS)
		-12	7630 / 7766
		COUNT	7631 /
		AC10 DATA	7632 / 0000 OR 0002
		K20	7633 / 0020
		BUF REG	7634 /

11.17.2 Checking the Command Register

The following program is used to check the Command Register. The data is obtained from the Switch Register and loaded into the Command Register. It is then shifted into the lower Data Buffer, and read into memory using maintenance IOT instructions.

1. Clear disk control logic
2. Load Command Register with data from the Switch Register
3. Enable maintenance logic
4. Enable shift to lower buffer
5. Set AC03 (check Command Register)
6. Issue maintenance IOT 12 times
7. Read DB4

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA CLL IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	1230	TAD -12	/ DESIRED SHIFT COUNT
7603	3231	DCA COUNT	/ SET-UP COUNTER
7604	7404	OSR	/ OR THE SWITCH REGISTER
7605	6746	DLDC	/ IOT 6746 LOAD COMMAND REGISTER
7606	7330	CLA CLL CML RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7607	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7610	7010	RAR	/ ENABLE SHIFT TO LOWER BUFFER DB4 (AC01=1)
7611	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7612	7012	RTR	/ ENABLE CHECK COMMAND REGISTER
7613	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7614	2231	ISZ COUNT	/ SHIFTED ONE WORD YET?
7615	5213	JMP -2	/ NO, SHIFT ANOTHER BIT
7616	7200	CLA	/ YES, CLEAR AC
7617	1232	TAD K20	/ ENABLE DB4 TO AC TRANSFER AC07=1
7620	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7621	3233	DCA CMD REG	/ STORE WORD
7622	5200	JMP START	/ LOOP OR HALT (HALT=1 PASS)
		-12	7630 / 7766
		COUNT	7631 /
		K20	7632 / 0020
		CMD REG	7633 /

11.17.3 Check Surface and Sector Register

This program is used to scope the Surface/Sector Register and Data Buffer 4. The data to be used is entered into the Console Switch Register (switches 5—11) then loaded into the Surface/Sector Register. It is then shifted into the lower Data Buffer (DB4 bits 5—11) where it is read into the AC and stored in memory.

1. Clear disk control logic
2. Enable maintenance logic
3. Load Surface/Sector Register with data from switches
4. Enable shift to lower Data Buffer
5. Enable shift Surface/Sector Register (AC04=1)
6. Issue maintenance IOT 12 times
7. Read DB4

Example:

Location	Contents	Mnemonic	Operation
7000	7301	CLA CLL IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7001	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7002	1230	TAD -12	/ DESIRED SHIFT COUNT
7003	3231	DCA COUNT	/ SET UP SHIFT COUNTER
7004	7330	CLA,CLL,CML,RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7005	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7006	7604	LAS	/ LOAD THE AC FROM THE SWITCH REGISTER
7007	6743	DLAG	/ IOT 6743 LOAD DISK ADDRESS
7010	7332	CLA,CLL,CML,RTR	/ ENABLE SHIFT TO LOWER BUFFER (AC01=1)
7011	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7012	7012	RTR	/ ROTATE AC AND LINK RIGHT TWO PLACES
7013	7010	RAR	/ ENABLE CHECK SURFACE AND SECTOR REGISTER / (AC04=1)
7014	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7015	2231	ISZ COUNT	/ SHIFTED ONE WORD YET?
7016	5214	JMP -2	/ NO, SHIFT ANOTHER BIT
7017	7200	CLA	/ YES, CLEAR THE AC
7020	1232	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7021	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7022	3233	DCA SS REG	/ STORE WORD
7023	5200	JMP START	/ LOOP OR HALT (HLT=1 PASS)
		-12	7030 / 7766
		COUNT	7031 /
		K20	7032 / 0020
		SS REG	7033 /

11.17.4 Check CRC Register

This program is used to scope the CRC Register logic. AC bit 10, CRC Register, and Data Buffer Register 4 are logically connected in series. A data bit is shifted 28 times through this series register to allow the last 12 bits to be read from DB4.

1. Clear disk control logic
2. Enable maintenance mode
3. Enable shift to lower buffer (DB4)
4. Load maintenance data into AC10
5. Check CRC Register (AC02=1)
6. Issue maintenance IOT 28 times
7. Read DB4
8. Shift 12 more data bits in
9. Read DB4
10. Jump back to step 8

Example:

Location	Contents	Mnemonic	Operation
7000	7301	CLA,CLL,IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7001	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7002	1230	TAD -28	/ DESIRED SHIFT COUNT
7003	3231	DCA COUNT	/ SET UP COUNT
7004	7330	LOOP-CLA,CLL, CML,RAR	/ ENABLE MAINTENANCE MODE (AC00=1)
7005	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7006	7010	RAR	/ ENABLE SHIFT TO LOWER DATA BUFFER (AC01=1)
7007	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7010	7010	RAR	/ ENABLE CHECK CRC REGISTER
7011	1232	TAD AC10 DATA	/ LOAD DATA BIT INTO AC10
7012	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7013	2231	ISZ COUNT	/ SHIFTED ONE 12 BIT WORD YET?
7014	5212	JMP -2	/ NO, SHIFT ANOTHER BIT
7015	7200	CLA	/ YES, CLEAR THE AC
7016	1233	TAD -12	/ DESIRED SHIFT COUNT
7017	3231	DCA COUNT	/ SET UP COUNT
7020	1234	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7021	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7022	3235	DCA CRC	/ STORE WORD
7023	5204	JMP LOOP	/ LOOP OR HALT (HALT=1 PASS)
		-28	7030 / 7744
		COUNT	7031 /
		AC10 DATA	7032 / 0000 OR 0002
		-12	7033 / 7766
		K20	7034 / 0020
		CRC	7035 /

11.17.5 Single Cycle Data Break Transfers (Read Operation)

This program transfers data from the RK05 to processor memory. It can be used to scope the data break control logic, Data Buffers, Current Address Register, Command Register, and the logic involved in read operation.

1. Clear control logic
2. Enable maintenance mode
3. Load AC from the Switch Register
4. Load Command Register
5. Enable shift to lower buffer
6. Set AC03 to 1 (check Command Register)
7. Issue maintenance IOT 12 times
8. Current address = 0000
9. Set AC06 to 1 (check data break request)
10. Issue maintenance IOT

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA,CLL,IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	1230	TAD -12	/ LOAD DESIRED SHIFT COUNT
7603	3231	DCA COUNT	/ SET UP SHIFT COUNTER
7604	7604	LAS	/ TRANSFER SWITCH REGISTER CONTENTS TO THE AC
7605	6746	DLDC	/ STORE DATA IN LOCATION 0000
7606	7330	CLA CLL CML RAR	/ ENABLE MAINTENANCE MODE (AC0=1)
7607	6747	DMAN	/ IOT 6747 MAINTENTANCE IOT
7610	7010	RAR	/ ENABLE SHIFT TO LOWER DATA BUFFER (AC01=1)
7611	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7612	7012	RTR	/ ENABLE SHIFT TO COMMAND REGISTER (AC03=1)
7613	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7614	2000	ISZ COUNT	/ SHIFT ONE WORD YET?
7615		JMP -2	/ NO, SHIFT ONE MORE BIT
7616	7326	CLA CLL CML RTL	/ ENABLE MAINTENANCE MODE
7617	7006	RTL	/ ENABLE DB4 TO AC TRANSFER
7620	7006	RTL	/
7621	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7622	7000	NOP	/ NO OPERATION
7623	7000	NOP	/ NO OPERATION
7624	7402	JMP START	/ (DEPOSIT A HALT TO MAKE ONE PASS)

11.17.6 Single Cycle Data Break Transfers (Write Operation)

This program transfers data from processor memory to the Data Buffer. It is used to scope the write operation control logic, Current Address Register, Command Register, and the data break control logic.

1. Clear control logic
2. Enable maintenance logic
3. Set Command Register to write function
4. Load the AC from the Switch Register
5. Store data in location 0000 of memory
6. Enable break request bit
7. Issue maintenance IOT
8. Read DB4

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA,CLL,IAC	/ ENABLE CLEAR CONTROL (AC10=0 AC11=1)
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	7330	CLA,CLL,CML,RAR	/ ENABLE MAINTENANCE MODE (AC0=1)
7603	6746	DLDC	/ IOT 6746 LOAD COMMAND REGISTER
7604	7604	LAS	/ LOAD AC FROM SWITCH REGISTER
7605	3000	DCA0	/ LOAD AC INTO LOCATION 0000
7606	7330	CLA,CLL,CML,RAR	/ ENABLE MAINTENANCE MODE (AC0=1)
7607	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7610	7012	RTR	/ ENABLE THE
7611	7012	RTR	/ MAINTENANCE DATA
7612	7012	RTR	/ BREAK REQUEST (AC06=1)
7613	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7614	7000	NOP	/ NO OPERATION
7615	7000	NOP	/ NO OPERATION
7616	7200	CLA	/ CLEAR AC
7617	1225	TAD K20	/ ENABLE DB4 TO AC TRANSFER (AC07=1)
7620	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7621	3226	DCA DATA	/ STORE DATA
7622	7402	JUMP START	/ (DEPOSIT A HALT TO MAKE ONE PASS)

11.17.7 Single Cycle Data Break Transfers (Write then Read)

This program transfers data in the Switch Register to DB1 of the RK8-E, then reads the data back into memory after it has transferred into DB4. The transfers are effected by causing one break request while the Command Register has a write command in it, then causing another break request with a read in the Command Register. Finally, check to see if the word read equals the word written.

1. Clear control logic
2. Load Command Register with a write function
3. Load memory location 0000 with data from the Switch Register
4. Enable maintenance logic
5. Initiate one single cycle data break request
6. Load Command Register with a read function
7. Initiate one single cycle data break request
8. Check data read with data from Switch Register

Example:

Location	Contents	Mnemonic	Operation
7600	7301	CLA CLL IAC	/ ENABLE CLEAR DISK CONTROL LOGIC
7601	6742	DCLR	/ IOT 6742 CLEAR CONTROL
7602	7330	CLA CLL CML RAR	/ ENABLE MAINTENANCE MODE AC00=1
7603	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7604	6746	DLDC	/ IOT 6746 LOAD COMMAND REGISTER (WRITE)
7605	7604	LAS	/ LOAD AC FROM SWITCH REGISTER
7606	3000	DCA 0	/ STORE WRITE DATA
7607	7326	CLA CLL CML RTL	/ ENABLE THE
7610	7006	RTL	/ MAINTENANCE DATA
7611	7006	RTL	/ BREAK REQUEST AC06=1
7612	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7613	7000	NOP	/ NO OPERATION
7614	7000	NOP	/ NO OPERATION
7615	7200	CLA	/ CLEAR AC
7616	6746	DLDC	/ IOT 6746 LOAD COMMAND (READ)
7617	7326	CLA CLL CML RTL	/
7620	7006	RTL	/ ROTATE AC AND LINK LEFT TWO
7621	7006	RTL	/ ENABLE MAINTENANCE DATA BREAK / REQUEST (AC06=1)
7622	6747	DMAN	/ IOT 6747 MAINTENANCE IOT
7623	7000	NOP	/ NO OPERATION
7624	7000	NOP	/ NO OPERATION
7625	5200	JMP START	/ (HALT=1 TIME) (NOP=CHECK DATA)
CHECK DATA			
7626	7300	CLA CLL	/ CLEAR AC AND LINK
7627	1000	TAD 0	/ LOAD AC WITH WRITE DATA

Location	Contents	Mnemonic	Operation
7630	7040	CMA	/ COMPLEMENT WRITE DATA
7631	3003	DCA 0003	/ STORE DATA FROM AC IN MEMORY
7632	1001	TAD 0001	/ LOAD AC WITH READ DATA
7633	0003	AND 0003	/ COMPARE READ AND WRITE DATA
7634	7440	SZA	/ SKIP ON ZERO AC (GOOD DATA)
7635	7402	HLT	/ HALT
7636	5200	JMP START	/ JUMP TO START

SECTION 6 SPARE PARTS

Table 11-16 lists recommended spare parts for the RK8-E. These parts can be obtained from any local DEC office, or from DEC, Maynard.

Table 11-16
RK8-E Spare Parts

DEC Part No.	Description	Quantity
11–00114	Diode, D664	1
19–05542	DEC IC, 7474	2
19–05575	DEC IC, 7400	2
19–05576	DEC IC, 7410	1
19–05579	DEC IC, 7440	1
19–05585	DEC IC, 7476	1
19–05587	DEC IC, 7473	1
19–09004	DEC IC, 7402	2
19–09055	DEC IC, 7495	1
19–09056	DEC IC, 74H00	1
19–09057	DEC IC, 74H10	1
19–09061	DEC IC, 74H52	1
19–09062	DEC IC, 74H53	1
19–09267	DEC IC, 74H11	1
19–09485	DEC IC, 380	2
19–09486	DEC IC, 384	1
19–09594	DEC IC, 8251B	1
19–09615	DEC IC, 8271	1
19–09667	DEC IC, 74H74	1
19–09686	DEC IC, 7404	2
19–09704	DEC IC, 314	1
19–09705	DEC IC, 8881	1
19–09931	DEC IC, 74H04	1
19–09935	DEC IC, 8235	1
19–10011	DEC IC, 7486	1
19–10018	DEC IC, 74193	1
19–10091	DEC IC, 7437	1
19–10155	DEC IC, 7408	1
19–10224	DEC IC, 7485	1
19–10363	DEC IC, 7496	1
19–10406	DEC IC, 75451	1
19–10436	DEC IC, 74123	1
19–10645	DEC IC, 75452	1
19–10650	DEC IC, 74161	1
19–10652	DEC IC, 74174	1
19–10656	DEC IC, 74155	1
18–10694	DEC Crystal Oscillator	1

11.18 DEC 74155 IC

The 74155 IC (Figure 11-34) is TTL circuit used as a 2-line to 4-line decoder (unit select decoder) and as a 3-line to 8-line decoder (function decoder) in the RK8-E. This IC may also be used as a 1-line to 8- or 4-line multiplexer, but it is not used this way in the RK8-E and will not be discussed here.

When the 74155 IC is used as a 2-line to 4-line decoder, as with the unit select decoder, the 1Y0 through 1Y3 outputs are selected by applying +3V to pin 1 and leaving pin 2 low. The inputs in this configuration are applied to pins 3 and 13 and the outputs (low) are taken from pins 4, 5, 6, and 7.

In the 3-line to 8-line configuration, as in the function decoder, external connections are installed to tie pin 1 to pin 15 and pin 2 to pin 14 (Figure 11-34). This allows both the 2Y and 1Y outputs to be used and provides for three inputs instead of two. In this configuration, the 74155 IC becomes a BCD to decimal decoder, which decodes three binary bits (Paragraph 11.15.3.1).

11.19 DEC 74193 IC

The DEC 74193 (Figure 11-35) monolithic circuit is a synchronous, reversible (up/down), 4-bit binary counter having a complexity of 55 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters. Figure 11-35 contains the logic diagram and pin locations.

The outputs of the four master/slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable, i.e., the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs, independently of the count pulses. This feature allows the counters to be used as Modulo—N Dividers by simply modifying the count length with the preset inputs.

A CLEAR input has been provided which forces all outputs to the low level when a high level is applied. The CLEAR function is independent of the count and load inputs. An input buffer has been placed on the CLEAR, COUNT, and LOAD inputs to lower the drive requirements to one normalized load. This is important when the output of the driving circuitry is somewhat limited.

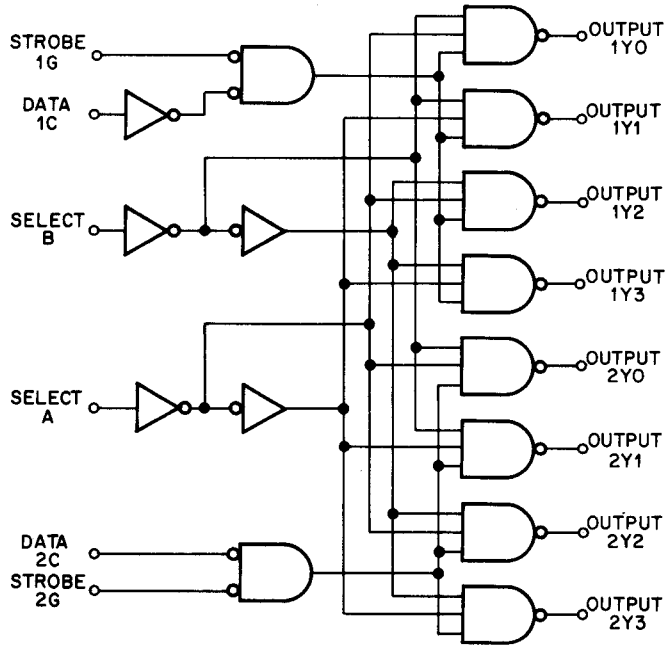
This counter was designed to be cascaded without the need for external circuitry. Both BORROW and CARRY outputs are available to cascade both the up- and down-counting functions. The BORROW output produces a pulse equal in width to the COUNT DOWN input when the counter underflows. Similarly, the CARRY output produces a pulse equal in width to the COUNT UP input when an overflow condition exists. The counters can then be easily cascaded by feeding the BORROW and CARRY outputs to the COUNT DOWN and COUNT UP inputs, respectively, of the succeeding counter.

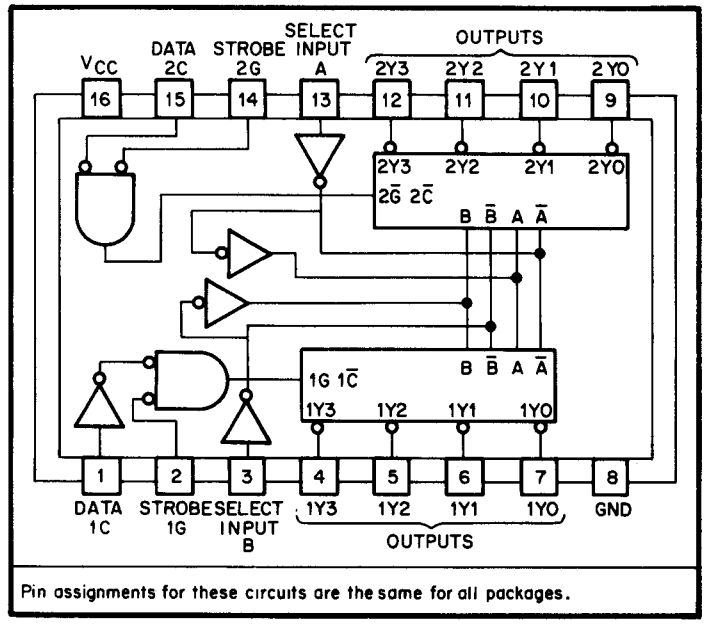
NOTE

Voltage values are with respect to network ground terminal.

11.20 DEC 7485 IC

The DEC 7485 IC performs magnitude comparison of straight binary and straight BCD codes. Three fully decoded decisions about two 4-bit words (A and B) are made and are externally available at three outputs. The delay time for a 4-bit comparison is 12 ns. Figure 11-36 shows the truth table, pin locator, and logic diagram.





Pin assignments for these circuits are the same for all packages.

8E-0605

Figure 11-34 DEC 74155 IC Illustration (sheet 1)

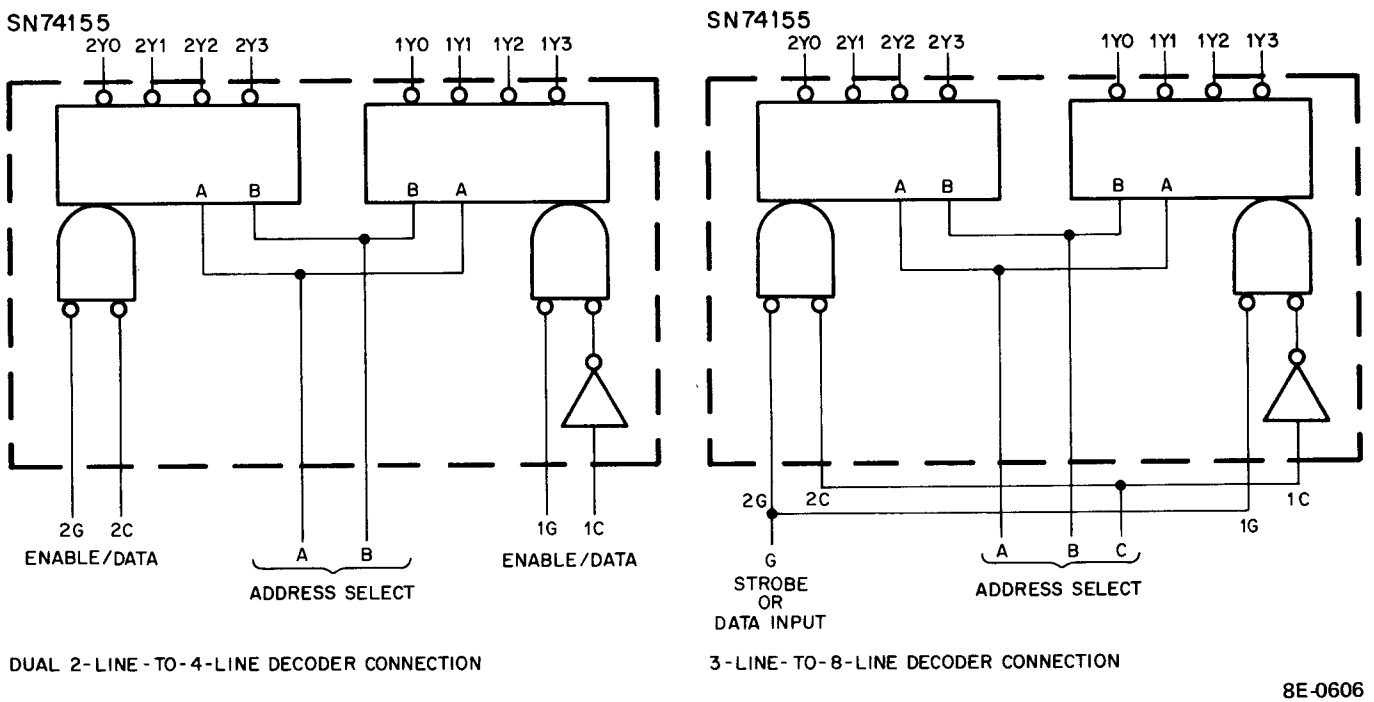


Figure 11-34 DEC 74155 IC Illustration (sheet 2)

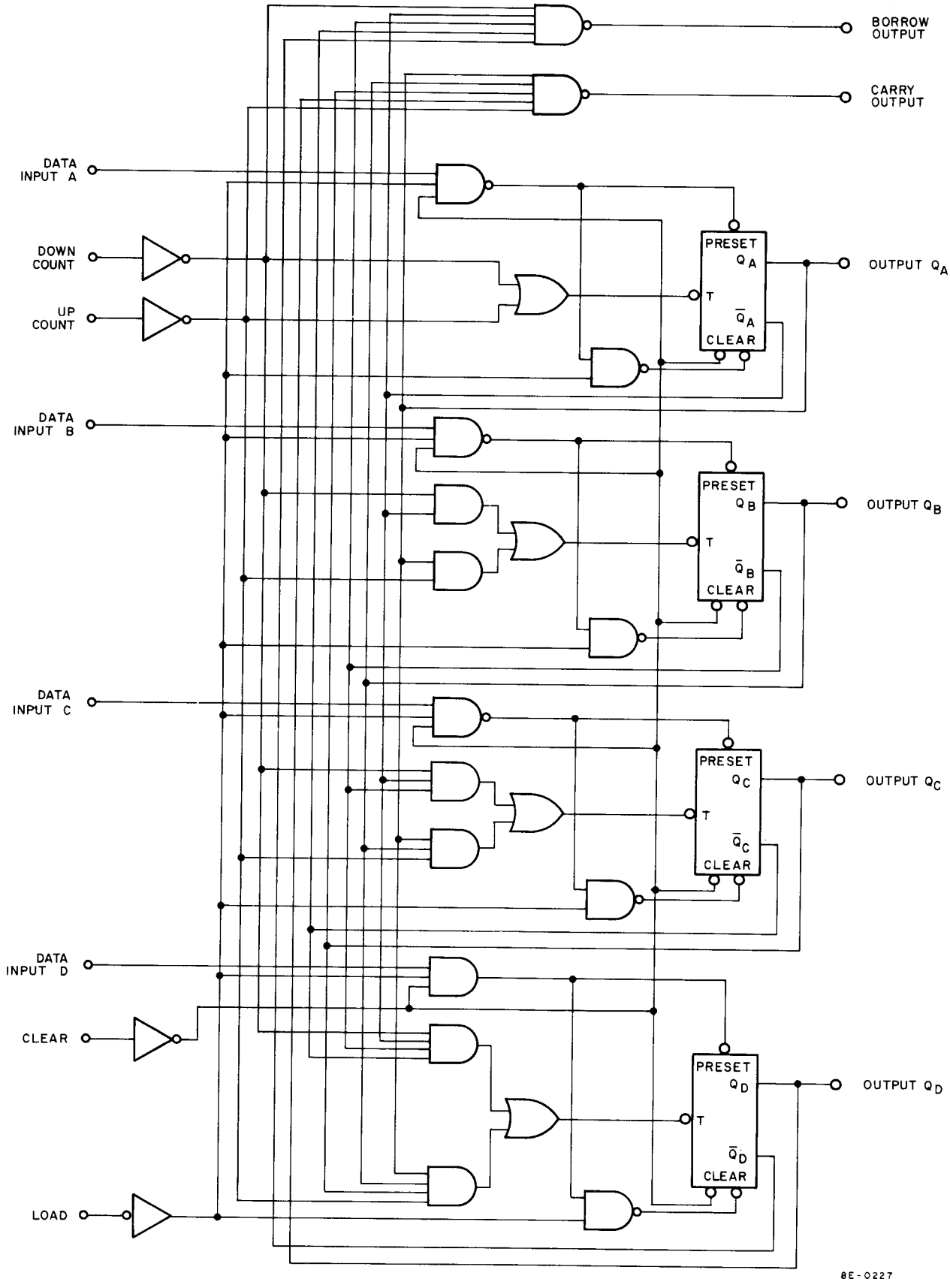
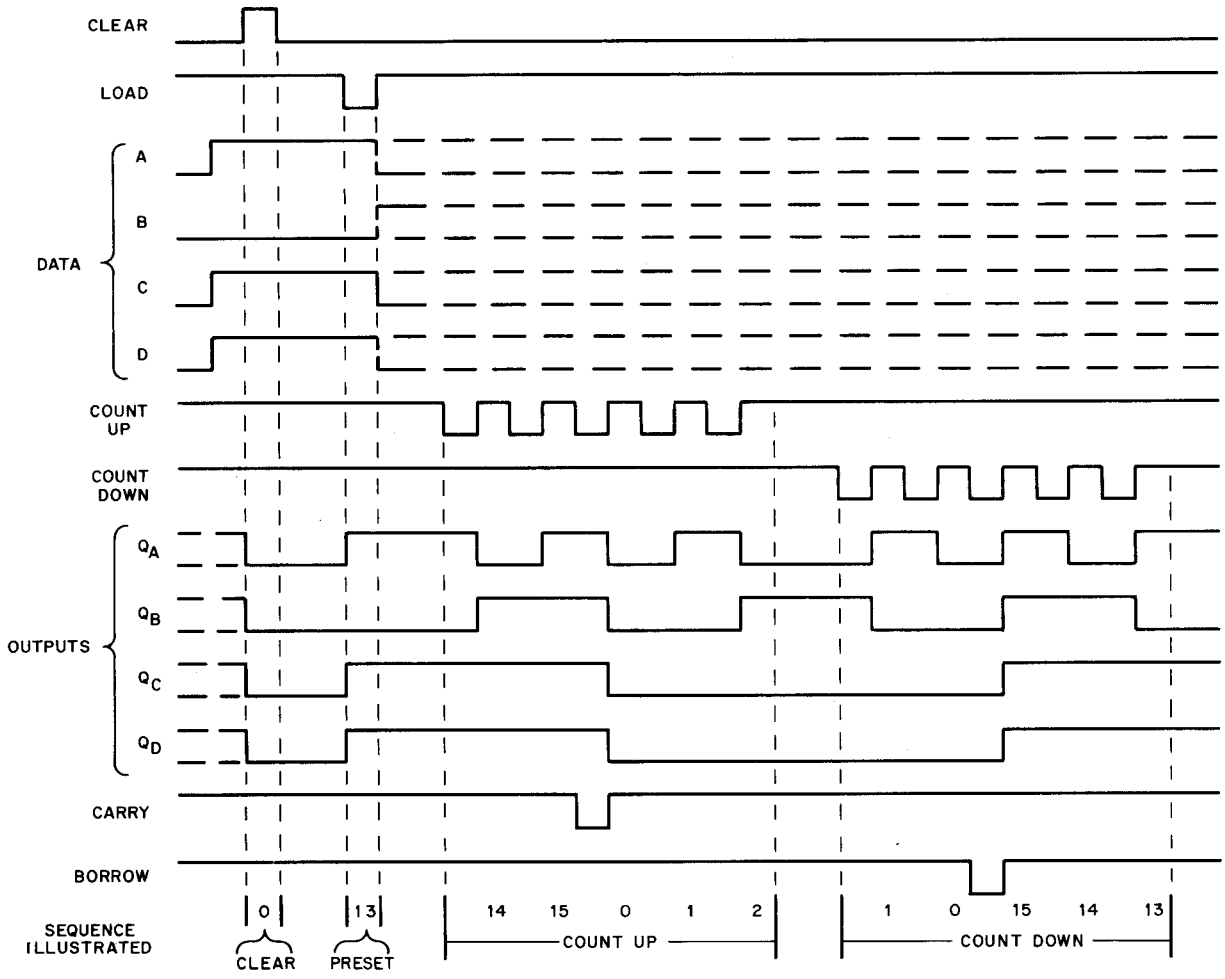


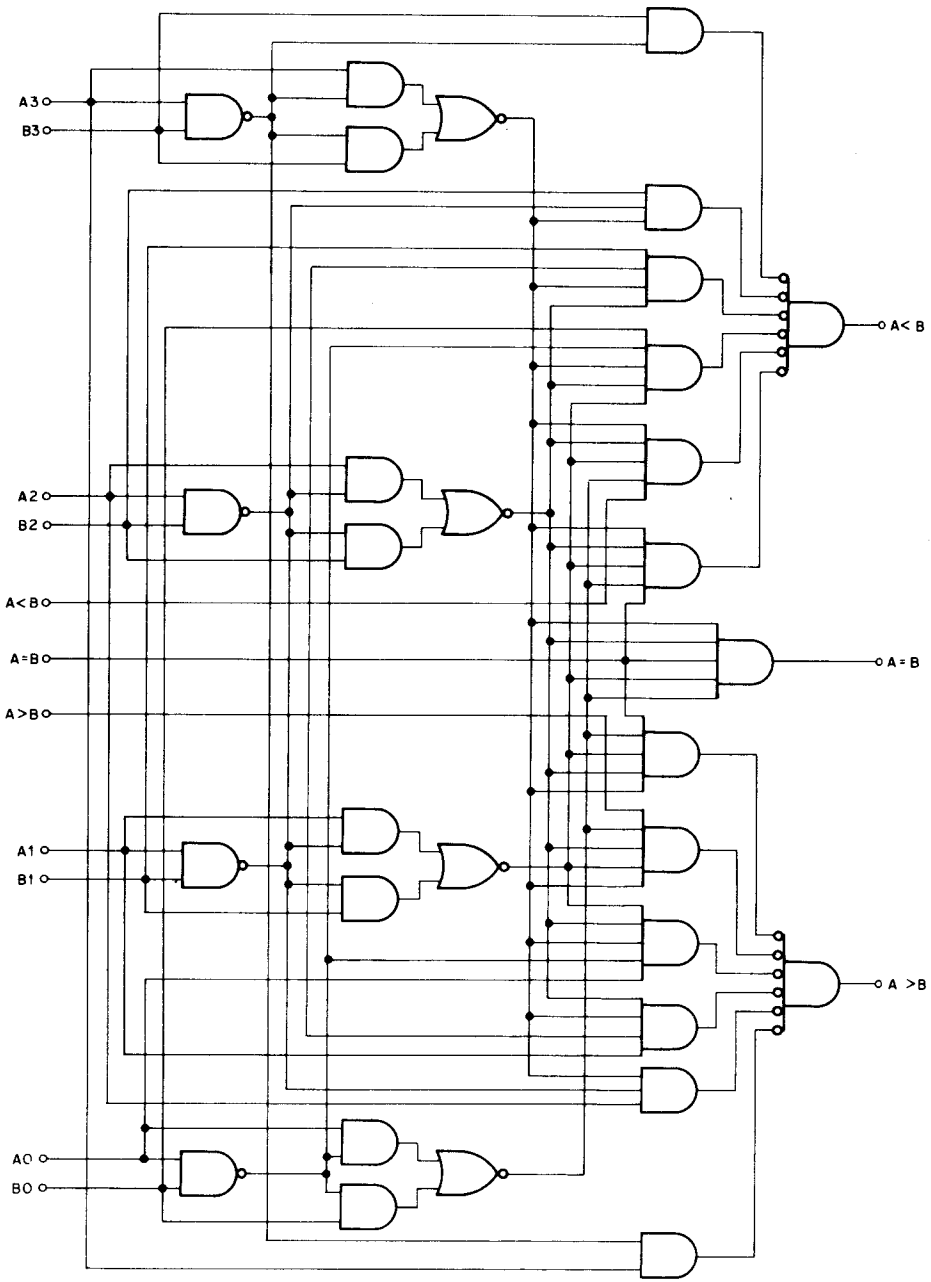
Figure 11-35 74193 IC Illustration (sheet 1)



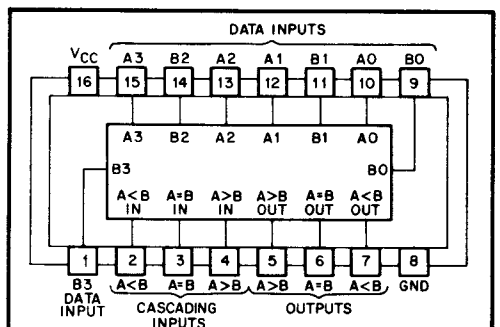
NOTE:
A. Clear overrides load data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

8E-0226

Figure 11-35 74193 IC Illustration (sheet 2)



TOP VIEW



Pin assignments for these circuits are the same for all packages.

8E-0604

Figure 11-36 DEC 7485 IC Illustration

The 7485 IC is used to compare the desired 4-bit sector address with a 4-bit sector address read from the disk cartridge in the RK8-E. This application asserts the A—B output when the two 4-bit addresses are equal.

11.21 DEC 74161 IC

The DEC 74161 IC (Figure 11-37) is a presetable high-speed binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates output counting spikes normally associated with ripple clock counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock input. To preset of load the counter register, the clock input and the enable must be asserted. The removal of enable allows the counter to be incremented by the clock input.

In the RK8-E, these ICs are cascaded to provide a 12-bit Current Address Register that is preset to an address in memory and incremented during the single cycle data break to select sequential memory locations.

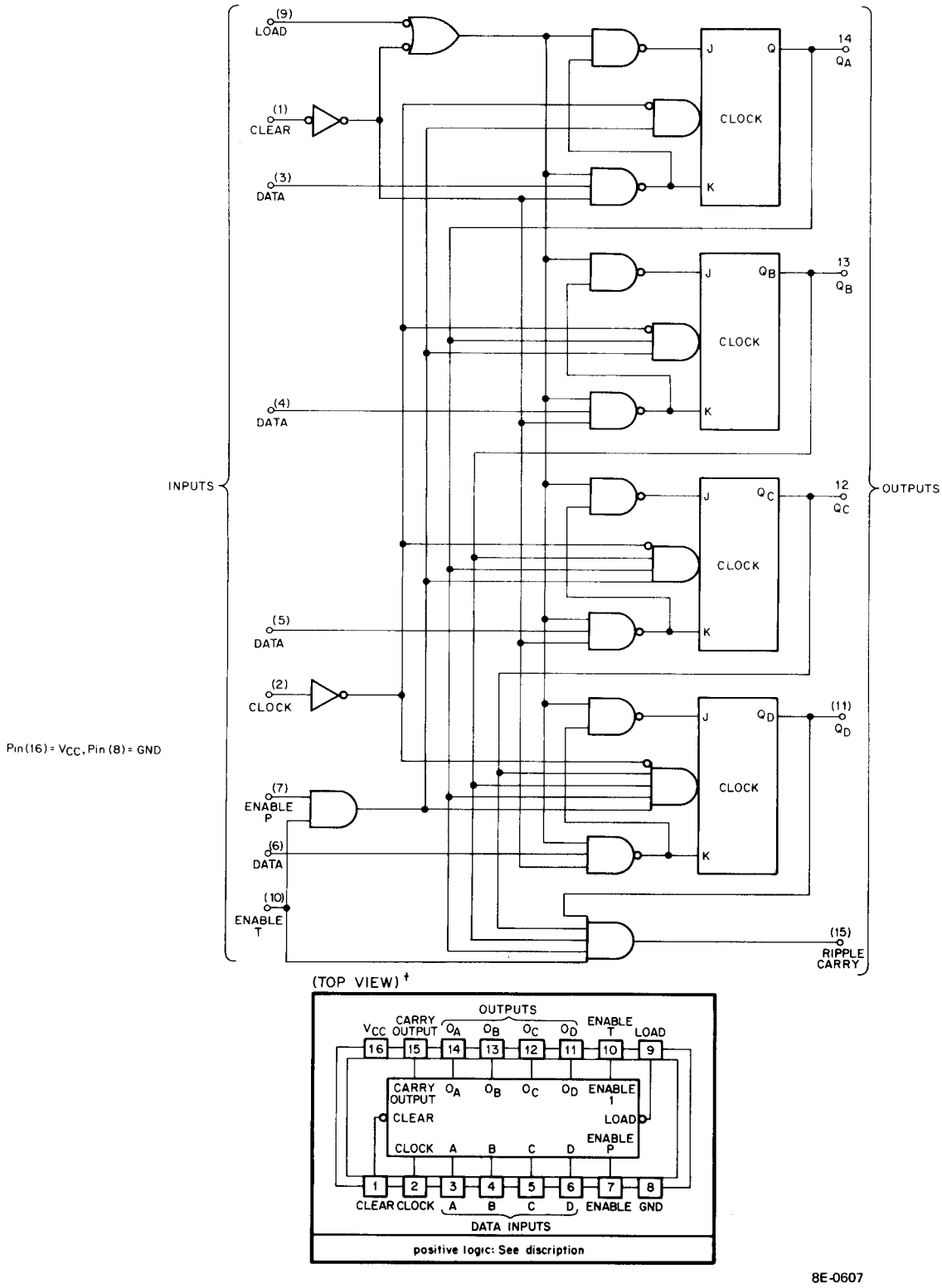


Figure 11-37 DEC 74161 IC Illustration (sheet 1)

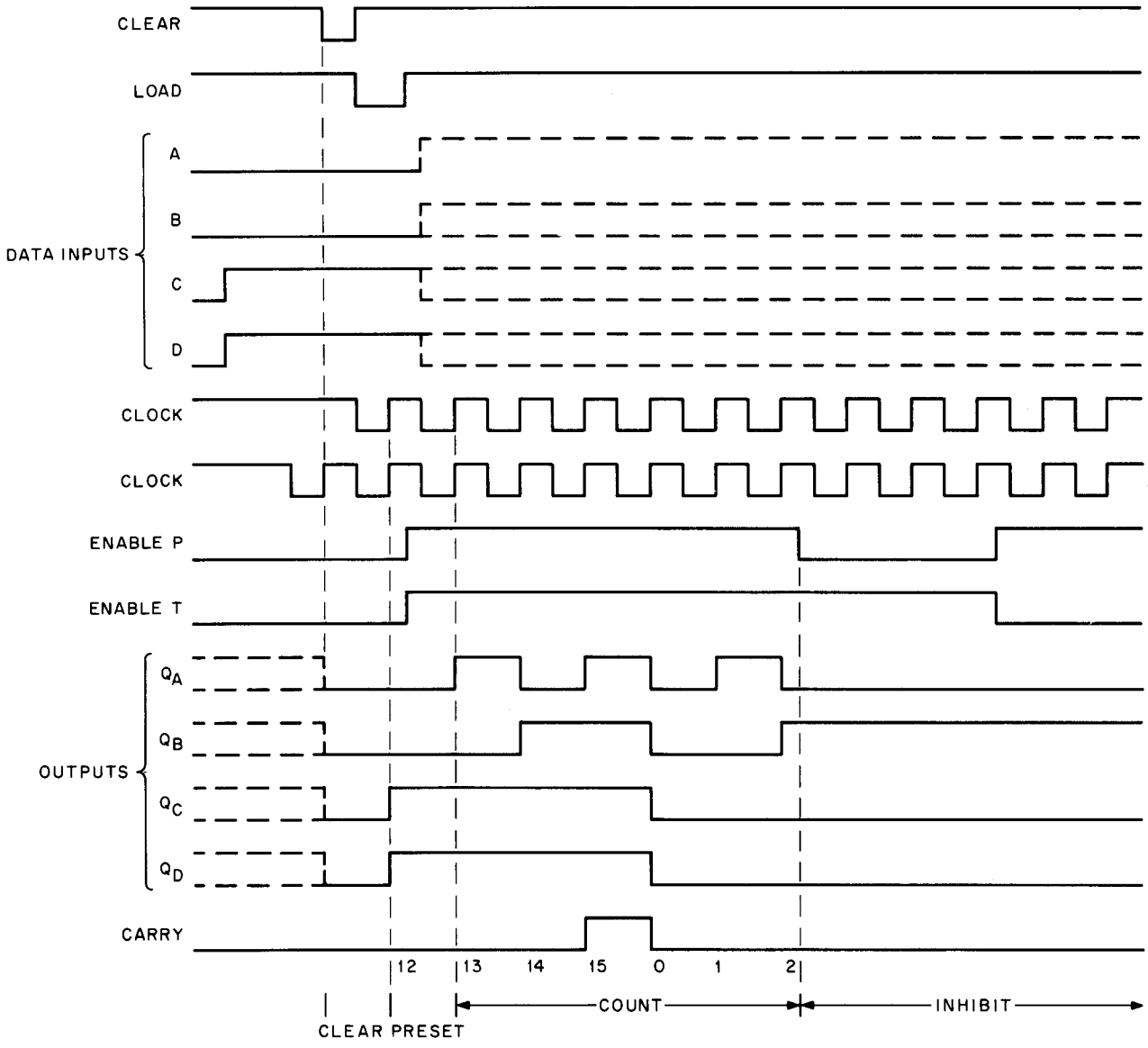


Figure 11-37 DEC 74161 IC Illustration (sheet 2)