

CHAPTER 6

TECHNICAL DESCRIPTION

6.1 INTRODUCTION

This chapter provides a technical description of the VT180 operating principles for repair or maintenance personnel. The VT180 is presented as a system consisting of several functional or replaceable subunits. The subunits will be described at the system level followed by a functional description of each subunit in its own section. Interaction between subunits is discussed in the section about the subunit most involved in the particular process.

The VT180 hardware is described both to the block diagram level and the functional block diagram level. The VT180 Field Maintenance Print Set (MP00633), the VT18X control module circuit schematics (CS 5415152-0-1), and the VT180 paddle board circuit schematics (CS 5415150-0-1) contain circuit details for the various subunits. These circuit schematics may be used while studying this chapter.

Numbers may be given in binary, octal, decimal, or hexadecimal (hex). The normal form will be decimal for scalar or ordinal values, and hex for data and addresses. Numbers are subscripted B for binary, Q for octal, H for hex, and there is no subscript for decimal.

6.2 SYSTEM DESCRIPTION

The VT180 personal office computer is a VT100 terminal that has been upgraded by installing a VT18X personal office computing upgrade kit. The addition of the VT18X upgrade kit provides the basic VT100 with the capability to operate in either personal computer mode or terminal mode. In personal computer mode, the VT180 runs under the control of an operating system called CP/M. CP/M allows the VT180 to run the many available CP/M programs that have been developed for various applications. In terminal mode, the VT180 retains VT100 functionality, and thus is capable of communicating with an external host computer.

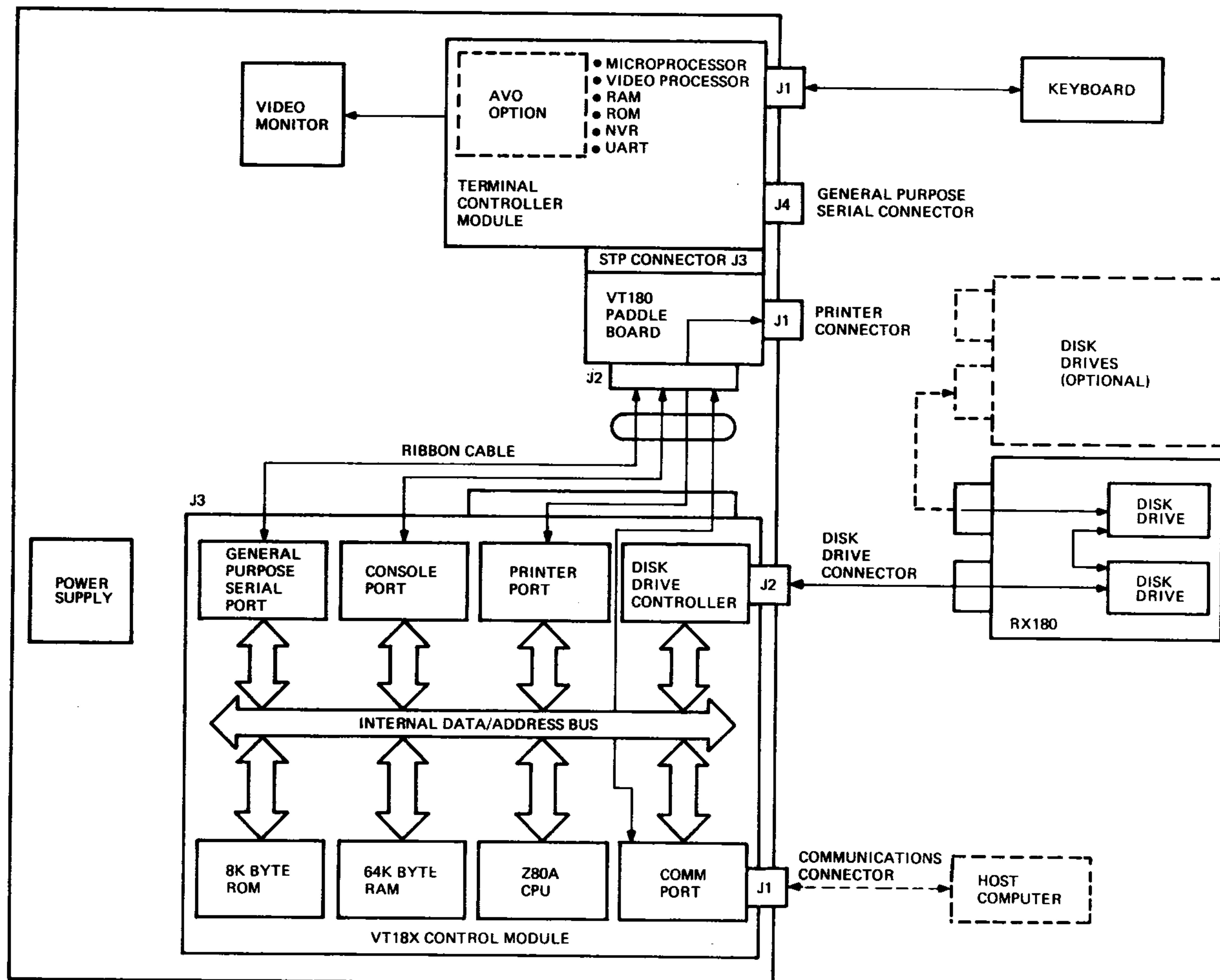
The VT180 has the following features.

1. Full VT100 functionality (except for printer port emulation)
2. Two operating modes (personal computer or terminal)
3. Extensive power-up self-test diagnostics
4. Z80[®] instruction set VT18X control module
5. A VT131 hardware compatible communications port
6. A printer port
7. A general purpose serial port
8. One or two RX180 dual disk drive units with up to 720K bytes of formatted data

6.2.1 System Subunits

The VT180 consists of a VT100, a VT18X control module, one or two RX180 dual disk drive units, a VT180 paddle board, RF shielding, signal and power cables, and miscellaneous mounting hardware. The various subunits of the VT180 are shown in the block diagram of Figure 6-1.

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Figure 6-1 VT180 System Block Diagram

6.2.1.1 Terminal Controller Module – The terminal controller is a single module that manages all displays and all communication between the keyboard and the host computer. Everything else connects to it. The terminal controller contains these functional components.

1. A microprocessor to manage terminal operations
2. A video processor for converting data to recognizable patterns
3. 3072 bytes of random-access memory (RAM) for screen data storage and microprocessor scratch memory
4. 8192 bytes of read-only memory (ROM) containing the microprocessor's programming to operate the terminal with its particular features
5. A nonvolatile RAM (NVR) to store the user-selectable operating features without requiring hardware switches

6. An asynchronous serial receiver-transmitter (UART) for data exchange with the personal computer or host computer
7. EIA level converters to adapt the on-board input and output (I/O) signals to the communications interface

6.2.1.2 Advanced Video Option (AVO) – The advanced video option provides greater display capacity, and it can carry extra firmware for the expanded functionality of other products in the VT180 series. The AVO is mounted on the terminal controller module.

6.2.1.3 Video Monitor – The video monitor is a video screen that displays exchanges between the operator and the personal computer or the host computer. It can display data in two modes: 80 characters by 24 lines, or 132 characters by 14 lines (or, with the AVO, 132 by 24). With the control circuitry on the terminal controller board, the CRT can perform many special character display functions.

6.2.1.4 VT180 Power Supply – The power supply converts the ac power line to the four dc voltages required by the terminal. It has a switching regulator for highest efficiency and coolest operation.

6.2.1.5 Keyboard – The keyboard is a typewriter-style input device for the operator. It has a loudspeaker for user feedback, keyclicks and bells, and indicators (LEDs) that show internal states of the terminal.

6.2.1.6 VT18X Control Module – The VT18X control module is a single-board microcomputer with a Z80A processor operating at 4 MHz and with 64K bytes RAM, 8K bytes software deselectable ROM, 4 communications ports, and an RX180 disk drive controller. The communications ports and disk drive controller functions are described in the following paragraphs.

Console Port

The console port communicates with the VT180 via the STP connector. Transmit and receive baud rates are fixed by the 15.7K bytes local clock on that connector. The console supports RS-232C signals, including transmit data, receive data, and data terminal ready from the VT180 for control. Software must support the XON/XOFF protocol for this port.

Communications Port

This port is used to communicate to another computer. It has full modem support and supports the same hardware signals as the VT131. It can support United States and European full- and half-duplex modems. The port has ASYNC as well as BISYNC modes with an RS-232C (V.24/V.28) physical interface conforming to CCITT V.21, V.22, and V.23. Break detection by this port is supported. The transmit and receive baud rates for this port are derived from the baud rate clocks on the terminal controller module. Therefore, the transmit and receive baud rates selected in the VT180's SET-UP B mode are the transmit and receive baud rates used for this port.

NOTE

It is important to note that the standard VT100 communications port (J4) on the terminal controller module now becomes a general purpose serial port, and the full communications port to the host computer is now the 25-pin, D-type connector (J1) on the VT18X control module.

Baud rates supported by the communications port are 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200. This port also has the capability to select external send and

receive clocks supplied by a modem. Any and all protocols to be supported by this port, other than terminal emulation pass-through mode, are run as applications under CP/M. The recommended cables are BC26R-10 and BC22B-10. A BC22C-10 must be used for bisynchronous operation.

Certain transmit and receive signals on the communications port are routed through a ten position switch on the VT18X control module. This switch is used to configure the module for use with various communications modems. Refer to Paragraph 6.6.6 for the modem switch configurations.

Printer Port

This is a printer port that provides an RS-232C serial interface compatible with Digital printers. EIA signals supported are transmit data, receive data, and data terminal ready. Programmable baud rates supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. Parity can be configured to none, odd, or even. Software should support XON/XOFF protocol for this port. This port requires a null modem cable. The 25-pin, D-type EIA printer port connector physically resides on the VT180 paddle board in the normal printer port location. The recommended cable for this port is a BC26U-15. A BC22A will also work but is a second choice.

General Purpose Serial Port

This port is provided as a general purpose RS-232C interface. Signals that are supported are transmit data, receive data, and data terminal ready. Programmable baud rates supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Parity can be configured to none, odd, or even. Programmable character formats that are supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. This port uses the VT100 communications port connector (J4) on the terminal controller module. Signals are passed from the VT18X control module through a ribbon cable to the VT180 paddle board. This port requires a null modem cable. A BC26U-XX is the recommended cable for this port. Another cable that may be used is a BC22A in either 10 or 25 foot length.

Disk Drive Unit Interface

This interface controls up to four 5¼ inch disk drives. The controller circuit supports double-density drives using a phase locked loop (PLL) circuit. Only soft-sectored, single-sided diskettes are supported. The interface adheres to drive capability and signal definition of the ANSI standard interface for disk drives. The connector to the drives is a 37-pin, D-type shielded cable (BC26K). This connector physically resides on the VT18X control module.

6.2.2 VT100 and VT18X Control Module Interconnection

The terminal controller module is interconnected to the VT18X control module by a 16-pin cable to the VT180 paddle board. This interconnection is very important in the operation of the VT180. All four serial ports on the VT18X control module depend upon signals from this connector. The INIT line from the terminal controller module to the Z80A CPU is also supplied via this channel. A 16-pin ribbon cable (70-08612-OM), which is 27.94 cm (11 inches) long, is used for the connection.

6.2.3 VT180 Paddle Board

The VT180 configuration has its own paddle board, which consists of the board (50-15149); a 25-pin, D-type EIA connector for the printer port; a jumper; and a 16-pin socket. Other components are present for FCC considerations. The 16-pin socket is used to connect the STP port and the VT18X control module. Printer, communications clocks, and general purpose serial port signals are supplied by the 16-pin ribbon cable connecting the VT100 terminal controller module and the paddle board.

6.2.4 RX180 Disk Drive Unit

The RX180 disk drive unit consists of two disk drives. In double-density operation, the RX180 will store 360K bytes of formatted data (180K bytes per drive). Two versions of the RX180 are available: an

RX180-AB, which is configured as CP/M drives A and B, and an RX180-AD, which is configured as drives C and D.

The RX180 contains its own power supply and is controlled by the VT18X control module via the disk drive connector, J2. The ac power cabling is serially routed through the drive units to the VT180 terminal. This routing scheme allows the user to power up the entire VT180 in a two drive unit system by using the power switch on the top drive unit.

6.3 VT100 FUNCTIONAL DESCRIPTION

The basic VT100 consists of the functional blocks shown in Figure 6-2. All of the subunits shown, with the exception of the keyboard, reside inside the terminal cabinet. This section provides a general description of each of the functional blocks.

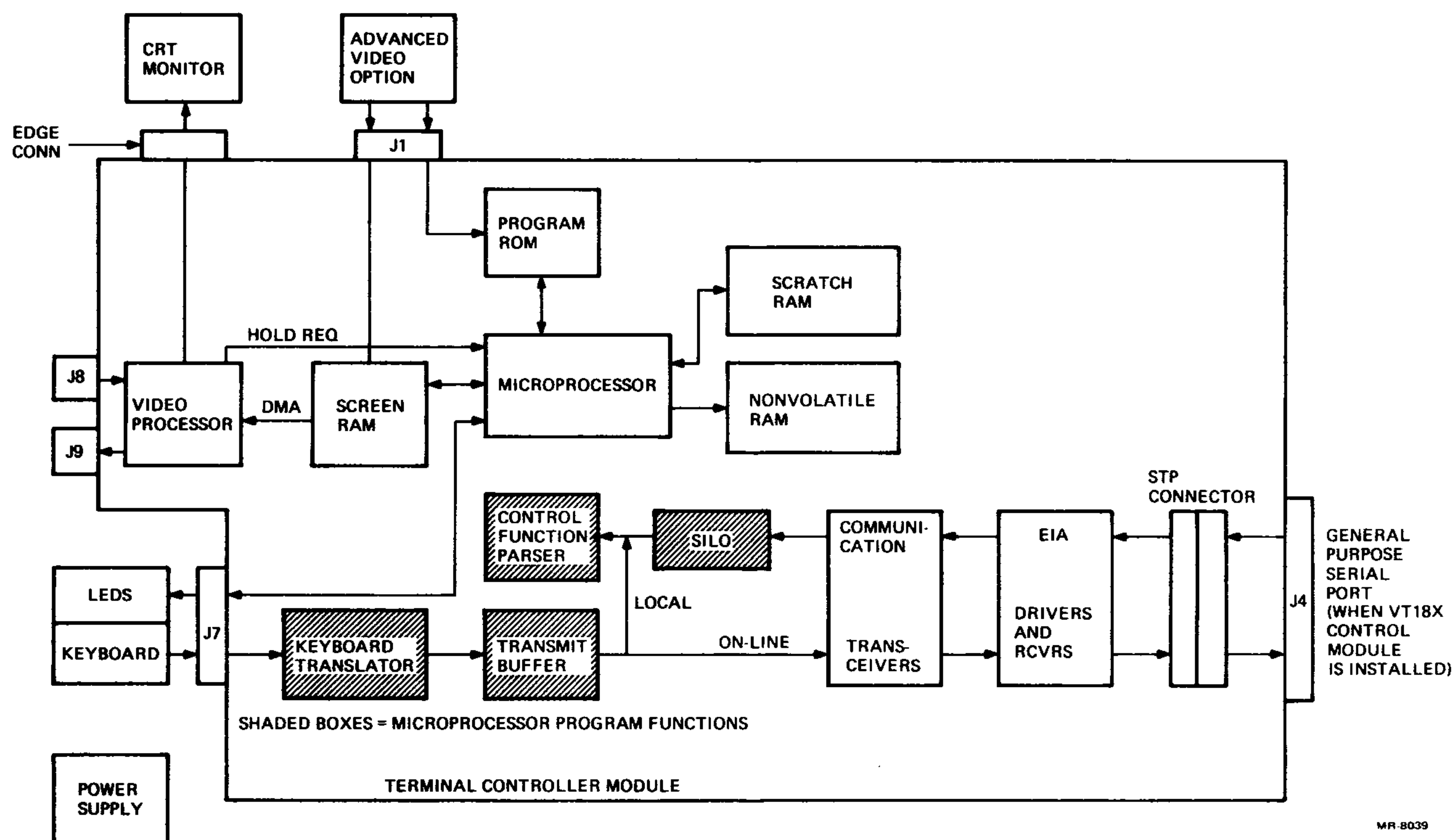


Figure 6-2 VT100 Functional Block Diagram

6.3.1 Microprocessor

A microprocessor (8080A) manages all terminal input and output operations. It also provides the intelligence that enables the VT100 to respond to and generate a wide range of ANSI control functions and to emulate the characteristics of the VT52. Several of the microprocessor's program functions are effectively in series with data paths in the terminal. These functions have their own blocks in the functional block diagram to clarify the processes involved. These blocks are shaded to indicate that they are program functions or that the microprocessor controls data transfers between the blocks. The microprocessor is a computer with its instructions in program ROM (read-only memory) and its working memory in the scratch RAM (random-access memory). Terminal parameters for start-up are stored in the nonvolatile RAM (NVR). The advanced video option (AVO) normally contains extra RAM, as described in Paragraph 6.3.5. It can also contain extra program ROM.

6.3.2 Program ROM

The VT100 program ROM is an 8K by 8 memory containing instructions and data tables for the terminal's microprocessor. Memory comes in four 2K packages (later VT100s may have a single 8K package). Checksum data stored in each ROM allows the terminal to confirm the condition of its programming during self-test.

6.3.3 Scratch RAM

The scratch RAM is the portion of RAM on the terminal controller that is not used for the screen RAM. That is, the RAM is 3K bytes long, but only about 2.3K bytes are used for screen display. The rest of the RAM contains the microprocessor stack, set-up data, various flag bytes, the communication silo, the keyboard buffer, and so on.

6.3.4 Nonvolatile RAM

The nonvolatile RAM (NVR) does not lose its data when its power is off. It stores all user-selectable features and parameters and the answerback message so that they are available each time the terminal is turned on. Even the screen intensity can be stored. There are no mechanical switches needed for configuration.

6.3.5 Advanced Video Option

The advanced video option (AVO) contains the 1K by 8 of extra screen RAM needed to expand the display from 14 lines of 132 characters to 24 lines. It also contains a 4K by 4 RAM to store an extended set of attributes for all characters. The AVO has an additional segment of video processor to manage the four extra bits of data. Sockets for ROMs and jumper- or switch-programmable decoders allow expansion or overlay of program memory. The AVO is a replaceable subunit of the VT180.

6.3.6 Keyboard

The keyboard is the user's input device to the terminal. The keyboard's output is a serial data signal that travels along the same wire as data coming from the terminal. The keyboard contains a bidirectional interface circuit, a set of keyswitches arranged like a typewriter, circuits to send the key information to the interface, LED indicators, and a small loudspeaker for keyclicks and bells. The connection to the terminal is a three-wire coil cord carrying signals, power, and ground. The keyboard is a replaceable subunit of the VT180.

6.3.7 LEDs

The terminal can inform the user of some internal conditions, such as on-line, local, and keyboard locked, through the LEDs on the keyboard. The LEDs also may indicate the location of a failure during self-test. They are user-programmable during normal operation.

6.3.8 Keyboard Translator

The output for each key is a number that represents the key's location (address) in the keyboard switch matrix. The microprocessor's keyboard translator translates the address to the industry-standard ASCII code.

6.3.9 Transmit Buffer

The ASCII codes wait in a transmit buffer until they can be transmitted. Some keys (such as the numeric keypad in application mode) produce control functions that are three bytes long. The transmit buffer is nine bytes long and thus can store at least three keys of any kind.

6.3.10 Communication Transmitter

The communication transmitter is one-half of a programmable universal synchronous/asynchronous receiver-transmitter (PUSART) and its associated circuitry and firmware routines. The PUSART is programmed to place data in a standard asynchronous format by adding control and error detection bits to the

original byte. The communication transmitter thus takes the parallel ASCII keycodes out of the keycode buffer, converts them to serial form, and delivers them to the EIA interface.

6.3.11 Communication Receiver

Data that the host sends to the terminal enters the communication receiver, which is the other half of the PUSART. The PUSART accepts serial data from the interface and converts it to parallel form. The PUSART also checks for errors and records them in a status byte. The microprocessor reads the data and then the status byte to confirm the correctness of the data. If an error is detected, a checkerboard is displayed on the screen instead of a character. If the microprocessor is busy managing the display, it devotes only enough time to the communication receiver to get the incoming code and check it for special codes requiring immediate action.

6.3.12 Silo

The rest of the incoming codes are stored in a part of RAM memory called a silo. This memory maintains the order of the data as it arrives; the first data to arrive leaves first. This memory gives incoming data a place to wait when the microprocessor cannot transfer data from the communication receiver to the screen RAM as fast as it arrives. The silo control routine checks the filling of the silo and can issue XON and XOFF commands to the host to try to keep from overflowing.

In local mode, data from the keyboard bypasses the communication receiver and transmitter and the silo.

6.3.13 Control Function Parser

When the microprocessor has enough time, it takes data from the silo and puts it through a control function parser routine in the microprocessor. Each code is tested to see if it is in the control range (<20H or 7FH). If it is, the microprocessor acts on it immediately. Line feed, for example, causes a one line scroll. If the code is 1BH (escape), more codes are read from the silo until the characters that define a control function are seen. Then the microprocessor executes the control function immediately or discards it if it is not a valid function. Noncontrol codes are recognized by the parser and are immediately written directly into the screen RAM.

6.3.14 Screen RAM

The screen RAM is a memory that stores data for display on the screen (CRT monitor). The memory is organized according to the set-up line length specifications. Basic terminal memory can hold 24 lines of 80 characters or 14 lines of 132 characters. With the extra memory provided by the advanced video option, the screen size may increase to 24 lines of 132 characters and four additional bits are appended to each character location to allow expanded character attributes. A character attribute modifies the display of that character relative to the preset values for the entire screen (that is, blinking, underline, etc.).

Most of the time the microprocessor can write to or read from the screen RAM. About 10 percent of the time, during the first scan of each 10 scan lines of characters, the video processor overrides the microprocessor and takes full control of the screen RAM, providing its own addresses to access the memory. This complete control of memory by a device other than the microprocessor, which is normally in control, is called a direct memory access (DMA). The DMA allows fast access of data in memory because the microprocessor does not have to perform all the steps of addressing, reading, and writing to a destination. The video processor needs the fast access because the data rate required to display a line of characters on the CRT is greater than the microprocessor can handle.

6.3.15 Video Processor

The microprocessor puts displayable data in the screen RAM. The video processor direct memory accesses (DMAs) data a line at a time from the RAM. It converts the ASCII-encoded data into streams of pulses that, when converted to light on a CRT screen, appear to form characters on the screen. Custom ICs provide the complex timing and control signals required for this conversion. The video processor can be pro-

grammed by the user to perform the conversion at different rates (called refresh rates) to minimize flicker at different power line frequencies. A number of other aspects of video processor operation can be programmed as well.

6.3.16 CRT Monitor

The cathode ray tube (CRT) monitor is a simplified, monochrome television set. It converts electrical pulse streams into dots of light by using a moving electron beam to excite a phosphor on the face of the tube. A video input from the video processor enters a cathode drive circuit that regulates the strength of the electron beam. The cathode driver is a linear amplifier that allows the CRT to display different intensities (gray scale). The monitor uses timing pulses from the video processor to drive the horizontal and vertical electron beam deflection circuits. These circuits cause the beam to travel down the screen slowly while rapidly moving sideways to draw horizontal traces called scans. This beam movement produces a pattern that is called a raster; the display system is called raster scanning. Because the beam repeatedly passes by each location on the screen, the video processor, synchronizing its output with the motion of the beam, makes rows of dots of light align forming characters.

The screen does not hold its image after the electron beam has painted dots on it. For the eye to perceive it as continuously illuminated (that is, without flickering) the screen must be repainted, or refreshed, repeatedly – some 30 or more times per second. Stray magnetic fields and electrical noise at the power line frequency can also cause distortions in the display. If the refresh frequency is different from the power line frequency, the distortions appear to move up or down the display. This is very noticeable. Most distortions disappear by matching the refresh rate to the power line frequency. The VT100 can refresh at either of the two world power frequencies, 50 Hz or 60 Hz, satisfying both flicker and distortion requirements. (Refresh is not locked to the power line but is close enough to conceal most distortions.)

The CRT monitor, the monitor circuit board, and the flyback transformer are replaceable subunits of the basic VT100.

6.3.17 Power Supply

The power supply provides enough power to run the basic terminal and a few options. It is a switching-type power supply to allow highest efficiency and to minimize the heat load on the rest of the terminal. It rectifies line voltage directly (without a transformer) and uses a transistor to chop the resulting high dc voltage to about 30 kilohertz. This ultrasonic ac is stepped down in a relatively tiny transformer and then regulated at low voltage to give the various outputs. The power supply is a replaceable subunit of the basic VT100.

6.3.18 Standard Terminal Port

The standard terminal port (STP) is a shorting connector in series with the communications port, the modem control lines, and some power and timing lines. By connecting to the terminal through this port, options can exchange signals with the terminal controller or intercept terminal host communications from inside the terminal cabinet.

6.3.19 EIA Drivers and Receivers

The Electronic Industries Association (EIA) interface used on the terminal controller module is the RS-232-C unbalanced bipolar voltage standard. The terminal controller has two types of ICs that provide conversion between EIA levels and the TTL levels used on the controller board. One IC is a line driver that outputs EIA levels for TTL inputs, and the other is a receiver that senses the EIA levels on the input line and converts them to TTL.

6.4 FIRMWARE INTRODUCTION

Figure 6-3 portrays the basic VT100 as a system with four levels of operation.

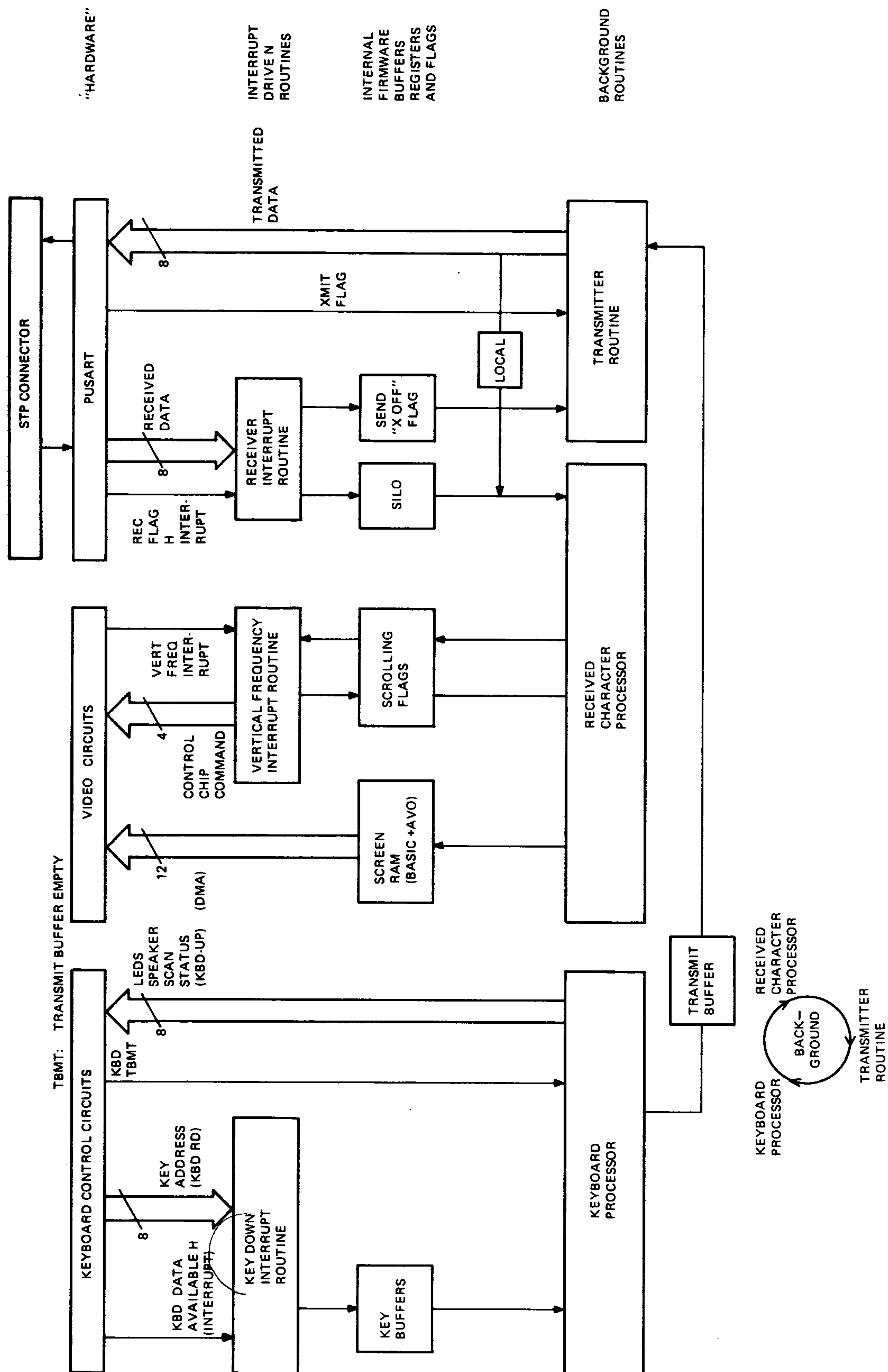


Figure 6-3 VT100 Firmware Block Diagram

At the deepest level, the background routines continually repeat in order to manage functions that do not require precisely timed responses. The keyboard processor commands the keyboard to perform address scans, controls the bell and LEDs, and manages the conversion of key information from hardware-dependent codes to ASCII. The transmitter routine manages the transmission of ASCII data to the host. The received character processor examines incoming data, manages the silo, initiates special functions as specified in the data, and writes displayable data into the screen RAM. When the terminal is in local mode, a logical shortcut bypasses the communication process and allows the keyboard data to enter the received character processor directly.

The background routines work on the internal buffers, registers, and flags, which are logical devices located in hardware and RAM. These are physical locations in hardware that contain information placed there by the hardware and by the firmware. The key buffers store up to three key addresses for the keyboard processor to pass through the transmit buffer to the transmitter routine for transmission to the host or CP/M processor. The screen RAM, which stores the displayable data, is the largest segment of RAM. The scrolling flags contain data for the scrolling process in the video processor. The silo stores data coming from the host in case the received character processor cannot transfer data to the screen RAM as fast as it arrives. The send XOFF flag, set by the silo manager, signals the transmitter routine to send the XOFF code to the host to halt transmission and prevent silo overflow.

Interrupt routines are segments of the firmware that take precedence over other business in the microprocessor because of the short-lived nature of the data that they handle. The key down interrupt routine is initiated by the appearance of data at the keyboard control circuits. It instructs the microprocessor to get the key address from the keyboard UART and put it in the key buffer. The vertical frequency interrupt routine occurs every fiftieth or sixtieth of a second and provides synchronization of video routines with the actual display timing. The receiver interrupt routine moves incoming data from the communication transceiver to the silo.

At the exterior level of the VT100 system, the hardware responds to the firmware by exchanging data between the user and the host computer or CP/M processor in forms that are understandable to each.

6.5 TERMINAL CONTROLLER DESCRIPTION

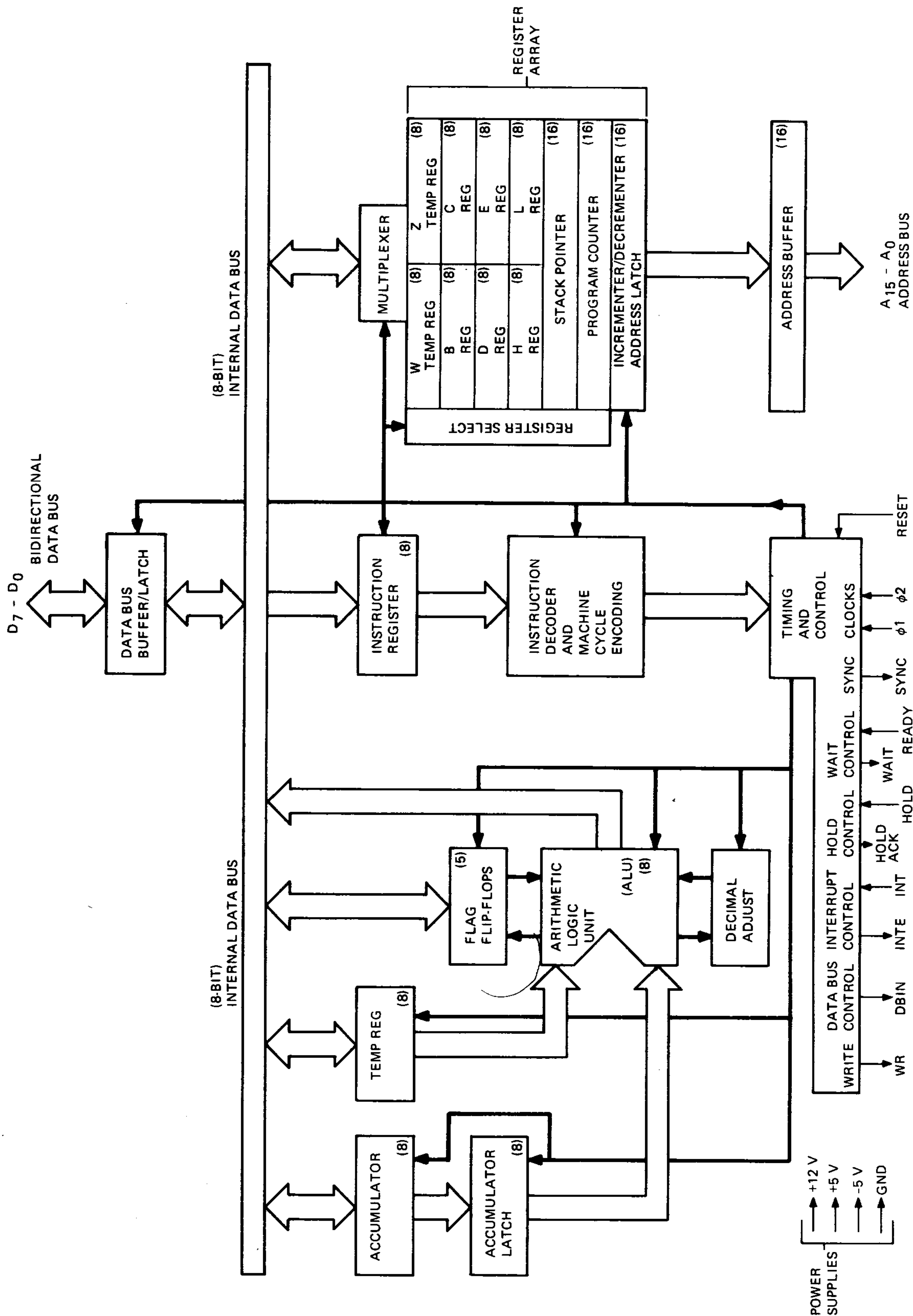
The 8080 microprocessor residing on the terminal controller module controls all of the basic VT100 functions. The 8080 performs all of the usual functions of a stored program computer, fetching instructions and data from ROM and RAM and responding to service requests from various devices in the system. Because of technical limitations in the implementation of the microprocessor hardware, some high-speed counting and timing circuits and some power circuits are located in peripheral ICs made with a different semiconductor technology. These components are bipolar (8224, 8228) while the 8080 is NMOS.

6.5.1 8080 Microprocessor

The 8080 (Figure 6-4) contains a set of general and special purpose registers (the register array), timing and control logic that responds to machine code instructions, and an accumulator and arithmetic logic unit that perform the computations associated with the microprocessor operation.

The stack pointer is an important register that points to the bottom of the stack. The stack is a last-in/first-out area in RAM that stores information about the current process when a subroutine or interrupt branches away from the current instruction sequence. By storing this information at the beginning of an interruption and restoring it at the end of the interruption, the 8080 can continue the main program without any disturbance. This is the meaning of the interrupt process as it applies to the interrupt-driven routines mentioned in the firmware block diagram in Figure 6-3.

Most of the pins on the 8080 are tristate data and address lines. Four pins are power supplies and ground. Descriptions of the others follow.



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Figure 6-4 Microprocessor Block Diagram

HOLD is an input that lets another device get control of the buses when the 8080 finishes the current machine cycle. Hold request from the video processor is the input signal.

HLDA (hold acknowledge) output indicates that the buses will be given up for the hold state.

INT (interrupt request) input accepts an **INTR H** signal that causes a read of the interrupt vector address and a branch to it.

READY is input for use with slow memory or I/O. If low, the 8080 enters the wait state (an indefinite portion of a machine cycle). It is not used in the VT100.

WAIT is output acknowledging the wait state. It is not used by the VT100.

INTE (interrupt enable) output indicates whether interrupts have been enabled or disabled with the related instructions or by servicing an interrupt request. It is not used by the VT100.

0/1, 0/2 are clock phases 1 and 2. These are inputs to drive the 8080.

SYNC is output that indicates the beginning of each machine cycle. It combines with the clock in the 8224 to produce status strobe (**STSTB**).

RESET clears the program counter so that when it is released, the program starts at location zero. It is used to initiate the power-up sequence and self-test.

WR (write) output controls memory and I/O writes by indicating the stable period of the data bus during a write instruction.

DBIN (data bus in) output indicates that the data bus can accept data.

For more detail, see Intel Corporation's 8080A manual.

6.5.2 Data Bus and System Controller

The microprocessor data bus passes directly to the 8228 bus driver and system controller. This device provides TTL output buffering and level translation for the MOS 8080 bus. Because of the large number of devices on the data bus, the drive capability of some devices would be exceeded at times if all devices were on the same bus. (The keyboard UART is the weakest low-level current driver.) To distribute the load, the bus is split into those devices that communicate bidirectionally or are only read by the microprocessor and those that are only written into. Read and writable devices are on the bidirectional data bus (**DB**). The write-only devices are driven by a one-way bus buffer and are on the data output (**DO**) bus. The terminal controller block diagram (Figure 6-5) shows which devices are on each bus.

The ROMs do not have sufficient high-level current capacity to drive all of the other inputs on the bus. Inactive devices have their outputs tristated, but their inputs still draw enough current to accumulate a significant load over the entire bus. Pull-up resistors are connected to the bus to provide the additional current required. Their resistance is selected to supply enough current to meet high-level needs on the bus without exceeding the low-level sink capacity of any driving device.

Pull-up resistors are used on the output-only **DO** bus because the baud rate generator, a MOS device, has an input threshold higher than TTL driver E58 is guaranteed to deliver. Pull-up resistors ensure that the data lines rise enough.

An additional function of the 8228 is a combination logic decode of the 8080 status byte. This byte, output by the 8080 at the beginning of each machine cycle, contains flag bits indicating the nature and function of the cycle. The byte is latched into the 8228 by the status strobe (STSTB) signal from the clock generator. In combination with three control output bits from the 8080, the system controller produces interrupt acknowledge (INTA), memory read and write (MEM WR,RD), and input/output read and write (I/O WR,RD). These signals reduce the external decoding requirements while saving pins on the 8080 package.

When the video processor asserts hold request during a direct memory access (DMA) of the screen RAM, the 8228 floats its outputs. Since these include the memory control signals, the video processor must provide its own memory control. The DMA enable signal, buffered into the MEM RD line by gate E28 (pin 13), provides memory read enabling during the DMA. The other control signals are pulled high by the pull-up resistors.

6.5.3 Clock Generator

The 8224 provides the asymmetrical two-phase clock required by the 8080 logic. Its running frequency is crystal-controlled. An LC circuit on the tank input improves the crystal's mode stability. The capacitor in series with the crystal compensates for internal phase shifts in the 8224 at the high operating frequency. The 24.8832 MHz crystal frequency gets divided by 9 to produce a 361.69 ns clock period. The buffered TTL phase 2 output clocks the PUSART and the baud rate generator. The system clock period for the microprocessor is 361.69 ns.

The sync signal from the 8080 combines with an internal clock phase to produce the status strobe (STSTB) during the last ninth of the first state of each machine cycle. STSTB latches the status byte into the 8228 system controller.

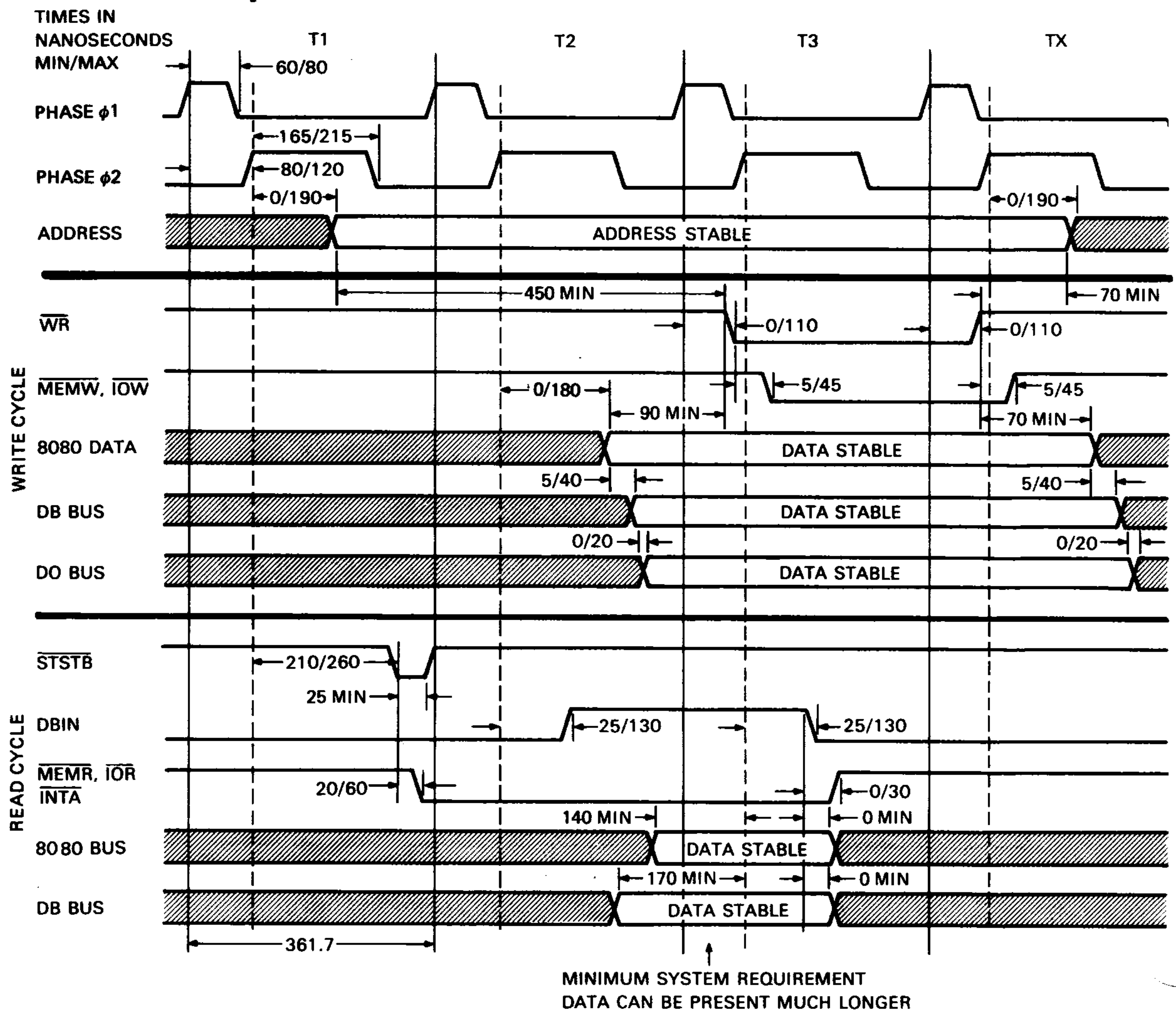
The ready input is not used in the VT100. It is an asynchronous input that gets synchronized to the machine cycles in the 8224. The synchronized signal can cause the microprocessor to enter a wait state during a memory access to wait for slow memory to respond. Memory used in the VT100 matches the processor speed so ready is not used.

The reset input is a Schmitt trigger. Its input is the +5 volt supply delayed by an RC circuit with a diode bypass for fast discharge. The reset input is held low until well after all power supplies have settled. When the capacitor voltage reaches the Schmitt threshold, reset is released and the microprocessor begins operation at memory location 0 (the start of the firmware ROM). The inverted and noninverted reset signals clear other portions of the terminal controller.

6.5.4 Bus Timing

The bus timing diagram in Figure 6-6 illustrates the basic time relations between the address, data, and control lines in the microprocessor system. The figure distinguishes between write and read cycles, with the exception of the three top lines. These show the constants of the system: the two clock phases from which all timing is derived, and the address bus that always provides the current address for either kind of cycle early in the cycle. Numbers on the diagram represent specified minimum/maximum nanoseconds between signals for normal operation.

Starting with the write cycle, note that the status strobe signal (STSTB L) shown in the read section occurs at the same point in the write cycle. Therefore, the status strobe latches the status byte into the 8228 during the first clock cycle. The 8228 delivers the decoded memory write L or I/O write L (MEMW or IOW) signals in the third clock cycle when data to be written is stable. The 8080 data bus, DB bus, and DO bus graphs show the propagation delays between the three buses. The 8080 bus is the output pins on the chip. The DB bus is the output of the buffered 8228 bidirectional bus, and the DO bus is the unidirectional buffered output-only bus.



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Figure 6-6 Microprocessor Bus Timing

In the read cycle, the memory read L signal (along with I/O read L and interrupt acknowledge L: MEMR, IOR, INTA) starts early to enable the chip selects and allow the data buses to stabilize. Data bus in (DBIN) goes high before data settles but does not latch data into the 8080 until its falling edge, when data is settled. The two bus graphs show the assertion of stable data and also show the delay through the bidirectional bus buffer to the 8080 data bus.

6.5.5 Microprocessor Memory

The basic terminal controller contains 8192 bytes (8K bytes) of program ROM and 3072 bytes (3K bytes) of static RAM. (One byte equals eight bits.) The original board utilizes four 2K by 8 ROM ICs; later versions may use a single 8K by 8 ROM. The RAM is six 1K by 4 ICs arranged in pairs. The microprocessor can address up to 64K memory locations. Some of these locations are reserved for future expansion. The memory map of Table 6-1 shows the portions of addressable space that are reserved as well as those areas that are available for new applications.

Table 6-1 ROM and RAM Memory Map

K Bytes	Address (Hex)	Description		Physical Location
0	0000 1FFF	8K × 8	Basic ROM	TCB*
8	2000 2BFF	3K × 8	Screen and scratch RAM	TCB*
11	2C00 2FFF	1K × 8	AVO screen RAM	AVO**
12	3000 3FFF	4K × 4	Attribute RAM	AVO**
16	4000 7FFF	16K × 8	Unassigned	
32	8000 9FFF	2K × 8 2K × 8 2K × 8 2K × 8	Program memory expansion (use 2K × 8 ROM/EPROM)	AVO**
40	A000 BFFF	8K × 8 8K × 8	Program memory expansion (use 8K × 8 ROM)	AVO**
48	C000 FFFF	16K × 8	Unassigned	
64				

*TCB = Terminal controller board

**AVO = Advanced video option

6.5.5.1 Memory Map – The basic terminal controller board contains 8K bytes of program ROM and 3K bytes of screen and scratch RAM. These account for the locations from 0000H to 2BFFH in memory. The advanced video option adds another 1K byte of RAM (2C00H to 2FFFH) to increase the number of characters that can be displayed. The AVO also contains additional memory for character attributes. This memory is only 4 bits wide, but to address each location in correspondence with each of the 4K characters, it uses another 4K of addresses from 3000H to 3FFFH.

The next 16K locations (4000H to 7FFFH) are unassigned. However, 4000H to 4FFFH can be addressed by the video processor using the DMA address counters, so 4000H to 4FFFH could be used for additional screen RAM with 5000H to 5FFFH as associated attribute storage.

Above 7FFFH is an 8K area intended for additions or changes to the program ROM in 2K segments, and above that is an area intended for the same purpose but in one 8K segment. The top 16K are unassigned.

6.5.5.2 Memory Devices – Each ROM has three ANDed chip select inputs that are mask-programmed to be either active-high or active-low. This eliminates the need for external inverters. The two address lines, A11 and A12, are decoded to select one of four ROMs. The third chip select line is common to all four ROMs. In later VT100s, jumpers W2 and W3 can be used to select either a high or low assertion for this single chip select to allow for 64K ROMs that do not have a programmable chip select. Table 6-2 shows the addressing of the ROMs.

Table 6-2 ROM Chip Select Addressing

Address Line 11	Address Line 12	Chip Select 2	Chip Select 3	ROM Selected
0	0	Active low	Active low	1
1	0	Active high	Active low	2
0	1	Active low	Active high	3
1	1	Active high	Active high	4

6.5.5.3 ROM Decoding – The program ROM is enabled when the top half of memory decoder E31 is enabled and the correct address space is requested by the microprocessor. MEM RD or MEM WR from the 8228, in the absence of MEM DISABLE, enables the decoder. The ROM is in addresses 0H to 1FFFH, so A13 (the 8K bit) is not asserted during ROM reads. Bit A12 is low or high for 0–4K or 4–8K sections of ROM. The decoded outputs from both states are ORed to provide one of the select signals for the ROM. Then bits A11 and A12 at two of the chip select lines enable the outputs in one of the 2K segments. The low 11 bits address one of the 2K bytes in the enabled ROM. If the program is in one 8K ROM, A11 and A12 are used as regular address lines; only one chip select line enables its outputs.

6.5.5.4 RAM Decoding – If A13 is asserted, the memory space between 2000H and 3FFFH is being addressed. The ROM outputs are disabled and the decoded output from the top half of the decoder enables the bottom half. Now bits A10 and A11 are decoded to select 1K segments of the screen RAM. The 1K by 4 RAMs are paralleled in pairs to make each location eight bits wide. There is 3K on the basic video board. The fourth 1K is located on the AVO; its addressing is decoded separately.

6.5.5.5 Memory Disable – Memory disable turns off all memory on the terminal controller board. It is used by options that plug into the advanced video option connector:

1. To replace (overlay) existing memory
2. To disable the terminal controller memory when using memory above 4000H (since the terminal controller does not decode A14, A15).

The advanced video option can contain overlaying program memory. This is a set of address locations and the AVO can be jumper programmed to decode and provide data for these locations. Since the main memory may also be decoding the same location, the AVO must assert MEM DISABLE to disable the main memory (ROM and RAM) so that only one data byte is asserted on the bus.

6.5.6 I/O Decoding

The I/O address space is divided into two regions. One contains the 8251 PUSART and has address bit A01 always low; the other region contains all other I/O devices and has bit A01 always high. The list of I/O addresses in Table 6-3 illustrates this by the presence of hex 2 in the low half of each non-PUSART address byte.

Table 6-3 List of Hex I/O Addresses

Address	Device
Read or write	
00H	PUSART data bus
01H	PUSART command port
Write-only (decoded with I/O WR L)	
02H	Baud rate generator
42H	Brightness D/A latch
62H	NVR latch
82H	Keyboard UART data input
A2H	Video processor DC012
C2H	Video processor DC011
Read-only (decoded with I/O RD L)	
22H	Modem buffer
42H	Flags buffer
82H	Keyboard UART data output

6.5.6.1 PUSART Read and Write – When bit A01 is low, the PUSART is enabled. The I/O RD and WR signals from the 8228 control the read or write operation. Address bit A00 selects either the command or data register for the I/O operation.

6.5.6.2 I/O Read and Write – When bit A01 is high, the PUSART is disabled. Bit A01 high is one of two signals required to enable the I/O write decoder (E27). I/O WR is the other signal. Address bits A05, A06, and A07 select one of the seven writable I/O devices. These are the baud rate generator, the brightness control D/A latch, the NVR latch, the keyboard UART transmit buffer, the DC011 video timing chip (E6), and the DC012 video control chip (E5).

Only three I/O devices are readable, so their addresses were chosen to allow read decoding directly from the three address lines. When the 8228 asserts I/O RD, I/O WR deasserts and decoder E27 is disabled. I/O RD enables the gates in E34 to allow reading of the keyboard UART receive buffer, the flag buffer, or the modem control signal buffer, depending on which address bit is asserted.

6.5.7 Interrupt Vector

When any of the three interrupting devices (communication receiver, vertical frequency, or keyboard) sets interrupt request (INTR H) through gate E23, the current instruction is completed. Then the microprocessor sets its interrupt acknowledge (INTA) status bit and performs an instruction fetch. The address requested in the fetch is the contents of the program counter. Its value is ignored in the interrupt process, but it is not incremented as it would be in a normal fetch cycle. The INTA bit is decoded from the status word in the 8228 system controller; it enables the tristate interrupt vector buffer (E41), which then presents a restart (RST) instruction to the data bus. Main memory does not conflict with the vector buffer because the 8228, in decoding the interrupt status word, does not produce the memory read or write command bits needed for address decoding. (Refer to Table 6-4.)

Table 6-4 Interrupt Addresses

Address (Hex)	Interrupting Device
00H	Power-up (not hardware driven)
08H	Keyboard
10H	Receiver
18H	Receiver and keyboard
20H	Vertical frequency
28H	Vertical frequency and keyboard
30H	Vertical frequency and receiver
38H	Vertical frequency, receiver, and keyboard

The RST instruction disables further interrupts, pushes the current program counter contents (the location of the next instruction in the interrupted program) onto the stack, and decrements the stack pointer. Then the program counter is loaded with the bits in the address field of the RST instruction. This field is produced by the interrupt signals of the interrupting devices. The signals are passed onto the data bus as bits in the address field (bits 3, 4, and 5). The rest of the instruction is hardwired through diodes that supply high level to the other data bits during INTA and that are reverse-biased to isolate these data bus lines when the vector buffer is inactive.

The RST address field, when mapped into the same bit locations in the program counter, defines a set of eight 8-byte long memory spaces at the beginning of the memory. The first address, 0, is the starting point for the terminal controller program and is not used for interrupts. The program is normally started by a hardware reset signal that sets the program counter to 0. It can also be started by an escape sequence that the host can send to force the program to jump to zero, or in set-up mode the RESET key can be pressed. The other seven memory spaces, starting at 8, 16, etc., contain jumps to places in an interrupt handling routine that can mediate requests for service from any of the seven combinations of interrupting devices.

At the end of the interrupt service routine, the stack is popped, interrupts are enabled, and the interrupted program continues.

Early VT100s can disable the receiver interrupt by programming D4 in the NVR latch. However, this is never used by the VT180. Later VT100s have the ability to add a communications transmit buffer empty interrupt by adding W6. The 8080 would then have to distinguish transmit and receive interrupts by testing the transmit flag on the flag buffer. This provision is not used on the VT180.

6.5.8 Communication Transceiver

The terminal controller module interfaces to the CP/M processor or host computer through the standard terminal port (STP) connector. An 8251 programmable universal asynchronous receiver-transmitter (PUSART), illustrated in Figure 6-7, drives the STP port. This device takes parallel data from the transmit buffer on the terminal control module, converts the parallel data to a serial format, and transmits the data through the STP connector. Data from the CP/M processor or host computer is received in serial format by the PUSART, converted to parallel data, and sent to the silo for processing. Three kinds of data can be exchanged between the basic VT100 and the CP/M processor or host computer: control characters, control functions, and displayable characters.

PUSART clocks are derived from the microprocessor clock. The microprocessor clock crystal was selected to provide a frequency within the limits of the 8080 that could be readily divided to provide standard baud rates. The division occurs in programmable baud rate generator E60 (see Figure 6-5). This device contains two independent counters that allow different receive and transmit baud rates (split baud rates). Each counter has 4 input lines to select 1 of 16 rates. Thus, a 1-byte load into the device can set up both send (transmit clock) and receive (receive clock) rates. The baud rate generator's input register is written into as a device in the I/O address space.

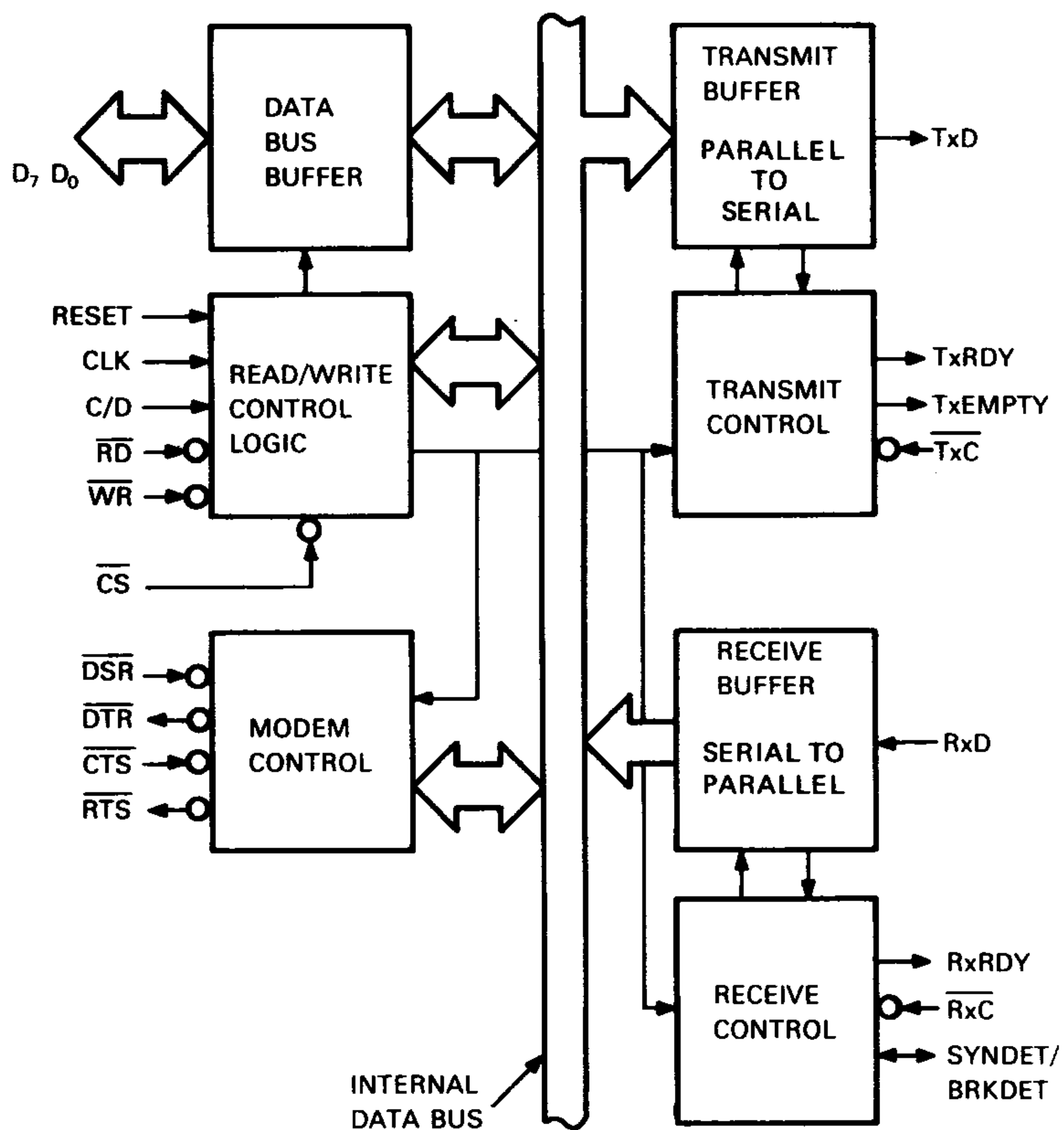
The baud rate generator E60 is factory mask-programmed with the division ratios required to get standard baud rates from the crystal frequency. The 4-bit input is an address for a ROM location containing the set-up information for each rate. The outputs of the baud rate generator are sent to the PUSART as the transmitter (TxC) and receiver (RxC) clock signals.

Certain pins on the PUSART are labeled with standard modem control designations. These pins are readable [data set ready (DSR)] or writable [data terminal ready (DTR) and request to send (RTS)] as buffered bits in the PUSART's status and control bytes. Other signals from the modem pass through EIA level translators with Schmitt trigger inputs to a tristate buffer that, when enabled by the MODEM RD command, presents them to the data bus. Another signal [speed select (SPDS)] is written from the data bus into the NVR latch, which is a convenient extra latch position. None of these signals are used to support modem control in the basic VT100. See Chapter 3 for more interface information.

6.5.8.1 Data Transmission – When the microprocessor wants to send a character out, it checks the XMIT flag at the flag buffer. If this flag is high, the transmit buffer is empty and can accept data. If the flag is low, the microprocessor continues through its background program and returns to check again later.

When the flag is high, the microprocessor loads a data byte into the transmit buffer. The PUSART is double-buffered; this means that there is a second data buffer inside that is automatically loaded from the first buffer. The second buffer's contents get start and stop bits and parity (if enabled) appended and are shifted out by the continuously running clock. Immediately after the second buffer is loaded, the transmit flag goes high and the first (transmit) buffer can be loaded again.

6.5.8.2 Data Reception – Any data that appears on the receive data line is shifted into the internal receive shifting buffer. When a full character of bits has arrived, the start, stop, and parity bits are stripped. Parity is checked, and if bad, the parity error flag in the status word is set. Data is transferred to the receive data buffer, and the receive flag is set. This flag requests an interrupt from the microprocessor. The microprocessor then has the amount of time it takes the next character to shift in, to read the first character. After reading the character, the microprocessor reads the status byte to check the integrity of the data. If the microprocessor does not read the receive data buffer in time, the second character writes over the first one. The first character is lost and an overrun error is reported in the status word. The checkerboard character appears on the screen for all errors.



PIN NAME	PIN FUNCTION
D ₇ D ₀	DATA BUS (8 BITS)
C/ D	CONTROL OR DATA IS TO BE WRITTEN OR READ
RD	READ DATA COMMAND
WR	WRITE DATA OR CONTROL COMMAND
CS	CHIP SELECT
CLK	CLOCK PULSE (TTL)
RESET	RESET
TxC	TRANSMITTER CLOCK
TxD	TRANSMITTER DATA
RxC	RECEIVER CLOCK
RxD	RECEIVER DATA
RxRDY	RECEIVER READY (HAS CHARACTER FOR CPU)
TxRDY	TRANSMITTER READY (READY FOR CHAR. FROM CPU)
DSR	DATA SET READY
DTR	DATA TERMINAL READY
SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT
RTS	REQUEST TO SEND DATA
CTS	CLEAR TO SEND DATA
TxEMPTY	TRANSMITTER EMPTY

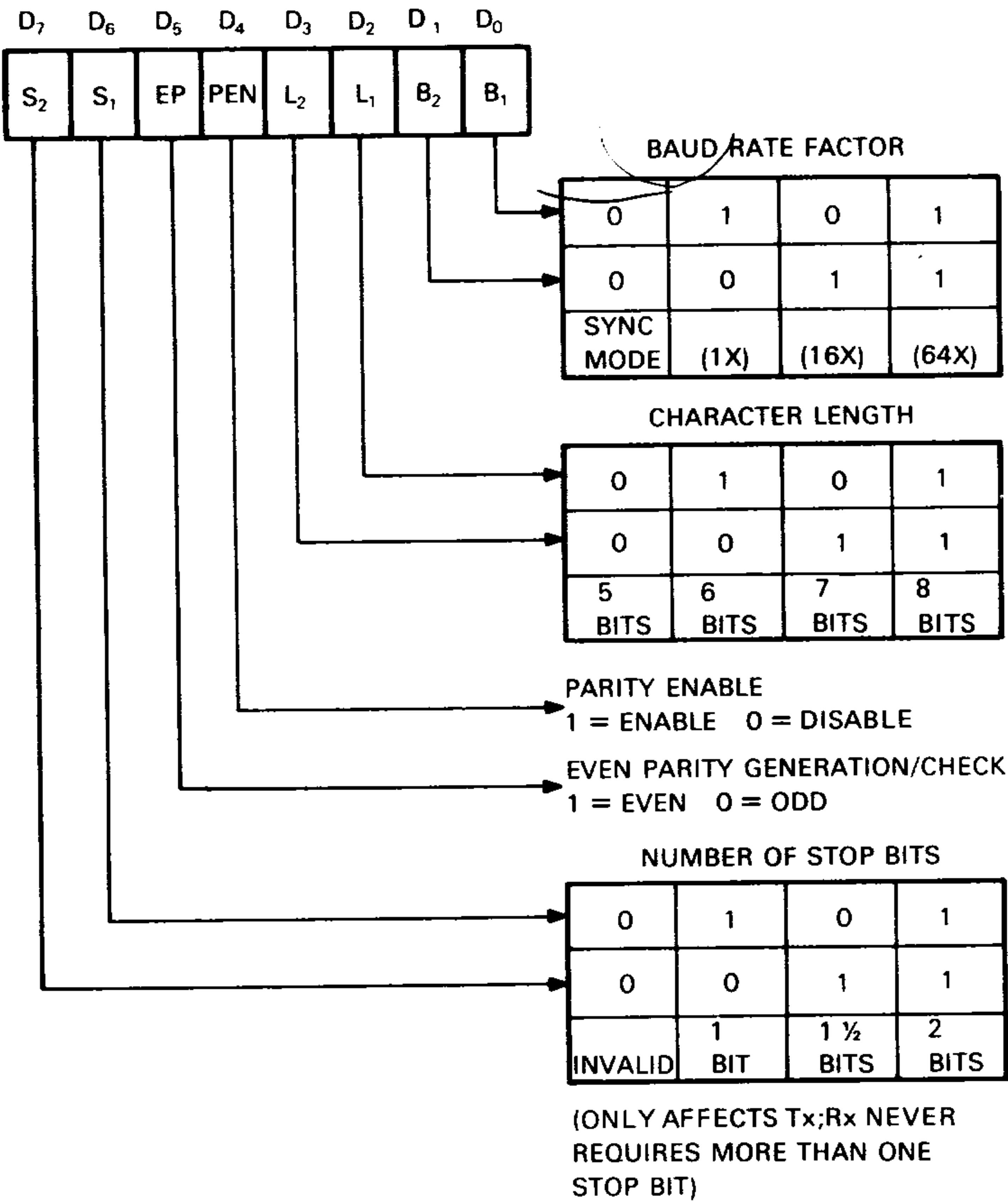
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Figure 6-7 8251A PUSART Block Diagram

The microprocessor checks each received character as it comes from the PUSART. Only four characters cause any special action at this time. Control codes XON and XOFF are immediately processed while NULL and DELETE are discarded. Everything else gets put in a 64 character (128 characters in later model terminals) first-in/first-out space in the scratch area of RAM called the silo (Figure 6-2). The silo processor routine maintains this area by updating two locations called SILIN and SILOUT. After the current action is finished, the microprocessor gets the longest-waiting character out of the silo and range checks it. If it is less than 20 H, it is a control character and the microprocessor processes it. If it is 20 H or above, the microprocessor puts it in the next character position in the screen RAM.

When the VT180 is in local mode, the communications transmitter and receiver and silo are bypassed and any inputs from the keyboard are acted on immediately by the microprocessor. The data terminal ready signal (DTR) is unasserted in local mode.

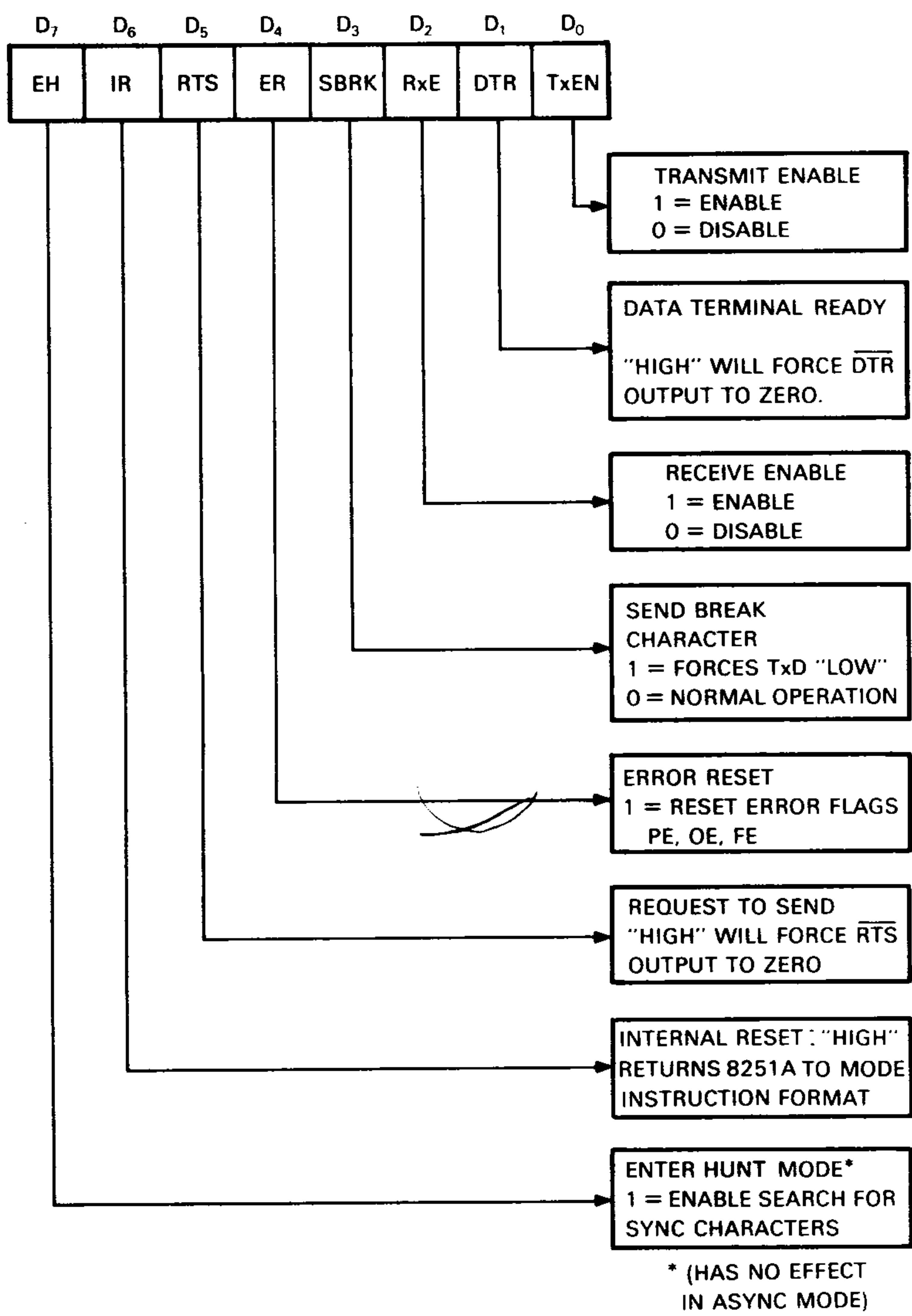
6.5.8.3 PUSART Programming – The microprocessor can program the PUSART to operate with several standards and parameters. Many of these parameters are predetermined by the VT180 specifications. Character length, number of stop bits, parity enabling and format, baud rate multiplication factor, and asynchronous operation are all programmed in at power-up through the mode instruction (Figure 6-8) from the stored set-up information. Address bit A00 selects either the command register in the PUSART for writing the byte containing this information or the transmit buffer for normal operation. The programmable baud rate generator provides the selected baud rate from set-up data.



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Figure 6-8 Mode Instruction

After the PUSART mode of operation is selected by writing a mode instruction, PUSART operation is controlled by writing a command instruction (Figure 6-9). Once the mode instruction has been written into the PUSART, all further control writes (C/D=1) load a command instruction. A reset operation (internal or external) returns the PUSART to the mode instruction format.



NOTE: ERROR RESET MUST BE PERFORMED WHENEVER RxENABLE AND ENTER HUNT ARE PROGRAMMED.

COMMAND INSTRUCTION FORMAT

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Figure 6-9 Command Instruction

The status of the PUSART can be read by the microprocessor by performing a read with C/D=1. Some of the bits in the status word (Figure 6-10) have the same meaning as output pins on the PUSART chip. The status word may be a maximum of 28 clock periods behind the event causing the update. This clock, from the microprocessor's phase 2 TTL signal, is the clock for the internal operation of the PUSART. It is a dynamic device requiring internal refresh at regular intervals.

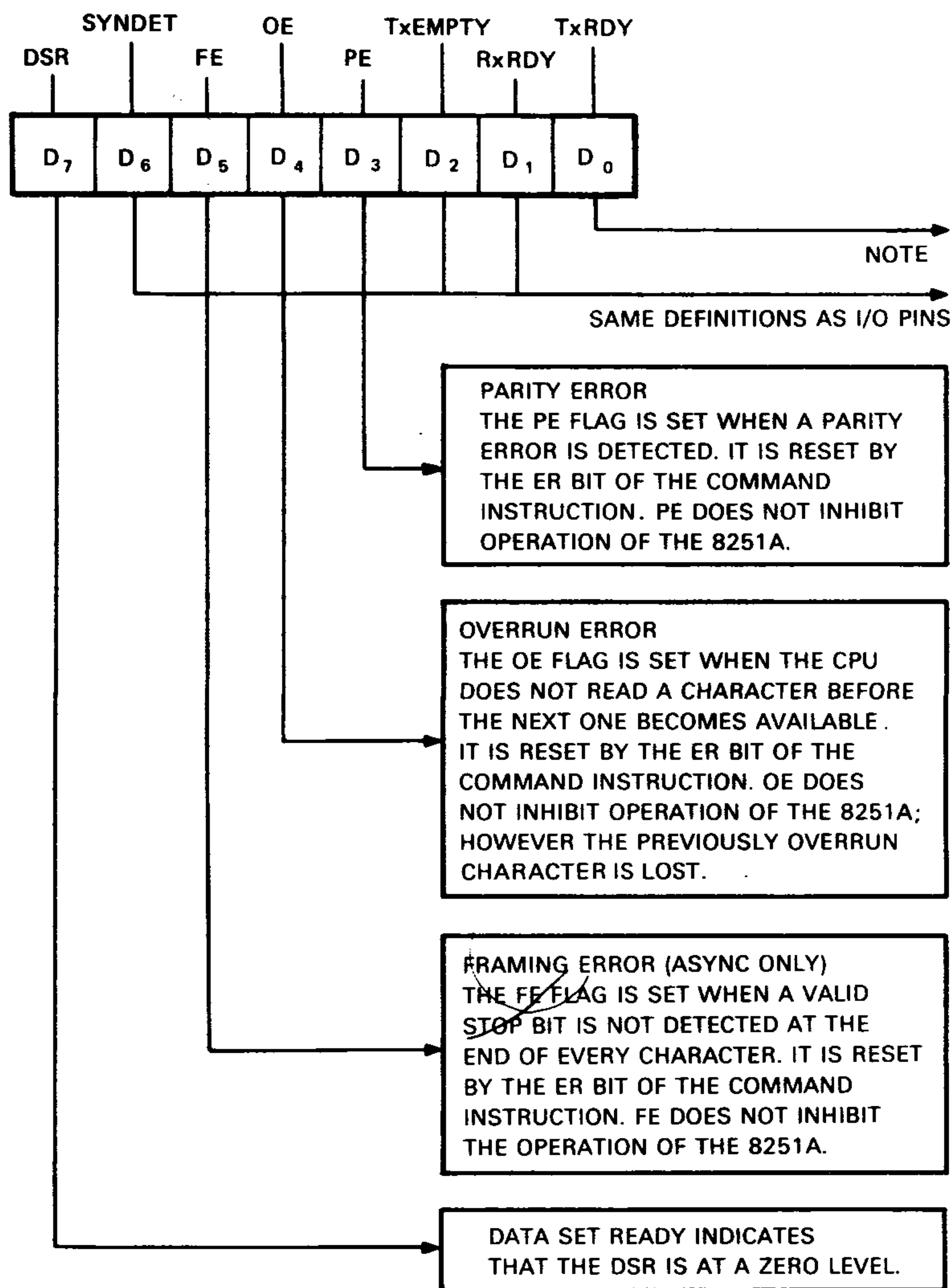


Figure 6-10 Status Byte Format

6.5.9 Standard Terminal Port

The standard terminal port (STP) is a printed circuit board edge connector on the terminal controller module that contains 20 pairs of contacts. When no board is plugged into the connector, the pairs of contacts meet. All EIA data and modem control signals plus the two baud clocks pass through this connector.

When the VT18X control module is connected to the STP connector through the ribbon cable and the VT180 paddle board, some of the EIA data and modem control signals are routed to and from the console, general purpose, and communications PUSARTs residing on the VT18X control module. The EIA data and modem control signals used by the VT18X control module are summarized in Table 6-5.

Table 6-5 EIA Data and Modem Control Signals

STP Pin	Signal	Function
2	CON REC DATA	Console received data from terminal controller PUSART
6	CON XMIT DATA	Console transmitted data to terminal controller PUSART
16	CON DTR	Console data terminal ready from terminal controller PUSART
27	CON CLK	Console operating clock (15.7 k baud) from terminal controller video processor
5	TRM REC DATA	Received data from general purpose serial port connector
8	TRM XMT DATA	Transmitted data to general purpose serial port connector
13	TRM DTR	Data terminal ready from general purpose serial port connector
28	COM TXC	Communication transmit clock from terminal controller baud rate generator
30	COM RXC	Communication receiver clock from terminal controller baud rate generator

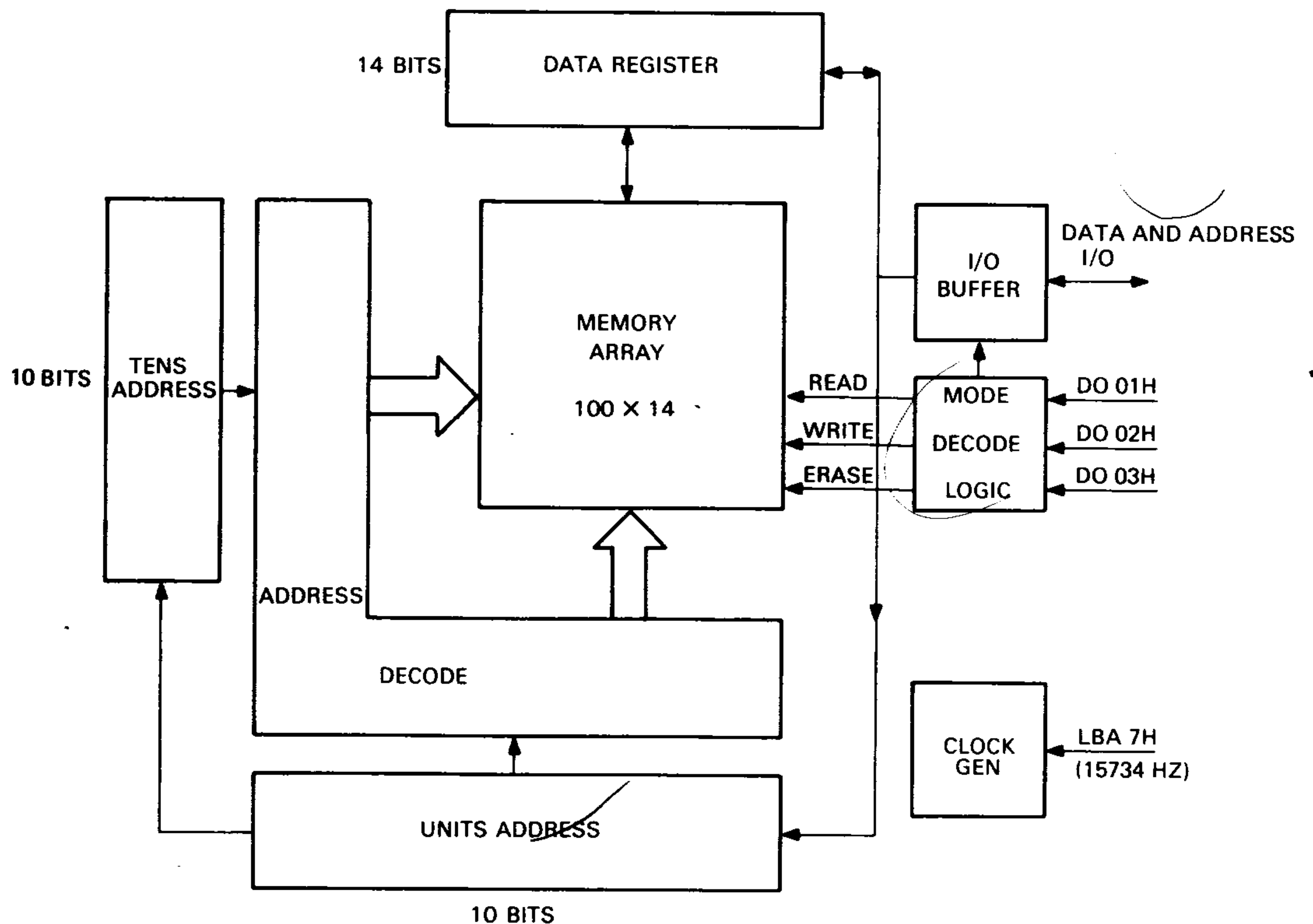
6.5.10 Nonvolatile RAM

The nonvolatile RAM (NVR) is used to store programmable set-up information that would otherwise have to be reentered every time the power was turned on or else stored in mechanical switches.

The ER1400 (NVR) is a 1400-bit memory arranged as 100 14-bit words. Data and addresses enter or leave the device in serial form through a single bidirectional line. Information is shifted with an external clock. Identification of the meaning of the bit stream is made by setting three control lines that specify the operation in progress. The block diagram of the NVR is shown in Figure 6-11.

6.5.10.1 NVR Control – NVR operation is controlled by three data inputs derived from signals obtained from the microprocessor. Seven combinations of these three data inputs are used to specify the NVR command states. These command states determine the operation in progress and are listed in Table 6-6.

6.5.10.2 Microprocessor Management – During an NVR operation, the microprocessor uses 21 bytes of scratchpad memory to set up a group of NVR address or data bits. Each group consists of 20 bits of address or 8 bits of data with another 6 bits of fill for the 14 bit NVR word. These groups must enter the NVR serially, with precise timing. The microprocessor cannot calculate the groups fast enough to keep up with the shifting process while also managing the shifting process, so it saves time by precalculating and storing each group of bits. Then it reads the stored groups and delivers them to the NVR at the NVR clock rate through the NVR latch.



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Figure 6-11 NVR Block Diagram

The microprocessor serializes its data by rotation in a register. It combines the data with command bits to control the NVR device. Output from the microprocessor reaches the NVR through an external NVR latch. The latch is updated at each clock during an NVR operation.

The microprocessor reads the NVR during the power-up process. The bits are deserialized by rotation as they are read in. Although 14 bits from each NVR word are written or read, only 8 bits are used by the microprocessor. The data goes into location in the scratch portion of RAM for use during a later portion of the power-up.

6.5.10.3 NVR Timing – The NVR clock is the lowest frequency line buffer address signal (LBA 7H). It occurs at the horizontal line rate, 15.734 kHz. This is the bit shifting rate during address and data transfers. A read operation requires only a single clock cycle to transfer data into the data register, but an erase or write of a word takes 20 milliseconds.

When shift data out mode is entered, the first data bit may appear, but it will become stable 25 μ s later. Subsequent data bits will be shifted out on the falling edge of the clock flag (rising edge of the signal on pin 5 of the chip) and will become valid 25 μ s later. This means that, following a change to shift data out mode or a falling edge of clock flag during this mode, a delay of 25 μ s must occur before reading of the NVR data flag is attempted. The first bit shifted in when writing is the first bit shifted out when reading.

When using the ER1400, it is necessary to operate with interrupts off.

6.5.11 Keyboard Interface

The keyboard interface is a bidirectional interface that separates incoming data from outgoing data on a single wire. The interface circuits contain a hardwired programmed universal asynchronous receiver-

Table 6-6 NVR Control States

Command State	Control Inputs			NVR Operation
	D003 H	D002 H	D001 H	
0	H	H	H	Standby. The device output floats.
3	L	L	H	Accept address. Two 1 of 10 addresses are shifted in at the clock rate. The first group is the 10's decade and the second is the 1's decade of the 1 of 100 word address.
2	H	L	H	Erase. The word stored at the addressed location is erased to all zeros.
7	L	L	L	Accept data. The data register accepts serial data shifted from the I/O pin. The address register remains unchanged.
6	H	L	L	Write. The word contained in the data register is written into the location designated by the address register.
4	H	H	L	Read. The addressed word is read from memory into the data register.
5	L	H	L	Shift data out. The output driver is enabled and the contents of the data register are shifted out.
1	L	H	H	Not used.

transmitter (UART), a comparator, and supporting gate circuits that encode the transmitted terminal data and keyboard clock. The UART converts parallel data from the terminal controller data out lines (DO 07-00 H) into serial data that is sent to the gate circuits. The gate circuits encode the data and keyboard clocks into a pulse-width modulated signal that is sent to the comparator and then transmitted to the keyboard over the single wire.

Serial data from the keyboard is received by the comparator, converted to TTL voltage levels, and then sent to the serial input of the UART. The UART converts the serial data input to parallel data for transfer to the data bus (DB 07-00 H).

6.5.12 Video Processor

The video processor is the heart of the monitor display. It is composed of the devices shown on the right side of the terminal controller block diagram (Figure 6-5). This section discusses the general mechanism that converts data into a visible display, followed by a discussion of the two central devices (the timing and control chips) and a general discussion of all the other blocks on the video processor side of the block diagram. The interactions between the data paths on the left of the diagram and the processor on the right are covered in Paragraph 6.5.13.

The video processor converts data into an electrical signal that a CRT monitor can turn into visible letters, numbers, and symbols. The video processor works with the characteristics of the CRT monitor to do this. The following is a brief description of these characteristics.

The Raster

The raster is the area on the CRT screen that is scanned by an electron beam moving in a regular pattern. Deflection coils cause the beam to quickly scan a series of horizontal lines while moving relatively slowly down the screen. This scanning repeats quickly and constantly, and persistence of vision makes the entire screen look continuously scanned. The beam may be on or off, lighting the fluorescent phosphor on the face of the CRT or leaving it dark, but the beam's continuous motion traces and defines the raster.

Character Formation

As the beam moves in its horizontal scans, it can be turned on and off very quickly. This means that a spot of light (called a dot) can be produced anywhere along each horizontal scan line. Each scan contains the same number of potential dots. If only one dot is lit in a scan but dots in the same position on several successive scans are also lit, the screen appears to have a vertical line on it. This ability to line up dots on different scans is the key operating feature of the video processor.

Limiting our discussion to 80 column lines for this description, each character that can be displayed on the monitor is made up of a matrix of dots, ten wide and ten high. There are 800 dots in a scan and the raster is made of 240 scans. Therefore, there are 80 groups of 10 dots in each scan horizontally, and 24 groups of 10 scans vertically. Each 10 dot by 10 scan group is a character cell, where a character can be displayed. There are 80 by 24 character cells on the screen. As the electron beam scans the raster, the video processor turns the beam on and off, assembling the characters scan by scan.

Video Processor Data

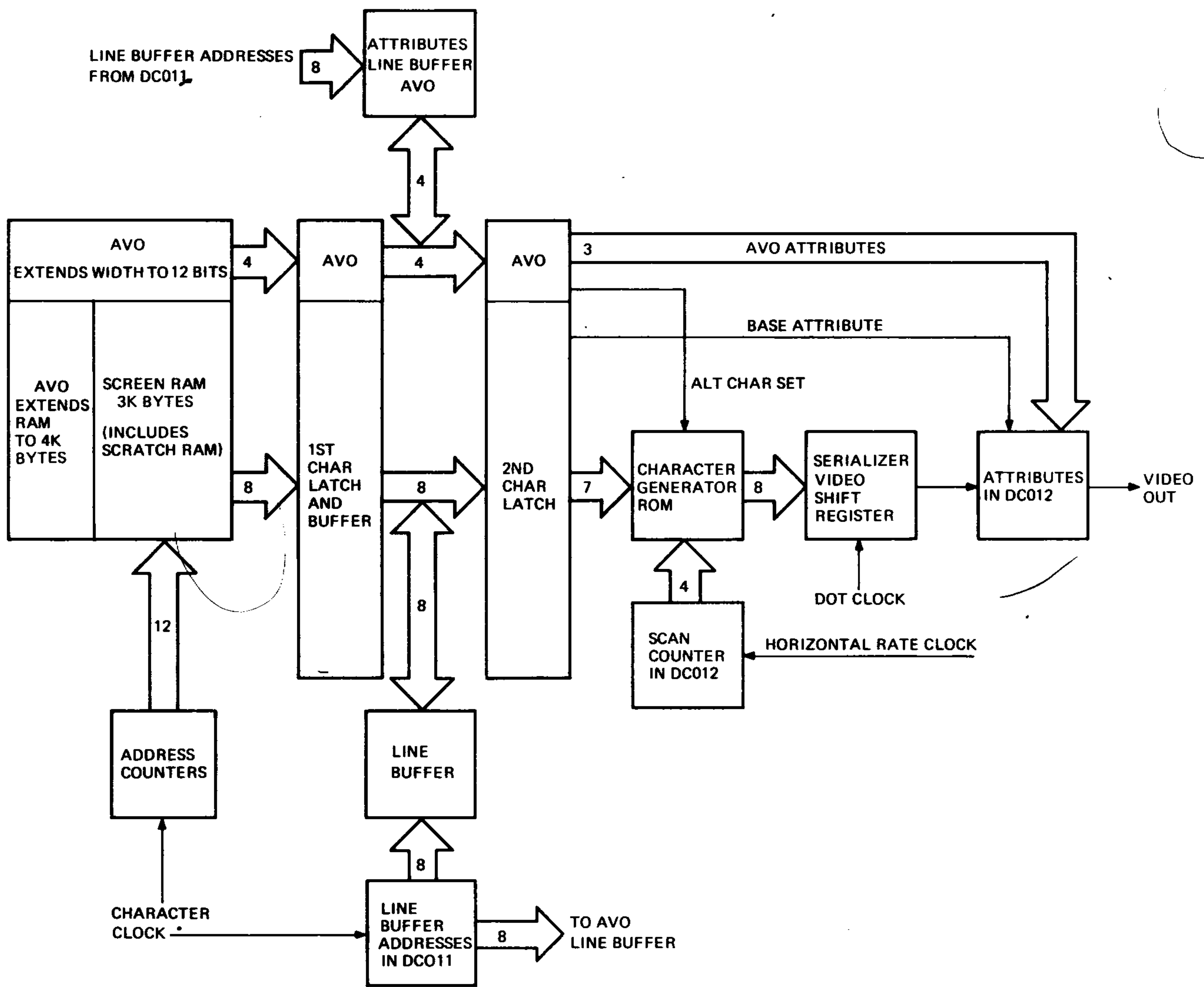
When we say the characters are assembled scan by scan, we mean that only one scan of information about a character is displayed and then the same scan for the next character is displayed. This continues to the end of a line of characters. Then the next scan of the first character is displayed, followed by the same scan of the next character, and so on. Therefore, each character must enter the video processor ten times, once for each scan, and remain only until the next character in the line is displayed.

Each character in a line is stored in one of a group of adjoining locations in the screen RAM. (See Figure 6-12 for the video processor functional diagram.) The process of moving a line of character data from the screen RAM to the video processor takes the same amount of time as a scan. During data movement the microprocessor cannot use the RAM; so, to give the microprocessor as much working time with the RAM as possible, the video processor accepts the line of character data for display during the first scan and stores it in its line buffer at the same time for use during the other nine scans. Movement of data from the screen RAM to the line buffer by the video processor is called direct memory access (DMA). During the DMA, the video processor provides addresses to the screen RAM with the address counters. The data is stored in the line buffer that gets its addresses from the line buffer address (LBA) outputs from the DC011 timing chip. Both kinds of addresses change values when they receive a clock (called character clock) that occurs after each ten dots. This clock makes the character data in the video processor change at the right times to provide proper alignment of the display.

The character latches hold the data coming from the screen RAM or line buffer and ensure that the data remains stable for long enough periods to be written into the line buffer or the video shift register. The buffer between the latches is tristatable and, during non-DMA time, prevents the normal data flow on the microprocessor data bus from interfering with the video processor's reading of data from the line buffer.

Video Processor Character Generation

Data, coming either from the screen RAM for scan 1 or the line buffer for scans 2 through 10, becomes part of an address to a character generator ROM. The rest of the address comes from a scan counter in the DC012 control chip. The scan counter addresses the ROM according to which of the ten scans is to be displayed. The 4-bit scan counter skips over the other 6 possible addresses to the ROM, so the ROM contains data in only 10 out of 16 locations. The output of the ROM is eight bits that represent the pattern of



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Figure 6-12 Video Processor Functional Diagram

sequential dots to be displayed for that character on that scan. The eight bits enter the video shift register, a serializer that converts the eight parallel bits into a 1-bit wide stream. An extra flip-flop stores the last bit so it can be output to the stream two or three extra times (depending on line length) to fill the intercharacter space. The stream enters the DC012 control chip, where the final adjustments for video display are made, and then the video signal goes to the CRT monitor.

Attributes

Three attributes apply to the monitor display: character, line, and screen. Character attributes provide a special appearance to characters as they appear on the CRT screen. In the basic VT100 (without an advanced video option) only one bit of memory (called the base attribute bit) is available to each character on the screen. The original character data from the screen RAM is eight bits wide, but only seven bits define the character itself. The eighth bit defines the base attribute. The attribute bit bypasses the character generator ROM and video shift register and enters the DC012. There it controls the presence or absence of the attribute as that character is displayed. The base attribute is displayed as either reverse video or

underline, depending on the selection of the cursor at set-up. It is invoked by the base attribute bit. Reverse video appears as all ten scans of a character cell reversed (black changes to white and vice versa). Thus, if two vertically adjacent characters are in reverse video, no black space appears between them. Underline forces the ninth scan on. (The ninth scan is forced off with reverse video screen attribute.) Once a character attribute or combination of attributes is set, all displayable characters sent to the terminal have that attribute regardless of where they are placed on the screen. This continues until the attribute selection is changed.

Line attributes are double-height, double-width, and scroll. The monitor displays single-width, double-width or double-height, double-width characters on a line by line basis. All characters on one line appear in the same mode. Double-width lines are generated by displaying each dot of a character twice in the horizontal direction. Double-height, double-width lines are generated by displaying each dot of a character four times (twice horizontally and twice vertically). The top and bottom halves of a double-height, double-width line must be entered as two separate lines of characters. The scroll attribute indicates that a line is part of the scrolling region.

Screen attributes affect the entire screen's characteristics at once. They include the base attribute selection (reverse or underline as mentioned under character attributes), reverse video over the entire screen, 80 or 132 character line length, 50 or 60 Hz refresh rate (chosen according to the local power supply), interlaced or noninterlaced operation, and jump or smooth scrolling of data over the screen.

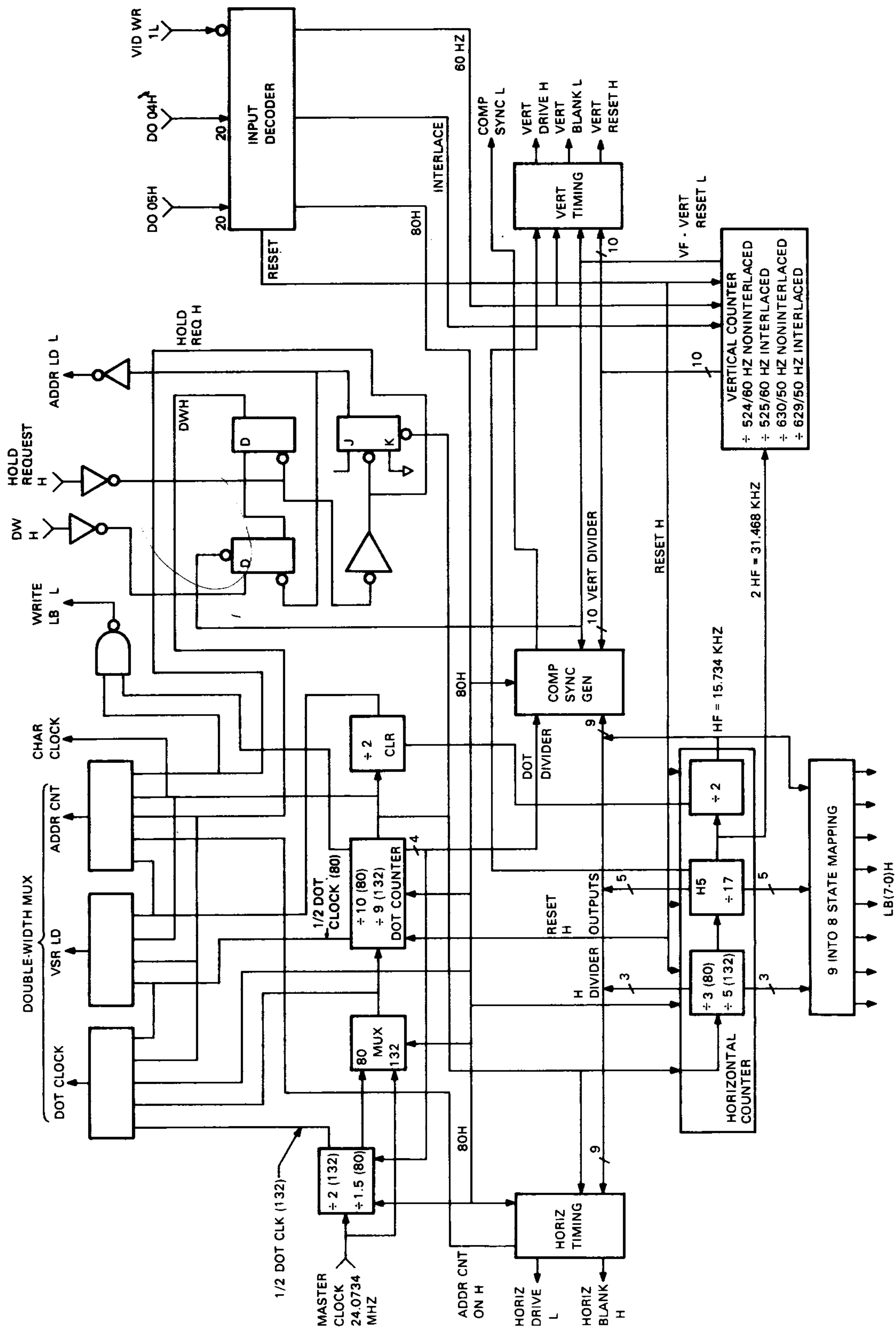
Advanced Video Option (AVO)

The AVO extends the length of the screen RAM so more characters can be displayed in 132 column mode. In addition, it allows each character to have four more attributes, for a total of five. Three of the AVO attribute bits enter the DC012 to control displayable features of each character. The fourth AVO attribute bit controls the selection of an extra character set by switching in an optional alternate character generator ROM that can provide non-ASCII characters or other special displays.

To provide the extra attribute bits, the AVO widens the entire screen RAM by 4 bits to make each character location 12 bits wide. It also contains a 4-bit wide extension of the character latches and a 4-bit wide attribute line buffer, addressed by the same LBA signals as the regular line buffer. This extension treats the attribute data with the same timing as the character part of the circuit and matches each character with its attributes.

With the AVO present, reverse video, underline, bold, and blinking are all available singly or in combination. Reverse and underline appear as described above with the addition that if both reverse and underline are asserted, the underscore is forced dark instead of light. Bold increases the intensity of the display. The blink rate is about half that of the cursor or about 0.5 Hz. Cursor selection is independent of character attributes when the AVO is installed.

6.5.12.1 Timing Chip Description – The DC011 is a custom designed, bipolar, integrated circuit that provides most of the timing signals required by the video processor. Internal counters divide the output of a 24.0734 MHz oscillator (located elsewhere on the terminal controller module) into the lower frequencies that define dot, character, scan, and frame timing. The counters are programmable through various input pins to control the number of characters per line, the frequency at which the screen is refreshed, and whether the display is interlaced or noninterlaced. These parameters can be controlled through set-up mode or by the host. In the following discussion, refer to the block diagram in Figure 6-13.



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Figure 6-13 DC011 Timing Chip Block Diagram

Input Decoder

The input decoder responds to commands on pins 20 and 21 (connected to DO 04 H and DO 05 H of the 8080 bus respectively) whenever the VIDEO WR 1 L pin is low. The outputs of the decoder select 80/132 column, 60/50 hertz refresh, and interlaced/noninterlaced modes of operation. Table 6-7 shows that when DO 05 H is low the number of columns is programmed according to the state of DO 04 H, and when DO 05 H is high the refresh rate is programmed. Interlaced mode is always selected when the column mode is set, and noninterlaced mode is selected when the refresh rate is set. The interlace mode that is in use depends on whether the number of columns or the refresh rate was selected last.

Table 6-7 Video Mode Selection (Write Address = C2H)

Inputs		Configuration	Function
D005 H Pin 21	D004 H Pin 20		
0	0	80-column mode	Sets interlaced mode
0	1	132-column mode	
1	0	60 hertz mode	Sets noninterlaced mode
1	1	50 hertz mode	

In addition to strobing data into the input decoder, VID WR 1 L acts as a reset signal for the DC011. Whenever VID WR 1 L is low, the counters in the DC011 are held in a cleared state. Resetting the counters serves no purpose in the VT100 because the remainder of the VT100 synchronizes itself to the DC011, but a reset is useful for testing both individual chips and complete modules. Writing into the DC011 is never done unless the mode is being changed because it would cause the counters to reset and disturb the display.

80/132 Column Selection

The column mode is changed by modifying the divisors of three of the counters in the DC011. The first of these counters divides the input clock (MASTER CLK) by 1.5 to produce the dot rate clock for 80-column mode. The DOT CLK output provides the signal that controls the shifting of dots out from the video shift register. A multiplexer determines what rate DOT CLK will have for the entire screen by selecting either the output of the divide-by-1.5 in 80-column mode or by selecting the 24 MHz MASTER CLK directly in 132-column mode. The other two counters affected by 80/132 selection are the dot counter and the horizontal counter.

Dot Counter

The dot counter uses four flip-flops to divide the DOT CLK that was selected by the multiplexer by 10 (in 80-column mode) or by 9 (in 132-column mode). The output of the dot counter is the character rate clock, which is used to move character codes in the latches that are outside the DC011. Character clock is further divided by the horizontal counter. CHAR CLK is unaffected by double-width mode. The output of the next-to-last flip-flop is used for the write enable signal for the line buffer RAMs (WRITE LB L). This signal allows the data and address changes, caused by the rising edge of CHAR CLK, to become stable before writing is enabled. It then disables writing before CHAR CLK rises again. WRITE LB L is gated directly with HOLD REQ H so that it is active only during DMAs. Intermediate signals from the four flip-flops are used by various other functions in the DC011 such as the double-width multiplexer and the composite sync generator.

Double-Width Multiplexer

The double-width multiplexer (MUX) produces the three signals whose timing must be changed when a line of characters is switched between single- and double-width modes. The frequency of DOT CLK must be divided in half on a double-width line so that the video shift register will shift half as often, making each dot (and therefore each character) twice as wide as it would be in single-width mode. In order for the video shift register to work properly with the half-rate DOT CLK in double-width mode, the load signal for the shift register (VSR LD H) must still come every 10 dots (80-column mode) or 9 dots (132-column mode). Therefore, loads must occur at every other CHAR CLK. Similarly, incrementing the DMA address counters occurs on every other CHAR CLK to ensure that characters that are stored sequentially in the screen RAM are presented to the shift register at the correct time for each VSR LD H pulse.

In single-width mode, the double-width MUX directs the output of the 80/132 MUX to the DOT CLK pin, providing either a 16 MHz or 24 MHz output. To get the half-rate DOT CLK for 80-column mode, the double-width MUX selects the output of the first flip-flop in the dot counter, which acts as a divide-by-2 because the dot counter is dividing by 10 and 10 is an even number. In 132-column mode the same selection cannot be made because the dot counter is dividing by 9. But the divide-by-1.5 is not needed in 132-column mode, so this divider is converted to a divide-by-2. The double-width MUX selects its output when a double-width line is displayed in 132-column mode.

The load input of the video shift register used in the VT100 is a synchronous input. This means that when the load input is high, the rising edge of DOT CLK causes a parallel load to be performed instead of a shift. To get one load and many shifts for each character, VSR LD H can only last for that one cycle of DOT CLK that is adjacent to CHAR CLK. Furthermore, transitions of VSR LD H must satisfy set-up and hold times with respect to the rising edge of DOT CLK. In single-width modes, VSR LD H is one dot time wide, generated from the outputs of the dot counter, and its set-up and hold times are guaranteed by internal propagation delays. In double-width mode, VSR LD H is created by selecting every other CHAR CLK and then delaying this signal by one single-width dot time.

The signal that increments the DMA address counter (ADDR CNT) has the same timing as CHAR CLK, but it does not run continuously. ADDR CNT can only be generated if HOLD REQUEST H is high. It is further controlled by a signal from the horizontal timing section (ADDR CNT ON H) that allows ADDR CNT to provide exactly three pulses, in single-width mode, before HORIZ BLANK H goes low. The three pulse delay primes the external character latches so that the dots for the first character on a line are being loaded into the video shift register at the same moment that HORIZ BLANK H enables the video at the beginning of a scan. The only change made to ADDR CNT for double-width operation is that every other pulse is deleted, beginning with the first pulse.

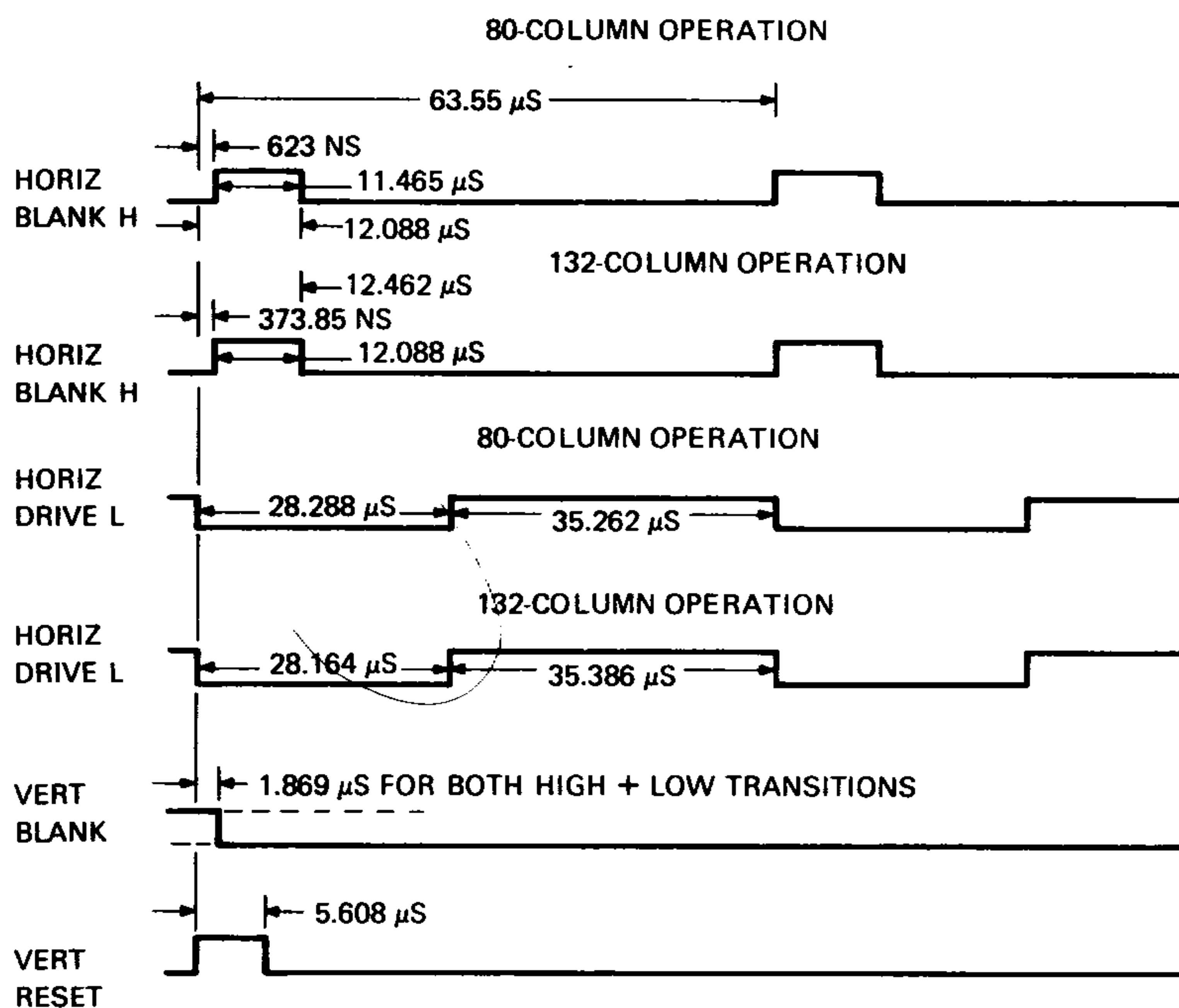
Horizontal Counter

The block diagram in Figure 6-13 shows the horizontal divider broken into three stages. The first divider is programmable according to the number of columns selected and is driven by CHAR CLK from the dot counter. For 80-column mode the divisor is 3; for 132-column mode the divisor is 5. The total division from MASTER CLK to the output of this first divider is 45, independent of column mode (for 80-column mode: $1.5 \times 10 \times 3 = 45$; for 132-column mode: $1 \times 9 \times 5 = 45$). Therefore, the operation of all of the remaining dividers in the DC011, which are driven from the first horizontal counter, is also independent of the column mode.

The second stage of the horizontal divider has a divisor of 17, which is chosen to give the required number of displayable columns plus about 28 percent more to allow time for the monitor to execute a horizontal retrace. The last stage is a simple divide-by-2 that provides the horizontal frequency. Therefore, at its input, the signal will have a frequency twice that of the horizontal frequency. This is required by the vertical dividers to create interlaced operation. The total division from CHAR CLK provided by the horizontal divider is 102 in 80-column mode and 170 in 132-column mode. In either mode the frequency at the output of the horizontal counter is 15.734 kHz.

Horizontal Drive and Horizontal Blank

Two timing signals are generated from the horizontal counter to control those system functions occurring at the scan rate. These signals begin at the end of a scan and last until the horizontal counter is incremented past a specific state that is decoded to turn the signals off. The monitor requires a pulse at the end of every scan to tell it when to initiate a retrace and begin the next scan; the duration of this pulse must be between approximately $\frac{1}{4}$ and $\frac{1}{2}$ of one scan. Figure 6-14 shows **HORIZ DRIVE L** as produced by the DC011. The slight difference in timing between 80- and 132-column modes is the result of design convenience and is not significant to the operation of the VT100.



NOTE: HORIZONTAL BLANK H IS SHORTER THAN ACTUAL HORIZONTAL BLANK TIME.

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Figure 6-14 Horizontal Timing

HORIZ BLANK H is designed to allow 83 characters during the forward scan in 80-column mode and 137 characters in 132-column mode. The extra characters are included for possible future use such as a field of indicators along the right margin of the screen or as extra symbols inserted to mark text.

The rising edge of **HORIZ BLANK H** is resynchronized to **CHAR CLK** to eliminate the accumulated delay of the horizontal counter. The falling edge of **HORIZ BLANK H** occurs between two **CHAR CLKs** to meet some requirements of the DC012, but inside the DC012 **HORIZ BLANK** is delayed to the falling edge of **CHAR CLK** so that the beginning of each displayed scan will coincide with a character boundary.

Line Buffer Addressing

The line buffer memory stores one line of characters during a scan on which a DMA occurs and then recalls these characters on each successive scan until the next DMA. Because the line buffer is a random-access memory, it has address inputs that must be provided with a sequence of addresses that change at each **CHAR CLK** such that each character is stored in a unique location. The horizontal counter can pro-

vide such addresses because it is incremented through a series of unique states that repeat in the same sequence on every scan. Because of the three stages that comprise the horizontal counter, there are nine flip-flops whose outputs must be converted into the eight line buffer address (LBAs) outputs. The conversion is possible because the 9 flip-flops represent a maximum of 170 states in 132-column mode (8 bits can represent 256 states). The DC011 contains gates that combine the output of the ninth flip-flop in the horizontal counter with the outputs of the other eight to generate some addresses that are not otherwise represented by the eight. The resulting LBAs do not follow a normal binary counting sequence; the sequence of unique addresses repeats exactly on each scan.

Several of the LBAs are used as general purpose clocks in the VT180. LBA 3 and LBA 4 are used to generate timing for the keyboard. These signals satisfy the keyboard's requirement of two squarewaves, one twice the frequency of the other, even though every sixteenth transition is delayed (the second stage of the horizontal counter divides by 17, not 16). LBA 7 is used by the nonvolatile RAM.

Vertical Operation

To paint a complete picture on the screen, the monitor moves the electron beam slowly from the top of the screen to the bottom while it is also moving the beam quickly from left to right to paint each scan. The vertical sweeps of the beam must be repeated continuously so that the picture is refreshed often enough to prevent flicker. In television terminology, a single pass of the beam from the top of the screen to the bottom (and the data displayed during that time) is referred to as one field. A complete picture, which may contain one or more fields depending on the type of interlacing in use, is called one frame. When the VT180 is used in noninterlaced mode, each successive field is identical and therefore only one field is contained in each frame. During interlaced operation in the VT180, there are two types of fields that alternate with each other so that each frame consists of two fields. Even fields start at the top of the screen and display 240 scan lines before reaching the bottom. Odd fields place their first scan line between the first and second scans of the preceding even field and then place each additional scan between succeeding scans of the even field. Interlacing the even and odd fields gives a whole frame of 480 scans instead of 240 scans. This provides increased vertical resolution.

In noninterlaced operation, commands to the monitor to begin a new field are always coincident with commands to begin a new scan. This causes the beam to always be in the same vertical position when the first displayed scan is begun. In interlaced mode, odd fields begin with a command for a new frame that occurs halfway through a scan line. This causes the beam to have moved down the screen from where it would have been during an even field (by the distance that it moves in one-half of a scan) when the first displayed scan is begun. Even and odd fields are made to alternate by including an odd number of half-scans in every field. This is in contrast to noninterlaced operation, where each field contains only complete scans. The monitor always displays the same video information on both even and odd fields. Interlaced mode is provided for future use by options that desire increased vertical resolution.

Vertical Counter

The 10-bit vertical counter, shown in Figure 6-13, determines the frequency at which the screen is refreshed by counting the number of horizontal scans included in each field. The vertical counter uses the 31.468 kHz output of the horizontal counter so that it can count the half-scans required for interlaced operation. Figure 6-13 lists the four available divisors that select the interlace mode and keep the refresh frequency as close to the local power line frequency as possible (to minimize interference with the screen from nearby equipment). The vertical frequencies produced by these divisors are approximately 1/20 Hz above or below the nominal power line frequency.

Vertical Outputs

Three outputs are derived from the flip-flops in the vertical counter to control the vertical refresh operations in the VT180. These signals are shown for all four modes in Figures 6-15 and 6-16.

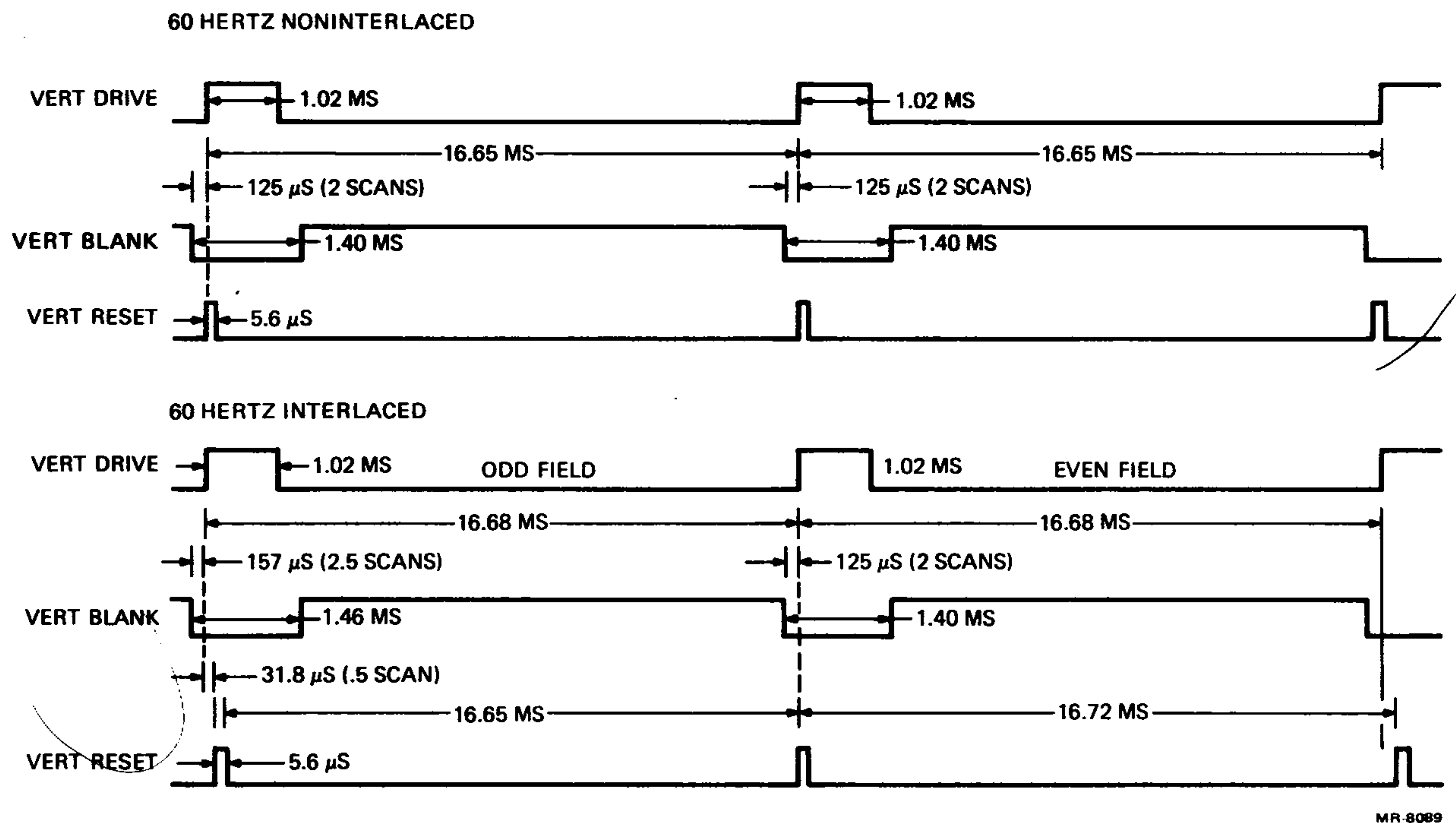


Figure 6-15 Vertical Signals - 60 Hz

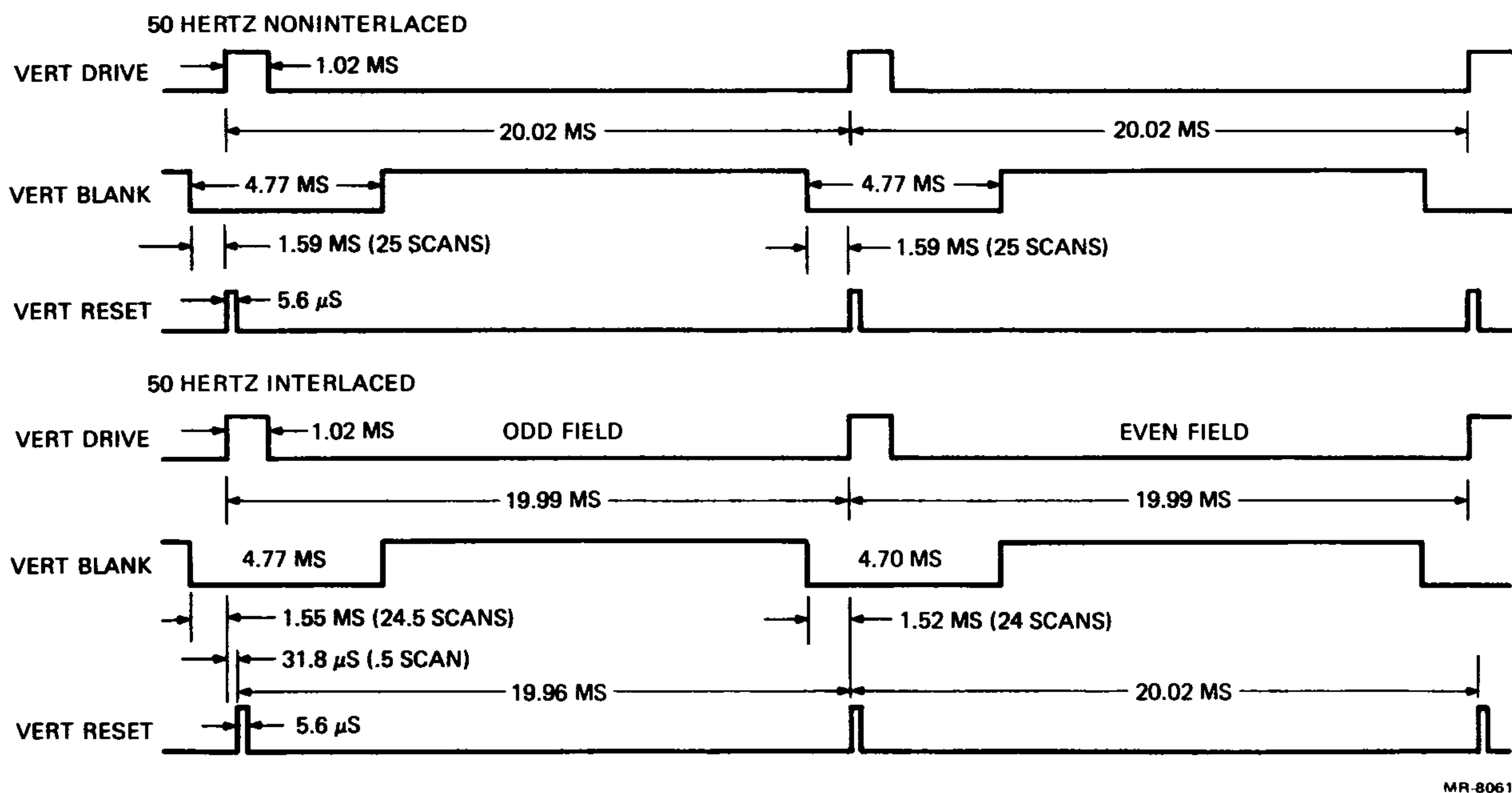


Figure 6-16 Vertical Signals - 50 Hz

VERT DRIVE H is issued at the bottom of the screen to initiate a vertical retrace followed by a new vertical scan. This operation is analogous to the effect of HORIZ DRIVE L on horizontal scans. The time between any two VERT DRIVE Hs is a constant, equal to an even number of half-scans in noninterlaced mode and equal to an odd number of half-scans in interlaced mode.

VERT BLANK L always enables exactly 240 scans during any field and blanks any remaining scans. Furthermore, VERT BLANK L is always turned off exactly 20 scans after VERT RESET H in 60 Hz mode and 50 scans after VERT RESET H in 50 Hz mode. VERT BLANK L is always adjusted to display complete scans even during odd fields in interlaced mode.

VERT RESET H initiates the DMA process at the start of every field. When VERT RESET H goes high, the DMA address counters are reset to point to address 2000H in the screen RAM, all line attributes are cleared, and the scroll counter in the DC012 is preset to the value stored in the scroll latch. (See the DC012 description for more explanation.) During noninterlaced operation and on even fields, VERT RESET H occurs at the same time as VERT DRIVE H; but, on odd fields VERT RESET H is delayed one-half of a scan to match the start of a horizontal scan. The relationship of VERT RESET H and transitions of VERT BLANK L to HORIZ BLANK H and HORIZ DRIVE L is depicted in Figure 6-14. Notice that VERT BLANK L always turns on or off when the video is already blanked by HORIZ BLANK H.

Composite Sync

The COMP SYNC L signal supplied by the DC011 is combined with video information by the terminal controller board to produce the composite video signal that appears on J9 at the back of the VT180. An external monitor can use the composite video signal to reproduce the image displayed on the monitor screen. This is accomplished by using the video information to control beam intensity and the composite sync waveform to synchronize the raster to the video information.

The composite sync generator in the DC011 uses outputs from the dot, horizontal, and vertical counters to generate the complex timing of COMP SYNC L. COMP SYNC L consists of one of the vertical intervals depicted in Figure 3-29 followed by 240 horizontal sync pulses, another vertical interval. The vertical synchronizing interval consists of a transition from horizontal sync pulses to six equalizing pulses, six vertical sync pulses, six more equalizing pulses, and then a return to horizontal sync pulses. Two vertical intervals are shown in Figure 3-29. The vertical interval that begins an odd field is similar to that which begins an even field except that the equalization and vertical sync pulses are shifted by one-half scan with respect to the horizontal sync pulses. In noninterlaced mode, all fields are even fields; but, in interlaced mode, every other field is an odd field. Figure 3-29 also shows the relationship of COMP SYNC L to both HORIZ BLANK H and VERT BLANK L. COMP SYNC L meets the requirements of EIA RS-170 and the NTSC standards for sync pulse generators.

Hold Request, Address Load, and Double-Width

The logic associated with HOLD REQ H, ADDR LD L, and DW H is shown in Figure 6-13. The falling edge of HOLD REQ H sets ADDR LD L to the low state; ADDR LD L is subsequently cleared by the falling edge of CHAR CLK, thus creating a short low pulse on ADDR LD L at the end of each DMA. ADDR LD L stores, in their respective registers, all line attributes and the memory address of the next line to be accessed by a DMA. The rising edge of HOLD REQ H causes the value of DW H that was stored in the holding flip-flop by the previous ADDR LD L to be transferred to a second flip-flop whose output controls the double-width MUX. This means that the value of DW H stored at the end of one DMA by ADDR LD L does not actually become effective until the beginning of the next DMA. The holding flip-flop for DW H is cleared by VERT RESET H at the start of every field. HOLD REQ H is also used to enable ADDR CNT and WRITE LB L only during DMAs. Interactions of HOLD REQ H with other signals during a DMA are further defined in Figure 6-19.

6.5.12.2 Control Chip Description – The control chip (DC012), like the timing chip, is a custom bipolar device. It accepts attribute specifications and timing signals and delivers addresses for the character generator ROM and attributes for the video output to the monitor. It also generates the hold request signal that halts the microprocessor and initiates DMAs to get lines of characters. Refer to the block diagram, in Figure 6-17.

The DC012 performs three main functions.

1. **Scan count generation.** This involves two counters, a multiplexer to switch between the counters, double-height logic, scroll and line attribute latches, and various logic controlling switching between the two counters. This is the biggest part of the chip. It includes all scrolling, double-height logic, and feeds into the underline and hold request circuits.
2. **Generation of hold request.** This uses information from the scan counters and the scrolling logic to decide when to generate hold request.
3. **Video modifications:** dot stretching, blanking, addition of attributes to video outputs, and multiple intensity levels.

Input Decoder Functions

The input decoder accepts a 4-bit command from the microprocessor when VID WR 2 L is asserted. Table 6-8 lists the commands.

The low eight values are used to load the scroll latch with the offset for smooth scroll. The scroll latch is loaded in two passes, first writing the two least significant bits and then the two most significant bits. Because the offset is a decimal value controlling ten display scans, the combination setting the most significant bits to 11B is not used in the VT180 (11B covers the range 12–16).

The input decoder also toggles the blink flip-flop by complementing the state of the flip-flop whenever 1000B is written. The blink flip-flop invokes blink only where the blink attribute is set.

To save external hardware, the vertical frequency interrupt flip-flop is located in the DC012 because a spare pin was available. It is set by the falling edge of vertical reset. It is cleared by writing 1001B into the input decoder.

Set and clear of reverse field are not toggled because the absolute state is important and there is no feedback for the system to detect the current state. Therefore, the two states are explicitly set to their desired values.

1100B means you set the base attribute to underline and 1101B means you set the base attribute to reverse video. 1110B and 1111B are for future specification.

Any time the input decoder is loaded with 11XXB, the blink flip-flop gets cleared. This is the only way to initialize blink in the chip testing process. The firmware does not currently use the ability to clear the blink flip-flop but if hard copy output was being implemented, it could be used to set the blink to a known state during a freeze.

Figure 6-17 DC012 Control Chip Block Diagram

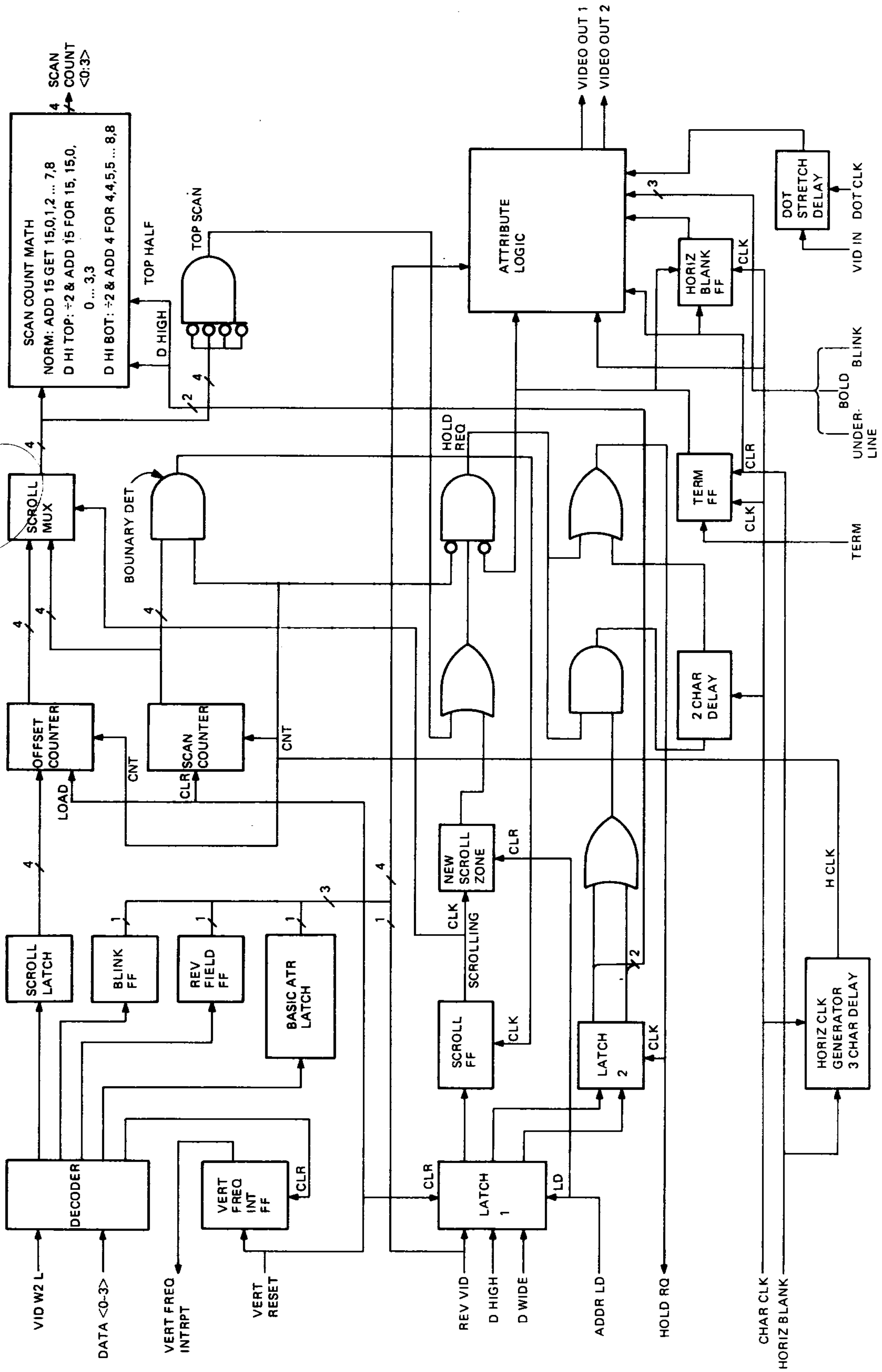


Table 6-8 Control Chip Commands (Write Address = A2H)

D3	D2	D1	D0	Function
0	0	0	0	Load low order scroll latch = 00
0	0	0	1	Load low order scroll latch = 01
0	0	1	0	Load low order scroll latch = 10
0	0	1	1	Load low order scroll latch = 11
0	1	0	0	Load high order scroll latch = 00
0	1	0	1	Load high order scroll latch = 01
0	1	1	0	Load high order scroll latch = 10
0	1	1	1	Load high order scroll latch = 11 (not used)
1	0	0	0	Toggle blink flip-flop
1	0	0	1	Clear vertical frequency interrupt
1	0	1	0	Set reverse field on
1	0	1	1	Set reverse field off
1	1	0	0	*Set basic attribute to underline
1	1	0	1	*Set basic attribute to reverse video
1	1	1	0	*Reserved for future specification
1	1	1	1	*Reserved for future specification

*These functions also clear blink flip-flop.

Attribute Latches

The line attributes are managed by two latches that store the scrolling, double-height (DH), and double-width (DW) bits. The first latch stores the incoming data when address load (ADDR LD) goes low at the end of a DMA. Scrolling means that the next line will be part of the scrolling region; DH means the next line will be double height; and DW specifies top or bottom half for double-height lines. There is no double-height, single-width combination, so in double-height, double-width is assumed. The DW pin also tells the DC012 to extend hold request during double-width. The second set of latches for double-width and double-height are clocked by the rising edge of hold request (similar to the second latch for double-width in the DC011) to invoke the attributes at the beginning of the new line. The first latch stores those attributes from the end of one DMA to the beginning of the next. It is the outputs of the second latch that invoke attributes in the chip. The scroll bit is invoked by a different signal that will be discussed later. The pin defining scrolling is the same pin as reverse video; it means scrolling when loaded in by ADDR LD L and it means reverse video at all other times. The reverse video signal passes from the input pin around the first latch directly to the attribute logic.

Scroll Counter

The scroll counter consists of two 4-bit, divide-by-10 counters called the scan counter and the offset counter. Both are clocked at the horizontal rate to count scans. The scan counter is cleared by vertical reset so that it starts at zero and counts by tens down to the end of the screen.

The offset counter is loaded with the contents of the scroll latch by vertical reset. The scroll latch is loaded by the microprocessor and defines the offset between the scan and offset counters for an entire frame because the offset counter is only loaded at vertical reset time. The microprocessor will load the latch with the offset for the next frame during the current frame.

At the beginning of a frame, the two counters divide by ten but start at different numbers. If not currently scrolling, the offset is zero and there is no functional difference between the counters. If in the middle of a smooth scroll, the offset will be some other value from one to nine. The scan address outputs from the chip to the character generator ROM are either the output of the offset counter or of the scan counter, depending on whether the current line is in or out of the scrolling region, respectively. One of the two counters is selected by a 4-bit wide multiplexer (MUX) whose output is the counter in use. The MUX is controlled by the scroll flip-flop, which is the second latch for the scroll attribute bit. Most line attributes (double-height, double-width) take effect when hold request goes high for the line in which they are effective. They always take effect with the actual data being displayed. However, the scroll flip-flop can only change state when crossing one of the fixed ten scan boundaries that are defined when the scan counter reaching zero.

When the scan counter reaches zero a change can occur from a nonscrolling to a scrolling region or from a scrolling to a nonscrolling region since this is normally where one line of data changes to the next if the line were not scrolling. To get into or out of a scrolling region, the scan counter must be at zero. A 4-bit boundary detect decoder gate is connected to the outputs of the scan counter and clocks the scroll flip-flop when all its inputs are zero. If the input to the scroll flip-flop (from the scrolling attribute latch) has been low and goes high at the end of the previous line's DMA, on zero (boundary detect) the output of the scroll flip-flop, which is the control line of the MUX, causes the MUX to switch from the scan to the offset counter. At the bottom of the scrolling region, the last DMA in the region gets a line from the screen RAM with its scroll attribute not set. When the next zero boundary is reached, as defined by the scan counter, the scroll zone is exited. This happens because the scroll flip-flop will get a zero input again, which will switch the MUX back to the scan counter right in the middle of the line that was part way through scrolling.

Scan Count Math

The scan count output of the scroll MUX goes through combinatorial logic that looks at the double-height bit and the top and bottom half bit and decides whether those scan counts need to be modified for double-height before going out of the chip. If double-height is not asserted, the top and bottom half bit is ignored and the scan is passed through with 1 subtracted in modulo 16 arithmetic. (Thus, 0 becomes 15, 3 becomes 2, 9 becomes 8.) If double-height is asserted and top half is asserted, then the operation is to divide the scan count by 2, and continue to subtract 1 after dividing by 2 so the first scan equals 15, the second scan equals 15, and the third scan equals 0. If bottom half is asserted, the operation is to divide by 2 and add 4. This particular arithmetic arrangement was designed for an external component that is no longer needed. Otherwise, dividing by 2 (and adding 5 for the bottom half) would be sufficient. The scan count changes on the rising edge of **HORIZ BLANK H**.

Generation of Hold Request

Hold request is the signal to the microprocessor that makes it give up control of the data bus. Then the video processor can DMA a line of data out of the screen RAM and place the data in the line buffer. Two principle conditions can generate hold request. The most common is when the output of the counter in use equals zero, meaning on the first scan of a new line of characters. (The counter in use, which is the output of the scroll MUX, is either the output of the offset or scan counter, depending on whether the current line is in or out of a scrolling region.) When a new line of characters starts, a hold request is needed to get the line's data; and therefore, a detector at the output of the scroll MUX detects scan zero of the counter in use.

The other condition for generating hold request is at the top of a new scrolling region. This is necessary because as the CRT beam moves from a nonscrolling region into a scrolling region, it switches from the last scan of a normally registered line to the first displayed scan of a line that is scrolling. Assuming the scrolling region is in midscroll, the first scan is not the zero scan of the scrolling line, so the counter in use is not zero. The new scroll zone flip-flop (whose clock input comes from the scroll flip-flop that controls the scroll MUX) is triggered by entrance into a scrolling region. When the new scroll zone flip-flop is set, it forces a hold request even if the counter in use is not also zero. If the counter in use is zero (implying an offset of zero between scrolling and nonscrolling lines) there are two simultaneous causes for hold request.

The new scroll zone flip-flop is cleared by ADDR LD that occurs at the end of the hold request generated by the new scroll zone flip-flop. That is, the new scroll zone flip-flop generates hold request. Hold request is cleared either by terminate or horizontal blank, whichever comes first (the VT100 is programmed so that terminate is always first). Termination of that hold request feeds back through ADDR LD and clears the new scroll zone flip-flop. More about hold request follows a discussion of horizontal blank and terminate.

Horizontal Blank and Terminate

Horizontal blank, in addition to blanking the video output, clears the terminate flip-flop and generates an internal timing signal (horizontal time reference) for clocking counters.

A short signal that occurs on every horizontal scan and lasts only a few character times is needed in the chip to clock flip-flops and to disable the decoder gates that detect boundaries and generate hold requests while the counters settle. Horizontal blank cannot be used for this purpose because hold request and boundary detect (and other signals) need to be settled well before horizontal blank ends. The required short signal comes from a small counter triggered by horizontal blank and further clocked by character clock. The counter has two outputs: a two character clock wide signal that enables and disables the boundary detect flip-flop (that drives the scroll flip-flop) and a three character clock wide signal (H CLK) that enables the hold request gate. Boundary detect is enabled earlier than the hold request gate so that the existence of scrolling can set up the new scroll zone flip-flop before hold request is enabled. A gate combines the output of the new scroll zone flip-flop and the output of the boundary detector (counter in use equals zero). The output of that gate is combined with H CLK (three character clocks long following horizontal blank) to generate the rising edge of hold request three character times after the rising edge of horizontal blank. It is also combined with the signal from the terminate flip-flop to end hold request when a terminator is detected.

If terminate did not cut off hold request, then hold request would be disabled by the next falling edge of the H CLK signal, but the VT180 is programmed to always end hold request with terminate. If the VT180 was not working correctly, hold request might be ended by horizontal blank.

Terminate causes a number of functions inside the DC012. The terminate input is not direct; it is sampled on each rising edge of character clock and latched into a flip-flop. When detected, it ends any hold request in progress. In normal screen mode, it blanks the video output, but in reverse screen mode it forces the video output to the dim intensity level. The terminate flip-flop output feeds back to its own input so that, as soon as the flip-flop is clocked with terminate asserted, the flip-flop latches itself up.

Once the terminate flip-flop is latched up by feedback from its output, there is only one way to clear it: through the asynchronous clear input. The flip-flop must not be cleared until horizontal blank has taken over blanking the video output; therefore, the clear is delayed slightly (by one character time after the onset of horizontal blank). The clear is maintained until just before the character clock, which corresponds to the first character on the screen, because data on the video data bus may be undefined and might contain extraneous terminators. These must not be detected during the horizontal blanking interval because they would latch up the terminate flip-flop for an entire scan. However, the internal signal that blanks the video outputs of the DC012 during the horizontal blanking interval cannot be used to clear the flip-flop directly because it must release the video output at the exact beginning of the first character on the screen, and the terminate flip-flop must be capable of detecting the terminator in the first character position. If the internal blanking signal was used to clear the terminate flip-flop, the release time of the flip-flop would not be satisfied; and it might miss a terminate in the first character position (as would be found in set-up and the top and bottom fill lines). Therefore, the horizontal blank output of the DC011 is made to end approximately one-half character time before video unblanking to release the clear on the terminate flip-flop. Inside the DC012, the falling edge of horizontal blank H is delayed to the following character clock to provide the correct video blanking.

Double-Width and Hold Request

The first occurrence of terminate or horizontal blank at the end of a DMA normally gates hold request off. But in double-width mode, hold request is extended by two character times. This is required because each character appears twice in the external character latch pipeline. To get the first and second byte of the next line's address correctly placed with respect to address load, the end of hold request must be delayed by two character times after terminate or horizontal blank. This delay occurs either when double-width is asserted alone or at any time double-height is asserted (because double-height implies double-width). Combine hold request with a two character time delayed version of hold request to give a hold request that starts at the normal time but ends two character times later.

Attributes

The attribute section of the DC012 decides how to interpret various combinations of attribute inputs. A number of different inputs determine attributes applied to each character. There are the four attribute pins: reverse video H, underline L, bold L, blink L. There are also internal signals, mostly from the input decoding section, that affect attributes. These are the blink flip-flop (toggled by the input decoder to provide blink timing), the reverse/normal field flip-flop (set by input decoder), the base attribute flip-flop (set by the input decoder to select whether the reverse video pin is interpreted as reverse or underline), and the scan counts (from the output of the double-height section, that enable the underline on the correct scan). These inputs are applied to a combination of gates that feed into a 4-bit latch before controlling the video outputs. This latch is clocked by character clock to change the attributes during the intercharacter space.

Normal characters appear uninverted at normal intensity by asserting VID OUT 2 whenever VID IN H is asserted. Bold characters are the same as normal characters except that VID OUT 1 and 2 are enabled. Reverse characters (exclusive-OR of reverse video and reverse screen) normally have dim backgrounds with black characters so that the large white spaces have the same impact on the viewer's eye as the smaller brighter white areas of normal characters. Bold and reverse asserted together give a background of normal intensity. Blink applied to nonreverse characters causes them to alternate between their usual intensity and the next lower intensity. (Normal characters vary between normal and dim intensity. Bold characters vary between bright and normal intensity.) Blink applied to a reverse character causes that character to alternate between normal and reverse video representations of that character. Underline causes the ninth scan of a character to be forced to white of the same intensity as the character for nonreversed characters, and to black for reverse characters.

Dot Stretcher

The dot stretcher reduces the video bandwidth required in the monitor (especially in 132 mode) by making the minimum dot width 80 nanoseconds. Wider dots give the CRT time to reach full intensity before turning off again. This makes vertical lines appear to have the same intensity as horizontal lines, rather than looking dimmer because of the brightness loss. The dot stretcher works by delaying the VIDEO IN H signal by one dot time (using a flip-flop clocked by dot clock) and then ORing the undelayed and delayed signals.

6.5.12.3 Address Counter and Data Structure in RAM – Refer to the print set and to Figure 6-5. The address counter (E21, E22, E25, E30) consists of three 4-bit binary counters that can be preset. They are cascaded to form 12 bits with an additional flip-flop that provides a thirteenth bit of address to the screen RAM. Vertical reset clears the counter to an initial hardwired value of 2000H so that the video processor always begins to process from that location after a vertical reset. The counter is loaded with a new address at the end of each DMA when the address load signal appears. The counter counts forward from this address at the character clock rate, using the address count (ADDR CNT H) signal. ADDR CNT H only occurs during hold request; thus, the counter only counts during the DMA portion of each line. The address is loaded at the end of the DMA scan and held until the next DMA begins. The thirteenth bit is programmed by D4 in the high byte of a DMA address. The VT100 firmware programs this bit high to access address 2000H plus the contents of the 12-bit counter. But if D4 were programmed low, DMAs would access address 4000H plus the contents of the 12-bit counter.

In double-width mode, the address count pulses occur half as often as in normal width. The line buffer receives the normal number of WRITE LB pulses, however, so each character gets copied into two adjacent locations in the line buffer.

6.5.12.4 Address Latch Buffer – Tristatable latches (E26, E33) store the address counter outputs for a character period to increase the speed of RAM accesses. This would otherwise be slowed by the long propagation delay of the address counters. The buffers provide sufficient output power to drive the address bus of the basic terminal controller board and the AVO, if present. The outputs are disabled during the non-DMA period to prevent conflict with the microprocessor address bus.

6.5.12.5 Line Buffer – Data arrives at the screen RAM latch (E20) during a DMA cycle and is latched in by the character clock. During the DMA, the tristate buffer (E15) is enabled. Data passes through it to the line buffer (E11, E17) for storage and to the character generator latch input (E16). The line buffer is a 256 by 8 RAM that can hold one full line of data including the three end bytes. The line buffer is written when WRITE LB L is asserted in the middle of each character clock period. Its outputs are disabled during the DMA by the hold request signal. During non-DMA operation, the screen RAM latch samples the 8080 data bus at the character rate; but the tristate buffer is off so the 8080 data has no effect. However, the outputs of the line buffer are enabled and the same data is presented to the character generator latch as was presented during the previous DMA scan.

6.5.12.6 Character Generator – The character generator is a ROM that is addressed by the coded representations of the desired characters stored in the screen RAM. Each code is used as the high 7 bits of the address to a 2K by 8 ROM. (That provides enough storage for 128 characters). The eighth character bit is the base attribute input to the DC012. The low four address bits are provided by the scan counter in the DC012. The seven character bits combine with the 4-bit scan count from the DC012 to give an 11-bit address to the ROM. The data stored at each (scan + character) address is eight bits representing the presence or absence of dots of light at sequential horizontal positions within that scan. Figure 6-18 shows the patterns supplied in the standard character generator ROM.

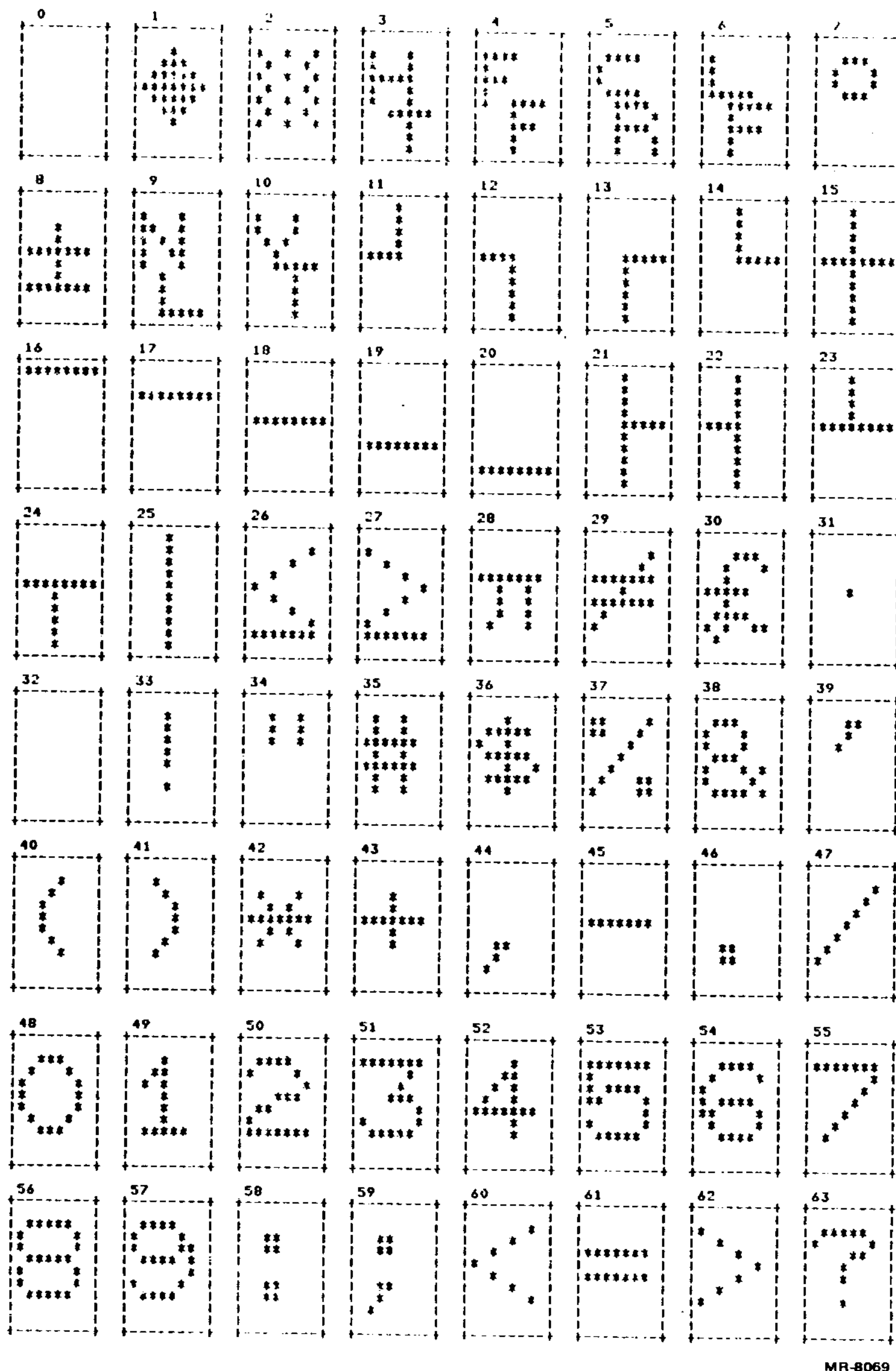
If the alternate character generator ROM and the advanced video option are present, the AVO may assert ALT CHAR SET L to disable ROM E4 and enable ROM E9 when the alternate character set attribute is set. If the AVO is installed without the alternate character ROM, any character cell in which the alternate set is selected will appear white (or black if in reverse video).

If the AVO is installed without the alternate character ROM, any character cell in which the alternate set is selected will appear white (or black if in reverse video).

If it is necessary to use a different main character set than the one provided in the VT180 but an alternate character set is not required, the following arrangement may be used.

1. Cut jumper W1 to disable the main ROM.
2. Plug a new main ROM into the alternate character ROM socket.
3. The new main ROM must be programmed exactly as the alternate ROM except that the chip select on pin 18 must be programmed for high assertion.

To use a UV erasable PROM in the socket for E9 (which must have Intel 2716 pinouts), cut jumper W4 and insert jumper W5 to put +5 volts on pin 21. The access time of the ROM must be less than 300 ns to guarantee operation in 132-column mode.



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Figure 6-18 Character Generator ROM Patterns (Sheet 1 of 2)

6.5.12.7 Video Shift Register – When VSR LD H is asserted, seven of the eight output bits from the character generator ROM are latched into the shift register. The eighth is latched into a flip-flop. At the same time, the last bit shifted out by the video shift register (VSR) during the previous character time is latched into the first bit position in the VSR. The VSR is continuously clocked by the dot clock. The first bit shifted out in the new character time has the same value as the last bit of the previous character. This provides horizontal continuity of characters from one character cell to the next. The seven new bits are then shifted out.

Meanwhile, the flip-flop that stored the eighth bit has delivered that bit to the serial input of the shift register. This bit was shifted into each successive register position as the first eight bits were shifted out. Now the shifting continues, for one more bit in 132 mode and for two more bits in 80 mode, causing the last bits shifted out to be the value that was stored in the flip-flop.

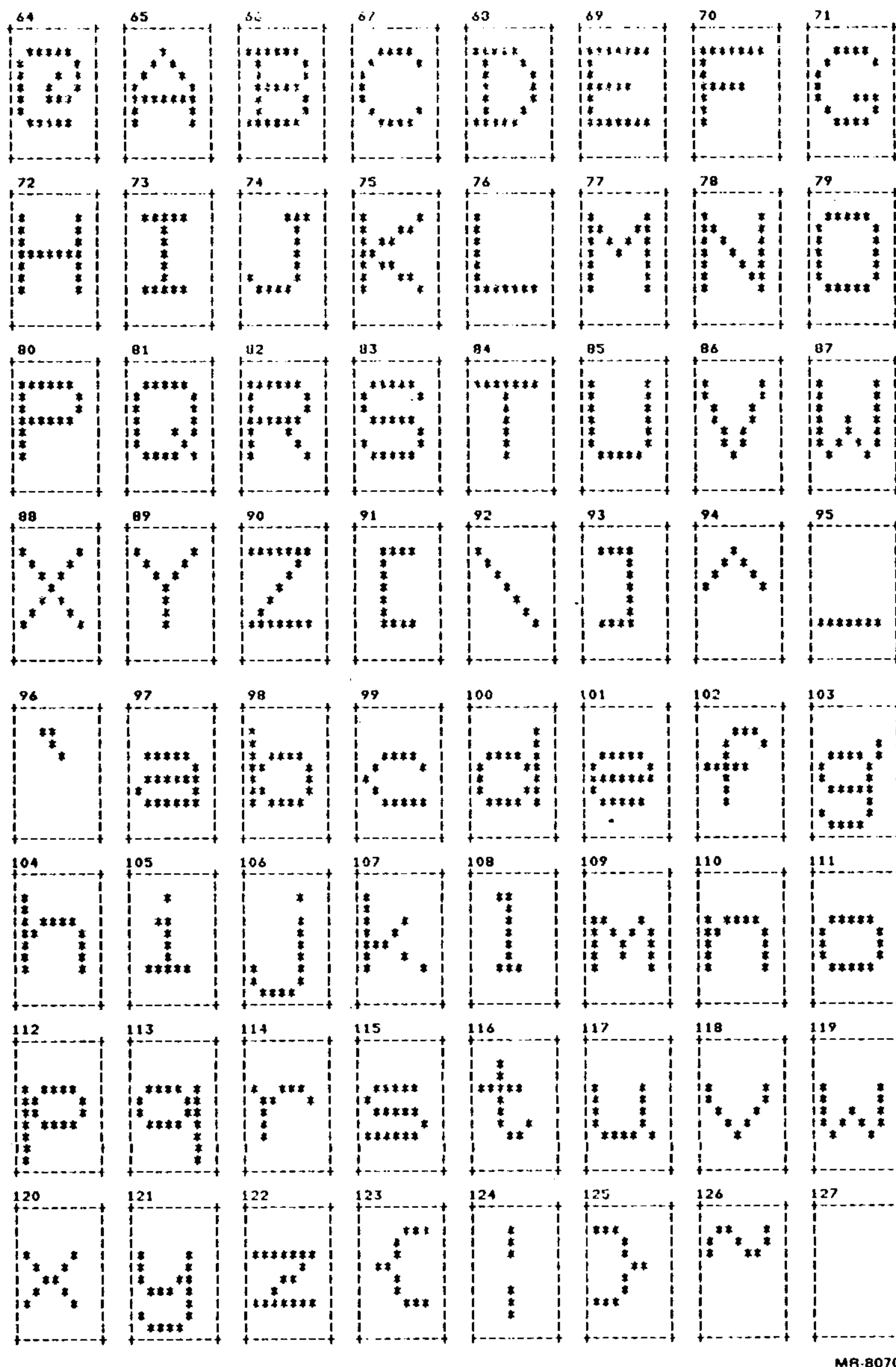


Figure 6-18 Character Generator ROM Patterns (Sheet 2 of 2)

VSR LD H then latches the next character into the VSR and flip-flop, with the last multiply-shifted bit in the first position. In this way, one bit from the character ROM defines the two or three dots between characters, while seven bits define the character itself.

At the end of the scan, horizontal blanking forces the flip-flop output low. Since blanking lasts more than one character time, the low level will be shifted to the first position before the start of the next line. This ensures that the first dot on the next scan will be at the screen background level.

6.5.12.8 Terminator – The seven bits of each character address in a line go to an eight-input terminator detector gate as they are passed to the character generator ROM. Only seven bits are examined because the eighth bit is an attribute and does not contribute to the uniqueness of a character. The last bytes in each line are a terminator character and two address bytes. Only the terminator character activates the gate. During the character time when the terminator reaches the detector gate, the first address byte is at the input to

the character generator latch and the second address byte is at the input to the screen RAM latch. On the next character clock, the terminator causes the DC012 to blank the display and end the hold request. The latch outputs now contain the two address bytes. The low order byte is at the inputs to counters E30 and E25, while the low four bits of the high byte are at E21. The fifth bit is at the input to flip-flop E22. This bit is normally high; it allows future development of screen RAM size. The high three bits go to the line attribute inputs to the DC012.

The address load (ADDR LD L) pulse, timed to arrive before the next character clock after the terminator, loads the address counters, flip-flop, and DC012 inputs with the two final bytes. The counters and flip-flop designate the address of the first character of the next line to be displayed.

6.5.12.9 DMA Cycle Timing Diagram – Figure 6-19 shows the complex timing in the video processor during the first scan of each new line of characters. The entire scan is shown, with the repeating portion compressed into the area represented by dashed lines. The diagram is for 80 columns, single-width display, as the VT180 is currently programmed. Diagrams in the DC011 timing chip description (Paragraph 6.5.12.1) show the differences in signals in other modes.

The first line shows the character clock. This continuous signal is the time reference for all DMA events.

The terminator occurs at the end of the previous scan. TERM L goes low for one character clock and then goes to an unspecified state that depends on the random characters that appear at the terminator detector gate. Character clock continues to shift data through the character latches, but invalid data is present in the character latches and is stored in the line buffer until just after DMA ENA is asserted. The terminator forces the video output to black or white (depending on normal or reverse screen), effectively blanking the end of the line (Paragraph 6.5.12.10). It also ends any DMA process in progress. The terminator's blanking effect is taken over by horizontal blank, and the terminate flip-flop in the DC012 is held cleared until just before the first character in the next scan. This prevents undefined data from triggering the flip-flop and blanking the whole scan.

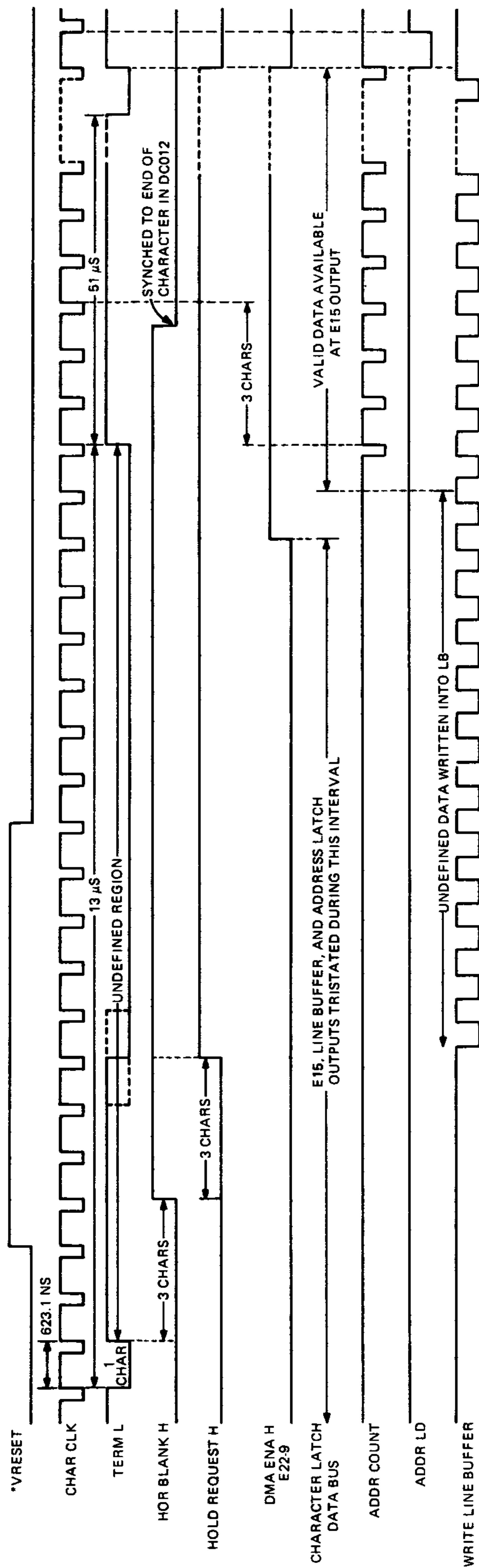
Horizontal blank occurs 3 characters after terminate in 80-column mode and 5 characters after terminate in 132-column mode. It forces all video to black (regardless of normal or reverse screen) for the horizontal retrace interval. The horizontal blank signal, as an output from the DC011, ends one-half character before the video actually needs to unblank. This early transition releases the clear for the terminate flip-flop in the DC012. The blank signal is resynchronized to character clock in the DC012.

Hold request silences the microprocessor so that the video processor can DMA data out of the screen RAM. It is initiated when the scan counter in use is equal to 0, or at the setting of the new scroll zone flip-flop. The terminate flip-flop must be cleared for hold request to occur. The start of hold request is delayed by three character times from horizontal blank to allow the counter in use to settle before the 0-boundary is detected. Hold request is ended by the detection of terminate at the end of a DMA scan.

DMA enable is generated from hold request and the microprocessor's hold acknowledge (HLDA) by discrete logic on the board (E22). It is enabled by the first rising edge of LBA4 if HLDA from the 8080 microprocessor is available. This ensures that the 8080 has given up the bus before DMA ENA H enables the DMA address counters onto the bus and drives MEM R low. DMA ENA H is cleared by the end of HOLD REQ H. While the use of LBA4 ensures that enough time has elapsed from the start of HOLD REQ H to guarantee that the 8080 is in its hold state, the use of HLDA H on the D input of the DMA enable flip-flop is required to prevent HOLD REQ from preventing a power-up cycle in the 8080.

The character latch data bus is shown to be tristated from the start of hold request until the start of DMA enable. Then it starts moving data through the video circuits.

Address count begins three character times before the end of horizontal blank (Paragraph 6.5.12.1).



*VERTICAL RESET DURING
1ST DMA OF FIELD ONLY

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Figure 6-19 DMA Cycle Timing Diagram

Address load is triggered by the falling edge of HOLD REQ H. It stores the line attributes for the next line and loads the address counters with the pointer address bytes at the end of the DMA line of characters. This address is the location of the first character of the next line to be DMAed.

Write line buffer L is described in Paragraph 6.5.12.1.

6.5.12.10 Video Blanking – The display is blanked by horizontal blank during the horizontal retrace interval, and by vertical blank during the vertical retrace interval. These hardware signals ensure that the CRT beam is turned off while it moves backward through the active screen area. Horizontal blank controls the video signal inside the DC012. Vertical blank controls the video signal at the video output circuit.

The horizontal blanking signal is timed to provide 83 columns of unblanking in 80-column mode, and 137 columns of unblanking in 132-column mode. The VT180 is currently programmed so that the three or five extra columns are blanked by terminate. In normal screen mode, this termination forces the beam to black, but in reverse screen, termination forces the beam to the screen background intensity. This means that in reverse screen mode, the last character that can fit on the screen is three or five characters in from the right edge of the illuminated screen. Because hardware blanking allows 83 or 137 columns on the screen, future program developments may allow the microprocessor to format the screen RAM for this ability. The main adjustment is to the position of the terminator and address bytes relative to the starting location of the line. Terminate, as the first character in the line, creates short lines during the vertical blanking interval to conserve memory while maintaining synchronization of the line address system.

6.5.12.11 Video Input and Output – The following paragraphs briefly describe the operation of the terminal controller video input and output circuits.

Direct Drive Video

The two video outputs from the DC012, video out 1 and video out 2, are combined with the vertical blank signal in two open collector nand gates of the direct drive generator. The outputs of the open collector gates are wire-ANDed with graphic 1 and 2 IN from any option board that may be present. The combined video and graphic signal is used to control the conduction of a transistor (Q4) to produce four different voltage levels, which are sent via the PC board fingers to the video monitor to vary the intensity of the screen display. The four voltage levels represent the four levels of intensity visible on the screen: black, dim, normal, and bright.

Composite Video Out

The combined video and graphic signal, along with the composite sync signal from the DC011, is used to control conduction of a transistor (Q2) in the same manner as described for direct drive video.

The result is a 75 ohm output (J9) from the terminal controller module consisting of four intensity levels (including black) and composite sync. This signal can directly drive a standard video monitor, or sync can be extracted to synchronize an external device for input to the terminal. The output is dc coupled. Although the use of dc coupling is not in strict agreement with EIA specification RS-170, this presents no problem with most monitors because they are usually ac coupled.

Video In

The video input stage terminates a standard video signal in 75 ohms. The video input is amplified by a linear biased transistor (Q5) and sent via the PC board fingers to the video monitor. The video input affects only the display on the internal monitor; it does not appear at the composite video output.

6.5.12.12 Intensity Control – The video input and output circuits can produce a range of voltages (as compared with circuits that can produce only two values, white or black levels for example). To do this they are biased into linear operating conditions. Because of the high power dissipation that results, the video circuits use discrete transistors.

Direct drive video is the output from the terminal controller to the video monitor's cathode driver transistor. It is a combination of video out 1 and 2 signals from the video processor, and by means of a transistor Q3, the signal from the video input (analog video in J9). The monitor already receives horizontal and vertical deflection signals directly from the terminal controller, so the terminal's video input only requires picture information. If the blanking level on the video input is greater than zero volts, the screen background intensity cannot be black. Note that composite sync on the input is also ignored by the terminal controller, because the terminal's timing is produced entirely by a crystal and cannot be synchronized to external signals. External sources may be synchronized with the composite sync signal that appears at the output jack (J9).

Transistors Q3 and Q4, in parallel, are one amplifier with common emitter and collector resistors. The collector load of the parallel transistors is the input impedance of the monitor to ground in parallel with a five resistor ladder network. The resistor inputs come from digital to analog latches via open collector buffers. The D/A latches are written into as an I/O device by the microprocessor. In set-up mode, the 8080 microprocessor uses the up and down cursor keys as inputs to a 5-bit software up-down counter. At each vertical reset, the microprocessor writes the current contents of the counter into the latch. Thus there are 32 possible intensity levels available, controlled from the keyboard, and frequently updated to minimize the effects of soft errors. Note that the variable intensity only applies to the internal monitor.

6.5.13 Microprocessor – Video Processor Interface

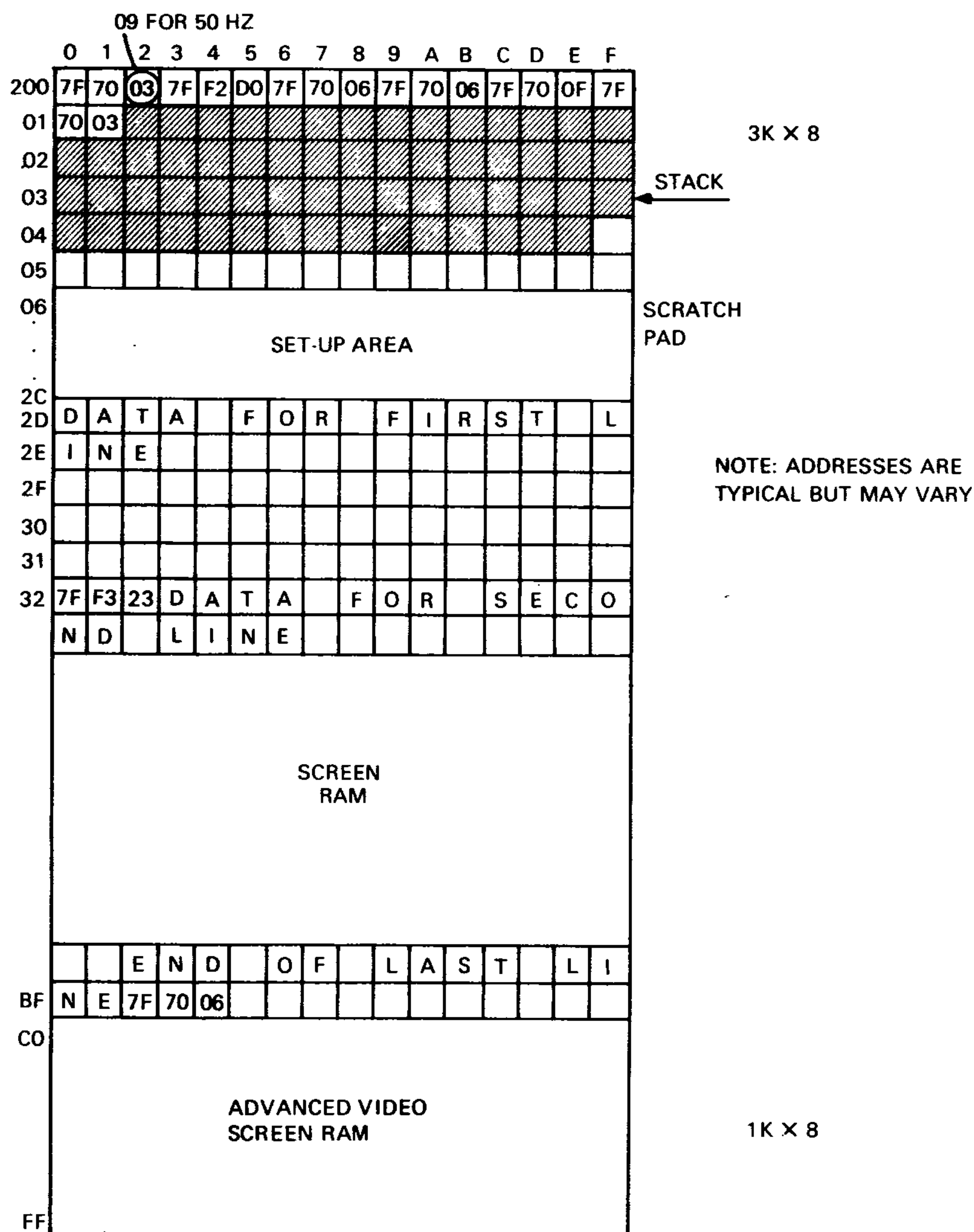
The microprocessor communicates with the video processor in the following ways.

1. During set-up, the microprocessor reads the set-up specifications and writes them into the DC011 and DC012 to establish screen attributes.
2. The contents of the screen RAM directly control the display of the lines and characters. This region of memory contains the displayable characters, their attributes, the line attributes, and the addresses that link one line to the next. The microprocessor modifies and updates this information in the intervals between DMAs. During each DMA, the video processor copies one line of characters from the screen RAM for display on the screen.
3. During smooth scrolling, the microprocessor updates the scroll latch in the DC012.

6.5.13.1 Screen Memory Organization – Three bytes of control data are located at the end of each line of characters. The first byte, called the terminator, is 7FH and is a unique character that the video processor recognizes as the end of the line. (The high bit is not tested by the terminator gate but is set to zero to avoid complications in the attribute circuits.) Five bits of the next byte and all of the last byte are an address pointing to the first character of the next line to be displayed. The three remaining bits in the first byte define the line attributes of the line pointed to by the address. The high bits of the address are hardwired at the address latch so that when vertical reset clears the address counter, it will point to the ROM-RAM boundary at 2000H.

During power-up or reset the microprocessor writes terminators and addresses into the screen RAM according to the specified line length and refresh rate. The 50/60 Hz refresh choice causes the microprocessor to arrange fill lines to place the beginning of the display in the right time slot relative to the vertical reset and vertical blanking signals. The line length determines the locations of the control bytes. For 80 column lines, the memory space is arranged in 83-byte intervals; for 132 columns, the interval is 135.

The memory organization for 80 column, 60 Hz mode is shown in Figure 6-20. Location 2000H is the start of the RAM space. When vertical reset resets the DMA address counter in the video processor to zero, the counter latch points to this location. The first 18 bytes are fill lines. Byte 2 is the only one written differently when 50 Hz refresh is selected. The change causes a longer fill time during the longer vertical blanking interval.



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Figure 6-20 Screen RAM Organization – 80 Column, 60 Hz

About 700 bytes of RAM are reserved for the microprocessor stack, scratchpad, and set-up areas. The rest of the 3K RAM is devoted to screen information. At program start, the microprocessor reads the contents of the NVR into the set-up area. Then the microprocessor reads the set-up parameters, erases the screen area, and writes in terminator and address/attribute bytes at the selected line length intervals. The address at the end of each line points to the first location of the next line. At start-up, this is the next physical location. The end of the last line points to a fill line, which points to itself. The fill line repeats until vertical reset.

6.5.13.2 Line Organization – In 132-column mode, 25 lines are set up in the RAM for a 24 line screen, and 15 lines are set up for a 14 line screen. With the advanced video option, 25 lines are set up for either 80 or 132 column lines. Except during a smooth scroll, only 24 lines are seen. But the microprocessor keeps the twenty-fifth line erased in reserve, and when a scroll takes place, the twenty-fifth line becomes visible as the new top or bottom line (depending on scroll direction). All new characters after the command that caused the scroll, go into this line. In preparation for a full screen scroll up, the microprocessor writes the address of the repeating fill line into the twenty-fifth line pointer as well as the twenty-fourth line pointer. This saves processing time during the address rearranging that is a part of each scroll.

The line organization changes when the first scroll occurs. Pointer addresses are revised any time a line is added to or removed from the screen. The extra line is used whenever the screen needs to be scrolled up or down. Then the extra line is displayed; and the old top or bottom line is scrolled off screen, erased, and made available as the new twenty-fifth line.

6.5.13.3 Scrolling Region – A scrolling region may be established on the screen on a horizontal line basis, within which data may be inserted or lines scrolled without affecting the positions of data outside the region. Only one region may be defined at a time, but it may be repeatedly redefined. Full screen scrolling is a special case in which the region margins and the screen margins are the same. A control sequence defines the region by specifying the line numbers of the top and bottom of the region. When the control sequence arrives, the microprocessor stops taking characters from the silo and waits for the current scroll to end. It then checks the parameters for legality (top less than bottom, bottom less than 14 or 24). If they are bad, the sequence is ignored and the next character is taken from the silo. If they are good, they are stored in locations labeled top and bottom. Then, starting at the pointer address on the last fill line, the microprocessor sets the fill line's scroll attribute bit to scroll or no scroll depending on the specification for top margin. The microprocessor then jumps to the end of the addressed line, setting its scroll attribute bit. The microprocessor continues down through the screen RAM until it reaches the top line of the scrolling region. It sets that attribute bit to scroll. Jumping down through the region, the microprocessor continues setting line attributes to scroll until it reaches the bottom line in the scrolling region. From there to the end of the screen it sets the bit to no scroll.

6.5.13.4 Cursor – The microprocessor keeps a running account of the cursor position. It starts at the reset position, line 1 – column 1 (top left corner) and responds to any change in position that might result from receiving a new character, a cursor position command, a line feed, etc. The microprocessor calculates the appropriate screen RAM address from the combination of previous line and column plus change in position, or from the specified line and column in a direct cursor address (DCA) control sequence. The microprocessor then records the current setting of the base attribute bit of the character at that address and then periodically inverts the attribute bit, showing the operator that the cursor is located at the spot on the screen where the attribute appears and disappears.

When a line scrolls on the screen, its location in RAM remains the same. To keep the cursor at the same screen location as before, representing the cursor moving down through the lines, the microprocessor calculates a new address for the cursor at the same column number but in the RAM location corresponding to the next line. Then, after resetting the attribute at the old location to its original value, it records and then toggles the attribute bit at the new location.

The attribute bit that the microprocessor toggles and the appearance on the screen depend on the set-up selection of the cursor attribute and on the absence or presence of the AVO. If the AVO is not installed, the microprocessor toggles the eighth bit in each character word. A set-up selection of reverse video causes the microprocessor to set the DC012 to interpret its base attribute input (REV VID H) as reverse video. If set-up specifies that underline is to be used for the cursor, the DC012 is set to interpret the base attribute as underline instead of reverse. Notice that without the AVO the cursor selection determines the appearance for all characters on the screen that have the attribute asserted. Furthermore, the microprocessor will accept the commands for either reverse or underline to assert the attribute.

With the AVO present, the microprocessor tells the DC012 to interpret the base attribute as reverse video. The cursor selection in set-up determines whether the microprocessor toggles the base attribute bit (eighth character bit) to get reverse video or one of the bits in the AVO RAM to get underline. With the AVO present, cursor selection is independent of attributes and all attributes are available at the same time.

6.5.13.5 Set-Up – The set-up area is a portion of the scratch RAM. It contains 8-bit bytes that are passed between the RAM and the NVR. Here is a list of the set-up area contents. This list is subject to change.

22 bytes	–	Answerback message (20 characters and 2 delimiters)
17 bytes	–	Tabs encoded in bits
1 byte	–	80/132-column mode
1 byte	–	Intensity
1 byte	–	Mode byte for PUSART
1 byte	–	On-line/local
1 byte	–	Switchpack 1 (scroll, auto repeat, screen, cursor)
1 byte	–	Switchpack 2 (bell, keyclick, ANSI/VT52, XON/XOFF)
1 byte	–	Switchpack 3 (US/UK #, wraparound, new line, interlace)
1 byte	–	Switchpack 4 (parity sense, parity, bits/character, power)
1 byte	–	Switchpack 5 (STP – visible only when the option is installed)
1 byte	–	Transmit baud rate
1 byte	–	Receive baud rate
1 byte	–	Parity
1 byte	–	Checksum for NVR

When the SET-UP key is pressed, the silo locks and any scroll in progress is allowed to finish. Now the 25th line (Extra) is available for one of the lines at the bottom of the screen. Another 135 bytes are available as line Extra2 for use as the other of the two bottom lines or for the NVR buffer area and the WAIT message displayed during NVR operations. Another 125 bytes are the set-up screen RAM. They store the words “SET-UP A” twice (for double-height) and the words “To exit press SET-UP” with the three lines’ terminator and address bytes, plus 19 more terminators and addresses for the 19 blank lines in the middle of the set-up screen.

For SET-UP A, the microprocessor performs a routine to fill the line at the bottom of the screen with a ruler. The other free line displays the cursor and letters T to indicate tab positions. Then the microprocessor counts from the beginning of the tab bytes in the set-up area to find the bit corresponding to the column number where the cursor is. If the bit is set, the microprocessor writes the letter T in the current cursor position. Keys (set/clear tab, clear all tabs) on the keyboard can toggle the setting of the bit in the set-up area, and the microprocessor writes or erases the T to agree.

For SET-UP B, the microprocessor displays the data contained in the switchpack and baud rate area by writing corresponding information into the bottom line. Switchpack 5 is only displayed if the option present flag is asserted at the STP. The other free line is not written into but is used to display the cursor position and to display the answerback message when the message is being entered. The switchpack data is changed by a key on the keyboard (toggle 1/0).

The nonswitchpack data is changed by separate keys. These include parameters that display themselves — line/local, displayed in the LEDs, and 80/132 column, seen on the screen. Transmit and receive are displayed numerically. Parity is displayed numerically in later models. Switching between set-up fields and starting reset can also be done with separate keys on the keyboard.

6.6 VT18X CONTROL MODULE DESCRIPTION

The VT18X control module is designed to fit into an option slot of the VT180 expansion backplane to allow the VT100 to function as a personal office computer in addition to its usual function as a satellite terminal to an external host. The module contains a Z80A microprocessor, which gives the terminal the capability to run existing control programs for microprocessor (CP/M) applications.

The VT18X control module has the following general features.

1. 4.0 MHz Z80A CPU.
2. 64K byte dynamic RAM with hardware refresh.
3. Up to 8K byte ROM selected upon power-up and software deselectable and configurable for 2716 type UV EPROMs.
4. Console port for communication with the basic VT100.
5. Serial printer port for Digital printers.
6. Communications port running at a baud rate set through the VT180 set-up mode with full VT131 communications hardware support and a synchronous external clock select mode.
7. General purpose serial port.
8. Communications receive-only interrupts.
9. Real time clock interrupt (13.2 ms).
10. Disk drive controller for up to four 5¼ inch 48 TPI disk drives with MFM recording technique (double-density).
11. All I/O devices are accessible by Z80 I/O instruction only.

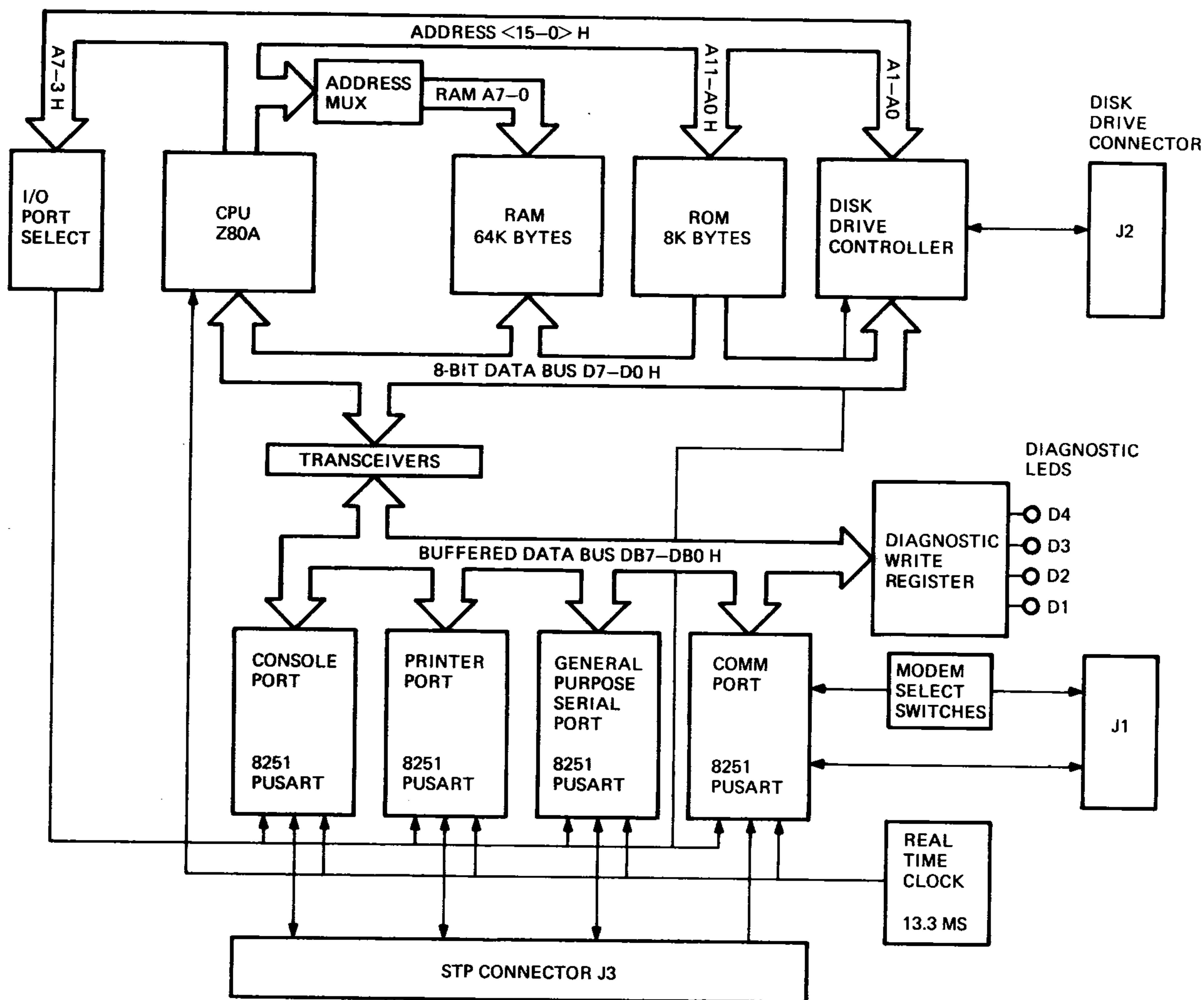
Figure 6-21 shows the major logical subunits of the VT18X control module and their relation to the address bus, the data bus, and the I/O connectors. The function of each logical subunit is described in the following paragraphs.

6.6.1 Z80A CPU

The Z80A is an 8-bit, parallel central processor unit (CPU). The Z80A transfers data and internal state information through an 8-bit, bidirectional data bus (D7–0 H). Memory and peripheral device addresses are transmitted over a separate 16-bit, unidirectional address bus (A15–0 H). Six Z80A outputs are used to control various functions performed by the logic circuits on the VT18X control module. Three inputs from the logic circuits on the VT18X control module are used for CPU control.

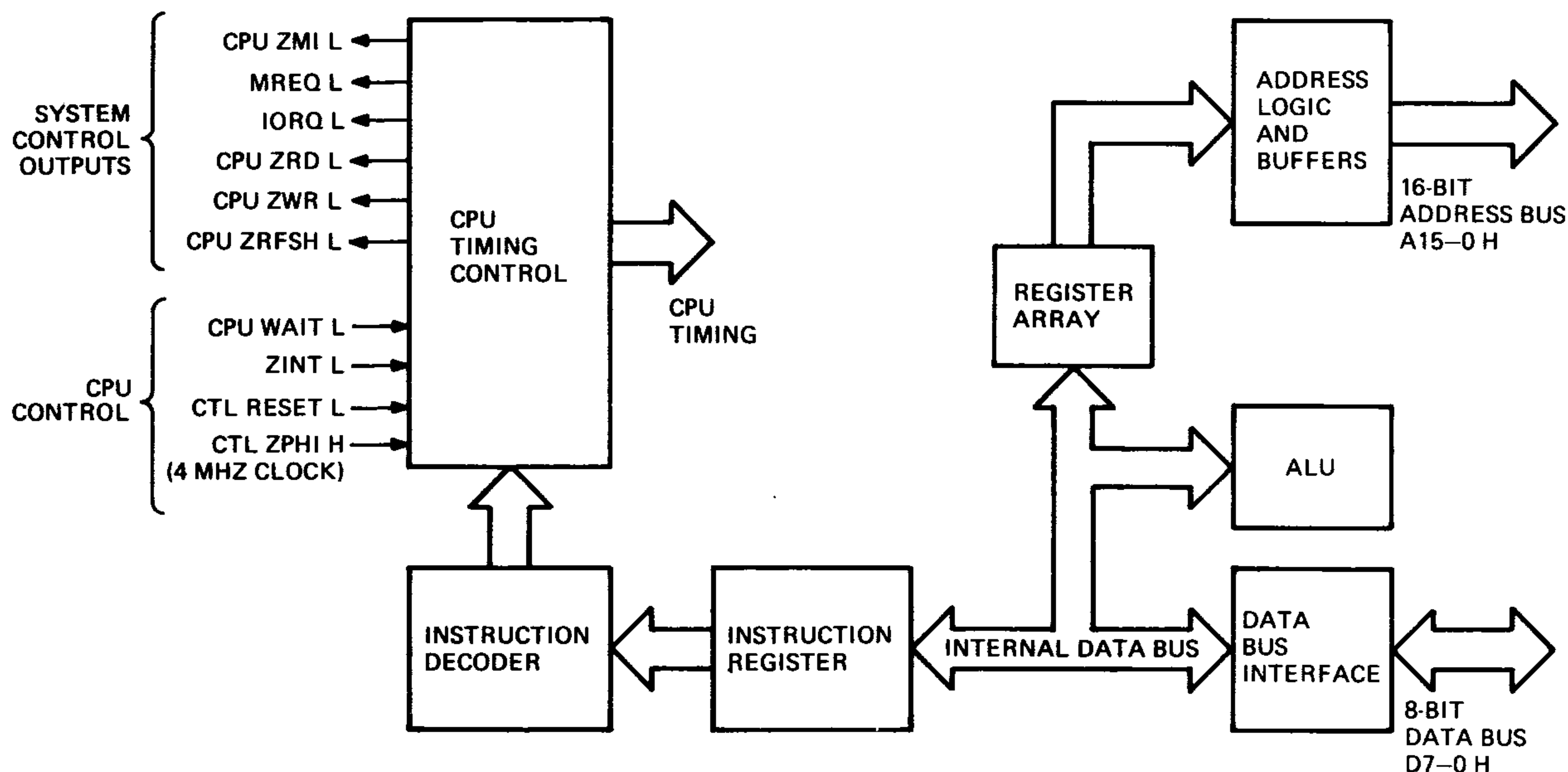
The Z80A internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers, which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of exchange instructions makes either set of main or alternate registers accessible to the programmer. The Z80A also contains a stack pointer, a program counter, two index registers, a refresh register (counter), and an interrupt register. The CPU requires only a single +5 V power supply source. All output signals are fully decoded and timed to control the memory and I/O devices. The Z80A block diagram is shown in Figure 6-22.

The Z80A operates at 4.0 MHz with no wait states for RAM, one wait state for ROM, and those wait states automatically inserted by the CPU for I/O instructions. All I/O is done by Z80A input or output instructions (no memory mapped I/O). Resets are done automatically upon power-up or can be done explicitly through the set-up reset sequence of the VT180. (The VT180 must be firmware operational.) Applications running with hardware dependencies are not supported. Only CP/M operating system calls for I/O are supported.



MR-8040

Figure 6-21 VT18X Control Module Block Diagram



MR-8041

Figure 6-22 Z80A CPU Block Diagram

6.6.2 Interrupts

The CPU accepts interrupts from the four 8251A PUSARTs and the real time clock (RTC). Figure 6-23 shows the relationship of the interrupting devices to the CPU and the address and data buses.

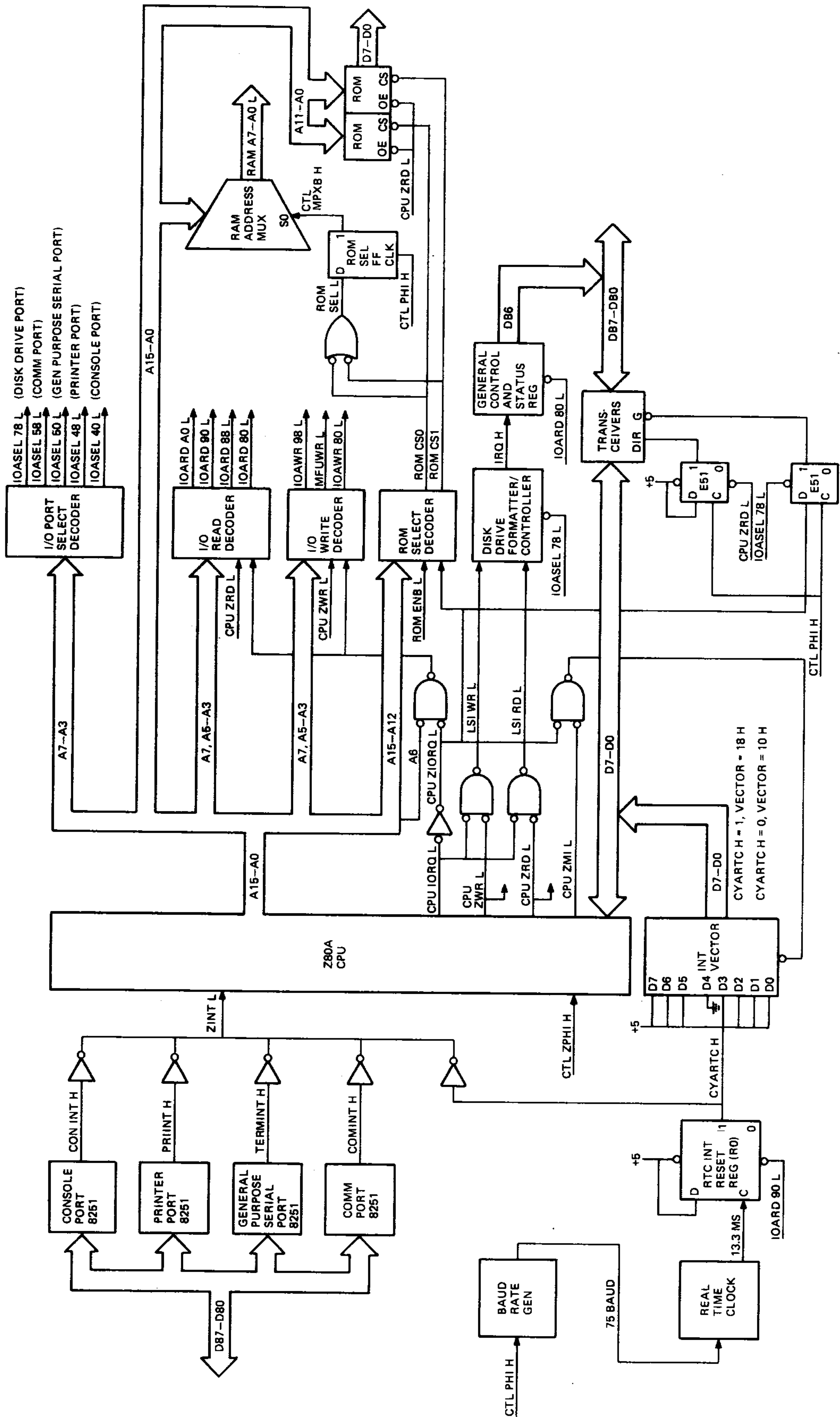
A PUSART will interrupt the CPU whenever its receiver buffer contains a character that is ready for input to the CPU. A CPU restart to location 10H occurs upon detection of an interrupt signal from any of the four PUSARTs. The CPU must then poll the PUSARTs to determine the source of the interrupt.

The real time clock signal (CYARTC H) interrupts the CPU every 13.3 ms and causes a restart to location 18H. RTC interrupts take precedence over PUSART interrupts and are reset by a dummy read to location 90H. All interrupts, including the RTC, are turned off while doing a disk drive I/O. Therefore, the RTC cannot be used for a time of day clock and is used only for communications control signal timing.

The interrupt output signals from the four PUSARTs and RTC are ORed together and become the maskable interrupt (INT) input to the CPU. Interrupts are implemented by the CPU as mode 0 maskable interrupts. A maskable interrupt is one that must be enabled in software in order to operate. In mode 0 interrupt operation, the interrupting device places a restart instruction on the data bus, which is then acted on six times by the CPU. The restart instruction causes an unconditional jump to location 10H for a PUSART interrupt or to location 18H for an RTC interrupt.

Interrupt Request/Acknowledge Cycle

The CPU samples the ZINT L signal with the rising edge of the last clock cycle (CTL ZPHI H) at the end of any instruction. When an interrupt is accepted, the CPU ZMI L cycle is generated. During this CPU ZMI L cycle, IORQ L becomes active to indicate that the interrupting devices can place an 8-bit vector on the data bus. The CPU automatically adds two CPU WAIT L states to this cycle.



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Figure 6-23 Microprocessor Interrupt Block Diagram

6.6.3 64K Byte RAM

The VT18X control module has 64K bytes of directly addressable RAM available for CP/M. The RAM is comprised of eight 64K by 1 parts whose address and control lines are connected in parallel. The bidirectional RAM data lines are connected to the CPU via the data bus (D7–D0 H). The block diagram in Figure 6-24 shows the RAM and its relationship to the CPU and associated logic.

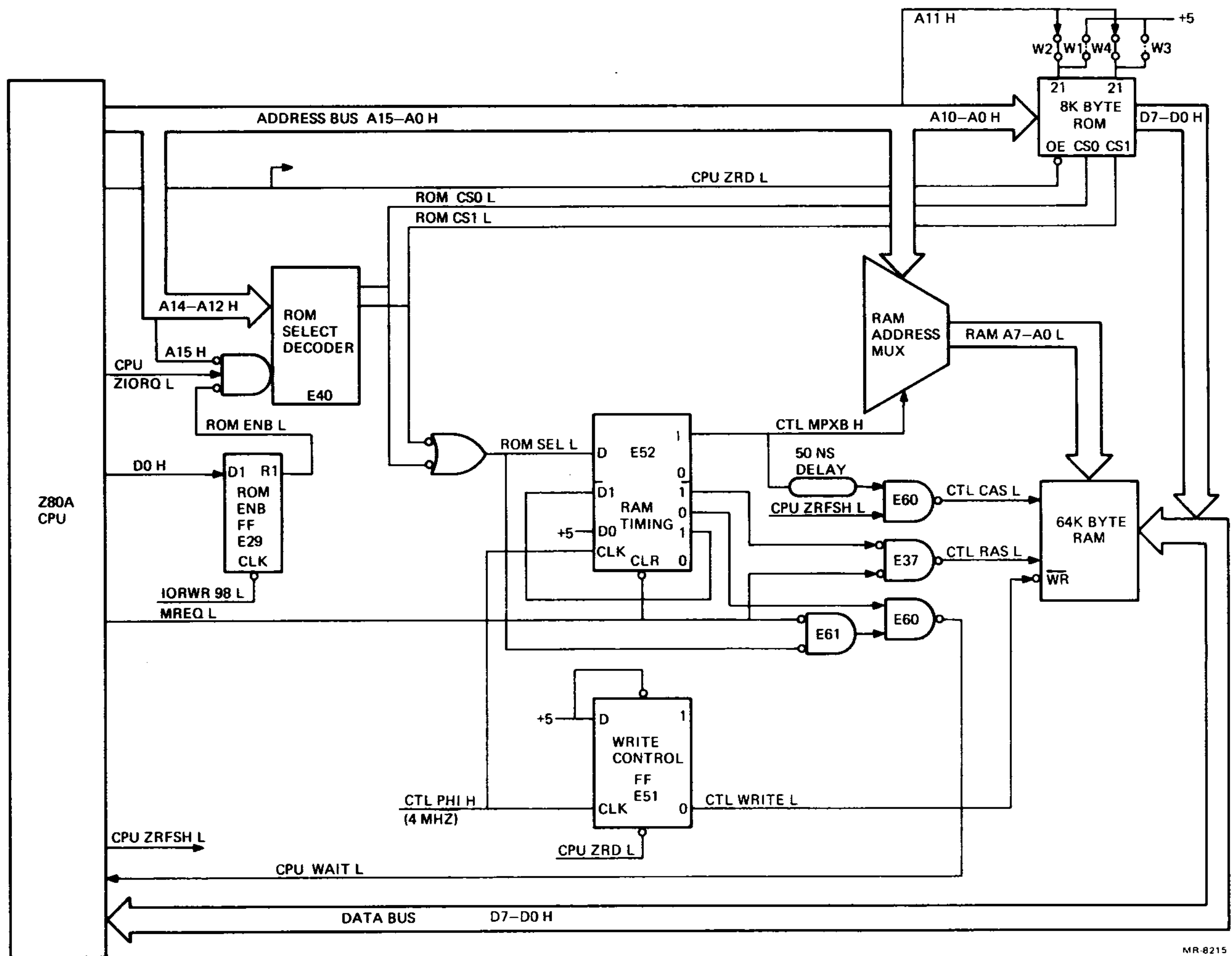


Figure 6-24 RAM and ROM Block Diagram

The RAM is 7-bit hardware refreshed by the CPU ZRFSH L signal. The RAM is refreshed during the third and fourth CTL PHI H clock pulses of a machine cycle one (M1) of an instruction op code fetch. CPU ZRFSH L together with MREQ L indicates that the lower seven bits of the address bus (A6–A0 H) can be used as a refresh address to the RAM.

The RAMs used are 64K parts with 128-cycle refresh. Only RAMs with the following Digital part numbers can be used.

21-18467-01
21-18470-01
21-18472-01

Before operating the RAM, a minimum of eight RAS cycles must be given to ensure data integrity. This can be accomplished by eight op code fetches or dummy reads from the RAM.

Memory Read or Write Cycle

A memory read or write cycle begins after the CPU places the contents of the program counter on the address bus (A15–A0 H). Approximately one-half clock cycle later, MREQ L goes active to indicate that the address bus holds a valid address for a memory read or write operation. MREQ L together with the output of the RAM timing FF D1 produces the row address strobe (CTL RAS L). The column address strobe (CTL CAS L) is generated 50 ns after CTL RAS L becomes active.

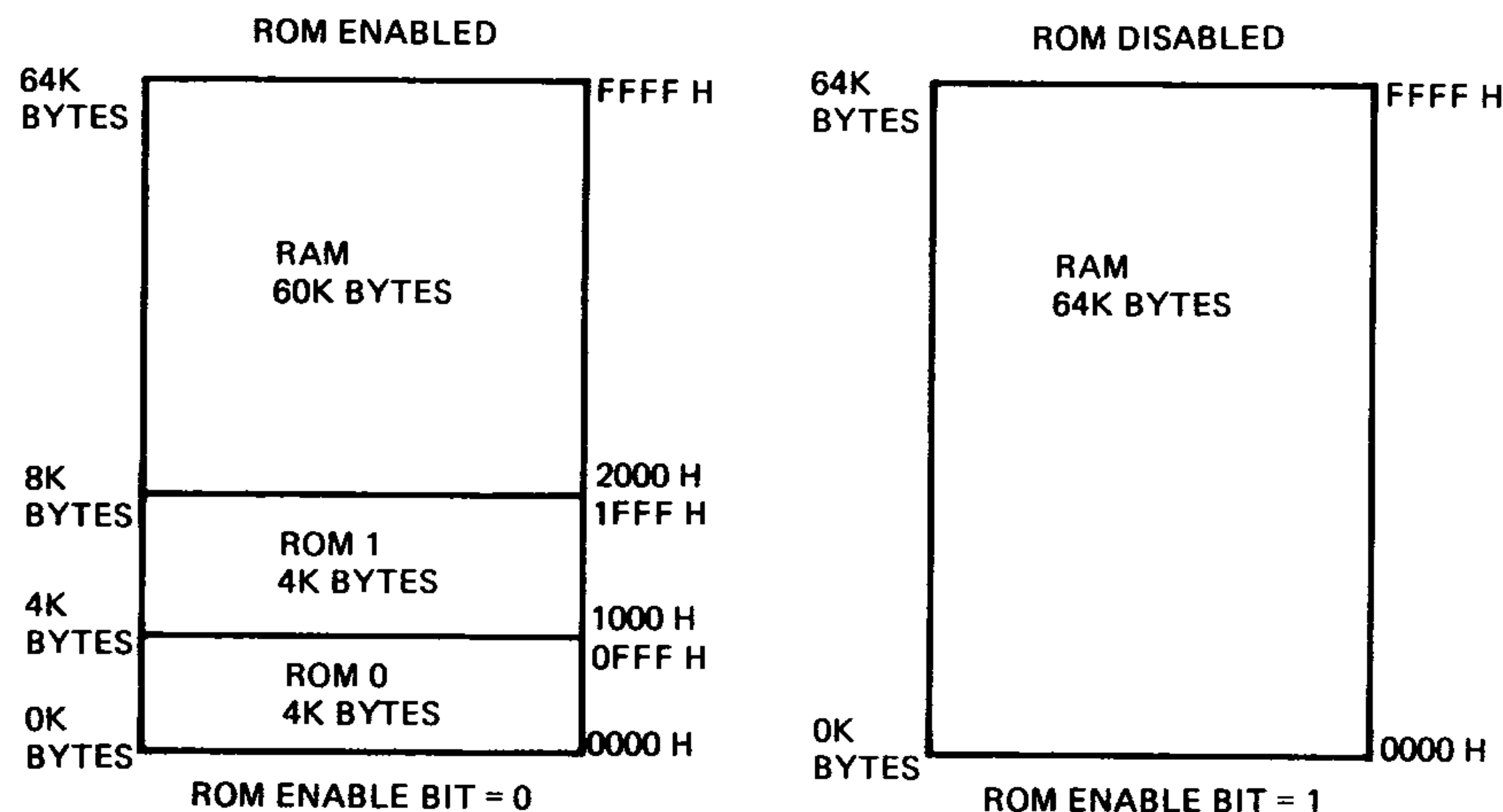
The read signal (CPU ZRD L) is connected to the clear input of the write control FF. In a read operation, CPU ZRD L goes active after the first CTL PHI H clock pulse and clears the write control FF. CTL WRITE L becomes active and allows the RAM data to be placed on the data bus.

In a memory write cycle, the write control FF is set as it was in a read cycle. However, in a memory write cycle CPU ZRD L is inactive and does not clear the write control FF. CTL WRITE L, therefore, is active and allows the data (D7–D0 H) to be written into the RAM location specified by address bits A15–A0 H.

6.6.4 8K Byte ROM

The VT18X control module contains space for up to 8K bytes of ROM (two 24-pin sockets). Figure 6-24 shows the ROM and its relation to the address bus, data bus, and associated logic. The ROMs supported are of the 2716 (2K × 8) and 2732 (4K × 8) pin out variety, with access times less than or equal to 450 ns.

The ROM contains diagnostics for the module, bootstrap code for CP/M, and a pass-through mode, which passes data between the VT180 and the communications port. (After ROM is disabled, the pass-through terminal mode is only available as an application run under CP/M.) The ROM is enabled upon power-up at location 0000 H and can be enabled or disabled by the least significant bit (D0 H) in port 98H. When the ROM is disabled, the full 64K bytes of RAM can be addressed. Figure 6-25 shows the 64K byte memory map with the ROM enabled and disabled.



MR-8055

Figure 6-25 64K Byte Memory Map

ROM Read Operation

Address bits A14–A12 H are used by the ROM select decoder to select the ROM to be read. If bits A14 through A12 are low, ROMCS0 L is active and ROM 0 is selected. If bit A12 is high and A14–A13 are low, ROMCS1 L is active and ROM 1 is selected. Address bit A15 L, together with CPU ZIORQ H and ROM ENB L enable the ROM select decoder. D0 H clocked into the ROM enable FF by IOAWR L will cause ROM ENB L to become inactive and disable the ROM select decoder. When D0 is low, it causes ROM ENB L to become active and enable the ROM when clocked by IOAWR L. The output of the ROM select decoder, ROMCS0 L or ROMCS1 L is sent to the chip select input of the ROMs and to an OR gate to produce ROM SEL L. ROM SEL L is the D input of a RAM timing FF. When ROM SEL L is clocked into the FF by CTL PHI H, CTL MPXB goes low and disables the RAM address multiplexer. CPU ZRD L then enables the ROM to output the data (D7–D0 H) from the location specified by the RAM address bits A10–A0 H.

6.6.5 Console Port

The console port on the VT18X control module communicates with the terminal controller module via the VT180 paddle board installed in the STP connector. The console transmit and receive data, transmit and receive clocks, and modem control signals are connected to a 16-pin IC socket (J3) on the VT18X control module. These signals are then routed to the terminal controller module through a ribbon cable connected to IC socket (J2) on the VT180 paddle board. Figure 6-26 shows the I/O ports and their relation to the I/O connectors, the data bus, and control logic. Transmit and receive baud rates are fixed by the 15.7 k baud clock (CON CK H) input on pin 3 of connector J3. This console clock is obtained from the video timing circuit (DCO11) on the terminal controller module.

RS-232C signals supported by the console port include transmit data (CON XMIT DATA H), receive data (CON REC DATA 1 H), and data terminal ready (CON DTR L) from the terminal controller module for control. Software must support XON/XOFF protocol for this port.

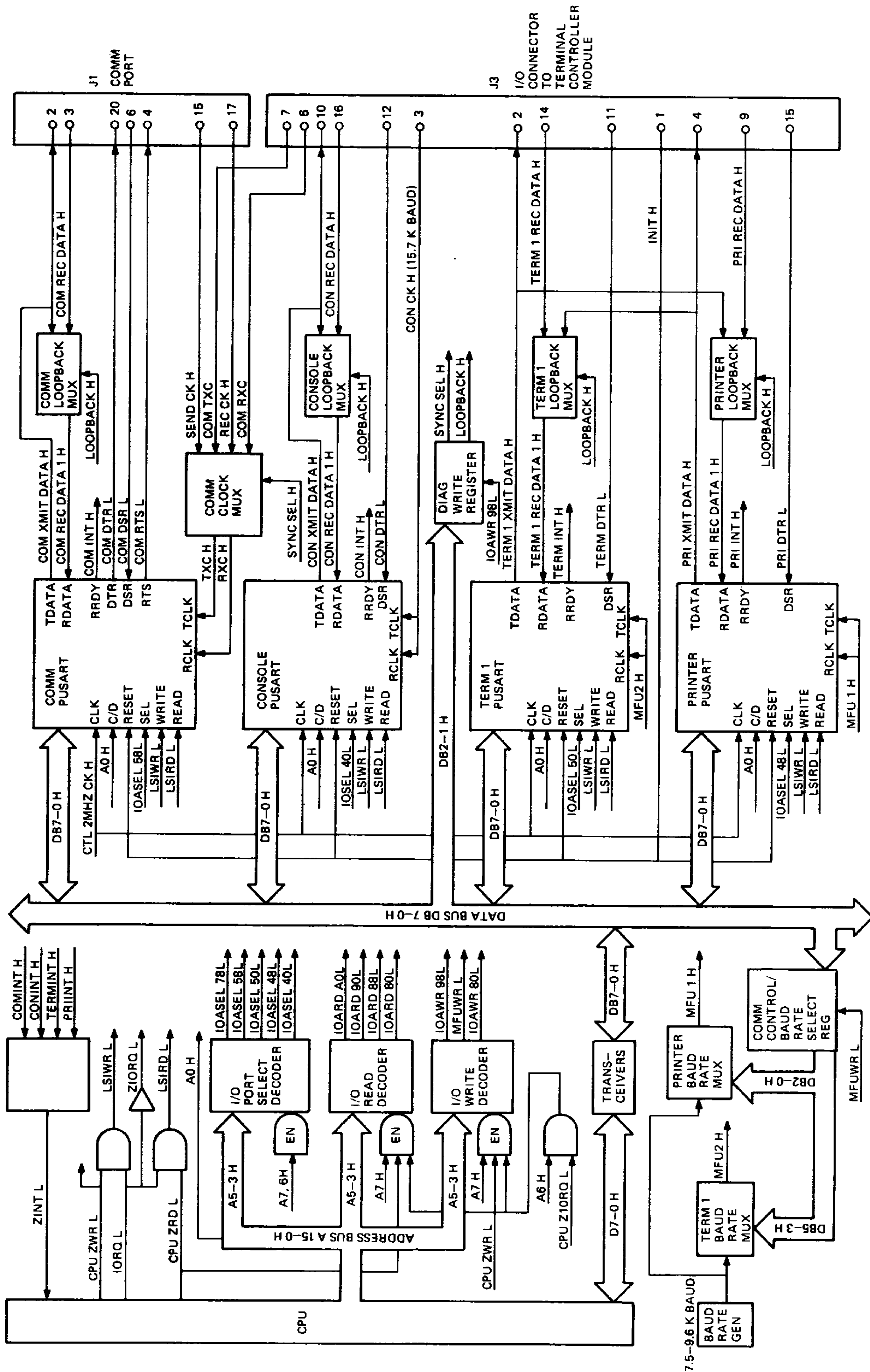
Console Port Functional Description

Address bits A5–A3 and A7–A6 from the CPU are used for select and enable inputs by the I/O port select decoder. The console PUSART is enabled when the CPU places address 40H on the address bus. The I/O port select decoder uses address bits A7–A3 of address 40H to generate IOASEL 40 L. This signal is applied to the select input to enable data to be written into or read from the console port data and control and status registers.

Address bit A0 applied to the console PUSART control/data (D/D) input is used, in conjunction with the write (LSIWR L) and read (LSIRD L) signals, to inform the PUSART that the word on the data bus (DB7–0 H) is either a data character, control word, or status information. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

The LSIWR L signal obtained by ANDing the CPU ZWR L and IORQ L signals asserted by the CPU is used to inform the console PUSART that it is outputting data or control words. The CPU asserts LSIRD L when it reads data or status information from the console PUSART.

Data transmitted by the console PUSART is taken from the data bus in parallel and converted to a serial bit stream by the PUSART's transmitter buffer. The transmitter buffer inserts the appropriate bits (based on communications techniques) and a composite serial stream of data (CON XMIT DATA H) is clocked out by CON CK H to pin 10 of connector J3. CON XMIT DATA H is also sent to the console loopback multiplexer to be used as the received data input to the console PUSART during diagnostic testing. The transmitted data output on pin 10 of J3 is sent to the received data input of the communications PUSART on the terminal controller module.



MR 8216

Figure 6-26 I/O Port Control Block Diagram

Data (CON REC DATA H) is received by the console PUSART from pin 16 of I/O connector J3 via the console loopback multiplexer. The received data for the console PUSART is data transmitted by the communications PUSART on the terminal controller module. The received serial data is clocked into the console PUSART by CON CK H, converted to parallel format in the receiver buffer, and checked for bits or characters that are unique to the communications technique. The console PUSART then asserts CON INT H to inform the CPU that the receiver buffer contains a valid character ready for input to the CPU.

The console data terminal ready (CON DTR L) connected to the data set ready (DSR) input of the console PUSART is obtained from the data terminal ready (DTR) output of the communications PUSART on the terminal controller module.

6.6.6 Communications Port

The communications port (Figure 6-26) is used to communicate with a host computer when the VT180 is operated in terminal mode. It has full modem support and supports the same signals as the VT131. United States and European full- and half-duplex modems can be supported by RS-232C (V.24/V.28) physical interface conforming to CCITT V.21, V.22, and V.23. This port supports break detection. The transmit and receive baud rate clocks for this port are derived from the baud rate generator on the terminal controller module. Therefore, the transmit and receive baud rates selected in the VT180's set-up mode are the transmit and receive baud rates for this port and must be set to match the transmit and receive baud rates of the host computer. Baud rates supported are 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19.2 k baud. Any and all protocols to be supported by this port, other than pass-through mode, are run as applications under CP/M.

The communications port contains a ten position switchpack (E22), which must be set to permit operation with a particular modem. Figure 6-27 shows the switches and the modem signals that must be switched. Table 6-9 describes the various modems supported by the communications port and the switch configuration required for each modem.

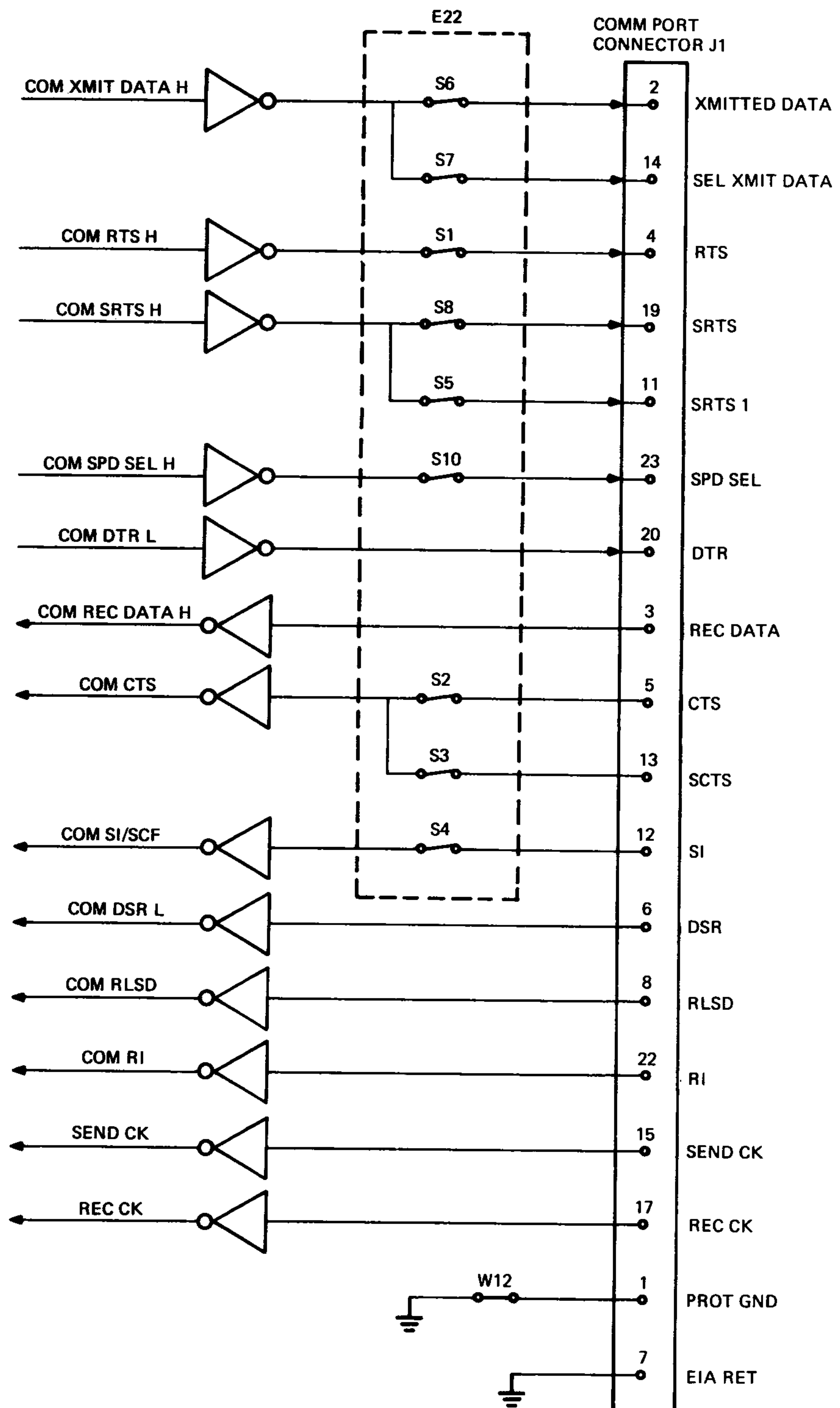
The communications port signals are connected to a 25-pin, D-type EIA connector residing on the VT18X control module.

Table 6-9 Communication Modem Switch Configuration

Modem Type	Switch Settings*									
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
Bell 103-X 300B, FDX, ASYNC, 2-W, 113-X	C	C	O	C	O	C	O	C		O
Bell 202-X 1200 B, FDX, ASYNC, 2-W, 1200B, BDX, ASYNC, 4-W	C	C	O	C	O	C	O	C		O
	C	C	O	C	O	C	O	C		O
Bell 212A 1200B, FDX, ASYNC, 2-W**	C	C	O	C	O	C	O	C		O

*Switch S9 not used. C = Closed, O = Open

**S10 must be closed when using the speed select feature of the Bell 212A.



MR-8042

Figure 6-27 Communications Port Modem Switches

Communications Port Functional Description

The communications PUSART is enabled for reading or writing by IOASEL 58 L from the I/O port select decoder when the CPU places address 58H on the address bus. Address bit A0, together with write (LSIWR L) or read (LSIRD L) are used to perform the same function for the communications PUSART as they did for the console PUSART. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

Serial data transmitted (COM XMIT DATA H) is clocked out of the PUSART by TXC H and routed to pin 2 of the communications port connector (J1). The transmitted serial data is also applied to the communication loopback multiplexer to be used as the received data input to the communications PUSART during diagnostic testing.

Serial data (COM REC DATA H) is received from the host computer via pin 3 of the communications port connector (J1) and clocked into the communications PUSART by RXC H. The communications PUSART converts the serial data to parallel data, checks for bits and characters that are unique to the communications techniques, and then asserts COM INT H to inform the CPU that the receiver buffer contains a valid character ready for input to the CPU.

The communications PUSART receives its transmitter (TXC H) and receiver (RXC H) clocks from the communications clock multiplexer. The transmitter and receiver clock inputs to the clock multiplexer are obtained from two sources. SEND CK H and REC CK H are received from the host computer via pins 15 and 17 of communications port connector (J1). COM TXC and COM RXC are received from the baud rate generator on the terminal controller module via pins 6 and 7 of connector J3. The status of SYNC SEL determines which set of clocks will be used by the communication PUSART. SYNC SEL is high when bit 2 (DB2) of the diagnostic write register (address 98 H) is programmed to one. When SYNC SEL is high, the host computer supplies the transmitter and receiver clocks for the communications PUSART. SYNC SEL is low when the VT180 is operated in personal computer mode and the transmitter and receiver clocks are supplied by the baud rate generator on the terminal controller module.

The three modem control signals (COM RTS L, COM DSR L, and COM DTR L) are always programmed at power-up to allow normal full-duplex operation with some modems when a standard EIA cable is installed between the modem and the VT180.

6.6.7 Printer Port

This is a general purpose printer port (Figure 6-26), which provides an RS-232C interface compatible with Digital printers. EIA signals supported are transmit data, receive data, and data terminal ready. Software programmable baud rates to be supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Software programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. Software should support XON/XOFF protocol for this port. The 25 D-type pin EIA printer connector physically resides on the VT180 paddle board in the normal printer port location and, just as previous VT100 printer ports have, uses a null modem cable to attach to a printer.

Printer Port Functional Description

The printer PUSART is enabled for reading or writing by IOASEL 48 L when the CPU places address 48H on the address bus. Address bit A0 with write (LSI WR L) or read (LSIRD L) is used to perform the same functions for the printer PUSART as it did for the console PUSART. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

Serial data transmitted (PRI XMIT DATA H) is clocked out of the PUSART by MFU1 H and routed to pin 4 of I/O connector J3. The transmitted serial data is also applied to the term 1 loopback multiplexer to be used as the received data input to the term 1 PUSART during diagnostic testing.

Serial data (PRI REC DATA H) during normal operation is received from the printer on pin 9 of the I/O connector J3 and routed through the printer loopback multiplexer to the receiver data input of the printer PUSART. During diagnostic testing, the transmitted data (TERM 1 XMIT DATA H) from the term 1 PUSART is routed through the loopback multiplexer to become the receiver data input for the printer PUSART. The received serial data is clocked into the receiver buffer of the printer PUSART by MFU 1. The PUSART then notifies the CPU that a character is ready for input by asserting PRI INT H.

The MFU 1 signal is used as both transmitter and receiver clocks for the printer PUSART. Therefore, split baud operation is not supported by the printer port. MFU 1 is the output of the printer baud rate multiplexer whose eight baud rate inputs are obtained from the baud rate generator. The baud rate for MFU 1 H is selected by programming bits 2–0 of the communications control/baud rate select register at address 90H.

6.6.8 General Purpose Serial Port

This port is provided as a general purpose RS-232C interface. Signals supported are transmit data, receive data, and data terminal ready. Software programmable baud rates to be supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Software programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. This port uses the term 1 PUSART (Figure 6-26). The term 1 PUSART transmits and receives data through connector J4 on the terminal controller module. Note that connector J4 was used as the communications port connector in the VT100. In the VT180, however, J4 is used as a general purpose serial port. Signals are passed between the term 1 PUSART and the general purpose serial port J4 via the VT180 paddle board and ribbon cable connected to I/O connector J3 on the VT18X control module.

General Purpose Serial Port Functional Description

The term 1 PUSART is enabled for reading or writing by IOASEL 50 L from the I/O port select decoder when the CPU places address 50H on the address bus. Address bit A0 with write (LSIWR L) or read (LSIRD L) is used to perform the same functions for the term 1 PUSART as it did for the console PUSART. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

Serial data transmitted (TERM 1 XMIT DATA H) is clocked out of the PUSART by MFU 2 H and routed to pin 2 of I/O connector J3. The transmitted serial data is also applied to the printer loopback multiplexer to be used as the received data input to the printer PUSART during diagnostic testing.

Serial data (TERM 1 REC DATA H) is received from pin 14 of the I/O connector J3, routed through the term 1 loopback multiplexer, and clocked into the PUSART by MFU 2 H. The term 1 PUSART converts the serial data to parallel data, checks for bits and characters that are unique to the communications techniques, and then asserts TERM INT H to inform the CPU that the receiver buffer contains a valid character ready for input to the CPU.

The MFU 2 H signal is used as both transmitter and receiver clocks for the term 1 PUSART. Therefore, split baud operation is not supported by the general purpose serial port. MFU 2 H is the output of the term 1 baud rate multiplexer whose eight baud rate inputs are obtained from the baud rate generator. The baud rate for MFU 2 H is selected by programming bits 5–3 of the communications control/baud rate select register at address 90H.

6.6.9 Terminal Controller and VT18X Control Module Interconnections

The VT18X control module is connected to the terminal controller module via a 16-pin ribbon cable to the VT180 paddle board. Figure 6-28 shows the signal interconnections and indicates the signal direction through the ribbon cable and paddle board. This interconnection is very important in the operation of the

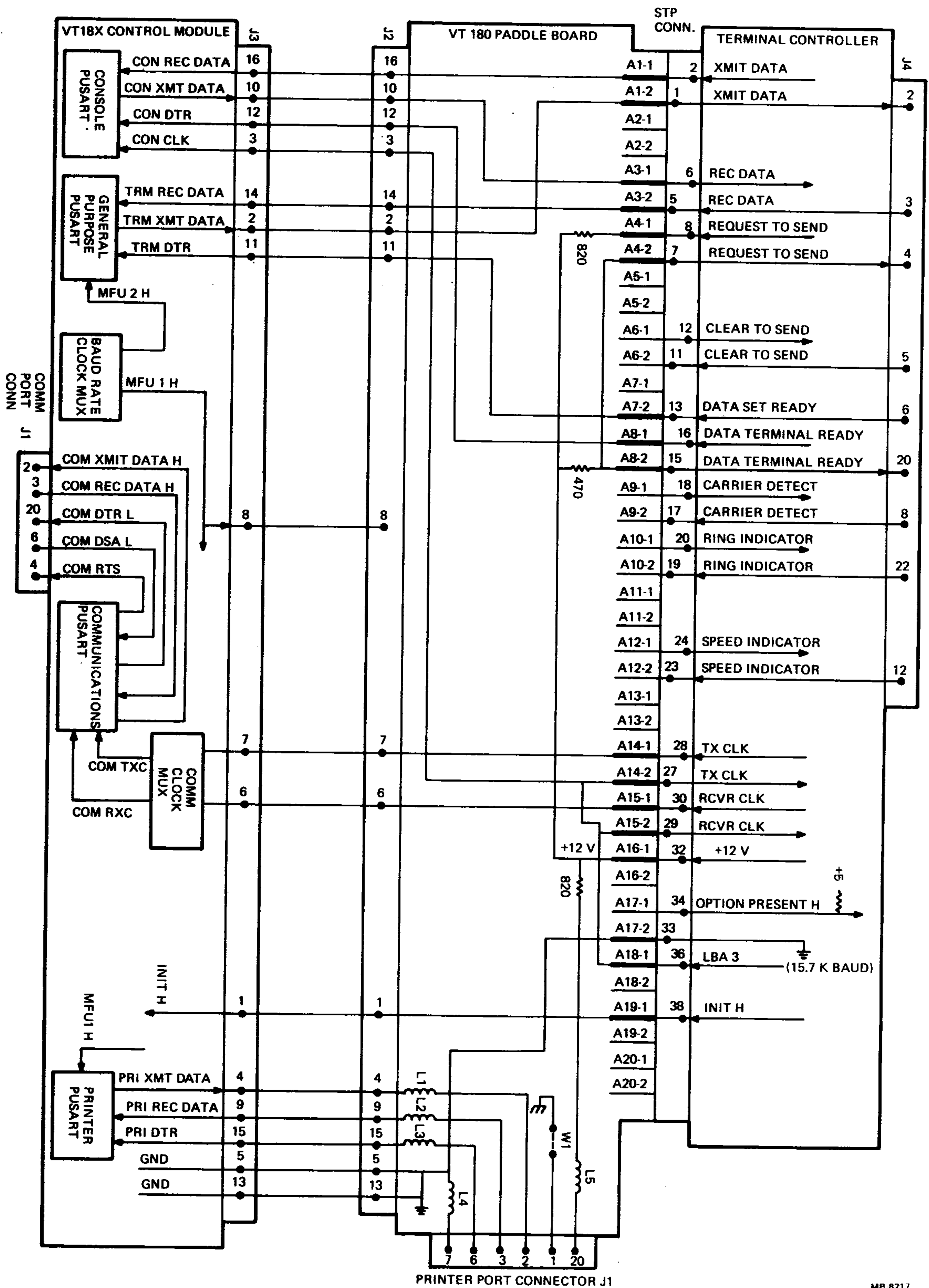


Figure 6-28 Terminal Controller and VT18X Control Module Interconnections

VT180. All four serial ports depend upon signals from the STP connector. Note that the transmit and receive data lines for the communications PUSART and printer PUSART are not routed through the STP connector but instead are routed through individual connectors. The INIT signal from the terminal controller module is also routed through the STP connector to the VT18X control module and is used as a general reset signal (CTL RESET) for all four serial ports and other logic on the module.

6.6.10 Disk Drive Controller

The disk drive interface is designed to control up to four 5¼ inch disk drives. The controller supports double-density drives using a phase-locked loop (PLL) circuit. Etch is also present on the VT18X control module for a state machine data separator, which is suitable for single-density operation, but it is not used. The controller circuits support only soft-sectored, single-sided diskettes.

The disk drive controller converts binary data from the CPU into modified frequency modulated (MFM) data. The MFM data is then transmitted to the disk drive where it is recorded on the diskette. MFM is a magnetic recording method for disk drives in which a clock signal is encoded in the flux transitions recorded on the diskette. When reading data from the diskette, the disk drive controller synchronizes on the data transitions, and with a PLL and MFM decoder, recovers the clock and data.

The disk drive controller data and control lines are routed to a 37-pin, D-type connector (J2) that physically resides on the VT18X control module. Connection from connector J2 to the disk drives is made via a 37-pin shielded cable (BC26K).

6.6.10.1 Disk Drive Controller Functional Description – The disk drive controller is comprised of a disk drive formatter/controller, a phase-locked loop, and associated logic. The functional relationship of the major components is shown in Figure 6-29 and described in the following paragraphs.

6.6.10.2 Formatter/Controller – The disk drive formatter/controller is a 40-pin, MOS, LSI circuit chip (WD1793). The 1793 IC contains a number of registers and other logic, which are used to manage the various functions provided by the formatter/controller. A brief description of the internal registers and associated logic is given in the following paragraphs.

The formatter/controller will accept eleven commands from the CPU. The commands are loaded into the command register to specify the disk drive operation presently being executed. The commands are divided into four types and are described in Paragraph 6.6.14.

Data Shift Register

This 8-bit register assembles serial data from the read data input (RAW READ) during read operations and transfers serial data to the write data (WD) output during write operations.

Data Register

This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel to the data register from the data shift register. In disk write operations, information is transferred in parallel from the data register to the data shift register. When executing the seek command the data register holds the address of the desired track position. This register is loaded from or gated onto D7–D0 under processor control.

Track Register

This 8-bit register holds the track number of the current read/write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during diskette read, write, and verify operations. The track register can be loaded from or transferred to D7–D0. This register should not be loaded when the device is busy.

Sector Register (SR)

This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The sector register contents can be loaded from or transferred to D7–D0. This register should not be loaded when the device is busy.

Command Register (CR)

This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a forced interrupt. The command register can be loaded from D7–D0 but not read onto D7–D0.

Status Register (STR)

This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto D7–D0 but not loaded from D7–D0.

CRC Logic

This logic is used to check or to generate the 16-bit cyclic redundancy check (CRC). The polynomial is: $G(x)=x^{16}+x^5+1$. The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic Logic Unit (ALU)

The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the diskette recorded ID field.

Timing and Control

All computer and disk drive interface controls are generated through this logic. The internal device timing is generated from an external crystal clock (CTL 1 MHz CLK) applied to pin 24.

The formatter/controller has two different modes of operation according to the state of DDEN. When DDEN equals 0, double-density (MFM) is assumed. When DDEN equals 1, single-density (FM) is assumed.

AM Detector

The address mark detector detects IC, data, and index address marks during read and write operations. The input/output signals of the formatter/controller are divided into two basic groups. Signals that are used for CPU interface control and those that are used for disk drive interface control. The signal functions and their pin locations are listed in Table 6-10.

Table 6-10 Formatter/Controller Pin Identification

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function																				
1	No connection	NC		Pin 1 is internally connected to a back bias generator and must be left open by the user.																				
19	Master reset	MR	CTL RESET L	A logic low on this input resets the device and loads hex 03 into the command register. The not ready (status bit 7) is reset during MR ACTIVE. When MR is brought to a logic high, a restore command is executed regardless of the state of the ready signal from the drive. Also, hex 01 is loaded into sector register.																				
20	Power supplies	Vss		Ground																				
21		Vcc		+5 V $\pm 5\%$																				
40		Vdd		+12 V $\pm 5\%$																				
Computer interface:																								
2	Write enable	WE	LSI WR L	A logic low on this input gates data on D7–D0 into the selected register when CS is low.																				
3	Chip select	CS	IOASEL 78 L	A logic low on this input selects the chip and enables CPU communication with the formatter/controller.																				
4	Read enable	RE	LSI RD L	A logic low on this input controls the placement of data from a selected register on the D7–D0 when CS is low.																				
5,6	Register select lines	A0, A1	CPU A0–A0 H	These inputs select the register to receive/transfer data on the D7–D0 lines under RE and WE control: <table><tr><td>A1</td><td>A0</td><td>RE</td><td>WE</td></tr><tr><td>0</td><td>0</td><td>Status reg</td><td>Command reg</td></tr><tr><td>0</td><td>1</td><td>Track reg</td><td>Track reg</td></tr><tr><td>1</td><td>0</td><td>Sector reg</td><td>Sector reg</td></tr><tr><td>1</td><td>1</td><td>Data reg</td><td>Data reg</td></tr></table>	A1	A0	RE	WE	0	0	Status reg	Command reg	0	1	Track reg	Track reg	1	0	Sector reg	Sector reg	1	1	Data reg	Data reg
A1	A0	RE	WE																					
0	0	Status reg	Command reg																					
0	1	Track reg	Track reg																					
1	0	Sector reg	Sector reg																					
1	1	Data reg	Data reg																					

Table 6-10 Formatter/Controller Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
7-14	Data access lines	DAL7-0	D7-D0 H	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by WE or transmitter enabled by RE.
24	Clock	CLK	CTL 1 MHz CLK	This input requires a free-running square-wave clock for internal timing reference, 1 MHz for drives.
31	Write data	WD	WDIN H	A 250 ns (MFM) pulse per flux transition. WD contains the unique address marks as well as data and clock.
32	Ready	READY	DREADY H	This input indicates disk readiness and is sampled for a logic high before a read or write operation is performed. If ready is low, the read or write operation is not performed and interrupt is generated. Type I operations are performed regardless of the state of ready. The ready input appears in inverted format as status register bit 7.
33	Write fault VFO enable	WF/VFOE	VFOE L	This is a bidirectional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled. (HLT = 1) VFOE will then go high until 8 bytes (MFM) before the address mark. It will then go active until the last bit of the second CRC byte of the data field. VFOE will remain low until the end of the data field.
34	Track 00	TR00	FTR00 L	This input informs the formatter/controller when the index hole is positioned over track 00.
35	Index pulse	IP	FIP L	This input informs the formatter/controller when the index hole is encountered on the diskette.

Table 6-10 Formatter/Controller Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
36	Write-protect	WPRT	FWPRT L	This input is sampled whenever a write command is received. A logic low terminates the command and sets the write-protect status bit.
37	Double-density	DDEN	DDEN L	This pin selects either single- or double-density operation. When DDEN = 0, double-density is selected. When DDEN = 1, single-density is selected.
38	Data request	DRQ	DRQ H	This open drain output indicates that the DR contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the CPU through reading or loading the DR in read or write operations, respectively.
39	Interrupt request	INTRQ	IRQ H	This open drain output is set at the completion of any command and is reset when the status register is written to.
Disk drive interface:				
15	Step	STEP	STEP L	The step output contains a pulse for each step.
16	Direction	DIRC	DIR L	Direction output is active high when the head is stepping in, active low when the head is stepping out.
17	Early	EARLY	EARLY	This indicates that the write data pulse occurring while early is active (high) should be shifted early for write precompensation.
18	Late	LATE	LATE	This indicates that the write data pulse occurring while late is active (high) should be shifted late for write precompensation.
22	Test	TEST	NOT USED	This input is used for testing purposes only and should be tied to +5 V or left open by the user unless interfacing to voice coil actuated motors. (It is not used by the VT18X control module.)

Table 6-10 Formatter/Controller Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
23	Head load timing	HLT	HLT H	When a logic high is found on the HLT input, the head is assumed to be engaged.
25	Read gate	RG	NOT USED	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization. (It is not used by the VT18X control module.)
26	Read clock	RCLK	RCLK H	A nominal square-wave clock signal derived from the data stream (raw data) is provided to this input from the PLL.
27	Raw read	RAW READ	RDD L	The data inputs signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	Head load	HLD	HLD L	The HLD output controls the loading of the read/write head against the media.
29	Track greater than 43	TG43	NOT USED	This output informs the drive that the read/write head is positioned between tracks 44–76. This output is valid only during read and write commands. (It is not used by the VT18X control module.)
30	Write gate	WG	WG H	This output is made valid before writing is to be performed on the diskette.

6.6.10.3 Phase-Locked Loop – The phase-locked loop (PLL) consists of a 20-pin IC (WD 1691) and an external voltage controlled oscillator (VCO). The PLL performs different functions during the writing and reading operation. During a write operation, the PLL receives the composite stream of data, clocks (WDIN H) from the formatter/controller, and sends it to the disk drive where it is recorded as flux transitions on the diskette. During a read operation, the composite stream of data and clocks (RAW DATA L) from the diskette are separated by the PLL into data pulses (RDD L) and clocks (RCLK H), and then input to the formatter/controller. The input/output signal functions of the WD 1691 are described in Table 6-11.

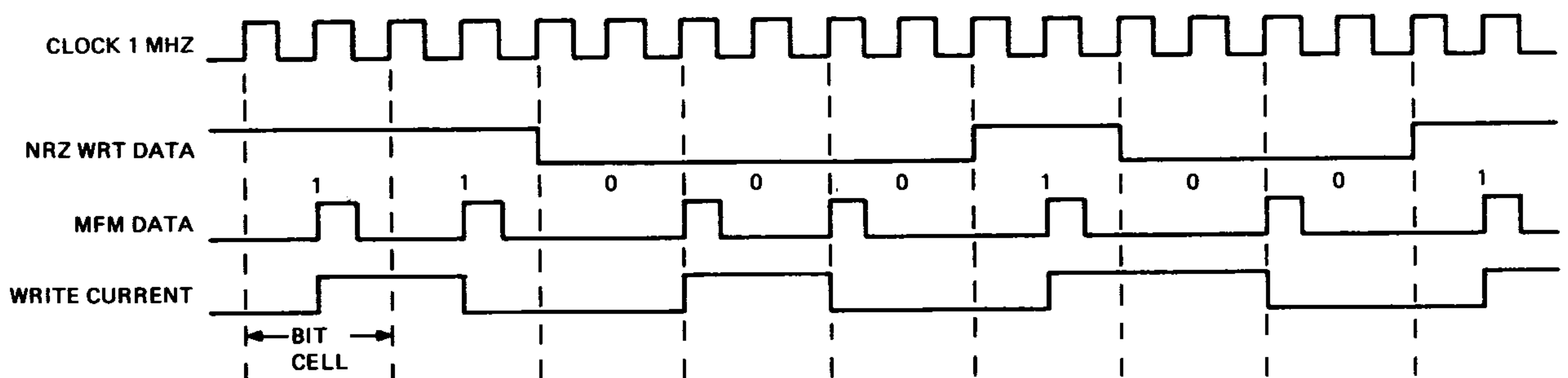
Table 6-11 WD 1691 Pin Identification

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
1	Write data input	WDIN	WDIN H	Ties directly to the formatter/controller WD pin and jumper W8. W8 is not installed for double-density operation.
2,3,4,19	Phase 2,3,1,4	02 03 01 04		4 phase inputs to generate a desired write precompensation delay. It is not used by the VT18X control module.
5	Strobe	STB		Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04. It is not used by the VT18X control module.
6	Write data output	WDOUT	WD H	Serial, precompensated write data stream to be sent to the disk drive's WRDOUT L line.
7	Write gate	WG	WG H	Write gate input from the formatter/controller.
8	VFO enable write fault	VFOE/WF	VFOE L	Input from the formatter/controller. Enables data recovery circuit in conjunction with WG H.
9	Track 43	TG43		Not used by the VT18X control module.
10	Vss	Vss	GND	Ground
11	Read data	RDD	RDD L	Composite clock and data stream input from the disk drive.
12	Read clock	RCLK	RCLK H	RCLK signal generated by the WD1691, connected to the formatter/controller.
13	Pump up	PU	PU H	Tristate output that will be forced high when the PLL requires an increase in VCO frequency.
14	Pump down	PD	PD L	Tristate output that will be forced low when the PLL requires a decrease in VCO frequency.

Table 6-11 WD 1691 Pin Identification (Cont)

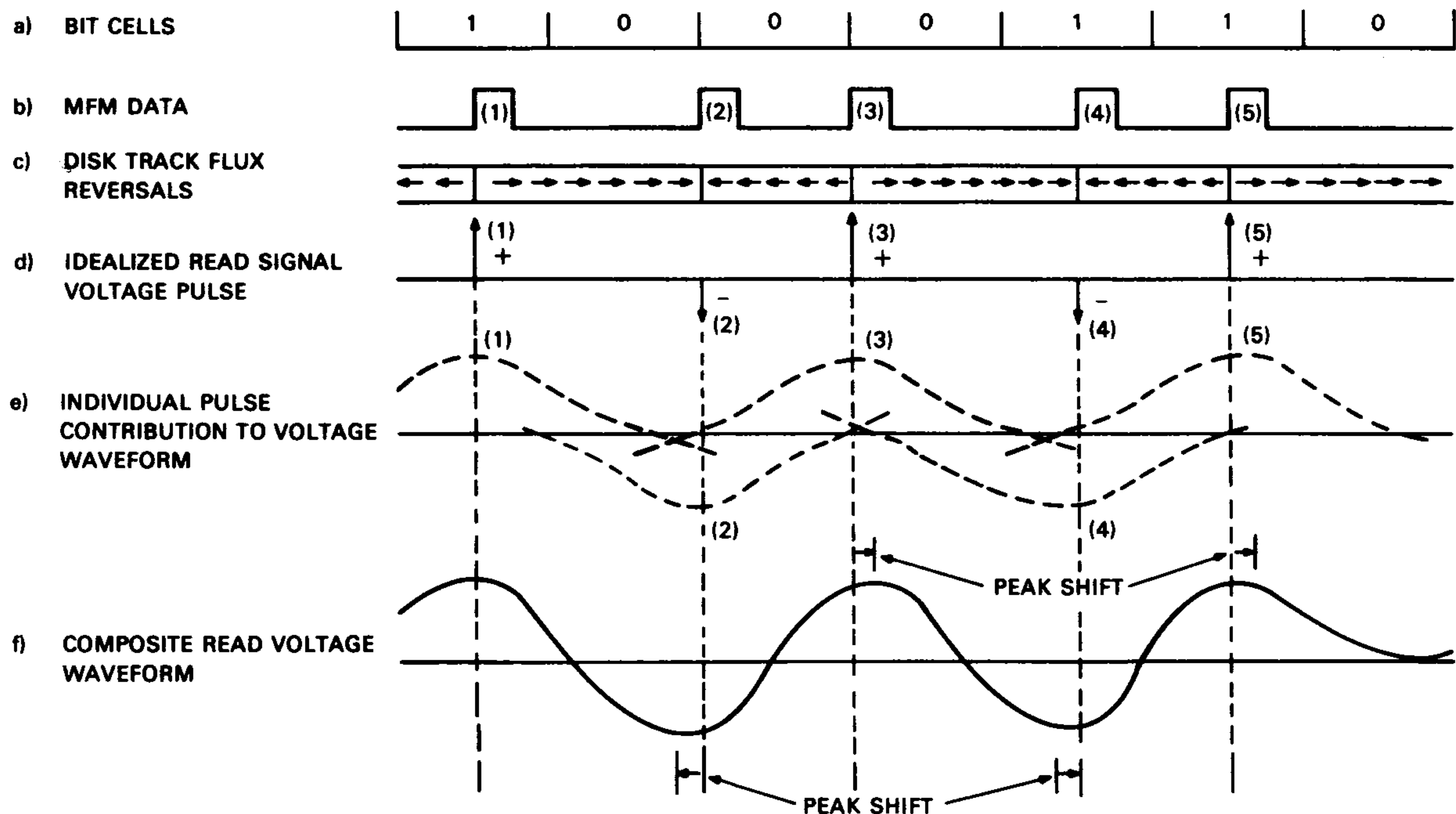
Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
15	Double-density enable	DDEN	DDEN L	Double-density select input. When DDEN is low, double-density is selected.
16	Voltage controlled oscillator	VCO	VCO	A nominal 2.0 MHz (5¼ inch drive) master clock input from VCO.
17, 18	Early late	EARLY LATE	EARLY LATE	Early and late signals from the formatter/controller used to determine write precompensation.
20	Vcc	Vcc	Q = 5 V	+5 V $\pm 10^\circ$ C power supply.

The MFM recording method produces an undesirable shifting of the peaks of adjacent flux transitions on the diskette so that they are moved from the position where they were written. Figure 6-30 shows binary data encoded into MFM format and Figure 6-31 shows how the diskette flux reversals shift the peaks of the composite read voltage waveform. The PLL includes a write precompensation circuit to shift the data in a direction opposite to that expected by the peak shift of the composite read voltage waveforms as a result of the MFM encoding. The write precompensation circuit uses the EARLY LATE and WDIN H signals from the formatter/controller in conjunction with the 1.0 MHz and 4.0 MHz clock signals to generate the pre-compensated MFM write data output (WRDOUT L).



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Figure 6-30 MFM Encoding



MR-5909

Figure 6-31 Peak Shift Waveform

During a read operation, a data separator circuit in the WD 1619 ensures the correct time relationship between the data (RDD L) and clock (RCLK H) signals when they are recovered from the composite data stream (RAW READ L) received from the disk drive. The data separator circuit uses four input signals (DDEN L, VCO, RDD L, and VFOE L) and produces three outputs: PU, PD, and RCLK. The data separator is enabled when the write gate (WG H) signal goes low and allows the VFOE signal from the formatter/controller to control a phase comparator in the PLL. VFOE goes low during a read operation after the head in the disk drive has loaded and settled. VFOE then goes high until eight bytes before the address mark. It then goes active until the last bit of the second CRC byte of the data field. VFOE remains low until the end of the data field.

When the RDD input to the WD 1691 goes low while VFOE and WG are low, the pump up (PU) and pump down (PD) signals become active. PU and PD are three-state output signals used to control the frequency of the VCO and therefore the frequency of RCLK H. The frequency of RCLK when DDEN equals zero (MFM operation) is the VCO frequency divided by eight. One half of the RCLK time period is used as a window for the read data. If the RDD line has made its transition in the beginning of the RCLK window, PU will go to a logic 1 state to request an increase in VCO frequency. If the RDD line has made its transition at the end of an RCLK window, PU will go to its high impedance state and PD will go to a logic zero requesting a decrease in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD remain three-stated, indicating that no adjustment of the VCO free-running frequency is needed. The VCO circuit includes a 50,000 ohm potentiometer, which is used to set the free-running frequency of the oscillator.

6.6.10.4 Disk Drive Controller Registers – The disk drive controller circuit includes two 8-bit registers (Figure 6-29), a diagnostic register, and a general control and status register. The diagnostic register is a read-only register that receives inputs from the disk drive interface connector (J2) and sends outputs to the data bus (DB7–DB0). The inputs provide the CPU with information on the current status of controller functionality during diagnostic testing. The contents of the diagnostic register may be obtained by performing a read to address A0 L.

The general control and status register holds various control and status information for the disk drive as well as the VT18X control module. The lower 4-bits of the register are read/write and can be accessed by a read or write to address 80H. The upper four bits of the register are read-only and are accessed by performing a read to address 80H.

6.6.10.5 Disk Drive Controller Latches – Two data latches are used by the disk drive controller to store control and status information. The write data bit latch is a D-type FF that is set whenever write data is sent to the disk drive. The output of the write data bit latch is sent to the diagnostic read register as bit 4 and is used during diagnostic testing to determine if data is being written out to the disk drive. The write data out bit is reset by a read to address 90H.

The control and status latch is a 4-bit latch used to store the disk select signals (DS1–DS0), the MOTOR ON H bit, and the double-density enable (DDEN) bit. These bits are obtained from DB3–DB0 and are stored in the latch by performing a write to address 80H. DDEN is sent to the disk drive formatter/controller, the PLL, and the general control and status register. MOTOR ON H is sent to the general control and status register, the diagnostic read register, the formatter/controller, and the disk drive via pin 16 of connector J2. DS1 and DS0 are sent to the general control and status register and are used to inform the CPU of the disk drive currently selected. DS1 and DS0 are also sent to the drive select decoder to select one of four drives depending on the binary combination of bits 1–0 stored in the control and status latch. The drive select signals (DRIVE 3 L–DRIVE 0 L) are sent to the disk drives via connector J2 to enable the read/write logic of the selected drive.

6.6.10.6 Disk Drive Interface Connector – The control and data lines for interfacing the disk drive controller to the disk drives are routed to a 37-pin, D-type connector (J2) on the VT18X control module. The control and data lines and the pins to which they are connected are listed in Table 6-12.

Table 6-12 Disk Drive Interface Connector Signals

Pin Number	Signal	Mnemonic	Direction	Function
6	Select 3	Drive 3 L	Out	This signal initiates a head load on drive 3 when it goes low.
8	Index	IP L	In	This signal is obtained each time the disk drive senses the index hole in the diskette. The signal indicates the start of a diskette track.
10	Select 0	Drive 0 L	Out	This signal initiates a head load on drive 0 when it goes low.
12	Select 1	Drive 1 L	Out	This signal initiates a head load on drive 1 when it goes low.
14	Select 2	Drive 2 L	Out	This signal initiates a head load on drive 2 when it goes low.
16	Motor on	MOTOR ON L	Out	This signal turns on the drive motor when it goes low.

Table 6-12 Disk Drive Interface Connector Signals (Cont)

Pin Number	Signal	Mnemonic	Direction	Function
18	Direction	DIR H	Out	When a logical 1 is present on this line, the read/write head will move away from the center of the disk when a pulse is applied to the step line. When this line is a logical low, a step pulse will move the read/write head to the center of the disk.
20	Step	STEP H	Out	When this line is pulsed low, the read/write head will move in the direction defined by the direction line.
22	Write data	WRDOUT L	Out	This signal is the data to be written on the diskette. Each transition from a logical 1 to a logical 0 causes the read/write head current to be reversed, thereby writing a data bit. This line is enabled when write gate is active.
24	Write gate	WRITE GATE L	Out	When this line is a logical 0, write data can be written on the diskette.
26	Track 00	TRACK 00 L	In	When this signal is low, it indicates that the read/write head is positioned at track zero (outermost track).
28	Write-protect	WPRT L	In	When this signal is low, it indicates that a write-protected diskette is installed in the drive.
30	Read data	RAW DATA L	In	This signal input is the composite clock and data stream from the disk drive.
34	Drive ready	READY L	In	This optional signal input from the disk drive is not used, and it is tied to a pull-up resistor. The READY L signal is grounded internally on the VT18X control module by jumper W6.

NOTE: Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, and 33 are connected to ground. Pin 32 is reserved.

6.6.11 VT18X Control Module Input/Output Addresses

Data or control and status information is read from or loaded (written) into the various data, control and status, and diagnostic read/write registers in the VT18X control module by the CPU under software control. These registers are read or loaded by the program using instructions referring to a particular register address. Table 6-13 lists the I/O addresses and the registers they access. The format and bit functions of the various registers are described in detail in the following paragraphs.

Table 6-13 VT18X Control Module I/O Addresses

Address	Register
40H	Console port data register
41H	Console port control/status register
48H	Printer port data register
49H	Printer port control/status register
50H	General port data register
51H	General port control/status register
58H	Communications port data register
59H	Communications port control/status register
78H	Disk drive controller control/status register WO/RO
79H	Disk drive controller track register R/W
7AH	Disk drive controller sector register R/W
7BH	Disk drive controller data register R/W
80H	General disk drive control/status register R/W
88H	Communications status register RO
90H	Communications control/ baud rate select register WO
90H	Real time clock interrupt reset register RO
98H	Diagnostic write register WO
AOH	Diagnostic read register RO

6.6.12 Communications Data and Control and Status Registers

The four communications ports use 8251A programmable communications interfaces and should be programmed alike. Prior to starting data transmission or reception, the PUSART must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the PUSART and must immediately follow a reset operation. The control words are split into two formats: a mode instruction and a command instruction. The mode instruction can be programmed in either a synchronous or asynchronous format. The asynchronous mode instruction can be used by all of the I/O ports, but synchronous mode can only be used by the communications port control and status register (59H).

The PUSARTs are programmed as follows; first, the control and status registers 41H, 49H, 51H, and 59H must be programmed with the synchronous or asynchronous mode byte. Then, the same register must be written with a command byte. A read of those locations reveals the current status of that PUSART. The PUSART data registers (40H, 48H, 50H, and 58H) hold the 8-bit data byte to be transmitted or received. The formats and bit definitions for the data and control and status registers are described in the following paragraphs.

6.6.12.1 Asynchronous Mode Instruction Format (41H, 49H, 51H, 59H) WO – Whenever a data character is transmitted by the CPU in the synchronous mode, the PUSART automatically adds a start and the programmed number of stop bits to each character. Also, an odd or even parity bit is inserted prior to the stop bit(s) as defined by the mode instruction.

Whenever a character is received in the asynchronous mode, the PUSART checks the validity of the start, data, parity, and stop bits. If an error has not been detected, PUSART strips the start, parity, and stop bits and then loads the data character into the parallel I/O buffer of the PUSART. The asynchronous mode instruction format is shown in Figure 6-32. Table 6-14 describes the bits.

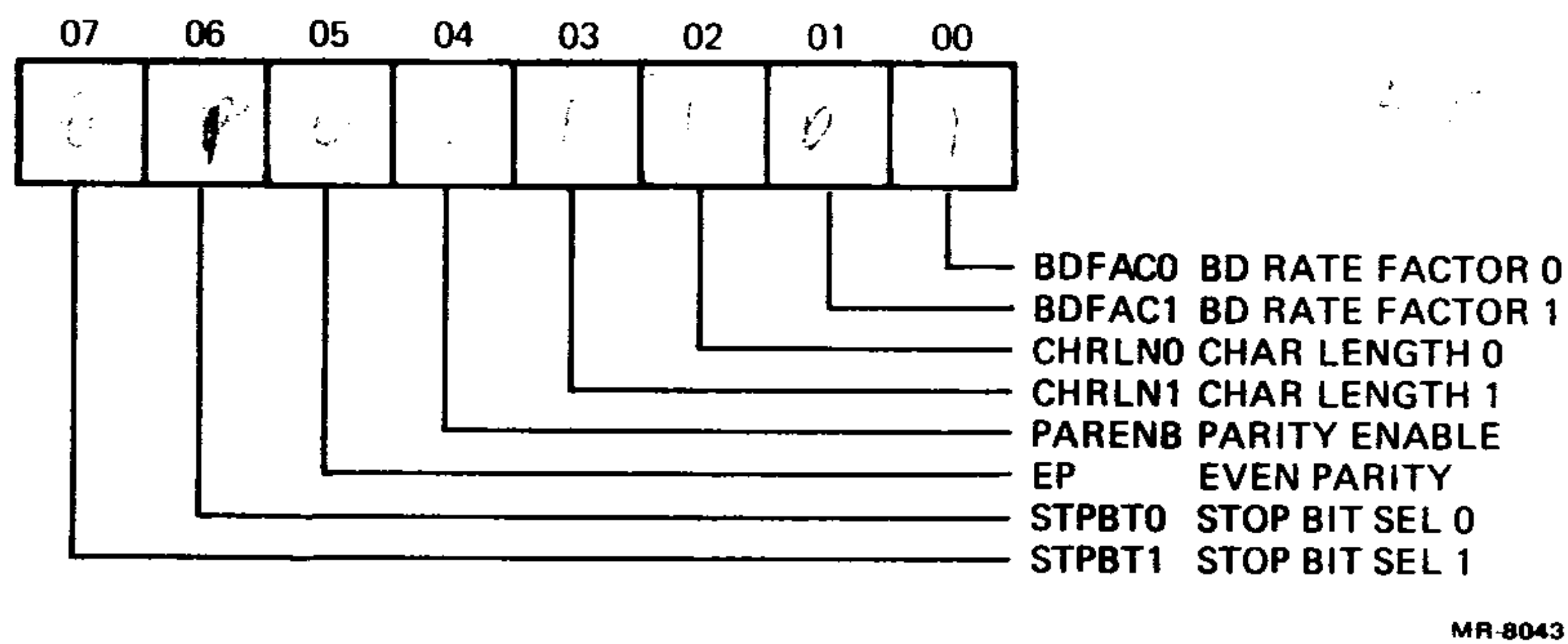


Figure 6-32 Mode Instruction Format, Asynchronous (41H, 49H, 51H, 59H) WO

Table 6-14 Asynchronous Mode Instruction Bit Description

Bits	Name	Description															
0, 1	Baud rate factor select	These bits hold the encoded value of the bits to be selected. <table> <tr> <th>Bit 1</th><th>Bit 0</th><th>Mode Selected</th></tr> <tr> <td>0</td><td>0</td><td>Synchronous mode</td></tr> <tr> <td>0</td><td>1</td><td>1 × clock</td></tr> <tr> <td>1</td><td>0</td><td>16 × clock</td></tr> <tr> <td>1</td><td>1</td><td>64 × clock</td></tr> </table>	Bit 1	Bit 0	Mode Selected	0	0	Synchronous mode	0	1	1 × clock	1	0	16 × clock	1	1	64 × clock
Bit 1	Bit 0	Mode Selected															
0	0	Synchronous mode															
0	1	1 × clock															
1	0	16 × clock															
1	1	64 × clock															
2, 3	Character length select	These bits hold the encoded value of the character length to be selected. <table> <tr> <th>Bit 3</th><th>Bit 2</th><th>Character Length</th></tr> <tr> <td>0</td><td>0</td><td>5 bits</td></tr> <tr> <td>0</td><td>1</td><td>6 bits</td></tr> <tr> <td>1</td><td>0</td><td>7 bits</td></tr> <tr> <td>1</td><td>1</td><td>8 bits</td></tr> </table>	Bit 3	Bit 2	Character Length	0	0	5 bits	0	1	6 bits	1	0	7 bits	1	1	8 bits
Bit 3	Bit 2	Character Length															
0	0	5 bits															
0	1	6 bits															
1	0	7 bits															
1	1	8 bits															
4	Parity enable	When set, this bit enables parity. When clear, no parity is used.															
5	Even parity generation/check	When set, this bit enables an even mode of parity and when clear, odd parity is enabled.															
6, 7	Number of stop bits	These bits hold the encoded value of the number of stop bits that are used. <table> <tr> <th>Bit 7</th><th>Bit 6</th><th>Stop Bits</th></tr> <tr> <td>0</td><td>0</td><td>Invalid</td></tr> <tr> <td>0</td><td>1</td><td>1 bit</td></tr> <tr> <td>1</td><td>0</td><td>1½ bits</td></tr> <tr> <td>1</td><td>1</td><td>2 bits</td></tr> </table>	Bit 7	Bit 6	Stop Bits	0	0	Invalid	0	1	1 bit	1	0	1½ bits	1	1	2 bits
Bit 7	Bit 6	Stop Bits															
0	0	Invalid															
0	1	1 bit															
1	0	1½ bits															
1	1	2 bits															

6.6.12.2 Synchronous Mode Instruction Format (59H) WO – The communications port is the only port that may be programmed to operate in the synchronous mode. In the synchronous mode, the PUSART can be programmed to transmit one or two sync characters followed by a stream of data characters. When the PUSART receives data in the asynchronous mode, character synchronization can be internally or externally achieved. The synchronous mode instruction format is shown in Figure 6-33. Table 6-15 describes the bits.

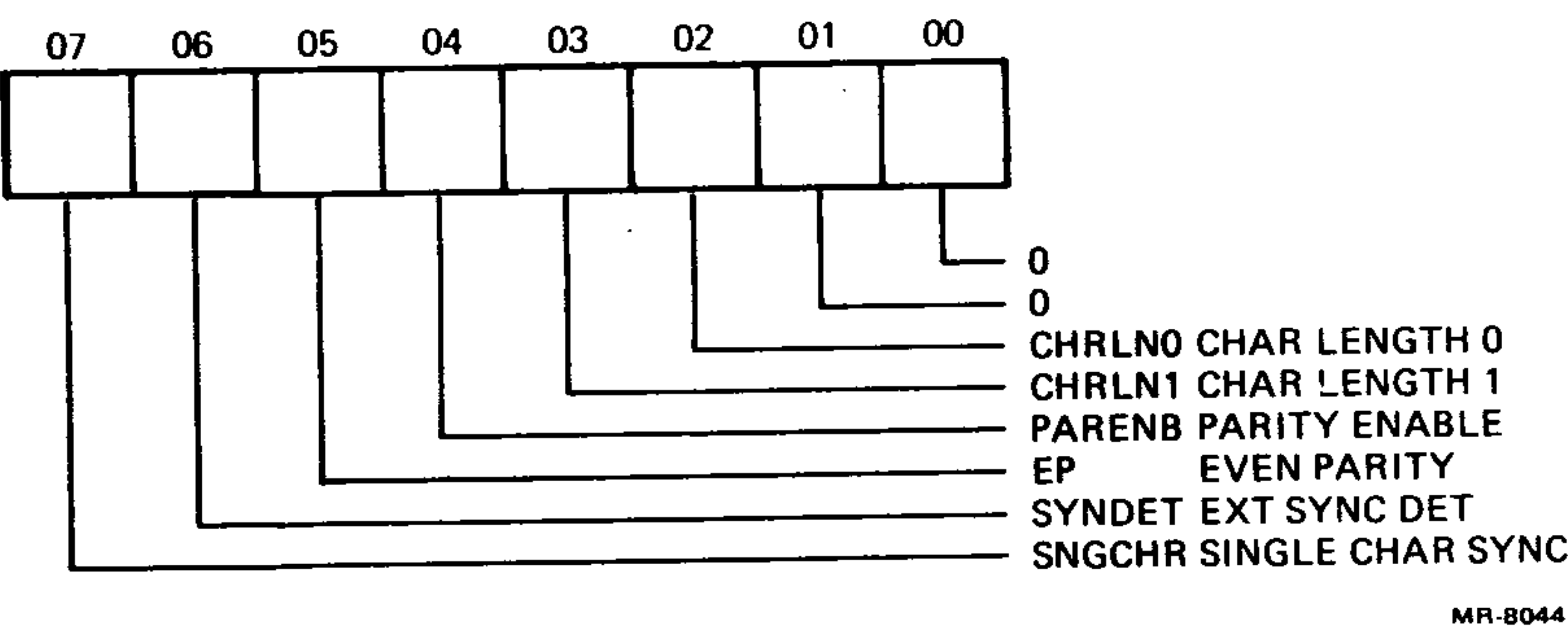


Figure 6-33 Mode Instruction Format, Synchronous (59H) WO

Table 6-15 Synchronous Mode Instruction Bit Description

Bits	Name	Description
0, 1		Always 0.
2, 3	Character length select	These bits hold the encoded value of the character length to be selected. Bit 3 Bit 2 Character Length 005 bits 016 bits 107 bits 118 bits
4	Parity enable	When set, this bit enables parity. When clear, no parity is used.
5	Even parity generation/check	When set, this bit enables an even mode of parity and when clear, odd parity is enabled.
6	External sync detect	When set, the PUSART is in external sync detect mode and character synchronization is achieved by an external input. When clear, the PUSART is in internal sync mode and will output a sync detect pulse to indicate that it has located the sync character in receive mode.
7	Single character sync	When set, single sync character mode is selected. When clear, double sync character mode is selected.

6.6.12.3 Command Instruction Registers (41H, 49H, 51H, 59H) WO – Once the mode has been set in the 8251, a command has to be issued. This is done by issuing a command to the same location that the mode instruction was programmed into. The command instruction format is shown in Figure 6-34. Table 6-16 describes the bits.

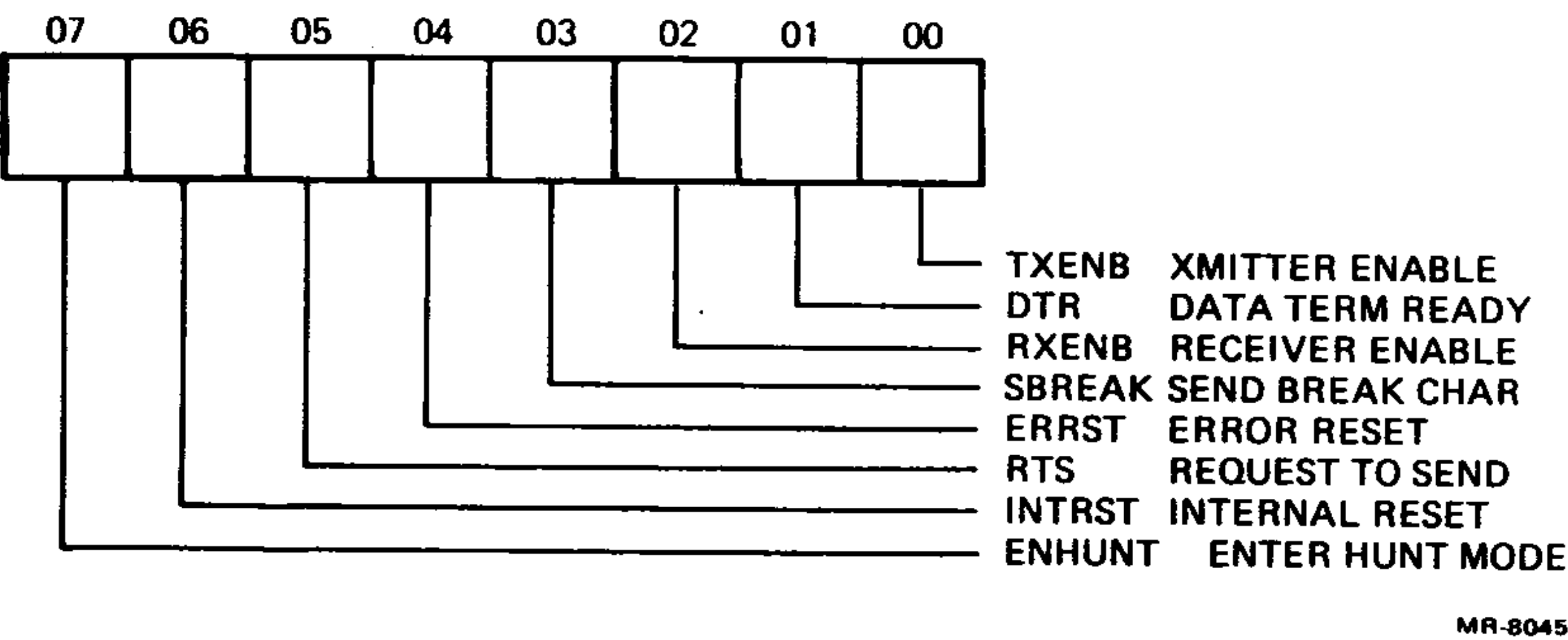


Figure 6-34 Command Instruction Format (41H, 49H, 51H, 59H) WO

Table 6-16 Command Instruction Bit Description

Bits	Name	Description
0	Transmitter enable	This bit must be set to enable the transmitter function.
1	Data terminal ready	This is a general purpose control bit that can be used for anything but is usually used to signify DTR. A one written to this register forces the DIR output pin to a zero.
2	Receiver enable	This bit must be set to enable the receiver function.
3	Send break character	A one written to this bit forces the TXD output pin low.
4	Error reset	Writing a one to this bit results in the parity error, overrun error, and framing error status bits being reset.
5	Request to send	This is a general purpose control bit that can be used for anything but is usually used to signify RTS. A one written to this register forces the RTS output pin to a zero.
6	Internal reset	A high on this bit internally resets the 8251A and returns it to mode instruction format.
7	Enter hunt mode	A one enables a search for sync characters in the data stream.

6.6.12.4 Status Read Registers (41H, 49H, 51H, 59H) RO – This register holds the status of the 8251A's operation. Note that the status may not be valid for 14 microseconds after the actual event occurred. The status read register format is shown in Figure 6-35. Table 6-17 describes the bits.

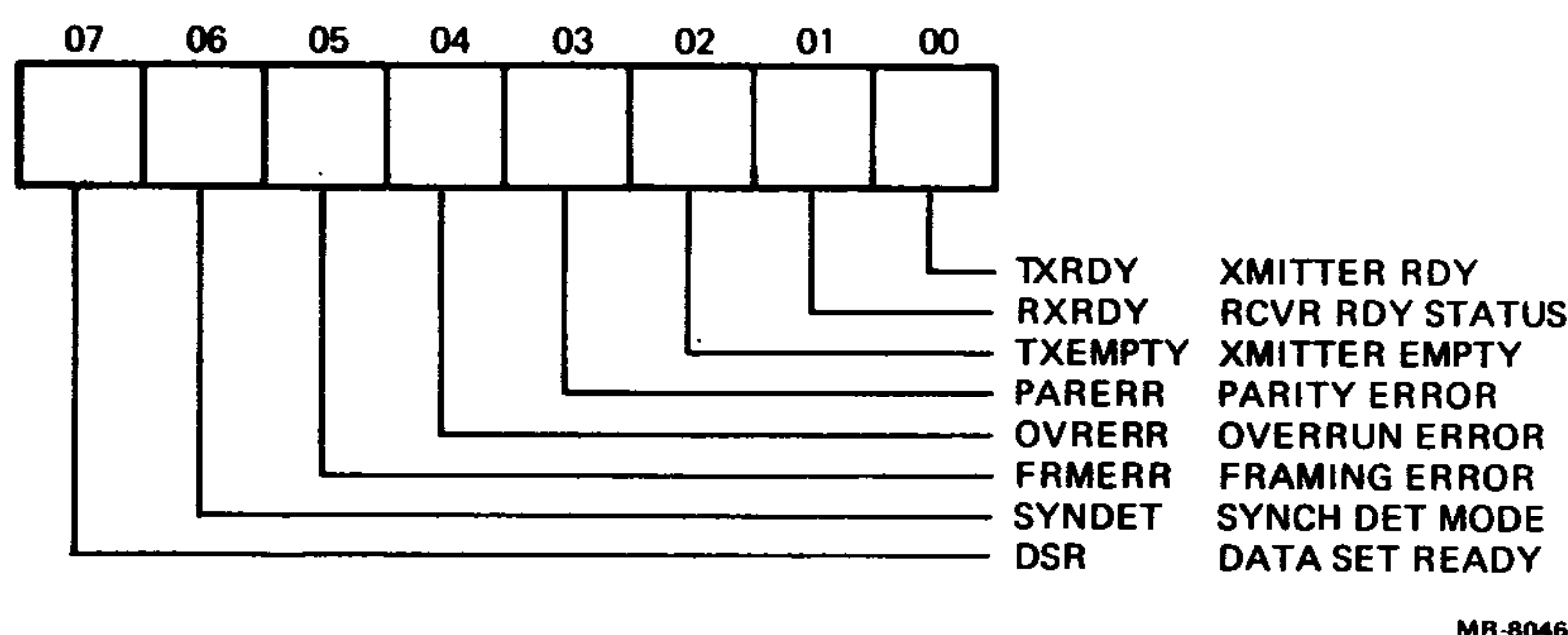


Figure 6-35 Status Read Format (41H, 49H, 51H, 59H) RO

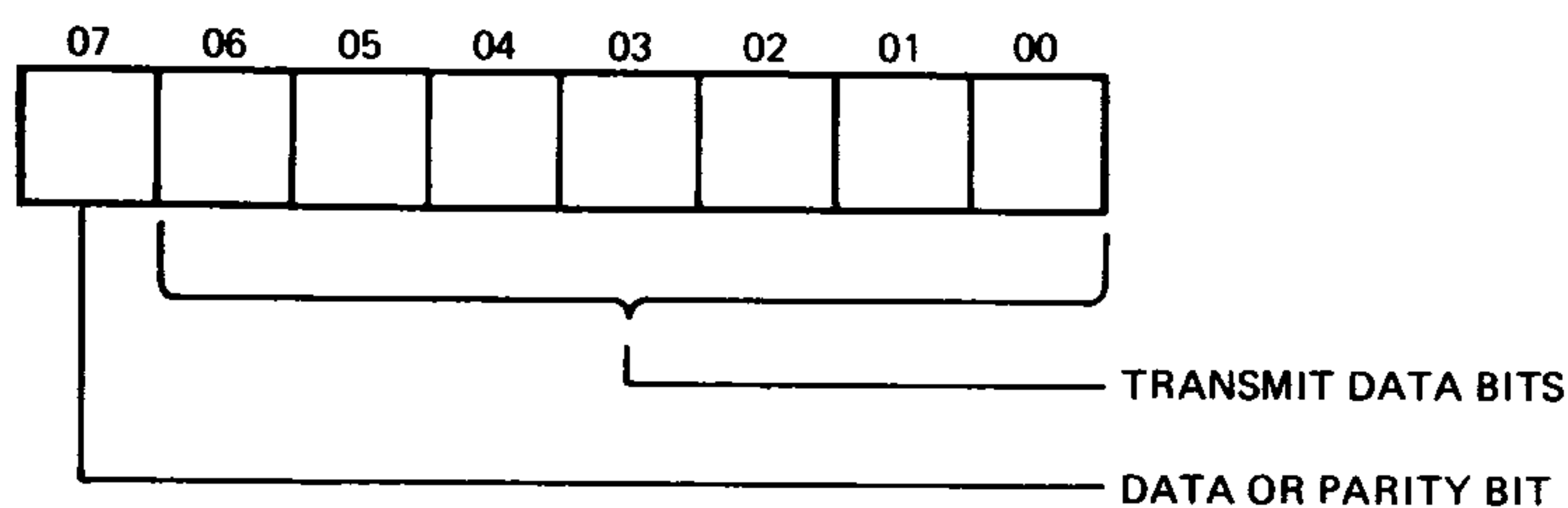
Table 6-17 Status Read Register Bit Description

Bits	Name	Description
0	Transmitter ready status	This bit has a different meaning than the TXRDY pin on the 8251A. The status bit is not conditioned by CTS and TXENB while the TWRDY pin is conditioned by these signals.
1	Received ready	This bit corresponds with the output pin of the same name. When set, it means that the receive data buffer is full and the CPU must read it. This is the bit that is wire ORed from the 8251As to create a restart (16 H) of the Z80A.
2	Transmitter empty status	This bit also has a corresponding I/O pin with the same meaning. When set, it indicates that the transmitter data buffer is empty and waiting for service.
3	Parity error status	This flag is set when a parity error is detected. It is reset through the error reset bit in the command registers. When set, this bit does not inhibit the operation of the 8251A.
4	Overflow error status	The overflow error status bit is set when the CPU does not read a character from the receive data buffer before the next one comes along. It is also reset by the error reset bit in the command registers. In the case of an overflow, the character is lost and the 8251A continues operation.

Table 6-17 Status Read Register Bit Description (Cont)

Bits	Name	Description
5	Framing error status (asynchronous only)	The framing error status bit is set when a valid stop bit is now detected at the end of every character. It is reset by the error reset bit in the command register of the 8251A. This flag does not inhibit the operation of the 8251A.
6	Sync detect status	This bit is used for synchronous mode for SYNDET and may be used as either input or output. It is programmable through the command register. It is reset to output mode low upon a reset. When used as an output, the SYNDET pin will go high to indicate that the 8251A has located the sync character in receive mode. While in bi-sync mode, the SYNDET line will go high in the middle of the last bit of the second sync character. SYNDET is automatically reset when a status read operation occurs.
7	Data set ready status	When set, this bit indicates that the DSR pin is low.

6.6.12.5 Transit Data Buffer Register (40H, 48H, 50H, 58H) WO – This is a write-only, 8-bit register that holds the data to be transmitted from the 8251A. The transmit data format is shown in Figure 6-36. Table 6-18 describes the bits.



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Figure 6-36 Transmit Data Format (40H, 48H, 50H, 58H) WO

Table 6-18 Transmit Data and Received Data Bit Description

Bits	Name	Description
7:0	Transmit data	Bit 0 is the least significant bit and bit 7 is the most significant bit. If seven data bits plus parity are selected, bit 8 is the parity bit. If character length is defined as 5, 6, or 7 bits, the unused bits are set to zero.
7:0	Received data	Bit 0 is the least significant bit and bit 7 is the most significant. If character length is defined as 5, 6, or 7 bits, the unused bits will be zero.

6.6.12.6 Received Data Buffer Register (40H, 48H, 50H, 58H) RO – This read-only, 8-bit register contains the received character after the receiver ready (RXRDY) bit becomes asserted. The received data format is shown in Figure 6-37. Table 6-18 describes the bits.

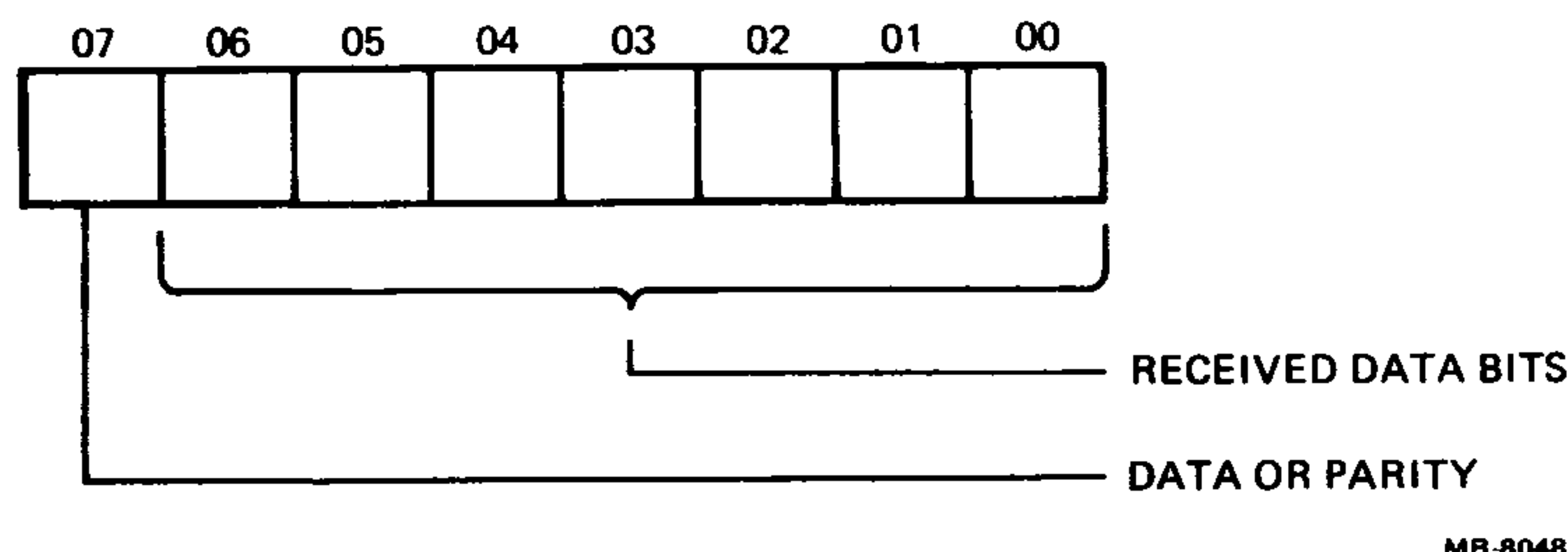


Figure 6-37 Received Data Format (40H, 48H, 50H, 58H) RO

6.6.13 Disk Drive Controller Registers

The disk drive controller contains four 8-bit registers that define and execute the programmed controller functions. These registers (command/status, track, sector, and data) are physically located in the disk drive formatter/controller IC (WD 1793) and are described in Paragraphs 6.6.13.1 through 6.6.13.5.

6.6.13.1 Command Register (Write-Only) – This 8-bit register at address 78H is used as a write-only register when it is loaded by the program with the command that is to be executed by the drive. Table 6-19 summarizes the command types that are written into this register.

NOTE

When bits are defined to be 1s or 0s (as in Table 6-19) they should not be changed in the specific commands.

Table 6-19 Disk Drive Controller Commands

Command Type	Command	Bits							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	v	r1	r0
I	Seek	0	0	0	1	h	v	r1	r0
I	Step	0	0	1	u	h	v	r1	r0
I	Step in	0	1	0	u	h	v	r1	r0
I	Step out	0	1	0	u	h	v	r1	r0
II	Read sector	1	0	0	m	0	e	0	0
II	Write sector	1	0	0	m	0	e	0	a0
III	Read address	1	1	1	0	0	e	0	0
III	Read track	1	1	1	0	0	e	0	0
IV	Force interrupt	1	1	0	1	I3	I2	I1	I0

Table 6-20 shows the delay that must be observed between operations of registers. Tables 6-21 and 6-22 show type I command bit descriptions and flags. Tables 6-23, 6-24, and 6-25 show type II command and type III command bit descriptions and flags.

Table 6-20 Required Delays

Operation	Next Operation	Delay Required (MFM)
Write to command register	Ready busy bit (Status bit 0)	12 μ s
Write to command register	Read status bits 1–7	23 μ s
Write to any register	Read from different register	0
Write to track, sector or data register	Read from same register	8 μ s
Write to any register	Write to another register	14 μ s
Interrupt request	Read status register	4 μ s

Table 6-21 Type I Command Bit Description

Bits	Name	Description
0, 1	Stepping rate (r1, r0)	These bits control the rate at which the stepping pulses are sent to the disk drive. See Table 6-22 for stepping rate breakdown.
2	Track verify (v)	This bit determines if there is a verification operation to take place on the destination track. During verification the head is loaded, and after a 30 ms delay, the HLT input is sampled. After a 1.0 second motor start-up time, the HLT input becomes active. When HLT is set, the first ID field is read off the diskette. The track address of the ID field is compared to the track register. If there is a match and a valid ID CRC, the verification is complete and an interrupt is generated. If not valid, the seek error status is set.
3	Head load flag (h)	This bit determines if the head is to be loaded at the beginning of a command. If the head is loaded, then the head remains loaded until either the formatter/controller receives a command that specifically disengages the head or 15 revolutions of the diskette have passed with the busy bit equal to 0.
4	Update (step commands) (u)	When set (1), the track register is updated for each step; otherwise the track register is not affected.
5-7		Determine the command to be executed.

Table 6-22 Type I Command Flags

Flag	Name	Function															
h	Head load flag (bit 3)	h = 1, Load head at beginning h = 0, Unload head at beginning															
v	Verify flag (bit 2)	v = 1, Verify on destination track v = 0, No verify															
r1, r0	Stepping motor rate (bits 1-0)	<table> <tr> <td>r1</td><td>r0</td><td></td></tr> <tr> <td>0</td><td>0</td><td>6 ms</td></tr> <tr> <td>0</td><td>1</td><td>12 ms</td></tr> <tr> <td>1</td><td>0</td><td>20 ms</td></tr> <tr> <td>1</td><td>1</td><td>30 ms</td></tr> </table>	r1	r0		0	0	6 ms	0	1	12 ms	1	0	20 ms	1	1	30 ms
r1	r0																
0	0	6 ms															
0	1	12 ms															
1	0	20 ms															
1	1	30 ms															
u	Update flag (bit 4)	u = 1, Update track register u = 0, No update															

Table 6-23 Type II Command Bit Description

Bit	Name	Description
0	Data address mark	When set upon a write sector command, this bit defines a data mark (OFBH) to be written on the diskette. If the bit is not set, then a deleted data mark (OF8H) is written onto the diskette. When writing valid data on the diskette, this bit should be set.
1		Always 0.
2	30 millisecond delay	When set during a command, there is a 30 ms delay before reading begins. For maximum controller throughput, this bit should be 0. It should be set if the last command was a seek or new drive select. (See Table 6-25.)
3		Always 0.
4	Multiple sector	When set, this bit allows multiple sectors to be transferred.
5-7		Determine the command to be executed.

Table 6-24 Type III Command Bit Description

Bits	Description
0, 1	Always set to 0.
2	Same as bit 2 for type II commands. (See Table 6-25.)
3-7	Determine the command to be executed.

Table 6-25 Type II and III Command Flags

Flag	Name	Function
m	Multiple record flag (bit 4)	m = 0, Single record m = 1, Multiple records
a0	Data address mark (bit 0)	a0 = 0, 373° (data mark) a0 = 1, 370° (deleted data mark)
e	30 ms delay (bit 2)	e = 1, 30 ms delay e = 0, No delay

Type IV Command Bit Description

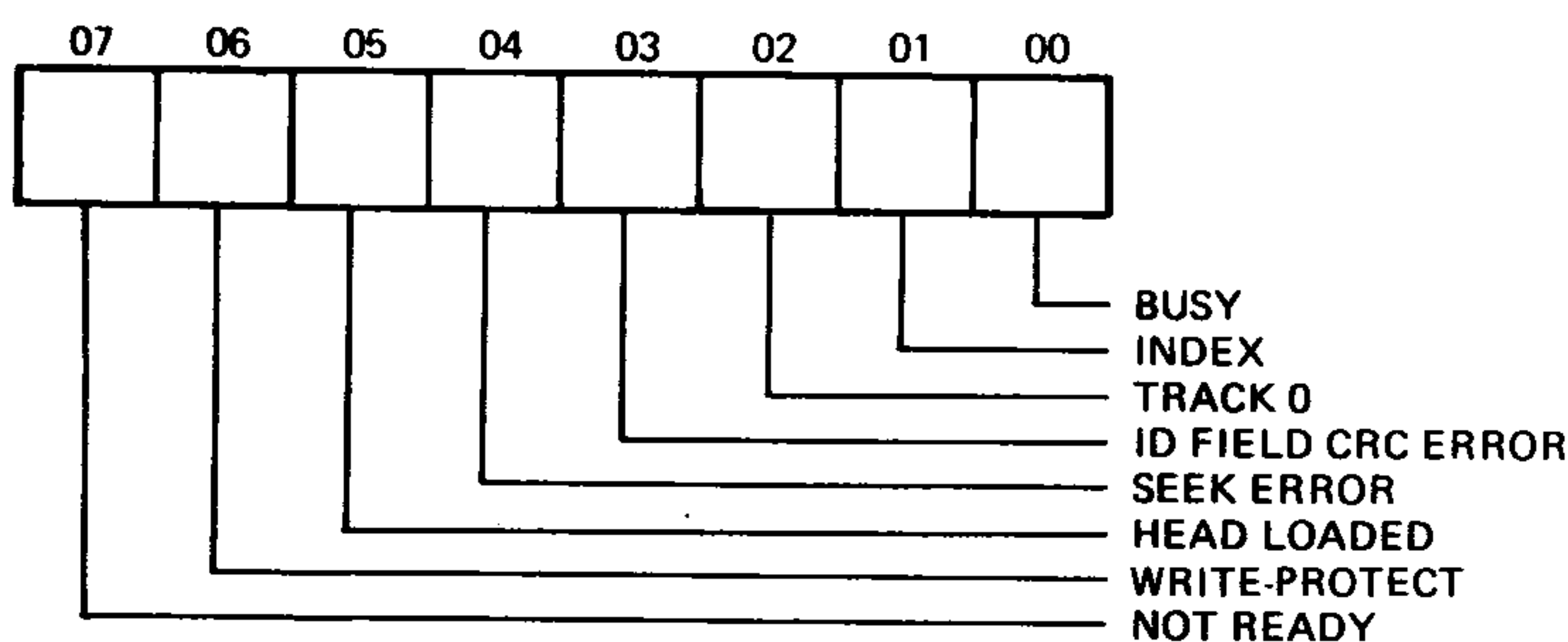
This command can be loaded into the register at any time. If there is a current command under execution, the command is terminated. See Table 6-26 for a description of conditions that terminate the command.

Table 6-26 Type IV Command Flags

Flag	Name	Function*
I0	Interrupt condition flag 0	I0 = 1, Not ready-to-ready transition
I1	Interrupt condition flag 1	I1 = 1, Ready-to-not ready transition
I2	Interrupt condition flag 2	I2 = 1, Index pulse
I3	Interrupt condition flag 3	I3 = 1, Immediate interrupt

*I3-I0 = 0, terminate with no interrupt.

6.6.13.2 Status Register (Read-Only) – This read-only register also resides at the same address (78H) as the command register. It contains the 8-bit status resulting from the completion of a command. The definition of the status bits varies according to the type of command executed. The format of the status register and bit definitions for all type I and type II (read and write sector) commands is shown in Figures 6-38, 6-39, and 6-40. Tables 6-27, 6-28, and 6-29 describe the bits.

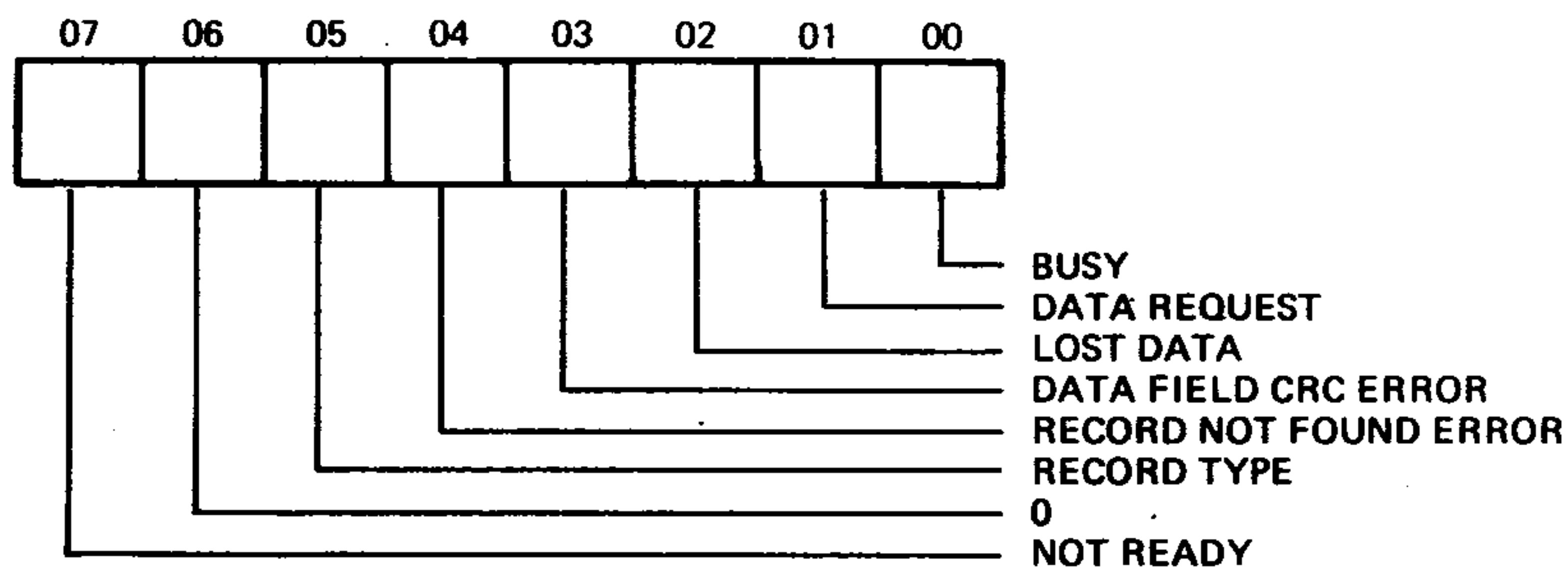


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Figure 6-38 Type I Status Register Format

Table 6-27 Type I Status Register Bit Description

Bits	Name	Description
0	Busy	When this bit is set (1), the formatter/controller is currently executing a command. Only a type IV command can be issued when this condition exists.
1	Index	When this bit is set (1), the index pulse is currently occurring.
2	Track 0	When this bit is set (1), the read/write head is currently positioned at track 0.
3	ID field CRC error	When set, this means that there was a CRC error of the ID field.
4	Seek error	When set, a seek error was encountered meaning that the destination track address was not found.
5	Head loaded	This bit reflects the current status of the head. When set, the head is loaded and the HLD output is asserted.
6	Write-protect	When set, the bit means that the current diskette is write-protected. An attempt to write a sector sets the interrupt flag.
7	Not ready	When set, the bit indicates that the disk drive is not ready. This could mean that the disk drive is not up to speed, the diskette is in upside down, or the door is open. This bit must be clear before any commands are issued to the formatter/controller.

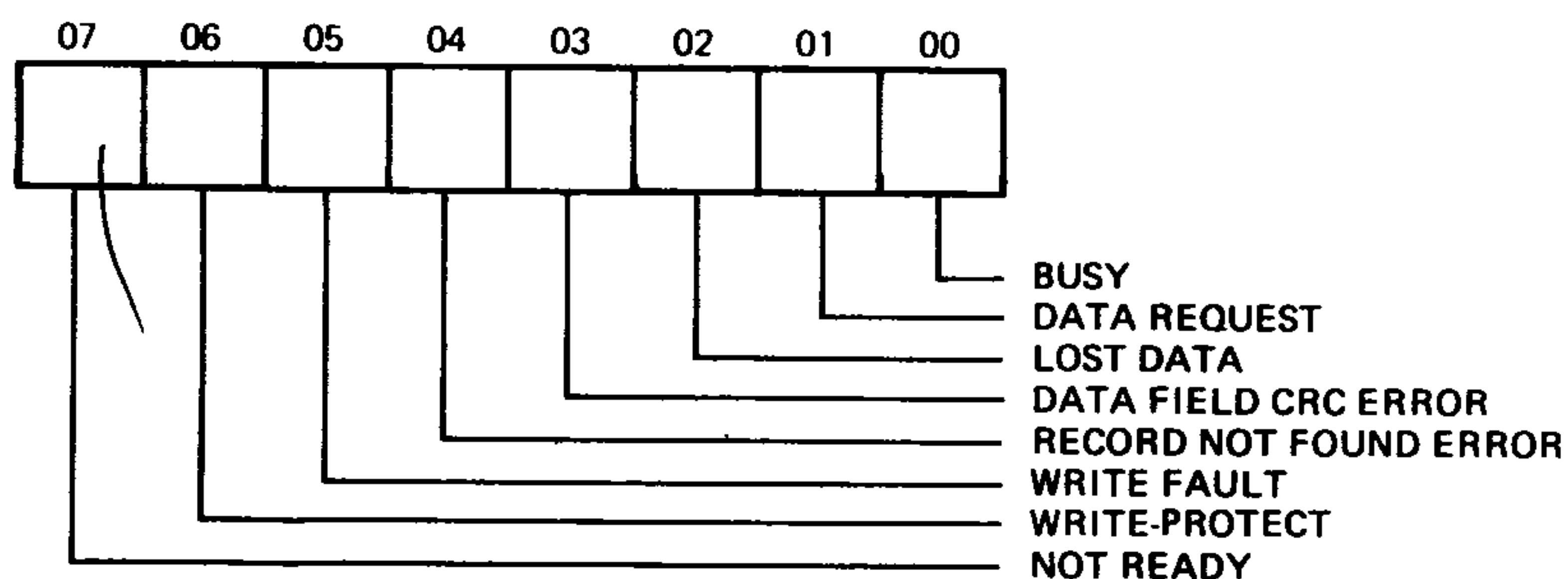


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Figure 6-39 Type II Read Sector Status Register Format

Table 6-28 Type II Read Sector Status Register Bit Description

Bits	Name	Description
0	Busy	Same as type I status.
1	Data request	When set, this bit means that the data register is full and is waiting for the CPU to read the register.
2	Lost data	When set, this bit means that the data register had not been serviced within 27.5 microseconds and the data in the data register is not valid.
3	Data field CRC error	When set, this bit indicates that the CRC of the read data field does not check with the data CRC that was written on the diskette.
4	Record not found error	When set, this bit means that a data address mark was not found within 43 bytes of the last ID field CRC byte.
5	Record type	This bit reflects the type of data mark that was encountered during the read. When set, a deleted data mark was found. If clear, a data mark was encountered.
6		Always set to 0.
7	Not ready	Same as type I not ready status bit.



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Figure 6-40 Type II Write Sector Status Register Format

Table 6-29 Type II Write Sector Status Register Bit Description

Bits	Name	Description
0	Busy	Same as type I status busy bit.
1	Data request	When set, this bit means that the data register is empty, and it is waiting for the CPU to write the register.
2	Lost data	When set, this bit means that data register had not been written within 23.5 μ s and the data on the diskette is not valid (zero bytes are substituted for data lost).
3	Data field CRC error	When set, this bit indicates that the CRC of the data that was written does not check with the data CRC that was written on the diskette.
4	Record not found error	When set, this bit means that a data address mark was not found within 43 bytes of the last ID field CRC byte.
5	Write fault	When this bit is set it indicates that there is a fault with the drive's write electronics.
6	Write-protect	When this bit is set after a write command, an attempt was made to write on a write-protected disk.
7	Not ready	Same as type I not ready status bit.

6.6.13.3 Track Register (Read/Write) – This R/W 8-bit register holds the updated address (00 H–39 H) of the current read/write head. It is incremented by one every time the head is stepped toward the spindle and decremented by one every time the head is stepped away from the spindle. The contents of the register are compared with the recorded track number in the ID field during diskette read, write, and verify operations. The track register address is 79H.

6.6.13.4 Sector Register (Read/Write) – This read/write 8-bit register holds the address (01 H–09 H) of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during diskette read and write operations. The sector register address is 7AH.

6.6.13.5 Data Register (Read/Write) – For a seek operation, this 8-bit read/write register holds the address of the desired track position. During data transfers, this register is the data buffer for the diskette. The data register address is 7BH.

6.6.14 Disk Drive Command Summary

The VT18X control module accepts 11 commands for disk drive control. Commands should only be loaded into the command register when the busy status bit is off. The one exception is the force interrupt command. The busy status bit is set when a command is executed.

6.6.14.1 Type I Commands – Type I commands are for head positioning. The stepping rate of these commands is dictated by the disk drive. The recommended stepping rate is $r1 = 1$ and $r0 = 1$ (30 ms). The head load flag determines if the head is loaded at the beginning of the command. Otherwise, the head is loaded at the end of a command. The verification flag allows a verification operation to take place on the destination track. The verification consists of reading the first encountered ID field off the diskette. The track address of the ID field is compared to the track register. If there is a match and a valid ID CRC, the verification is complete. If not valid, the seek error status bit in the formatter/controller is set. The step, step-in, and step-out commands contain an update flag for updating the track register when this bit is set after the step has been completed.

6.6.14.2 Type II Commands – The type II commands allow you to read and write sectors of the diskette. Prior to loading the type II command into the command register, the sector register must be loaded with the desired sector number. Upon receipt of the command, the busy status bit is set. If the e flag is set (normal case), the head is loaded and the HLT signal is sampled after 30 ms. Otherwise, no delay is incurred after a command. The HLT does not become active until 1.0 second after the head is loaded. This allows the spindle motor to have time to accelerate. The formatter/controller then attempts to find the ID field with the specified track and sector. If it is not found within four revolutions of the diskette, the record not found status bit is set. Otherwise, the command is executed by the formatter/controller generating data requests (DRQs) for servicing the data register.

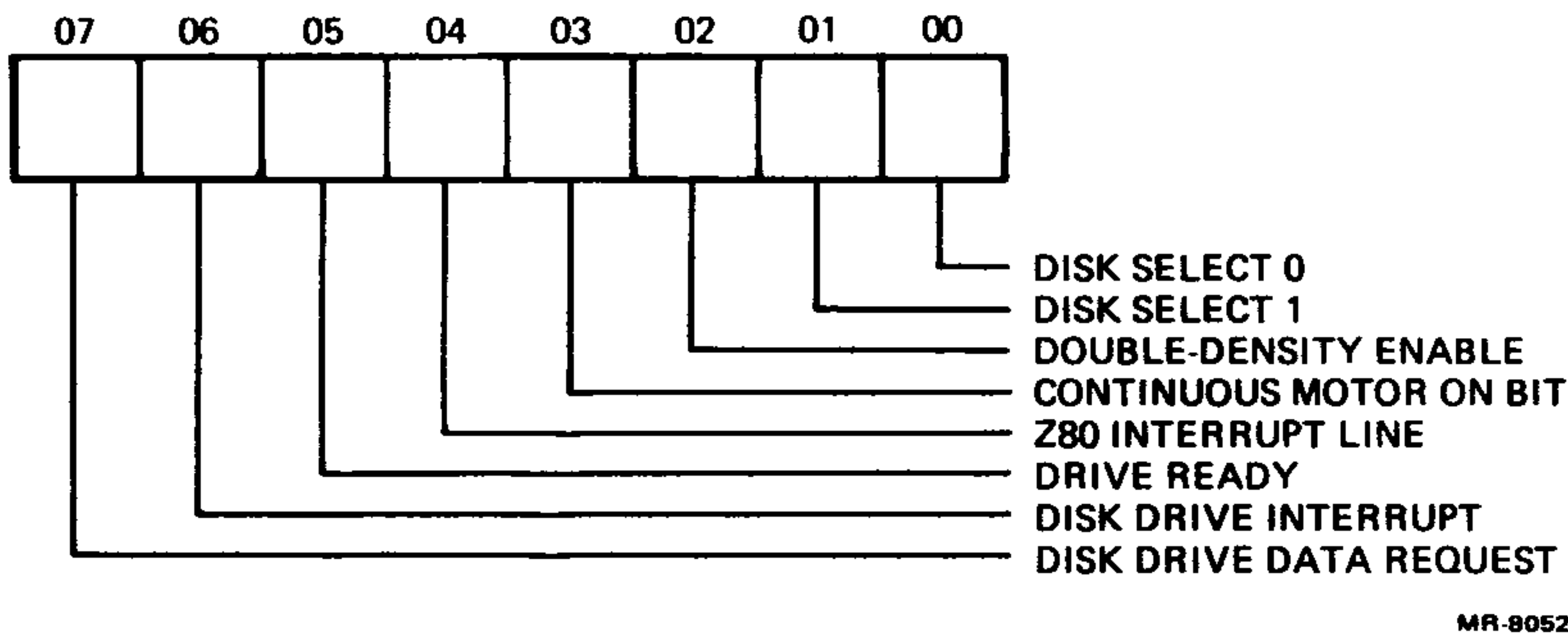
Each of the type II commands contains an m flag that determines if multiple sectors are to be read or written, depending upon the command. When set, multiple sectors are read or written with the sector register internally updated for address verification on the next track. The formatter/controller continues to do the transfers until the sector register exceeds the number of sectors on the track or until a force interrupt command is loaded into the command register. If the sector register exceeds the number of sectors on the track, the record not found status bit is set. When the head is loaded, the busy status bit is set; and when an ID field is encountered that has the correct track, sector, side numbers, and correct CRC, the data field is presented to the CPU (read) or presented by the CPU (write). At the end of the read operation, the type of data address mark encountered is recorded in the status register (bit 5). On a write operation, the a0 flag (bit 0) determines the type of data address mark to be written onto the diskette. If set, a deleted data mark is written. If reset, a data mark is written.

6.6.14.3 Type III Commands – These commands allow you to read and write format information on the diskette. The read address command is to read in the six bytes of the ID field (track number, side number, sector address, sector length, and two bytes of CRC). The read track command is to read a full track of raw information. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. The write track command is used to format a diskette.

6.6.14.4 Type IV Command – This command allows you to terminate an operation upon the condition specified in bits 3–0. See Table 6-26 for descriptions of the termination conditions.

6.6.15 General Control and Status Register (80H)
This 8-bit register holds various control information for the disk drive and the VT18X control module. The lower four bits are read/write, while the upper four bits are read-only.

The general control and status register format is shown in Figure 6-41. Table 6-30 describes the bits.



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Figure 6-41 General Control and Status Register Format

Table 6-30 General Control and Status Register Bit Description

Bits	Name	Description															
0, 1	Disk drive select	These bits hold the encoded value of the current disk drive to be selected. The configuration is as follows. <table><tr><th>Bit 1</th><th>Bit 0</th><th>Drive Selected</th></tr><tr><td>0</td><td>0</td><td>Drive 0</td></tr><tr><td>0</td><td>1</td><td>Drive 1</td></tr><tr><td>1</td><td>0</td><td>Drive 2</td></tr><tr><td>1</td><td>1</td><td>Drive 3</td></tr></table>	Bit 1	Bit 0	Drive Selected	0	0	Drive 0	0	1	Drive 1	1	0	Drive 2	1	1	Drive 3
Bit 1	Bit 0	Drive Selected															
0	0	Drive 0															
0	1	Drive 1															
1	0	Drive 2															
1	1	Drive 3															
2	Double-density enable	When low (0), this bit enables the read/write electronics of the formatter/controller in double-density mode. Since single-density will never be run on the system, this bit should always be low.															
3	Motor on	When set (1), this bit turns on the motor if W9 is installed. When cleared (0), the motor is under the control of a three second delay before it is shut off.															
NOTE When the motor is first turned on using this bit, a one second software delay must be observed before accessing the drive.																	
4	Z80 interrupt	When low (0), it means that the interrupt line of the Z80 CPU is asserted low (0). When high (1), no interrupt is pending.															
5	Drive ready	This bit indicates the status of the drive ready line of the interface. It is a read-only bit.															
6	Disk drive controller interrupt	When set (1), the disk drive controller has gone through a control sequence that normally would end in an interrupt. It is cleared by reading the floppy status register.															
7	Disk drive controller data request	This is a read-only bit that is a direct copy of the bit in the disk drive controller status register with one exception — the case of issuing a read or write sector command with DRQ still asserted.															

NOTE
When a command is issued, bit 7 is cleared internally (disk drive status) but not externally. Therefore, if the DRQ bit is set, the data register should be read in order to reset the external DRQ line, before issuing read or write commands.

6.6.16 Communications Status Register (88H)

This read-only register holds the status of modem control signal lines on the communications port as well as the status of the ROM enable bit. The communications status register format is shown in Figure 6-42. Table 6-31 describes the bits.

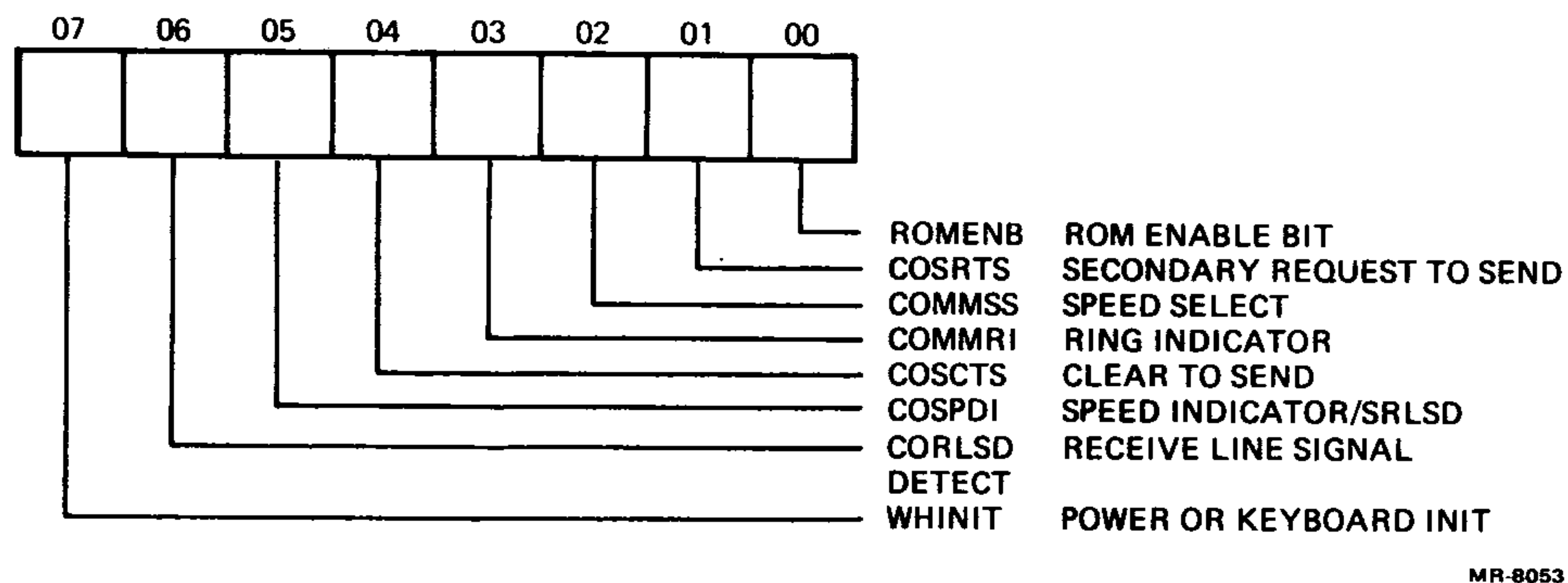


Figure 6-42 Communications Status Register Format

Table 6-31 Communications Status Register Bit Description

Bits	Description
0	When clear (0), this bit indicates the presence of the ROM starting at location 0000H. When set (1), the ROM is disabled and 64K bytes of RAM is available to the user. This bit represents the status of bit 0 in the diagnostic write register (98H).
1	This bit reflects the status of the SRTS line of the communications port as set by bit 6 of the communications control register.
2	This bit reflects the status of the speed select line of the communications port as set by bit 7 of the communications control register.
3	This bit reflects the status of the ring indicator line of the communications port.
4	This bit reflects the status of the clear to send line of the communications port.
5	This bit reflects the status of the speed indicator line or the secondary receive line signal detect line of the communications port.
6	This bit represents the status of the receive line signal detect line of the communications port.
7	This bit allows diagnostics to determine whether the system was initialized by a power on INIT or a keyboard initialize. After power on INIT, this bit will be set and should be cleared by a dummy read of register 90H so that subsequent initializes through the keyboard are detected by a low (0) condition.

6.6.17 Communications Control/Baud Rate Select Register (90H)
 Bits 0–2 in this register select the printer baud rate. Bits 3–5 select the terminal port’s baud rate while bits 6 and 7 toggle modem signals. This is a write-only register.

The communications control/ baud rate select register format is shown in Figure 6-43. Table 6-32 describes the bits.

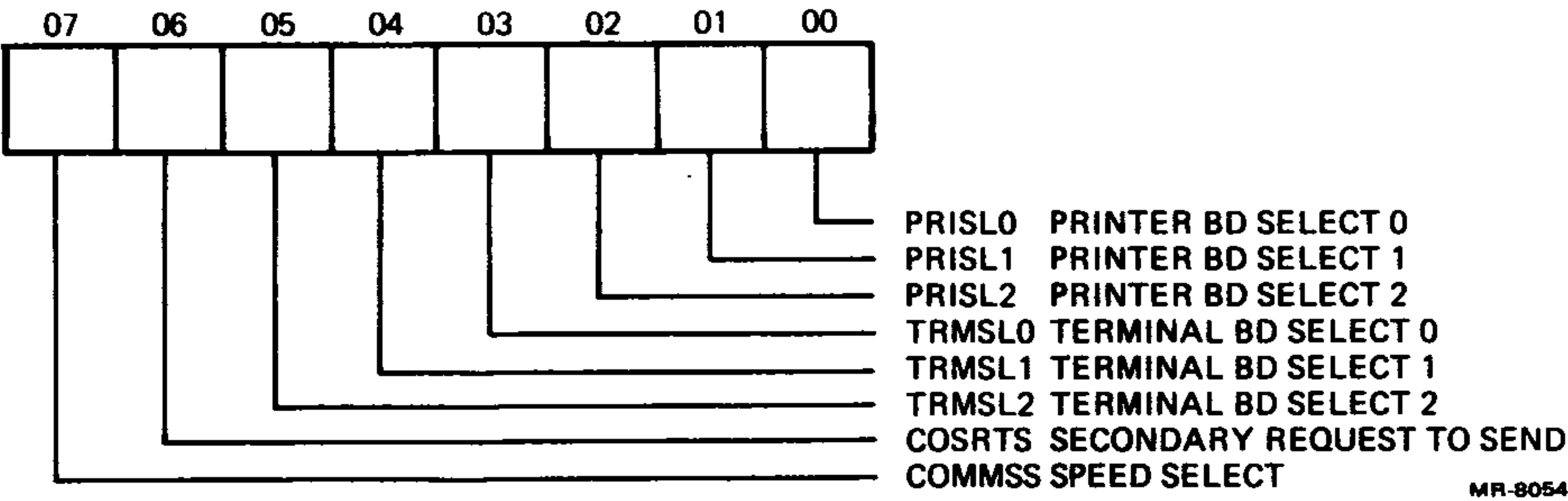


Figure 6-43 Communications Control/Baud Rate Select Register Format

Table 6-32 Communications Control/Baud Rate Select Register Bit Description

Bits	Description		
0-2	These bits hold the encoded value of the baud rate to be selected for the printer port.		
Bits			
2	1	0	Baud Rate
0	0	0	75
0	0	1	150
0	1	0	300
0	1	1	600
1	0	0	1200
1	0	1	2400
1	1	0	4800
1	1	1	9600
3-5	These bits hold the encoded value of the baud rate to be selected for the general purpose terminal port.		
Bits			
5	4	3	Baud Rate
0	0	0	75
0	0	1	150
0	1	0	300
0	1	1	600
1	0	0	1200
1	0	1	2400
1	1	0	4800
1	1	1	9600

6.6.18 Interrupt and INIT Reset Register (90H)

This register must be read while in an interrupt service routine for the real time clock in order to reset the interrupt line. This is merely supplying a dummy read to clear the interrupt. Any data read back has no significance. The same dummy read operation must be done to reset the who initialized (WHOINIT) line (bit 7) of the communications status register so that the next initialize sequence can be recognized. A read also resets the write data output (bit 4) in the diagnostic read register. A read from this register resets both of the bits.

6.6.19 Diagnostic Write Register (98H)

This write-only register is used for diagnostic control purposes. The upper four bits (7-4) directly address four LEDs that are turned on during a power-up or an INIT. Also contained in this register is a bit used during diagnostic testing to loopback all communications transmitted data to the communications receiver inputs. The diagnostic write register format is shown in Figure 6-44. Table 6-33 describes the bits.

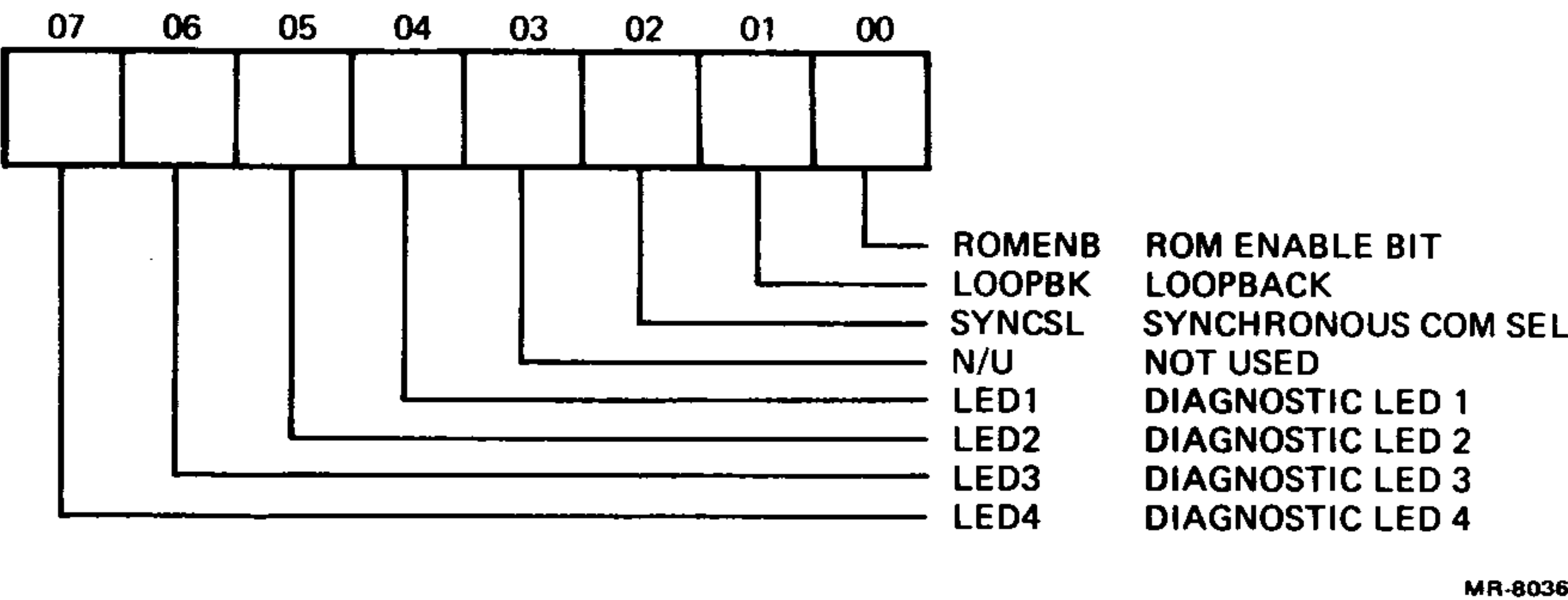


Figure 6-44 Diagnostic Write Register Format

Table 6-33 Diagnostic Write Register Bit Description

Bits	Description
0	This bit is cleared (0) upon an initialize to enable 8K bytes of ROM space starting at location 0000H. The ROM can be disabled by writing a 1 to this location, but the user must be careful not to write a 1 while executing code from ROM.
1	When set (1), this bit enables the transmit data of the communication and console ports to be looped back to the receive data of those same ports. Also, the transmit data of the printer and general terminal ports are looped back to the receive data line of the opposite port to allow checking of baud rates. This allows acceptable testability of the communications ports.
2	When this bit is set (1), the transmitter and receiver baud rates for the communications PUSART are supplied by the modem connected to the communications port. When low (0), the transmitter and receiver baud rates for the communication PUSART are the baud rates selected during VT180 set-up mode.
3	Not used.
4-7	These bits directly control the four LEDs on the VT18X control module. They are cleared upon an INIT, turning the LEDs on. When the bits are set, the LEDs are turned off.

6.6.20 Diagnostic Read Register (A0H)

This read-only register allows diagnostics to read signals from the disk drive interface connector so as to determine, as much as possible, controller functionality. The latched write data bit is latched so that the diagnostic can see if data is being written out. This bit is reset by a read to the address of 90H. The diagnostic read register format is shown in Figure 6-45. Table 6-34 describes the bits.

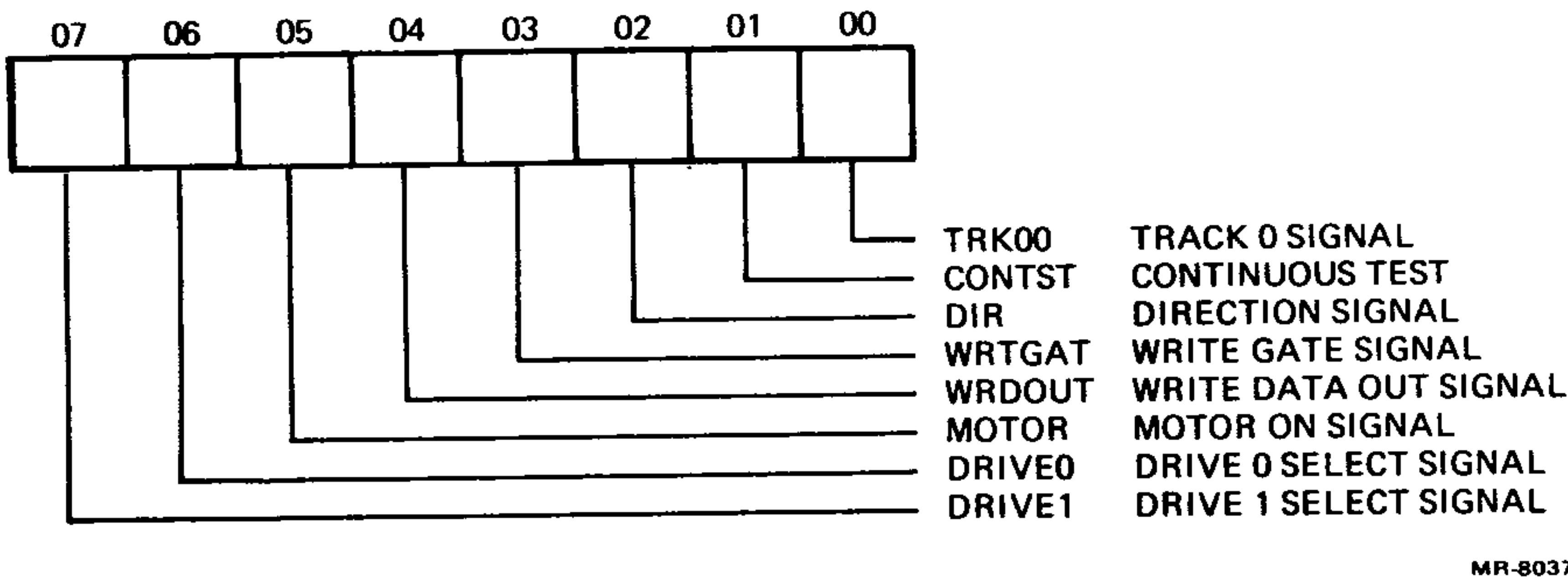


Figure 6-45 Diagnostic Read Register Format

Table 6-34 Diagnostic Read Register Bit Description

Bits	Description	
0	When set (1), this bit informs the formatter/controller that the R/W head is positioned over track 0.	
1	This bit is used only for manufacturing testing. It is set to 1 for normal operation.	
2	When set, this bit indicates that the R/W head is stepping away from the spindle. When low, the R/W head is stepping toward the spindle.	
3	When cleared, this bit indicates that writing may be performed.	
4	When set, this bit indicates that write data has been sent to the disk drive.	
5	When set, this bit indicates that the disk drive motor is turned on.	
7, 6	These bits indicate which disk drive is currently selected. The bit indications are as follows.	
Bit 7	Bit 6	Drive Selected
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

6.7 VT180 PADDLE BOARD DESCRIPTION

The VT180 paddle board is a printed circuit board (Digital part number 50-15149) that is 11.45 cm (4.51 inches) wide and 12.47 cm (4.91 inches) high. The printed circuit board contains a 25-pin, D-type EIA connector for the printer port, a jumper, a 16-pin socket, and a 40-pin edge connector that plugs into the STP connector on the terminal controller module. The printed circuit board also contains pull-up resistors for modem control signals and filter components needed to satisfy FCC requirements. The 16-pin socket is used to connect signals between the STP connector and the VT18X control module. Printer, communications clocks, and general purpose serial port signals are supplied by the 16-pin ribbon cable connecting the terminal controller module and the VT180 paddle board. Table 6-35 describes the 16-pin IC socket (J2) connector signals, and Table 6-36 lists the printer port J1 signals.

Table 6-35 VT180 Paddle Board Signals

J2			
Pin No.	Mnemonic	Direction*	Description
1	INIT	In	When asserted high, the VT100 is issuing an initialize to the VT18X control module.
2	TRM XMT DATA	Out	This signal is the transmitted data line to the 25-pin, D-type connector extending from the terminal controller module.
3	CON CLK	In	This signal is the local clock that the VT180 uses to talk with the VT18X control module. This signal is a 15.7 k baud signal that originates in the terminal controller module.
4	PRI XMT DATA	Out	This signal is the transmitted data line to the 25-pin, D-type connector extending from the VT180 paddle board.
5	GND		This is the logic ground between the terminal controller module and the VT18X control module.
6	COM RXC	In	This signal is the communications receive clock. The signal frequency is set through the VT180 SET-UP B mode as the value called R SPEED XXXX, where XXXX multiplied by 16 is the frequency of this signal.
7	COM TXC	In	This signal is the communications transmit clock. The signal frequency is set through the VT180 SET-UP B mode as the value called T SPEED XXXX where XXXX multiplied by 16 is the frequency of this signal.
8	MFU1	Out	This signal is the printer baud rate of the printer port on the VT18X control module. This signal is not used in the VT180.
9	PRI REC DATA	In	This signal is the received data line from the 25-pin, D-type connector extending from the VT180 paddle board.
10	CON XMT DATA	Out	This is the transmitted data line to the terminal controller module via the STP connector.

*Direction of these signals as viewed from the VT18X control module.

Table 6-35 VT180 Paddle Board Signals (Cont)

J2			
Pin No.	Mnemonic	Direction*	Description
11	TRM DTR	In	This signal is the data terminal ready signal from the 25-pin, D-type connector supporting the general purpose serial port.
12	CON DTR	In	This is the data terminal ready signal from the terminal controller module.
13	GND		This is a logic ground between the terminal controller module and the VT18X control module.
14	TRM REC DATA	In	This is the received data from the general purpose serial port.
15	PRI DTR	In	This is the data terminal ready signal from the 25-pin printer connector.
16	CON REC DATA	In	This signal is the received data input from the terminal controller module.

*Direction of these signals as viewed from the VT18X control module.

Table 6-36 Printer Port Signals

Pin Number	Signal Description	Mnemonic	Direction*
1	Protective ground	PROT GND	
2	Transmit data	TXD	Out
3	Receive data	TXD	In
6	Data set ready	DSR	In
7	Signal ground	GND	
20	Data terminal ready	DTR	Out**

*Direction of these signals as viewed from the VT18X control module.

**This output is always asserted high.

6.8 VT100 MONITOR

Two monitors have been used in VT100 production. Early VT100s used a monitor manufactured by Ball Brothers that is identified by Digital part number 30-14590. (For a description of the Ball Brothers monitor, refer to the *VT100 Series Technical Manual*.) Later terminals used a monitor manufactured by Elston, and this monitor is identified by Digital part number 30-16080. Most of the circuitry in these monitors is standard television technique, and this description simply highlights the signal path. An overview of the general principles of the horizontal section is included since this circuit is not intuitively understandable from an examination of the schematic. It is also the likely candidate for failure because of high stresses in the components.

6.8.1 Elston Monitor Board Description (Digital part number 30-16080)

6.8.1.1 Video Driver – The cathode driver stage gets its operating supply of 38 volts from a winding of the flyback transformer. R108 is the collector load resistor. C101 bypasses the emitter resistor to improve high frequency response. The stage is intended to be biased by the driving circuit (direct video out in the terminal controller). R105 couples the video signal to the cathode limiting current flow if the CRT arcs.

6.8.1.2 Brightness – The brightness control circuit gets its –150 volt operating supply from the horizontal output circuit. A charge pump (C104, C105, CR103, CR104) produces a large negative voltage by inverting the large positive swings in the stage. The brightness voltage returns to the +38 volt video output power supply rather than ground, to allow the brightness control output to vary from –42 to +17 volts. The brightness control potentiometer R109 varies the bias on the first grid of the CRT. C107 bypasses currents resulting from internal CRT arcs from the high voltage anode and also bypasses video signals from the grid to ground.

6.8.1.3 Vertical Oscillator – The vertical oscillator receives its synchronizing drive through inverter-buffer Q298. R331 and C314 are a low pass filter on the input for noise immunity. The input is ac-coupled so that if the drive stops in either a high or low state, the circuit can self-oscillate to keep the beam moving on the CRT.

Basically, the oscillator is an RC timer with R333 and R334 through CR304 charging a capacitor made of C318 and C319 in series. As the voltage across the capacitor rises, emitter follower Q309 drives the output amplifier Q310 so that its collector current rises at the same rate. CR304 is two diode drops to compensate for the drops in Darlington Q309 so the voltage at the base of Q310 is the same as the voltage at the top of C318. When Q308 receives a vertical drive pulse, it discharges the capacitor.

R341 and R342 are positive feedback to the junction of C318 and C319. As Q310's emitter voltage rises with increasing current, the two resistors couple that voltage back to the timing capacitor. This makes the voltage across the capacitor rise faster than it would with only the charging current from R333 and R334. But because the rise in capacitor voltage causes Q310 to turn on more, the feedback voltage increases as well. The exponential rise in Q310's output current that results closely matches the variations in L301's current. This is explained more under Linearization (Paragraph 6.8.1.6).

6.8.1.4 Self-Oscillation – If the vertical circuit does not receive a drive signal, it oscillates by itself to keep the electron beam moving to prevent a phosphor burn. The self-oscillation period is longer than the period between vertical drive pulses so the drive pulses, when present, always control the vertical scanning rate.

Without a drive signal, Q308 is off. The regular RC circuit produces a rising voltage at the base of Q310. While Q310's output moves the electron beam, its base voltage is coupled to Q308 through R335 and CR302. When the voltage rises above the diode drops of CR302 and Q308 base-emitter junction, Q308 turns on, discharging the timer and cutting off Q310. The retrace voltage that forms at L301 is coupled by

R344, C316, and R339 back to Q308 to keep it on long enough to complete a retrace even though the voltage from Q310's base (that started the cycle) has started to decrease. After the voltage at L301 falls (due to current flow to the yoke), the drive to Q308 is gone, Q308 turns off, and the self-oscillation cycle begins again.

6.8.1.5 Vertical Output – Consider L301, which is a large inductor, to be a constant current source. Assume that the yoke starts with a current that deflects the beam to the top of the screen and that Q310 is off. The current flows out of L301 through C321 and into the yoke. Q310 now turns on with a gradually rising voltage on its base. Q310 thus draws an increasing amount of current from the junction of L301 and the yoke. Because L301's current is relatively constant, less current is available for the yoke; so as Q310's current increases the yoke's current decreases. Eventually Q310 passes all of L301's current and the yoke current is zero with the beam in the center of the screen. As the current in the collector of Q310 increases further, the current in the yoke reverses and adds to the current coming from L301. This opposite current deflects the beam toward the bottom of the screen. Now the vertical drive pulse turns Q310 off, and L301 produces a large positive voltage to try to maintain its constant current. This voltage rapidly reverses the current in the yoke and makes the beam return to the top of the screen very quickly. Q310 turns back on and the cycle repeats.

C320, R338, and R340 limit the voltage across L301 during vertical retrace.

6.8.1.6 Linearization – Because L301 is not an infinitely large inductor, it is not a perfect current source. Current through it decreases gradually until the beam reaches the center of the screen and then increases again toward the end of the cycle. This nonramp component of the current would cause character height to vary from top to bottom if allowed to pass to the yoke. The exponential drive to Q310 as a result of feedback causes Q310 to accept the varying current from L301 at the same time that a ramp current through the yoke is maintained.

6.8.1.7 Horizontal Driver – The horizontal driver receives a TTL level drive pulse from the terminal controller. R468 limits the base current to Q413. C435 provides noise immunity for the drive input.

When the input is high, Q413 is on. With pin 6 of transformer T403 pulled low by Q413 and with about half the supply voltage at pin 4, there is approximately 6 volts across the primary winding 4-6. The secondary winding 3-2 sees one quarter of this voltage across itself due to the 4:1 turns ratio, but no current flows because Q414's base-emitter junction is reverse biased. Meanwhile, current increases through winding 4-6 while Q413 is on, storing energy in T403's core. When the drive signal falls, turning Q413 off, winding 3-2 reverses polarity. Current now flows from T403 winding 3-2 through Q414's base-emitter junction, Q414 saturates, and the horizontal output functions as discussed in the following paragraphs.

When the drive signal goes high again at the beginning of horizontal retrace, Q414 needs to turn off very quickly to minimize dissipation. The purpose of opposite polarities in T403 is to force Q414 off by turning Q413 on. When Q413 turns on, winding 3-2 reverses polarity again and this voltage forces Q414's base-emitter junction into a reverse biased state, rapidly discharging Q414's stored base charge and cutting off Q414's collector current.

R470 limits the peak current through Q413. R470 and R471 (if present) limit the on time of Q414. C443 (if present) speeds up the turn-off of Q414. C436 limits the peak voltage that develops across Q413 caused by leakage inductance in the primary of T403 that prevents complete coupling of the primary energy into the secondary. C437 filters Q413's power supply.

6.8.1.8 Horizontal Deflection Operation – The horizontal output circuit consists basically of Q414, CR406, C438, C441, and the horizontal deflection yoke. Assume that the beam is at the center of the screen during a scan. Refer to the waveform diagram (Figure 6-50) for reference points T0 through T4.

T0: Right half of scan (Figure 6-46)

Initial Condition: The current through the yoke is zero. C441 is charged to +15 volts. Q414 is on.

Action: Current now flows out of the yoke through Q414, pushed by the voltage across C441. The voltage across C441 is nearly constant so the current through the yoke's inductance increases linearly. As the current increases, the beam moves to the right of the screen. The magnetic field building in the yoke stores energy.

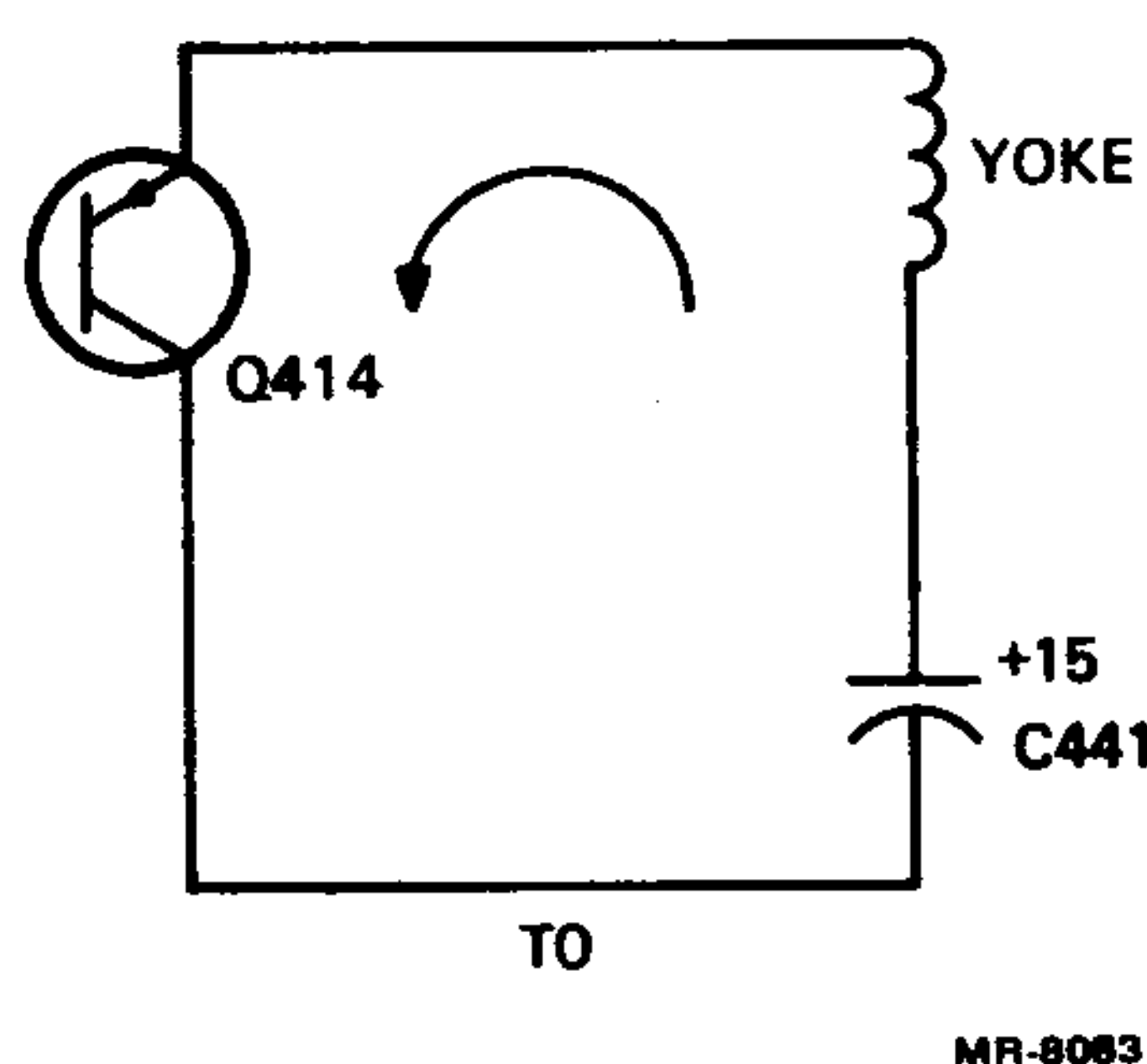


Figure 6-46 Horizontal Deflection Current – T0

T1: Start of retrace (Figure 6-47)

Initial Condition: Current out of the yoke is maximum. Q414 is switched off. C438, which had been grounded by Q414, has zero volts across it.

Action: Current continues to flow out of the yoke by inductive inertia as the stored magnetic field collapses. C438, which is a small valued capacitor, quickly charges to a high voltage. This voltage opposes current flow and causes a rapid reduction in current. The beam quickly returns to the center of the screen.

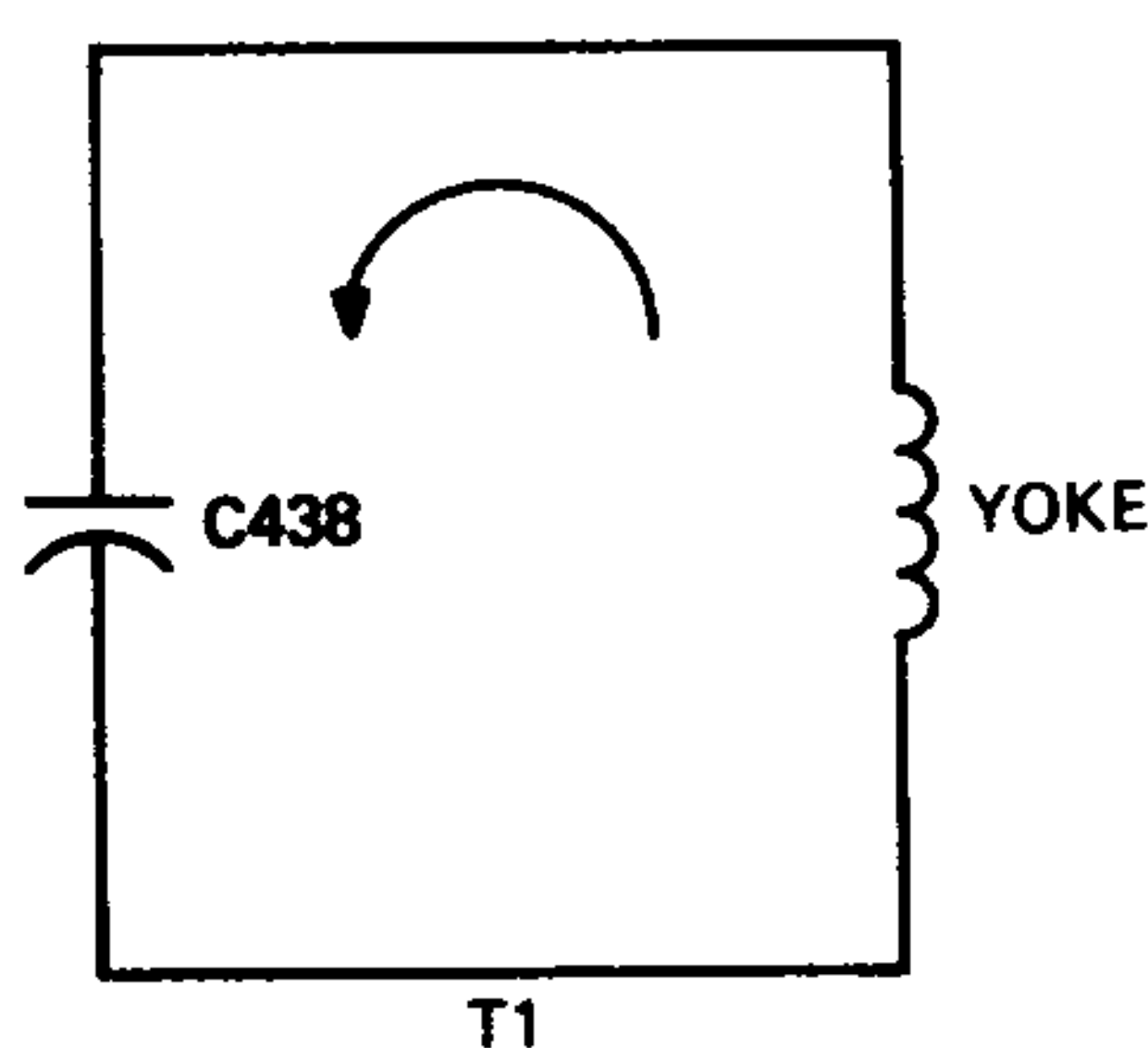


Figure 6-47 Horizontal Deflection Current – T1

T2: Middle of retract (Figure 6-48)

Initial Condition: Current through the yoke is zero. C438 is charged to +175 volts.

Action: The high voltage across C438 causes a rapid rise in current into the yoke. The beam moves to the left of the screen.

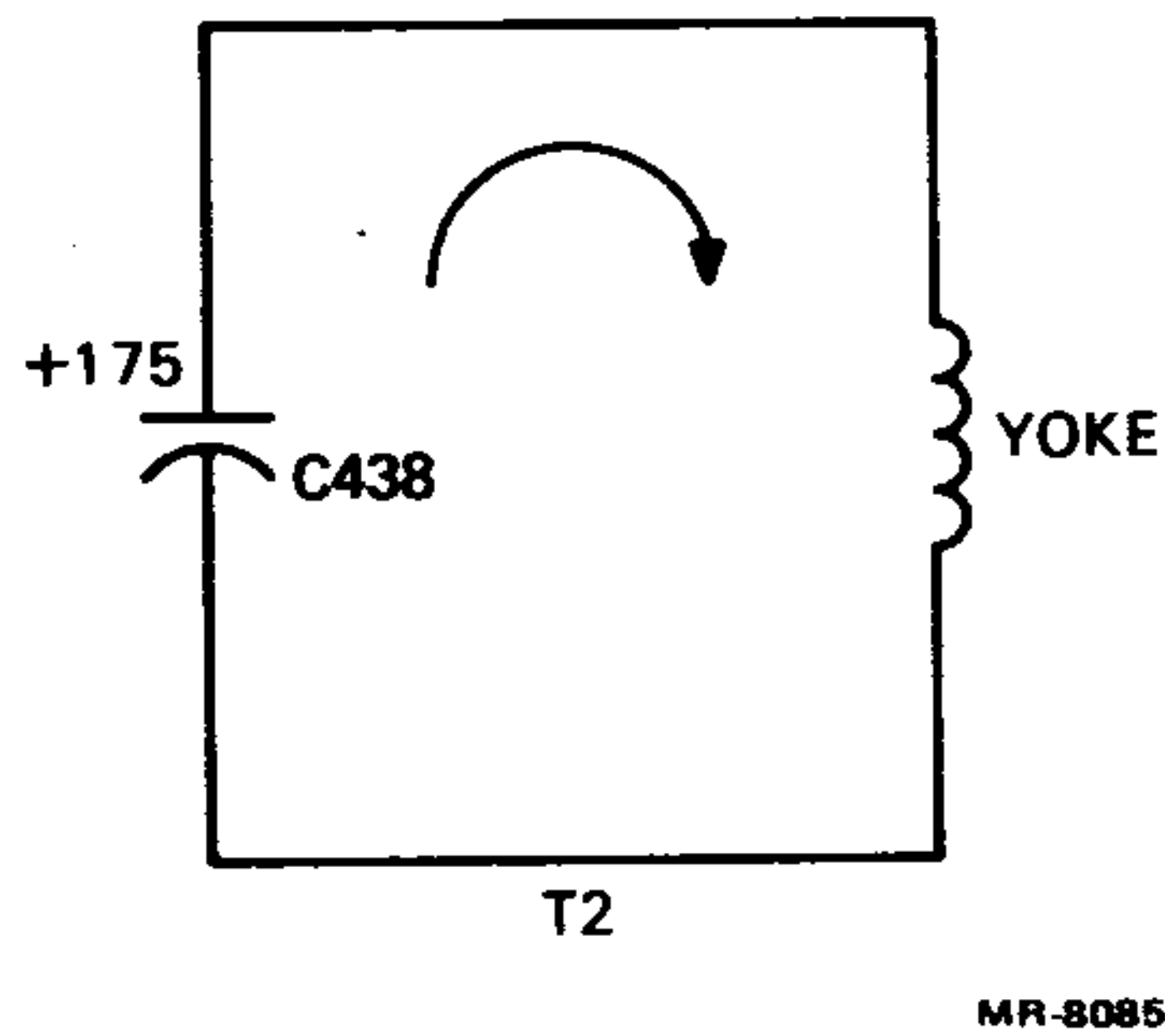


Figure 6-48 Horizontal Deflection Current – T2

T3: Start of scan (left half) (Figure 6-49)

Initial Condition: Current into the yoke is maximum. C438 is discharged.

Action: Inductive inertia makes the top of the yoke slightly negative, forward biasing CR406 to provide a return path for current out of the bottom of C441. The yoke current gradually decreases as the magnetic field collapses and discharges into C441 against the voltage across C441. The beam moves to the center of the screen.

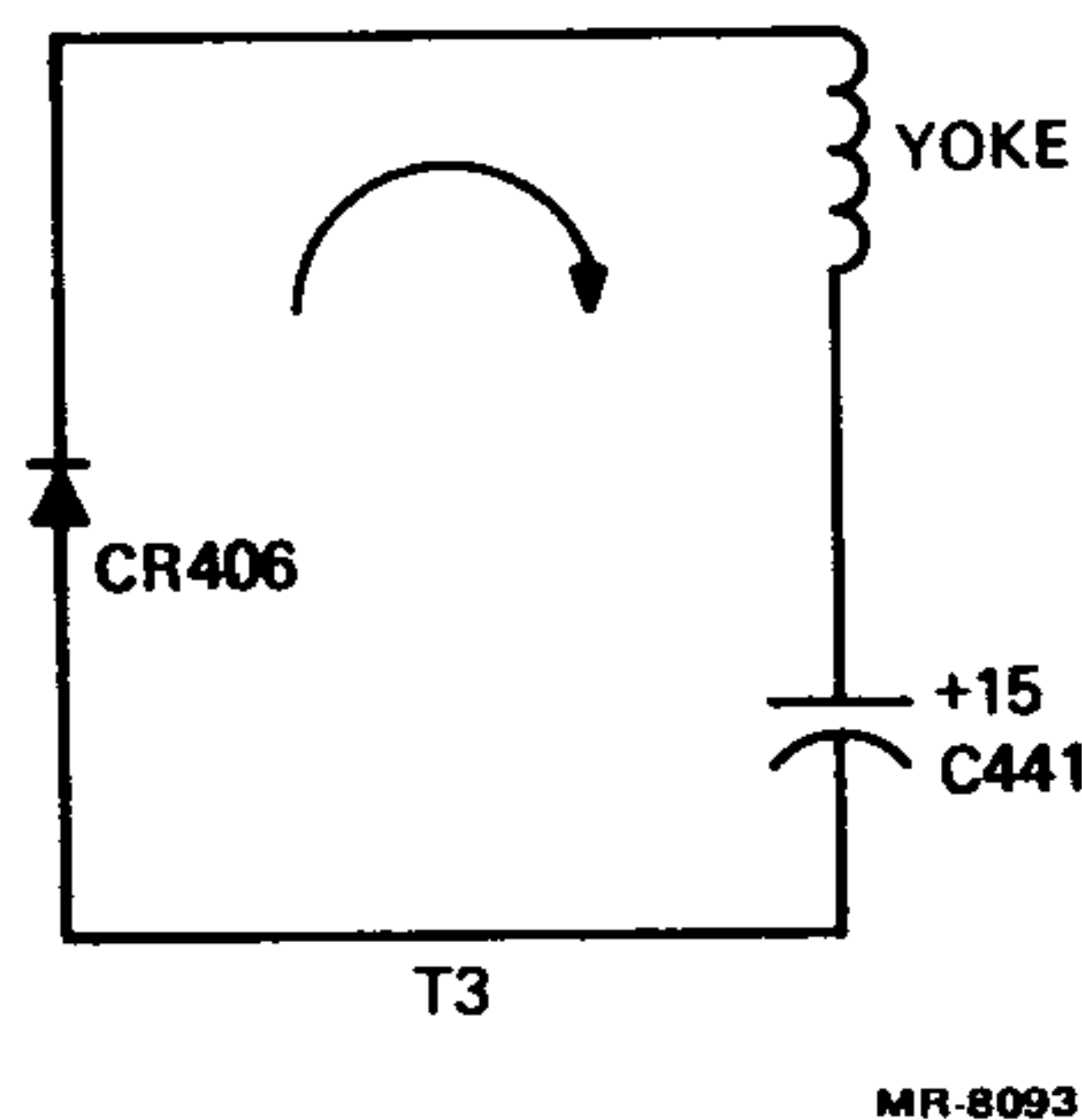


Figure 6-49 Horizontal Deflection Current – T3

T4: Return to T0

6.8.1.9 Horizontal Output Circuit – (Refer to Figure 6-50.) L403 adds a variable inductive reactance that controls current in the circuit to vary the scan width. L402 is a magnetically biased inductor whose reactance varies nonlinearly with changes in yoke current. This, with R481 and C442, provides correction for nonlinearity caused by the decaying exponential rate of current increase in the yoke caused by the yoke's resistance. It does this by allowing more voltage across the yoke at the end of the scan. This is needed, because as current increases, the voltage drop increases across the resistance of the yoke tending to reduce the rate of current increase.

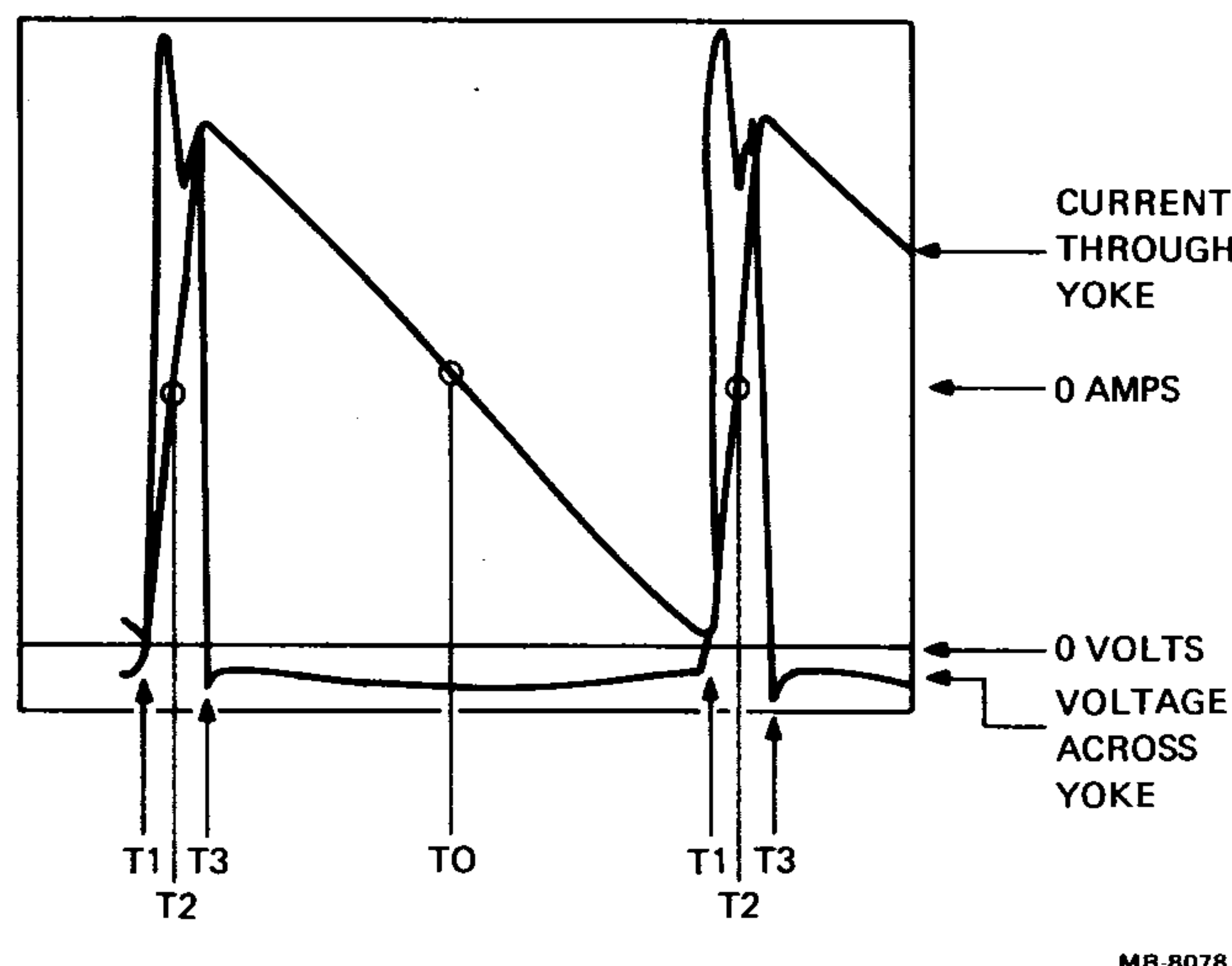


Figure 6-50 Horizontal Deflection Waveforms

Power enters the circuit through the primary of the flyback transformer. CR408 and C439 work with an autotransformer winding on the primary to boost the stage's operating voltage to +15 volts. The output circuit shuttles yoke current back and forth between C438 and C441, losing only a small amount of power in resistive losses. Therefore, the average current through the flyback primary is small (approximately 800 mA). C438 is relatively small so that the voltage drop across its reactance can provide S correction for the horizontal scan. This compensates for the difference between the arc of the tube face and the arc of the beam's deflection. Each time Q414 turns off, a 175 volt pulse, lasting the interval of horizontal retrace, appears at the dotted end of the flyback primary. This pulse passes into the flyback secondary to provide high voltages for the CRT.

6.8.1.10 High Voltage and Focus – When the 175 volt pulse appears on the flyback primary at retrace, the flyback secondary produces 12 kV, which is rectified by CR407 and filtered by the capacitor made by the aquadag (graphite) coatings on the inside and outside of the CRT's glass envelope. Screen and focus grid voltages of about 370 volts come from a lower voltage winding on the flyback and are rectified by CR409. For the cathode driver, 38 volts comes from another winding and is rectified by CR102.

6.9 POWER SUPPLY

The power supply is a switching supply that has 95 watts capacity with four separate voltage outputs. Figure 6-51 is a block diagram of the power supply.

6.9.1 Power Input

The input to the supply consists of an electromagnetic interference (EMI) filter, an on/off switch, a fuse, and a 120/230 voltage selector switch. Either on 120 Vac or 230 Vac input, thermistors R1 and R50 reduce the start-up inrush currents to safe levels. For 120 Vac operation a voltage doubler rectifier is used;

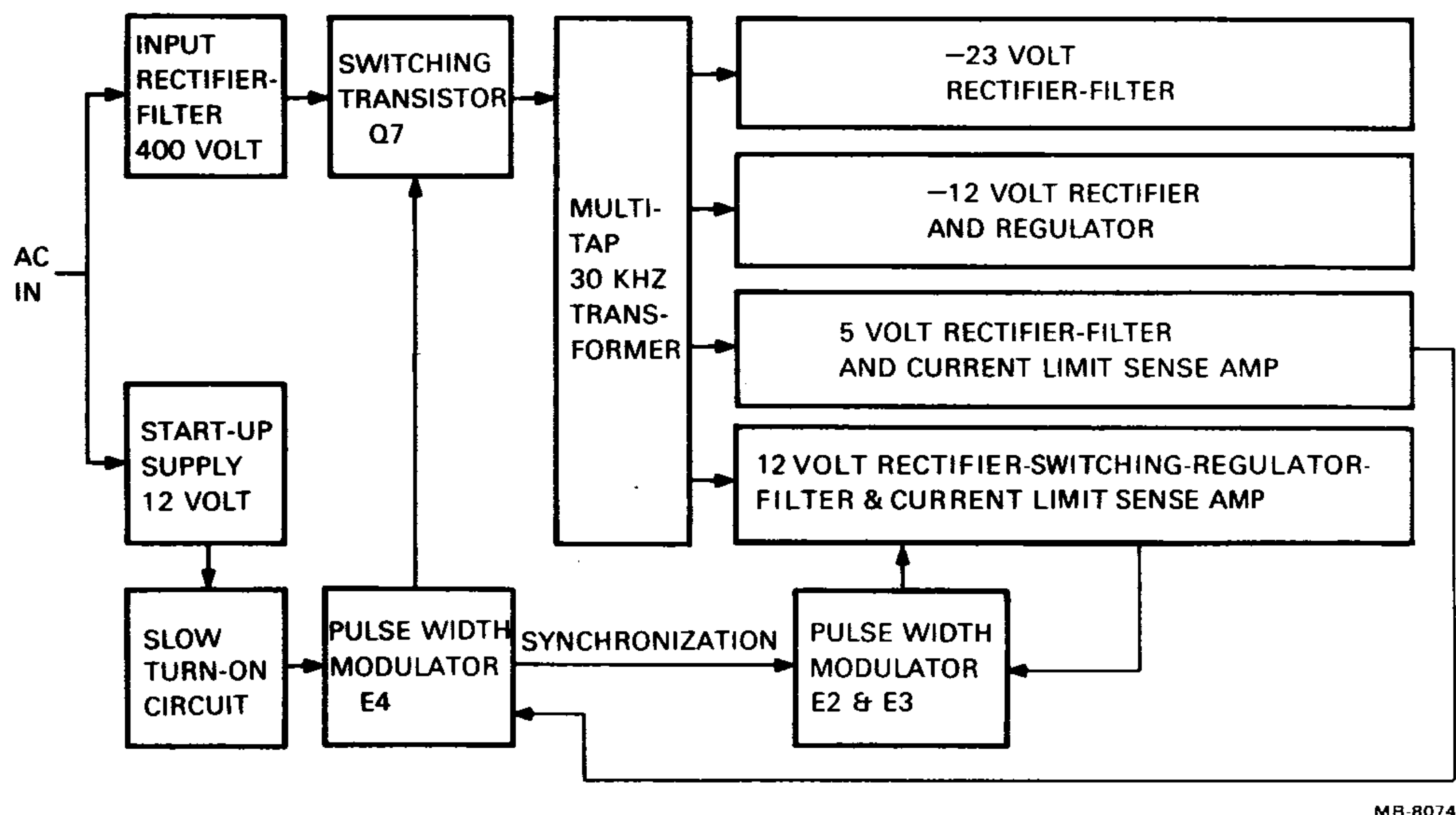


Figure 6-51 VT100 Power Supply Block Diagram

for 230 Vac operation a full wave bridge rectifier is used. The storage voltage across both C9 and C14 varies with the input line voltage from 200 to 360 Vdc. R19 and R20 are bleeder resistors.

6.9.2 Start-Up Circuit

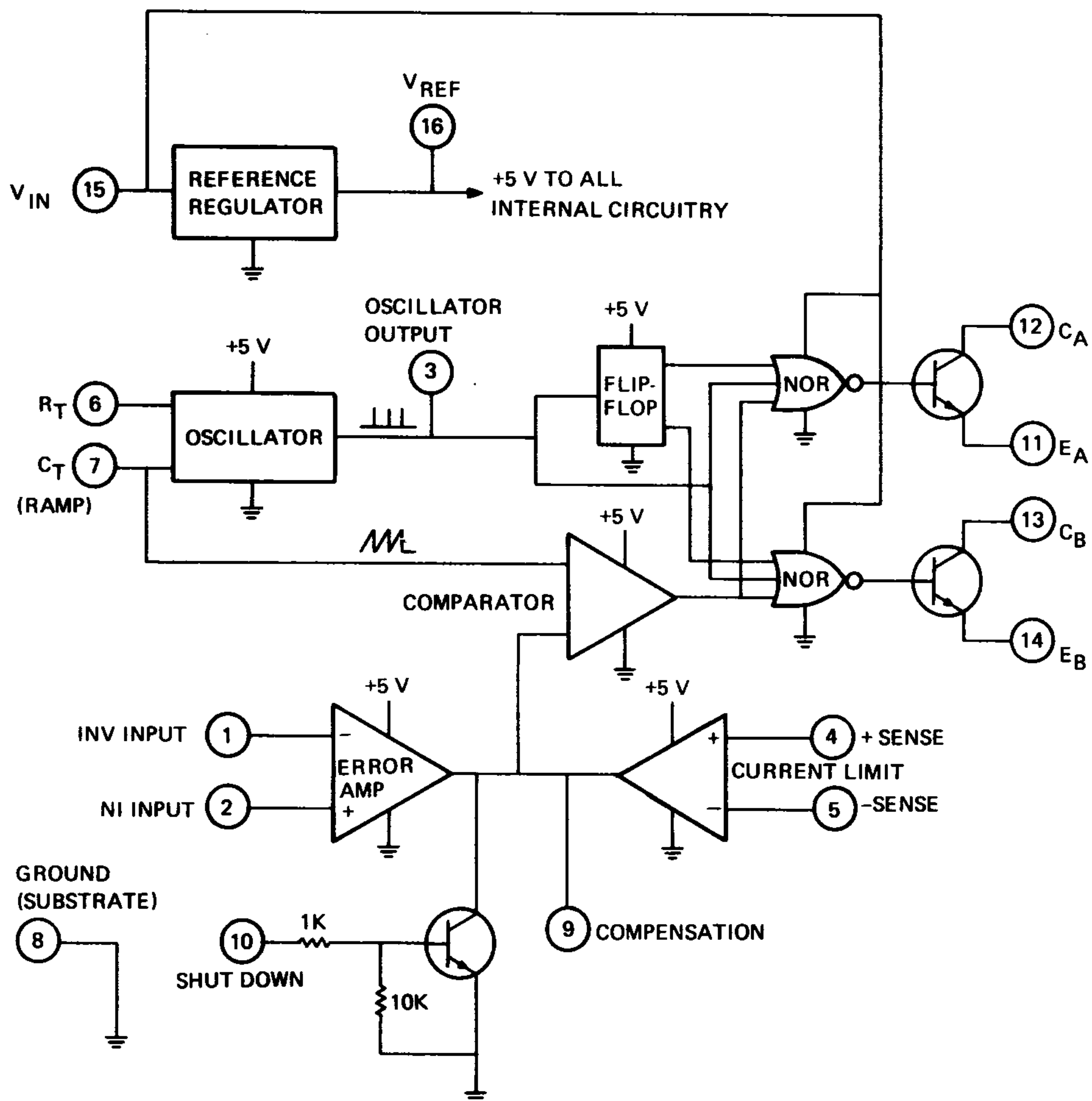
Transformer T2 is a start-up transformer that supplies the power to start the control circuit. The ac voltage on the primary of T2 is stepped down, rectified, and filtered by C33. The dc voltage is applied to the input of +12 volt regulator Z2. The output passes through two diodes, D24 and D25, to the control circuitry. When the unit is turned on, the only voltage supplying power to the control circuit is from the regulator Z2. After the outputs come up, the +12 output is fed back through diode D34 to the control circuitry. Because it is higher than that delivered by the start-up circuit, this voltage will back bias D24 and D25, isolating the Z2 regulator. This scheme of returning the output through D34 enables the power supply to also meet its ride-through specification (ability to supply power during brief outages).

6.9.3 Control Circuit

The control circuit in the power supply is designed around the 3524 pulse width modulator (PWM) IC. It houses a voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switcher, current limit circuit, and a shutdown circuit. Refer to the regulator IC block diagram in Figure 6-52 and the power supply timing diagram in Figure 6-53.

The oscillator frequency is determined by resistor R18 and C7. The ramp generated by C7 is used as a reference for the comparator. The discharge time of C7 determines the pulse width of the oscillator output pulse. This pulse is used as a blanking pulse to ensure that the outputs of the 3524 cannot turn on simultaneously. Capacitor C5 ensures that the blanking pulse is wide enough.

The error amplifier in the 3524 is a transconductance amplifier with an output (pin 9) impedance of approximately 5 megohms. Pin 9 is a convenient point to place the compensation network, R30, C17, and R13. It is also an ideal point to turn off the switching regulator and to put the slow-turn-on circuit. The slow-turn-on circuit consists of D39, R51, D40, and C34. When the power supply is initially turned on, pin 9 is pulled to ground by C34 through D39. As C34 charges slowly and exponentially, pin 9 follows, turning the power supply on slowly and exponentially. The current that charges C34 comes from pin 9 and the +12 volt start-up. Pin 9 operates at a dc level that is determined by the input error voltage into the amplifier. C34 eventually charges to +12 volts, thus back biasing D39. When the supply is turned off, C34 discharges through D40, allowing the supply to be ready for another soft start.



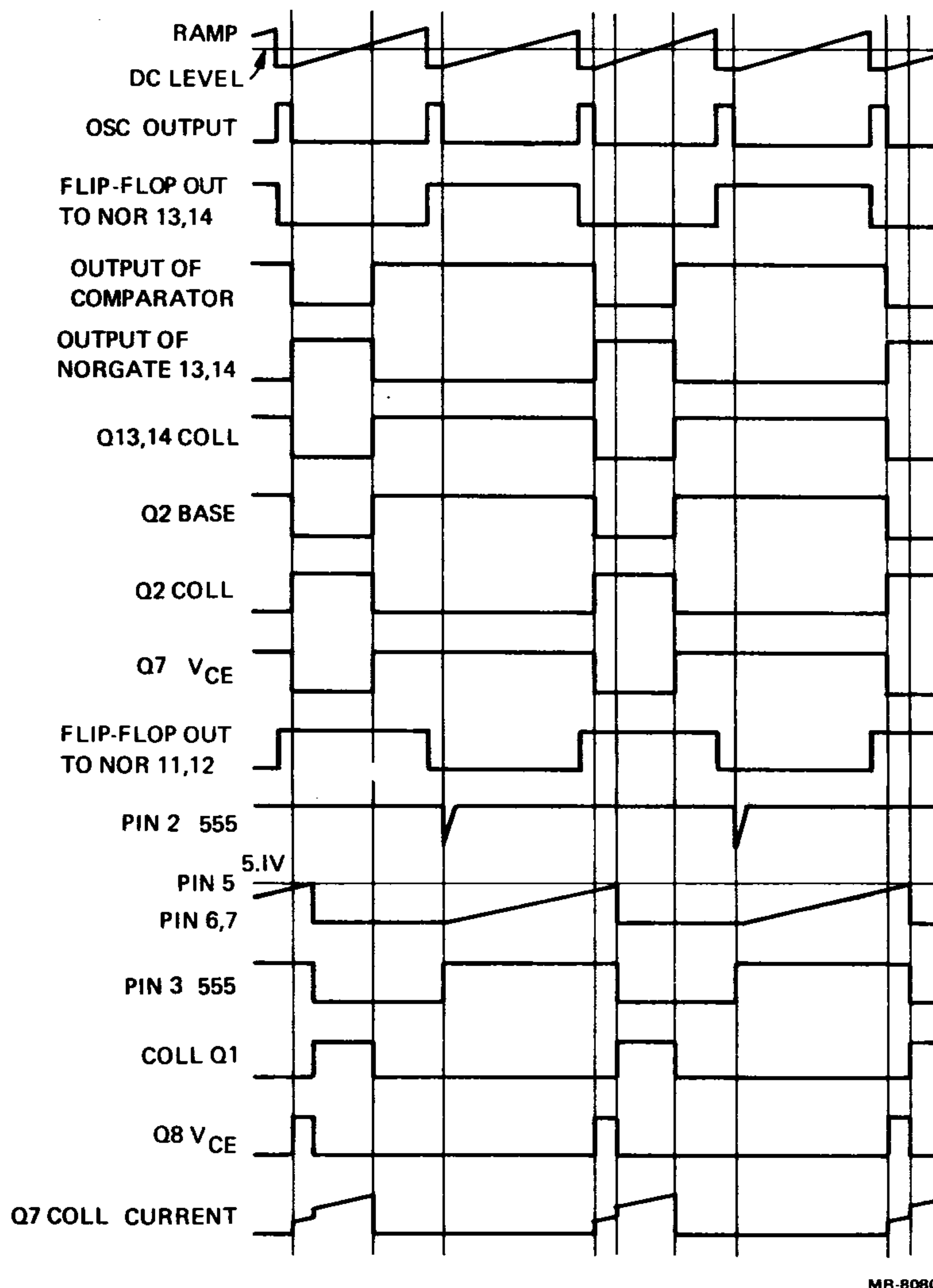
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Figure 6-52 3524 Regulator Block Diagram

The inverting side (pin 1) of the input to the error amplifier is tied to the +5 volt output through a dividing network, R32 and R48. The noninverting side (pin 2) is referenced to a 5.1 volt zener, D38, through a divider network, R41 and R49. An error appearing at the input causes pin 9 (output of the error amplifier) to shift. This dc level shift is tied into an input of a comparator. As mentioned earlier, the ramp generated by C7 is tied into the other input of the comparator. This is the means by which the regulator is pulse width modulated.

The actual frequency of the oscillator is 60 kHz. The switching frequency of the power supply is one-half that of the oscillator, 30 kHz, because only one of the single-ended outputs is used. This output (pin 13) a pulse width modulated wave, turns transistor Q4 on and off. When Q4 is off, Q3 supplies base current to Q2, turning it on. D7 and D8 are antisaturating diodes. R14 limits the base drive, and R15 and C4 are a speed-up circuit to turn Q2 on and off fast. When Q2 is on, Q7 (high voltage switch) is off.

Current flows from +12 through R11, D6, and winding 5,6 of pulse transformer T3 through transistor Q2 to ground. The circuit remains in this state until the base drive to Q2 is removed by the control circuit. When Q2 turns off, the voltage across T3 winding 5,6 reverses, causing all the dotted ends of windings in T3 to become negative. Current starts to flow into the base of Q7. This causes collector current to flow. This current flows through winding 1,2 of T1, through the transistor and winding 2,1 of T3. The current in winding 2,1 of T3 produces current flow in windings 3,4 and 7,8 of T3. The action that takes place is



MR-8080

Figure 6-53 Power Supply Timing Diagram

regenerative and causes Q7 to snap on. When Q7 conducts, energy is transferred from the primary of T1 to the secondary. The positive voltage at terminal 5 of T1 charges capacitor C6 through D14 and R21. The voltage at terminal 5 depends on the conduction time of the switch. When the control circuit switches Q2 on, C6 discharges through D9, winding 5,6 of T3 and transistor Q2. The current through winding 5,6 of T3 makes all dotted ends positive on T3. The negative polarity on the base of Q7 turns it off. D11 is across T3 and Q2 for noise immunity. Diodes D41, D12, and D3 are antisaturation diodes. C19, R27, and D27 form the snubbing network.

Winding 1,3 of T1 is a reset winding. On turn-off, this winding clamps the collector of Q7 to two times the storage voltage. It is also used for resetting the high frequency transformer core.

6.9.4 Outputs

There are four secondary outputs. The -23 volt output is rectified by D28, filtered by C18, and passed on through a 300 ohm resistor. The output goes to two zeners mounted on the video board. The 300 ohm resistor limits power dissipation in the zeners and also dissipates all power under short circuit conditions.

The -12 volt output consists of a rectifier diode (D29), filter capacitor (C20), and a regulator Z1.

The voltage at winding 9,10 of T1 is rectified by D36 and goes into an averaging network L2 and C31.

The catch diode, part of D36, completes the conduction path when Q7 is off. When Q7 is on, there is a voltage on the secondary, with pin 9 being positive. D36 is forward biased, and current flows through L2. This causes the inductor current to increase at this time. With the switch open, stored energy in the inductor forces the current to continue to flow to the load and return through the catch diode (D39). The voltage across L2 is now reversed and is approximately equal to the output voltage. During this time the current in L2 decreases. The average current through L2 equals the load current. Since C31 keeps the output voltage constant, the load current will also be constant.

The +12 volt output circuitry works in the same manner except the voltage at winding 4,5 is turned on by Q8 and turned off by the voltage at terminal 5 going negative.

The current limit circuits for the +5 and +12 outputs have identical configurations; only some resistance values differ. The voltage at pin 5 of the comparator referenced to the junction of R16 and R37 is compared to the voltage drop across R37. When the voltage across R37 increases to a point where pin 6 is more positive than pin 5, E1 switches and pin 7 goes low, pulling pin 9 of E4 to ground and thus turning off the switching regulator.

The +12 volt control circuitry is synchronized to the 3524 pulse width modulator at a 30 kHz rate. When pin 12 of E4 is high, capacitor C15 charges up from the +12 start-up through R29, R26, and D13. The polarity on the capacitor is such that when pin 12 of E4 goes low, the emitter of Q6 is pulled negative with respect to the base, which is at ground. Q6 saturates, pulling pin 2 of E3 down and thereby allowing the ramp generated at pins 6 and 7 by C13 to ramp up. Pin 6 is the threshold pin. The input to this pin is compared to the voltage at pin 5. When the voltage at pin 6 is equal to that of pin 5, pin 7 discharges capacitor C13 and pin 3 of E3 goes low. Whenever the voltage at pins 6 and 7 is ramping up, the output of E3, pin 3, is high.

C13 is the timing capacitor for the +12 volt pulse width modulator. C13 is charged from a voltage-controlled current source. The voltage at pin 5 of E3 is connected to the 5 volt reference. Thus, when the voltage across C13 reaches 5 volts (pin 6 of E3), the output of E3 pin 3 drops low, turning Q1 off and thereby turning Q8 on. Q7 and Q8 are turned off simultaneously when Q2 is turned on. The pulse width that determines the length of time Q8 is on is determined by the rate of voltage rise on capacitor C13. The faster C13 charges, the longer Q8 conducts. The error voltage that determines the rate of rise on C13 is generated by error amplifier E2. The noninverting input of the error amplifier is referenced to D38, a 5.1 volt zener. The inverting input is divided up by R2 and R3 and senses the +12 volt output. Any difference creates an error signal on pin 6 of E2. This increase or decrease in voltage at pin 6 divided by R33 generates a proportional change in current through Q5, thereby changing the rate of voltage charge on capacitor C13. As described above, the change in rate of charge affects the pulse width.

R4, C1, and R5 are the compensating components of error amplifier E2. D1 and D2 are antisaturating diodes. R6 limits the base drive and R7 and C3 are a speed-up circuit to turn Q1 on and off.

6.9.5 Power Supply Specifications

6.9.5.1 Input Specifications

Voltage

Single-phase, two-wire

90–128 Vrms (switch-selected).
180–256 Vrms.

Frequency	47–63 Hz.
Current	2.2 Arms maximum at 115 Vrms. 1.1 Arms maximum at 230 Vrms.
Input power	250 VA apparent 150 W maximum.
Power factor	Ratio of input power to apparent power is greater than 0.6 at full load and minimum input voltage. The VT180 appears capacitive to the line.
Leakage current	When installed in a VT180 terminal, current to ground is 0.5 mA maximum. Each line to ground at 250 Vrms sine, 50 Hz.
Current limiting	When installed in video terminal, 3.0 A normal blow fuse.
Electrical magnetic interference susceptibility	
Conducted transients	Single voltage transient without causing system degradation: 600 V at 2.5 W/s maximum.
Single voltage transient, survival	1000 V at 2.5 W/s maximum.
Average transient power, survival	0.5 W maximum.
Conducted cw noise	Unit operates without error at conducted noise levels up to 10 kHz–30 MHz: 3 Vrms. RF field susceptibility: 10 kHz–30 MHz: 2 V/M; 30 MHz–1 GHz: 5 V/M with power supply installed in video terminal.
Power line disturbance	
Ride-through capability	The power supply provides a minimum of 20 ms ride-through during a power outage condition. Ride-through capability is at low line and full load. During this time, all power supply outputs must be within their specified limits.
Overvoltages	The power supply withstands an overvoltage of 110% of the maximum input voltage(s) specified in Paragraph 6.9.5.1 for one second without causing system degradation or damage.
Undervoltages, disturbances, and outages	The power supply is capable of withstanding undervoltage disturbance and power interruptions without physical damage.

Hi-pot

Input to frame for 1 min – 2.15 kV dc; input to output for 1 min – 2.5 kVrms.

Output specifications

General

The dc output distribution provides dc outputs. The dc distribution buses define dc output specifications. Distribution systems must be designed according to this document since no output voltage adjustments are provided.

Output power

+5 V at 1.5 A minimum to 11.0 A maximum.
+12 V at 1.0 A minimum to 2.75 A maximum.
–12 V at 0.0 A minimum to 0.5 A maximum.
–23 V at 10 mA.

+5 V Specifications

Total regulation

±5%

Static line regulation

±0.75%

Static load regulation

±2.0%

Long term stability

0.1% – 1000 hrs

Thermal drift

±0.025% – degrees C

Ripple

150 mV peak-to-peak for frequencies less than 66 kHz

Dynamic load regulation

±2.2% (see notes)

Noise

1% peak at frequencies greater than or equal to 100 kHz
(noise is superimposed on ripple)

–12 V Specifications

Total regulation

±5%

Static line regulation

±0.5%

Static load regulation

±1.0%

Long term stability

0.1% – 1000 hrs

Thermal drift

±0.025% – degrees C

Ripple

240 mV peak-to-peak for frequencies less than 66 kHz

Dynamic load regulation

±1.1% (see notes)

Noise

1% peak at frequencies greater than or equal to 100 kHz
(noise is superimposed on ripple)

–12 V Specifications

Total regulation	$\pm 5\%$
Static line regulation	$\pm 0.5\%$
Static load regulation	$\pm 1.0\%$
Long term stability	0.1% – 1000 hrs
Thermal drift	$\pm 0.025\%$ – degrees C
Ripple	240 mV peak-to-peak for frequencies less than 66 kHz
Dynamic load regulation	$\pm 1.1\%$ (see notes)
Noise	1% peak at frequencies greater than or equal to 100 kHz (noise is superimposed on ripple)

–23 V Specifications

Total regulation	$\pm 10\%$
Static line regulation	$\pm 2\%$
Ripple	500 mV peak-to-peak

NOTES

- 1. For all outputs, the long term stability and thermal drift specifications apply after a five minute minimum warmup, measured at the dc distribution buses with an averaging meter.**
- 2. Dynamic load regulation is measured in +25% load steps from a starting point of 75% of full load. Measurements are made at the power supply terminals.**
- 3. Zener diodes for –23 V supply are located at the load and not on the power supply.**

Ripple and noise	Ripple and noise must be measured with a wide band oscilloscope in the differential mode between ground and the output under test. The oscilloscope must be grounded so as to minimize spurious responses. The specification applies only to repetitive voltage variations that occur while operating with a constant input voltage and fixed load.
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Overload protection

+5 V output	Current limit with foldback. Limit point is 18 A maximum; foldback is 6.0 A maximum.
+12 V output	Current limit with foldback. Limit point is 6 A maximum; foldback is 3 A maximum.
−12 V	Internal current limit of the three-terminal regulator is per Digital specifications PS-19-12048-02.
−23 V	Current limited to less than 150 mA.
Voltage adjustments	None.
Weight	1.68 kg (3.7 lbs) maximum.

6.9.5.2 Cooling – Cooling is by natural convection. Adequate space must be provided around the supply to allow a free flow of air.

6.10 KEYBOARD DESCRIPTION

The VT180 keyboard is a typewriter-like array of momentary, normally-open switches. The array is mounted in a small case with a speaker for audio feedback and electronics for interfacing the array to the terminal. The keyboard connects to the terminal controller board through a three-conductor cable that plugs into the back of the terminal cabinet. The cable carries power, ground, and a complex bidirectional data and clock signal. The terminal sends the clock signal and a status word that controls the LED indicators, the bell, and the keyboard scan process. The keyboard sends the row and column address of each key that is pressed. The terminal's microprocessor then translates that address into an ASCII character and transmits it serially to the host through a UART or performs internal actions such as set-up and no scroll. Refer to Paragraph 6.5.8 for a discussion of UART principles.

This section describes the operation of the keyboard and its interface to the hardware and software in the terminal.

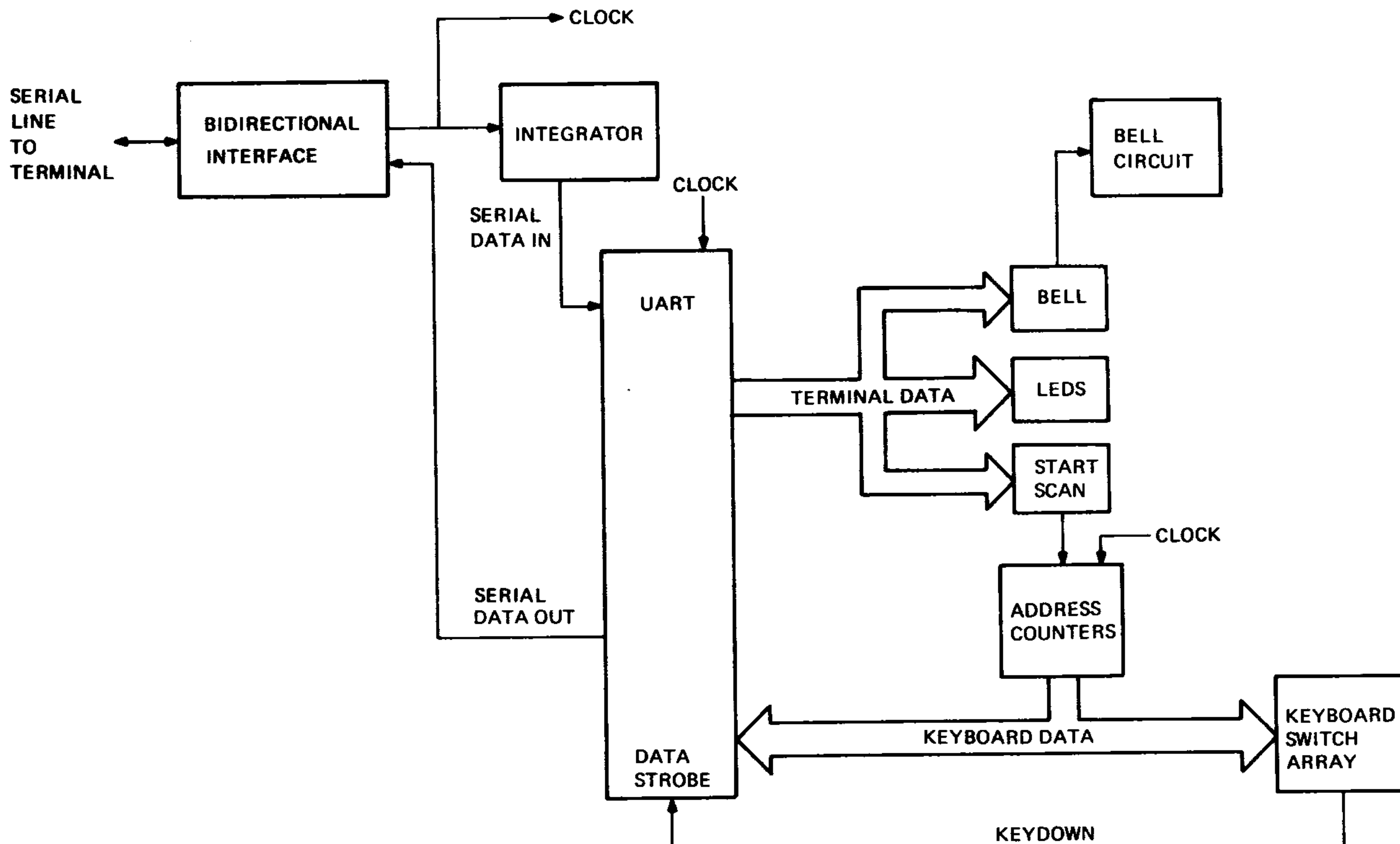
6.10.1 Keyboard Block Diagram

Figure 6-54 is the keyboard block diagram. The bidirectional interface separates incoming data from outgoing data on the single signal line. Incoming data from the terminal contains a clock that passes directly to the UART and the address counter circuit. Then the data and clock are integrated. The duty cycle encoded data becomes serial data. The UART deserializes the terminal data and produces an 8-bit parallel output. These bits control the bell and LEDs and start address scanning, depending on which bits were set by the terminal in the keyboard status byte.

The address counters start on command and send row and column addresses to the keyboard switch array. When an address matches a key that is down, the key down signal strobes that address into the UART. The UART serializes the address and the bidirectional interface sends it to the terminal.

6.10.2 Keyboard UARTs

Information is exchanged between the terminal and the keyboard in serial form. One start bit, eight data bits, and one stop bit are transmitted using a clock derived from the horizontal timing circuits in the terminal. Besides timing the serialization of data in the terminal, the clock is also transmitted to the keyboard to time its circuits. The terminal data is a status byte that controls the keyboard by commanding key scans and other functions.



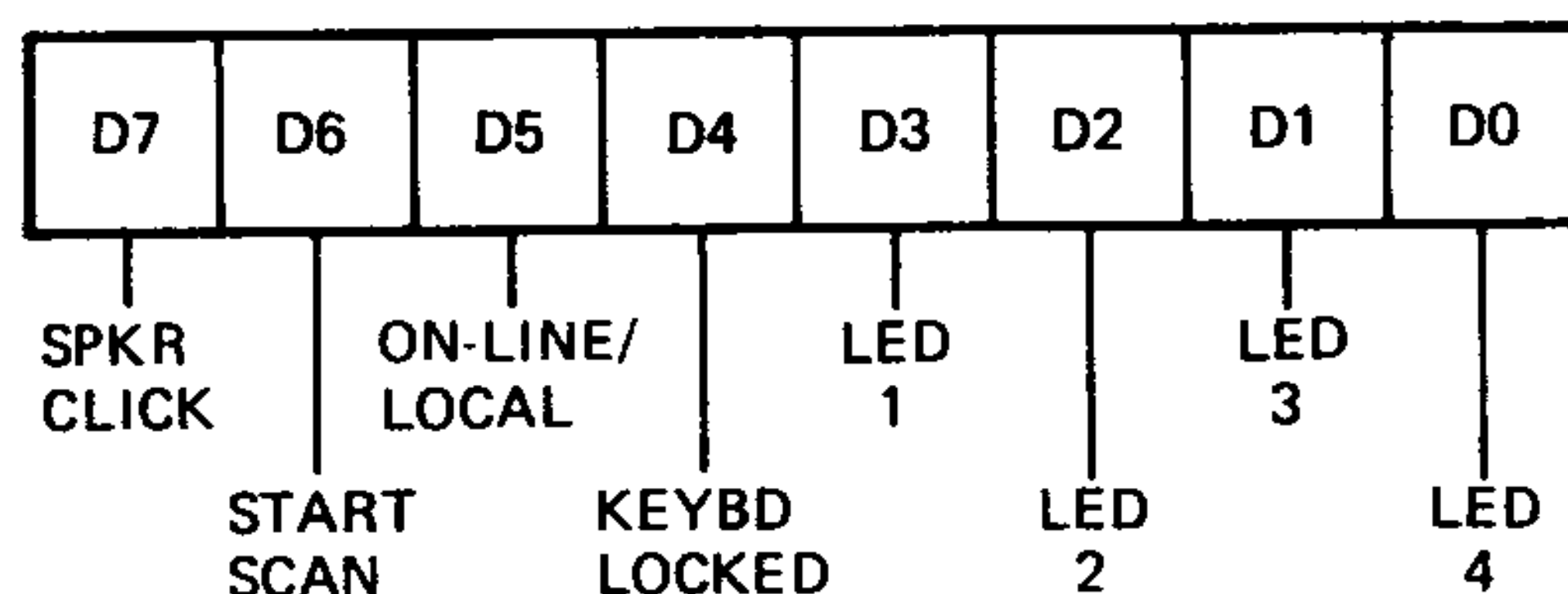
MR-8094

Figure 6-54 Keyboard Block Diagram

The keyboard transmits its data in the same format and with the same clock. Its data is the addresses of whatever keys are down during a scan. The last key address sent has the highest address possible and is always sent to indicate to the microprocessor in the terminal controller that the scan is complete.

6.10.3 Keyboard Status Byte

The terminal controls the keyboard through a status byte that it sends through the interface along with the keyboard clock. The first six bits of the 8-bit byte (Figure 6-55) control the on-line/local, keyboard locked, and four user-programmable LEDs on the keyboard. Every time the status byte is sent, it refreshes the LEDs even if no new action is being taken. The seventh bit is sent only once in a vertical interval and initiates the scanning process in the keyboard. The eighth bit, if sent only once, causes the keyboard speaker to click. (Keyclick is defeatable at set-up.) If the bit is sent approximately 200 times in a row for about a quarter second, it sounds a bell.



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Figure 6-55 Keyboard Status Byte

The operating clock for the keyboard interface comes from an address line in the video processor (LBA4). This signal has an average period of 7.945 microseconds. Each data byte is transmitted with one start bit and one stop bit, and each bit lasts 16 clock periods. The total time for each data byte is 160 times 7.945 or 1.27 milliseconds. Each time the transmit buffer empty flag on the terminal's UART gets set (when the current byte is being transmitted), the microprocessor loads another byte into the transmit buffer. In this way, the stream of status bytes to the keyboard is continuous.

6.10.4 Key Address Counter

Keyboard addresses are outputs from a counter that correspond to locations in a keyswitch matrix. The counter can address all locations in the matrix. If a keyswitch is closed, the counter output addressing that location is transmitted. The address counter is a pair of 4-bit binary counters arranged so that only the top seven bits go to the switch matrix. These outputs also connect directly to the UART transmit data inputs. The output of the first bit in the counter is a squarewave with a period equal to the amount of time that each key is sampled during a scan. Key down L appears at the input to flip-flop E6 when the counter reaches the address of a key that is pressed. Half a sample period later, the first counter bit clocks the key down signal through flip-flop E6. The half period delay allows any glitches in the address counter to settle before key down asserts data strobe. Data strobe loads the UART transmit buffer with the address count present at the data input at that moment. That address count represents the key that was down when key down was asserted.

The UART, which is double-buffered, deasserts transmit buffer empty while the transmit (outer) buffer is full. This stops the counter by blocking the clock at gate E4. As soon as the data moves into the inner shifting register, the transmit buffer empties, TBMT is asserted, and the count continues. In this way, any number of key addresses can be sent to the terminal. The time the scan takes to finish varies with the number of keys down. On the first address load, when transfer from the transmit buffer into the shifting register is immediate, the UART reasserts TBMT almost immediately. For address loads later in the scan, the UART deasserts TBMT for a longer period because an address that loads into the transmit buffer must wait with the counter stopped until the previous transmission is done. Because the transmission time is 160 counts and the complete address scan takes only 128 counts, there is a minimum wait of 32 counts or about 20 percent of a character transmission time between the scan of address 7FH and the transmission of address 7FH if the first key in the scan was down. (Refer to Figure 6-56.)

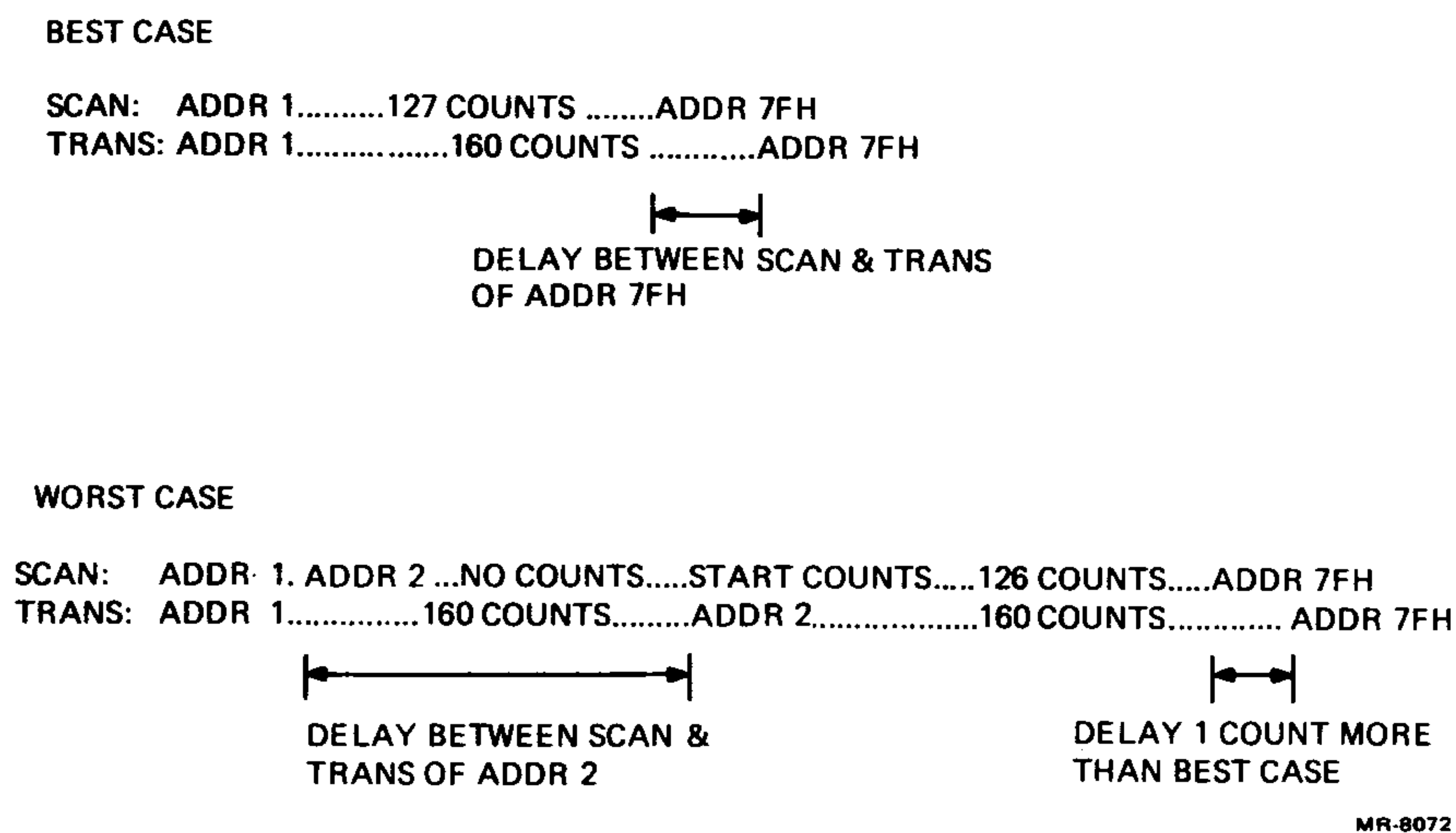


Figure 6-56 Key Address Transmission Delays

Because it is hardwired, the highest address (7FH) always asserts key down and gets transmitted, indicating end of scan to the terminal. The highest bit also clocks flip-flop E3, which clears the counters and stops the count. This is the only way that the scan is terminated. The scan begins again when the terminal sends the start scan bit in the status byte to the keyboard. When the data arrives, the UART asserts its data available flag. On the next clock transition, flip-flop E6 passes a short, clock-synchronized data available pulse to gate E5, resetting the flag in the process. E5 combines the data available pulse with the start scan bit, if present, to clear E3 and allow the count to begin.

After the terminal starts the scan, it waits for the 7FH address and then for a vertical interrupt (a synchronizing signal) before it will start the scan again. If there are a lot of keys down, the scan may take more than one vertical interval to finish. The keyboard ignores further requests to scan until the current scan is complete.

Here is a formula that estimates the delay between the time that the terminal asserts the start scan bit at its UART and the time that the terminal UART asserts data available upon receiving the final address 7FH. The clock driving the address counter and UART has a period of $7.945\ \mu\text{s}$. The serial transmission of an address takes 160 clock periods (16 clocks per bit, 8 data bits, 1 start and 1 stop bit).

160	start scan command word to keyboard
+ m	counts to first key
+ $n \times 160$	for n keys down
+ 160	transmission of 7FH
Total $\times 7.945 = \text{microseconds}$	

For example, suppose that one key, #24, is down.

160	start scan command word to keyboard
+ 24	counts
+160	transmission of key #24 address
+160	transmission of 7FH
$504 \times 7.945 = 4004\ \text{microseconds (} 4.0\ \mu\text{s)}$	

6.10.5 Key Scanning and Address Formation

The keyboard is an array of contact pairs arranged in 16 rows and 8 columns (Figure 6-57). One side of each pair is connected to all the others in its column and each column connects to +5 volts through a resistor. Each of the eight columns also connects to an input on the eight-to-one multiplexer E14. The other side of each contact pair connects to all the others in its row and to an output on one of the one-to-eight demultiplexers E11 and E13. The seven outputs of the keyboard scan counter control the multiplexer and demultiplexers. The rows are selected by the lower four bits and the columns by the upper three.

A low input to the selected column line on the multiplexer causes a key down L signal. If a key is pressed when the row and column address is not on its position, the unselected demultiplexer line is high and there is no change in level across the contacts. If the demultiplexer line is selected, it is low and the closed contact pulls the column low through the resistor. Each column is scanned top to bottom as the low four address lines count; then the next column is selected and scanned. The complete keyboard scan takes about 1 millisecond when no keys are down.

The last row and column position (address 7FH) is wired to always indicate key down. This value indicates to the terminal that the scan is ended.

		COLUMNS							MSD
		7	6	5	4	3	2	1	0
ROWS	LSD	9	.	8	7	↑	←	→	ALWAYS OPEN
	0	3	,	ENTER	PF4	PF3			
	1	6	5	2	PF2	PF1	↓		
	2	-	4	1	0	BACK-SPACE	BREAK		DELETE
	3		RETURN		LINE FEED	+ =	~ \	}]	RETURN
	4	? /	> .	" ,	 \ /	) 0	_	{ [	P
	5	M	< ,	: ;	L	* 8	(9		O
	6	SPACE BAR	N	J	K	^ 6	& 7	U	Y
	7	V	B	H	G	% 5	\$ 4	R	T
	8	C	X	D	F	@ 2	# £ 3	E	W
	9	Z	NO SCROLL	S	A	TAB	ESC	! 1	Q
	A	SET-UP							
	B	CTRL							
	C	SHIFT							
	D	CAPS LOCK							
	E	ALWAYS CLOSED							
	F								

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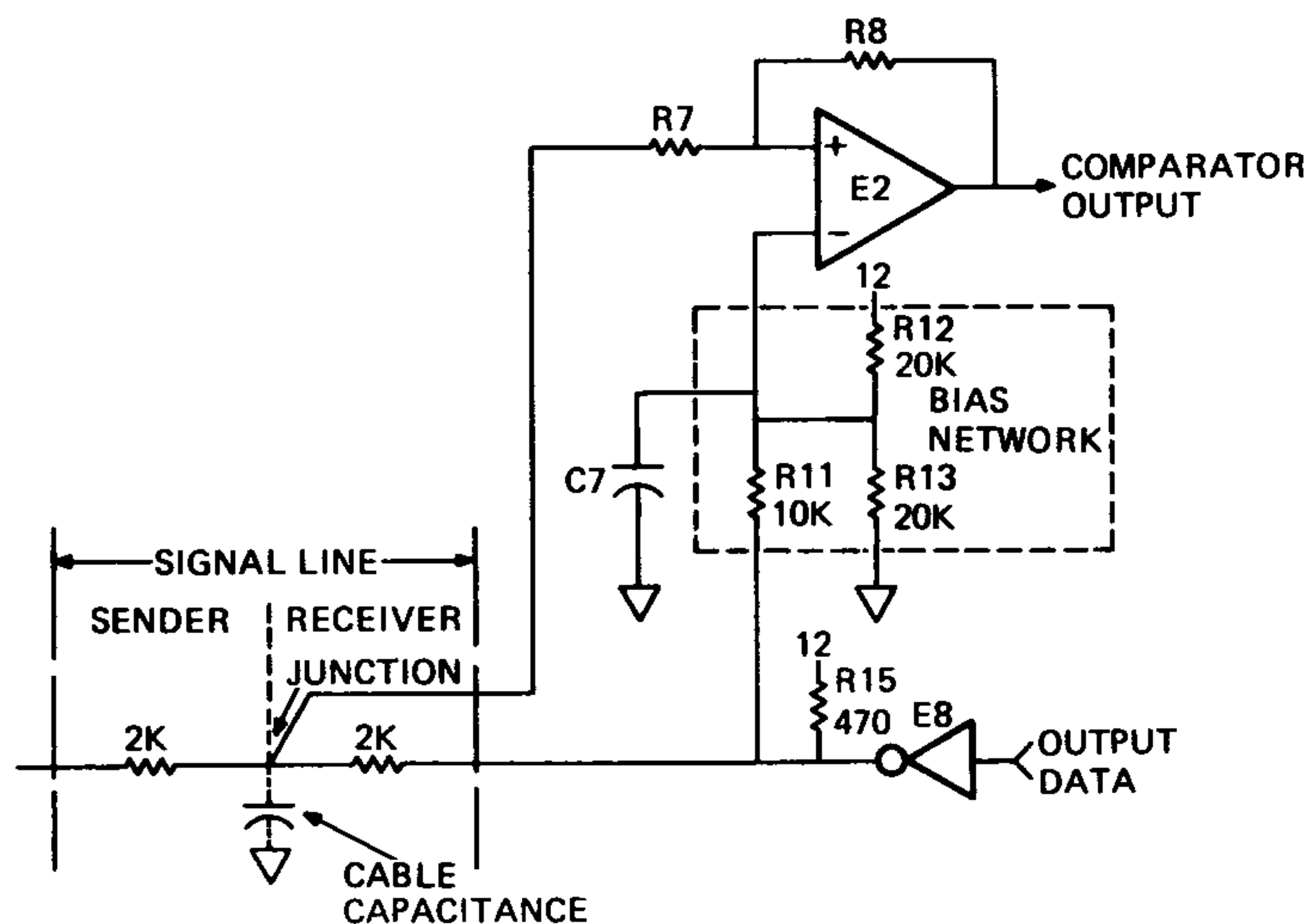
Figure 6-57 Keyboard Switch Array

6.10.6 Bidirectional Interface Operation

The terminal sends data and clocks to the keyboard; the keyboard sends data only. Transmission is asynchronous, full duplex, serial, 8-bit data with 1 start bit and 1 stop bit over a single signal line. Four states can exist on the line, representing the two signal states from each end of the line.

Both signals may coexist on the same wire, originate at opposite ends, and simultaneously communicate provided that sensing resistors are put at each end. The interface works by observing the voltage variations on its input (across the sensing resistor) while biasing the input in an opposite direction with its own output signals so that only input variations can cause enough change to exceed the threshold of detection.

6.10.6.1 Interface Line – Refer to the keyboard interface schematic, Figure 6-58. If one side of the line is at +12 volts and the other is at ground, then by Ohm's Law, the center of the two equal resistors will be at $V/2 = 6$ volts. If both sides are at 0 or 12, the center will be identically at 0 or 12. Thus the signal line can either have no current flow but with the junction of the two resistors at either 0 or 12 volts, or the junction can be at 6 volts with current flow to the left or to the right, thereby representing the four required states.



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Figure 6-58 Keyboard Interface Circuit

6.10.6.2 Receiving Side – The receiving side of the keyboard interface separates the incoming signal from its own output by delivering a sample of its output to the inverting input of a comparator. Refer back to Figure 6-58. This provides an additional input for the comparator, which compensates for the variation that occurs on the noninverting input at the same time that the output changes. R12 and R13 (both approximately 20 kilohm) and R11 (10 kilohm) are a divider providing bias to the comparator. If E8 (an open collector driver) is off (high), then the end of R11 connected to E8 is essentially at +12 volts through R15 (470). The R11, R12, R13 divider outputs 9 volts at the junction of the three resistors. If E8 is on (low), the end of R11 connected to the output of E8 is at ground, and the divider outputs 3 volts.

Meanwhile, the signal from the other end of the signal line is admitted to the noninverting input of the comparator through a resistor (R7) whose value is small compared to the comparator's high input impedance. The positive feedback resistor R8 provides a small amount of hysteresis to improve the circuit's noise immunity.

For the case where the junction is at 12 volts, there is no ambiguity about what signal the sender is sending. The comparator must produce a high output because the sender is outputting a high level. (The receiver is

also sending a high level but no distinction between the two needs to be made.) The bias network presents a 9 volt signal to the inverting input, so the comparator sees a +3 volt difference and goes high.

For the case where the junction between the sender and the receiver is at 0 volts, there is again no ambiguity. The comparator must produce a low output because both sender and receiver are outputting low levels. The bias network presents a 3 volt signal to the inverting input, so the comparator sees a -3 volt difference and goes low.

For the case where the junction is at 6 volts, either end could be the high or low sender. The decision is made at each end by each circuit examining its own output to decide whether it or the other end is sending a particular level. If the sending end is at 0, the noninverting input sees 6 volts. The receiving end is outputting 12 volts, and the network outputs 9 volts to the inverting input. The comparator sees a difference of -3 volts and outputs low in recognition of the low level at the sending end. If the sending end is at +12, the noninverting input sees 6 volts. The receiving end is outputting 0 volts, and the network outputs 3 volts to the inverting input. The comparator sees a difference of +3 volts and outputs high in recognition of the high level at the sending end.

Table 6-37 summarizes the effects of the various signals.

Table 6-37 Keyboard Receiver Signals

Sending End	Receiving End	Noninverted Input (Junction)	Inverted Input	Difference	Output
0	0	0	3	-3	0
0	12	6	9	-3	0
12	0	6	3	+3	5
12	12	12	9	+3	5

Keyboard Cable Compensation

C7 compensates the circuit for the capacitance of the cable. If C7 were not present, the output of the comparator would glitch when the output driver on the same end of the line changed state. This would be caused by the output signal propagating immediately to the inverting input of the comparator but being delayed (by the RC time constant of the line) to the noninverting input. C7 is chosen so that the time constant of the line is the same at both inputs. Because the resistance seen at the middle of the line is approximately 1000 ohms (two 2 kilohm resistors in parallel) and the resistance seen at the inverting input is approximately 5000 ohms (one 10 kilohm and two 20 kilohm resistors in parallel), C7 is about one-fifth of the cable capacitance. The value is not critical because the ratio of the two time constants can be as large as two and still provide acceptable noise immunity.

6.10.6.3 Terminal Data Encoding – The keyboard requires a clock for its operation and is provided with one by the terminal controller side of the interface. To transmit a clock independently of data on the same wire, the terminal side of the interface generates a clock signal within which data is encoded as a pulse width modulation. The terminal circuit produces a 75 percent high pulse width output for the mark state. Data transmission causes the clock output to switch between 75 and 25 percent pulse width (duty cycle).

Figure 6-59 is a timing diagram that illustrates the formation of the pulse width modulation. Three nand gates, I, II, and III, combine three signals, data, LBA 3, and inverted (not) LBA 4. The three gate outputs are wire-ANDed so that all three must have high outputs to produce a high to the out inverter, which drives the terminal's end of the bidirectional interface. The timing is not precisely correct in this drawing because the LBA signals, addresses to the line buffer in the video processor, are not pure squarewaves and have variations in their periods (see Paragraph 6.5.12.1). These variations give the keyboard signal the appearance of clustering in groups of four, but they do not affect the operation of the circuit.

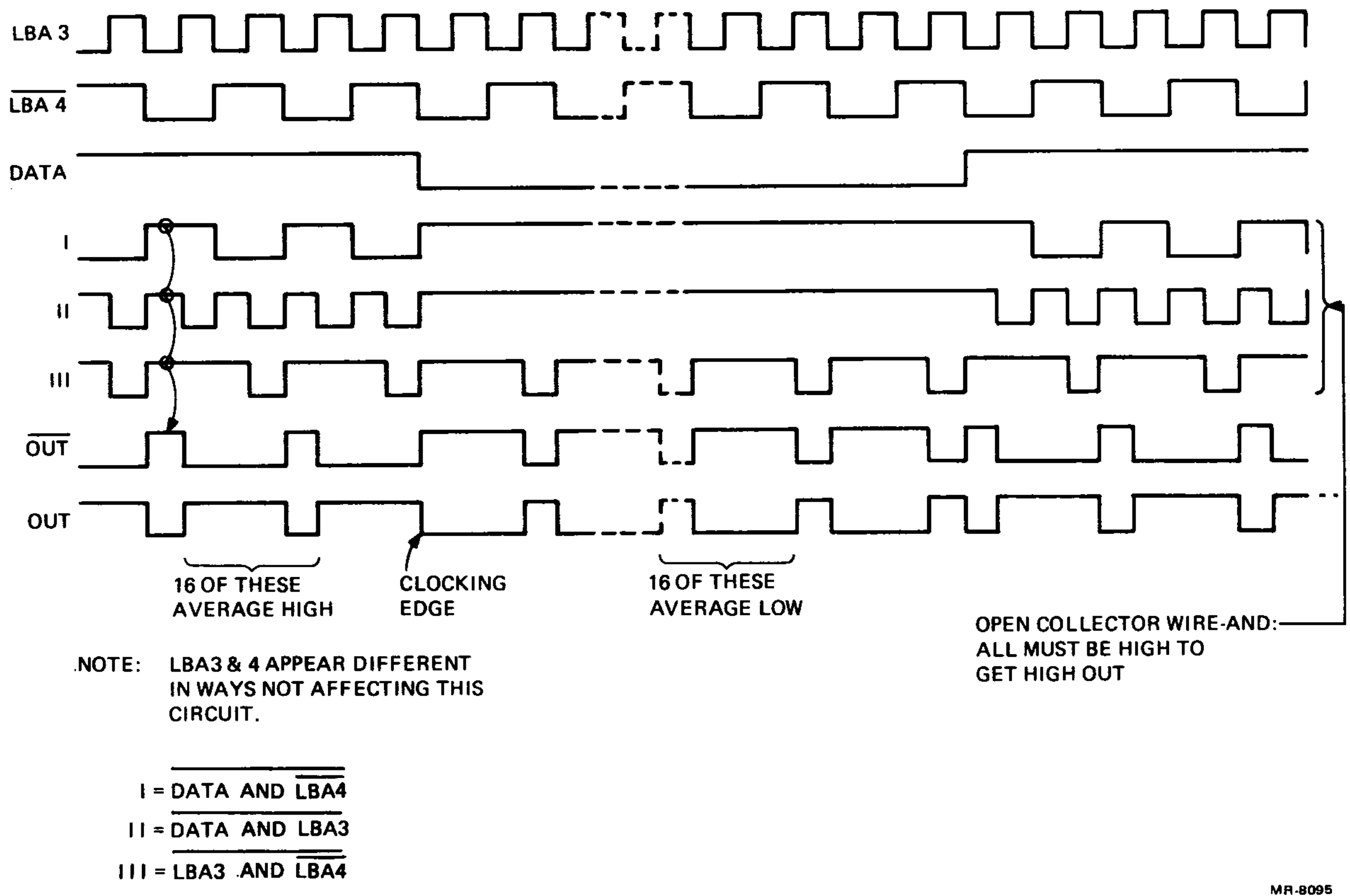


Figure 6-59 Encoding of Terminal Data and Clock

The negative transition of each output pulse occurs at the clock interval regardless of the presence of data. This transition is therefore the reference point for the keyboard clock at the receiving end.

6.10.6.4 Combined Interface Signal – Figure 6-60 illustrates the four possible conditions on the interface line when the effect of the clock is included. Figure 6-61 shows all four states and the transitions between each of them. Two series sensing resistors in the interface circuit divide the signal in half at the wire. Therefore, although the drivers swing 12 volts at each end, the figures show only 6 volt variations.

6.10.6.5 Decoding of Data from Terminal – The keyboard recovers the modulated clock signal sent by the terminal but must also separate the data from the clock. The signal is sent directly to the UART and address counter circuits as a clock. The negative edge of the clock occurs at a fixed interval while the positive edge varies according to the duty cycle modulation. The keyboard circuits use the negative edge and ignore the variable pulse width.

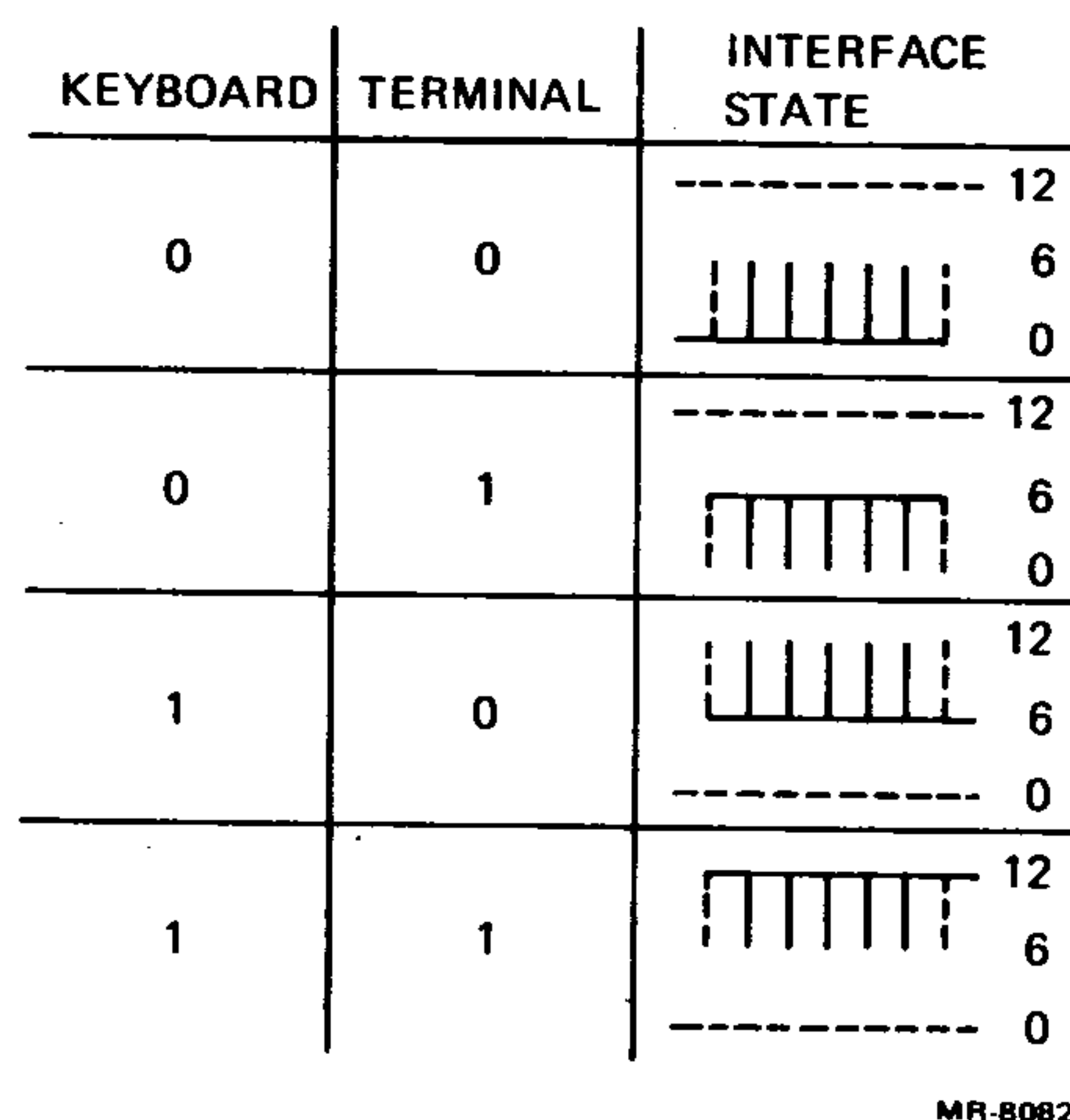


Figure 6-60 Four Keyboard Interface States

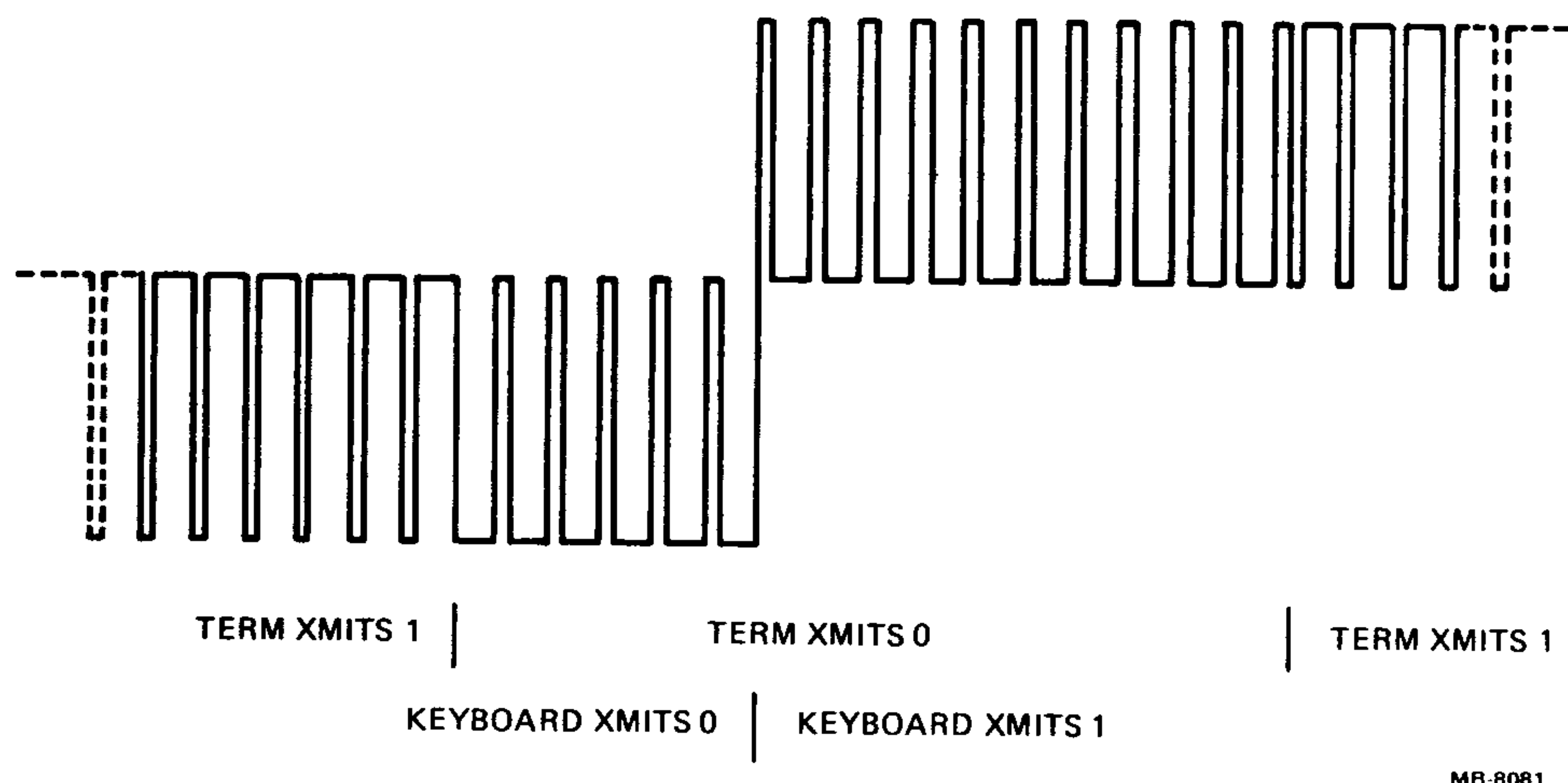


Figure 6-61 Keyboard Interface Signal

Data is extracted from the combined clock-data by a simple resistor-capacitor filter on one input to a comparator. The other comparator input is referred to one-half the power supply. Because the duty cycle of incoming data is either $\frac{1}{4}$ or $\frac{3}{4}$, the capacitor charges to that proportion of the supply voltage over the 16 clock periods of each bit. The comparator switches when the capacitor voltage rises or falls past the reference value. The short duty cycle of zeros averages to a low voltage that holds the comparator output low. The long duty cycle of ones averages to a high voltage and switches the comparator to a high state. The comparator output goes to the serial data input of the UART where it is deserialized. When all ten bits of a transmitted character are loaded into the UART, it asserts data available. This signal enables the bell and scan start if the appropriate bits were set in the byte. The LED bits remain latched at the parallel output of the UART until the next command byte arrives.

6.10.6.6 Keyboard Output – The keyboard UART serial output goes directly to an open collector driver that swings its end of the bidirectional signal line between 0 and +12 volts. This is shown as E8 and R15 in Figure 6-58. The circuit is identical at both ends of the interface.

6.10.7 Bell

The keyclick/bell circuit provides audio feedback and attention signals for the user. A bit in the keyboard status word controls the bell. Refer to Figure 6-62 for the circuit. Capacitor C8 charges to +5 volts through resistor R16. The speaker connects between the capacitor and the collectors of the transistors in E1. When a single status word contains the bell bit, flip-flop E3 toggles and turns on E1. C8 discharges through the speaker and E1, generating a click. When the voltage on C8 falls low enough, it clears E3. E1 turns off and C8 charges up for the next click. The value of C8 is selected to determine the volume of the click. D8 protects the transistors from inductive spikes from the speaker.

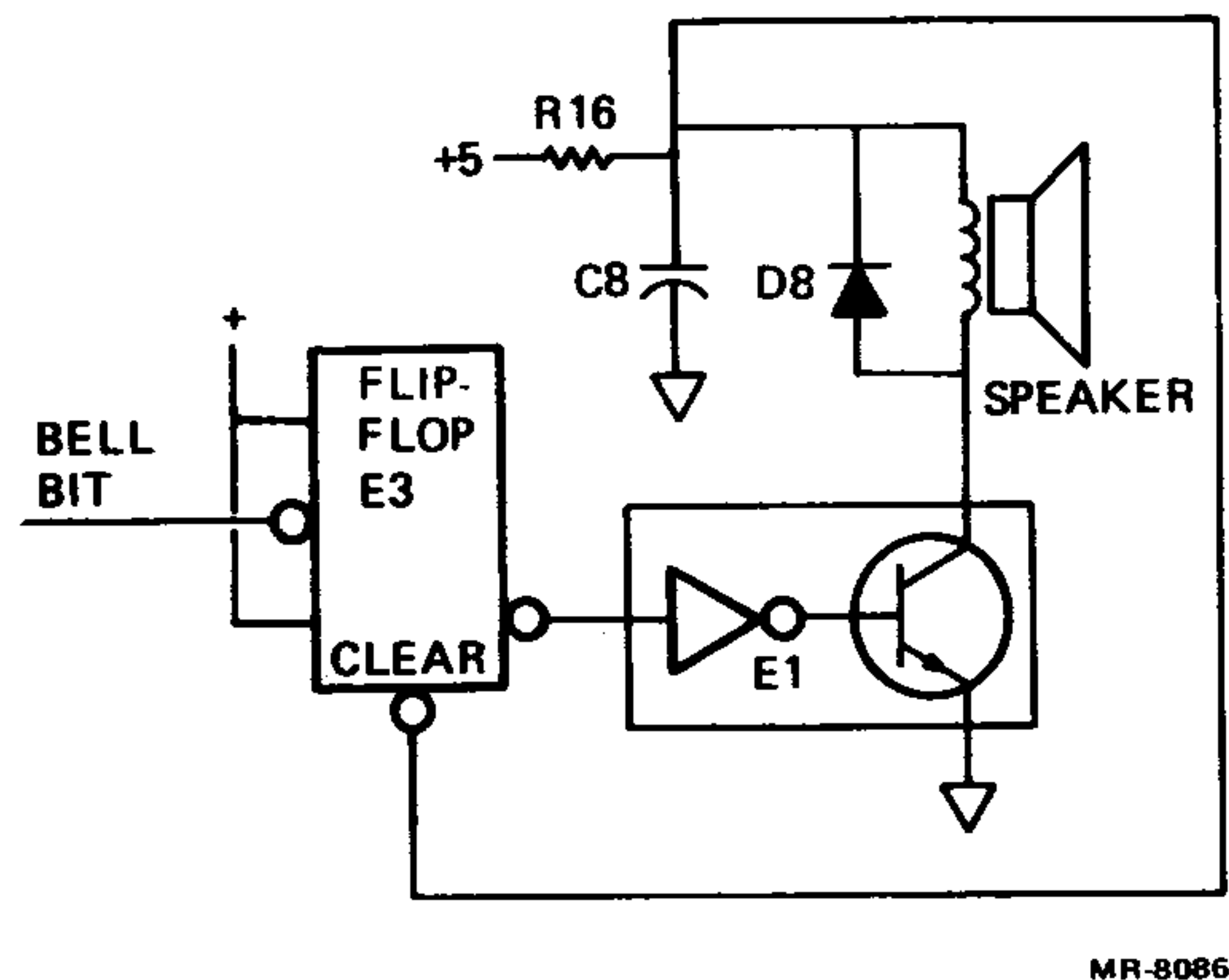


Figure 6-62 Bell Circuit

If the bell bit is set for many words in succession, the UART latch holds the data output constant. A one clock period pulse from the data available flip-flop E6 gates the bell bit through E5 to form a clock to E3. As C8 discharges through the speaker and E1, E3 clears itself, turning E1 off. Then C8 charges up again until the next data available pulse clocks E3 on again to repeat the discharge cycle. C8 discharges fast enough so each data available pulse (which arrives every 1.28 ms) triggers a cycle, allowing the circuit to produce an 800 hertz tone. Bell is generated by setting the bell bit for 0.25 seconds (about 200 status words). Each cycle of the tone is at a reduced amplitude compared with the single keyclick because R16 is selected to limit C8's charging rate. The overall effect of the tone on the ear is that of a beep.

6.10.8 Keyboard Interrupt Routine

When the microprocessor on the terminal controller module responds to an interrupt from the keyboard UART and reads a key address from the UART data output, it immediately range tests the address. The function key addresses are all above the regular key addresses, with set-up the lowest at 7BH and the always closed key at 7FH. An incoming function key address causes a bit to be set in a flag byte called keys (Figure 6-63).

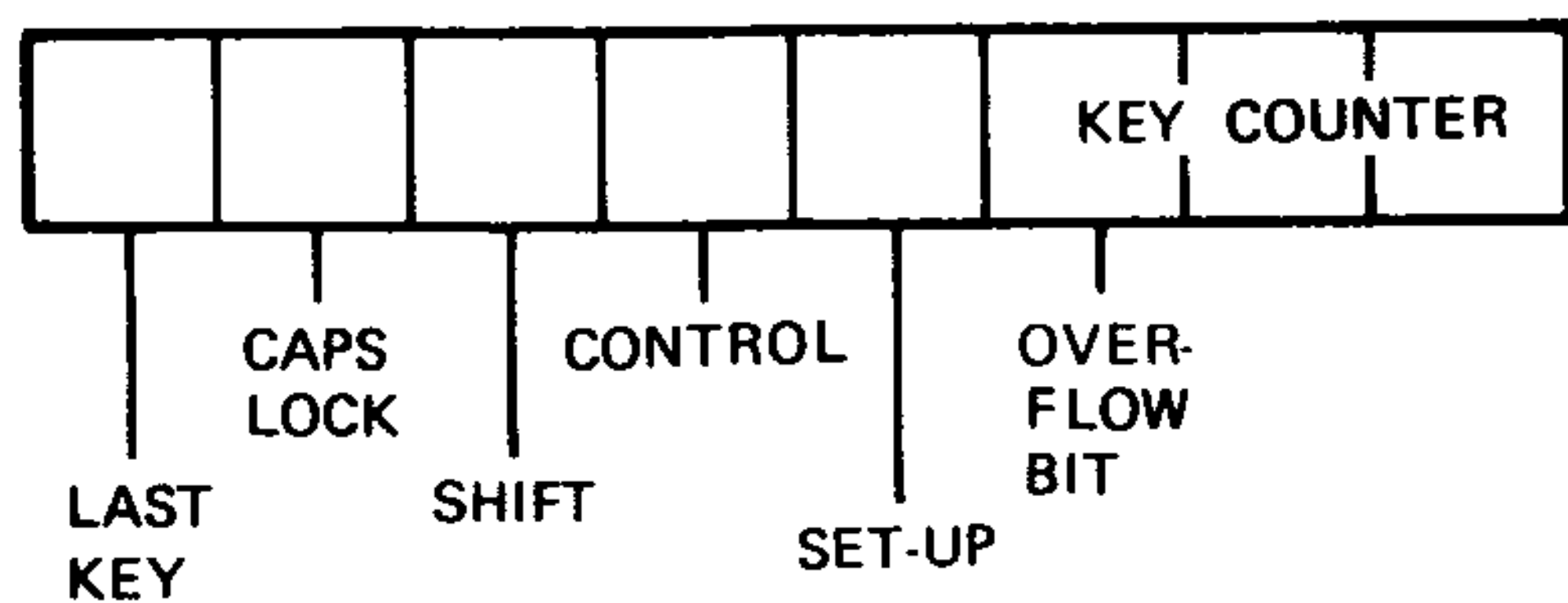


Figure 6-63 Keys Flag Byte

When a key address below the function range arrives, the microprocessor checks the low three bits in keys for the key count. If the count is less than three, the key address is stored in a three place new key address buffer and the counter is incremented. If the count is already three, the counter is incremented but the key address is discarded.

6.10.9 Logical Keyboard Processor

The logical keyboard processor is that portion of the operating firmware that manages the interpretation and transmission of keyboard data. It consists of several processes.

6.10.9.1 Key Recognition – For a key to be recognized as a new key, it must not have been down in the scan before entry is accepted. The microprocessor checks each key's history at each scan. If a key was down during the last scan, it is old and is not entered. Only new keys, those not previously seen, are entered. This system allows a key to be held down without being continuously entered at each scan. (This process and auto repeat are discussed later.)

If a key is detected as down for the first time in a while, the microprocessor assumes that it has been pressed. During the scan when the key is first down, the contacts may bounce for several milliseconds. The time window when the contact is scanned is very short. If the contact happens to be bouncing open during that interval, it is not detected in that scan but the time between scans is long so it is finished bouncing by the next scan and is detected normally. If the contact happens to be closed for the first scan while still bouncing, it is detected. It is also detected on the next scan after it has stopping bouncing but now it is an old key and is not reentered.

When the microprocessor is free to perform its background routines, it processes the results of the last keyboard scan. First it checks the high bit of the key's byte to see if the scan is finished. If it is not, the microprocessor continues with other work (exits). If it is , the microprocessor checks the key counter overflow bit representing four or more keys sent in the scan. If the bit is set, the microprocessor clears the new key address buffer and exits.

If the overflow bit is not set, the first key is taken from the new key address buffer and tested. If it is either the SET-UP or NO SCROLL key, the microprocessor acts on it immediately and branches to the appropriate routine. It then returns to the keyboard process.

Another three place buffer contains the keys from the last scan. The microprocessor compares the three new keys with those in the old key buffer. If an old key is not in the new key address buffer, that key is cleared from the old key buffer. New keys then go into the old key buffer. Each key address is only seven bits long, so the high bit in each key entry is used to indicate how long that entry has been in the buffer. If a key is new, the bit is set to 0. This means that the microprocessor has only seen the key once. If the key appears in the new key address buffer on the next scan, the microprocessor sets the high bit to 1, converts the key address to an ASCII code, and sends it to the keycode buffer. Only one key is converted and sent in each cycle of the logical keyboard processor routine. Since the set bit indicates that the key has been sent, in the next cycle that key will be ignored and the next key will be processed.

6.10.9.2 Key Rollover – Key rollover means that more than one key can be down at the same time and be accepted. Normally the VT100 accepts three-key rollover. If the keys were pressed during different keyboard scans, they will be accepted in the order in which they were pressed. If they were all pressed during the same keyboard scan, they will be accepted in the order of their addresses.

Certain conditions will limit the rollover to only two keys. The 2.5 key rollover specification reflects the presence of these conditions. Because there are no isolating diodes in the switch matrix, certain patterns of contact closure can produce false key down indications. Specifically, three switches closed in three corners of a rectangular pattern, as in Figure 6-64, will cause a fourth apparent key address to be sent to the terminal. (Refer back to Figure 6-56 to see how the pattern fits into the row-column configuration.) For

this reason, although any number of key addresses may be sent by the keyboard during a scan, no more than three may be sent if any are to be accepted. If four or more appear, the terminal ignores all of them and waits for a scan with only three. The special function keys (SHIFT, CAPS LOCK, CONTROL, SET-UP) are in a part of the matrix where there is no pattern sensitivity and no ambiguity. They all are accepted in the same scan with the regular keys and are not counted in the three-key maximum.

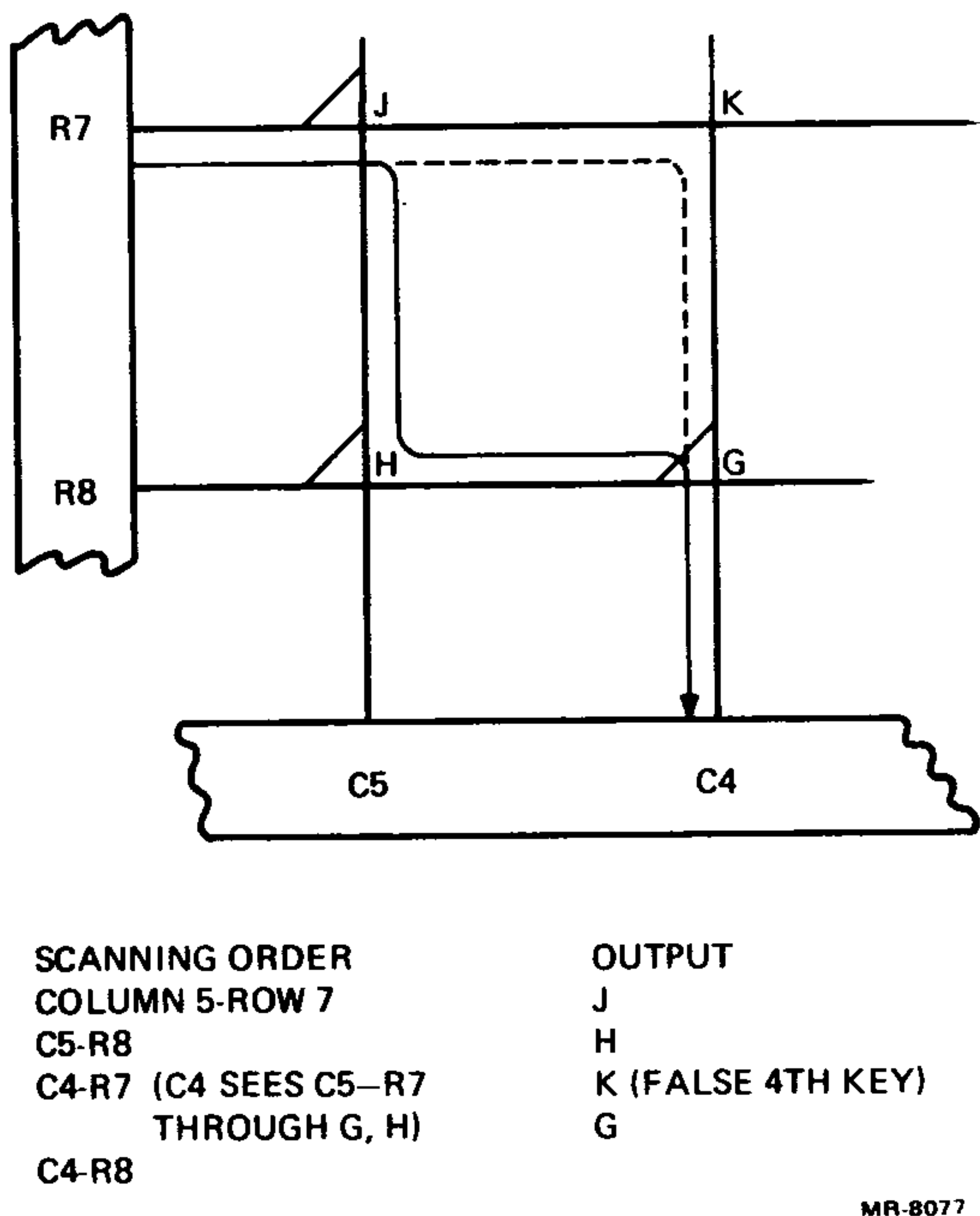


Figure 6-64 Sneak Path

The sneak path problem is also the reason that the keyboard processor looks for the appearance of a key in two successive scans. In Figure 6-64, the keys are scanned in the order J, H, K, G. Normally, the keyboard processor counts the number of keys in a scan and ignores all of them if the count is over three, as it is in this case. But it is possible for a user to briefly press keys J, H, and G and then release G before the scan is completed. Then the keyboard processor might see J, H, the false key K, and, because G was lifted just before it was scanned, register only three keys. One key would be false, but with a count of only three, all would be accepted. To prevent this, the keyboard processor looks for the same keys two scans in a row. Because the G key is released, the K key does not appear in the second scan, and only J and H appear and are accepted by the keyboard processor.

6.10.9.3 Generation of Codes – Because the keys are essentially randomly ordered with respect to the ASCII standard, the program ROM includes several look-up tables that assist in the generation of ASCII codes. Most keys convert directly from an address to an ASCII code. The codes for alphabetic keys with SHIFT or CAPS LOCK down are formed from the tables with bit 5 forced to 0 to produce uppercase alphabetic codes. Holding down the control key when another key is pressed causes another table look-up.

If the key is in the table of valid control codes, that keycode is changed by forcing bits 5 and 6 to 0. For example, the ASCII code for the letter g is 67H. Holding down the control key and typing G transmits the ASCII code 07H.

	B7	B6	B5	B4	B3	B2	B1	B0
Normal code	x	1	1	0	0	1	1	1
Control code	x	0	0	0	0	1	1	1
Shift code	x	1	0	0	0	1	1	1

Nonalphabetic keys have a second look-up table that provides the shifted code given the unshifted code. CAPS LOCK performs the shift function only on alphabetic codes, leaving the nonalphabetic to be performed with an extra shifting action. If a key that does not make a standard control code is pressed with CTRL, it is not sent.

6.10.9.4 Keyboard Transmit Buffer – Some keys generate three byte ASCII codes. For example, when the auxiliary keypad is in alternate mode, it transmits escape sequences that a system can be programmed to interpret in a special way. Cursor control keys also send escape sequences that the operator can use to control the cursor position. To store the codes that might be generated by three simultaneous keys, a 9-byte buffer is provided for the communications port. If the buffer fills up, the keyboard is locked and the appropriate LED lights. When a key is about to be converted to ASCII and stored in the buffer, the microprocessor checks the buffer to see if there is room. Since any key might produce three bytes of code, the microprocessor must be sure that there are at least three places available in the buffer. If six 1-byte keys have been sent, the next 1-byte key leaves only two places. Therefore, the keyboard locks with only seven places filled in the buffer.

6.10.9.5 Auto Repeat – If only one key is in the old key buffer (in the logical processor) and if it appears continuously, it may be a candidate for auto-repeating. A key with control cannot repeat, and a nonrepeat table contains a few keys that do not repeat. These are SET-UP, NO SCROLL, ESCAPE, RETURN, BREAK, and ENTER.

A countdown timer gets loaded with a value each time the buffer changes. When there is no change for a while, the timer decrements to zero. This takes about one-half a second. Then the key is sent to the keyboard buffer a second time and the timer is loaded with a smaller value. This time the count lasts about one thirtieth of a second. The key is sent and the timer reset the same way until the key is lifted or another key is pressed while the first is still down. If the second key is lifted, the count continues at the fast rate. The timer is decremented every time a status byte is sent to the keyboard (every 1.27 ms).