DEC-11-HTCB-D

TC11
DECtape system manual

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The material in this manual is for informational purposes and is subject to change without notice.

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FOREWORD

This manual provides the information necessary to operate the TC11 DECtape System. It also provides the theory of operation and logic diagrams necessary to understand and maintain the TC11 Controller.

This manual and the *TU56 DECtape Transport Manual* (DEC-00-HRTA-D) must be used together for a complete understanding of the entire TC11 System. The prime subject matter of this manual is the TC11 Controller and the DECtape magnetic tape; the prime subject matter of the TU56 manual is the tape transport. In addition, this manual serves as an overall system operating guide.

Table 1 indicates the coverage in the two manuals, and Table 2 lists related PDP-11 documents that are applicable to the TC11 DECtape System.

Table 1
TC11 System Manuals

Title	Number	Coverage
TC11 DECtape System	DEC-11-HTCA-D	**Overall System** – description, installation, operation, programming, and preventive maintenance. **TC11 Controller** – detailed theory of operation and logic diagrams. **DECtape Magnetic Tape** – detailed description of tape format.
TU56 DECtape Transport	DEC-00-HRTA-D	**Tape Transport** – description and installation; detailed theory of operation; logic diagrams; maintenance.

Table 2
Applicable Documents

Title	Number	Coverage
Unibus Interface Manual, Second Edition	DEC-11-HIAB-D	Provides detailed theory, flow, and logic descriptions of the Unibus and external device logic. Includes detailed discussions of the following modules used in the TC11 Controller: M105 Address Selector M782 Interrupt Control M783 Unibus Transmitter M784 Unibus Receiver

Table 2 (Cont)
Applicable Documents

Title	Number	Coverage
Unibus Interface Manual, Second Edition (cont)		M795 Word Count and Bus Address Register M796 Unibus Master Control M798 Unibus Drivers
TU56 DECtape Transport	DEC-00-HRTA-D	Provides detailed theory, operation, maintenance, and logic diagrams for the tape transport.
PDP-11/20 System (7-volume series)	DEC-11-HR1B-D through DEC-11-HR7B-D	Provide detailed theory of operation, flow, logic diagrams, operation, installation, and maintenance for components of the PDP-11 System including processor, memory, console, and power supply.
PDP-11 Handbook	Second Edition, 1970	A general handbook that provides discussions of addressing modes, the overall PDP-11 System, and the basic instruction set from a programming point of view. Includes some interface and installation information.
Logic Handbook	DEC, 1970	Presents functions and specifications of the M-Series logic modules, accessories, and connectors used in the TC11 Controller and the TU56 Tape Transport. Includes other types of logic produced by DEC but not used with PDP-11 devices.
Paper-Tape Software Programming Handbook	DEC-11-GGPB-D	Provides a detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs; input/output programming; and the floating-point and math package.

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The TC11 DECtape System is a high-speed magnetic tape handling system designed to interface with the PDP-11 family of processors and peripherals to provide storage of large amounts of digital information. The system performs data acquisition, storage and retrieval, merging, sorting, and duplication operations for business, research, education, and manufacturing applications.

The basic TC11 System consists of three distinct components:

TU56 Tape Transport – a dual-unit, bidirectional magnetic tape handling device that reads and/or writes information on magnetic tape at fixed positions. Uses redundant recording of each character bit on nonadjacent tracks to minimize bit dropout and skew errors.

Up to three additional TU56 transports can be added to each basic system.

TC11 Controller – an interface between the tape unit and the PDP-11 Unibus. Controls information transfers between the transport and other devices in a PDP-11 System. One controller services up to four transports (up to eight tape drives).

Also referred to as "control unit", "interface", or "DECtape control"

DECtape Magnetic Tape – the recording medium used for data storage. Reel-mounted magnetic tape that is formatted to permit read/write operations in either direction; error checking; block identification; and timing control.

1.2 GENERAL DESCRIPTION

The TC11 DECtape System is a magnetic tape storage facility consisting of a TC11 Controller and up to four TU56 DECtape transports (8 tape drives). The system stores information at fixed positions on magnetic tape, in the same manner as magnetic disk or drum storage devices, rather than at unknown or variable positions as in the case of conventional magnetic tape systems. This recording method permits replacement of blocks of data on tape in an ordered fashion without disturbing other previously recorded information. Specifically, during writing of information on the tape, the system reads format (mark) and timing data from the tape and uses this data to determine the exact position at which to record the information to be written. Similarly, during reading, the same mark and timing information is used to locate data to be played back from the tape.

The TC11 DECtape System has a number of features that improve its reliability and make it exceptionally useful for program updating and editing applications. These features are:

a. phase (polarity-sensed) recording on redundant tracks;

b. bidirectional reading and writing;

c. a simple mechanical mechanism that uses aerodynamically-lubricated tape guides (the tape floats on air and never touches any metal surface).

The three major functional components of a TC11 System are:

a. the TU56 Transport,

b. the TC11 Controller,

c. the DECtape magnetic tape.

Each of these functional components is briefly described in subsequent paragraphs.

1.2.1 TU56 Tape Transport

The TU56 is a dual tape transport containing two identical tape handling units. Each unit is a solid-state, bidirectional, magnetic tape handling device that controls tape motion and reads or records information on the magnetic tape.

The TU56 tape unit employs a 10-track read/write head. Tracks are arranged in five nonadjacent, redundant channels: timing channel, mark channel, and three data channels. Redundant recording of each character bit on nonadjacent tracks materially reduces bit dropout and minimizes the effect of skew. The corresponding track heads within a channel are connected in series and the resultant output is the analog sum of the two signals. Each head can be used for either reading or writing.

The timing of operations performed by the tape drive is governed by a prerecorded timing track on the tape. Therefore, wide variation in the speed of tape motion does not affect system performance.

Because of the bidirectional operation of the tape transport, high-speed access to stored program and data files is possible. Reading, writing, searching, and updating may be conducted in either direction. Reading and writing is performed at the rate of 5000 16-bit words per second.

1.2.2 TC11 Controller

The TC11 Controller is the interface between the tape transport and the PDP-11 Unibus. Thus, it controls data and command transfers between the tape unit and any device connected to the bus, such as the processor or memory. One controller can handle up to four TU56 DECtape Dual Transports (eight tape units).

The controller has two main functions: issuing control commands, and handling data transfers. Whether reading or writing, the controller first decodes the mark track information to make certain the transport is in the proper tape region.

During data transfer functions, the controller assembles the data word and places it on the bus (read operation) or loads it into the read/write heads (write operation) for recording on tape. The commands necessary to perform the specified operation are generated by the controller under program control.

The controller may issue other commands governing tape unit selection, direction of tape travel, maintenance tests, etc. The controller also monitors various functions and provides indications of error conditions.

Normal data word transfers are performed by DMA transactions (at the NPR level). If the controller is ready to begin a new function or if an error condition exists, it issues an interrupt request (provided the interrupt enable bit is set) so that the controller can be serviced by an interrupt program.

NOTE

Whenever an interrupt is mentioned in this manual, it is assumed that the interrupt enable (IE) bit in the command register has already been set; this is a condition that must be met prior to issuing an interrupt.

The five major registers within the controller are assigned standard addresses and can be loaded or read by any PDP-11 instruction referring to that address with the exception of certain read only, load only, or unused bits as described in Chapter 4. Thus, the controller is under program control. Certain functions may be enabled or disabled by switches on the controller maintenance panel, which also provides indicator lights to represent error conditions and selected functions.

1.2.3 Magnetic Tape

The DECtape magnetic tape is the recording medium used with the TC11 System. The Mylar tape is coated on both sides. Each small (3.9 in.) reel stores up to 147,968 16-bit words (assuming the standard format is used).

Data is recorded in blocks of 256 16-bit PDP-11 words. Each of 578 blocks is assigned a block number that is recorded at both ends of the block. Therefore, a search may be performed in either direction.

The tape format used is identical to that used in the PDP-9, PDP-10, and PDP-15 Systems. It is identical to that used in the PDP-8 except for the number of data words. The tape is divided into three major types of zones or areas: end zone, extension area, and information area. The end zones mark the physical end of the tape, the extension areas mark the end of the information area, and the information area contains the blocks of data.

The mark track recorded on the tape consists of a series of codes representing control or data words. These codes specify where the tape is and what is contained on that segment of the tape. The codes are constructed in such a manner that they read the same in either direction.

A timing track is also prerecorded on the tape to provide pulses that synchronize the control and data transfer operations. In effect, this track tells the controller when to perform a function.

1.3 SPECIFICATIONS

Operating and physical specifications for the TC11 Controller, the TU56 Tape Transport, and the DECtape magnetic tape are given in Table 1-1.

Table 1-1
TC11 System Specifications

Tape Characteristics

Capacity:	260 ft of 3/4 in., 1 mil, Mylar sandwich tape, coated both sides
Reel Diameter:	3.9 in.
Tape Handling:	direct-drive hubs and specially designed guides float the tape over the head. No capstans or pinch rollers are used.
Speed:	97 ±14 ips
Density:	350 ±55 bpi
Data Capacity:	147,968 16- or 18-bit words in blocks of 256 words
Tape Motion:	bidirectional (forward and reverse)

Word Transfer Rate

One tape character consisting of three data bits is read or written in parallel every 33-1/3 μs; one 16-bit (or 18-bit) word is read and assembled or disassembled and written in 200 μs.

Addressing

Mark and timing tracks allow searching for a specific block (under program control; no auto-search capability) by number in either the forward or reverse direction.

Tape Motion Timing

Start Time:	150 ±15 ms max.
Stop Time:	100 ±10 ms max.
Turnaround Time:	200 ±20 ms max.

Recording Method

Manchester method; this method employs phase-sensing and is basically an NRZ-M method with a timing track (also referred to as phase modulation).

Controller Register Addresses

Status Register (TCST):	777340
Command Register (TCCM):	777342
Word Count Register (TCWC):	777344
Bus Address Register (TCBA):	777346
Data Register (TCDT):	777350
Read/Write Buffer (RWB):	not accessible to program
Longitudinal Parity Buffer (LPB):	not accessible to program

Interrupt

Priority Level:	6
Vector Address:	214

Table 1-1 (Cont)
TC11 System Specifications

TU56 DECtape Transport

Mounting:	mounts in standard 19-in. rack
Size:	10-1/2 in. high, 19 in. wide, 9-3/4 in. deep
Cooling:	internally-mounted fan
Controls:	Front panel mounted – includes: unit select, WRITE ENABLE/WRITE LOCK, forward/reverse (FWD/REV), REMOTE-OFF-LOCAL.

TC11 Controller

Mounting:	mounts in standard 19-in. rack
Size:	10-1/2 in. high, 19 in. wide
Controls:	mounted behind blank front panel; includes: write all and write timing and mark enable/disable switches; error, ready, interrupt enable, and function indicators.

Environmental Conditions

Temperature:	40° to 90° F for system 60° to 80° F for magnetic tape
Humidity:	10% to 80% (noncondensation) for system 40% to 60% (noncondensation) for tape

Power and Cabling (see Figure 1-1)

Input Power:	115 Vac, 60 Hz, 6A for TC11 Controller 115 Vac, 60 Hz, 3A for each TU56 Tape Transport (also available in 240 Vac, 50 Hz)
TC11 Power:	system power supplied by one H720 Power Supply mounted at back of cabinet. Provides +5V at 16A and -15V at 10A for use by both TC11 and up to four TU56s.
TU56 Power:	tape transport power provided by internal power supply except for +5V and -15V
Power Usage:	TC11 uses: 5A at +5V, 0.5A at -15V. TU56 (one) uses: 800 mA at +5V, 550 mA at -15V
Cabling:	BC11-A cable to connect controller to Unibus M908 ribbon connector to connect command signals between controller and TU56 and between TU56 units. W032 connector to connect analog signals between controller and TU56 and between TU56 units.

1.4 ENGINEERING DRAWINGS

A complete set of engineering drawings and module circuit schematics is provided with each TC11 System. These drawings are bound in a separate volume entitled *TC11 DECtape System, Engineering Drawings.* A list of individual modules and associated drawings is included in Chapter 7 of this manual. The general logic symbols used on these drawings are described in the *DEC Logic Handbook, 1970.* Specific symbols and conventions are also included in the *PDP-11 Conventions Manual,* DEC-11-HR6B-D.

1.5 TERMINOLOGY

The *PDP-11 Conventions Manual,* DEC-11-HR6B-D, contains a list of terminology and abbreviations used with the PDP-11 family of systems. A glossary of PDP-11 terms, as well as general computer and programming terms, is also included.

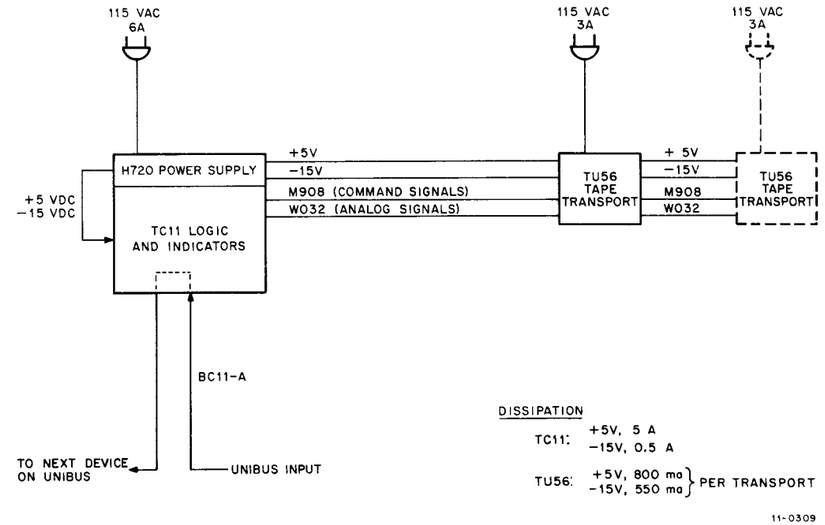


Figure 1-1 System Power and Cabling (simplified)

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains general information on the installation of the TC11 DECtape System. Detailed information on the installation of the TU56 Tape Transport is presented in the *TU56 DECtape Transport manual*, DEC-00-HRTA-D. Information on various mounting cabinets is presented in the *H720 Power Supply and Mounting Box manual*, DEC-11-HR5B-D.

2.2 CONFIGURATION

Installation procedures vary greatly dependent on the system configuration. For example, if the user has ordered a complete PDP-11 System, the TC11 DECtape is shipped already installed in its appropriate rack together with the required cables. If the complete system is shipped, the interconnecting cables are already installed.

If, on the other hand, only a part of the system is shipped because the user already has a basic PDP-11 System, then the TC11 DECtape System is shipped separately together with appropriate cables. Installation procedures may vary depending on whether the unit is mounted in a DEC- or customer-supplied cabinet, the number of tape transports used with the system, and other variable factors.

2.3 UNPACKING

The equipment should be unpacked as follows:

Step	Procedure
1	Place the equipment package within the installation site near its final location. Cut the shipping straps and carefully remove all packing material.
2	Remove the machine screws that hold the cabinet to the shipping pallet. Slide the cabinet off the pallet and move to its final location.
3	Remove any tape holding the modules in place within the mounting panels and any tape holding the power and interconnecting cables to the floor of the cabinet.

2.4 INSPECTION

Inspect all of the equipment before installing it, checking each piece against the parts list. Any damage must be reported immediately to the shipper and to the DEC representative.

2.5 SPACE REQUIREMENTS

No special site preparation is required for installation of the TC11 DECtape. However, when installing the system, make certain that front and rear of the cabinets are accessible to maintenance personnel. If the cabinets are separated by long distances, consideration should be given to overhead trenching ducts or floor ducts for the cabling.

2.6 POWER AND CABLE REQUIREMENTS

The TC11 DECtape Controller and associated TU56 DECtape Transports operate from a line voltage of either 115 Vac at 60 Hz or 240 Vac at 50 Hz, depending on the model ordered by the customer. The maximum current required is 6A for the controller and 3A for each tape transport. System power is supplied by one H720 Power Supply mounted on the back door of the cabinet. This supply provides sufficient power for the controller and up to four tape transports. In addition, each tape transport has an internal power supply. Power supply specifications are listed in Table 1-3.

Interconnecting cables are listed in Table 2-1. A diagram of system power and cabling is shown in Figure 1-1.

Table 2-1
Interconnecting Cables

Cable	Function
BC11-A Cable	Connects TC11 Controller to PDP-11 Unibus.
*M908 Ribbon Connector	Connects command signals between controller and TU56 transport; connects command signals between transports.
*W032 Connector	Connects analog signals between controller and TU56 transport; connects analog signals between transports.

*Number of cables supplied is dependent on number of transports in system.

2.7 INSTALLATION

If the TC11 DECtape System is shipped separately, there are only three components that must be installed: the TC11 Controller, the TU56 DECtape Transport (or transports), and the H720 Power Supply. The TC11 Controller is 19 in. wide and 10-1/2 in. high; therefore, it can be mounted in any standard 19-in. rack or cabinet. Installation of the power supply and tape transport are covered in the appropriate manuals referenced in Paragraph 2.1.

When the components are installed, connect interconnecting cables according to the diagram in Figure 1-1.

2.8 FINAL CHECKOUT

After the system is installed and all cables connected, a final checkout should be performed. The first step is to apply power and check all manual controls of the transports, power clear operation, etc. The second step is to run the diagnostics supplied with the system.

CHAPTER 3
OPERATION

3.1 INTRODUCTION

This chapter provides the information necessary to operate the TC11 DECtape System. The description is divided into two major parts: controls and indicators, and operating procedures.

The description of the controls and indicators (refer to Paragraph 3.2) is in tabular form and provides the user with the type and function of each operating switch and indicator on the TU56 Tape Transport and the TC11 Controller maintenance panel.

Step-by-step operating procedures for both on-line and off-line system operation are given in Paragraph 3.3. Maintenance-type procedures and adjustments for the TU56 are beyond the scope of this manual and are covered in the *TU56 DECtape Transport Manual.*

3.2 CONTROLS AND INDICATORS

The controls and indicators used to operate the TC11 DECtape System are detailed in the following paragraphs. These paragraphs describe the TU56 Tape Transport control panel and the TC11 Controller maintenance panel.

3.2.1 Tape Transport Control Panel

The TC11 DECtape System is controlled by switches mounted on the control panel of the TU56 DECtape Transport. These switches can be used for manual operation of the transport or can be used to enable the TC11 Controller for on-line operation under program control.

The tape transport control panel (see Figure 3-1) is the front panel of the TU56. The transport shown in the figure is a two-unit version, consisting of two identical transports mounted side by side. The TU56 may also be ordered in a single unit version. In either case, controls and indicators are identical.

Table 3-1 lists all controls and indicators on the tape transport and includes the type and function of each.

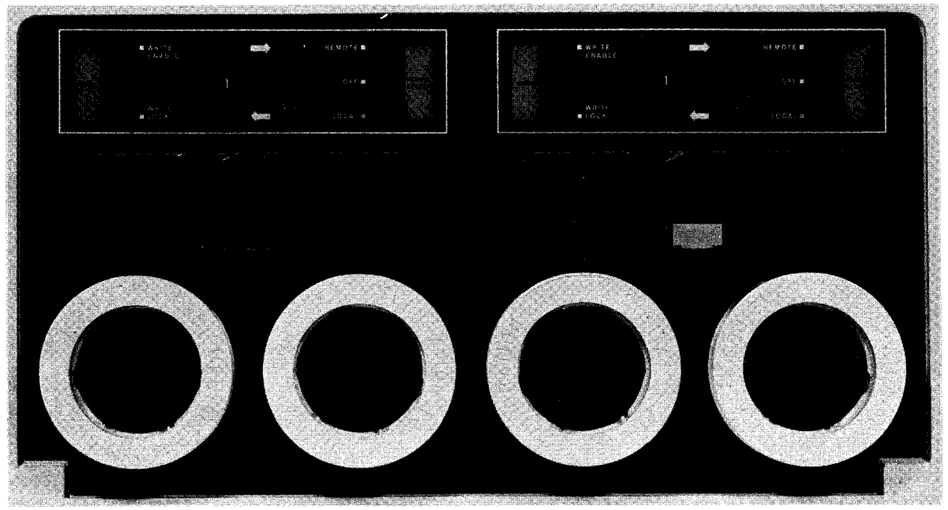


Figure 3-1 TU56 DECtape Control Panel

Table 3-1
TU56 DECtape Transport Controls

Control	Type	Function	Remarks
REMOTE/OFF/ LOCAL switch	3-position butterfly switch	Controls on-line and off-line operation of the tape unit.	
		REMOTE position – allows on-line system operation under program control.	Tape unit is not completely on-line until the tape unit has been selected by the program and the unit selector switch.
		The read/write head channels are not connected to the controller until the program selects a tape unit.	
		LOCAL position – disconnects the tape transport from the TC11 Controller to allow manual off-line operation.	Tape unit cannot be remotely selected when switch is in LOCAL or OFF.
		Tape motion is controlled by the FWD/REV switch when in LOCAL position.	
		OFF position – de-energizes tape drive reel motors to place the tape unit completely off-line.	
FWD/REV switch	3-position butterfly switch	Moves tape in selected direction during off-line (local) use of transport.	Tape direction is indicated by the appropriate white arrow.
	(spring-loaded to center position)	**FWD position** – when depressed, moves tape in forward direction as long as switch is held. Tape motion stops when switch is released.	This switch is disabled unless the REMOTE/OFF/LOCAL switch is set to LOCAL position.
		REV position – when depressed, moves tape in reverse direction as long as switch is held. Tape motion stops when switch is released.	
		Center (HOLD) position – normal rest position of the switch. Retains equal tension on tape but there is no tape motion.	Although not marked on the control panel, this position is often referred to as the HOLD position. Drawings in the TU56 manual normally refer to this as HOLD.
Unit selector switch	8-position thumbwheel switch	Permits remote selection of a tape unit by the program.	
	Each position has corresponding indicator	The tape unit is selected for use when the selection code	Enables the WRITE ENABLE/ WRITE LOCK switch of the

Table 3-1 (Cont)
TU56 DECtape Transport Controls

Control	Type	Function	Remarks
	number. These are numbers 0 through 7.	of the TC11 Controller corresponds to the numeral on the unit selector switch.	specific unit selected by the controller
Unit selector switch (cont)		When a tape unit is selected by the controller and the REMOTE/OFF/LOCAL switch is in REMOTE, the REMOTE indicator lights to indicate that the tape unit is on-line.	
REMOTE indicator lamp	single lamp (located to the right of the REMOTE/ OFF/LOCAL switch)	When lit, indicates that the tape unit is on-line. Tape unit is on-line when: *a.* REMOTE/OFF/LOCAL switch is in REMOTE position. *b.* Unit selector switch setting agrees with the controller selection code and the function is other than SAT or the MAINT bit is not set.	If REMOTE/OFF/LOCAL switch is set to REMOTE but the tape unit is *not* selected, this indicator does not light.
WRITE ENABLE/ WRITE LOCK switch	2-position butterfly switch	Determines whether or not the TC11 Controller can write on the tape.	This switch is enabled by the unit selector switch.
		WRITE ENABLE position – when set to this position, permits the TC11 Controller to write on the tape (if selected). Lights the WRITE ENABLE indicator.	
		WRITE LOCK position – when set to this position, prevents the controller from writing on the tape. If the controller attempts any write operation (WDATA; WALL, WRTM), the illegal operation (ILO) indicator lights.	Stops tape motion during on-line operation. The ILO indicator is on the TC11 Controller maintenance panel (refer to Paragraph 3.2.2).
WRITE ENABLE indicator lamp	single lamp (located to the left of the WRITE ENABLE/WRITE LOCK switch)	When lit, indicates that the WRITE ENABLE/WRITE LOCK switch is set to WRITE ENABLE.	If WRITE ENABLE/WRITE LOCK is set to WRITE ENABLE but the tape unit is *not* selected, this indicator still lights.

3.2.2 Controller Maintenance Panel

The TC11 Controller maintenance panel is used primarily for monitoring purposes during on-line operation of the system. The panel contains various indicator lamps that display error conditions, operational status of the tape unit, and specific functions being performed by the system. In addition, the panel contains two control switches that permit enabling or disabling of certain write functions used for tape formatting.

The controller maintenance panel is located to the right side of the TC11 Controller wired assembly. The panel is behind a blank mounting panel that must be removed before the maintenance panel can be observed.

Figure 3-2 shows the location of the maintenance panel, and Figure 3-3 shows the controls and indicators on the panel.

Table 3-2 lists all controls and indicators on the maintenance panel and includes the type and function of each. The three FUNCTION indicator lamps can be lit in any combination to denote one of eight possible functions. These functions are discussed in Paragraph 3.2.3.

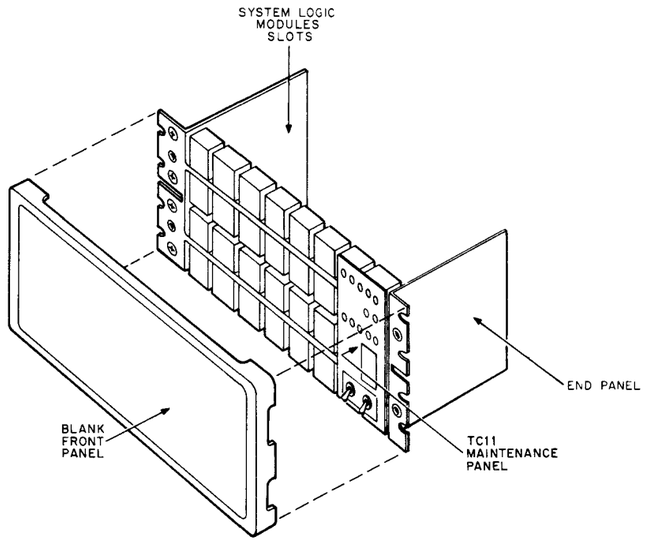


Figure 3-2 Location of Maintenance Panel

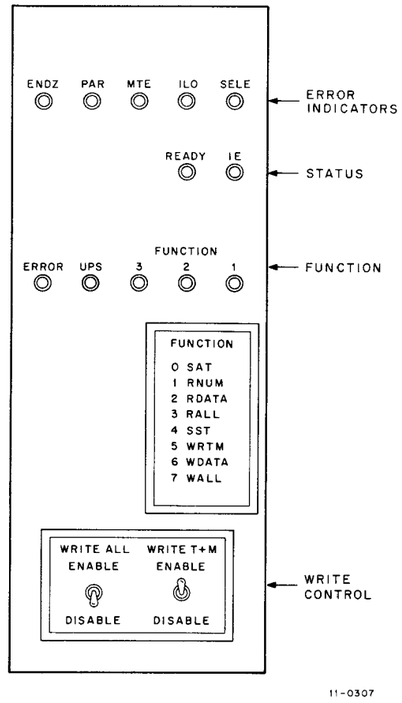


Figure 3-3 Maintenance Panel Controls and Indicators

Table 3-2
Maintenance Panel Controls and Indicators

Control	Type	Function	Remarks
ENDZ error indicator lamp	single lamp	When lit, indicates that the selected transport is in an end zone region of the tape. This represents an error condition because no data is stored in the end zones, and tape is about to run off the reel. An end zone error condition also causes the selected tape transport to stop.	An ENDZ error condition may be cleared in one of three ways: *a.* generating an initialize (INIT) signal *b.* loading a 0 into bit 15 (ERROR) of the command register *c.* setting bit 00 (DO) in the command register. INIT is normally generated by issuing a RESET instruction or by

(continued on next page)

Table 3-2 (Cont)
Maintenance Panel Controls and Indicators

Control	Type	Function	Remarks
ENDZ error indicator lamp (cont)			depressing START on the PDP-11 console. INIT is also generated during power-up and power-down sequences.
PAR error indicator lamp	single lamp	When lit, indicates a parity error. The parity error occurs if the calculated and written checksums disagree. This indicator is functional only when data is being read as indicated by octal 2 on the FUNCTION indicators.	A parity error condition is cleared in the same manner as an ENDZ error.
MTE error indicator lamp	single lamp	When lit, indicates that an error occurred during decoding of the mark track. A mark track error (MTE) stops the selected tape unit.	A mark track error is cleared in the same manner as an ENDZ error condition.
ILO error indicator lamp	single lamp	When lit, indicates an illegal operation that is a conflict between panel switch positions and the controller function. The switches that can cause an illegal operation (ILO) are: *a.* WRITE ENABLE/WRITE LOCK on the TU56 control panel *b.* WRITE ALL and WRITE T & M on the controller maintenance panel.	ILO error stops the selected transport. ILO error condition cleared (light goes out) when switches are reset to legal positions or when the function is changed. Refer to descriptions of these switches for explanation of correct and incorrect settings.
SELE error indicator lamp	single lamp	When lit, indicates that the program has selected a nonexistent tape unit or that more than one on-line tape unit has been dialed to the same number. SELE error refers only to units with the REMOTE/OFF/LOCAL switch set to REMOTE. Units set to LOCAL have no effect on SELE error. For example, if two on-line tape units each have the unit selector set to 3 (all other units in LOCAL) and the program selects 2, then the selection code is for a nonexistent unit. If the program selects	The SELE error light is cleared when unit selection switches are placed in valid position or when the program selects another valid unit. The SELE error indicator is disabled whenever bit 13 (MAINT) in the command register is set. The SELE error indicator is disabled whenever the stop all transports (SAT) function is being used as indicated by octal 0 on the FUNCTION indicators.

Table 3-2 (Cont)
Maintenance Panel Controls and Indicators

Control	Type	Function	Remarks
		3, then both tape units are selected. Both cases represent a selection error. A selection error condition stops the tape unit.	
READY status indicator lamp	single lamp	When lit, indicates that the controller is ready to accept a new command. The READY indicator lamp is lit on completion of a command, when an INIT signal occurs, or when any error condition (ENDZ, PAR, MTE, ILO, SELE, DATM, BLKM, or NEX) occurs.	The READY indicator is cleared whenever bit 00 (DO) in the command register is set.
IE status indicator lamp	single lamp	When lit, indicates that the interrupt logic is enabled, therby allowing a priority interrupt to occur. If READY is lit at the same time as interrupt enable (IE), a normal service interrupt routine is performed. If ERROR is lit at the same time as interrupt enable, the interrupt routine is normally used to branch to some type of error handling program.	Interrupt occurs if the READY or ERROR indicator lamp is lit. The IE indicator is cleared by an INIT signal or by loading with a 0 or 1.
ERROR indicator	single lamp	When lit, indicates that one or more of eight possible errors exist. Five of these errors are indicated by respective lights (ENDZ, PAR, MTE, ILO, and SELE). The other three errors are indicated by the status register (TCST) and are: *a.* BLKM – block number missed. *b.* DATM – data missed *c.* NEX – nonexistent memory location.	All eight error conditions (except ILO and SELE) are cleared in the same manner as an ENDZ error. If IE (interrupt enable) is lit when ERROR lights, then an interrupt is initiated. Whenever ERROR lights, it causes READY to light. Refer to Paragraph 5.8.3 for an explanation of BLKM, DATM, and NEX errors.
UPS indicator lamp	single lamp	The UPS (up-to-speed) indicator indicates that the selected tape unit has reached the speed required for proper operation. This indicator lamp is lit when the tape transport motor reaches the	The lamp is cleared either by an INIT signal or by changing tape direction or tape units, or by issuing a stop function (SAT or SST).

(continued on next page)

Table 3-2 (cont)
Maintenance Panel Controls and Indicators

Control	Type	Function	Remarks
		required speed; whenever bit 13 (MAINT) in the command register is set; or when a WRTM function occurs.	
FUNCTION indicator lamps	three lamps (1, 2, 3)	Specify a particular command to be initiated on the selected tape unit. When lit, these lights indicate the binary equivalent of the function (command) number.	Refer to Paragraph 3.2.3 for an explanation of the various function commands.

3.2.3 Function Indicators

The TC11 Controller can select any one of eight commands that control operation of the TU56 DECtape Transport. When the system is operated on-line, these commands are used for reading or writing data on the tape and for controlling tape motion.

The desired command is selected by the program that sets or clears bits 03, 02, and 01 in the command register (TCCM) to select the desired command. The command selected by the program is indicated by the three FUNCTION indicator lamps (3, 2, 1) which represent the binary representation of the command in use. When lit, the specific lamp represents a binary 1; when extinguished, it represents binary 0. In this discussion, these bits are usually referred to by their octal equivalent (0 – 7).

The eight function commands are listed and described in Table 3-3. Additional information on the commands, including certain conditions that must be adhered to during programming, are covered in Paragraphs 4.2 and 4.4.

Table 3-3
Function Indicators

Function Indicators 3 2 1	Octal Code	Mnemonic	Name	Function	Remarks
0 0 0	0	SAT	Stop all transports	Stops all tape motion. READY indicator lights after 10 μs.	Number on selected tape unit does not have to agree with programmed code as the SAT command stops all transports regardless of unit selection switch setting. Because the function bits are cleared after initialization, SAT is forced after power up, power down START, and RESET.
0 0 1	1	RNUM	Read block number	Finds the mark track code that identifies the block number on the tape in the selected tape unit and reads the block number into the controller.	Search can be performed in either direction of tape motion (forward or reverse).

Table 3-3 (Cont)
Function Indicators

Function Indicators 3 2 1	Octal Code	Mnemonic	Name	Function	Remarks
				When a block number is found, READY indicator lights and the block number is available in data (TCDT) and status (TCST) registers. Tape motion continues.	TCDT contains BD15 through BD00. TCST contains BD17 and BD16 (XD17 and XD16).
0 1 0	2	RDATA	Read data	RDATA is normally executed after a block has been found by the RNUM function. RDATA assembles one word of data at a time and transfers it directly on to the Unibus. Transfers continue until a word count overflow condition occurs at which time data is read to the end of the current block. Data that is read after word count overflow is not transferred but is used in the checksum calculation of the block. After checking parity (checksum), READY indicator lights. Tape motion continues.	Bus address is specified by TCBA. Refer to WDATA, function 6. When data is read in the reverse direction, the hardware performs the obverse complement function. Transfers can occur across block boundaries. If a checksum error exists, the PAR (parity) error indicator lights, READY is set, and all NPRs stop.
0 1 1	3	RALL	Read all	Reads information on the tape that is not read by the RDATA function. When tape unit is up to speed, data is read beginning at the first occurrence of a checksum area following a block mark. READY is set after bits are read for all six three-bit characters in a data word. 16 of the 18 bits are available in the data register (TCDT). The remaining two bits are bits XD17 and XD16 in the status register (TCST). READY is cleared when the TCDT register is read. Reading of data continues until another function command is issued, an end zone is detected, or an error condition arises.	RDATA function transfers only 16 bits; RALL function reads and makes available all 18 bits in the six 3-bit characters that make up a data word. When tape unit is up to speed, UPS indicator lights. Data is **not** transferred directly to memory as in RDATA (no NPRs). Data must be read by program controlled transfers. During reading, data appears in obverse complemented form if read in the opposite direction from which it was written. The hardware does not perform the obverse complement operation.

(continued on next page)

Table 3-3 (Cont)
Function Indicators

Function Indicators 3 2 1	Octal Code	Mnemonic	Name	Function	Remarks
1 0 0	4	SST	Stop selected transport	Stops all tape motion in selected transport only. READY indicator lights after 10 μs.	Execution time of commands is 10 μs. The tape actually stops in approximately 100 ms.
1 0 1	5	WRTM	Write timing and mark track	Writes timing and mark track information on DECtape. Used for formatting tape.	This command functions only if the WRITE T & M switch is set to ENABLE.
				Command enables a timing circuit for writing the timing track. Information written serially on the mark track is taken sequentially from bits 15, 12, 09, 06, 03, and 00 of the data loaded into the data register (TCDT).	WRTM functions in the same manner as WALL except that the mark track rather than data tracks is written. WRTM function does not use NPRs.
					WRTM can be stopped by forcing a DATM (data miss) error.
				READY indicator lights when data for next six lines is needed; READY goes out when the TCDT register is loaded.	WRITE ENABLE/WRITE LOCK switch must be in the WRITE ENABLE position.
				Writing continues until a new command is given or until an error occurs.	
1 1 0	6	WDATA	Write data	Writes data into the three data tracks. Sixteen bits of data are transferred directly onto the Unibus. The bus address is specified by the bus address register (TCBA). This 16-bit word plus bits XD17, XD16 = 0 are written as the six 3-bit characters.	This command is usually used only after the block number has been found (refer to function 1, RNUM).
					WRITE ENABLE/WRITE LOCK must be in WRITE ENABLE position.
				The bus address (TCBA) and word count (TCWC) registers are incremented and the next word is assembled and written.	Transfers can continue across block boundaries.
				Continuous transfers are made until the word count register overflows at which time all 0s are written to finish out the block. (1s are written in reverse.)	For each block written, a checksum is computed and written out in the checksum area of the tape.
					When data is written in the reverse direction, the hardware writes the data in obverse complement form so that it can be read normally in the forward direction.
				The READY indicator lights on completion.	

Table 3-3 (Cont)
Function Indicators

Function Indicators 3 2 1	Octal Code	Mnemonic	Name	Function	Remarks
1 1 1	7	WALL	Write all	Writes information on areas of tape not accessible to WDATA function.	This command functions only if WRITE ALL switch is in ENABLE position and WRITE ENABLE/WRITE LOCK switch is in WRITE ENABLE.
				When tape unit is up to speed, data is written beginning at the first occurrence of a checksum area following a block mark.	WDATA function writes only 16 bits, bits 16 and 17 are always written as 0s; WALL function writes all 18 bits in the six 3-bit characters that make up a data word.
				Sixteen bits from the data register (TCDT) and two bits (XD17 and XD16) from the status register (TCST) are written onto the tape.	The bus address (TCBA) and word count (TCWC) registers are not affected by this function. No hardware obverse complement is performed.
				READY indicator lights when data for the next word is needed; READY goes out when the TCDT register is loaded.	WALL is stopped by forcing a data miss (DATM) error.
				Writing continues until a new command is given, an end zone is detected, or an error condition develops.	

3.3 OPERATING PROCEDURE

The TC11 DECtape System can be used in either a local or remote operating mode. The local mode (also referred to as off-line or manual mode) is controlled by switches on the front panel of the TU56 transport. The remote mode (also referred to as on-line or program-controlled mode) is controlled by programmed commands from the PDP-11 System.

The following paragraphs present procedures for operating the TC11 DECtape System. Both local and remote operating modes are discussed. Although procedures for setting up remote (on-line) operation are included, it is beyond the scope of this chapter to present any programming details. Programming information is covered in Chapter 4.

3.3.1 Mounting Tape

Before using the TC11 DECtape System in either mode, it is necessary to make certain that magnetic tape is properly loaded in the TU56 tape unit. The following procedure is used for mounting tape:

Step	Procedure
1	Set REMOTE/OFF/LOCAL switch to OFF position.

(continued on next page)

Step	Procedure
2	Hold the DECtape reel with the label facing out, the blank side facing toward the tape unit. Press the reel onto the left-hand mounting hub of the tape unit. Make certain the reel is solidly seated all around.
	CAUTION **Do not attempt to use any reels other than DECtape reels on the TU56 tape unit.**
3	Pull the tape leader over the two tape guides and magnetic head until it reaches the take-up reel on the right-hand side of the tape unit.
4	Hold the tape against the hub of the take-up reel and rotate the reel clockwise by hand to wind four or five turns of tape onto the reel.
5	Verify that power is applied to the tape unit. Set REMOTE/OFF/LOCAL switch to LOCAL position.
6	Depress and hold the FWD switch until at least 15 turns of tape are wound onto the take-up reel. This ensures that the data portion of the tape is positioned over the magnetic head.

3.3.2 On-Line Operation

The following procedure is used to place the TC11 DECtape System on-line. When placed on-line, the system is controlled by programmed commands from the PDP-11 System.

Step	Procedure
1	Verify that the REMOTE/OFF/LOCAL switch is set to either LOCAL or OFF position and that system power is on.
2	Make certain that the desired tape is properly loaded (refer to Paragraph 3.3.1).
3	If writing is to be inhibited, set WRITE ENABLE/WRITE LOCK switch to WRITE LOCK position. If writing is required, set WRITE ENABLE/WRITE LOCK to WRITE ENABLE position. Set either WRITE ALL or WRITE T & M switch on maintenance panel to ENABLE according to required function. Make certain that nonselected switch is set to DISABLE.
4	Set the unit selector switch on the tape unit to the number required by the program.
	NOTE **If the tape transport is used as a multiplexed system, the unit selector switch on each unit must be set at a different number. For example, if four TU56 Dual DECtape Transports (eight tape units) are active, the unit selector of each tape unit must be set at a different number to prevent a SELE (selection error) indication.**
5	Set the REMOTE/OFF/LOCAL switch to REMOTE. The unit is now on-line and can be controlled by the program.
6	Whenever it is desired to stop on-line operation, set REMOTE/OFF/LOCAL switch to either OFF or LOCAL.

Step	Procedure
	If it is desired to stop a tape that is *moving* under remote command, jam the REMOTE/OFF/LOCAL switch from REMOTE position to LOCAL position without stopping in the OFF position. The OFF position de-energizes the motors completely and proper braking of the moving tape cannot be achieved. When tape motion stops, the switch can then be moved to the OFF position.

3.3.3 Off-Line Operation

Off-line operation of the TU56 DECtape Transport is used primarily for loading and unloading magnetic tape reels as discussed in Paragraphs 3.3.1 and 3.3.4, respectively. In addition, off-line operation can be used to check the tape drives as follows:

Step	Procedure
1	Set the REMOTE/OFF/LOCAL switch to OFF position.
2	Apply power to the desired tape unit.
3	Set the REMOTE/OFF/LOCAL switch on the desired tape unit to the LOCAL position.
4	Alternately depress and hold the FWD and REV tape motion switches. Verify that tape moves properly and that all reels are running freely and are not mounted in a skewed position.
5	Repeat steps 3 and 4 for second tape unit on the transport.

3.3.4 Removing Tapes

The following procedure is used for removing magnetic tape from the tape unit:

Step	Procedure
1	Set the REMOTE/OFF/LOCAL switch to LOCAL.
2	Depress and hold the REV switch until all the tape is wound onto the left-hand tape reel.
3	Set the REMOTE/OFF/LOCAL switch to OFF.
4	Remove the full reel from the left-hand hub.

3.3.5 Formatting Tapes

There are three possible cases that require a magnetic tape to be formatted:

a. a new, blank tape is to be used

b. an obsolete tape is to be reused, and it is necessary to write it in an up-to-date format

c. a tape of questionable quality exists (as evidenced by a high number of errors), and it is necessary to reformat the tape. In this case, data must first be stored elsewhere before the tape is formatted.

Formatting of tapes is accomplished by a special program supplied with the TC11 System. It is beyond the scope of this discussion to describe the program. Program information is included with the program documentation. However, it should be noted that this program is run with the system on-line (refer to Paragraph 3.3.2) and makes use of the WRITE ALL and WRITE T & M switches on the TC11 Controller maintenance panel (refer to Paragraph 3.2.2).

The format program permits the standard structure to be written, that is, 578 blocks of 256 words to a block.

CHAPTER 4
PROGRAMMING INFORMATION

4.1 SCOPE

This chapter presents general programming information for software control of the TC11 DECtape System. Although a few typical program examples are included in this chapter, it is beyond the scope of this manual to provide detailed programs. For more detailed information on programming in general, refer to the *Paper-Tape Software Programming Handbook*, DEC-11-GGPB-D.

This chapter of the manual is divided into five major portions:

a. device registers
b. interrupts
c. function commands
d. timing considerations
e. programming examples.

4.2 DEVICE REGISTERS

All software control of the TC11 DECtape System is performed by means of five device registers. These registers have been assigned bus addresses and can be read or loaded using any PDP-11 instruction that refers to their address. The five device registers and associated addresses are listed in Table 4-1. Note that these addresses can be changed by altering the jumpers on the M105 Address Selector Module. However, any DEC programs that refer to these addresses must also be modified accordingly if the jumpers are changed.

Figures 4-1 through 4-5 show the bit assignments within the five device registers. The "unused" and "load only" bits are always read as 0s. Loading "unused" or "read only" bits has no effect on the bit position. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by depressing the PDP-11 System START switch; by issuing a RESET instruction; or by a power-up or power-down sequence.

Table 4-1
Standard Device Register Assignments

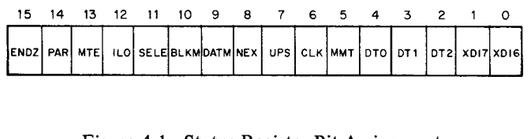
Register	Mnemonic†	Address
Control and Status Register	TCST	777340
Command Register	TCCM	777342
Word Count Register	TCWC	777344

†First two letters of mnemonic (TC) refer to tape control; second two letters represent mnemonic of specific register.

Table 4-1 (Cont)
Standard Device Register Assignments

Register	Mnemonic†	Address
Bus Address Register	TCBA	777346
Data Register	TCDT	777350

†First two letters of mnemonic (TC) refer to tape control; second two letters represent mnemonic of specific register.



11-0306

Figure 4-1 Status Register Bit Assignments

Bit		Meaning and Operation
15	ENDZ	indicates that the selected tape unit is in an end zone region of the tape. Cleared by INIT; cleared by loading a 0 into bit 15 (ERROR) of command register; cleared by loading a 0 into bit 00 (DO) of the command register. Stops selected tape unit.
14	PAR	indicates a parity error. The parity error occurs during READ DATA function if the calculated and written checksums disagree. Cleared in the same manner as ENDZ.
13	MTE	indicates that an error occurred during decoding of the mark track. Stops selected tape unit. Cleared in the same manner as ENDZ (bit 15).
12	ILO	indicates an illegal operation caused by a conflict in switch positions of the WRITE ALL, WRITE T & M, and WRITE ENABLE/WRITE LOCK switches. These conflicts are: *a.* WRITE LOCK on during WRTM, WALL, or WDATA modes *b.* WRITE T & M switch off during WRTM mode *c.* WRITE ALL switch off during WALL mode Stops selected tape unit. Cleared when switches reset to valid positions or when a nonconflicting operation is selected.

(continued on next page)

Bit		Meaning and Operation
11	SELE	indicates that the program has either selected a nonexistent tape unit or that more than one on-line tape unit has been dialed to the same unit number. The SELE bit is affected only by tape units on-line (switch set to REMOTE). Off-line units (switch in LOCAL) have no effect on this bit. Stops selected tape unit. Disabled if MAINT bit (bit 13 in TCCM) is set or if function is SAT (bits 03, 02, and 01 in TCCM cleared). Cleared when unit selection switches set to valid positions or when another unit is selected.
10	BLKM	indicates a block was missed. The transfer from read block number (RNUM) to read data (RDATA) or write data (WDATA) functions occurred too late. Also, indicates switch to RDATA from WDATA was too late. Cleared in the same manner as ENDZ (bit 15).
09	DATM	indicates data was missed. Request for data transfer not honored in time during RDATA, WDATA, WALL, or RALL. Cleared in the same manner as ENDZ (bit 15).
08	NEX	indicates nonexistent memory. This occurs when the TC11 Controller is bus master during RDATA or WDATA and does not receive a SSYN response within 20 μs after asserting MSYN. Cleared in the same manner as ENDZ (bit 15).
07	UPS	indicates that selected tape unit is up to the speed required for proper operation. Cleared by INIT; cleared when UNIT SELECT or REV bit is changed. Set when unit is up to speed; set when MAINT bit (bit 13 in command register) is set or when the selected function is WRTM.
06	CLK	clock bit used to simulate timing track. May be loaded when MAINT bit is set. When CLK is set, produces TP1; when cleared, produces TP0.
05	MMT	maintenance mark track used to simulate the bit read from the mark track. May be loaded when MAINT bit is set. Cleared by INIT.
04	DT0	data track 0 used to simulate output of the read amplifier when loaded; when read, reads the input to the write amplifier. When MAINT bit is set, DT0 loads into RWB2 and reads as RWB5.
		NOTE **Bits 04, 03, and 02 function as six bits. When loaded, they simulate the read amplifier and are loaded into RWB2, RWB1, and RWB0. When read, they read the write amplifier inputs from RWB5, RWB4, and RWB3.**
03	DT1	data track 1. Functions the same as DT0 except loads into RWB1, reads as RWB4.
02	DT2	data track 2. Functions the same as DT0 except loads into RWB0, reads as RWB3.
01	XD17	extended data bit 17 which allows reading and writing on areas of the tape not accessible during 16-bit word transfers. Cleared by INIT.
00	XD16	extended data bit 16. Cleared by INIT.

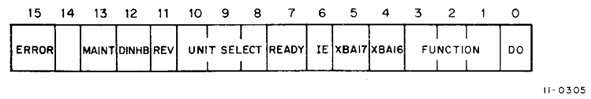


Figure 4-2 Command Register Bit Assignments

Bit		Meaning and Operation
15	ERROR	indicates an error condition that is the inclusive OR of all error conditions (bits 15–08 in TCST). Causes an interrupt if enabled (see bit 06). Clears errors (except ILO and SELE) when loaded with 0. Sets READY bit (bit 07).
14	Unused	
13	MAINT	used for maintenance functions. When set, enables operation of bits 06–02 in the TCST. Cleared by INIT.
12	DINHB	delay inhibit bit. This bit is set in the special case where it is desired to inhibit the delay associated with bringing a tape unit up to speed. For example, reselecting (in the same direction) a tape unit known to be up to speed. Cleared by INIT.
11	REV	specifies direction of tape motion. When set, specifies reverse motion; when cleared, specifies forward motion. Cleared by INIT.
10–08	UNIT SELECT	specify the number of the tape unit which is to receive the desired command. These three bits are set or cleared to represent an octal code which corresponds to the unit number of the tape unit to be used. Cleared by INIT.
07	READY	indicates that the TC11 controller is ready to receive a new command. Cleared when DO (bit 00) is set. Set when command execution is complete; set by INIT or ERROR (bit 15). Read only.
06	IE	interrupt enable bit. This bit allows an interrupt to occur provided either READY (bit 07) or ERROR (bit 15) is set. Cleared by INIT.
05	XBA17	extended bus address bit 17. Used to specify address line 17 in direct memory transfers. Increments with the TCBA. Cleared by INIT.
04	XBA16	extended bus address bit 16. Function is same as XBA17 (bit 05).
03–01	FUNCTION	specify a command to be performed on the selected transport. Cleared by INIT or SAT. The function commands are:

Bit 03	02	01	Function
0	0	0	SAT – stop all transports
0	0	1	RNUM – read block number
0	1	0	RDATA – read data
0	1	1	RALL – read all
1	0	0	SST – stop selected transport
1	0	1	WRTM – write timing and mark track
1	1	0	WDATA – write data
1	1	1	WALL – write all

00	DO	loaded with a 1 when a new function is given. Clears READY. Write only.

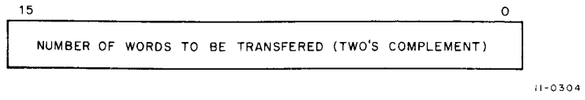


Figure 4-3 Word Count Register Bit Assignments

Bit		Meaning and Operation
15–00	WORD COUNT	contains 2's complement of the number of words to be transferred. This register counts the number of word transfers made during RDATA (read data) and WDATA (write data) functions. The word count register is loaded prior to initiation of one of the functions. The register is incremented by 1 after each transfer. When the contents of the register equal all 0s, further transfers are inhibited. If the word count register (TCWC) is cleared when RDATA or WDATA is initiated, then 2^{16} transfers are attempted. Cleared by INIT.

NOTE

The word count register must not be modified by using byte instructions. Use only word instructions when loading this register. The register is wired in such a manner that the entire word is loaded even if a byte instruction is used. Therefore, if the programmer attempts to load only the low-order byte, for example, the data on the high-order data lines is also loaded. This latter data may be useless and/or unknown to the programmer.

Figure 4-4 Bus Address Register Bit Assignments

Bit		Meaning and Operation
15–01	ADDRESS	specify the bus or memory address to or from which data is to be transferred during RDATA (read data) and WDATA (write data) operations. These bits are used in conjunction with bits XBA17 and XBA16 in the command register. After each transfer (during RDATA or WDATA) is made, this register is incremented to advance it to the next word location. Note that command register bits XBA17 and XBA16 participate in the incrementation; they are a logical extension to this register. The bus address register (TCBA) is loaded prior to initiating an RDATA or WDATA command. Cleared by INIT.

NOTE

The bus address register must not be modified by using byte instructions. Use only word instructions when loading this register.

00	Unused	a read/write bit. It is not tied to A00, forcing addressing to words on even boundaries.

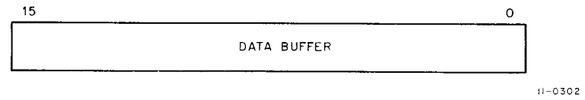


Figure 4-5 Data Register Bit Assignments

Bit		Meaning and Operation
15–00	DATA	contains data word to be read from or written on the magnetic tape. These bits and bits XD17 and XD16 in the status register form three 6-bit shift registers which are active during control operation. These 18 bits correspond one to one with the six 3-bit characters read or written on the tape. The data register accepts information under program control during WALL (write all) and WRTM (write timing and mark) operations. During RALL (read all) and RNUM (read block number) operations, the data register contains data read from the tape. During WDATA (write data) and RDATA (read data) operations, the data register is used to buffer information between the controller and the Unibus. Cleared by INIT.

NOTE

The data register must not be modified by using byte instructions. Use only word instructions when loading this register.

4.3 INTERRUPTS

The TC11 Controller uses NPR or BR interrupts to gain control of the bus in order to perform data transfers or to cause a vectored interrupt, thereby causing a branch to a handling routine. The NPR requests are made during RDATA and WDATA functions. When the processor grants the request and other Unibus conditions are met, the TC11 gains control of the bus and performs either a DATI or DATO to transfer data directly on to the Unibus.

A BR interrupt can occur only if the interrupt enable (IE) bit in the command register is set. With IE set, setting either the READY or ERROR bit in the command register initiates an interrupt request. When READY is set, it indicates that a block number has been found (RNUM) or that a block transfer is complete (WDATA or RDATA). READY also indicates that the controller is ready to perform a data transfer. In this case, which is true for WRTM, WALL, and RALL functions, the interrupt service routine is used to perform the bus cycle.

When ERROR is set, it indicates that some type of error condition exists. In this case, an interrupt is used to cause a program branch to an error-handling routine.

If the DO bit in the command register is set (indicating that a command function is to be performed) and the ERROR bit remains set (indicating the error condition has not been cleared), then a new interrupt occurs that either tries to clear the error or make the selection required by DO.

The interrupt priority level is 6, and the interrupt vector address is 214. Note that the priority level can be changed by the priority chip on the G736 Module, and the vector address can be changed by jumpers on the M782 Interrupt Control. However, any DEC programs referring to the level or address must also be changed if the jumpers are changed.

4.4 FUNCTION COMMANDS

The eight function commands used for reading or writing data on tape and for controlling tape motion are covered in detail in Table 3-3. In addition to understanding the operation of each specific function, the programmer should note that information written on the tape is not completely bidirectional in nature due to the obverse complement recording characteristic of the system. A complete discussion of obverse complement numbers, including methods used by the system for reconverting them to the original numbers, is presented in Paragraph 5.3.

All DECtape functions operate independently of tape motion direction because of the symmetry of the mark track coding. This symmetry is possible because the mark track codes used by the tape format are numbers that are identical in both the normal and obverse complement forms. Thus, the proper code can be read regardless of tape direction.

However, total bidirectional symmetry of the functions is not possible because of the orientation of words within a block (lower memory addresses written first) and because of the location of bits within a word. This means that a block of data written in one direction does not read the same if read in the opposite direction. Its position, rather, is reversed in the order of increasing memory addresses and the bits are the obverse complement of the original data. The obverse complement problem of the bits is corrected by the hardware which performs an obverse complement operation on the data during RDATA (read data) and WDATA (write data) functions performed in the reverse direction. The hardware *does not*, however, perform the obverse complement operation during RALL, WALL, or WRTM operations.

During normal modes of operation (RDATA or WDATA), as long as a block is written and read in the same direction (either both forward or both reverse), there is no problem. However, if a block is read in the opposite direction from which it was written, the bits in the block of data are inverted in form and may or may not have to be swapped around before use.

4.5 TIMING CONSIDERATIONS

When programming the TC11 DECtape System, it is important to consider timing of certain functions in order to prevent lost data and/or to use the system in the most efficient manner. Timing considerations for the data rate, transport motion, and latency are discussed in the following paragraphs.

4.5.1 Data Rate

When tape motion is up to speed, one 3-bit character is read or written every 33.3 μs. Thus, the data rate is 200 μs per word (six 3-bit characters per word) or 53.2 ms per block (one block equals 256 data words and 10 control words). Although variations in recording density and tape speed may cause these rates to change, they always remain within a tolerance of approximately ±30%.

4.5.2 Transport Motion

The TU56 DECtape Transport tape drive operates at the speeds listed below. Note that these times are given for 90% of maximum possible speed.

Start time	150 ms ±15 ms (maximum)
Stop time	100 ms ±10 ms (maximum)
Turnaround time	200 ms ±25 ms (maximum)

Tape motion can be reversed by re-issuing the specified command with the REV bit in the command register complemented.

4.5.3 Latency

When the RNUM (read block number) function is used, the program has a maximum of 533 μs from the time READY (bit 07 in the command register) is set until the time the program can switch the controller to either the RDATA (read data) or WDATA (write data) function. If the switch is not made within this time, a block miss (BLKM) error occurs. For switching to RALL or WALL, a BLKM occurs if switching is not completed within 333 μs.

When the RALL (read all), WALL (write all), or WRTM (write timing and mark) function is used, the program must respond to READY within 67 μs. If it does not respond within this time, a data miss (DATM) error occurs. During the RDATA and WDATA functions, if the TC11 Controller does not receive control of the bus within 67 μs of making an NPR request, a DATM error occurs.

4.6 PROGRAMMING NOTES

The following notes pertain to programming the TC11 Controller and contain information that may be useful to the programmer. More detailed programming information is given in the *Paper-Tape Software Programming Handbook,* DEC-11-GGPB-D and in the individual program listings.

1. **Block Addressing** – blocks can be randomly accessed in either the forward or reverse direction with the following restriction: turnaround is not symmetric. As described in Paragraph 4.5.2, the tape can stop quicker than it starts. Thus, if while searching forward for block n, block n+1 is found, then the tape must be moved to block n+3 before a turnaround time is given. This ensures that the tape is up to speed before coming to block n in the reverse direction.
2. **Reading or Writing Blocks** – blocks can be read or written in either direction. No problems occur if the tape is read in the same direction that it was written in. If read (RDATA) in the opposite direction from that the tape was written (WDATA) in, then the order of the words in the block is reversed. That is, the first word read is the last word written. No complement obverse problems occur in RDATA and WDATA because the hardware formats the data when reading or writing in reverse.
3. **Transfers** – transfers always begin at block boundaries. Length of the transfer may be any length and may be partial or multiple blocks. The unused portion of a partially written block is written as 0s forward or 1s in reverse.
4. **Obverse Complement Problem** – there is no hardware assistance in RALL, WALL, or WRTM modes. The programmer must tackle the full obverse complement problem whenever the direction of reading is opposite the direction that the tape was written in. All bits are displaced and complemented within each word.
5. **Reading Block Numbers** – there is no obverse complement problem when reading block numbers in reverse because the REV BLOCK number is formatted in obverse form to begin with so that when it is read in reverse, all bits appear normal.
6. **Identification of Available Tape Unit** – the SST function is a convenient method of identifying tape units available for use by the controller. The function can be given and, if no selection error (SELE) develops, then the tape unit is on-line (remote) and dialed up to that unit number.
7. **Maintenance Mode** – the maintenance mode is selected by setting the MAINT bit in the command register. In this mode, the controller deselects all transports, disables the SELE logic, and disables the WRITE LOCK switch. The programmer can then load various bits into the status register to simulate the bit read from the mark track or bits loaded into or read from the three data tracks or the timing track.

(continued on next page)

8. **Use of DINHB Bit** – DINHB in the command register is used *only* when reselecting a transport in the same direction that it was *left* running in. For example, assume the following:

   a. Unit 0 is selected, searches for block numbers while running in *reverse* direction.

   b. Unit 7 is now selected (unit 0 is still moving but is no longer in control), searches for block numbers while running in the *forward* direction.

   Under the above conditions, if unit 0 is reselected (it must be reselected before it runs off the reel), it must be reselected in *reverse* which is the direction it was moving, if DINHB is to be used. The advantage of using DINHB is to shorten the amount of time (10 ms rather than 120 ms) that it takes to select a transport in this special case.

   Note that the TC11 Controller can only sense the timing and mark track of one unit at a time. However, units can be left running forward, reverse, or stopped. If left running unattended, the tape eventually runs off the reel since the controller cannot detect the end zone unless that unit has been selected. If multiple units are to be run (for example, rewinding one tape while searching for data on another), then each active unit must be scanned continually to ensure that it is not approaching the end zone.

4.7 PROGRAM EXAMPLES

The following two examples represent typical methods of programming the TC11 Controller. The first example finds a specified block; the second example is a routine for writing data into a specific block.

a. **Routine to find a specified block**

```
;ENTER WITH R0 = BLOCK WANTED
;FINDS BLOCK IN FORWARD DIRECTION
SEARCH:  MOV R0, BWANT
         SUB #3, BWANT          ;Offset
         MOV #4003, TCCM        ;Unit 0, Reverse, RNUM, DO
LOOP1:   BIT #100200, TCCM      ;Check READY and ERROR
         BEQ LOOP1
         BMI ERROR
         SUB TCDT, BWANT        ;Check block found
         BLT SEARCH
FORWRD:  MOV R0, BWANT
         MOV #3, TCCM           ;Unit 0, Forward, RNUM, DO
LOOP2:   BIT #100200, TCCM      ;Check for READY and ERROR
         BEQ LOOP2
         BMI ERROR
         SUB TCDT, BWANT        ;Check block found
         BGT FORWRD
         BLT SEARCH
         RTS PC                 ;Return when block is found
ERROR:   TST TCST               ;Test for ENDZ
         BMI LOOP3
         HALT                   ;HALT on error other than ENDZ
LOOP3:   BIT #4000, TCCM        ;Check direction
         BNE FORWRD             ;If REV, now search FORWARD
         BR SEARCH              ;If FOR, now search REVERSE
```

b. **Routine to write 100 words into block 47 on unit 0**

```
START:   MOV #47, R0            ;Set up R0 for subroutine call
         JSR PC, SEARCH         ;Go find block
         MOV #-100, TCWC        ;Set up word count
         MOV #BUFFER, TCBA      ;Set up bus address
         MOV #15, TCCM          ;Give command: WDATA, DO,
                                 Unit 0, FORWARD
LOOP4:   BIT #100200, TCCM      ;Check READY and ERROR
         BEQ LOOP4              ;Branch on READY and ERROR = 0
         BMI ERR                ;Branch to error service
          .
          .
          .                     ;Continue with program
          .
          .
BUFFER:  0                      ;Start of buffer
          .
          .
          .
          .
```

CHAPTER 5
THEORY OF OPERATION

5.1 INTRODUCTION

This chapter provides a detailed description of the TC11 Controller and consists of three major parts: *a)* functional description of overall controller operation, *b)* block diagram description, and *c)* detailed theory of operation covering controller logic circuits. The discussions in this chapter are supported by a complete set of engineering drawings contained in a companion volume entitled, *TC11 DECtape System, Engineering Drawings.*

The TC11 Controller may be divided into eight functional areas: *a)* selection logic, *b)* bus control logic, *c)* register logic, *d)* tape control logic, *e)* read/write logic, *f)* error logic, *g)* maintenance mode logic, and *h)* control panel logic. Each of these areas is covered separately in the detailed descriptions of this chapter. The purpose of each of these functional units is as follows:

selection logic — determines if the controller has been selected as a slave and what type of operation (read or write) has been selected. Permits selection of one of five internal registers for use and determines if the register performs an input or output operation.

bus control logic – permits the controller to gain bus control either by means of an NPR for transferring data words or by means of a programmed interrupt to request service by the program because an error condition exists or because the controller is ready to perform a new operation or make a transfer in RALL, WALL, or WRTM modes.

register logic – five internal registers, addressable by the program, provide data transfer functions, command and control functions, and status monitoring functions for the TC11 Controller.

tape control logic – controls selection of tape unit, direction of tape motion, and decoding of timing and control information from the timing and mark tracks on the tape.

read/write logic – controls assembly, disassembly, and transfer of data between the magnetic tape and the Unibus.

error logic – monitors controller operation and provides an indication of any error condition that arises. Stops the operation and issues an interrupt request for most error conditions.

maintenance mode logic – permits checking of controller logic. Disables tape input circuits and provides simulated tape data.

control panel logic – provides signals that light error indicators; controls operation of the two WRITE ENABLE/DISABLE switches on the controller maintenance panel.

5.2 TAPE FORMAT

The tape format used in the TC11 System is identical to that used by the PDP-9, PDP-10, and PDP-15 Systems. It is also identical to that used by the PDP-8 System except for the number of data words. It is assumed that the reader is familiar with this standard DECtape format. If not, a comprehensive explanation is presented in Appendix A. This appendix covers the recording method (both the Manchester method used in the TC11 and a review of other methods); bidirectional reading and writing (obverse complement problem); and the tape format itself including a description of the function of each DECtape code. The user must have a thorough understanding of these topics in order to understand the detailed descriptions of the logic circuits. Although tape formats for DEC systems are basically identical, there is a distinction in packing and labeling of bits within a data word. This distinction is illustrated in Appendix B, which also illustrates how PDP-8 words are read by the TC11 Controller.

The format used for the TC11 is identical to that used by the PDP-8 except for the number of data words. The standard PDP-8 block contains 129 12-bit words or the equivalent of 86 18-bit words. Appendix B shows how three 12-bit words would be read back as two 18-bit words.

Note that in the normal (direct memory transfers) TC11 read/write operations, only 16-bit words are transferred. During the read operation, the two most significant bits of an 18-bit word are truncated; during the write operation, the two most significant bits are written as 0s. However, if the TC11 read all (RALL) or write all (WALL) mode is used, 18-bit words are available for program-controlled transfers.

5.3 FUNCTIONAL DESCRIPTION

The TC11 Controller performs two primary functions: transferring data, and controlling transport operation. Both of these functions are under control of the program.

When performing data transfers, the controller operates in either a read or write mode. If a write mode is used, the data to be eventually stored on the tape is located in some memory location or other storage device. The device or the TC11 Controller itself transfers the data on the Unibus, and the information is strobed into the controller in parallel form. The controller holds this data in a data buffer register and then rotates and shifts it out in parallel (three bits at a time) during the write operation so that the data is assembled on the tape into words consisting of six 3-bit characters. If a read mode is used, data is read from the tape one 3-bit character at a time and loaded into the buffer register. This character is shifted when the next character is loaded and the process repeated until the entire word read from the tape is loaded into the buffer register. The word is then placed on the bus in parallel form where it can be strobed into memory or some other storage device. A word count register in the controller keeps track of the number of words transferred during a read or write operation and stops the transfer function when the required number of words has been reached.

The control function is handled basically by a command register, a status register, and timing and mark track decoders. The command register specifies the tape unit to be used, the direction of tape motion, and the particular function (such as read, write, stop transport) to be performed. The status register reports the functional status of the operation and is monitored to determine if any error conditions (such as parity, illegal operation, end zone) exist. The mark track decoder decodes the control words on the tape to inform the controller of the area of the tape being used and the information on that area (such as block number).

Other control logic in the TC11 Controller permits NPR and interrupt requests to be made. Thus, the controller requests use of the bus when it is ready to transfer data or when it needs to go to a service routine because of an error condition.

Selection logic within the controller permits each register to be addressed individually so that all transfer and control functions are under direct program control.

The normal sequence of TC11 Controller operation consists of reading block numbers until the target block is found, then reading or writing as many data words as required, and then writing or checking parity to ensure that the information is valid. If an error occurs during this sequence, the controller issues an interrupt so that the program jumps to an error handling routine. Some errors automatically cause the transport to stop, other error conditions must be monitored and serviced by the program.

When searching for a specific block number, the mark track decoder reads the first block mark code (26) encountered and the data associated with this block number code is then loaded into the data register. The controller then issues an interrupt so that the processor can examine the number. Under program control, the processor compares the number from the controller with a number stored in the program (this number represents the required block).

If the numbers do not agree, the process is repeated with the next sequential block number on the tape. If the numbers do agree, then the program loads the command register to select the desired function (such as read or write). There are eight possible functions: three read functions, three write functions, and two stop functions.

The read block number (RNUM) function is used to search for a specific block on the tape and can be used regardless of direction of tape motion. When the required block is found, the number is available in both the status and data registers. The status register contains the two high-order bits (these are usually 0s and are ignored), and the data register contains the 16 low-order bits.

The read data (RDATA) function assembles one word of data at a time and transfers it directly to memory. Transfers are accomplished through NPR control and continue until a word count overflow occurs. Although the entire 18-bit word is read and assembled, only 16 bits are transferred. Read data is the normal function used whenever a tape is being read.

The read all (RALL) function makes the entire 18-bit word accessible to the program. The controller assembles the word, placing 16 bits in the data register and the other two in the status register. The word is not transferred at this time, rather, an interrupt request is made. The program then decides what to do with the 18 bits. This function is normally only used when the programmer needs to have access to the two additional bits (such as reading tapes produced by other DEC systems).

The write data (WDATA) and write all (WALL) functions operate similarly to the corresponding read operations except data is written on the tape rather than read.

The write timing and mark track (WRTM) function is used to format a tape by adding the timing marks and mark track data. This function may also be used to rewrite mark and timing information that may have been destroyed. Whenever this function is used, any data or previously written mark track information is destroyed. The mark and timing tracks for the entire tape are generated in a single pass.

The two stop functions are used to stop the tape transport. If the stop all transports (SAT) function is used, all transports stop regardless of the setting of the unit selector bits. If the stop selected transport (SST) function is used, only the selected transport is stopped. The unit selector switch on the transport must agree with the number issued by the program in order for the transport to stop with the SST function.

The SST function is a convenient method for identifying tape units available for control use. The SST function can be issued, and, if no selection error (SELE) develops, then the tape unit is on-line (remote) and dialed up to that unit number.

5.4 BLOCK DIAGRAM DESCRIPTION

Figure 5-1 is a simplified block diagram of the TC11 DECtape System showing the relationship of the TC11 Controller to the TU56 Tape Transports and to PDP-11 System components. Figure 5-2 is a detailed block diagram illustrating the major components constituting the TC11 Controller. This detailed block diagram is briefly discussed below.

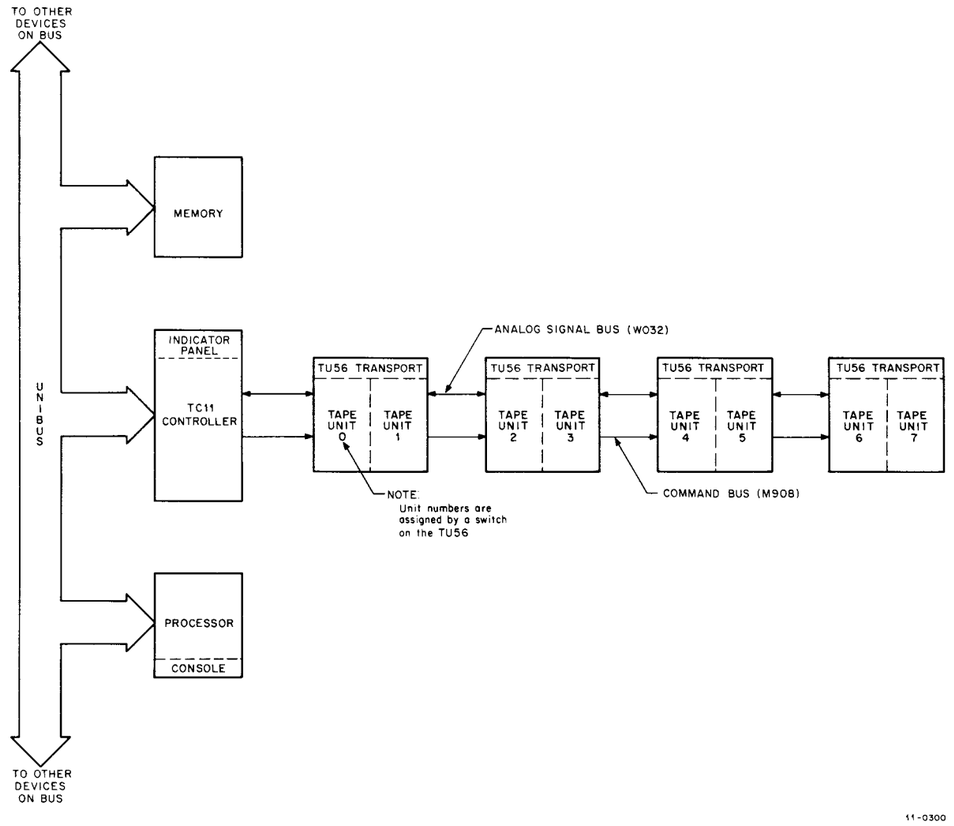


Figure 5-1 TC11 System – Simplified Block Diagram

The address selector, in conjunction with the register control logic, decodes the incoming address from the Unibus to determine if the controller has been selected as a slave, what type of operation (read or write) is to be performed, and which of the five interface registers is to be used.

If the controller has been selected for a write operation, data from the bus is applied through the bus receivers to the specified registers. Commands from the command register are applied to the transport control logic which sends appropriate signals to the tape transports to select a specific transport, select the direction of tape motion, and initiate the function to be performed. The data to be written on the magnetic tape is fed from the data buffer register to the data assembly logic which formats the data. The formatted data is then applied through the read-write amplifiers to the write heads in the selected tape transport and the data is written on the tape.

The required timing signals are supplied by the timing and control logic, which is also activated by signals from the interface registers. If any error conditions arise during the write operation, they are detected by the error detection circuits, which send an appropriate signal back to the interface registers so they can be monitored by the program. The register can thus be read by the program to find the specific error condition.

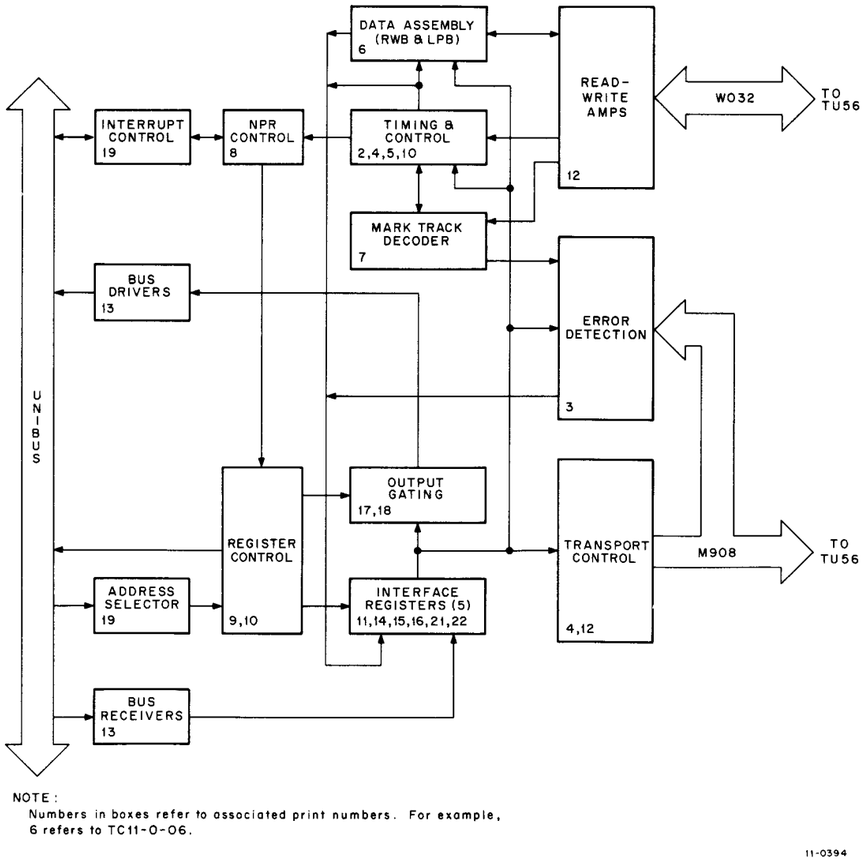


Figure 5-2 TC11 Controller Block Diagram

If the controller has been selected for a read operation, the registers activate the transport control logic as before to select the transport and the function to be performed. The tape transport read heads read the information from the tape and feed it into the read-write amplifiers. These amplifiers are connected to controller logic in such a way that mark track codes are decoded by the mark track decoder, timing track data is fed to the timing and control logic, and data from the data tracks is applied to the data assembly logic, which assembles the information and loads it into the data buffer register. When the data has been properly loaded into this interface register, it can be transmitted through the output gating logic and bus drivers to the Unibus where it is available to the program, or transferred directly to memory storage.

During either write or read data functions, the controller can request the bus when it needs another word from memory or when it desires to transmit a word to the bus. In these cases, a non-processor request (NPR) is generated by the controller. The timing and control logic generates the signal that activates the NPR control. The NPR control and interrupt control logic issue the bus request and receive the bus grant from the processor. The NPR control logic then activates the appropriate register control logic to select either a DATO (transmit a word to the bus) or DATI (receive a word from the bus) operation. The register control logic also enables appropriate address lines so that data is sent or received from the required bus address.

The interrupt control logic is also used to issue vectored interrupts. An interrupt request is generated whenever the controller is ready to execute a new command or whenever an error condition exists.

5.5 ADDRESS SELECTION

The TC11 Controller selection logic decodes the address on the bus lines to determine if the controller has been selected for use. Unique addresses are assigned to each of the five registers in the controller. The manipulation of these registers determines whether information is to be written on or read from the tape or if some other control function is to be performed.

The TC11 Controller consists, basically, of five registers (or bus addresses). In addition to decoding the incoming address, the selection logic controls the information flow between the Unibus and the controller registers. The logic produces SELECT line and gating IN or OUT signals, which determine the register to be used and whether it is to perform an input or output function.

The selection logic consists of an M105 Address Selector Module and register control gating logic.

5.5.1 Address Selector Module

The M105 Address Selector Module (drawing TC11-0-19) decodes the address information from the bus and provides three gating signals (IN, OUT LOW, and OUT HIGH) and five select line signals (SELECT 0, 2, 4, 6, and 10) that activate appropriate TC11 Controller logic circuits for the selected register. The M105 module (etch revision C or later) jumpers are arranged so that the module responds only to the standard device register addresses 777340 through 777356. Although these addresses have been selected by DEC as the standard assignments for the TC11 Controller, the user may change the jumpers to any address desired. However, any MainDEC program (or other software) that references the TC11 standard address assignments must be modified if other than the standard assignments are used.

A normal M105 module provides only four select line signals. However, the M105 used in the TC11 Controller is wired slightly different because five select line signals are required. Address line A03 is fed into a bus receiver external to the module and then ANDed with the SELECT 0 output from the M105. Thus, rather than using two address lines to provide four select lines, three address lines are used to provide five select lines. These signals are listed in Table 5-1.

Table 5-1
M105 Select Lines

Input Lines A ⟨03:01⟩	Select Lines True (+3V)
0 0 0	0
0 0 1	2
0 1 0	4
0 1 1	6
1 0 0	10
1 0 1	2
1 1 0	4
1 1 1	6

Pin L2 of the M105 is normally used as a test point. However, in the TC11 Controller, this pin is used to provide the REG SELECT signal, which is the logical OR of the select lines and indicates that one of the five registers has been selected for use. When the REG SELECT signal is present, it activates a timing chain that ultimately produces the SSYN response (see drawing TC11-0-10 and the timing diagrams, drawing TC11-0-25 through TC11-0-28).

It is beyond the scope of this discussion to cover operation of the M105 Address Selector; detailed descriptions of this module are covered in the *1970 DEC Logic Handbook* and in the *Unibus Interface Manual, Second Edition* (DEC-11-HIAB-D).

5.5.2 Gating Logic

The gating and select line signals from the M105 Address Selector are applied to the register control gating logic (drawing TC11-0-09). This logic provides the pulses that activate appropriate controller registers.

The five select line signals indicate which register is being referenced as follows:

SELECT 0 – TCST (Status Register)

SELECT 2 – TCCM (Command Register)

SELECT 4 – TCWC (Word Count Register)

SELECT 6 – TCBA (Bus Address Register)

SELECT 10 – TCDT (Data Register)

The gating signals (IN, OUT LOW, OUT HIGH) determine the direction of data flow. Note that direction on the Unibus is defined in relation to the master device, which in this case is the processor. Thus, IN H means that the processor is reading information from the selected register, and OUT (or ~ IN) means that the processor is loading data into the selected address. The ~ IN signal is used to load registers defined to be words rather than bytes.

The select line and gating signals and their associated functions are listed in Table 5-2.

Table 5-2
Gating and Select Line Signals

SEL 10	SEL 6	SEL 4	SEL 2	SEL 0	Gating Signal	Function	Reg	Bus Cycle
0	0	0	0	1	IN	Status to bus	TCST	DATI or DATIP
0	0	0	1	0	IN	Command to bus	TCCM	DATI or DATIP
0	0	1	0	0	IN	Word count to bus	TCWC	DATI or DATIP
0	1	0	0	0	IN	Bus address to bus (NOTE 4)	TCBA	DATI or DATIP
1	0	0	0	0	IN	Data to bus	TCDT	DATI or DATIP
0	0	1	0	0	~IN	Bus to word count	TCWC	DATO or DATOB
0	1	0	0	0	~IN	Bus to bus address (NOTE 4)	TCBA	DATO or DATOB
1	0	0	0	0	~IN	Bus to data	TCDT	DATO or DATOB
0	0	0	0	1	OUT LOW	Bus to extended data (NOTE 1) Bus to MAINT (NOTE 2) Bus to RWB (NOTE 3)	TCST	DATO or DATOB
0	0	0	1	0	OUT LOW	Bus to command (low byte)	TCCM	DATO or DATOB
0	0	0	1	0	OUT HIGH	Bus to command +1 (high byte of command register)	TCCM+1	DATO or DATOB

NOTES: 1. MAINT bit must be clear.
2. If MAINT bit set, allows loading of MMT and CLK.
3. If MAINT bit set and read function used, allows loading of the read/write buffer (RWB2 0)
4. TCWC, TCBA, and TCDT are word-only registers.

5.6 BUS CONTROL

The TC11 Controller communicates with the processor, memory, and other storage devices through the Unibus. The controller is connected to the bus data and address lines through input buffering and output driving gates. Most of the data originates, and ultimately is stored or received by, locations external to the controller. In addition, command functions come from programmed instructions provided by the processor. Therefore, during normal tape system use, the majority of information transfers take place through the Unibus.

In addition to being connected to the Unibus, the TC11 Controller is connected to the TU56 Tape Transport by two busses. The first bus is an M908 command bus, which is used to transmit signals to the tape units. These command signals cause the tape unit to perform the required function. The second bus is a W032 analog signal bus, which is used to transfer data between the controller and the tape unit. Information read or written passes through this bus as shown on the TU56 Connections drawing, D-BS-TC11-0-12.

The Unibus control logic performs three main functions:

a. NPR transfers

b. interrupts

c. slave response.

Each of these functions is briefly explained in Table 5-3 and discussed in detail in the following paragraphs.

Table 5-3
Bus Control Functions

Function	Controller Status	Bus Cycle	Description
NPR Transfer	Bus Master	DATO	The bus control logic requests control of the bus for NPR *data* transfers whenever the controller is ready to send data to the bus (read data function).
		DATI	The bus control logic requests control of the bus for NPR *data* transfers whenever the controller is ready to receive data from the bus (write data function).
Interrupt Request	Bus Master	INTR	The bus control logic issues an interrupt request if the controller requires servicing by the program either because it is ready to begin a new operation or because an error condition exists. INT ENB must be set.
Slave Response	Bus Slave	DATO †DATOB ††DATI ††DATIP	Whenever the TC11 Controller is selected for use, it must respond with SSYN in order for the command instructions to be supplied by the processor or other bus master. This logic provides the proper slave response.

†This bus cycle is illegal for the TCWC, TCBA, and TCDT registers as these are word-only registers.
††The DATI and DATIP bus cycles are treated identically by the TC11.

5.6.1 NPR Transfers

The NPR control logic circuits are shown on drawing TC11-0-08. The main portion of the control logic consists of an M796 NPR Control Module. This module permits the TC11 Controller to gain control of the bus and, as bus master, to transfer data to and from any slave device on the bus. This operation is performed independently of processor control and is often referred to as "direct memory access".

The logic necessary to gain control of the bus is provided by the M7820 Interrupt Control Module (drawing TC11-0-19), which generates the nonprocessor request (NPR).

NOTE
Earlier versions of the TC11 use an M782 or M7820 Interrupt Control Module. The prime differences between the three modules are:

M782 –drives bus D⟨07:02⟩ for vector address range of 000–377. Jumper for 0.

M7820–drives bus D⟨08:02⟩ for vector address range of 000–777. Jumper for 0.

M7821–drives bus D⟨08:02⟩ for vector address range of 000–777. Jumper for 1.

When the proper responses are received from the processor, the M7820 asserts BUS BUSY to indicate bus control. On becoming bus master, the controller is free to conduct a data transfer. A DATI cycle is performed if the device needs data from a bus address; a DATO cycle is performed if the controller transmits data to memory or some other device. Basically, a DATI is used during write operations, and a DATO is used during read operations.

The signal that controls selection of a DATI or DATO is the function 3 (FCT 3) signal. This bit is always clear for read operations (octal numbers 1, 2, and 3) and is always set for write functions (octal numbers 5, 6, and 7). However, a bus cycle is performed only for WDATA and RDATA functions. Therefore, by using this bit for bus cycle selection, the proper cycle is used for the selected function (read = DATO, write = DATI).

An NPR sequence is initiated by the SET REQUEST pulse (drawing TC11-0-0-5), which is generated whenever the controller needs to obtain a word from memory for writing or needs to transfer a word to memory for reading. This pulse direct sets the REQUEST BUS flip-flop (drawing TC11-0-08). With the REQUEST BUS flip-flop set, the Master Control B section of the M7820 Interrupt Control Module generates a request on BUS NPR (TC11-0-19). When the processor has completed its current bus cycle and all higher priority device requests have been satisfied, the processor issues a grant on BUS NPG. The M7820 module responds with BUS SACK, and, when BUS SSYN, BUS BBSY, and BUS NPG are negated (indicating the bus is free), the M7820 claims bus control by asserting BUS BBSY.

At this time, the M7820 Interrupt Control Module produces a MASTER B signal, which activates the M796 NPR Control Module. This MASTER B signal produces an internal START signal in the M796. Detailed descriptions of both the M7820 Interrupt Control and the M796 NPR Control modules are provided in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D. Note, however, that in the Interface Manual, the M796 is referred to as the Unibus Master Control Module.

Regardless of the bus cycle selected, a bus address must be used to indicate where the controller is to send or receive data. The M796 module produces the ADRS TO BUS signal which enables the address line drivers in the bus address register (TCBA).

When a read operation is performed, the controller reads information from the tape, formats it by means of the read/write buffer (RWB), assembles it in the data register (TCDT), and, when the word is properly assembled and stored, sends the word to the bus. This is a DATO bus operation. When a DATO is selected by the M796 module, the module produces the NPR DATA TO BUS signal, which produces the DAT TO BUS signal (see drawing TC11-0-09) which enables the output gating logic so that the information in the data register is gated onto the bus. After the necessary Unibus time delays, BUS MSYN is asserted and, thus, a slave is selected. When the slave responds with SSYN, MSYN is dropped and the bus cycle is complete.

When a write operation is performed, the controller receives information from the Unibus, holds it temporarily in the data register while the data is shifted into the read/write buffer, and transmits it to the write heads for writing on the magnetic tape.

When a DATI is selected by the M796 module, the module first produces the ADRS TO BUS as usual but, rather than produce an NPR DATA TO BUS, the M796 waits for the slave to respond and then produces two sequential pulses: NPR DATA CLEAR and NPR DATA STROBE. The NPR DATA CLEAR pulse allows time for the data on the Unibus to deskew and settle. This pulse is also used internally (see drawing TC11-0-09) to produce CLEAR DATA and CLEAR XDAT, which clears the 18-bit data register (TCDT). The second pulse (NPR DATA STROBE) is used to produce BUS TO DAT (drawing TC11-0-09), which is used to direct set those bits in the data register that are being loaded with a 1.

Note that as a result of this DATI cycle, XDATA bits 17 and 16 are cleared. The trailing edge of NPR DATA STROBE is tied back into the M796 and, as a result, MSYN is dropped and the bus cycle is complete.

At the end of either bus cycle, the CLEAR BUS pulse is generated (drawing TC11-0-08). This pulse is used to increment the bus address (TCBA) and word count (TCWC) registers by means of the INC WC & BA signal (drawing TC11-0-08). The trailing edge of CLEAR BUS clears the REQUEST BUS flip-flop, which drops at the input to the M782 Interrupt Control, which, in turn, drops BUS BBSY.

A time-out flip-flop, referred to as NEX (nonexistent memory), in the M796 is set if a SSYN response from the slave device does not occur within 20 μs after BUS MSYN is asserted by the controller. When this flip-flop is set, the bus cycle is not performed and the NEX error bit in the status register is set by the error logic circuits. However, the END CYCLE pulse is produced which increments the word count and bus address registers even though no transfer occurred.

The additional logic gates shown on drawing TC11-0-08 are used to provide signals used during NPR transfers. If the REQ BUS flip-flop is set and the REV (1) signal is present, indicating that the tape is moving in the reverse direction and that data is about to be transferred to or from memory, the OBVERSE ENB H signal is produced to enable one leg of the AND/OR inputs to the data register so that the obverse complement function can occur.

When writing in reverse, a DATI operation is performed (FCT 3 bit set) and obverse is enabled, then at the end of the bus cycle (after the data has been loaded into the data register by means of DATA STROBE), the CLEAR BUS pulse is gated through to produce CLOCK DAT (drawing TC11-0-08). The data in the data register is, therefore, obverse complemented; for example, bits 15 and 02 are swapped and complemented in the process.

When reading in reverse, a DATO operation is performed (FCT 3 bit clear), the same CLOCK DAT pulse is generated at the instant the TC11 Controller becomes bus master (this is indicated by MASTER B H on drawing TC11-0-08). Thus, just as the cycle is starting, the data can be obverse complemented before being sent to the Unibus.

Thus, the CLOCK DAT signal strobes information into the data register flip-flops if any one of three conditions exist: *a)* a write operation is being performed while the tape is moving in the reverse direction; *b)* a read operation is being performed while the tape is moving in the reverse direction; *c)* both the READY and REQ BUS flip-flops are clear, indicating an internal transfer is being performed. The latter condition occurs during all read and write operations.

If either a read or write data operation is being performed (RWDAT H) and the current operation is complete (CLEAR BUS H), then the INC BA-WC signal is produced to increment the bus address register and the word count register to the next value.

The timing diagram for DATI NPR transfers is shown on drawing TC11-0-27, and the timing diagram for DATO NPR transfers is shown on drawing TC11-0-28.

5.6.2 Interrupt Request

An interrupt request is generated when the controller is ready to send or receive data to or from the bus or whenever an error condition exists. Interrupt requests are controlled by the M7820 Interrupt Control Module shown on drawing TC11-0-19.

The M7820 module provides the logic necessary to make bus requests and gain control of the bus (become bus master). The module also includes the circuits necessary for generating an interrupt. The module contains two completely independent request and grant acknowledge circuits (channels A and B) for establishing bus control. The following paragraphs provide a brief functional description of both channels. A detailed description of the M782 module, including circuit schematics, is contained in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D.

Channel B (MASTER CONTROL B) is used only for NPR requests and is activated when the REQ BUS flip-flop is set as described in Paragraph 5.6.1. The output of channel B activates the NPR control logic so an NPR DATI or DATO function can be performed. No vector address is used with this channel.

Channel A (MASTER CONTROL A) is used to generate interrupts. This channel is activated by the ANDing of two signals: INT ENB (interrupt enable) and TC INT (controller interrupt). The first signal occurs whenever the interrupt enable (IE) bit in the command register (TCCM) is set by the program. The second signal is produced by a series of logic gates. The NOR gate that produces TC INT has as inputs READY (1) L and another input that is normally enabled. Thus, whenever READY is set or there is an error condition (which forces READY to be set), TC INT is true. The other input to the NOR gate is used to momentarily turn TC INT off, allowing the circuit in the M7820 to return to its rest state. Thus, if READY is set, producing TC INT, and an error condition develops, ERROR L triggers the M606 one-shot (50 to 100 ns), which momentarily removes TC INT. In a similar manner, if the DO bit is set, DO STROBE performs the same momentary disabling of TC INT.

The jumpers on the M7820 module are wired for a standard vector address of 214. Other vector addresses can be selected by the user, provided the jumpers are changed accordingly. However, all DEC programs reference the standard address of 214 and must be modified if any other address is used.

A timing diagram of the ready and error sequence is shown on drawing TC11-0-26.

5.6.3 Slave Response

When the TC11 Controller participates in a data transfer as a slave device, the slave response logic provides the necessary acknowledgement signals required by the bus master. The slave response logic is shown on drawing TC11-0-10, and the timing diagram is shown on drawing TC11-0-25.

The master device places the address of the TC11 Controller on the bus A lines, data to be transferred on the bus D lines, and signals on the bus C lines to select the appropriate register and function to be performed.

The master device waits 150 ns (75 ns to allow for worst case signal skew and 75 ns for address decoding) and then asserts BUS MSYN, provided the bus is clear (SSYN is clear).

When the controller decodes the address, it produces the REG SELECT signal at the time MSYN is received. The REG SELECT signal triggers the SLAVE CLEAR one-shot, which is sometimes used to clear the selected register in the controller. Following the 500-ns clear signal, the SLAVE STROBE one-shot is fired. At this time the controller sometimes strobes in the data from the bus lines. At the end of this second 500-ns interval (when SLAVE STROBE times out), the SSYN flip-flop is set and BUS SSYN is asserted.

The master device receives SSYN, clears MSYN (which clears REG SELECT), and triggers a third 500-ns time delay, D10T2 (output pin). When the 500-ns time delay times out, the controller clears the SSYN flip-flop, negating BUS SSYN to signify the end of the bus transaction.

5.7 BUS DRIVERS AND RECEIVERS

The bus drivers and receivers provide the signal levels required for compatibility with the Unibus. The M798 Transmitter Module contains bus drivers for interfacing controller outputs to the bus. The M784 Receiver Module contains inverting circuits that provide buffered bus signal outputs that are used as inputs to the controller.

The bus receivers are used primarily on the input lines to the various controller registers. The bus transmitters are used in the output gating circuits.

The M783, M784, and M798 modules are described in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D. Figure 5-3 shows a typical driver/receiver.

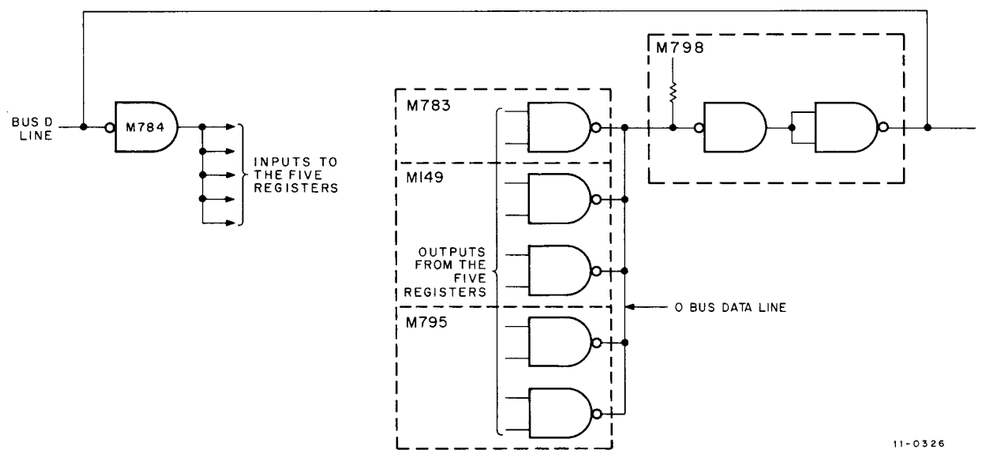


Figure 5-3 Typical Driver/Receiver

5.8 REGISTERS

All software control of the TC11 Controller is performed by five device registers. These registers are assigned Unibus addresses and can be read or loaded with any PDP-11 instruction that refers to their address (with certain exceptions such as load only, read only, or unused bits). Table 5-4 lists these registers and the function of each. Subsequent paragraphs discuss each of the registers and the register control from a hardware standpoint. A discussion of the registers from a programming standpoint is presented in Chapter 4.

An additional internal register is also discussed in this section. This is the read/write buffer (RWB) register covered in Paragraph 5.8.7.

Table 5-4
Device Register Functions

Register	Mnemonic	Function
Control and Status Register	TCST	provides detailed information on the status of the TC11 Controller. Such information includes error indications and tape up-to-speed indication.
		provides maintenance functions such as simulation of timing track and mark track.
	TCST	provides the two extended data bits for the data register.
Command Register	TCCM	main control register in the TC11 Controller. Specifies the operation to be performed on the tape unit. Also indicates the status of the operation that was selected.
		provides the two extended address bits for the bus address register.
Word Count Register	TCWC	counts the number of words transferred during read data or write data operations. The 2's complement of the desired word count is preset by program. When register counts the number of specified words, it prevents further transfers.
Bus Address Register	TCBA	specifies the bus or memory address to or from which data is transferred during read data and write data operations. After each transfer is completed, the register automatically increments to the next word location.
		Note that incrementation is by two; this register is not used with byte instructions.
Data Register	TCDT	contains the information read from or written on the tape. Accepts program data during write modes; during read modes holds the data read from the tape. During read data and write data, the register buffers information between the controller and the Unibus.

5.8.1 Register Control

The register control logic (drawing TC11-0-09) provides the pulses that activate a specific register for use. This selection is described in Paragraph 5.5.2. In addition, the register control provides certain maintenance signals (refer to Paragraph 5.12) and signals used with the data register (refer to Paragraph 5.8.4) and the read/write buffer register (refer to Paragraph 5.8.7).

5.8.2 Command Register

The command register is the main control register in the TC11 Controller. Most of the 16 bits in this register are set or cleared to specify operations to be performed by a particular tape unit. Such operations include transport selection, direction of tape motion, and selection of read, write, or stop functions. In addition, the register contains an error bit which is the inclusive OR of all error conditions in the controller.

Three bits in the command register are used to select one of eight possible read, write, or stop functions. The function logic consists of a binary-to-octal decoder that decodes these three bits and provides a signal representing the selected function. The decoder signal is then used throughout the controller logic to perform the function.

The tape control logic uses signals from the command register, the status register, and the selection logic. These signals pass through various gating networks and delays to produce the signals needed to perform the desired tape control functions such as stop, go, forward, and reverse.

Each of the bits in the command register is discussed separately in the following paragraphs, beginning with the most significant bit.

5.8.2.1 Error Bit (15) – The ERROR bit (bit 15) is the inclusive OR of all error conditions in the status register. If any error condition exists, the status register generates a level that passes through an OR gate (drawing TC11-0-03) and produces an ERROR H signal. This signal is also fed through an inverter to produce ERROR L. The ERROR L signal passes through another OR gate (drawing TC11-0-02) and inverter to place a low level on the direct-set input of the READY flip-flop, which is bit 7 of the command register. With these two conditions existing [ERROR L and READY (1) L], a series of gates (drawing TC11-0-19) produces a TC INT H signal. This interrupt signal is applied to the MASTER CONTROL A section of the M7820 Interrupt Control Module. If INT ENB (1) is high (command register bit 6 set), then the controller performs an interrupt routine. Thus, any error causes an interrupt provided the interrupt enable (IE) bit is set.

The error conditions (except ILO and SELE) can be cleared by loading a 0 into the ERROR bit. As shown on drawing TC11-0-03, the BUS TO TCCM+1 signal, which indicates the command register is being referenced, is ANDed with the ~B D15 L signal, which indicates a 0 loaded into bit 15. The output of the AND gate passes through two OR gates to produce the RESET ERRORS L signal. This signal clears all error flip-flops. Note, however, that the ILO and SELE errors are produced by switch settings rather than flip-flops and are, therefore, not cleared by the RESET ERRORS signal. These errors are cleared by manually correcting the switch settings or selecting another unit. Note also that the RESET ERRORS signal can be produced by either a bus initialize (BINIT) or DO CLEAR signal.

5.8.2.2 Maintenance Bit (13) – The MAINT bit (bit 13) enables operation of bits 06 through 02 in the status register. The MAINT flip-flop (drawing TC11-0-11) is set by the BUS TO TCCM+1 H signal, which indicates that the command register has been referenced for use, and the BD13 H signal, which indicates that bit 13 is to be set. When the MAINT flip-flop is set, it enables generation of BUS TO MAINT (drawing TC11-0-09). Both the MMT and CLK flip-flops can now be set or cleared by loading appropriate bits in the status register (drawing TC11-0-10).

The MAINT, MMT, and CLK flip-flops are cleared by a bus initialize (B INIT) signal.

When the MAINT bit is set, it performs the following:

a. Deselects all tape transports.
b. Disables selection (SELE) error.
c. Disables WRITE LOCK switch.
d. Enables the MMT to shift into the window on TP1.
e. Forces UPS set (bypasses the 120-ms delay).
f. Disables loading of extended data bits XD17 and XD16.
g. Enables loading of CLK and MMT.
h. Enables loading of DT2, DT1, and DT0 only if the function is RALL, RNUM, or RDATA. Any other function or MAINT = 0 disables any modification of these bits.

5.8.2.3 Delay Inhibit Bit (12) – The delay inhibit bit (DINHB) shortens the delay associated with bringing a tape transport up to speed. Normally, a 120-ms delay is triggered whenever a transport is selected. However, if the DINHB bit is set, the delay is shortened to 10 ms. (The DINHB is used when selecting a transport known to be up to speed in order to make more efficient use of program time.)

The time-delay interval is necessary when deselecting a previous transport and selecting a new transport. Switching from one transport to another is relatively slow because the five head signals of each unit are switched on to and off of the analog signal bus by reed relays (G851 module).

The DINHB bit (drawing TC11-0-11) is one section of a 4-bit counter/storage element. It is loaded by the BUS TO TCCM+1 signal, which indicates that the command register is being used, and by the data on bus data line BD12, which indicates the status of bit 12. When bit 12 is a 1, the output of DINHB is the DINHB (1) signal, which is also inverted to produce DINHB (0) H. Note that the counter is not used as a counter but can be functionally considered to be four flip-flops.

The up-to-speed delay circuits are shown on drawing TC11-0-04. If the inhibit is not used, the DINHB (0) H signal is high and is ANDed with the high output of the 120-ms delay circuit. This produces a low on the direct clear input of the UPS flip-flop and prevents it from being set for the duration of the delay. If the DINHB bit in the command register is set, the DINHB (0) H signal is low and prevents the output of the 120-ms delay from being gated. The low side of the 10-ms delay circuit passes through the OR gate and holds the direct clear side of the UPS flip-flop low for 10 ms. This delays setting of the flip-flop for 10 ms. Note that this delay holds UPS clear which inhibits the generation of TP timing pulses.

The DINHB bit is cleared by the BINIT signal, which is internally called RESET on the counter/storage module. Refer to programming note 8 (Paragraph 4.6) for an explanation of the proper method of using the DINHB bit.

5.8.2.4 Reverse Bit (Bit 11) – The reverse bit (bit 11) specifies the direction of tape motion. When set, it specifies the reverse direction. When clear, it specifies forward direction.

The reverse bit is controlled by the REV flip-flop shown in drawing TC11-0-11. The clock input to the flip-flop is the BUS TO TCCM+1 signal, which indicates the command register has been selected for use. The data input to the flip-flop is bus data line BD11. When a 1 is on this line, it sets the flip-flop indicating reverse direction. A 0 on the line clears the flip-flop, indicating forward direction.

The output of the REV flip-flop is applied to the motion control logic circuits shown on drawing TC11-0-04. These circuits are described more fully in Paragraph 5.9.2. The REV flip-flop is cleared by the B INIT signal.

5.8.2.5 Unit Select Bits (10–08) – The three UNIT SELECT bits (bits 10 through 08) specify the tape unit that is to be used for a particular operation. The state of these three bits represents an octal code corresponding to the number of the unit as set by the unit selector switch on the tape transport.

The three UNIT SELECT bits are shown on drawing TC11-0-11. These three bits (UNIT 3, UNIT 2, UNIT 1) are set or cleared by loading 1s or 0s from bus lines 10, 09, and 08. Each bit that is set produces a respective UNIT (1) H.

The three unit select signals [UNIT 3 (1) H, UNIT 2 (1) H, and UNIT 1 (1) H] are applied to a binary-to-octal decoder shown in drawing TC11-0-12. Depending on which signals are high, one of eight tape units is selected for use as long as the decoder is enabled.

The decoder (M161 module) is enabled when the AND gate on its input is satisfied. The decoder is disabled if any one of the following conditions occur:

a. The MAINT bit is set. This ensures that no transports are selected when using the maintenance mode.

b. The SAT function is used. This ensures that no units are selected after INIT. INIT clears function bits to 0, which is SAT.

c. NEW UNIT SELECT is asserted (this disables the decoder only momentarily). This prevents spurious unit selections from occurring while the UNIT SELECT bits are being altered.

The NEW UNIT SELECT signal (drawing TC11-0-04) detects modification of the UNIT SELECT bits of a change in the REV bit. This signal triggers the 120-ms delay required in order to bring a transport up to speed. A delay is necessary for the following reasons:

a. If the UNIT SELECT bits are changed, the previously selected transport must deselect, and the newly selected transport must select.

b. The tape must be moving above a certain speed to ensure that timing and data are read properly. Thus, reading of the tape must be inhibited while a unit accelerates from a stop to operating speed.

c. When a tape is to be "turned around" (that is, when a forward moving transport is switched to reverse or vice versa), reading of the tape must be inhibited until the tape is moving fast enough in the new direction. Thus, during turnaround, reading a tape is inhibited while the tape is slowing down, while the tape is momentarily stopped (the read amplifiers oscillate at this point), and while accelerating in the opposite direction.

5.8.2.6 Ready Bit (07) – The ready bit (bit 07) indicates that the controller is ready to receive a new command. It is set (indicating ready) whenever the previous command is completed, an initialize signal is given, or an error condition exists. It is cleared when a DO command is issued.

The READY flip-flop is shown on drawing TC11-0-02. A series of gates are connected to the direct set input of the flip-flop. If the B INIT signal goes high (indicating initialize), the ERROR signal goes high (indicating some type of error condition), a stop (STP) function is performed, or the block number has been read, the output of the OR gate goes high, passes through the inverter, and direct sets the READY flip-flop.

The clock input to the flip-flop is derived from an AND gate that is qualified when READY is clear. This allows the timing pulse, TP00, to clock the flip-flop.

The data input to the READY flip-flop is controlled by a series of gates that provide a high level to the data input of the flip-flop whenever certain conditions are met. A simultaneous high data input and a clock sets the flip-flop. Note that when the flip-flop is set, the clock is disabled.

The conditions that provide the high data input to the flip-flop specify completion of the function and are indicated by qualifying a gate with the function signal, a READY ENABLE signal, and a timing pulse. These functions are: WRTM (write timing and mark), RDATA (read data) or WDATA (write data), RALL (read all), and WALL (write all).

READY is cleared by the direct-clear input to the flip-flop. It is held low by a series of gates when the data register is being referenced as indicated by SELECT 10 H, IN H, when the function is RALL, WALL, or WRTM. When a DO command is issued, the DO STROBE goes high and direct-clears the READY flip-flop, indicating that a command is now being executed.

5.8.2.7 Interrupt Enable Bit (06) – The interrupt enable (IE) bit permits an interrupt to occur provided either the READY or ERROR bit is set. The IE bit is shown on drawing TC11-0-11. This bit is set by using the BUS TO TCCM H signal as a load pulse to load a 1 from bus line BD06. INTR ENB (1) H is applied to one input of an

AND gate in the MASTER CONTROL A section of the M7820 Interrupt Control Module (drawing TC11-0-19). The other input to the AND gate is the TC INT signal, produced if either the READY or ERROR flip-flop is set.

The INTR ENB bit is cleared by the B INIT H signal (also referred to as RESET on the drawing).

5.8.2.8 Extended Bus Address Bits (05 and 04) – The extended bus address bits 05 and 04 represent bus address bits A17 and A16, respectively. These bits are used to specify 18-bit addresses when required, because the bus address register is only 16 bits long. Although functionally part of the bus address register (TCBA), these bits are loaded by a BUS TO TCCM signal, which indicates that the command register has been selected for use. The bus address register can be incremented and any incrementation also affects the two extended address bits. These bits are cleared by the B INIT (RESET) signal.

5.8.2.9 Function Bits (03, 02, 01) – The three function bits are set or cleared to provide an octal code that selects any one of eight commands that control operation of the tape system. These commands are used for reading or writing data on the tape and for controlling tape motion.

The three function bits (FCT 3, FCT 2, FCT 1) are shown on drawing TC11-0-11. The appropriate 1 or 0 on the associated bus data line is loaded into the flip-flop by means of a load pulse, which is BUS TO TCCM H. The output of each flip-flop is inverted so that a high level is present for a 0 or a 1.

The (1) H line from each of the three function bits is applied to a binary-to-octal decoder (drawing TC11-0-05), which decodes the state of the three bits and provides the selected function signal. The appropriate function signal is then applied to control logic to institute the function. Note that the decoder is disabled when the DO STROBE signal is present. This prevents the decoder from producing spurious signals while the function bits are being loaded.

5.8.2.10 DO Bit (bit 00) – The DO bit initiates operation of the selected function. This bit is not a flip-flop but simply an AND gate (drawing TC11-0-05). When a 1 is loaded into bit position 00, it is ANDed with OUT LOW H and SELECT 2 H, which is, in effect, the BUS TO TCCM operation. Note that there are three derivatives at DO as shown in Figure 5-4. The DO STROBE signal is applied to the reset side of the READY flip-flop (drawing TC11-0-02).

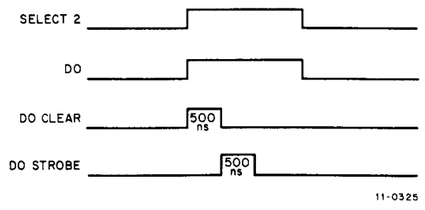


Figure 5-4 Derivatives of DO Signal

5.8.3 Status Register (TCST)

The status register is primarily used to provide indications of error conditions. In addition, it provides certain maintenance functions.

The status register error logic is shown on drawing TC11-0-03. Whenever an error signal is present, it passes through an OR gate, which is the inclusive OR of all error conditions. The resultant output signal (ERROR L) sets the READY flip-flop in the command register. This allows the controller to issue an interrupt request whenever an error exists. All error bits (15 through 08) in the status register are read-only bits. They can be read (tested) by the program to determine if a specific error exists or not, but they cannot be loaded by the program.

The select (SELE), illegal operation (ILO), end zone (ENDZ) and mark track error (MTE) bits stop the selected tape transport when set. This is accomplished by means of the logic shown on drawing TC11-0-04. If any one of these bits is set, it inhibits the GO pulse and stops the transport.

The up-to-speed (UPS) bit and all error bits except ILO and SELE are cleared by either generating an initialize signal (B INIT) or by loading a 0 into the ERROR bit or a 1 into the DO bit of the command register.

Each individual error bit is discussed separately in the following paragraphs.

5.8.3.1 End Zone Error – The ENDZ flip-flop is bit 15 of the status register and indicates that the selected transport is moving forward in the forward end zone or reverse in the reverse end zone. This represents an error condition because if tape motion continues in the same direction, the tape can run off the reel.

The ENDZ flip-flop (drawing TC11-0-03) is set at TP0 time provided MK END H is also present. The MK END H (mark end zone) is generated by the mark track decoder when it decodes the end zone mark (22) as the tape passes through the end zone associated with its direction of motion. Note that the mark track code 55 is read as 22 in the reverse direction.

The ENDZ flip-flop is cleared by RESET ERRORS L, which is produced by a series of gates shown on drawing TC11-0-03. This signal is generated: if BD15 H is not present and BUS TO TCCM+1 is present (loading a 0 into the ERROR bit of the command register); if B INIT L is present (indicating an initialize operation); or if DO CLEAR H is present (indicating a 1 loaded into the command register DO bit).

5.8.3.2 Parity Error – The PAR (parity) flip-flop (drawing TC11-0-03) is bit 14 of the status register and indicates that, during the read data operation, the calculated and written parity values disagree.

The RDATA and clock inputs to the AND gate ensure that the parity error flip-flop can be set only during reading of data at the proper clock time after the first two characters of the forward parity area are read. If the LPB register does not contain all 1s, the AND gate is qualified and the PAR flip-flop is set. The PAR flip-flop is cleared in the same manner as the ENDZ flip-flop (refer to Paragraph 5.8.3.1).

Note that the condition for proper block parity is for the longitudinal parity buffer (LPB) to contain all 1s after reading the six bits of REV CHECK, all data words, and the six bits of FOR CHECK. If this is not the case, then the PAR flip-flop is set. Also note that parity is checked block-by-block even during a continuous multiple block transfer.

5.8.3.3 Mark Track Error – The mark track error (MTE) flip-flop (drawing TC11-0-03) is bit 13 of the status register and indicates an error in the decoding of the mark track. Although the mark track decoder ensures that a decoded mark track follows a specific mark track bit configuration, the MTE flip-flop logic checks to make certain that valid marks are decoded every six bits of the mark track during certain time states. The MTE flip-flop is cleared in the same manner as the ENDZ flip-flop (refer to Paragraph 5.8.3.1).

The clock for the MTE flip-flop is derived from C3. When C3 clears, the flip-flop is clocked. When the flip-flop is set, the clock is disabled. The MTE sets when clocked if the D input is low. This D input is derived from a series of gates that check to verify that if the controller is not in ST IDLE or ST BLK MK states, then the decoder should be decoding a MK END, a MK BLOCK END, a MK DATA, or a MK BLOCK START. If this is not true, the D input is low, and the MTE flip-flop is set when C3 clears.

5.8.3.4 Illegal Operation Error – The illegal operation (ILO) error is bit 12 of the status register and indicates a conflict between the manual switch positions and the selected function. The ILO logic (drawing TC11-0-03) consists of gating logic rather than a flip-flop.

The ILO logic consists of three 2-input AND gates, each gate representing one of the three illegal operations. The first gate is qualified by the write function (WRITE H) and the WRITE ENABLE/WRITE LOCK switch in the WRITE LOCK position (~WRITE OK). This indicates an attempt to write with the write function disabled.

The second gate is qualified by the write all function (WALL H) and the WRITE ALL switch in the DISABLE position (~WALL EN H). This indicates an attempt to perform a write all function with the associated switch disabled.

The third gate is qualified by the write timing and mark function (WRTM H) and the WRITE T & M switch in the DISABLE position (~WRTM EN H). This indicates an attempt to write timing and mark data with the associated switch disabled.

When any one of these three gates is qualified, it produces the ILO H signal indicating an error and stopping the selected transport. Note that the ILO is cleared by removing the conflict. In other words, the program either changes the function or the operator manually alters the switch position.

5.8.3.5 Selection Error – The selection (SELE) error is bit 11 of the status register (see drawing TC11-0-03) and indicates that either more than one transport has been selected (unit select switch on two or more transports set to the same number) or that a nonexistent transport has been selected (no transport unit select switch set to the number specified by the program).

Each TU56 tape unit produces a SELECT ECHO signal when the unit has been selected for use. This signal is the output of a driver and is applied through a resistor to a signal line common to all units and wired back to the TC11 Controller. The common SELECT ECHO signal line is connected to a G879 Comparator Amplifier. Operation of this amplifier is dependent on the input loading, which is the analog sum of the SELECT ECHO signals. If the input signal is such that it represents either no SELECT ECHO signal or more than one SELECT ECHO signal, the amplifier produces a low level, which is applied to one input of an AND gate. The other leg of the gate (ERROR DISABLE) disables the generation of SELE if the stop all transports (SAT) function is used, the maintenance (MAINT) bit is set, and the delay is active (UNIT SELECT DELAY). This third condition momentarily disables the detection of SELE while deselecting one unit and selecting another.

When the above conditions are met, the AND gate is qualified and produces the SELE H signal indicating a selection error. Because of the gating, the selection error logic is disabled if the MAINT bit is set, or if the SAT function is being used, or if a tape unit is being switched.

5.8.3.6 Block Miss Error – The block miss (BLKM) error flip-flop (drawing TC11-0-03) is bit 10 of the status register. During normal operation, the block number is first read and then the controller issues either a read or write command in order to use the located block. If the read or write function is not started within a specified time after the block number is read, the function would begin in an improper area of the tape because tape motion continues. Therefore, if the read or write function is not started on time, the BLKM error flip-flop is set to indicate an error condition.

Basically, an error occurs if after finding a block, the read or write function is not given before a certain point is reached on the tape. In RDATA or WDATA modes, this point occurs when the BLKM flip-flop is set at ZLPB time, which corresponds to two-thirds through the REV CHECK mark area. (Note that MISS is cleared whenever READY becomes set.) If the function and the DO command are issued after this point, BLKM is set. This allows 2-2/3 marks (or 533 μs) to switch functions after reading a block number.

In the RALL and WALL modes, the controlling flip-flop is READY ENB, which is set two-thirds through the REV LOCK area. This leaves 1-1/3 marks (or 333 μs) for the program to switch functions.

5.8.3.7 Data Miss Error – The data miss (DATM) error flip-flop (drawing TC11-0-03) is bit 09 of the status register. During normal operation, the controller makes an NPR request to gain control of the bus and initiate a data transfer (either read or write). After issuing a request for the bus, the processor must issue a bus grant signal within 67 μs or a data miss error occurs indicating that the request for data transfer was not honored in time. (Data is buffered 1-1/3 times because the RWB holds six bits.)

During WDATA and RDATA modes, the logic controlling the DATM error consists of the REQ BUS flip-flop (drawing TC11-0-08) and the DATM flip-flop shown on drawing TC11-0-03. If the bus request is not granted within the specified time, the REQ BUS flip-flop is set and enables the gate connected to the set line of the DATM flip-flop. DATM is then set if DO is not present when the next TP00 pulse occurs. However, if the request is granted in time, the REQ BUS flip-flop remains cleared, the gate is disqualified, and the DATM flip-flop is not set.

During WALL or RALL modes, DATM is set as a function of READY. In these two modes, the READY flag becomes set for each word to be written or read on the tape. If the program does not respond to the flag within 67 μs (1/3 of a word) by reading or loading the data buffer, then DATM is set at the next TP00 pulse, provided DO is not present. DATM ENB (drawing TC11-0-08) disables clocking of the data register if a transfer is occurring.

5.8.3.8 Nonexistent Memory Error – The nonexistent memory (NEX) error flip-flop is bit 08 of the status register. When set, this bit indicates that the controller was bus master but did not receive a SSYN response from the slave device within 20 μs after asserting the MSYN signal.

The NEX error flip-flop is part of the NPR control circuits on the M796 module (drawing TC11-0-08) and is described in Paragraph 5.6.1.

5.8.3.9 Up-To-Speed – The up-to-speed (UPS) flip-flop is bit 07 of the status register. When this bit is set, it indicates that the selected tape transport has attained a sufficient speed to ensure proper operation.

The UPS flip-flop and associated logic is part of the DECtape control logic shown in drawing TC11-0-04. Whenever a tape unit is selected for use or a turnaround command is given, a 120-ms delay is triggered. The output of the delay circuit holds the UPS flip-flop cleared for the duration of the delay.

When the delay times out, the flip-flop remains cleared until set by means of the C and D inputs. Together, these inputs verify that the rate of incoming timing pulses is high enough to ensure proper tape operation. The retriggerable one-shot associated with the D input is fired on the trailing edge of the PTP0 pulse. The clock is the leading edge of PTP0. Thus, the trailing edge of the first PTP0 pulse fires the one-shot. If the one-shot times out before the leading edge of the next pulse, then the D input is high and the UPS flip-flop remains cleared. When the rate of PTP0 pulses is high enough (less than 70 μs between pulses), then the one-shot does not time out and the D input is low, thus setting the flip-flop when the clock goes high.

The UPS flip-flop is used to enable the generation of timing pulses and the decoding of the mark track. The transitions of the timing track (READ TM), shown on drawing TC11-0-04, produce timing pulses PTP0 and PTP1 provided neither the WRTM or MAINT mode is being used. When UPS is set, PTP0 and PTP1 produce TP0 and TP1. The occurrence of either TP0 or TP1 fires a one-shot that inhibits the generation of any timing pulse for 10 μs. This is necessary because while in a write function, simultaneous writing is being performed in the data tracks. The switching of the write currents is coupled into the timing track, possibly causing false readings. Thus, after each timing pulse, the sensing of the timing track is inhibited for 10 μs. The next timing pulse would normally occur after 17 μs.

The 10 μs one-shot is also used to produce the LPB TP pulse. This pulse generator is enabled by C0 clear. Thus, LPB TP is essentially a delayed TP0 pulse.

UPS is also applied to the M228 Mark Track Decoder. When UPS is clear, the window is held cleared and ST IDLE is forced. Because no marks can be decoded and the system is in ST IDLE, the controller is essentially in a rest state.

A programmer may desire to bypass the UPS delay; for example, if the maintenance mode is used or if a tape unit is selected that is known to be up to speed. This is accomplished by setting the delay inhibit (DINHB) bit in the command register. With DINHB set, the AND gate on the output of the 120-μs delay is inhibited, and the pulse to the direct-clear line of the flip-flop is not present. However, the select signals trigger a 10-ms delay that holds the flip-flop clear until it times out. Thus, if DINHB is used, the UPS flip-flop can be set after the 10-ms delay.

The UPS flip-flop is cleared whenever an INIT signal is issued (because INIT sets the function to SAT) or when a stop function (SAT or SST) is selected. The latter produces the STP signal. An ERROR STP signal also clears the UPS flip-flop. This signal is generated whenever an ENDZ, MTE, ILO, or SELE error occurs. Any modification of the UNIT SELECT bits or the REV bit also clears the UPS flip-flop because the new UNIT SELECT triggers the delay. Thus, any time a new unit is selected, tape motion is reversed, or the tape unit is stopped, the up-to-speed delay triggers when the next function is selected.

The timing circuits associated with UPS are bypassed, and UPS is unconditionally set by TP control during the WRTM function or when the MAINT bit is set.

5.8.3.10 Clock – The clock (CLK) flip-flop is bit 06 of the status register and is used during the maintenance mode to simulate the tape timing track. This bit can only be loaded if the MAINT bit in the command register is set. Setting the flip-flop generates timing pulse TP1; clearing the flip-flop produces TP0.

The CLK flip-flop is shown on drawing TC11-0-10, and the associated gating circuits are shown on drawing TC11-0-04.

If MAINT is set and bit 06 is loaded with a 1, the CLK flip-flop is direct-set. If MAINT is set and bit 06 is loaded with a 0, the flip-flop is direct-cleared.

The MAINT bit being set produces the TP CONTROL signal, which is ANDed with the 0 side of the CLK flip-flop. Depending on whether the 0 side is high or low, a series of gates is qualified to produce the TP1 or TP0 timing pulses.

The clock is also toggled during the WRTM function by a free-running oscillator shown on drawing TC11-0-10. The one-shot is enabled if WRITE ENABLE and WRTM ENABLE is present; the function is WRTM; the controller is not in the MAINT mode; and there is no SELE error. The output of the one-shot is fed back into the input, thereby causing the one-shot to retrigger itself. An intermediate flip-flop phases the toggling of CLK and TAPE CLK so that the two pulses are out of phase by 90 degrees. The CLK pulse is used to generate TP0 and TP1 for internal use. The TAPE CLK is used by circuits shown on drawing TC11-0-12 to write the timing track.

A timing diagram of the various timing pulses mentioned above is shown in Figure 5-5.

5.8.3.11 Maintenance Mark Track – The maintenance mark track (MMT) flip-flop is bit 05 of the status register and is used during the maintenance mode to simulate a bit read from the tape mark track. When the MAINT bit in the command register is set, the resultant BUS TO MAINT signal is applied as a clock input to the MMT flip-flop (drawing TC11-0-10) as an enabling level. The data input is bus data line 05. Therefore, the flip-flop can be set or cleared by loading a 1 or a 0 respectively into bit 05 of the status register.

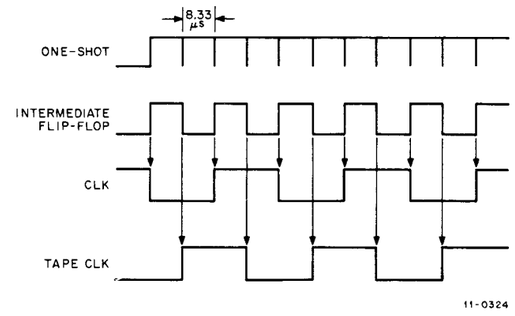


Figure 5-5 Clock Timing Diagram

The MMT flip-flop output is applied through an AND/NOR gate to the mark track decoder (drawing TC11-0-07). As each new bit is loaded into the MMT flip-flop, a corresponding simulated bit is shifted into the mark track decoder when TP1 is generated by the CLK bit. Thus, the programmer can simulate mark track codes and observe operation of the mark track decoder circuits.

5.8.3.12 Data Tracks – The three data track bits (04, 03, and 02) in the status register provide maintenance checks of controller read and write operations. During normal operation, these three bits read the inputs to the write amplifier (RWB 5, 4, 3). Thus, the inputs to the controller can be compared with the inputs to the tape unit to verify controller operation during the write mode.

During the maintenance mode and a read function, these data track bits are loaded into the read/write buffer flip-flops (2, 1, 0) to simulate inputs from the tape unit read amplifiers. When loading these bits, the MAINT bit in the command register must be set and a read function selected. This produces the BUS TO RWB signal that enables the direct set line on RWB 2, 1, and 0. These three bits were cleared prior to loading by the CLEAR RWB 2-0 signal (see drawing TC11-0-09).

The read/write buffer (RWB) is shown on drawing TC11-0-06. Table 5-5 indicates which RWB flip-flops are used to represent specific data tracks during reading and loading.

Note that Table 5-5 implies that, when programming in the maintenance mode, only MOV instructions should be used when attempting to load the CLK, MMT, DT0, DT1, or DT2 bits.

Table 5-5
Data Track Bits

Status Register Bit	Data Track	Read/Write Buffer Flip-Flops	
		Reads As	Loads Into
04	0	RWB5	RWB2
03	1	RWB4	RWB1
02	2	RWB3	RWB0

NOTE: During MAINT mode, use only MOV instructions when loading CLK, MMT, DT2, DT1, DT0 bits.

5.8.3.13 Extended Data – Bits 01 and 00 of the status register are extended data bits 17 and 16 respectively. These bits serve as an extension to the data register so that it can function as an 18-bit rather than a 16-bit register. Normal PDP-11 words are 16 bits long, and it is not often necessary to use these extended bits. However, the word on a magnetic tape consists of six 3-bit characters (18 bits). Use of the extended bits allows reading or writing in all bit positions of a tape word.

Although these two bits are part of the status register and must be addressed with the status register address if they are to be used, they are shown as part of the data register logic on drawings TC11-0-14 and TC11-0-15.

The extended data bits cannot be loaded if the system is in the maintenance mode.

When the system is in the WDATA mode, bits 17 and 16 are cleared and always written as 0s. This clearing operation occurs during the DATI bus sequence but occurs prior to the obverse complement operation.

5.8.4 Data Register (TCDT)

The data register stores data words as they are disassembled or assembled during read and write operations. Basically, this register serves as a buffer for information transmitted between the TC11 Controller and the memory, processor, or other bus device.

The data register is shown on drawings TC11-0-14, 15, and 16. The register consists of 16 data flip-flops (bits 15 –00), two extended data flip-flops (bits 17 and 16), and associated input and output logic.

Loading the register is functionally accomplished in one of two ways. The first method is for the controller to issue an NPR and, as bus master, strobe in data from the bus during a DATI bus cycle. The second method is for the processor (or other device) to select the controller as a slave and strobe data into the controller register during a DATO bus cycle.

When loading data into the data register, one of two methods may be used. The first is the direct-set method. In this case, the register is always cleared first, then strobed. The second method is the D input method in which the register is first enabled, then clocked. These two methods are outlined in Table 5-6 and described briefly below.

When the bus to data function is used, the output of each bus data line is applied to one side of an AND gate. There is one AND gate associated with the flip-flop for that bit position in the register. The gate output is connected to the direct set side of the flip-flop. The AND gate is qualified when the BUS TO DAT H signal occurs. The BUS TO DAT H is produced by the register control circuits (drawing TC11-0-09) and is the result of either an NPR DATA STROBE, which indicates that data is to be strobed in from the bus during an NPR data transfer, or it is the result of SLAVE STROBE, which indicates that the data register has been selected for use by the bus master and, as the slave, is ready to strobe in data from the master device. Note that NPR DATA CLEAR occurs before NPR DATA STROBE and SLAVE CLEAR occurs before SLAVE STROBE so that the data register is cleared prior to loading.

Table 5-6
Loading Data Register

1. DIRECT SET METHOD (clear/load)

Function	TC11	Signal Sequence	Operation
Bus to Data	Master	NPR DATA CLEAR NPR DATA STROBE	Clears 17–00 Sets 15–00

Table 5-6 (Cont)
Loading Data Register

1. DIRECT SET METHOD (clear/load) (cont)

Function	TC11	Signal Sequence	Operation
	Slave	SLAVE CLEAR SLAVE STROBE } note 1	Clears 15–00 Sets 15–00
Bus to XData	Slave	SLAVE CLEAR SLAVE STROBE } note 2	Clears 17–16 Sets 17–16
LPB to Data	–	ZDAT LPB TO DAT	Clears 17–00 Sets 17–12

2. D INPUT METHOD (enable/clock)

Function	Tape Direction	Signal Sequence
Read/Write	Forward/ Reverse	SHIFT ENABLE = $\overline{\text{REV}} \cdot \overline{\text{REQUEST BUS}}$ CLOCK DAT = $\overline{\text{READY}} \cdot \overline{\text{DATM EN}} \cdot$ TP00
	Reverse	OBVERSE ENABLE = REV · REQUEST BUS
		Either: WDATA · OBVERSE ENABLE · CLEAR BUS or: RDATA · OBVERSE ENABLE · MASTER B

NOTES: 1. And SELECT 10, ~IN.
2. And SELECT 0, OUT LOW, ~MAINT.
3. "Set" means direct setting of those bits which are to be loaded with 1s.

When the bus to extended data function is used, it operates in a similar manner as the bus to data function. However, in this case the controller always functions as slave and only the extended data bits are cleared and loaded.

When the longitudinal parity buffer contents are loaded into the data register (LPB to Data), the operation is again similar. However, in this case, the entire register is first cleared but only the six most significant bits are loaded because the LPB is a 6-bit buffer register.

The D input method (enable/clock) is used during read or write operations. During read operations, for example, the contents of the 6-bit read/write buffer (RWB) is shifted into the data register. When the RWB fills up again, the previous six bits in the data register are shifted over and the next six bits from the RWB are shifted into the six lowest bit positions.

A 2-wide AND/NOR gate is tied to the D input of each flip-flop in the data register. One of the AND gates is used to provide the shift and load function. One leg of this gate is tied to the DAT SHIFT ENB signal which enables the shift/load function. The other leg of the AND gate enabled by DAT SHIFT ENB is tied to a data source: for DAT 05–00, it is tied to RWB 05–00 respectively; for DAT 11–06, it is tied to DAT 05–00; and for DAT 17–12, it is tied to DAT 11–06. Thus, when the flip-flop is clocked by CLOCK DAT (derived from TP00 in this case), information in the RWB is loaded into the lowest six bits of the data register, the lowest six bits of the data register are shifted to the middle 6-bit position, etc. The same load/shift sequence occurs during write operations. However, in this case the information in DAT 17–12 is loaded into the RWB simultaneously with the data shifting in the data register.

If the tape is travelling in the reverse direction, it is necessary to perform an obverse function in the WDATA and RDATA modes. When reading in reverse, the data that is being assembled in the RWB and shifted into the data register is in obverse complement form. Thus, it is necessary to correct it before sending it to memory. When writing in reverse, the data in the data register must be obverse complemented before being written in order to maintain a "forward-oriented" data word structure. In both of these cases (reverse read, reverse write), the TC11 Controller performs an obverse complement operation on the data held in the data register. The bit pattern of the word before and after the obverse complement function is shown in Figure 5-6.

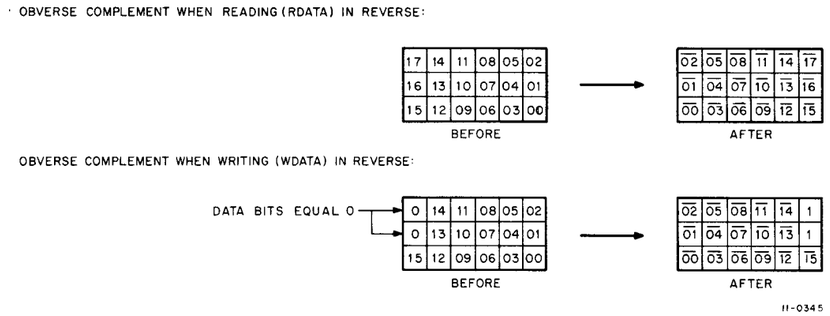


Figure 5-6 Obverse Complement Bit Pattern

The obverse function is accomplished by the second AND gate in the 2-wide AND/NOR gate. One leg of the AND gate is tied to an output of a data register flip-flop (0 output of 15 to AND gate for 00, etc.). The other leg is tied to the OBVERSE ENB signal from the NPR control logic. The latter signal is produced if the transport is moving in the reverse (REV) direction and a bus cycle is either being performed or is about to be performed.

When reading (RDATA) in reverse, after the 18 bits of the data are assembled and available in the data register, the obverse complement function must be performed before the data is transferred to memory. First, the OBVERSE ENABLE is generated (drawing TC11-0-08). This allows the complement obverse data to be applied to the data register inputs. For example, the 0 side of data bit 2 is applied to the input of data bit 17. Next, a CLOCK DAT pulse occurs (drawing TC11-0-08). The leading edge of this pulse occurs just when the TC11 gains bus control at the time MASTER B is asserted. Thus, the data is obverse complemented just prior to the initiation of the DATO bus cycle.

When writing (WDATA) in reverse, the same OBVERSE ENABLE is active. However, this time CLOCK DAT occurs after the DATI bus cycle is complete at END CYCLE. Thus, the data is obverse complemented just after being read from memory but prior to being written on the tape.

5.8.5 Word Count Register (TCWC)

The word count register (drawing TC11-0-22) is used to count the number of full word transfers made during read and write operations. Prior to a read or write operation, the word count register is loaded with the 2's complement of the number of words to be transferred. After each transfer is made, the register is incremented by 1. When the word count reaches 0, it indicates that the entire block of words has been transferred and further operations are inhibited.

The 2's complement number representing the word count is placed on the bus data lines and loaded into the word count register under program control. This is accomplished by the BUS TO TCWC signal from the selection logic, which indicates that the word count register has been selected for a load operation.

Each time either a read or write function is complete, the NPR control logic produces an INC BA-WC (increment bus address – word count) signal, which steps the counter by 1. When the counter reaches 0, an AND gate produces the WCOF (word count overflow) signal, which sets the WCO flip-flop that, in turn, inhibits further transfers. The counter output is applied through a series of selection gates to the output bus lines. Thus, whenever desired by the program, a TCWC TO BUS signal can be initiated by the selection circuits in order to read the current state of the counter.

A detailed explanation of the M795 Word Count and Bus Address Module is presented in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D.

5.8.6 Bus Address Register (TCBA)

The bus address register (drawing TC11-0-21) specifies the bus or memory address to or from which data is to be transferred during read and write operations. The register consists of 16 bit positions (15–00) plus the two extended bus address (XBA) flip-flops in the command register. Bit 00 of the register is implemented but not tied to A00, thus forcing addressing of words at even boundaries. After each transfer is made during either a read or write operation, the register is incremented to advance it to the next word location.

The bus address register is functionally almost identical to the word count register. Rather than load a word count number, the starting address is loaded into the register by the BUS TO TCBA signal. Incrementation is accomplished by the INC BA-WC signal, and the address is available on the bus lines and can be read by the TCBA TO BUS signal.

Bits XBA17 and XBA16 in the command register are a logical extension of the bus address register and increment along with the register.

A detailed explanation of the M795 Word Count and Bus Address Module is presented in the *Unibus Interface Manual, Second Edition,* DEC-11-HIAB-D.

5.8.7 Read/Write Buffer Register (RWB)

The read/write buffer register is a 6-bit register that handles information transfers between the data register and the read/write heads on the tape unit. During read operations, the outputs from the three data read/write heads are strobed into the lower half of the buffer (bits 2, 1, 0→ RWB ⟨02:00⟩) and then shifted to the upper half during the next timing cycle. When the next character on the tape passes under the heads, it is strobed into the lower half of the buffer, thereby filling it. When the next timing pulse occurs, the entire contents of the buffer is now shifted into the data register (into bits ⟨05:00⟩). This process continues until the entire word is read and loaded into the data register. The data register can be addressed by the program and the word moved to the bus.

During write operations, the reverse process occurs. The buffer is loaded (all six bits) from the data register (from bits ⟨17:12⟩) and then shifted out three bits at a time to the write amplifiers when the appropriate timing signal occurs. This causes the write heads to write one 3-bit character on the tape at a time.

5.9 TAPE CONTROL

The TC11 Controller provides various tape control and decoding functions. The tape control functions are: unit selection and tape motion control. The tape decoding (and encoding) functions are: tape mark track decoding, tape timing track decoding, and parity generation and checking. Each of these functions is described in detail in subsequent paragraphs.

5.9.1 Unit Select

The unit select logic determines the tape unit to be used for the selected function. Because the TU56 transport is a dual unit system, and because up to four TU56s may be used with one TC11 Controller, up to eight individual tape units may be used with a single TC11 System.

The number of the tape unit (0 through 7) to be selected is represented by a 3-bit number generated by the command register (drawing TC11-0-11). This number is loaded into the command register from bus data lines 10, 09, and 08. The three UNIT flip-flops are set or cleared dependent on the bus input data, and the flip-flop outputs are applied to the decoder shown on drawing TC11-0-12.

The decoder is not enabled until an input AND gate is qualified. This gate is qualified provided the system is not in the maintenance mode, the stop all transports (SAT) function has not been selected, and the NEW UNIT SELECT signal from the tape control circuits is not present. The NEW UNIT SELECT signal momentarily disables the decoder when the UNIT SELECT bits are changing. When the decoder is enabled, it decodes the UNIT bits from the command register and provides a level on one of eight output lines, depending on the input code.

NOTE
When the decoder input and gate are disabled, all of the outputs are false.

The level representing the selected unit passes through an inverter amplifier and is connected to the M908 bus as shown on drawing TC11-0-12.

5.9.2 Tape Motion Control

The tape motion control logic (drawing TC11-0-04) provides signals that control tape unit operation (start, stop, and all stop) and direction (forward and reverse). This logic also includes the up-to-speed time delays used to make certain that the tape unit is up to proper operating speed before the program attempts to read from or write on the tape. Tape unit operation and direction logic is discussed below. Up-to-speed logic circuits are covered in Paragraph 5.8.3.9.

The tape unit start signal (GO L) is produced by a series of gates. These gates are qualified if: no error stop condition (SELE, ILO, ENDZ, or MTE) exists; neither the stop selected transport (SST) or stop all transports (SAT) signal is present; and DECODE DLY is absent.

The tape unit stop signal (STOP L) is produced by a series of gates if either the SST or SAT function has been selected or if an ERROR STP condition exists. These signals are produced by the function decoder shown on drawing TC11-0-05. The ALL HALT L signal is produced by gates that are qualified when the SAT function has been selected.

The tape unit direction logic basically consists of two 2-input AND gates: one for the forward direction, one for the reverse direction. One leg of each gate is qualified if a STOP signal is not present.

The other input to the AND gate is the output of the reverse (REV) flip-flop. If the flip-flop is set, one AND gate is qualified and the REVERSE L signal is produced to cause the tape unit to move in the reverse direction. If the flip-flop is cleared, the other AND gate is qualified and the FORWARD L signal is produced. The REV flip-flop is shown on drawing TC11-0-01. This flip-flop is set or cleared under program control by loading an appropriate bit from the bus data lines.

A summation of the motion controls is presented in Table 5-7.

Table 5-7
Motion Controls

Function	Condition
ALL HALT	SAT
FORWARD	$\overline{REV} \cdot \overline{SAT} \cdot \overline{SST}$
REVERSE	$REV \cdot \overline{SAT} \cdot \overline{SST}$
STOP	ERROR STP + SAT + SST
GO	$\overline{SAT} \cdot \overline{SST} \cdot \overline{ERROR\ STP}$
	Note
ERROR STP	SELE + ILO + ENDZ + MTE

Whenever the low byte of the command register is loaded, SELECT 2 and OUT LOW are true, thereby producing DECODE DLY which disables the motion controls to the TU56. This prevents unwanted pulses from occurring on the output lines while the function bits are modified. Note that DECODE DLY is true even though the function bits are not modified; thus, STOP, GO, FORWARD, REVERSE, and ALL HALT functions are disabled during this period. However, the TU56 logic contains flip-flops that store the motion commands.

All tape unit control functions (STOP, GO, REVERSE, FORWARD, and ALL HALT) pass through inverter amplifiers and are connected to the M908 bus as shown on drawing TC11-0-12.

5.9.3 Mark Track Decoder

Bits read from the mark track of the tape are serially-shifted into the mark track decoder, which contains a 9-bit shift register that decodes the bits and generates levels used to control operation of the TC11 Controller. The mark track decoder module also contains a timing state generator that steps through six different time states as different regions of a block appear.

The term "mark track decoder" normally refers to both the decoder shift register and the timing state generator. In this discussion, however, these two components are covered separately. Paragraph 5.9.4 covers the shift register, and Paragraph 5.9.5 covers the timing state generator.

5.9.4 Shift Register (Window)

The mark track code defines the areas on tape where control and data words are positioned. The purpose of the shift register is to decode the mark track code. This 9-bit register is three bits longer than that required to decode a legal mark of six bits. This ensures that one legal mark follows another in proper order. Because the register effectively allows the controller to "see" a portion of the tape, it is sometimes referred to as the "window register"

The shift register and associated decoding gates are shown on drawing D-CS-M228-0-1. The control logic that activates the register is shown on drawing TC11-0-7.

Initially, the UPS flip-flop is cleared, and the resultant signal indicates that the selected unit is not up to speed. This signal qualifies a gate to produce a low output, which is applied to the direct-clear lines of all nine register flip-flops. In other words, this signal performs an initialize function.

When the selected tape unit is up-to-speed, the UPS flip-flop is set, removing the low input to the direct-clear inputs of the flip-flops, thereby enabling them to be set. At this point, the TP1 timing pulse is applied to the clock input of flip-flop W9, and the output from the mark track read head amplifier is applied to the data input of the flip-flop. This causes the mark track code to be shifted into the register, beginning with the most significant bit.

Bits from the mark track continue to be shifted serially into the register until flip-flop W1 is set. No decoding is performed until flip-flop W1 is set, thereby ensuring that at least eight bits have been loaded into the register. Actually, more than eight bits can be shifted through if the initial bits are 0s. Because decoding of the "window" register does not begin until W1 is set, the W1 flip-flop is sometimes called the "window shade".

The outputs of all flip-flops are applied to a gate decoder circuit, which is not qualified until the W1 output is available. At that time, the states of the flip-flops qualify a specific combination of gates to produce an output signal representing the decoded mark track code. The eight codes that are produced are: sync, block mark, data sync, block start, data, block end, end, and block sync. Decoding of the various codes is described in subsequent paragraphs.

Note that during the WRTM mode, the controller is writing mark track information on the tape. Therefore, mark track data is prevented from being shifted into the window. Also, the window is held clear until the UPS flip-flop is set, thereby ensuring that no erroneous bits read at slow tape speed are shifted into the window.

5.9.4.1 Block Mark Decoding – As the tape moves out of one block and into the next, the first legal code appears in the extension area preceding the forward block number. The decoding is shown in Figure 5-7. Because the register actually examines eight bits eight times, the first number decoded is octal 125, which is the sync code followed by six sync codes (seven total). The final three octal digits decoded are 126, which is the block mark. When this number is decoded, the mark track decoding gates produce the MK BLK MK (mark track block mark) level, which indicates that the region of the tape containing the block number has been found.

The MK BLK MK level is ANDed with the RNUM (read block number) function to set READY in order to indicate to the programmer that the controller has just read the block number recorded in the data bits of the forward block number area.

Note that SYNC is enabled only for RNUM or RDATA functions. For the other functions, SYNC is enabled until the controller is up-to-speed and shifts out of ST IDLE.

Note that if the tape were to move in the opposite direction, all binary bits would be complemented and read in the reverse direction. The resultant codes would be the same, and the reverse block number code would produce the MK BLK MK level.

5.9.4.2 Data Sync and Block Start Decoding – After the block mark has been decoded, the mark track decoder decodes the information in the reverse guard portion of the tape to produce the MK DATA SYNC (232) level as shown in Figure 5-8. Following the MK DATA SYNC, four MK BLK START (block start, 210 or 010) levels are decoded to indicate the start of data information on the tape. This information begins with the reverse parity word and is followed by the data words. A block start level is produced each time an octal 10 is decoded.

5.9.4.3 Data Word Decoding – All data word regions on the tape, except for the first two words and last two words, are coded with octal number 70. This code is decoded in a manner similar to the block start decoding (070) (see Figure 5-9).

The controller has already begun reading information from the data regions of the tape, because the BLK START level indicated the start of data words on the tape. The purpose of the MK DATA level is to prevent a mark track error (MTE) indication as long as data word decoding is valid. Any time the mark track decoder ceases reading a valid data word code of 70, the MK DATA level is absent, and a series of gates are qualified to set the MTE flip-flop, indicating an error condition.

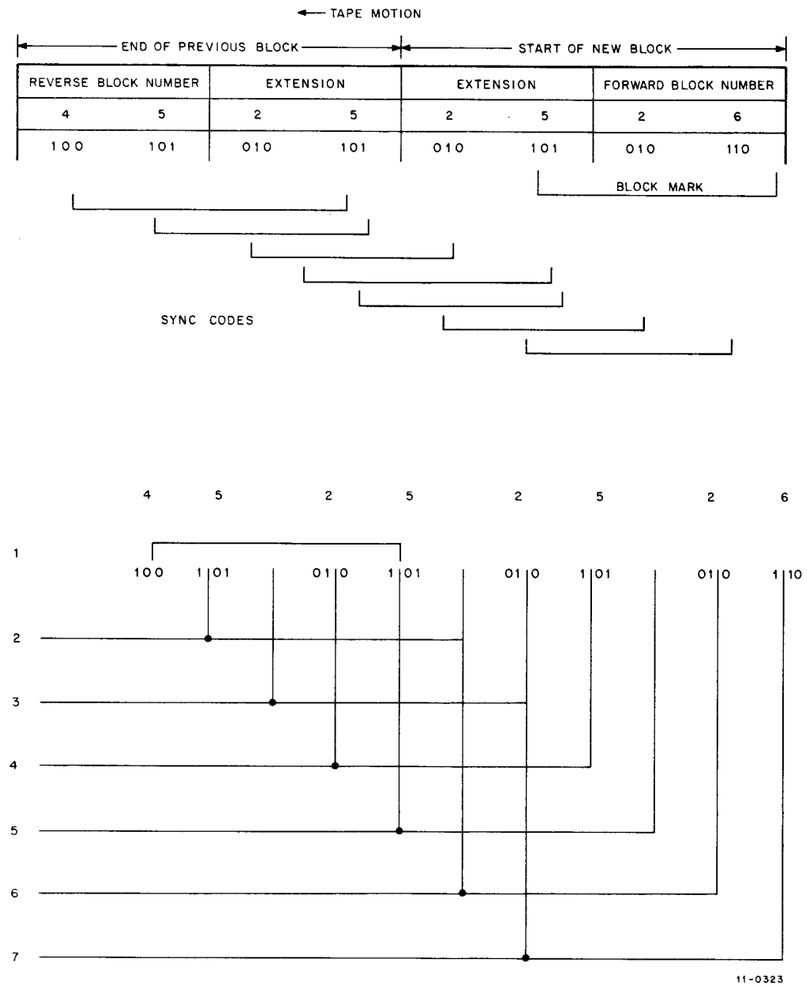


Figure 5-7 Block Mark Decoding

5.9.4.4 Block End Decoding – The last two data words in the block, the forward-check and the forward-lock regions, are all coded with octal 73 to indicate the end of the data portion of the tape. These four codes are decoded in the same manner as before, to produce the MK BLK END (block end) level (see Figure 5-10).

As the last MK DATA block is decoded and the first MK BLK END level is produced, a series of gates is qualified to step the timing state generator (refer to Paragraph 5.9.5) to the final (ST FINAL) time state.

5.9.4.5 Block Sync Decoding – The last level to be produced by the mark track decoder when reading (or writing) a block of data is the MK BLK SYNC (block sync, 351). The decoding of the MK BLK SYNC is shown in Figure 5-11. The dotted portions of the figure indicate block mark decoding that is identical to Figure 5-7. The controller now begins decoding the mark track for the next block of information.

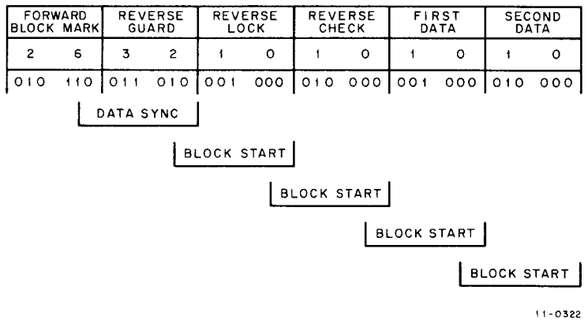


Figure 5-8 Data Sync and Block Start Decoding

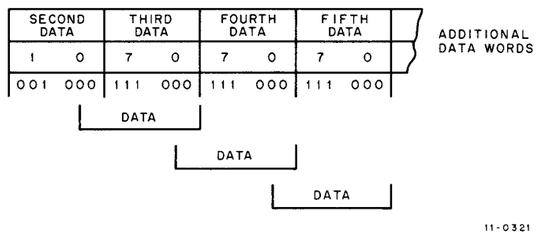


Figure 5-9 Data Word Decoding

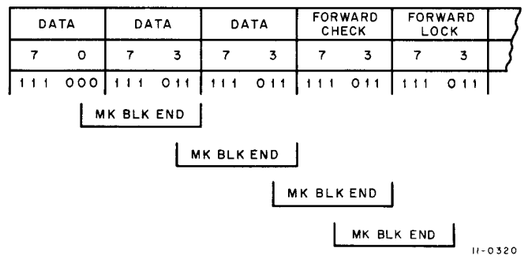


Figure 5-10 Block End Decoding

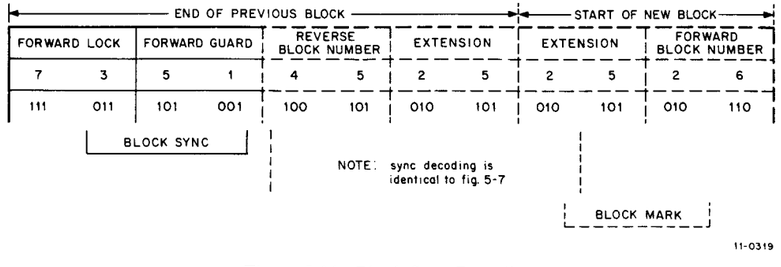


Figure 5-11 Block Sync Decoding

5.9.5 Timing State Generator

As the shift register (window) decodes information from the mark track, the timing state generator responds by interpreting the code and stepping through six states as different regions of the block appear. This process guarantees that a block of data is handled completely. For example, it prevents the controller from starting to write in the middle of a block simply because it has detected a data region on the mark track.

The timing state generator (drawing D-CS-M228-0-1) is six bits long and consists of six flip-flops. It is normally in the idle state (ST IDLE), which is the last flip-flop. When sequenced, it steps from the idle state through the following states: state block mark (ST BLK MK), reverse parity check (ST REV CK), data (ST DATA), final (ST FINAL), and parity check (ST CK). It then enters the idle state again. The timing state generator passes through all six states as a complete block passes the read heads. It cannot leave the idle state unless it recognizes the beginning of a block; therefore, there is no chance that a block is partially written into or read. It should be noted that on the drawing, pin AM1 (SH ST H) is connected to pin BC1 (SH ST H). Thus, the output of the timing state generator decoding gates is tied directly to the input of the 6-bit shift register, i.e., the timing state generator.

The six time states are shown on timing diagram TC11-0-24. Table 5-8 shows the relationship between the shift register (window) decoding and the mark track as well as their functions within the controller. Note that the mark track code over any given tape area depends on the direction of tape motion. If the tape is reversed, then the mark track codes are transformed into their obverse complements. For example, code 73 becomes 10, 51 becomes 32, 45 becomes 26, 70 remains 70, and 25 remains 25. This results in the *same order of codes* on the mark track regardless of the direction of tape motion.

Table 5-8
Mark Track and Window Codes

Mark Track Code	Name	8-Bit Window Code	Name	Function
55	Reverse end zone	155	none	This code requires no operation. It indicates that the tape is leaving an end zone.
25	Extension	325 125	SYNC	This code is used by the timing state generator to synchronize its counters with the beginning of a block. It occurs between blocks and at either end of the tape.
26	Forward block number	126	MK BLK MK	This code occurs when the block number is in the data register. This code also steps the timing state generator from idle to block mark state.
32	Reverse guard	232	MK DATA SYNC	This is a no-operation code which gives the controller time to respond to the block number found in the above operation.
10	Reverse lock	210	MK BLK START	This code steps the time state from block mark (ST BLK MK) to parity check (ST REV CK). During this state, the longitudinal parity buffer is activated.
10	Reverse check	010	MK BLK START	Steps timing state generator to data time state (ST DATA). The controller can now perform data transactions.

(continued on next page)

Table 5-8 (Cont)
Mark Track and Window Codes

Mark Track Code	Name	8-Bit Window Code	Name	Function
10	First data	010	MK BLK START	No action. Decodes to make certain no mark track error exists. Indicates first data word has occurred.
10	Second data	010	MK BLK START	Same as above. Indicates second data word has occurred.
70	Data	070	MK DATA	These codes indicates a data word is under the tape heads. Primarily used to inhibit error circuits. If a coding error occurs, MK DATA is not produced, and a mark track error (MTE) occurs.
73	255th data	073	MK BLK END	This code indicates that the last data word is about to be read (or written). Causes timing state generator to step to final time state (ST FINAL).
73	256th data	373	MK BLK END	This code indicates that the last data word has been read (or written). The timing state generator steps to check state (ST CK) to examine the parity word. It then steps to the idle state (ST IDLE).
73	Forward check	373	MK BLK END	The longitudinal parity word is stored in this area. No operation occurs when MK BLK END is decoded.
73	Forward lock	373	MK BLK END	No operation.
51	Forward guard	351	MK BLK SYNC	No operation in this direction other than to set up controller logic for new upcoming block.
45	Reverse block number		none	No operation. Becomes code 26 in opposite direction for reading block number.
22	Forward end zone	222	MK END	Indicates end zone has been reached. Sets ERROR and halts tape.

5.9.6 Timing Track Decoder

The timing track contains a square wave with a period of 33 μs. Each edge is used to produce positive and negative pulses that synchronize TC11 Controller operations. The timing track decoding logic may be functionally divided into three areas: read logic, write logic, and counter.

During read operations, the timing track passes under the read head and is received by a G888 Read Amplifier. These edges are separated by pulse generators (drawing TC11-0-04) to produce TP0 and TP1 timing pulses as shown on Figure 5-12. When either the TP1 or TP0 timing signal is produced, it triggers a 10-μs time delay that eliminates any noise that may follow the pulse. This is discussed more fully in Paragraph 5.8.3.9.

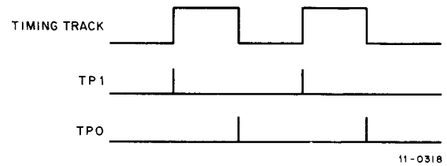


Figure 5-12 Pulses Derived From Timing Track

The TP0 and TP1 pulses trigger a counter (drawing TC11-0-02) consisting of four flip-flops (C0, C1, C2, and C3). The outputs of these flip-flops provide various internal time states. The output C1 flip-flop shown on drawing TC11-0-04 is ANDed with the TP0 L pulse to produce the TP00 and TP01 timing pulses. The TP00 is actually every even TP0 pulse; the TP01 pulse is every odd TP0 pulse (see Figure 5-13).

The timing track write logic is used only when tape is being formatted. In this instance, timing is initiated by the write timing and mark (WRTM) function as described in Paragraph 5.8.3.10. Generation of internal timing signals is covered in Paragraph 5.8.3.9. The write amplifier for the timing track receives the TAPE CLK outputs and a TM ENABLE signal to write the timing track on the tape.

5.10 TIMING LOGIC

The basic timing pulses synchronize all operations of the TC11 Controller. These pulses are generated by the timing track output, which is read from the magnetic tape. The timing track contains alternately polarized bits that are formatted on tape prior to reading or writing of information. The negative transition produces the TP0 timing pulse, and the positive transition produces the TP1 timing pulse. These two pulse trains are identical in frequency but different in phase. Thus, each TP1 pulse occurs in between two TP0 pulses. (The TP1 pulses occur every 17 μs as do the TP0 pulses.)

Note that much of the logic references TP00 and TP01 pulses. These are simply methods of designating every other TP0 pulse. The TP00 timing pulse is every *even* TP0 pulse; the TP01 pulse is every *odd* TP0 pulse (see Figure 5-13).

A timing state generator is used in conjunction with the mark track decoder to provide six time states. As information is decoded from the mark track, the state generator responds by interpreting the code appropriately and stepping through the six states as different regions of a block appear. This process guarantees that a block of data is handled completely. In other words, it ensures that the TC11 Controller does not start writing half way into a block because it has detected a data region on the mark track.

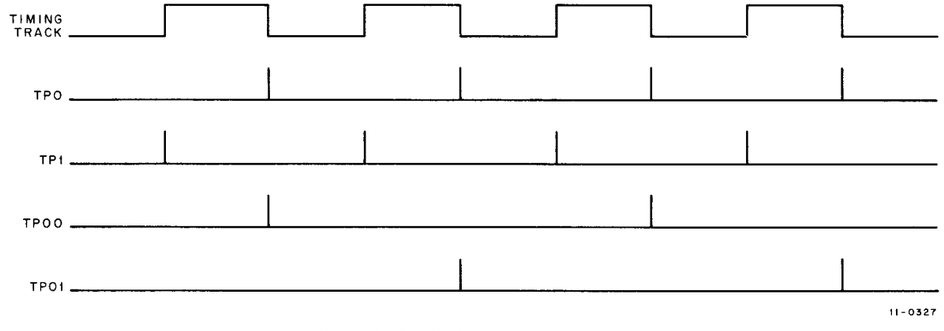


Figure 5-13 Timing Pulse Designations

5.11 PARITY LOGIC

The DECtape format provides two parity error regions (one at each end of the block) to provide a bidirectionally operative hardware parity check. A 6-bit longitudinal parity word (two 3-bit parity characters) is written to force the number of 0s written as data and the forward and reverse checksums to be odd. This is calculated on the basis of three 6-bit characters per data frame that pass through RWB 5–0. Because a parity check area is included at each end of the block and taken into account during reading and writing, a block written in either the forward or reverse direction reads with correct parity.

The parity word is formed, or read, by the longitudinal parity buffer (LPB) in the controller. The LPB is a 6-bit register that samples the data in the read/write buffer register; i.e., the LPB bit is complemented when the data bit is 0. When the end of the block is reached, the contents of the LPB are loaded into the read/write buffer and written on the tape in the parity check area. At the completion of every block in the RDATA mode, the LPB is sampled to determine if a parity error exists. The parity error flip-flop is discussed in Paragraph 5.8.3.2.

An example of generation of parity is given in Table 5-9.

Table 5-9
Generation of Parity

Data Bit	Present State Of LPB	Next State Of LPB
0	0	1
0	1	0
1	0	0
1	1	1

5.12 MAINTENANCE MODE LOGIC

The TC11 Controller includes maintenance logic that permits simulation of certain operations of a tape transport. The maintenance mode is selected by setting the MAINT bit in the command register. When in the maintenance mode, the controller deselects all transports and disables the selection error (SELE) logic and the WRITE LOCK switch. The program can then load various bits into the status register to simulate the bit read from the mark track or bits loaded into or read from the three data tracks.

Refer to descriptions of the MMT, CLK, DT0, DT1, and DT2 bits of the TCST register (Paragraph 5.8.3), and the MAINT bit of the TCCM register (Paragraph 5.8.2).

5.13 READ OPERATION

Figure 5-14 is a functional diagram of the read operation. Note that the information written on the data tracks is stored in parallel form in six 3-bit characters. As the first character in the data word passes under the read heads, clock pulse TP1 strobes the character into the first three bits of the read/write buffer. In effect, the parallel character is loaded serially, beginning with the bit in data track 0. The next timing pulse (TP0) shifts the data in the read/write buffer so that the first character now occupies bit positions 3 through 5. When the next TP1 timing pulse occurs, the second character from the tape is strobed into the read/write buffer, which now contains the first two characters of the data word. The next TP0 timing pulse rotates the entire contents of the read/write buffer into the lowest bit positions of the data register (TCDT).

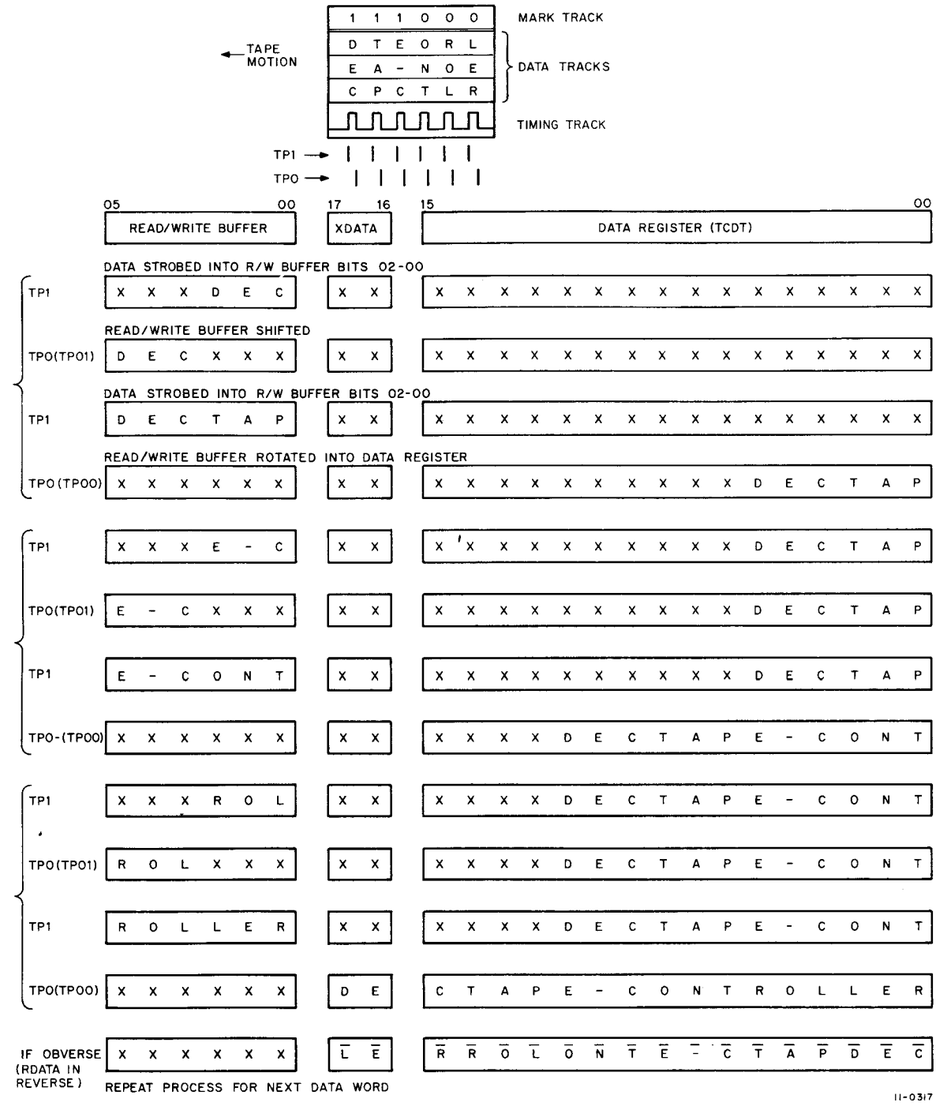


Figure 5-14 Read Operation – Functional Diagram

Every other TP0 pulse is referred to as TP00 or TP01. Basically, a complete read cycle consists of four operations: strobe R/W buffer (TP1), shift R/W buffer (TP0), strobe R/W buffer again (TP1), and rotate R/W buffer contents into data buffer (TP00).

This cycle is repeated two more times to load the entire six-character word into the data register. However, because the word is 18 bits and the register stores only 16 bits, the two extended data (XDATA) bits in the status register are used for the overflow.

Figure 5-15 illustrates a read operation from a hardware point of view. The first read amplifier decodes the timing track to provide the timing pulses (TP1, TP0) required for synchronizing the read operation. An internal clock can be activated to feed the timing circuits but this clock can only be used when the maintenance mode (MAINT) has been selected. The internal clock is never active during normal read operations.

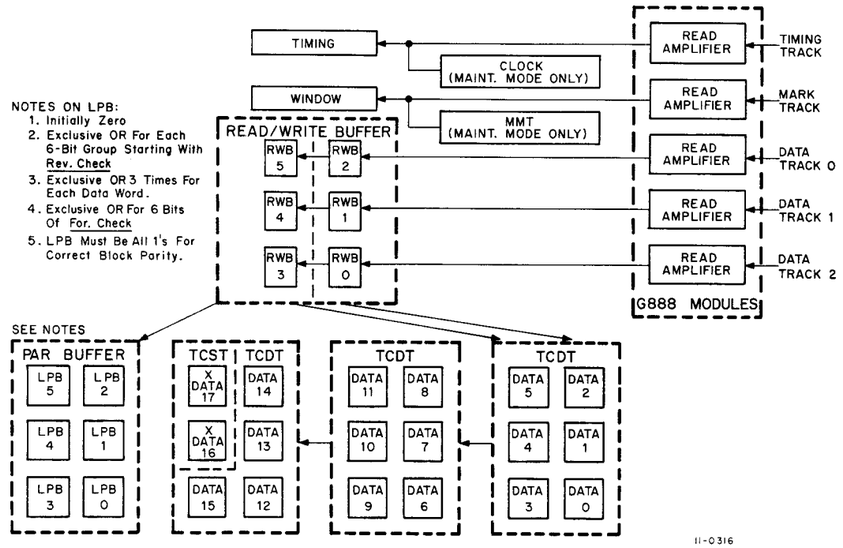


Figure 5-15 Read Operation – Hardware Point of View

The second read amplifier decodes the mark track to provide the window required for reading the data tracks. The MMT can be used to simulate the mark track during the maintenance mode.

The next three read amplifiers provide the bits in data tracks 2, 1, and 0. The first character read is loaded into the lower bit positions of the buffer. These are then shifted over and the next character loaded into the buffer. At this point, the entire buffer is unloaded into bit positions 0 through 5 of the data register. The next two characters are loaded into the read/write buffer and again loaded into the first six bit positions of the data register, the former contents of these bits shifting over to bit positions 6 through 11. This process is performed one more time until the entire 18-bit word is loaded into the data register and the two extended bits of the status register.

When the data register is filled, the data is ready for transfer. In the RALL mode, READY is set and the program must read the contents of the register into memory while the next two lines are being read (that is, within 67 μs). In the RDATA mode, an NPR request is made and, when the TC11 Controller becomes bus master, it performs a DATO. If, however, the RDATA was in reverse, the raw data is obverse complemented before being sent to the memory. This transformation is shown in the last line on Figure 5-14.

5.14 WRITE OPERATION

Figure 5-16 is a functional diagram of the write operation. The first clock pulse (TP00) is used to request that the data register (TCDT) be loaded. In the WALL or WRTM modes, READY is set and the program then loads the status register (TCST) for bits 17 and 16 and the TCDT for bits 15 through 00. In the WDATA mode, the first TP00 sets the REQUEST BUS flip-flop, which causes an NPR request. When the DATI is completed, the TCDT is loaded and the two extended data bits are cleared. If WDATA is being performed in reverse, the data received from the Unibus is obverse complemented at the end of the DATI cycle. The loading of TCDT and TCST is overlapped with writing of the previous data word.

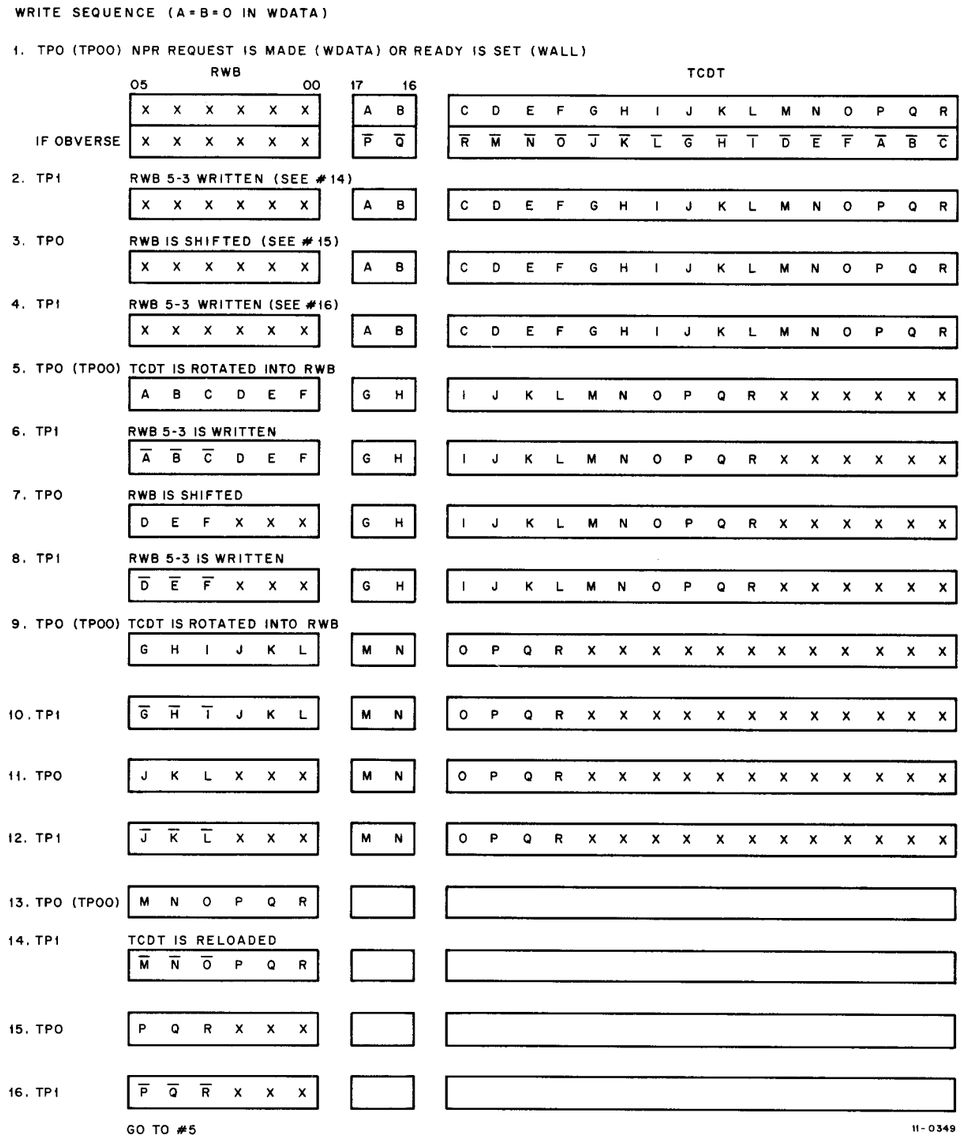


Figure 5-16 Write Operation – Functional Diagram

When the next TP00 pulse occurs, the six most significant bits in the data register are rotated into the read/write buffer (RWB). The next timing pulse (TP1) complements the high-order bits (5–3) in the RWB. This complement operation, amplified through the write head amplifiers, writes the data as a flux reversal on the magnetic tape. The three low-order bits are then shifted into the high bit positions of the RWB during TP0 time. The next TP1 pulse complements and thus writes these bits on the tape. This entire process is then repeated for the next six bits in the data register.

Basically, a complete write cycle consists of four operations: rotate six bits out of the data register and into the RWB (TP00), complement and write the three highest bits onto the tape (TP1), shift the remaining three bits over (TP0), and complement and write the remaining three bits onto the tape (TP1).

This complete cycle is performed a total of three times to write the entire 18-bit word on the magnetic tape. Because of the method of writing only three bits at a time, the word is formatted on the tape as a six-character word with three bits per character.

Figure 5-17 illustrates a write operation from a hardware point of view. This figure shows the method of shifting six bits at a time into the read/write buffer and the shifting of three bits out of the buffer into the appropriate write amplifiers. A timing diagram of a write operation is shown in Figure 5-18.

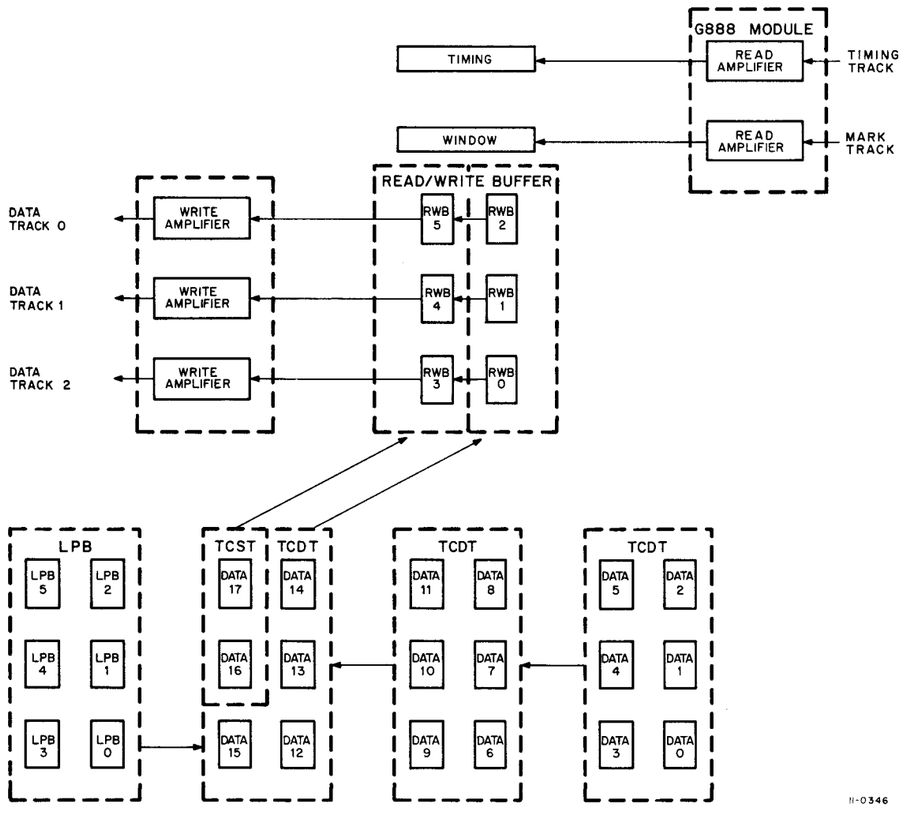


Figure 5-17 Write Operation – Hardware Point of View

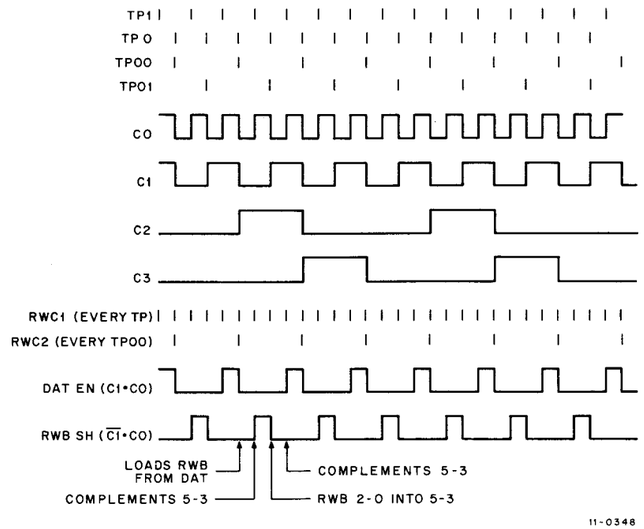


Figure 5-18 Write Operation – Timing Diagram

The write amplifiers are turned on or off by a write enable (WREN) signal from the WREN flip-flop (drawing TC11-0-02). This flip-flop is direct cleared, indicating that writing is inhibited, under any one of the following conditions:

a. Function bit 3 (FCT3) is clear. When this bit is clear, it indicates a non-writing function. Note that power up clears all function bits, thereby forcing the WREN flip-flop to clear.

b. Any error condition is present.

c. The DO bit is set.

d. The WRITE ENABLE/WRITE LOCK switch is in the WRITE LOCK position.

e. During the WDATA mode of operation, the WREN flip-flop is cleared after six bits (two characters) have been written in the FWD CHECK area of the tape.

The WREN flip-flop is set, indicating that writing can be performed, under either one of the following conditions:

a. During the WALL mode of operation, WREN is set at the first MK BLK START code (provided READY is clear) in order to write data starting at the check word.

b. During the WDATA mode of operation, WREN is set in order to write the last two characters in the check area, prior to writing data.

When the WDATA mode of operation has been selected, a zero data (ZDAT) signal is used to zero the data register under any one of the following conditions:

a. After WC0 (indicating that the word count register has reached the specified number, i.e., has overflowed), the rest of the block is written as all zeros.

b. During STATE REV CHECK so that the first two characters of the checksum are written as zeros.

c. During ST FINAL so that the data register is cleared prior to loading from the longitudinal parity buffer (LPB). The LPB to DATA operation must be preceded by a ZDAT signal. This is necessary for writing multiple blocks when the word count register has not yet overflowed.

When the write timing and mark (WRTM) mode of operation has been selected, the TAPE CLOCK flip-flop output is applied to the write amplifier for the timing track write head so that timing pulses are written on the magnetic tape. The mark track write amplifier is fed from RWB3. Therefore, to write a code of 26 into the mark track, for example, octal 010110 is loaded into the data register as shown in Figure 5-19. Note that the write amplifiers for data tracks DT0, DT1, and DT2 are not enabled, because WREN is not set during the WRTM mode.

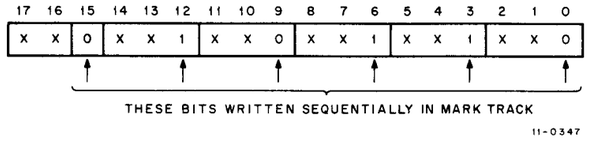


Figure 5-19 Mark Track Writing

CHAPTER 6
MAINTENANCE AIDS

6.1 SCOPE

The basic maintenance philosophy of the TC11 DECtape System is to present the user with the information necessary to understand normal operation of the system. The user can then use this information when analyzing trouble symptoms to determine necessary corrective action. Although it is beyond the scope of this manual to present detailed troubleshooting information, some specific maintenance aids that are not obvious are included in subsequent paragraphs. This section also contains preventive maintenance procedures.

General PDP-11 maintenance information is presented in the *PDP-11 Conventions Manual*, DEC-11-HR6B-D. Detailed maintenance and troubleshooting procedures for the TU56 DECtape Transport are given in the *TU56 DECtape Transport Manual*, DEC-00-HRTA-D.

6.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures that are performed prior to the initial operation of the equipment and periodically during its operating life. These procedures include visual inspection, mechanical checks, cleaning, and running of diagnostic programs. All preventive maintenance should be performed once a month or every 200 operating hours, whichever occurs first. It is helpful to keep a log book for recording specific operational data that indicates rate of performance, deterioration, and malfunctions in order to provide data for determining when components should be replaced.

It is beyond the scope of this manual to provide information on diagnostic programs. The main purpose of this section is to provide information on visual inspection, cleaning, and proper tape handling.

6.2.1 Visual Inspection

The TC11 DECtape System should be visually inspected according to the information given in Table 6-1.

Table 6-1
Visual Inspection Check List

Item	Check
Mechanical Connections	*a.* Check that all screws are tight and that all mechanical assemblies are secure.
	b. Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors.
Wiring and Cables	*a.* Check all wiring and cables for breaks, cuts, frayed leads, or missing lugs. Check wire wraps for broken or missing pins.

Table 6-1 (Cont)
Visual Inspection Check List

Item	Check
Wiring and Cables (cont)	*b.* Check that no wire or cables are strained in their normal positions or have servere kinks. Check that cables do not intefere with doors and that they do not chafe when doors are opened or closed.
Air Filters	Check all air filters for cleanliness and for normal air movement through cabinets. Clean if necessary.
Modules and Components	Check that all modules are properly seated. Look for areas of discoloration on all exposed surfaces. Check all exposed capacitors for signs of discoloration, leakage, or corrosion. Check power supply capacitors for bulges.
Indicators and Switches	Check all indicators and switches for tightness and ease of operation. Check for cracks, discoloration, or other obvious defects.

6.2.2 Tape Handling

Whenever tape is handled, the operator's hands must be clean to prevent contamination of the tape by body oils and salts. The use of sticky masking tape or cellulose tape for splicing or for holding down the end of the tape on a reel is not recommended because small deposits of the adhesive stick to the tape.

6.2.3 Cleaning Tape Reels

If the tape is covered with dust, carefully wipe the surface and backing of the tape with a soft, lint-free cloth such as a very soft chamois. Contamination that does not brush off easily can be washed off with a cloth slightly moistened with Freon TF. Aliphatic hydrocarbon-type solvents (heptane, gasoline, naphtha) can also be used but extreme care must be used because these compounds are highly flammable. Never use carbon tetrachloride, ethyl alcohol, trichlorethylene, or any other unknown cleaning agent, because these compounds may soften the oxide coating on the tape, deform the backing, or both.

6.2.4 Storing Tapes

The best method of tape storage is to place the reel of tape in the self-sealing plastic case supplied for that purpose by DEC. The case should then be stored on edge in a storage bin equipped with partitions between each reel. The plastic case protects tape from dust and sudden changes in humidity and temperature. It also guards both tape and reel from damage that may occur in handling when the tape is transported between work and storage areas. Plastic tape cases and storage bins can be ordered from DEC.

If the tape must be stored in the presence of magnetic fields (either ac or dc), special containers are available from DEC that protect the data from erasure in all but extremely high fields. However, it is desireable to store magnetic tapes away from any such fields if at all possible.

Temperature and humidity extermes should be avoided when possible. Recommended storage conditions are at a temperature of between 60° and 80°F, and within a relative humidity range of 40% to 60%. If extreme temperatures are encountered during storage or transit, the tape should be allowed to be brought up to the ambient temperature before it is used.

6.2.5 Physical Distortion

Most signal dropouts in digital recordings are caused by specks of dust and other contaminants that lift the tape away from the head. However, two other significant causes are dents and creases in the base material. Dents are caused by particles wound up tightly in the roll or by roughness in the surface of the hub on which the tape is wound. These may cause permanent dents or creases in many layers of the tape that cannot be stretched out flat as the tape passes over the head. Stresses in the roll that stretch the backing more than 5% usually leave a permanent impression. Stresses below this level are usually not permanent. Creases are caused by improper tape handling (threading, splicing, removing tape from guides) or by damage to the edges of the tape caused by uneven winding.

6.2.6 Accidental Erasure (or Saturation)

The magnetic properties of DECtape are extermely stable, and the magnetic retention is permanent unless altered by strong magnetic fields such as those generated by permanent magnets or electromagnets. If magnets of this type are placed near a tape, partial erasure may occur.

Both unrecorded and recorded magnetic tape should be kept away from electromagnetic bulk erasers and storage cabinets with magnetic latches. Unrecorded tapes should not be placed near dc magnetic fields (such as travelling wave tubes or magnetron magnets) because the tapes may become heavily biased or may even cause gross distortion during the recording process (in other words, the signal-to-noise ratio may be reduced).

If portions of the tape transport become magnetized, they can cause tape erasure, possible tape saturation, and signal degradation. Periodic demagnetization of critical transport components, particularly the recording heads, is recommended as a preventive maintenance measure.

6.2.7 Head Care

The following factors must be considered when maintaining tape recording heads:

a. Cleanliness of tape, tape transport, and the operating environment.

b. Maintenance procedures that involve checking tape tension, tracking, etc.

c. Abrasive qualities of the tape being used.

d. Solvents used for cleaning tape and recording heads.

Cleanliness in and around the head area is of extreme importance in all tape transports. Dirt particles and oxide buildup become serious threats to proper operation because they cause spacing loss. These particles can also become minute scrapers, gougers, and cutters to the head and tape surfaces when dragged between them.

Care must be taken not to touch the heads with any metallic or hard object to avoid scratching, gouging, or magnetizing the heads. The heads should be cleaned only with Freon TF, alcohol, naptha, or gasoline. Freon TF is probably the best all-around cleaner and can also be used for cleaning tape. Note that most head cleaners also dissolve lubricating greases and tape binders and, therefore, should be used carefully, especially around bearings and the tape. Cotton swabs make good disposable cleaning tools.

CHAPTER 7
MODULE DESCRIPTIONS

7.1 INTRODUCTION

This chapter provides descriptions of the logic modules used in the TC11 Controller. The position of the modules within the mounting boxes is shown in drawing D-MU-TC11-0-01 (two sheets).

A list of all TC11 modules is presented in Table 7-1. This table lists the modules in numerical order, the number of each type used in the system, and the name of the module. The last column in the table has a reference number indicating the document containing the detailed description of that particular module.

Table 7-1
Module Utilization

Module Number	Quantity Used	Title	Reference
G736	1	Jumper Module	–
G879	1	Transport Detector	1
G888	5	Manchester Read/Write Amplifier	1
M050	1	50 mA Indicator Driver	2
M105	1	†Address Selector	3
M111	3	Inverter	2
M112	3	NOR Gate	2
M113	8	Ten 2-input NAND Gates	2
M115	5	Eight 3-input NAND Gates	2
M117	3	Six 4-input NAND Gates	2
M119	1	Three 8-input NAND Gates	2
M121	5	AND/NOR Gate	2
M127	1	2-2-2-3 AND/NOR Gate	–
M141	1	NAND/OR Gates	2
M149	2	9x2 NAND Wired OR Matrix	–
M161	2	Binary-to-Octal/Decimal Decoder	2
M202	1	J-K Flip-Flop	2
M203	1	Eight Reset/Set Flip-Flops	2
M205	6	Five "D" Flip-Flops	–
M206	2	General Purpose Flip-Flop	2
M207	1	General Purpose Flip-Flop	2
M228	1	Mark Track Decoder	4
M239	1	Three 4-bit Counter/Registers	–

Table 7-1 (Cont)
Module Utilization

Module Number	Quantity Used	Title	Reference
M302	2	Dual-Delay Multivibrator	2
M307	4	Integrating One-Shot	–
M502	1	Negative Input Converter	2
M602	1	Pulse Amplifier	2
M606	1	Pulse Generator	2
M611	2	Power Inverter	–
M627	1	NAND Power Driver	2
††M782	1	Interrupt Control	3
M783	2	Unibus Transmitter	3
M784	2	Unibus Receiver	3
M795	1	Word Count and Bus Address Register	3
M796	1	Unibus Master Control	3
M798	1	Unibus Drivers	3

NOTES: †The address selector used in the TC11 is the C etch revision or higher.

††The referenced description is for the M782. The prime difference between the M782 and the M7820 used in the TC11 Controller is given in Paragraph 5.6.1.

REFERENCES

1. Chapter 7 of this manual.
2. *DEC Logic Handbook, 1971 Edition.*
3. *Unibus Interface Manual, Second Edition, DEC-11-HIAB-D.*
4. Paragraph 5.9.3 of this manual.

7.2 DEC LOGIC

All but four of the modules used in the TC11 Controller are M-series logic modules. The M-series modules are high-speed, monolithic integrated circuit modules employing TTL logic (transistor-transistor logic). These circuits provide high speed, high fan out, large capacitance drive capability, and excellent noise margins.

A general description of DEC logic and detailed circuit descriptions of TTL logic gates is provided in the *1971 DEC Logic Handbook*. The symbology used with all PDP-11 logic drawings is shown and explained in the *PDP-11 Conventions Manual*, DEC-11-HR6B-D.

7.3 MEASUREMENT DEFINITIONS

Timing is measured with the input driven by a gated pulse amplifier of the series under test and with the output loaded with gates of the same series. Percentages are assigned as follows: 0% is the initial steady-state level, 100% is the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50% input change to 50% output change. Rise and fall delays for the same module are usually specified separately. Rise time and fall time are measured from 10% to 90% of waveform change, either rising or falling.

7.4 LOADING

Input loading and output driving are specified in "unit loads" where one unit load is 1.6 mA by definition. The inputs to low-speed gates usually draw one unit load. High-speed gates draw 1-1/4 unit loads, or 2 mA.

7.5 MODULE CHARACTERISTICS

The following paragraphs describe the more important TC11 modules that are not described in other documents. These modules are the G879 Transport Detector and the G888 Manchester Read/Write Amplifier. Note that the M228 Mark Track Decoder is described in Paragraph 5.9.3 of this manual.

7.5.1 G879 Transport Detector

The G879 Transport Detector Module is designed to detect an error condition in the select circuits of the DECtape system. This module switches if either the input voltage is too low (indicating that no transport has been selected) or if the voltage is too high (indicating that more than one transport has been selected). If there is no input or more than one input to the module, its output goes negative. If there is only one input, the output remains high (+3V).

Specifications for the G879 module are given in Table 7-2, the circuit schematic is included in the engineering drawing manual (*TC11 DECtape System, Engineering Drawings*), and a description of the unit select logic is given in Paragraph 5.9.1.

Table 7-2
G879 Specifications

Inputs	
Input Impedance:	100 Ω (minimum)
Levels:	0V to -15V
Outputs	
Levels:	Standard TTL levels
Fan Out:	30 Unit Loads
Input/Output Function	
Input Voltage	**Output Voltage**
-15V to -9V	0V
- 9V to -4.7V	+3V
-4.7V to 0V	0V

7.5.2 G888 Manchester Read/Write Amplifier

The G888 Manchester Read/Write Amplifier module is used to drive (write) or receive (read) current to or from the DECtape read/write heads of the TU56 Tape Transport. One G888 module is used for each of the five read/write heads in the transport.

The write portion of the module is similar to a push-pull amplifier; it can drive current in either direction, depending on the relative polarity of its inputs. It can drive a square current pulse into the write head.

The read portion of the module is a high-gain amplifier with positive feedback. This amplifier responds to inputs of 500 μV. There are three stages to the read amplifier: a linear amplifier with a gain of 100; a zero crossing detector; and a limiter, which drives a 7400-series TTL gate. A test point (pin M2) is provided to sample the output of the first stage.

Specifications for the G888 module are given in Table 7-3, the circuit schematic is included in the engineering drawing manual (*TC11 DECtape System, Engineering Drawings*), and an explanation of the Manchester recording technique is given in Appendix A.

Table 7-3
G888 Specifications

Write Amplifier	
Inputs:	Standard TTL voltage Load at 0V is 1 unit R2 should be tied to +3V when not used
Outputs:	Can drive 100 mA in either direction Pins L2 and M2 are the outputs of the 7400 TTL gates Pins J2 and K2 are the outputs that drive the tape unit write head
Read Amplifier	
Inputs:	Can detect an input voltage as low as 500 μV.
Outputs:	Pins U and V are standard TTL voltages
Fan Out:	Pin U2 = 9 unit loads Pin V2 = 10 unit loads
Test Point:	Pin H2 is a test point that monitors the first stage output
Power Dissipation	
50 mW at +5V	
250 mW at -15V	

APPENDIX A
DECtape FORMATS

A.1 INTRODUCTION

This chapter describes the DECtape magnetic tape used in the TC11 DECtape System. It is necessary to understand the tape format and bidirectional read/write capabilities of the system before attempting to understand detailed theory of the TC11 Controller logic.

The tape format used with PDP-11 Systems is identical to the format used in the PDP-9, PDP-10, and PDP-15 Systems. It is also identical to the format used in PDP-8 Systems with the exception of the number of data words. If the reader is already familiar with the tape format on one of these systems, this appendix can be used either for a brief review or can be eliminated entirely.

This appendix covers three basic subjects:

a. recording method,

b. bidirectional reading and writing (obverse complement problem),

c. data format.

A.2 RECORDING DEVICE

The three basic elements that are required for making and reproducing a magnetic recording are:

a. **write (record) head** – a device that responds to an electrical signal and creates an appropriate magnetic pattern on the tape.

b. **magnetic tape** – a magnetizable medium that can hold the magnetic pattern.

c. **read (reproduce) head** – a device that detects the magnetic pattern on the tape and converts it back into the original electrical signal.

The addition of electronic amplification and a mechanical tape handler to the above three elements results in a basic magnetic tape recorder such as the TU56 DECtape Transport. In the TU56, however, the record and reproduce heads are combined into a single read/write head.

The following paragraphs briefly discuss the physics of writing and reading in relation to the read/write heads. The special recording method used to control signals applied to the heads is discussed in Paragraph A.3.

A.2.1 Writing

A write head is similar to a transformer with a single winding. As current flows through this winding, it produces a magnetic flux in the core material. The core of the write head is built in the form of a closed ring. However, unlike a transformer core, the ring has a short nonmagnetic gap in it (see Figure A-1). When this gap is bridged by magnetic tape, the flux detours around the gap and passes through the magnetic tape, thereby completing the magnetic path.

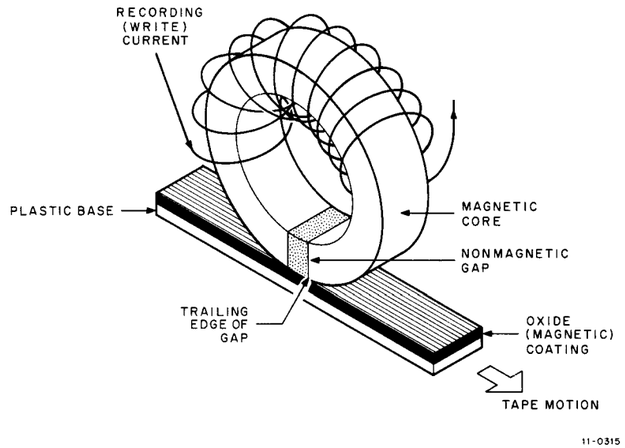


Figure A-1 Write Head (simplified diagram)

The magnetic tape is a ribbon of plastic on which particles of magnetic material have been uniformly deposited. As the tape moves across the write head gap, the magnetic material (or oxide) is subjected to a flux pattern proportional to the signal current in the head winding. When the tape leaves the head gap, each tiny particle retains the state of magnetization that was last imposed on it by the flux. Thus, the actual writing takes place at the trailing edge of the write head gap.

A.2.2 Reading

The original signal is read (reproduced) from the tape by moving the magnetic pattern on the tape across a read head. In this case, the nonmagnetic gap in the core is bridged by the magnetic oxide in the same manner as previously described for writing. The lines of flux surrounding the tape are proportional to the magnetic gradient of the pattern on the tape. These flux lines pass through the core and induce a current in the head winding that is proportional to the rate of flux change rather than to the magnitude of the flux. Thus, the read head functions as a differentiator so that the reproduced signal is actually a derivative of the recorded signal and not the signal itself. This distinction is important because the method employed by the TC11 System uses the rate of change (phase) rather than the magnitude (amplitude) of the current when reproducing information from a DECtape.

A.3 RECORDING METHOD

Both data and instructions are recorded on (or reproduced from) the magnetic tape by the Manchester method. This method employs phase-sensing rather than amplitude-sensing techniques for reading the tape. In addition, the Manchester method uses a prerecorded timing track to synchronize reading and writing of information on the tape.

Before discussing the Manchester method in detail, it might be helpful to review briefly three of the basic recording techniques, including the advantages and disadvantages of each. These three techniques (return-to-zero, pulse, non-return-to-zero) are shown in Figure A-2 and described in the following paragraphs. The Manchester method used in the TC11 System is described in Paragraph A.3.4.

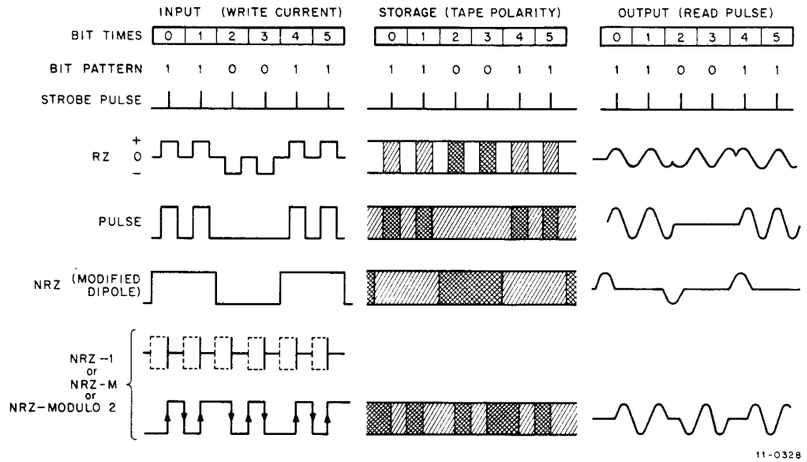


Figure A-2 Basic Recording Methods

A.3.1 Return-to-Zero (RZ)

The return-to-zero method is the least complex technique for recording information on magnetic tape. Prior to recording, the tape is completely unmagnetized. One magnetic state is assigned for binary 1, the opposite state is assigned for binary 0. Reading is then accomplished by simply determining the magnetic state for each bit position.

However, note that the write current returns to the zero (mid-point) level after each pulse is written. During this time, the tape is not magnetized. Therefore, a recorded tape consists of three states; two magnetic and one nonmagnetic. Because three levels (+, 0, -) of magnetization are on the tape, selective erasure and re-recording are virtually impossible. The entire tape must be erased and re-recorded. Another disadvantage of this method is the low packing density because of the nonmagnetic space between pulses. If the packing density is increased (thus the nonmagnetic space decreased), the positive and negative pulses tend to blend into a sine wave output and only the change of states between a 1 and 0 is decipherable. Long strings of like bits are lost.

Although the RZ recording method has the advantage of taking some positive action at each bit time, it also requires both a positive and negative transition to produce each single pulse, which also decreases the packing density.

A.3.2 Pulse Recording

Binary information can be represented by only two states (1 or 0, on or off); thus, it is not necessary to use three states (+, 0, -) to record information as in the case of the RZ method. Pulse recording uses only two states: pulse, or no pulse. A pulse is represented by one magnetic state only. If the other magnetic state or a nonmagnetic state occurs, it represents no pulse. Reading is accomplished by simply detecting the presence or absence of a pulse.

Although pulse recording is actually a variant form of return-to-zero (RZ), it does not retain all of the disadvantages of the RZ method. For example, the pulse height is doubled and, hence, facilitates detection. The packing density is increased because of the absence of the nonmagnetic gap and some of the erasure problems are also eliminated.

Although an improvement over RZ, pulse recording does have certain disadvantages. No positive action is taken during each bit time when a long string of zeros exists. This increases decoding problems. The zero pulse is susceptible to noise because pulse recording is basically an amplitude-sensing technique. Finally, the writing of each pulse requires two transitions and each pulse must somehow be separated, thus decreasing the packing density.

A.3.3 Non-Return-to-Zero (NRZ)

The non-return-to-zero (NRZ) method uses a positive current for writing 1s and a negative current for writing 0s. When a 1 is to be recorded, the current goes to the positive level and remains there as long as there are 1s in the bit pattern. When a 0 occurs, the current switches to negative and then remains at the negative level until another 1 occurs. Therefore, the magnetic tape is continually magnetized in either one state or the other. Basically, RZ and pulse recording are pulse-type methods, and NRZ is a level-type method.

The NRZ method provides both higher packing densities and higher operating frequencies. Unfortunately, it has numerous disadvantages such as wide bandwidth requirements, complex circuits for reading, higher power requirements, and the necessity of external timing pulses.

The main disadvantage of the NRZ method, which is the inability to generate clock pulses for synchronization and control, can be overcome by using a modified NRZ method. In the modified method, the direction of magnetization is changed each time the bit pattern contains a 1. This modified method may be called NRZ-1 because every time a 1 occurs, a change in state occurs; it may be called simply NRZ-M indicating non-return-to-zero mark; or it may be called NRZ-Modulo 2 (or IBM method) when a complementing flip-flop is used as a current source for writing.

A.3.4 Phase Modulation (Manchester Method)

The TC11 DECtape System employs the Manchester method of recording, which uses RZ polarity characteristics in terms of phase information. As an aid in understanding phase modulation, simply consider it as an NRZ-M recording technique with the addition of an external timing signal.

Assume that a binary number (such as 111000101) is to be written on a track of the magnetic tape surface using ordinary recording techniques. The maximum rate of current change occurs between 1s and 0s. During these changes, maximum flux is induced into the magnetic surface and subsequent reading develops a maximum output current. Thus, a long string of 1s or 0s tends to appear as one long 1 or 0.

Although it is possible to decipher such signals, it is more desireable to use a writing technique that causes some positive action in the center of each bit time. This can be accomplished by changing the direction (phase) of the write current in the middle of each bit time. This is called phase modulation.

In order to produce phase modulation, the normal steady-state logic to be stored must be changed before it reaches the write head. This is accomplished by using a write buffer that is loaded with the bit to be written during the main timing pulse and is then complemented at the center of the bit time.

In order to fulfill this requirement, two clock pulses are required to implement the Manchester method of recording. These pulses are Clock A and Clock B (see Figure A-3). Because Clock A occurs at the beginning of the bit time and Clock B at the center, they are sometimes referred to as the main clock pulse and the half-clock pulse, or (in the case of the TC11 System) as the TP0 and TP1 pulses. The half-clock pulse has the same frequency as the main clock pulse but is displaced by 180 degrees. Both clock pulses are prerecorded in the timing track of the DECtape magnetic tape.

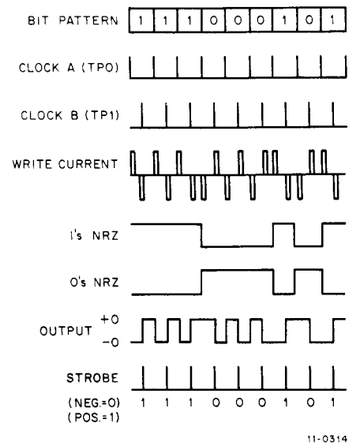


Figure A-3 Phase Modulation (Manchester)

As shown on Figure A-3, the write current uses a reversal of polarities. If a 1 is to be written, the write current is positive for the first half of a bit time and negative for the second half of the bit time. If a 0 is to be written, the opposite effect occurs: negative current for the first half, positive current for the second half. Note that if only the pulse in the first half of the bit time is considered, each bit time contains the information in an RZ code.

This method of writing is known as phase-modulation coding. The binary input information, retaining 1s and 0s for polarity indications, is written at Clock A time. The output signal polarity is complemented at Clock B time (each half bit time). Therefore, at the center of each bit time, a field reversal occurs as indicated by maximum signal output. The direction of each field reversal contains the written binary information. The resultant output waveform of the write operation is shown in Figure A-3. Note the similarity between this waveform and an NRZ-M waveform.

When information is to be read from the magnetic tape, Clock B serves as the strobe pulse. During the strobe operation, the transition (or phase) of the waveform is sensed. If the transition is positive, a 1 is read. If the transition is negative, a 0 is read. Note that the read current peaks near the center of each bit time whether a string of 0s or 1s occurs or not. The choice of polarities is arbitrary but there is a distinct 180-degree difference between a 0 and a 1 readout.

The Manchester method is virtually immune to noise because of the relatively narrow strobe pulse and because the system senses direction (phase) rather than amplitude. Noise outside of the narrow strobe time cannot affect the pulse. Noise occurring at strobe time cannot affect the pulse unless the noise is so large that it completely reverses the polarity of the data pulse.

With the Manchester technique, the timing pulses (Clock A and Clock B) are written directly on the tape in a special timing track. Therefore, data can be written immediately adjacent to previously written data without presenting any deciphering or synchronization problems.

A.4 BIDIRECTIONAL READING AND WRITING

The TC11 DECtape System can read from or write on a magnetic tape regardless of the direction of tape travel. In order to achieve this capability, two problems had to be considered. It is necessary to know the nature of these problems in order to understand the DECtape format and the operation of the TC11 Controller.

The first problem arises because the polarity of the magnetic pattern on the tape changes each time the tape is moved in a different direction over the read/write head. If a 1 is written on a tape moving in the forward direction, the 1 is reproduced as long as the tape is read in the forward direction. However, if the tape is read while moving in the reverse direction, the 1 is read as a 0. Thus, information written in one direction of tape motion is complemented if the tape is read in the opposite direction.

The second problem occurs because, in any given track, information is recorded serially on the tape. Assume that the number 001 110 has been written on the tape in the forward direction. Now, ignoring the complement effect for the moment, if the tape is read in the opposite direction, the number is assembled in reverse (obverse) order or 011 100.

The combined effect of these two problems (complement and reverse or obverse assembly) is referred to as *obverse complement.*

Figure A-4 illustrates the process of bidirectional reading and writing. This process is further clarified by an example of the obverse complement effect, which is shown in Figure A-5. In this example, the octal number 561 is recorded in one direction. If it is read in the opposite direction, all bits are first complemented (1s become 0s, 0s become 1s) and are then assembled in reverse order. Therefore, the number reproduced is octal 342.

The obverse complement can be converted to the original number by simply taking the obverse complement of the obverse complement. For example, the obverse complement of 001 is 110. Taking the obverse complement of 110 provides the number 001, the original number.

There are two methods employed in the TC11 System for reproducing the original number, regardless of the direction of reading. One method is used for the mark track, the other for the data tracks. Both methods are explained below.

A.4.1 Mark Track Reading

The DECtape magnetic tape contains a mark track that is used to identify data or control words. To simplify control operation, the mark track coding is designed to read the same regardless of the direction of tape travel. This is accomplished by using the codes that are identical in both the original and obverse complement forms. Thus, the controller recognizes a data word when it sees a 70 code, regardless of tape direction. For example, the obverse complement of 70 is 70; of 25 is 25. Thus, the system creates a mark track code structure that is symmetrical and implemented by obverse complement codes. For example, the controller recognizes a 26 as the block number code. This is what is read as the tape moves forward into the block. For symmetry, a block number is assigned at the opposite end of the block and given the code 51. When entering the block in the reverse direction, the 51 is read as 26 exactly as if the tape were moving forward. Another example is the code used for the end marks. The forward end mark is 22, the reverse end mark is 55. When the tape travels in the reverse direction, the obverse complement of 55 is 22, which is the same code used for the forward end mark.

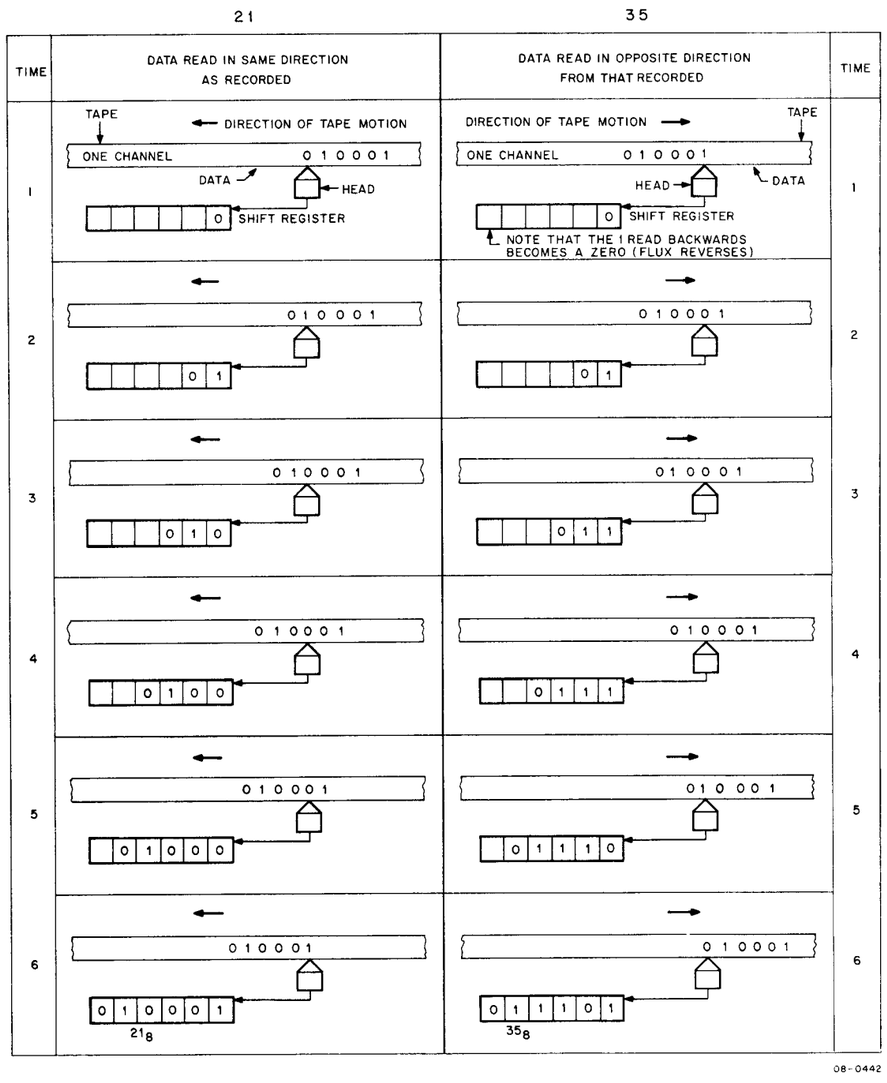


Figure A-4 Bidirectional Reading

The entire mark track is coded in this manner so that if the tape travels in the opposite direction, the mark track read head sees an identical series of codes and can react identically to them.

A.4.2 Data Track Reading

To read data tracks correctly, the programmer must know how the data was recorded in order to determine if he is reading the data or the obverse complement of the data.

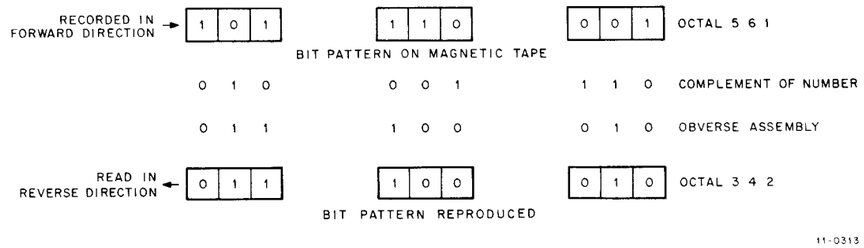


Figure A-5 Example of Obverse Complement

Because of the recording techniques, a word written in one direction does not read the same in the other direction. Each bit is complemented and displaced with the word (obverse complement). This effect must be considered during RALL and WALL functions because the hardware does not perform the obverse complement operation.

During READ DATA however, if the controller is reading in reverse, it converts the obverse raw data before transferring it to memory so that all data bits appear normal. During WRITE DATA, data is always written forward-oriented. As the tape moves forward, data is written directly on the tape. If the tape moves in reverse, each word is converted before being written so that when read in the forward direction, the bits appear normal.

The DECtape format provides two check areas to allow for a bidirectional hardware parity check. The 6-bit check is a longitudinal parity character written to force the number of 0s written as data to be odd on the basis of three 6-bit bytes to each data frame. With two check areas, a block written forward or reverse is read with correct parity in either direction.

A.5 TAPE FORMAT

Data is written on or read from the magnetic tape by means of a read/write head as described in previous paragraphs. In the TC11 System, there are 10 such heads distributed along the width of the tape, each head covering a narrow path referred to as a tape track or channel. Figure A-6 shows the tape stretched over the 10 heads.

Although there are 10 tracks on the tape, only five need be considered. These five are: timing track, mark track, and three data tracks. The other five tracks are identical counterparts to the first five and are used for redundant recording to increase system reliability. During writing, corresponding heads record identical information because they are wired in series. For example, the timing pulse is applied to both timing channel read/write heads and is recorded in both the normal and the redundant channel. During reading, the analog sum of the two heads is used to detect the correct value of the bit. Therefore, a bit cannot be misread unless the noise on the tape is sufficient to change the *polarity* of the *sum* of the signals being read.

The redundant recording of each character bit on nonadjacent tracks materially reduces bit drop out and minimizes the effect of skew. Series connection of corresponding track heads within a channel and the use of Manchester phase-recording techniques (Paragraph A.3.4) rather than amplitude-sensing techniques, virtually eliminates drop-outs.

The outside channel of the tape is the timing track. This track contains timing signals that have been prerecorded at a fixed frequency. The timing of operations performed by the tape drive is determined by the timing signals; thus, wide variations in the speed of tape motion do not affect system performance. The timing signal is also used to strobe information into or from the data channels.

The next channel is referred to as the mark track. The mark track records instructions that are used by the TC11 Controller to determine the exact position of the tape and to determine the type of information stored in the

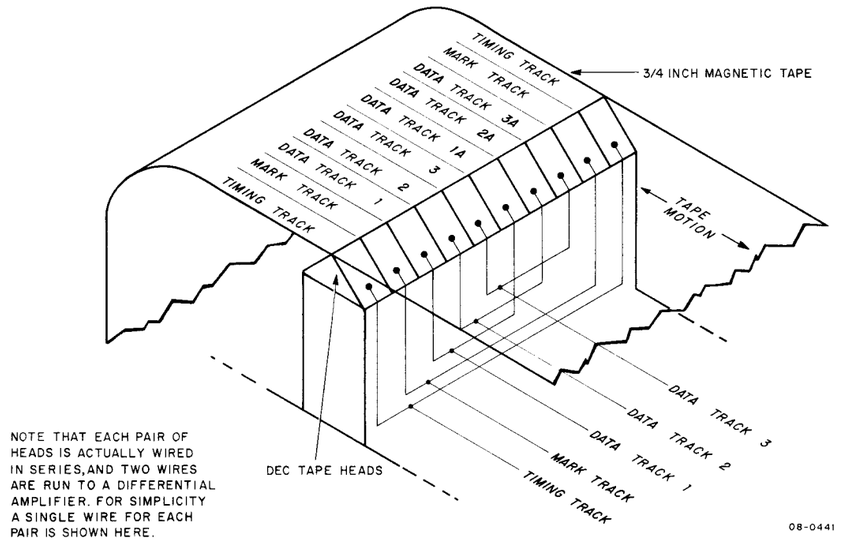


Figure A-6 DECtape Heads and Tape Tracks

associated data tracks. In effect, the mark track is used during reading and writing to indicate the beginning and end of data blocks and to determine the functions performed by the system. The codes used in the mark track are selected so that they read the same regardless of tape motion, thereby eliminating the obverse complement problem. An error check circuit associated with the mark track ensures that only permissible marks are used.

Note that once a tape is formatted (that is, timing and mark track recorded), the timing and mark tracks are then always read even though simultaneous write operations occur on the data tracks.

The next three channels are data tracks. These are located in the middle of the tape where the effect of skew is minimum. The data in one bit position of each track is referred to as a line or as a character. Six lines, or characters, make up a word; thus, the tape can record 18-bit data words. During normal data writing, the TC11 Controller disassembles the 18-bit word and distributes the bits so they are recorded as six 3-bit characters. Because PDP-11 computer words are 16 bits long, the controller (during normal operation) writes the extra two bits as 0s and ignores them when reading. However, during special modes, the extra two bits can be written and recovered.

A.5.1 Basic Tape Format

A 260-ft reel of DECtape (see Figure A-7) is divided into three major types of zones or areas: two end zones (forward and reverse), two extension areas (forward and reverse), and the information area.

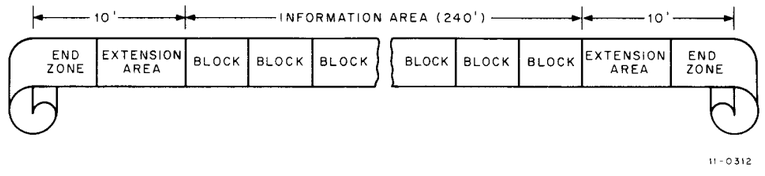


Figure A-7 Basic Tape Format

The forward and reverse end zones mark the end of the physical tape and are used for winding the tape around the heads and onto the take-up reel. The end zones never contain data. The length of each end zone (approximately 10 ft) is sufficient to ensure that once it is entered, there is adequate distance to stop tape motion without having the tape unwind off the reel.

The forward and reverse extension areas mark the end of the information region of the tape. The length of these areas is sufficient to ensure that once the end zone is entered and tape motion is reversed, there is adequate distance for the transport to come up to proper tape speed before entering the information area.

The third area of a DECtape is the information area, which consists of blocks of data. The standard is a nominal 578 blocks, each block containing 256 data words (nominally). In addition to the data words, each block contains 10 control words. An explanation of the block format is given in the following paragraph.

A.5.2 Block Format

Recording information on tape in blocks permits digital data to be partitioned into groups of words that are interrelated while at the same time reducing the amount of storage area that would be needed for addressing individual words. A simple example of such a group of words is a program. A program can be stored and retrieved from magnetic tape in a single block format, because it is not necessary to be able to retrieve only a single word from the program. The processor normally needs the complete program or none of it. It is necessary, however, to be able to identify and retrieve different programs that may not be related in any way. Thus, each program is stored in a different block on the tape.

Data is stored on the DECtape in a block format. The block format has the following advantages:

a. **identification** – each block is numbered and can be easily identified by a random search in either direction.

b. **error detection** – errors can be detected within each block by using serial parity checking.

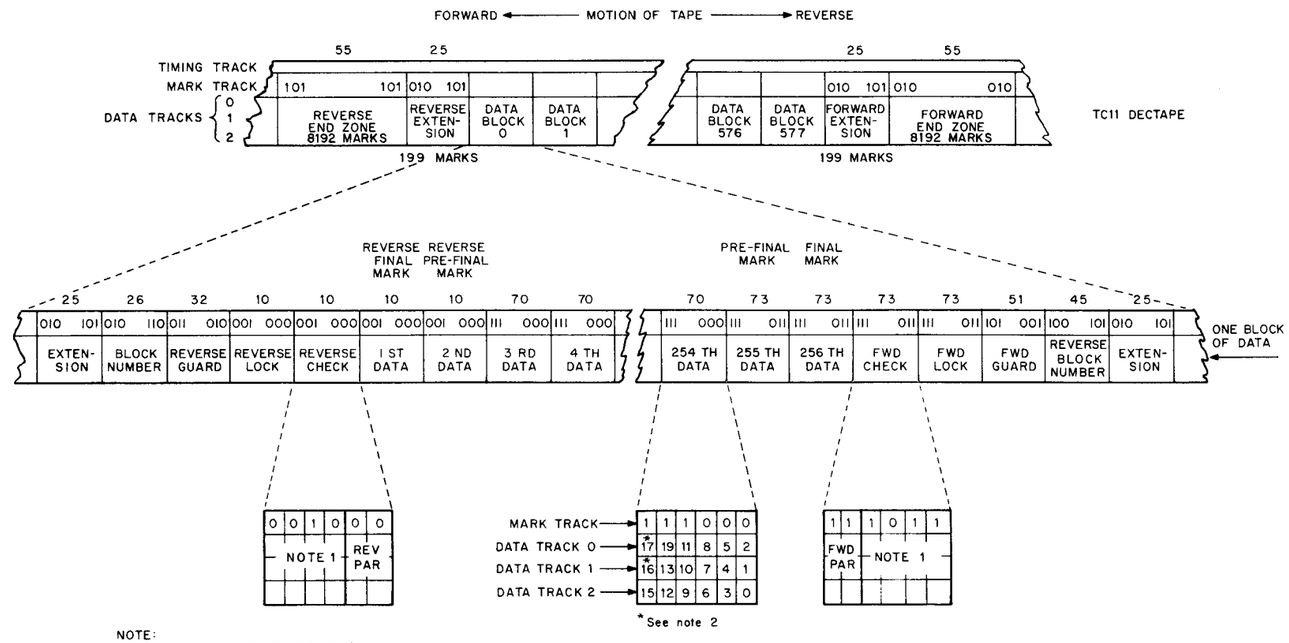
c. **bidirectional recording** – a block can be read or written while the tape is travelling in either direction.

The format of a block of data is shown in Figure A-8. A block of data consists of 256 data words and 10 control words (five on either side of the data words).

The mark track contains a code that identifies the information in each specific word position. For example, the octal code 70 indicates a data word, the octal code 26 indicates the block number, and the octal code 25 indicates an extension area. These codes are selected so that the entire block reads the same in either direction (it is assumed that the mark track is written in the forward direction).

As an example of the bidirectional quality of the mark track codes, assume that the tape is moving in the forward direction. In this instance, the octal code 26 represents the block number word, code 10 represents the first data word, and 73 represents the checksum word. If the tape is run in the reverse direction, the first block number to occur is the reverse block number (code 45), then the 256th data word (code 73), and then the reverse checksum (code 10). However, because the tape is running in the opposite direction, it causes the obverse complement of these codes to be read. Thus, 45 becomes 26, 73 becomes 10, and 10 becomes 73. Therefore, the codes read by the controller are identical to the codes that would be read if the tape were travelling in the forward direction. The entire mark track is coded in a similar fashion to ensure bidirectional reading and writing.

An explanation of each control or data word, including associated coding, is given in Table A-1.



NOTE:
1. IGNORED BY RDATA OR WDATA.
2. WRITTEN AS ZERO'S IN WDATA TRUNCATED IN RDATA RECOVERABLE IN SPECIAL MODES.

Figure A-8 DECtape Block Format

Table A-1
DECtape Codes

Code	Name	Function Detected
55	REVERSE END ZONE	Identifies the end zone that the tape transport leaves as it moves toward the data block zone. No action is taken by the TC11 Controller as this end zone is only for when the tape travels in the reverse direction.
25	REVERSE EXTENSION	This is a no-op code lying between blocks and for several feet on the inside of the end zone. When tape moves in the reverse direction, this area allows for turnaround time when reading the first and last blocks of data. Used by the TC11 Controller to synchronize timing logic between blocks.
26	BLOCK NUMBER	Contains the number assigned to the block by the TC11 Controller. When the system searches in the forward direction for a specific block of data, it examines the number stored in this word position. When code 26 is decoded by the mark track decoder in the controller, it indicates that the block number has been found and the processor is notified.
32	REVERSE GUARD	These two word positions are no-op codes that give the processor time to decide what function to perform on the block of data that has been identified.
10	REVERSE LOCK	

Table A-1 (Cont)
DECtape Codes

Code	Name	Function Detected
10	REVERSE CHECK	This is the last word occurring before a data word. The code initiates the checksum logic, which is actually a longitudinal parity character. This character forces the number of 0s written as data to be odd as calculated on the basis of three 6-bit characters per data word. The checksum character is not written until the FORWARD CHECK block is reached. The checksum character written in this block is the parity initiated by the FORWARD CHECK code when the tape is written in the reverse direction. Note the following: all 0s are written with a WDATA in the forward direction; read and included in parity check when RDATA in forward direction; written with parity when WDATA in reverse direction; read and included in parity check when RDATA in reverse direction.
10	FIRST DATA (REVERSE FINAL)	Indicates the first data word in the block. If tape is being read in the reverse direction, indicates the final data word loaded into the controller.

(continued on next page)

Table A-1 (Cont)
DECtape Codes

Code	Name	Function Detected
10	SECOND DATA (REVERSE PRE-FINAL)	Indicates the second data word in the block. If tape is being read in the reverse direction, indicates that the next to the last data word is being read.
70	DATA	Indicates that a data word is being read or written. The TC11 Controller continually checks to ensure that the mark track is coded. This code (70) is used for 252 of the 256 data words. The other four words are either coded 10 (first two data words in the block) or 73 (last two data words in the block).
73	PRE-FINAL MARK	Indicates the next to the last data word in the block. If tape is being read in the reverse direction, indicates the second data word.
73	FINAL MARK	Indicates the last data word in the block. If tape is being read in the reverse direction, indicates the first data word.
73	FORWARD CHECK	The parity checksum which has been calculated during transfers is either deposited here (during writing) or compared (during reading). If an error exists, it is detected by the controller which provides an error indication and notifies the processor. The checksum is written in the first two bit positions of the word. When the tape is moving in the reverse direction, this word initiates the checksum logic and the parity character is written in the REVERSE CHECK word.
73 51	FORWARD LOCK FORWARD GUARD	These two word positions are no-op codes used during reverse operation to give the processor time to decide what function to perform on the block of data that has been identified.
45	REVERSE BLOCK NUMBER	Contains the block number assigned by the controller when tape is used in the reverse direction. Performs the same function as the BLOCK NUMBER (26) word.

Table A-1 (Cont)
DECtape Codes

Code	Name	Function Detected
25	FORWARD EXTENSION	This is a no-op code lying between blocks and for several feet on the inside of the forward end zone. When tape moves in the forward direction, this area allows for turnaround time when reading the first and last blocks of data. Used by the TC11 Controller to synchronize timing logic between blocks
55	FORWARD END ZONE	Identifies the end zone that the tape transport leaves after reading the block. Indicates to the program that the tape has run out and that some action must be taken such as stopping or reversing the tape.

Because the DECtape used with PDP-11 Systems is identical in format to DECtapes used with other systems (such as the PDP-9, 10, and 15), the standard nomenclature has been retained for the codes listed in Table A-1. However, some of these code names might be confusing. For example, the FORWARD BLOCK NUMBER is used during forward tape motion and the REVERSE GUARD and REVERSE LOCK codes are also used during forward tape motion.

Figure A-9 illustrates the block format in a different manner. The top portion of the figure shows only the format used for forward tape motion. The bottom portion shows the format used only for reverse motion. Note that the codes used for reverse motion would be obverse complemented as read, making the two formats identical. Notes beneath the top portion of the figure describe the prime functions being performed.

A.5.3 Nonstandard Formats

The following notes refer to nonstandard formats and are included here for information purposes.

a. Must have a minimum of four data words (that is, two 10s, two 73s).

b. Must have an even number of words. Otherwise, there would be an odd number of 6-bit bytes for parity calculations. If an odd number of bytes exists, then: 1s become 0s, 0s become 1s in the reverse direction. This would cause an odd number of 0s in the forward direction and an even number of 0s in the reverse direction, thus causing incorrect parity.

c. May have a total of 173,530 mark track codes of which 2 x 8192 are for end zone codes, 2 x 199 are for extension codes, and 14 (minimum) are for each block of data (10 control and four data words).

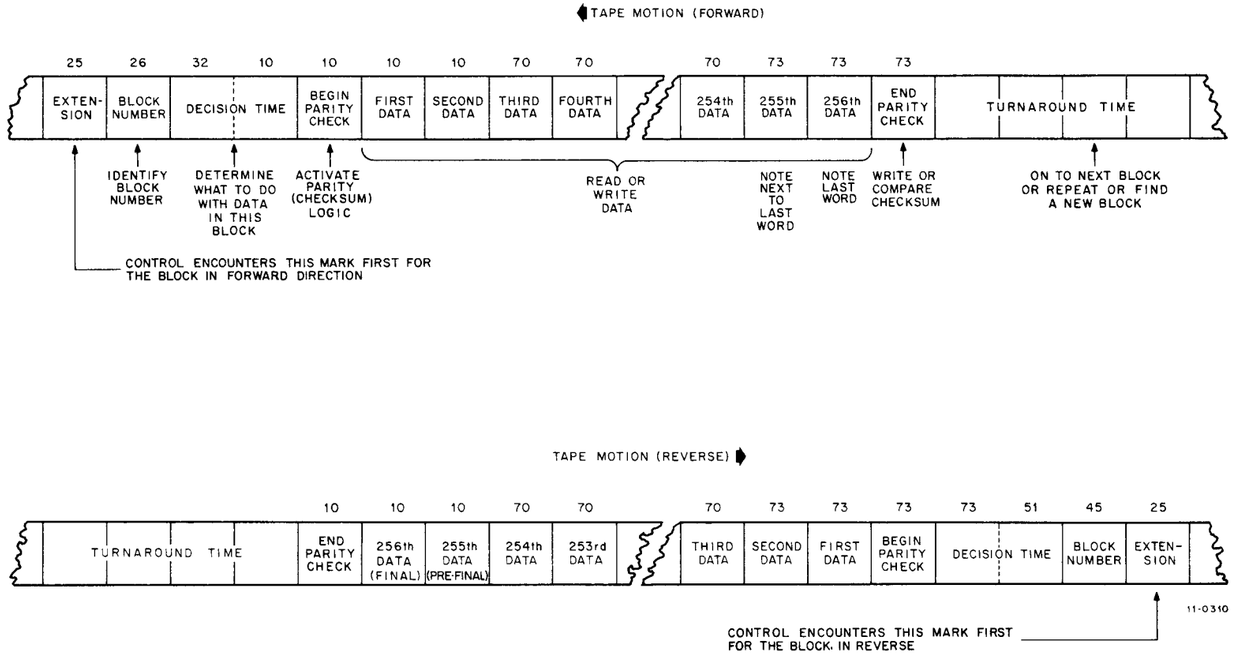


Figure A-9 DECtape Block Format for Forward or Reverse Motion

APPENDIX B
COMPARISON OF DECtape FORMATS

Although the tape formats for other DEC systems are often described as being identical, there is a distinction in the packing and labeling of bits in a data word. This distinction is illustrated in Figure B-1, which shows data word formats for the PDP-8, PDP-9, PDP-10, PDP-11, and PDP-15.

NOTE
The TC11 Controller is not compatible with the DECtape format used on the PDP-12 and the LINC-8.

Figure B-2 shows how three PDP-8 12-bit words would be read back as two PDP-11 18-bit words.

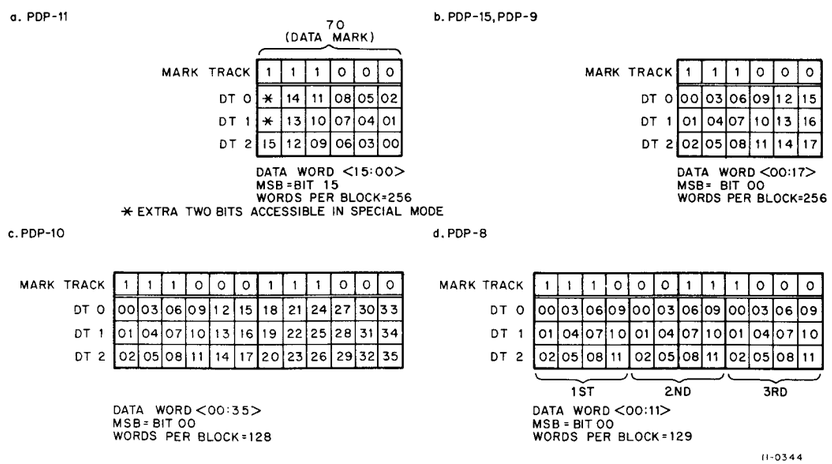


Figure B-1 Data Word Formats

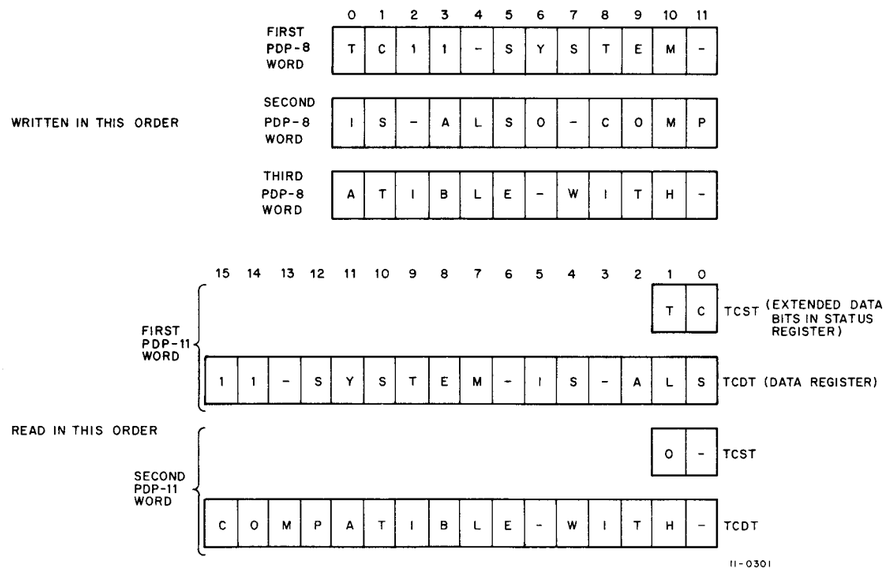


Figure B-2 Reading PDP-8 Words in PDP-11 Format