PART 1
CONSOLE TELEPRINTER

CHAPTER 1
LC8-E DECWRITER CONTROL

SECTION 1 INTRODUCTION

The LC8-E DECwriter Control interfaces the parallel version of the LA30 DECwriter (LA30P) to the PDP-8/E. The Control consists of a single M8329 quad module that plugs into the OMNIBUS and connects to the DECwriter with a signal cable that is supplied with the module.

The LA30 DECwriter is discussed here only to the extent necessary to both fully describe LC8-E Control operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the LA30, itself, can be found in the *LA30 DECwriter Maintenance Manual,* DEC-00-LA30-DA. Other publications and documents relevant to the LC8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* – DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. LA30 DECwriter Diagnostic, MAINDEC-8E-D2FA
d. DEC Engineering Drawing, DECwriter Control, E-CS-M8329-0-1.

SECTION 2 INSTALLATION

The LC8-E DECwriter Control is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the LC8-E Control in the PDP-8/E OMNIBUS. See Table 2-3, Volume 1, for information concerning recommended module priorities (the LC8-E is a "non-memory" option).

Connect the LC8-E to the DECwriter with the signal cable provided. J1 of the LC8-E, a 40-pin Berg Connector, connects to module slot A02 of the LA30P logic rack.

See Chapter 2 of the *LA30 DECwriter Maintenance Manual* for additional information concerning system installation and for procedures to be followed to checkout both the Control and the DECwriter.

SECTION 3 DESCRIPTION

Figure 1-1 is a block diagram of the LC8-E Control. Pin assignments for OMNIBUS signals and connector J1 signals can be found on engineering drawing no. E-CS-M8329-0-1. Information concerning pin assignments of the interconnecting cable is given in Section 5.

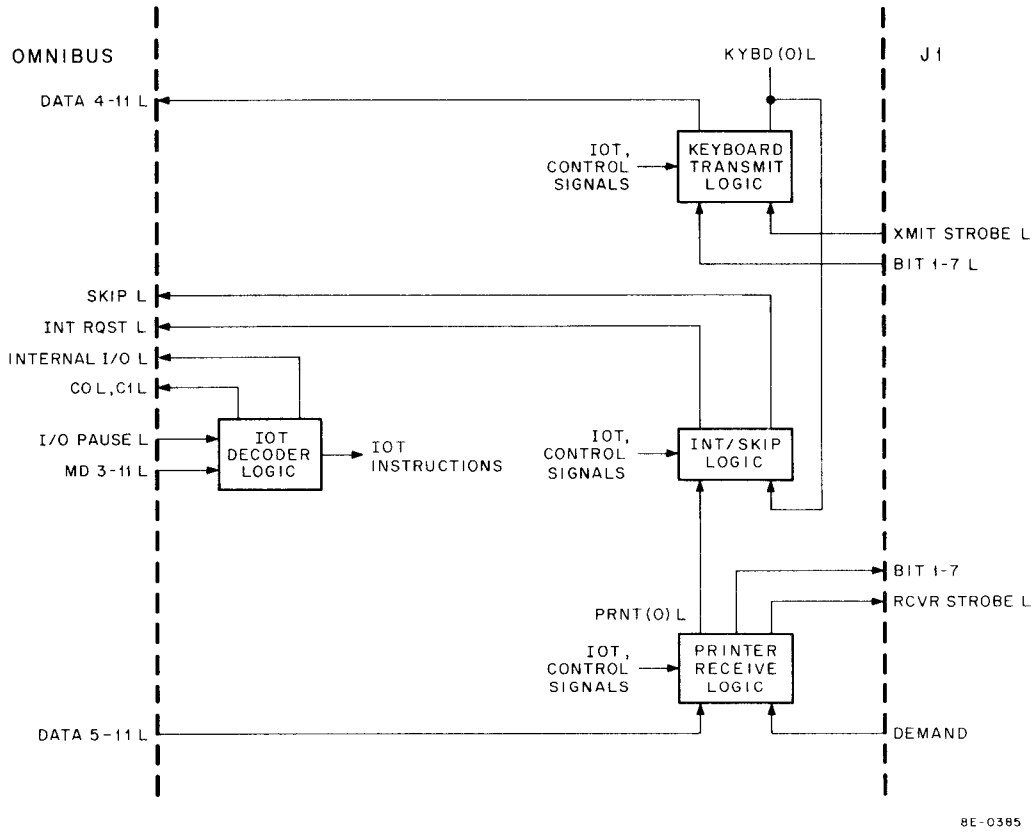

Figure 1-1 LC8-E Block Diagram

The LC8-E has two distinct functions: transfer of data from the CPU AC Register to the LA30 Printer Buffer Register and transfer of data from the LA30 Keyboard Buffer Register to the AC Register. The transfer of data to the LA30 Printer Buffer is carried out by the printer receive logic. When the LA30 is able to receive data, it asserts the DEMAND signal. This signal sets the printer flag in the printer receive logic. The resulting PRNT (0) L signal causes the INT/skip logic to assert OMNIBUS INT RQST L if the LC8-E has been logically connected to the interrupt system. Alternatively, PRNT (0) L can be tested by a program skip instruction in the INT/skip logic. In either case, the computer ultimately proceeds to a program subroutine that begins the data transfer. When this subroutine is executed, the information is transferred from the AC Register to the DATA 5–11 lines and clocked into a 7-bit register in the printer receive logic. The register outputs are available at J1 as the BIT 1–7 signals. The logic then generates a RCVR STROBE L signal that clocks the BIT 1–7 data into the Printer Buffer Register, clears the Printer flag, and causes the LA30 to negate the DEMAND signal.

The transfer of data from the LA30 Keyboard Buffer Register to the AC Register is carried out by the keyboard transmit logic. When an LA30 key is depressed, information is applied, via the BIT 1–7 lines, to a 7-bit register in the keyboard transmit logic. When the LA30 generates an XMIT STROBE L signal, the information is clocked into the 7-bit register and the KYBD (0) signal is asserted. The KYBD (0) L signal can be tested in the INT/skip logic with a skip instruction, or the interrupt system can be used to cause the program to enter an appropriate subroutine. When the subroutine is executed, the information is gated from the register in the keyboard transmit logic to lines DATA 5–11 (the logic asserts the DATA 4 L signal separately so that the input character is compatible with the modified-ASCII Teletype® code), then to the AC Register. The AC is loaded and, simultaneously, KYBD (0) L is negated.

®Teletype is a registered trademark of Teletype Corporation.

SECTION 4 DETAILED LOGIC

1.1 IOT DECODER LOGIC

The IOT decoder logic is shown in Figure 1-2. The LC8-E uses 12 IOT instructions, 6 for the keyboard functions and 6 for the printer functions (one of the listed printer IOTs — Skip on Printer or Keyboard Interrupt — applies to both functions). More than one LA30 DECwriter can be interfaced to the PDP-8/E at the same time. The LC8-E Control associated with each LA30 must have a unique device selection code. Therefore, the M8329 Control Module is fabricated with machine-inserted jumpers and solder terminals that allow the user to assign any two of 64 possible device selection codes to a particular LC8-E (care should be taken when assigning device selection codes to preclude multiple assignments of the same code). Figure 1-2 illustrates the octal codes and mnemonics that pertain when the LC8-E Control is manufactured. The octal codes and mnemonics are listed in Table 1-1 and the respective functions, which remain constant regardless of the code or mnemonic, are detailed.

Figure 1-2 identifies the 12 machine-inserted jumpers, W1 through W12, and 6 groups, lettered from A to F, of 4 numbered solder terminals (jumper and terminal designations are etched on the quad module for each identification). To change a control device selection code, first cut a selected "W" jumper (or jumpers); then, solder a new jumper between designated terminals associated with the "W" jumper(s). For example, the device selection code for the keyboard functions can be changed from 03 to 13 by removing W5 and connecting terminals C3 and C4; the printer functions device code can be changed from 04 to 10 by removing W6 and W8 and connecting terminals C2 and C4 and D2 and D3.

As Figure 1-2 shows, the device selection code signals, 603X and 604X, are applied to separate DEC 7442 Decoder ICs. The device operation codes represented by bits MD 9, 10, and 11 are then decoded by E9 and E6 to provide the listed IOT instruction signals. Note that the device selection code signals assert the OMNIBUS INTERNAL I/O L signal; thus, the positive I/O bus interface ignores the IOT instruction.

Three of the keyboard IOT instruction signals cause OMNIBUS "C" lines to be activated. When the KCC L signal is generated, both the C0 L and C1 L signals are asserted; the resulting transfer of 0s clears the AC Register. The KRB L signal also results in a transfer to the AC; however, this transfer involves data from the keyboard, rather than 0s. Finally, the KRS L signal causes only the C1 L signal to be asserted; the result is an inclusive-OR transfer of data to the AC.

1.2 PRINTER RECEIVE LOGIC

The printer receive logic is shown in Figure 1-3. The 7-bit register is shown only in part, the logic associated with bits DATA 10–6 being similar to that illustrated for bits 11 and 5. Significant signals are related by the timing diagram in Figure 1-4. Refer to both figures when reading the logic description.

The LA30 printer routine is initiated by the program instruction TFL, Set the Printer Flag. At TP3 time of this instruction, NAND gate E7 is enabled, causing the PRNT flip-flop to be set. This flip-flop is also set by the DEMAND signal, which is asserted by the printer each time it completes a print cycle (Figure 1-4 illustrates this signal rather than the TFL L signal). If the LC8-E is logically connected to the interrupt system, as Figure 1-4 and this discussion assume, PRNT (0) L causes the INT/skip logic to assert OMNIBUS INT RQST L. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The TSK instruction in the routine causes the program to jump to an LC8-E routine that determines if the printer or keyboard requested the interrupt (other options are open to the programmer, this is but one example). Ultimately, the LC8-E printer routine executes the TLS instruction.

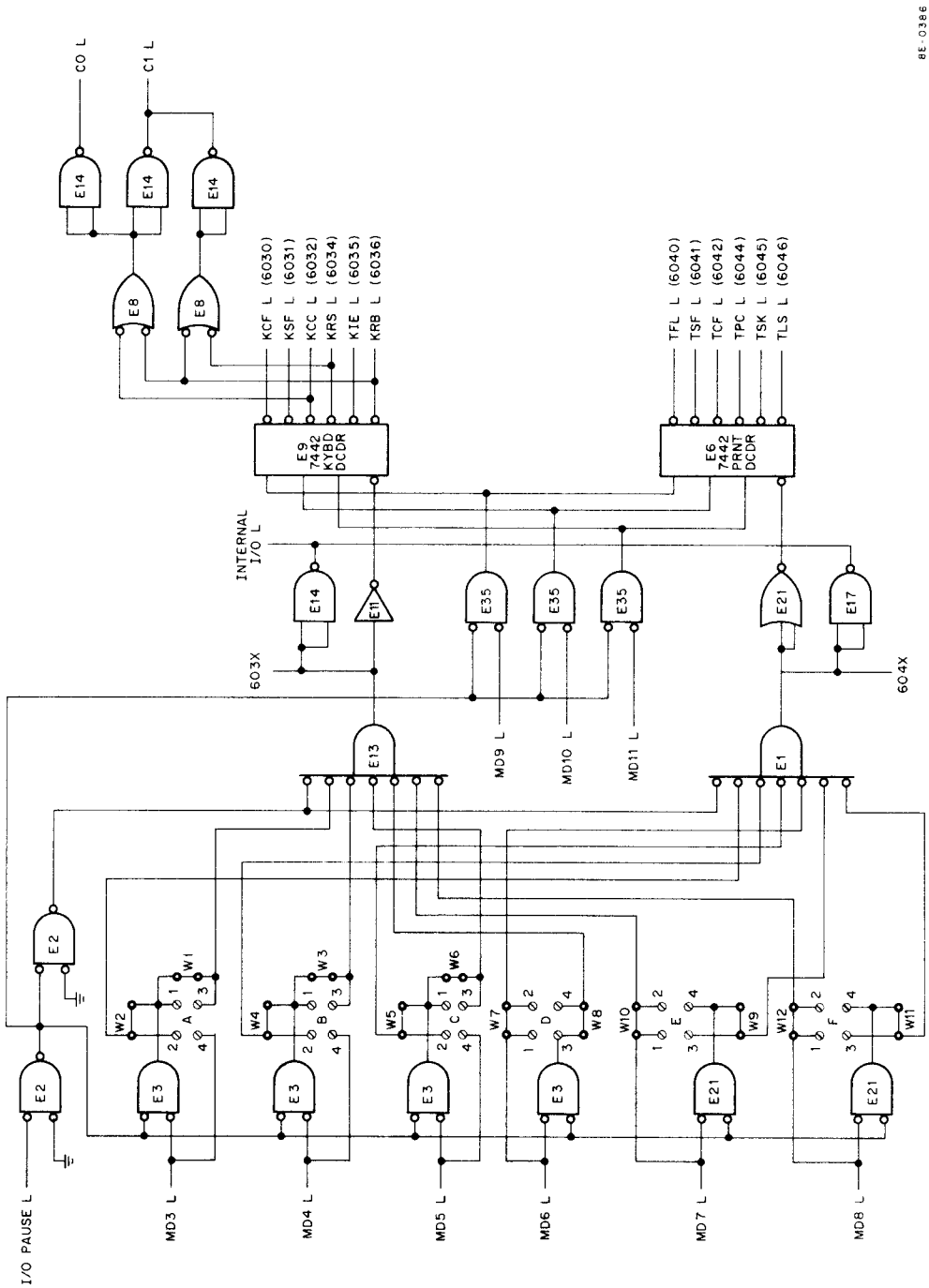

Figure 1-2 LC8-E IOT Decoder

Table 1-1
LC8-E IOT Instruction List

Octal Code	Mnemonic	Function
6030	KCF	Clear the Keyboard flag. Clears the KYBD flip-flop.
6031	KSF	Skip on the Keyboard flag. Senses the state of the KYBD flip-flop. If the flip-flop is set, increments the program counter so that the next sequential instruction is skipped.
6032	KCC	Clear the flag, clear the AC. Clears both the KYBD flip-flop and the AC Register.
6034	KRS	Read the keyboard buffer. Gates character information from the keyboard transmit logic and ORs it into AC Register bits 5 through 11. Sets AC4.
6035	KIE	Set/clear interrupt enable. Sets the INT ENA flip-flop if AC11 is logic 1; clears the flip-flop if AC11 is logic 0.
6036	KRB	Read the keyboard buffer, clear the flag, clear the AC. Gates character information from the keyboard transmit logic and jams it into AC Register bits 5 through 11. Sets AC4. Clears the KYBD flip-flop.
6040	TFL	Set the printer flag. Sets the PRNT flip-flop.
6041	TSF	Skip on the Printer flag. Senses the state of the PRNT flip-flop. If the flip-flop is set, increments the program counter so that the next sequential instruction is skipped.
6042	TCF	Clear the Printer flag. Clears the PRNT flip-flop.
6044	TPC	Load the printer buffer and print. Causes the character information to be gated to the BIT 1—7 lines. Sets the RCVR STROBE flip-flop. At TS2 of the next instruction, the information is loaded into the LA30 input buffer.
6045	TSK	Skip on a keyboard/printer interrupt request. Skips the next sequential instruction if the INT ENA flip-flop is set (the LC8-E is logically connected to the interrupt system) and if either the KYBD flip-flop or the PRNT flip-flop is set.
6046	TLS	Load the printer buffer and print. Clears the flag. The character information is gated to the BIT 1—7 lines. Sets the RCVR STROBE flip-flop. At TS2 of the next instruction, the information is loaded into the LA30 input buffer. Clears the PRNT flip-flop.

During TS2 of the TLS instruction, information is gated from the AC Register to the DATA lines and remains on the DATA lines through TS3. When TLS L is decoded in the IOT Decoder logic, it enables NOR gates E5B and E5D (Figure 1-3). The enabled output of E5D causes the information on lines DATA 5—11 to be gated to the D-inputs of the register flip-flops, while at the same time providing a high level on the D-input of E27B, the RCVR STROBE L flip-flop. At TP3 time of the instruction the register flip-flops are clocked, flip-flop E27B is set, and the PRNT flip-flop is cleared. The register data is applied, via the BIT 1—7 lines, to the printer buffer

register. During TS2 of the instruction following TLS, NAND gate E29 asserts the RCVR STROBE L signal (flip-flop E27B is cleared at TP3 time of this instruction). This signal loads the printer buffer register and negates the DEMAND signal. When the print cycle ends approximately 30 ms later, the DEMAND signal is again asserted and a new transfer is begun.

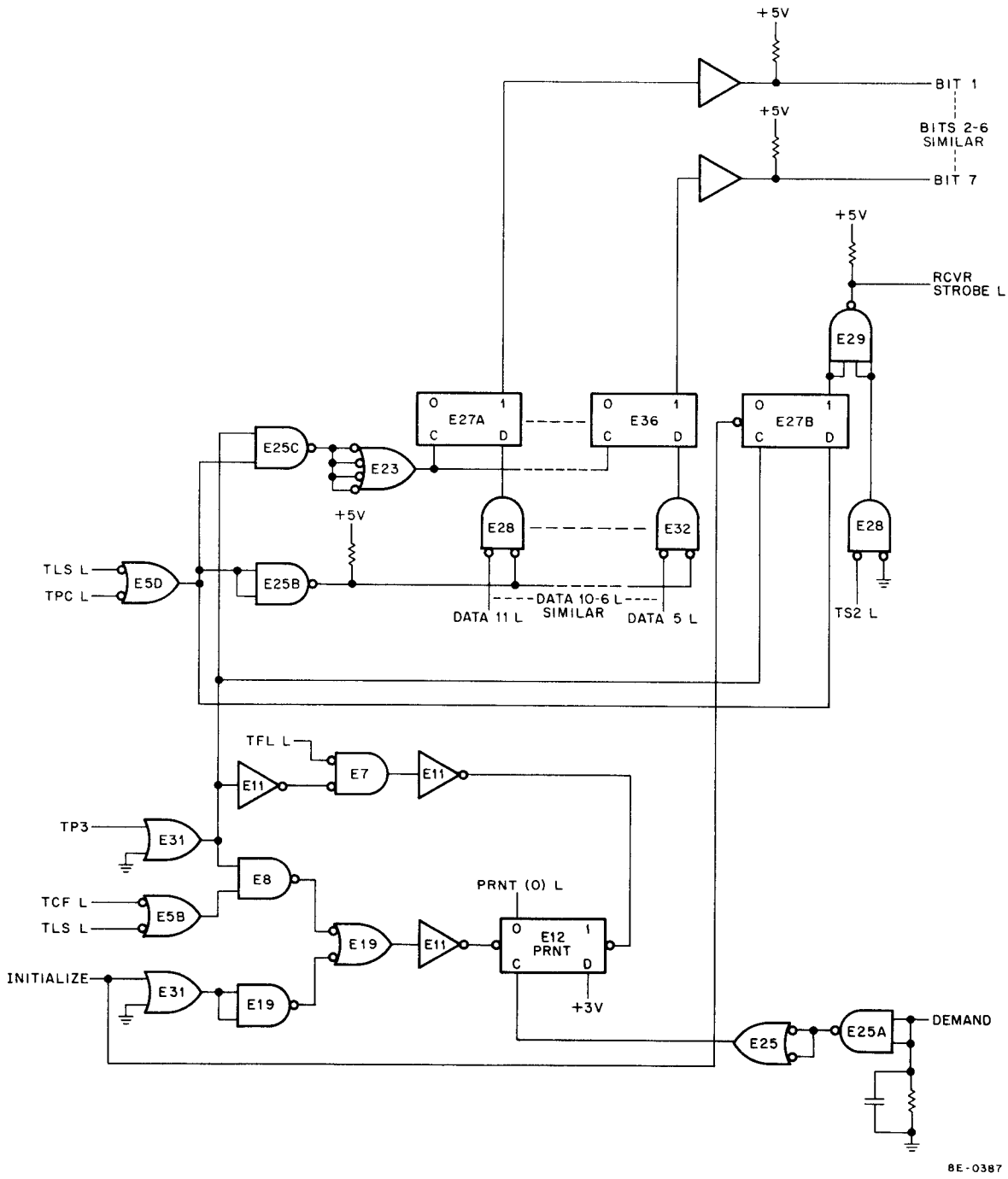

Figure 1-3 Printer Receive Logic

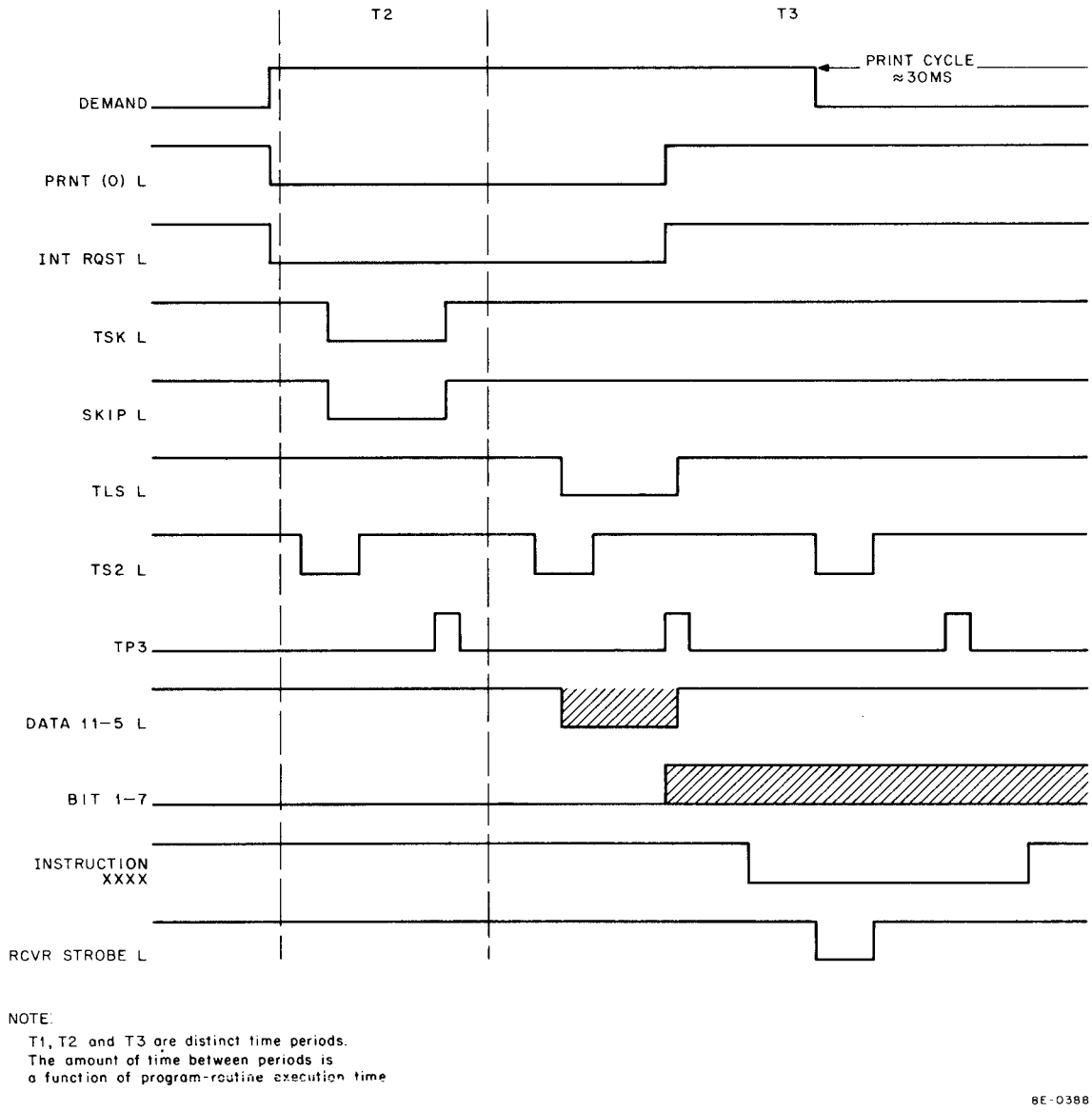

Figure 1-4 Timing, Printer Receive Logic

1.3 KEYBOARD TRANSMIT LOGIC

The keyboard transmit logic is shown in Figure 1-5. The 7-bit register is shown only in part. Significant signals are related by the timing diagram in Figure 1-6. Refer to both figures when reading the logic description.

The user initiates the keyboard sequence by depressing a key on the LA30. The character information is placed on the BIT 1–7 lines. After a period of time that allows the BIT lines to settle, the keyboard generates the XMIT STROBE L signal. This signal clocks the information into the 7-bit register and sets the KYBD flip-flop. If the LC8-E is logically connected to the interrupt system, as assumed, KYBD (0) L causes the INT/skip logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The TSK instruction in the routine causes the program to jump to an LC8-E routine that determines if the printer or keyboard requested the interrupt. Ultimately, the LC8-E keyboard routine executes the KRB instruction.

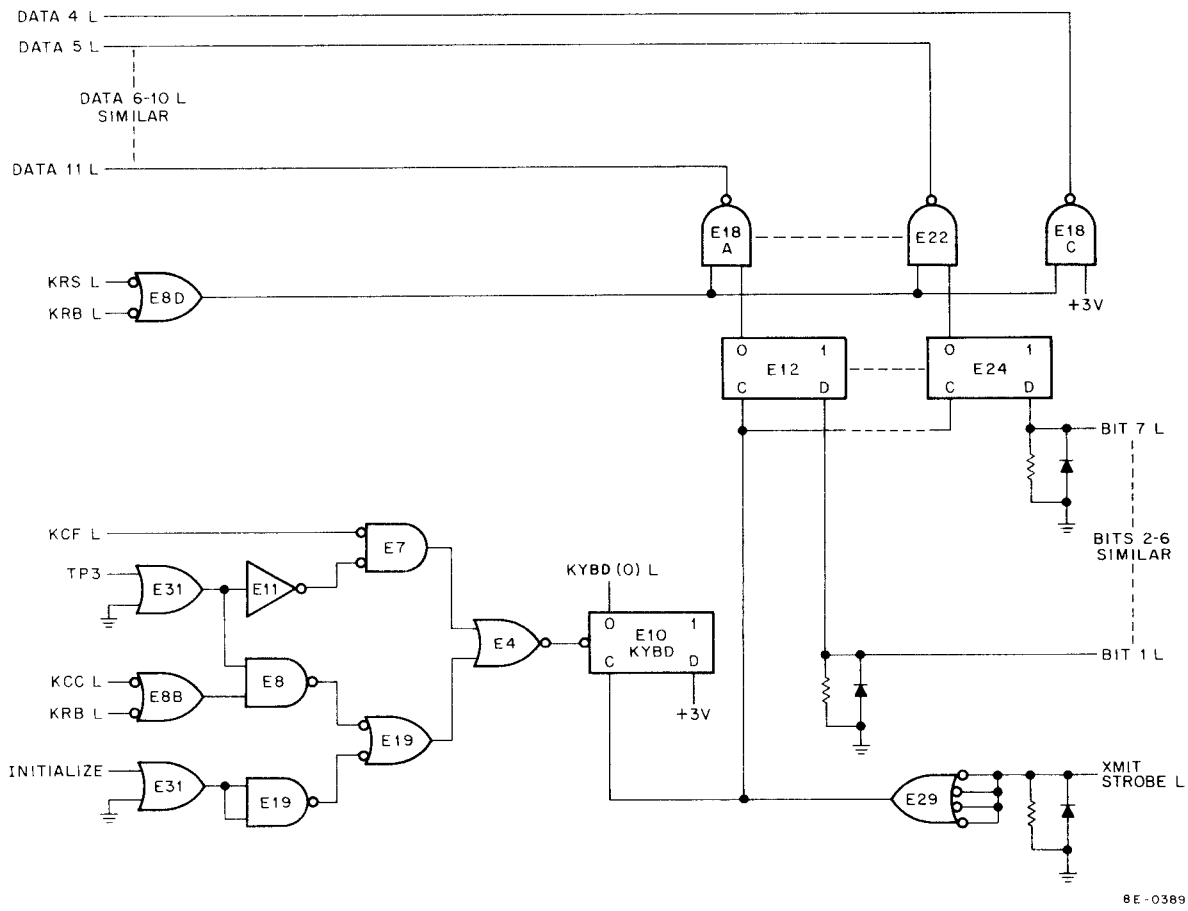

Figure 1-5 Keyboard Transmit Logic

When the KRB instruction is decoded, the IOT decoder logic generates the KRB L signal and activates the C0 and C1 lines. The KRB L signal enables NOR gate E8D; the output signal from E8D gates the information from the register outputs to DATA lines 5–11, and also causes NAND gate E18C to assert DATA 4 L. The DATA lines are gated to the AC Register and the information is clocked into the register at TP3 time. Also at TP3, the KYBD flip-flop is cleared, readying the logic for a new data transfer.

1.4 INT/SKIP LOGIC

The INT/skip logic is shown in Figure 1-7. The PRNT (0) L signal and the KYBD (0) L signal can cause program skips when tested by instructions TSF and KSF, respectively. The signals can also be tested by the TSK instruction, provided the INT ENA flip-flop, E10, has been set, logically connecting the LC8-E to the interrupt system. When E10 is set, the TSK L signal enables NAND gate E4D, which, in turn, enables AND-NOR gate E15 if either the PRNT (0) L signal or the KYBD (0) L signal is asserted. Simultaneously, NAND gate E17 asserts the INT RQST L signal.

The INT ENA flip-flop is set by the OMNIBUS INITIALIZE signal for the PDP-8 Family program compatibility. To clear the flip-flop, removing the LC8-E from the interrupt system, load AC11 with logic 0 and then program the KIE instruction. The logic 0 in AC11 keeps the DATA 11 L signal negated. Thus, the D-input of E10 remains high. At TP3 time, NAND gate E7 provides a clock pulse for E10, clearing the flip-flop. E10 can be set at any time with the same instruction merely by loading AC11 with logic 1.

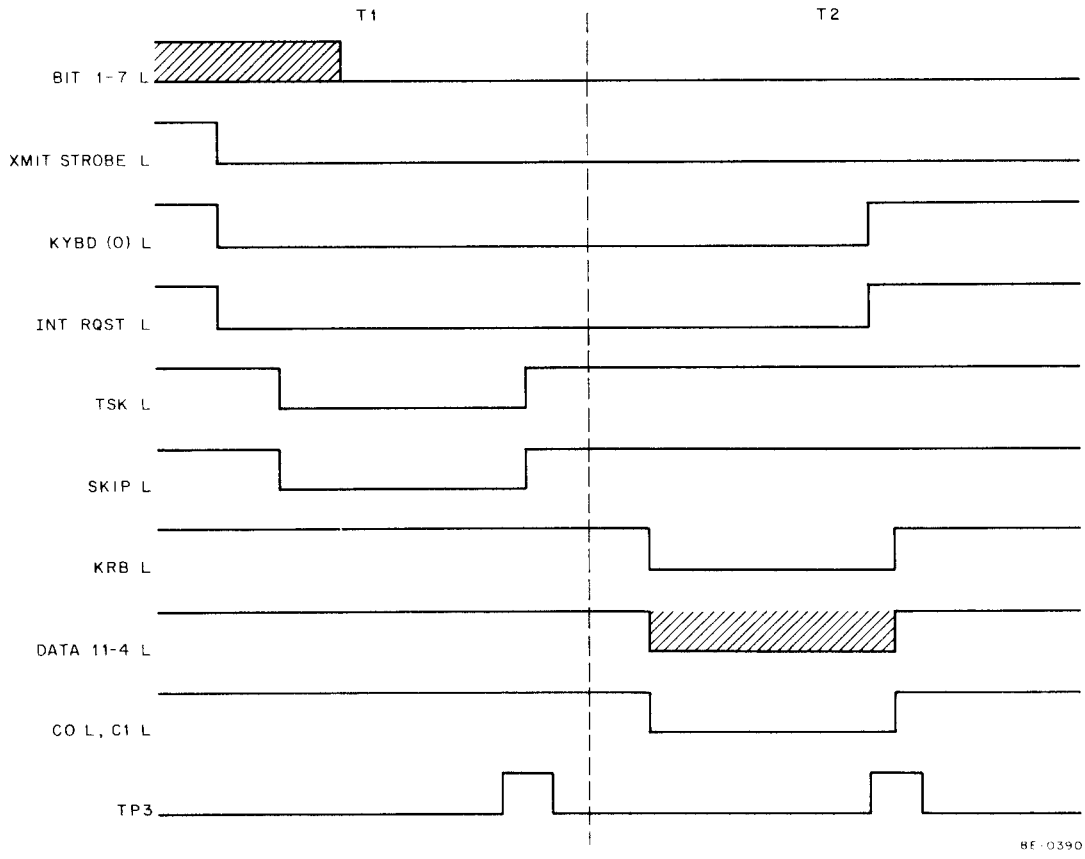

Figure 1-6 Timing, Keyboard Transmit Logic

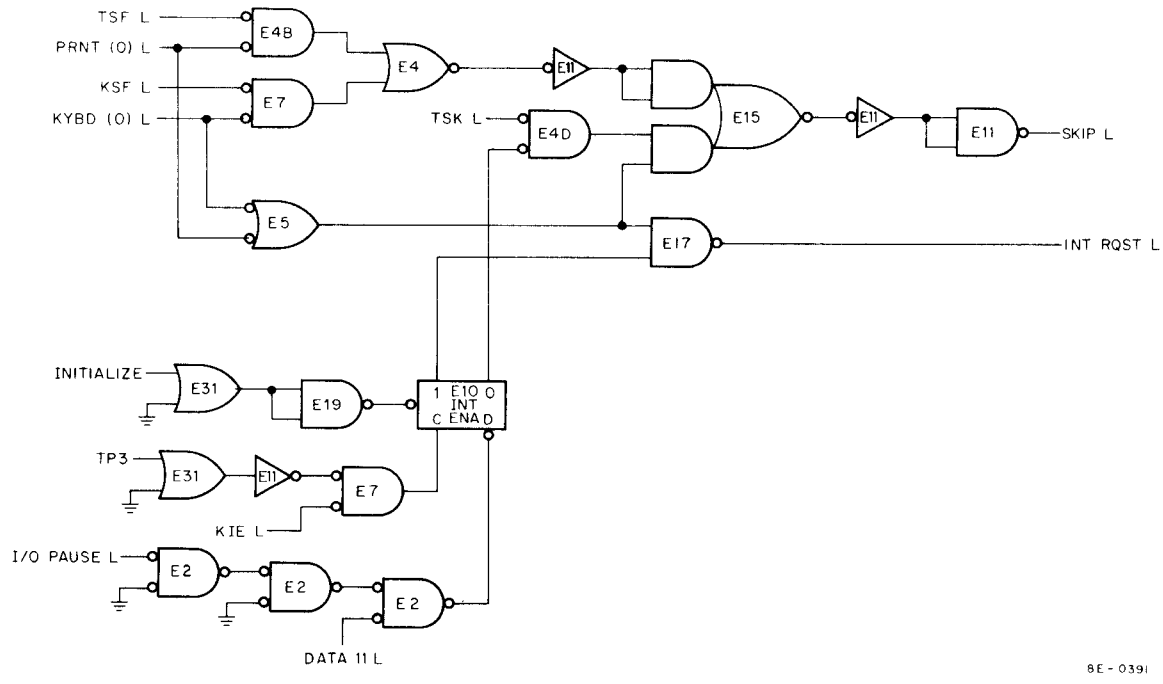

Figure 1-7 INT/Skip Logic

SECTION 5 MAINTENANCE

Refer to Volume 1 and to the *LA30 DECwriter Maintenance Manual* for maintenance information that pertains to both the LC8-E Control and the LA30 DECwriter. The LA30 DECwriter Diagnostic, MAINDEC-8E-D2FA, should be run when an error is suspected.

SECTION 6 SPARE PARTS

Table 1-2 lists recommended spare parts for the LC8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-2
LC8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
19-10394	IC DEC 5384	1
19-10392	IC DEC 5380	1
19-10391	IC DEC 5314	1
19-10046	IC DEC 7442	1
19-9929	IC DEC 7417	1
19-9973	IC DEC 97401	1
19-9686	IC DEC 7404	1
19-9056	IC DEC 74H00	1
19-9004	IC DEC 7402	1
19-5580	IC DEC 7450	1
19-5579	IC DEC 7440	1
19-5575	IC DEC 7400	1
19-5547	IC DEC 7474	1
10-1610	Capacitor, 0.01 μF, 100V, 20% Disk	1
10-0067	Capacitor, 6.8 μF, 35V, 20% Tant	1
10-0024	Capacitor, 47 pF, 100V, 5% DM	1
70-8417	Signal Cable	1

PART 2
PAPER-TAPE READER/PUNCH

CHAPTER 2
PC8-E HIGH-SPEED PAPER-TAPE READER/PUNCH

SECTION 1 INTRODUCTION

The PC8-E (or the desk-top model, PC8-EB) Reader/Punch option consists of a control module and a high-speed paper-tape reader/punch manufactured by DEC [Model PC04BL (60 Hz) or PC04BM (50 Hz)]. The control (DEC M840) plugs into the PDP-8/E OMNIBUS and connects to the external reader/punch via two signal cables that are supplied with the system.

The PC04 Reader/Punch is discussed here only to the extent necessary to fully describe control operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the reader/punch, itself, can be found in the *PC04/PC05 Paper-Tape Reader/Punch Maintenance Manual* [DEC-00-PC0A-D (1)]. Other publications and documents relevant to the PC8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. *Roytron Model 500 Maintenance Manual*
d. PC8-E Diagnostic, MAINDEC-8E-D2CA
e. DEC Engineering Drawing, Reader/Punch Control, E-CS-M840-0-1.

SECTION 2 INSTALLATION

The PC8-E Reader/Punch and Control is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the PC8-E Control Module in the PDP-8/E OMNIBUS. Refer to Table 2-3, Volume 1, for information concerning recommended module priorities (the PC8-E is a "non-memory" option).

Connect the control to the reader/punch with the two signal cables provided. J1 of the control, a 40-pin Berg Connector, connects to reader/punch module slot B1, a DEC M955 Connector. J2 of the control connects to module slot A1 (refer to Section 5 for cable and connector pin assignments).

Refer to Chapter 2 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* (DEC-00-HGPA-D) for additional information concerning system installation and for procedures to be followed to checkout both the control and the reader/punch.

SECTION 3 DESCRIPTION

Figure 2-1 is a block diagram of the PC8-E Control. The functions of the control can be grouped conveniently according to reader functions and punch functions, as illustrated by the block diagram. Consider the reader functions, represented by the logic blocks above the broken line.

The control logic generates signals that control the PC04 tape-feed operation. As the paper tape passes over the PC04 photoarray, signals representing the punched characters are strobed into the Control Buffer Register. The buffered information is then transferred to the PDP-8/E AC Register and operated on by subsequent program instructions.

The tape-feed operation can be initiated under program control or by activation of the Reader FEED switch on the PC04 front panel. If the switch is used, the tape feeds through the read station but data is not transferred from the Control Buffer Register. If data is to be transferred, the tape-feed operation must be program-initiated.

Two IOT instructions, 6014 (Fetch Reader Character) and 6016 (Read Buffer, Fetch Reader Character), read the information currently over the photoarray and then initiate tape feed. When either of these instructions is decoded by the IOT decoder logic, the read tape logic generates an ENABLE signal that triggers the clock logic. The first CLOCK PULSE produced enables the read tape logic to generate an RDR DATA STROBE pulse. This pulse clocks the RDR Buffer Register, loading the register with the information present on the READ HOLE 1–8 lines.

In addition to clocking the RDR Buffer Register, the RDR DATA STROBE signal sets the RDR FLAG flip-flop in the INT/skip logic and clears the RDR RUN flip-flops in the tape read logic. If the control has been logically connected to the computer interrupt system by a previous 6010 instruction, or by the INITIALIZE signal, the OMNIBUS INT RQST L signal is asserted. The computer enters the interrupt servicing routine to determine the identity of the requesting device. The 6011 instruction in the routine causes the computer to proceed to the PC8-E subroutine to service the interrupt request (refer to Table 2-1 for IOT instruction descriptions).

After producing the first CLOCK PULSE, the clock logic generates a SHIFT PULSE. This causes the motor control logic to provide stepping signals for the PC04 Reader Motor. The motor shaft turns, feeding the tape through the read station. After two steps, the next character on the tape appears over the photoarray; the current read operation is completed. If a new 6014 or 6016 instruction has been issued, another RDR DATA STROBE is generated and this character is loaded into the RDR Buffer Register. Each RDR DATA STROBE loads a character into the register. The register data is transferred to the CPU AC Register by the 6012 or 6016 instruction. If a 6014 or 6016 instruction is decoded between each RDR DATA STROBE and the next CLOCK PULSE, reader operation is continuous, at a rate of 300 characters/second. Otherwise, the character rate is limited to 25 characters/second.

The tape status logic monitors the FEED HOLE signal from the PC04. When the tape-read mechanism is out of tape, the tape status logic provides a signal that inhibits program generation of the motor stepping signals and clears the tape read logic.

Now consider the punch functions, represented by the logic blocks below the broken line in Figure 2-1. The punch motor operates continuously when power is applied to the PC04. The punch mechanism (Roytron Model 500) provides a PUNCH SYNC signal at the beginning of each punch mechanical cycle. This signal synchronizes the control timing and the rotating motor shaft. If a 6024 or 6026 instruction is decoded, the ENABLE PUNCH BUFFER L signal is generated by the IOT decoder logic. Whatever information is on the DATA 4–11 lines can now be clocked into the Punch Buffer Register. At TP3 time of the instruction the PUNCH STROBE signal clocks the register, transferring the character signals from the DATA 4–11 lines to the HOLE 1–8 lines.

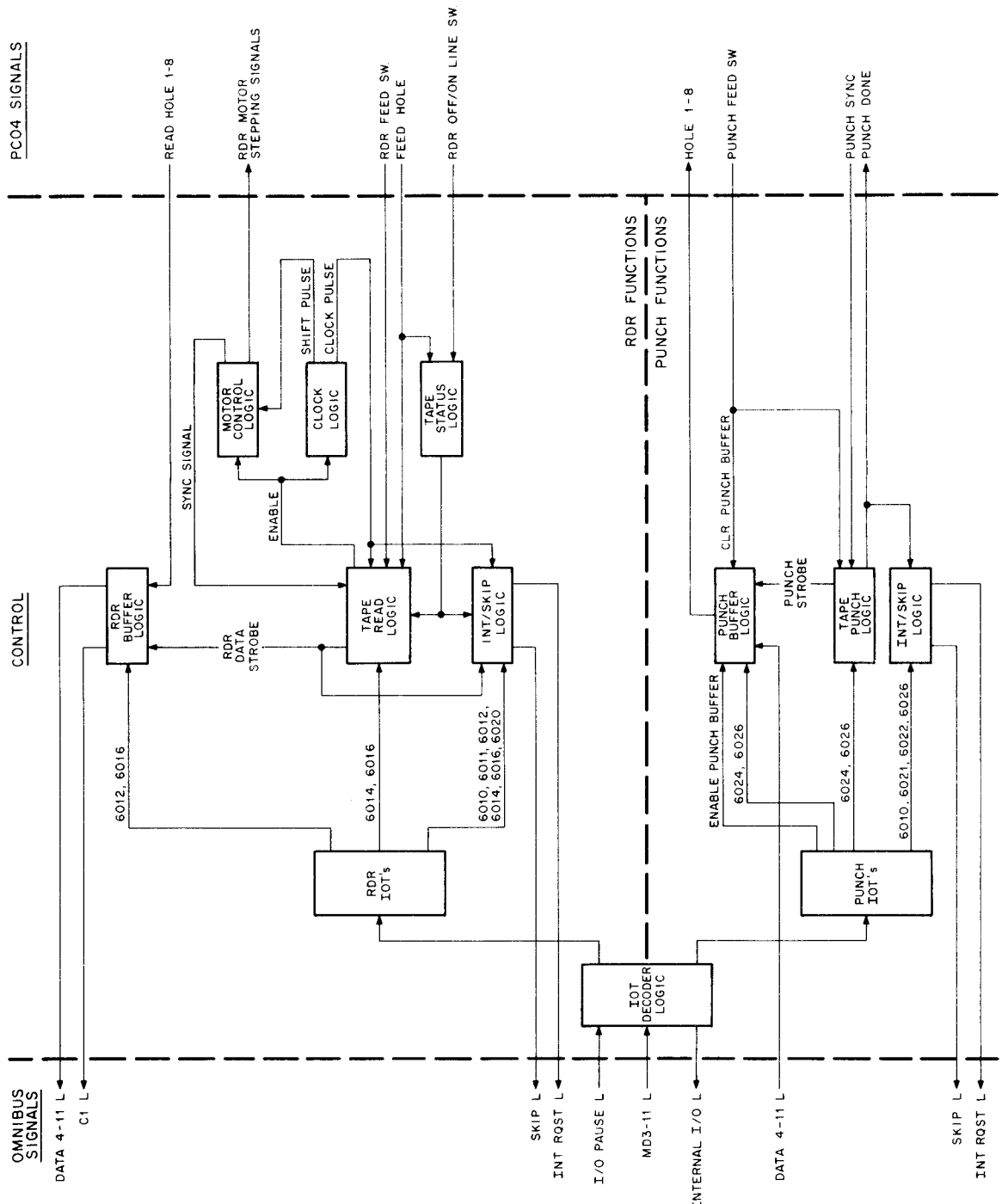

Figure 2-1 PC8-E Control, Block Diagram

Table 2-1
PC8-E IOT Instructions

Octal Code	Mnemonic	Function
6010	RPE	Set the INT ENA flip-flop. The PC8-E is logically connected to the computer interrupt system.
6011	RSF	Skip on Reader flag. Senses the state of the RDR FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6012	RRB	Read the RDR Buffer Register. Causes the RDR Buffer Register to be ORed into the AC Register, clears the RDR FLAG flip-flop.
6014	RFC	Fetch a character from the tape. Clears the RDR FLAG flip-flop, loads a character into the RDR Buffer Register from the tape, sets the RDR FLAG flip-flop when the RDR Buffer Register is loaded.
6016	RRB, RFC	Microprogram of 6012 and 6014. RDR Buffer Register contents are ORed into AC Register, RDR FLAG flip-flop is cleared, character is loaded into Register, and RDR FLAG flip-flop is set.
6020	PCE	Clear the INT ENA flip-flop. The PC8-E is disconnected from the computer interrupt system.
6021	PSF	Skip on Punch flag. Senses the state of the PUNCH FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6022	PCF	Clear the Flag. Clears the PUNCH FLAG flip-flop.
6024	PPC	Load Punch Buffer Register, punch character. Transfers the AC4—11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.
6026	PLS	Microprogram of 6022 and 6024. Clears the PUNCH FLAG flip-flop, transfers AC4—11 contents to the Punch Buffer Register, punches the character, sets the PUNCH FLAG flip-flop when done.

At the same TP3 time, the tape punch logic is prepared for the punch cycle. When the PUNCH SYNC signal is generated at the start of the punch cycle, the tape punch logic asserts the PUNCH DONE signal. This signal lasts for 10 ms, during which time the punch solenoid drivers are activated and the character is punched onto the tape. At the end of the PUNCH DONE signal, the PUNCH FLAG flip-flop is set. If the punch logic has previously been logically connected to the computer interrupt system, the PUNCH FLAG flip-flop asserts the OMNIBUS INT RQST L signal. The computer enters the interrupt servicing routine to determine the identity of the device. The 6021 instruction in the routine causes the computer to proceed to the PC8-E subroutine to service the interrupt request.

SECTION 4 DETAILED LOGIC

2.1 IOT DECODER LOGIC

Figure 2-2 shows the IOT decoder logic. Table 2-1 lists the PC8-E IOT instructions and a description of each. Bits MD3–8 and I/O PAUSE L are gated to produce signals 601X and 602X representing reader and punch IOTs, respectively. Both signals cause the OMNIBUS INTERNAL I/O signal to be asserted, thereby ensuring that the positive I/O bus interface ignores the IOT instruction.

The 601X signal and bits MD9–11 are applied to the BCD-to-Decimal Decoder, E31 (refer to Appendix A, Volume 1, for details); the decoder provides the reader IOT signals, as illustrated. The 602X signal and bits MD9–11 are applied to decoder E27, which provides punch IOT signals; in addition, the 602X signal causes the ENABLE PUNCH BUFFER L signal to be asserted each time a punch IOT is generated.

2.2 TAPE READ LOGIC

The tape read logic is shown in Figure 2-3. This logic generates control basic timing signals in response to an IOT instruction or a signal from the PC04 FEED switch. Assume that the PC04 Reader motor is stopped (either the reader is between blocks of characters or has just been put on-line).

When the tape is stopped, a character is always directly over the PC04 photoarray. (Refer to Paragraph 4.1 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for a detailed description of the tape-feed operation.) When an IOT instruction (6014, for example) is decoded, the control logic first causes the character to be loaded into the RDR Buffer Register by the RDR DATA STROBE signal. It then generates stepping signals that cause the PC04 Reader Motor to turn.

Refer to Figure 2-3. The 6014 L signal sets the RDR RUN flip-flop. Both the CLOCK PULSE L signal and the RDR MOTOR STOPPING L signal are negated at this time; thus, the RDR ENA flip-flop is set via NAND gate E5 (the clock logic is disabled until the ENABLE signal turns it on; the RDR MOTOR STOPPING L signal applies only when the stepping signals are removed). The ENABLE signal generated by the 0-output of the RDR ENA flip-flop initiates both the clock logic and the reader motor control logic. The clock logic first produces a single CLOCK PULSE that is applied to NAND gate E32 and to the C-input of the RDR ENA flip-flop. Because the flip-flop D-input is high at this time, the flip-flop remains set. The NAND gate must be enabled if an RDR DATA STROBE signal is to be generated. The second high input to this NAND gate is produced by either the $(A \cdot B)$ L signal or the $(\overline{A} \cdot \overline{B})$ L signal (one of these two sync signals, generated by the reader motor control logic, is high when the paper-tape holes are directly over the PC04; assume, for this discussion, that $(A \cdot B)$ L is asserted). The negative pulse from E32 sets the R/S flip-flop. The FEED HOLE signal, produced by the PC04 photoarray, enables the 1-output of the R/S flip-flop to activate E23. The negative-going edge of E23's output resets the R/S flip-flop after a small delay determined by the RC network. Consequently, the RDR DATA STROBE signal generated by NOR gate E35 is a narrow pulse (approximately 100-ns wide) and occurs only when the tape-feed hole is over the photoarray. The RDR DATA STROBE signal resets the RDR RUN flip-flop.

After the RDR DATA STROBE signal is generated, the clock logic produces a SHIFT PULSE that causes the reader motor control logic to generate a stepping signal. The tape holes move from over the photoarray; the FEED HOLE signal and the $(A \cdot B)$ L signal are negated. The D-input of the RDR ENA flip-flop is now low. If a 6014 L is not provided before the clock logic generates another CLOCK PULSE, the RDR ENA flip-flop is cleared, initiating a controlled motor-stopping operation. The clock logic is disabled and the reader motor control logic generates a final stepping signal. The reader motor stops and the tape halts with the holes directly over the photoarray. The FEED HOLE signal is again asserted and now the $(\overline{A} \cdot \overline{B})$ L signal is high. The RDR RUN flip-flop can be set by an IOT instruction any time after the RDR ENA flip-flop is cleared. However, the RDR ENA flip-flop can be set again only after a 40-ms delay (the reader motor control logic asserts RDR MOTOR STOPPING L for 40 ms after the RDR ENA flip-flop is cleared).

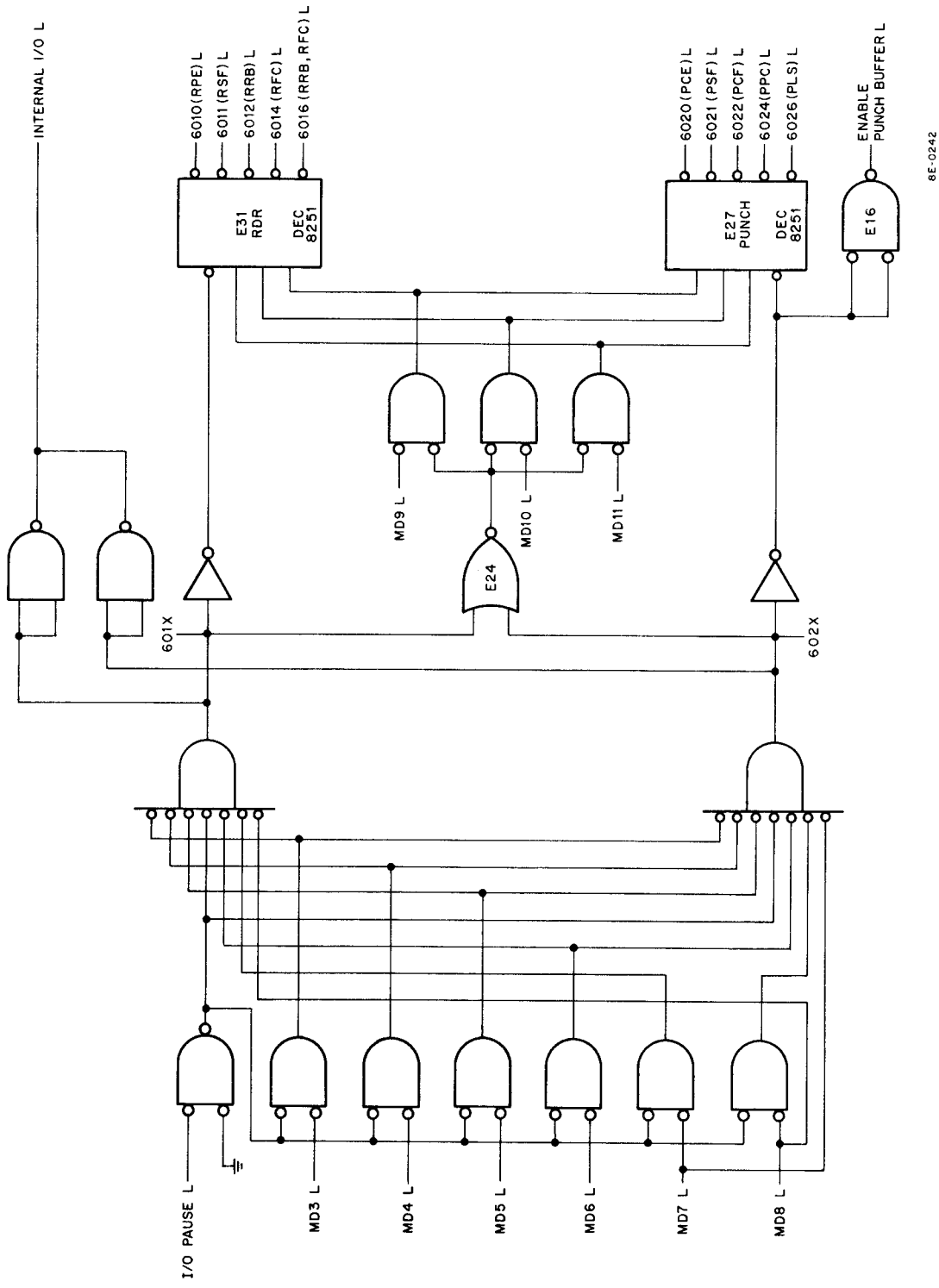

Figure 2-2 IOT Decoder Logic

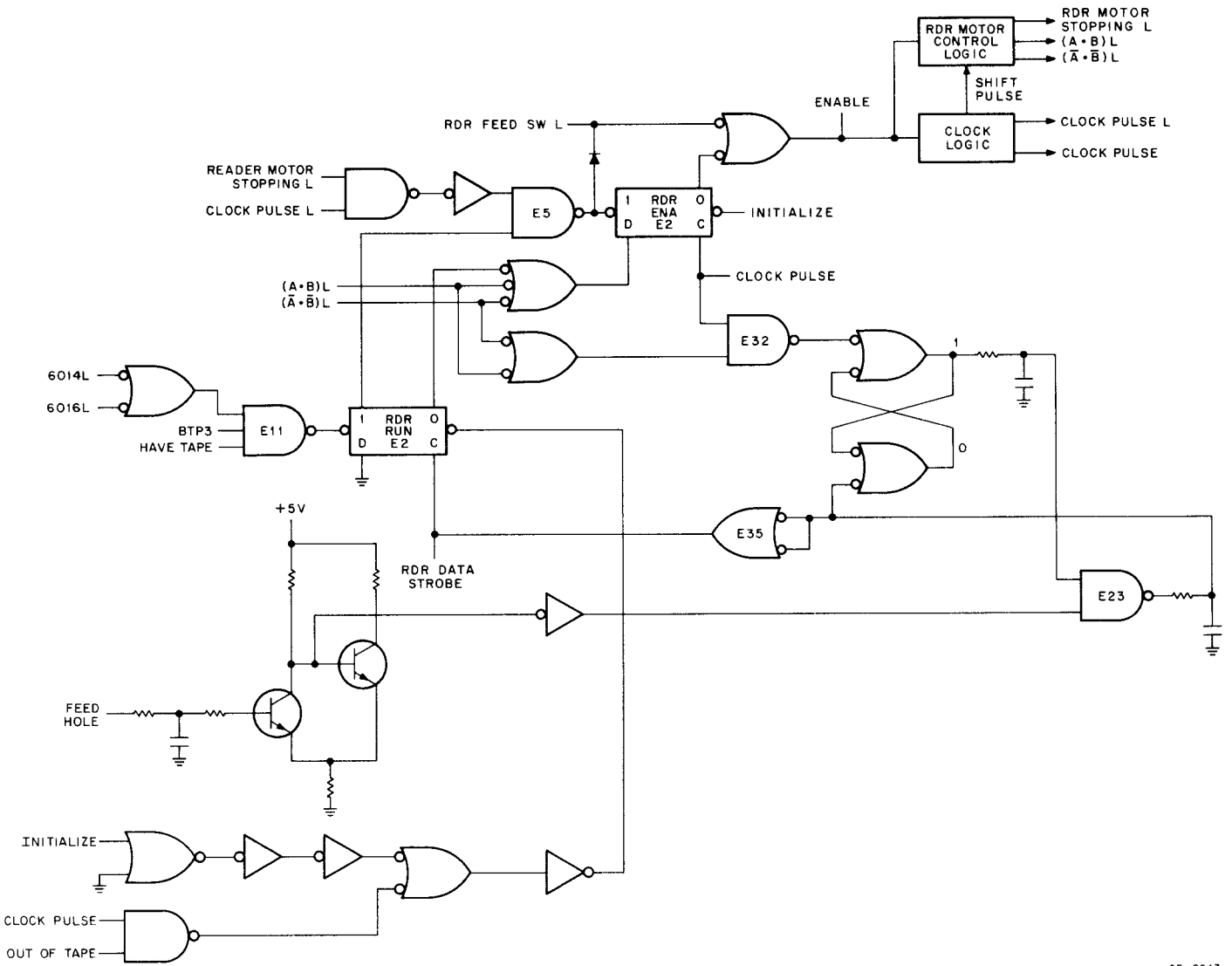

Figure 2-3 Tape Read Logic

If the RDR RUN flip-flop had been set by an IOT instruction before the second CLOCK PULSE occurred, the RDR ENA flip-flop would remain set. The second CLOCK PULSE would then be followed by the second SHIFT PULSE. At this SHIFT PULSE time the $(\overline{A}\cdot\overline{B})$ L and the FEED HOLE signals are asserted. The third CLOCK PULSE causes RDR DATA STROBE to be generated and the RDR RUN flip-flop is again cleared. Thus, a 6014 or 6016 instruction must be decoded at least once for every other clock pulse in order to maintain a 300 character/second rate of operation.

Figure 2-4 is a timing diagram that illustrates the tape read logic signals, as well as those of the reader motor control logic and the clock logic. The first clock period illustrated shows the RDR RUN flip-flop being cleared by an RDR DATA STROBE. A 6014 IOT is decoded before the next CLOCK PULSE. However, between the third and fourth CLOCK PULSES, no IOT is decoded and, therefore, the controlled motor-stopping operation is begun (this is covered fully in Paragraph 2.4).

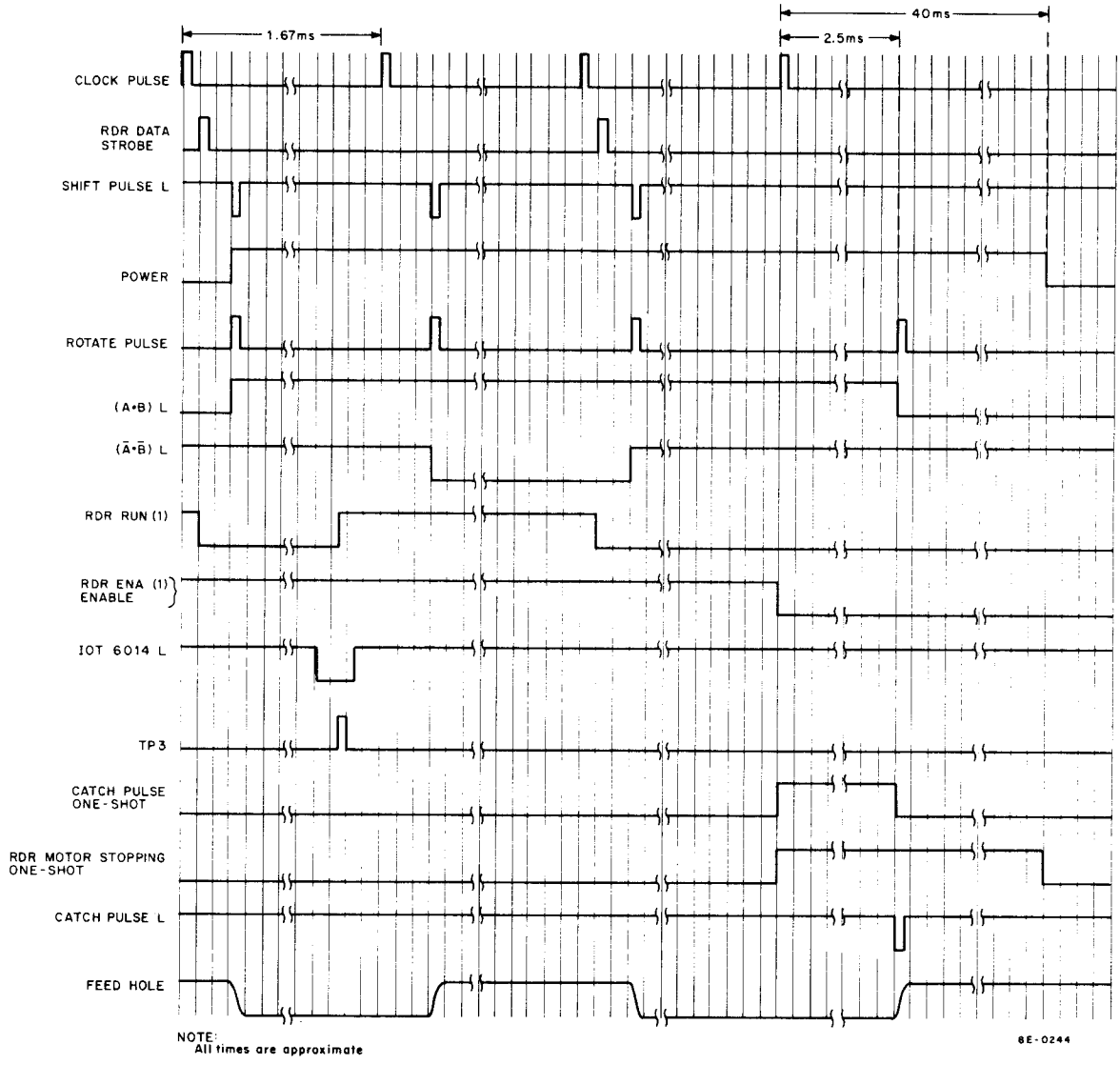

Figure 2-4 Reader Timing

2.3 CLOCK LOGIC

The clock logic is shown in Figure 2-5. The logic consists of a ramp generator, a triggered free-running multivibrator, and two pulse-forming delay networks.

During continuous operation, the reader motor is stepped once every 1.67 ms. However, when the motor must be started from a dead stop, the inertia of the motor and the tape drive wheel must be overcome. Initially, the shaft turns more slowly, and, consequently, the tape moves over the photoarray more slowly than at continuous operating speed. With each step of the motor the speed of the tape approaches continuous operating speed. In order to maintain a nearly constant ratio of tape speed to CLOCK PULSE frequency, the ramp generator, which includes transistors Q1 and Q2, is used.

When the ENABLE signal is asserted by the tape read logic, the free-running multivibrator, Q4/Q5, is triggered on via Q3. At the same time, the ramp generator is triggered. The emitter of Q2 provides the charging potential for the multivibrator. This potential is initially such that the first CLOCK PULSE period is 5 ms. The emitter potential of Q2 rises at a rate determined by the RC time constant, which can be varied by R27 (refer to Paragraph 5.3.8 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for adjustment procedures). As the potential rises, the capacitors in the base circuits of Q4 and Q5 take less time to charge. Thus, the on/off cycle of Q4 and Q5 decreases. Ultimately, when the ramp has ended, the CLOCK PULSE period is 1.67 ms.

The method used to generate the SHIFT PULSE L signal and the CLOCK PULSE signal is illustrated in Figure 2-6. The RC delay circuits are used extensively in the control logic. Because the circuit in Figure 2-5 is more detailed than others, it has been selected as an example of the technique. The timing diagram is mainly self-explanatory. The RC delays indicated can be roughly calculated by using the formula Delay = 0.7 RC.

2.4 READER MOTOR CONTROL LOGIC

The reader motor control logic is shown in Figure 2-7. (Refer to Paragraph 4.1.1 of the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for a detailed description of how the reader motor control logic stepping signals control the reader motor.) When the ENABLE signal is asserted by the tape read logic, the two one-shot multivibrators, E4 and E7, are readied for triggering. During continuous operation, the clock logic generates SHIFT PULSEs, the first of which sets the PWR flip-flop, thereby asserting the POWER signal. Each SHIFT PULSE L signal generates a ROTATE PULSE that clocks the A/B end-around shift register. At every other ROTATE PULSE either the $(A \cdot B)$ L signal or the $(\overline{A} \cdot \overline{B})$ L signal is asserted, indicating to the tape read logic that a character is over the photoarray.

If, as explained in Paragraph 2.2, the RDR ENA flip-flop is cleared, the ENABLE signal is negated (provided the reader FEED switch is not activated). The down-going edge of the ENABLE signal triggers E4 and E7 (Figure 2-4). After 2.6 ms, E4 times out and a CATCH PULSE L signal is generated. This pulse produces the ROTATE PULSE that steps the motor a final time. The motor stops with either $(A \cdot B)$ L or $(\overline{A} \cdot \overline{B})$ L asserted and the FEED HOLE signal high.

The E7 one-shot remains set for 40 ms before timing out. During this 40-ms period, the RDR MOTOR STOPPING L signal is asserted and prevents the RDR ENA flip-flop from being set. At the end of the period, the 0-output of E7 clears the PWR flip-flop, negating the POWER signal. Reader operation can be restarted by again setting the RDR ENA flip-flop.

The 40-ms delay provided by E7 ensures that the motor, if not pulsed for continuous operation, has sufficient time to come to a complete stop before it is activated again. If the complete stop were not allowed, undesirable oscillations in the drive motor would result, causing possible false data outputs.

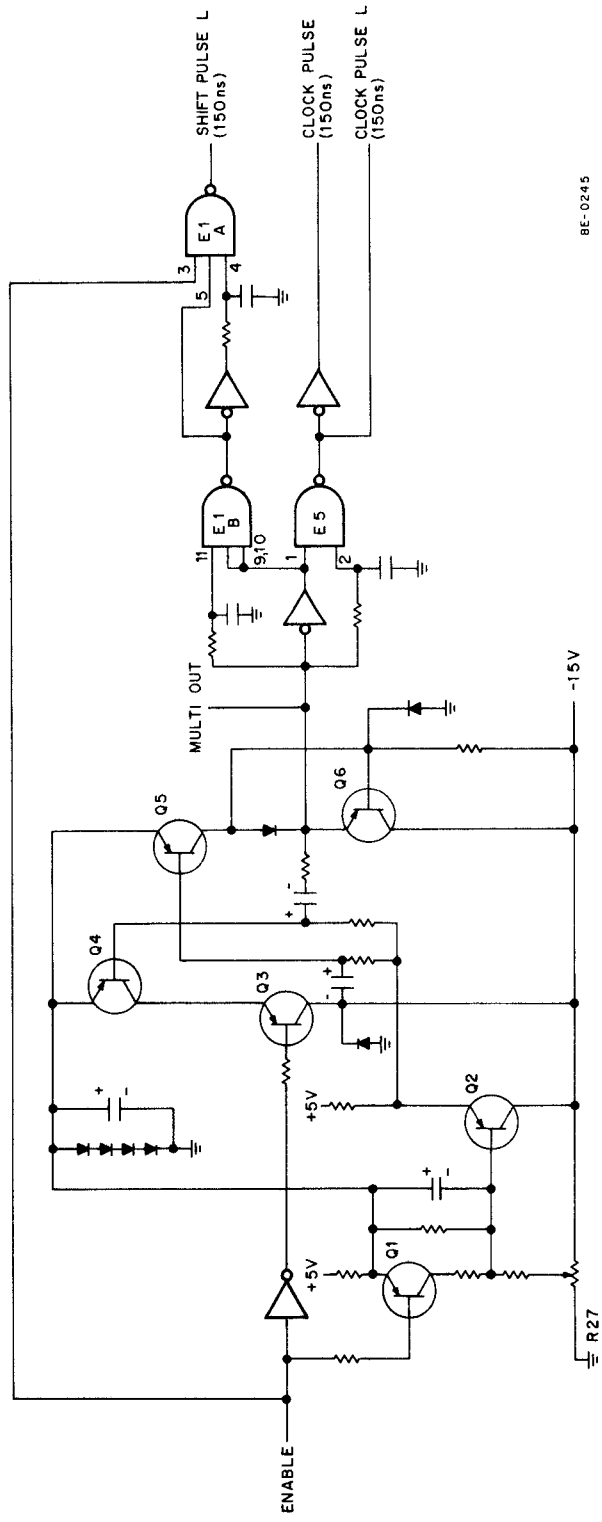

Figure 2-5 Clock Logic

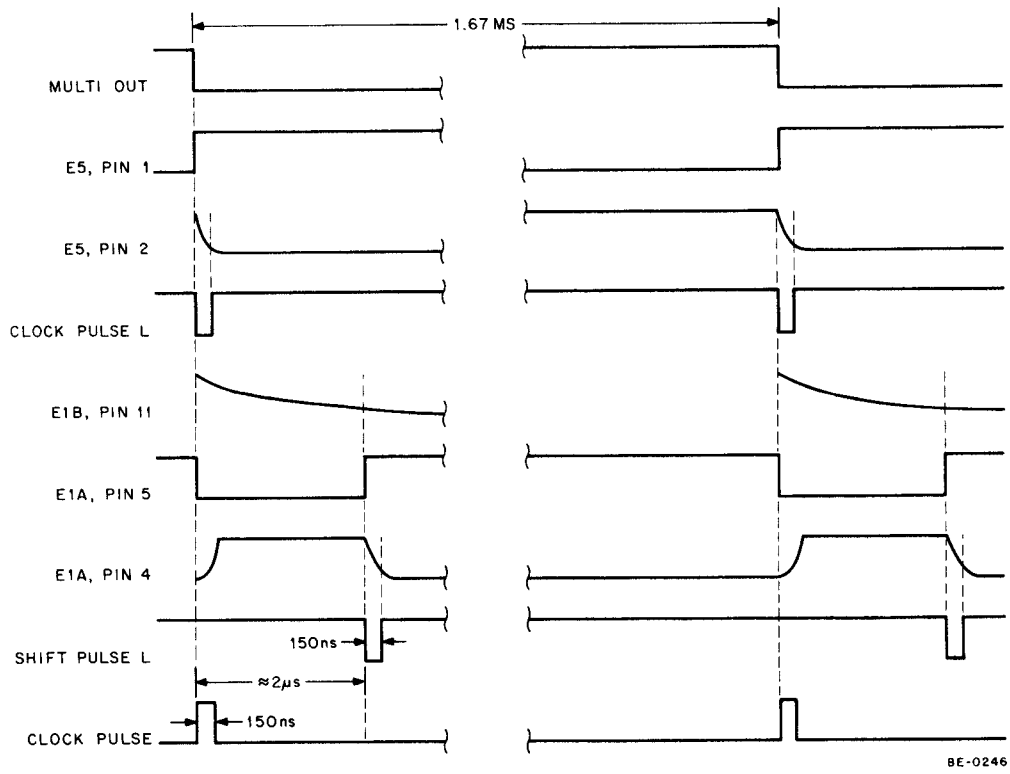

Figure 2-6 Clock/Shift Pulse Timing

2.5 RDR INT/SKIP LOGIC

The RDR INT/skip logic is shown in Figure 2-8. When an RDR DATA STROBE signal is generated it sets the RDR FLAG flip-flop (the RDR RUN flip-flop provides the necessary high at E12's D-input before being cleared, itself, by RDR DATA STROBE). Because RDR DATA STROBE also loads the RDR Buffer Register, the RDR FLAG flip-flop being set indicates that the control is ready to transfer data. If the INT ENA flip-flop has been set previously, either under program control or by INITIALIZE, the OMNIBUS INT RQST L signal is asserted. When the computer enters the PC8-E servicing subroutine, an appropriate IOT instruction reads the Buffer Register and clears the RDR FLAG flip-flop via NOR gate E1.

2.6 RDR BUFFER LOGIC

The reader buffer logic is shown in Figure 2-9. Data supplied on the READ HOLE 1–8 lines is clocked into the register by the RDR DATA STROBE signal. Either 6012 L or 6016 L gates the character onto the OMNIBUS DATA 4–11 lines. At the same time, the IOT instruction asserts the OMNIBUS C1 L signal, resulting in an ORing of the DATA 4–11 bits and the CPU AC Register contents.

2.7 TAPE STATUS LOGIC

The tape status logic is shown in Figure 2-10. The logic monitors both the FEED HOLE signal and the RDR ENA flip-flop, generating an OUT OF TAPE signal when tape is not loaded in the PC04 Tape Feeder. This signal ensures that the tape read logic cannot be triggered by a program instruction read command. The complementary signal, HAVE TAPE, is generated when tape is in the feeder, enabling the tape-feed operation to begin when program-directed.

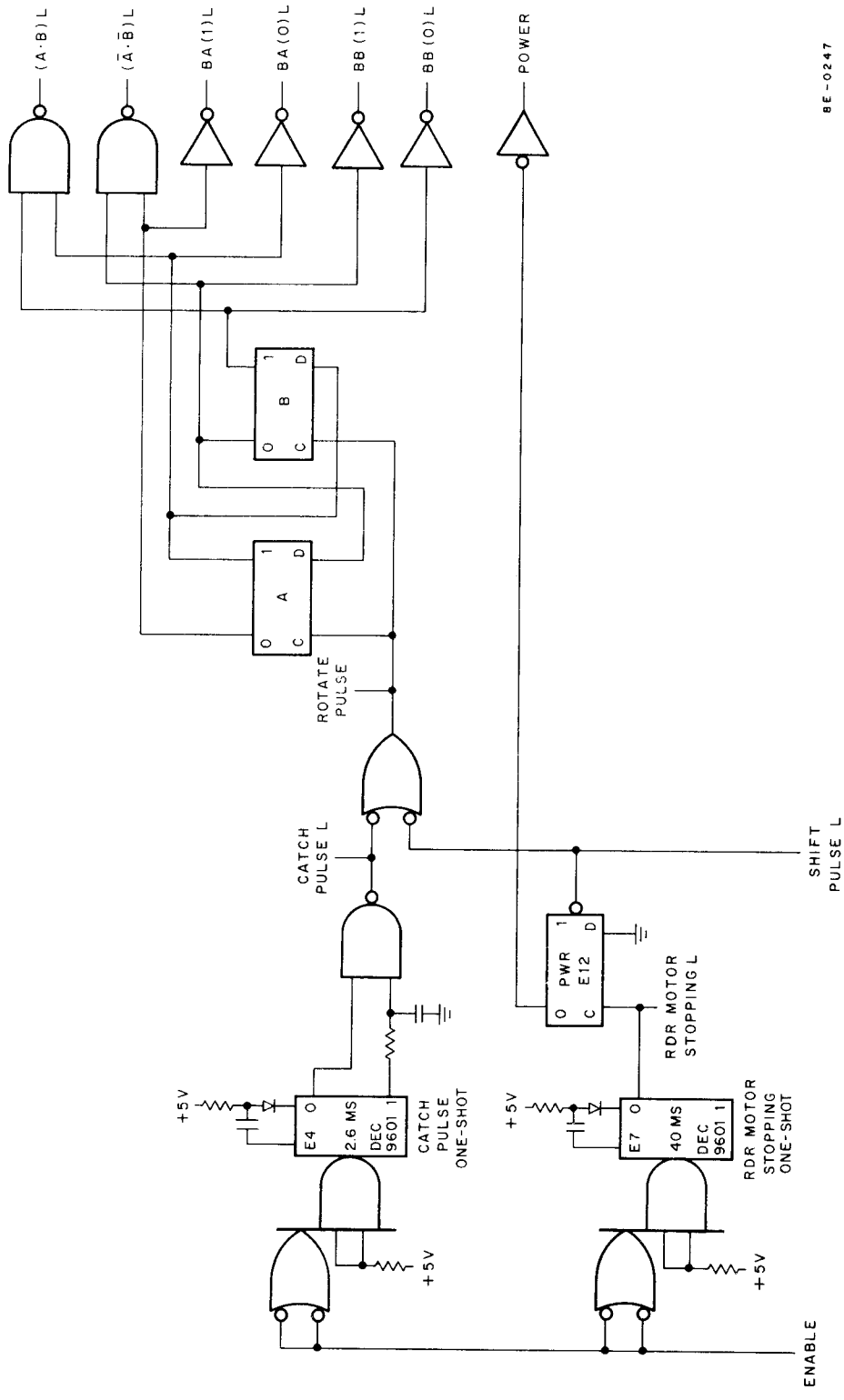

Figure 2-7 Reader Motor Control Logic

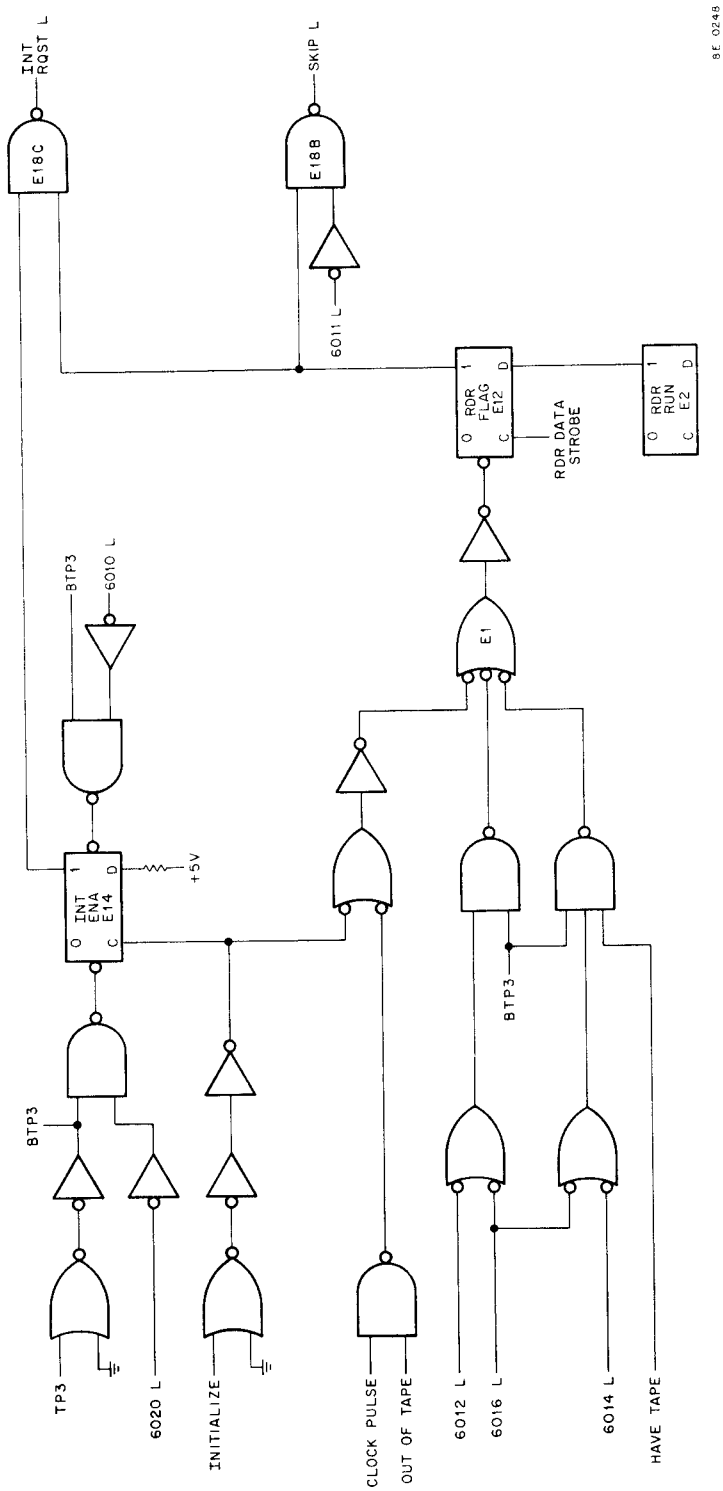

Figure 2-8 RDR INT/Skip Logic

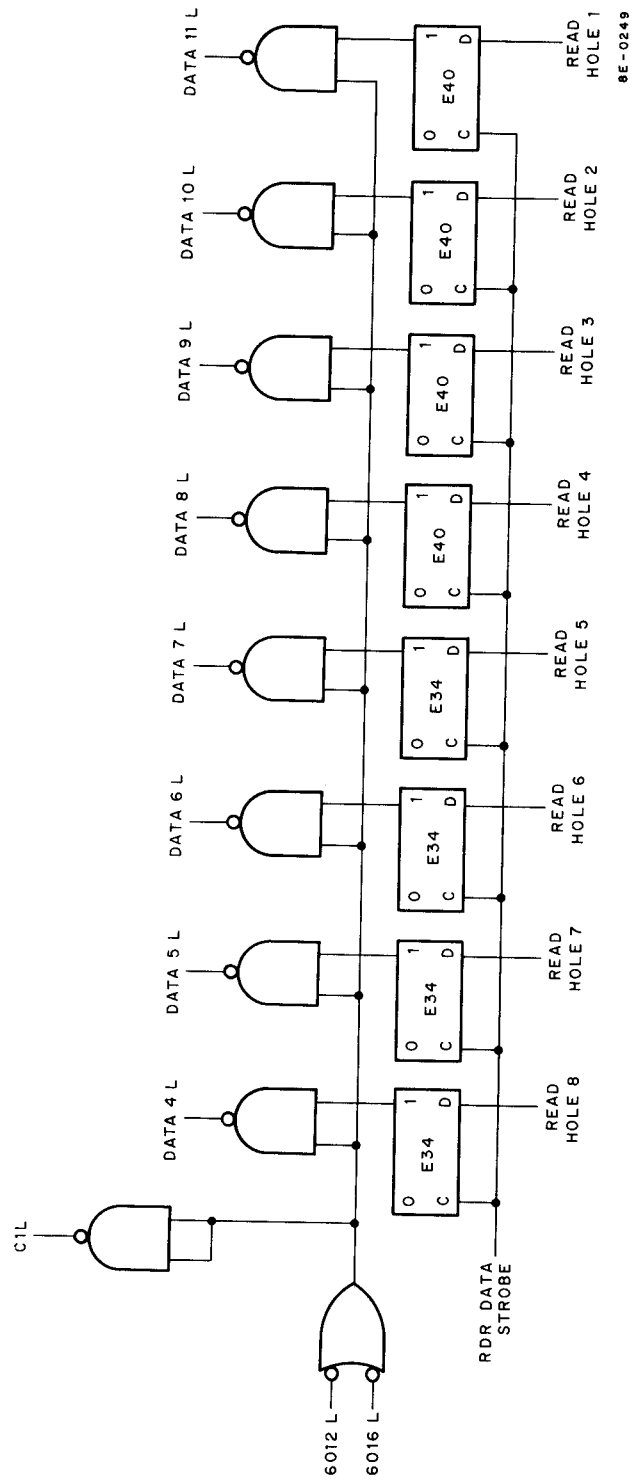

Figure 2-9 Reader Buffer Logic

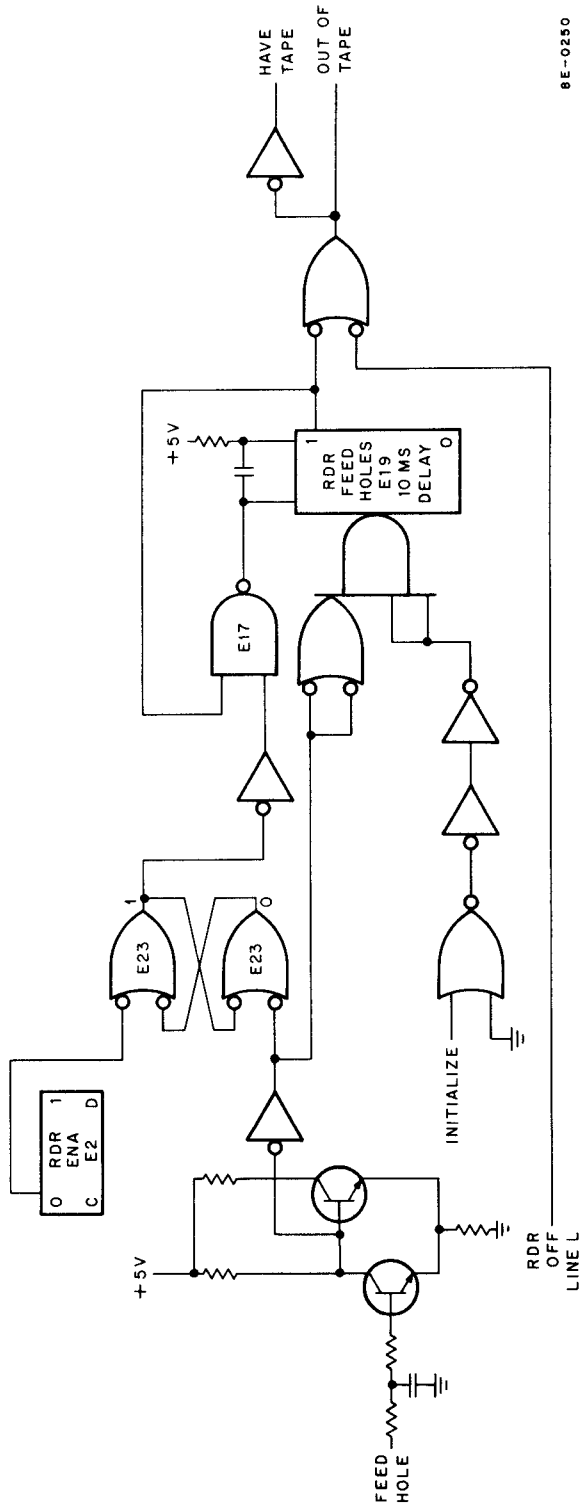

Figure 2-10 Tape Status Logic

If no tape has been inserted in the feeder, the FEED HOLE signal is high, just as it is when an actual feed hole is detected by the photoarray. The RDR FEED HOLES one-shot, E19, is in its stable state; thus, the OUT OF TAPE signal is asserted. If a read command is issued by the program, the RDR RUN flip-flop (Figure 2-3) is prevented from being set by the HAVE TAPE signal that is low at this time. Therefore, the RDR ENA flip-flop is not set and the clock logic is not triggered.

When a tape is inserted in the feeder, the photoarray light source rays are interrupted briefly by the tape web. The FEED HOLE signal goes low, and the negative-going edge causes one-shot E19 to be triggered; thus, the HAVE TAPE signal is asserted. At the same time that E19 is triggered, the flip-flop consisting of the cross-coupled NOR gates is cleared. Because the RDR ENA flip-flop is also clear, flip-flop E23 is latched in the clear state. NAND gate E17 is enabled; the resulting low at pin 11 of E19 holds the one-shot in the triggered state, i.e., the 1-output stays high. The HAVE TAPE signal remains high indefinitely, if the program does not issue a read command.

When a read command is issued, the RDR RUN flip-flop is set, causing the RDR ENA flip-flop to be set, also. The 0-output of the RDR ENA flip-flop triggers the clock logic, which generates a CLOCK PULSE, and sets flip-flop E23, which disables NAND gate E17. The one-shot enters the timeout state, during which it can be re-triggered by each trailing edge of the FEED HOLE signal. A ROTATE PULSE, generated by the clock logic approximately 2 μs after the CLOCK PULSE (Figure 2-4), causes the tape to begin feeding through the read station. The resulting negative transition of the FEED HOLE signal re-triggers the one-shot (note that flip-flop E23 is held in the set state by the 0-output of the RDR ENA flip-flop). If another trailing edge occurs within 10 ms, the one-shot is again re-triggered (a 10-ms period is necessary because the reader motor is being started from a dead stop and, consequently, the tape moves more slowly than at continuous operating speed; in continuous operation, a trailing edge occurs at 3.34-ms intervals). If the program issues read commands at such a rate that continuous operation results (at least one command between each RDR DATA STROBE and the next CLOCK PULSE), one-shot E19 is re-triggered continuously, and the HAVE TAPE signal remains asserted.

Suppose that at some point during this continuous operation a read command is not issued within approximately 3.34 ms of the preceding command. In such a situation, the motor-stopping operation is initiated. At the moment this operation begins, the RDR ENA flip-flop is cleared, and the FEED HOLE signal is low. Therefore, flip-flop E23 is again latched in the clear state, and one-shot E19 is held in its triggered state. The HAVE TAPE signal remains high while the motor is stopped.

If read commands are issued at a continuous rate and the tape runs out of the tape feeder, the OUT OF TAPE signal must be asserted. When the last portion of tape web uncovers the light source, the FEED HOLE signal goes high and remains high. One-shot E19 times out approximately 8.5-ms later, and the OUT OF TAPE signal goes high. During this 8.5-ms period, three RDR DATA STROBE pulses occur. Each of these pulses loads the Reader Buffer with 1s. Consequently, at least two transfers, possibly three, of 1s to the AC Register take place before the RDR RUN flip-flop is cleared and the clock logic is disabled.

2.8 TAPE PUNCH LOGIC

When the punch ON/OFF switch is in the ON position, the punch motor runs continuously. A tape that is loaded in the punch feeder mechanism can be punched if the FEED switch is in the FEED position, or if the program issues a punch command IOT instruction, 6024 or 6026. Either method results in the PUNCH DONE signal being generated in the tape punch logic (Figure 2-11).

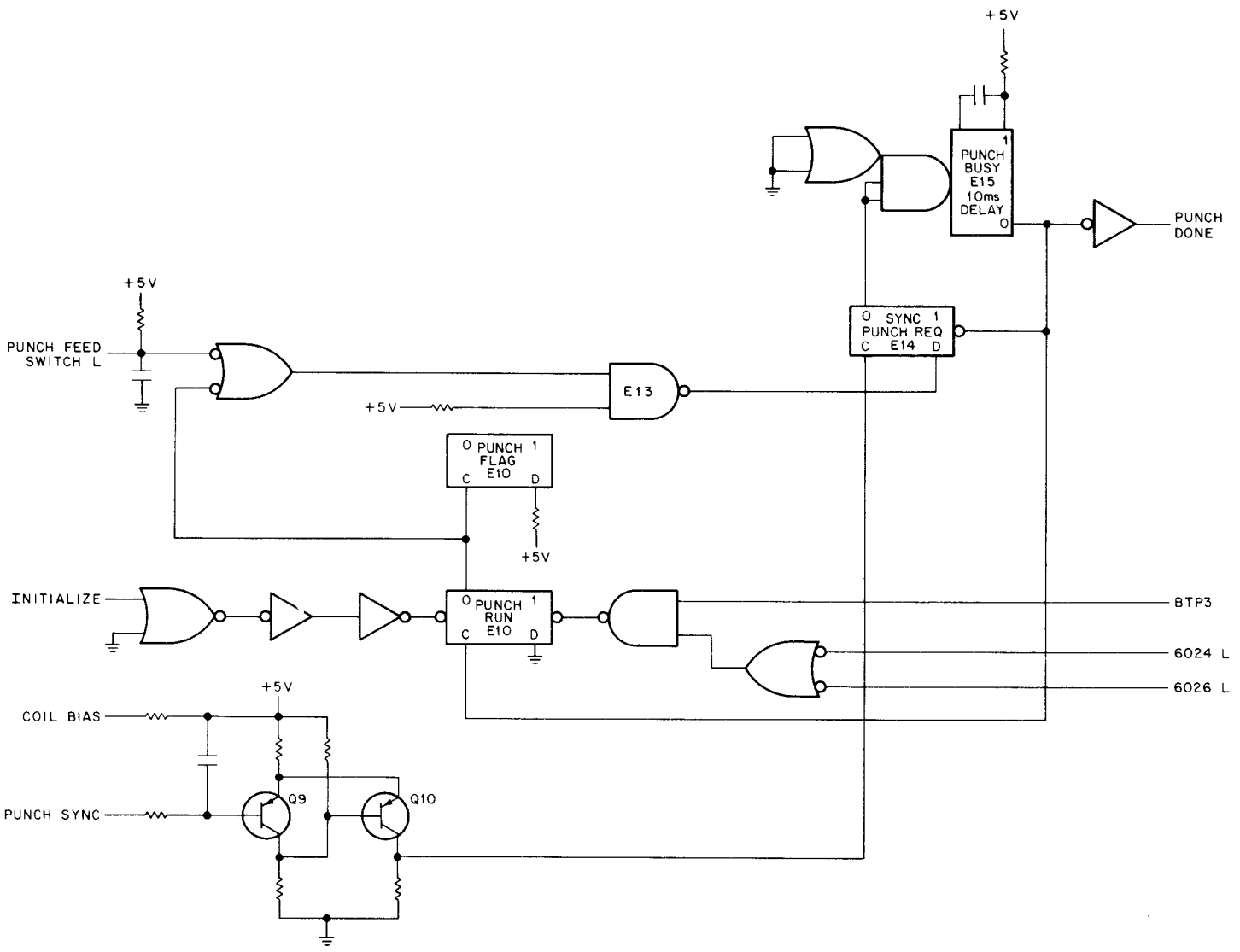

Figure 2-11 Tape Punch Logic

When the 6026 IOT instruction is issued, for example, the PUNCH RUN flip-flop, E10, is set. Setting E10 causes the D-input of the SYNC PUNCH REQ flip-flop, E14, to go low. A PUNCH SYNC signal from the tape punch mechanism can clear E14, thereby triggering the PUNCH BUSY one-shot, E15. This PUNCH SYNC signal occurs once during each punch motor revolution and signals the start of the punch mechanical cycle. The signal is applied to the Schmitt trigger, Q9 and Q10, and the output at the collector of Q10 clears E14. The resulting 10-ms PUNCH DONE signal enables the PC04 solenoid drivers to activate the punch mechanism. The tape is punched with the character that was placed on the HOLE 1–8 lines by the punch buffer logic, shown in Figure 2-12 and discussed briefly in Paragraph 2.9.

2.9 PUNCH BUFFER LOGIC

The punch buffer logic is shown in Figure 2-12. Either the 6024 L signal or the 6026 L signal enables the Buffer Register to be loaded at TP3 time with the information carried on the DATA 4–11 lines. This information is then gated to the HOLE 1–8 lines, respectively. Note that the information loaded at this time remains in the register until another punch instruction is issued or until the FEED switch is activated.

2.10 INT/SKIP LOGIC

After the tape has been punched and the punch mechanical cycle ends, the PUNCH BUSY one-shot times out. The PUNCH RUN flip-flop is cleared and the 0-output of the flip-flop sets the PUNCH FLAG flip-flop (Figure 2-13). If the INT ENA flip-flop, E14, is set at this time, the OMNIBUS INT RQST L signal is asserted. The computer enters the interrupt routine and proceeds from there to the punch subroutine.

SECTION 5 MAINTENANCE

Refer to Volume 1 and the *PC04 High-Speed Perforated Paper-Tape Reader/Punch Maintenance Manual* for PC8-E maintenance information.

Table 2-2 presents cable and connector pin assignments for the two cables that connect the control and the PC04.

SECTION 6 SPARE PARTS

Table 2-3 lists recommended spare parts for the PC8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

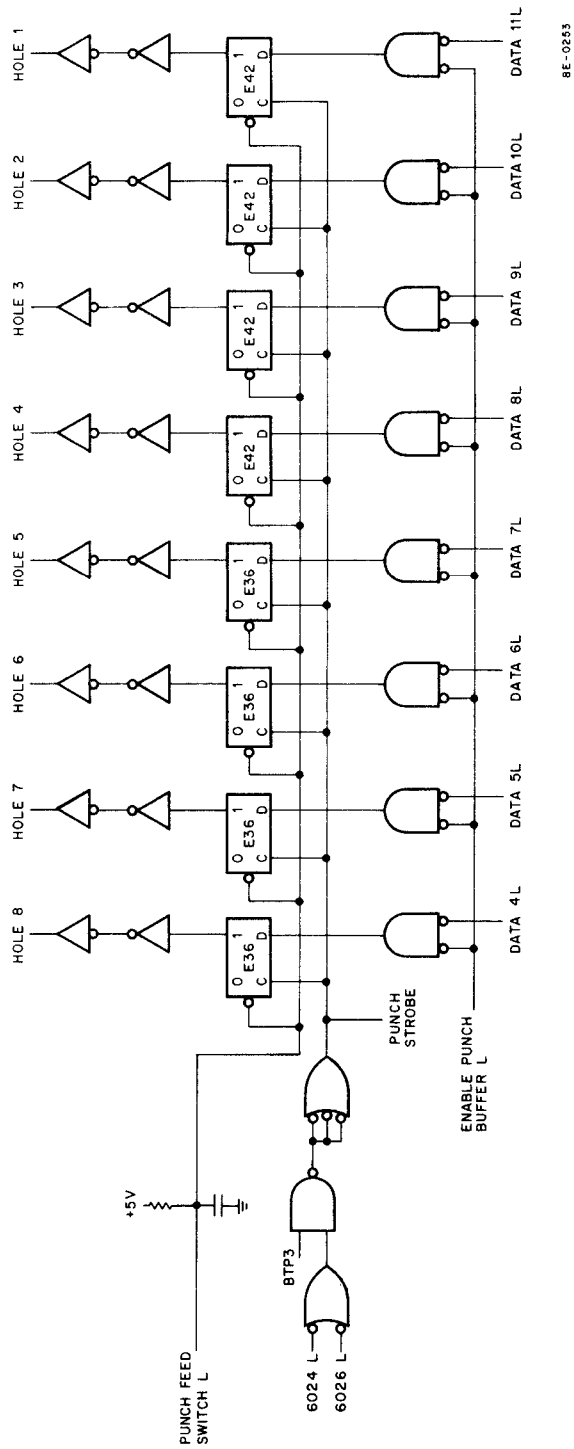

Figure 2-12 Punch Buffer Logic

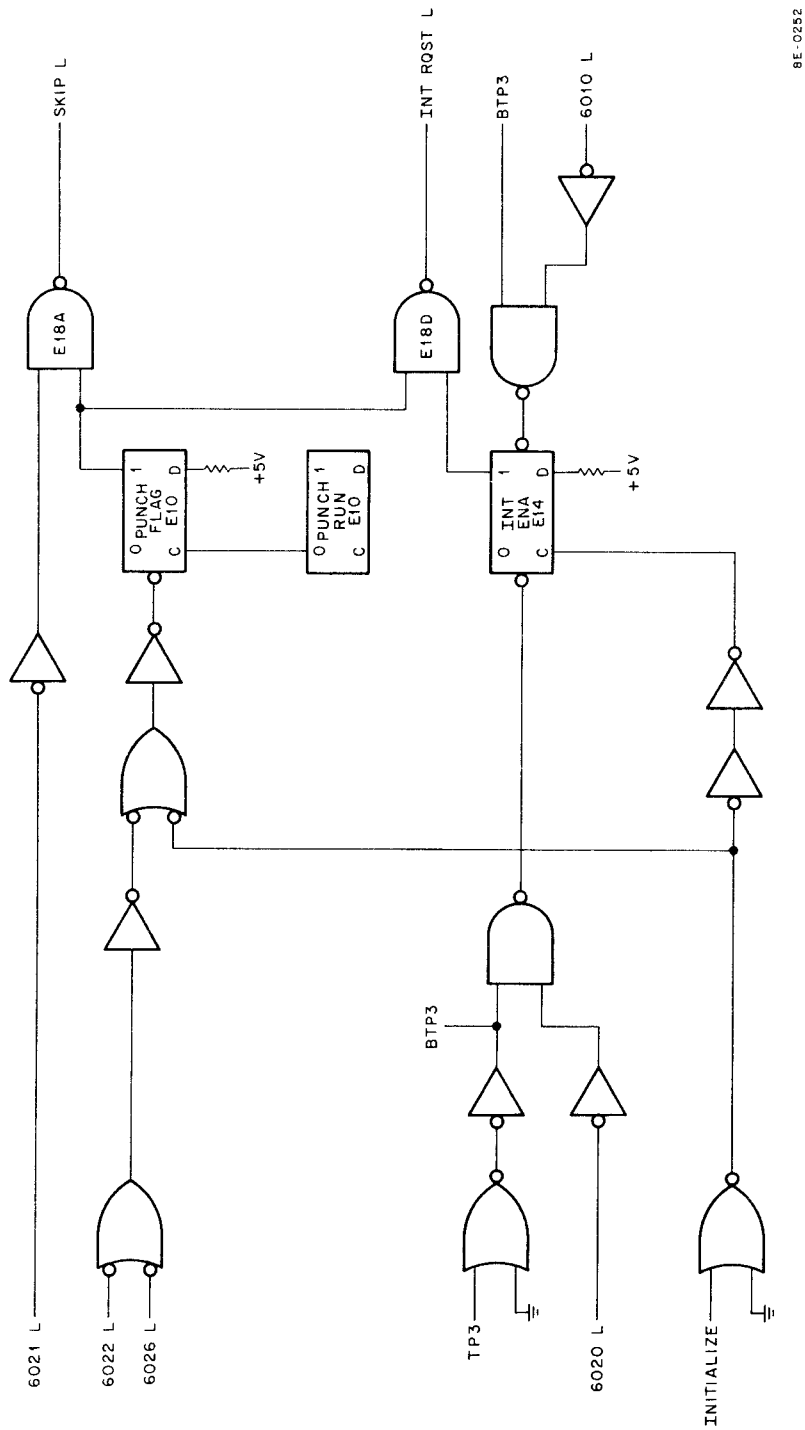

Figure 2-13 Punch INT/Skip Logic

Table 2-2
Cable/Connector Pin Assignments

Control Connector Pin	Signal Name		M955 Connector Pin
	J1 (Connects to B1)	J2 (Connects to A1)	
D	PUNCH FEED SWITCH	N/C	A
F	SCR ACTIVE	RDR ON/OFF LINE	B
J	PUNCH SYNC	GND	C
L	N/C	READ HOLE 1	D
N	PUNCH DONE	READ HOLE 2	E
R	PUNCH NOT UP TO SPEED	READ HOLE 3	F
T	HOLE 8	READ HOLE 4	H
V	HOLE 7	READ HOLE 5	J
X	HOLE 6	READ HOLE 6	K
Z	HOLE 5	READ HOLE 7	L
BB	COIL BIAS	READ HOLE 8	M
DD	HOLE 4	FEED HOLE	M
FF	HOLE 3	BA (0)	P
JJ	HOLE 2	BA (1)	R
LL	HOLE 1	BB (0)	S
NN	N/C	BB (1)	T
RR	N/C	POWER	U
TT	N/C	RDR FEED SWITCH	V
GND PINS A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, SS, UU, VV			

Table 2-3
PC8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	2
19-05576	IC DEC 7410	1
19-09486	IC DEC 384	1
19-09487	IC DEC 9601	1
19-09686	IC DEC 7404	2
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1
19-09973	IC DEC 97401	1
19-09594	IC DEC 8251	1
19-05579	IC DEC 7440	1
19-10087	IC DEC MC4015P	1
15-03409	Transistor, 6543 D	1
15-09338	Transistor, PMS 6531	1
11-00113	Diode, D662	1
11-00114	Diode, D664	2
10-01610	Capacitor, 0.01 μF, 100V, 20%	2

PART 3
X/Y PLOTTER

CHAPTER 3
XY8-E PLOTTER CONTROL

SECTION 1 INTRODUCTION

The XY8-E Plotter Control interfaces a digital incremental plotter with the PDP-8/E. The XY8-E operates with a variety of plotters, both encoded and unencoded types, to display data on paper or film. All XY8-E logic is contained on a single quad module that plugs into the OMNIBUS. The XY8-E connects to the incremental plotter with a signal cable that is supplied.

The XY8-E transmits directions to the plotter that originate in the computer AC Register. Data is transferred in six parallel bits that cause pen or drum movement (the plotter can be either a drum or flatbed type) in the plotter. All plotter operations, except the setting of the coordinates at which plotting begins, are guided by the XY8-E logic and the CPU. A series of functions, specified by IOT instructions, initialize the XY8-E logic, initiate plotter operation, and generate program interrupts to indicate completion of the operation.

The XY8-E will interface readily with any of the following incremental plotters:

a. CalComp Plotters — Series 500, 600, 700, and 800.
b. Houston Instruments Plotters — Types 6400, DP-1, and DP-10.

Four Plotter Control/plotter systems, featuring plotters from those listed, are offered by DEC. Details concerning installation, operation, troubleshooting, and maintenance of these plotters can be found in the respective CalComp or Houston Instruments instruction manual. DEC publications and documents relevant to the XY8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. XY8-E Plotter Control and Display Diagnostic, MAINDEC-8E-D6AB
d. DEC Engineering Drawing, Plotter Control, E-CS-M842-0-1.

SECTION 2 INSTALLATION

The XY8-E Plotter Control is installed on site by DEC Field Service personnel. Customers should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the XY8-E Control Module in the PDP-8/E OMNIBUS. Refer to Table 2-3, Volume 1, for information concerning recommended module priorities (the XY8-E is a "non-memory" option).

Connect the Plotter Control to the plotter with the signal cable provided (if the plotter is one of those listed in Section 1). If the plotter is an unencoded type, J2 of the Plotter Control, a 40-pin Berg Connector, connects to the plotter 19-pin Cannon Plug; if the plotter is an encoded type, J1 of the Plotter Control connects to the plotter Cannon Plug (refer to Section 5 for cable and connector pin assignments).

The XY8-E can be checked for correct operation by running the diagnostic program, MAINDEC-8E-D6AB. Refer to the plotter instruction manual for checkout procedures for the plotter itself.

SECTION 3 BLOCK DIAGRAM

Figure 3-1 is a block diagram of the XY8-E Plotter Control. Programmed IOT instructions are decoded by the IOT decoder logic. Signals representing the IOT instructions are then applied to the timing logic, the interrupt/skip logic, and the direction transfer logic.

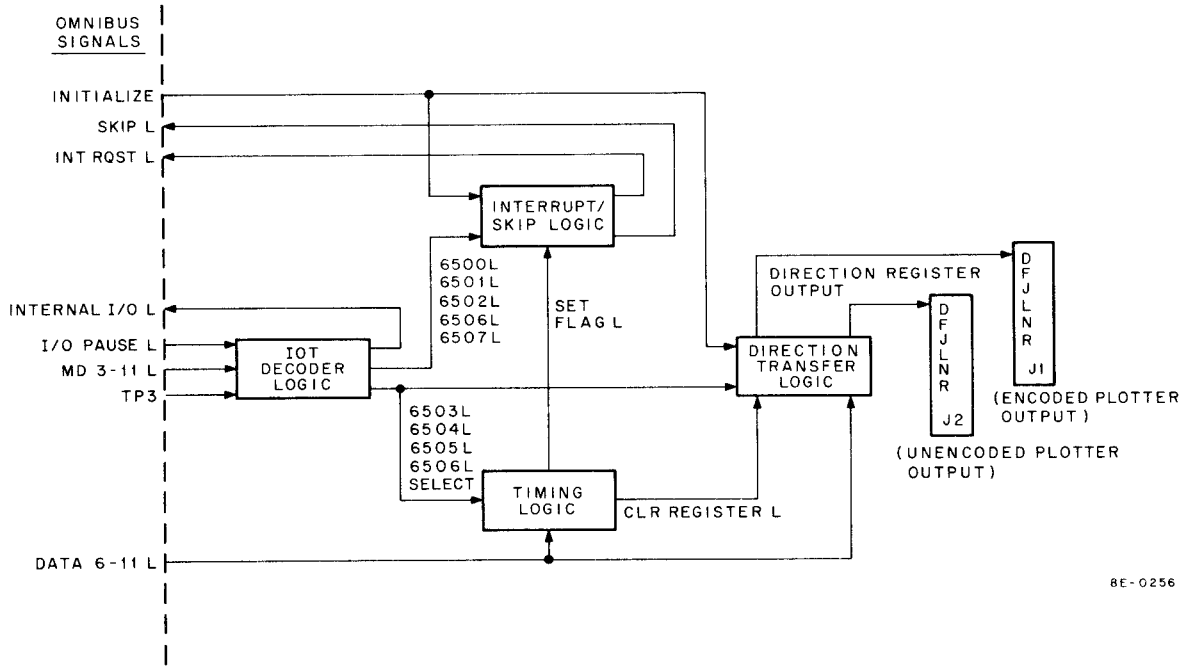

Figure 3-1 XY8-E Block Diagram

Plotter directions are gated from the AC Register via the DATA 6–11 lines to a 6-bit Decision Register in the direction transfer logic. The Direction Register outputs are transferred to the plotter, which begins the directed operation. At the same time, the timing logic is triggered; after a delay period the timing logic generates a signal, CLR REGISTER L, that clears the Direction Register, readying it for the next direction. After a further delay period that ensures completion of the direction by the plotter, the timing logic generates the SET FLAG L signal. This signal is applied to the interrupt/skip logic where it sets the PLOTTER FLAG flip-flop. This action causes the Plotter Control to request a program interrupt, resulting in the transfer of another direction from the AC Register.

SECTION 4 DETAILED LOGIC

3.1 IOT DECODER LOGIC

The IOT decoder logic is shown in Figure 3-2. The I/O PAUSE L signal gates bits MD3—8 to generate the SELECT signal that indicates an XY8-E instruction has been decoded. See Table 3-1 for the XY8-E instruction list and a description of each instruction.

Table 3-1
XY8-E IOT Instruction List

Octal Code	Mnemonic	Function
6500	PLCE	Clear the INT ENA flip-flop.
6501	PLSF	Skip on the Plotter flag. Senses the state of the PLOTTER FLAG flip-flop. If the flip-flop is set, the program counter is incremented so that the next sequential instruction is skipped.
6502	PLCF	Clear the PLOTTER FLAG flip-flop.
6503	PLPU	Pen up. Raises the plotter pen from the surface of the graph paper (unencoded plotters only).
6504	PLLR	Load Direction Register, clear Direction Register, set Plotter flag. Loads the Direction Register from AC06—11 (see Table 3-2 for the list of directions), clears the register after the plotter has had enough time to carry out the direction, sets the PLOTTER FLAG flip-flop.
6505	PLPD	Pen down. Lowers the pen to the surface of the graph paper (unencoded plotters only).
6506	PLCF, PLLR	Microprogram of 6502 and 6504. Clears the PLOTTER FLAG flip-flop, loads the Direction Register, clears the Direction Register, sets the PLOTTER FLAG flip-flop.
6507	PLSE	Set the INT ENA flip-flop.

The SELECT signal asserts the OMNIBUS INTERNAL I/O L signal that directs the positive I/O bus interface to ignore the IOT instruction; also, it gates bits MD9—11 to provide inputs for E21, the BCD-to-decimal decoder (see Appendix A, Volume 1, for details). With one exception, E21 provides the signals that represent the XY8-E IOT commands. The exception is the signal that represents the 6501 instruction, Skip on the Plotter Flag. Note that the IOT signals generated by E21 are produced at TP3 time. However, the OMNIBUS SKIP L signal is sampled at TP3 time by the CPU skip logic. Therefore, the XY8-E Plotter Control must assert the SKIP L signal before TP3 time; this is the reason for generating the 6501 L signal separately.

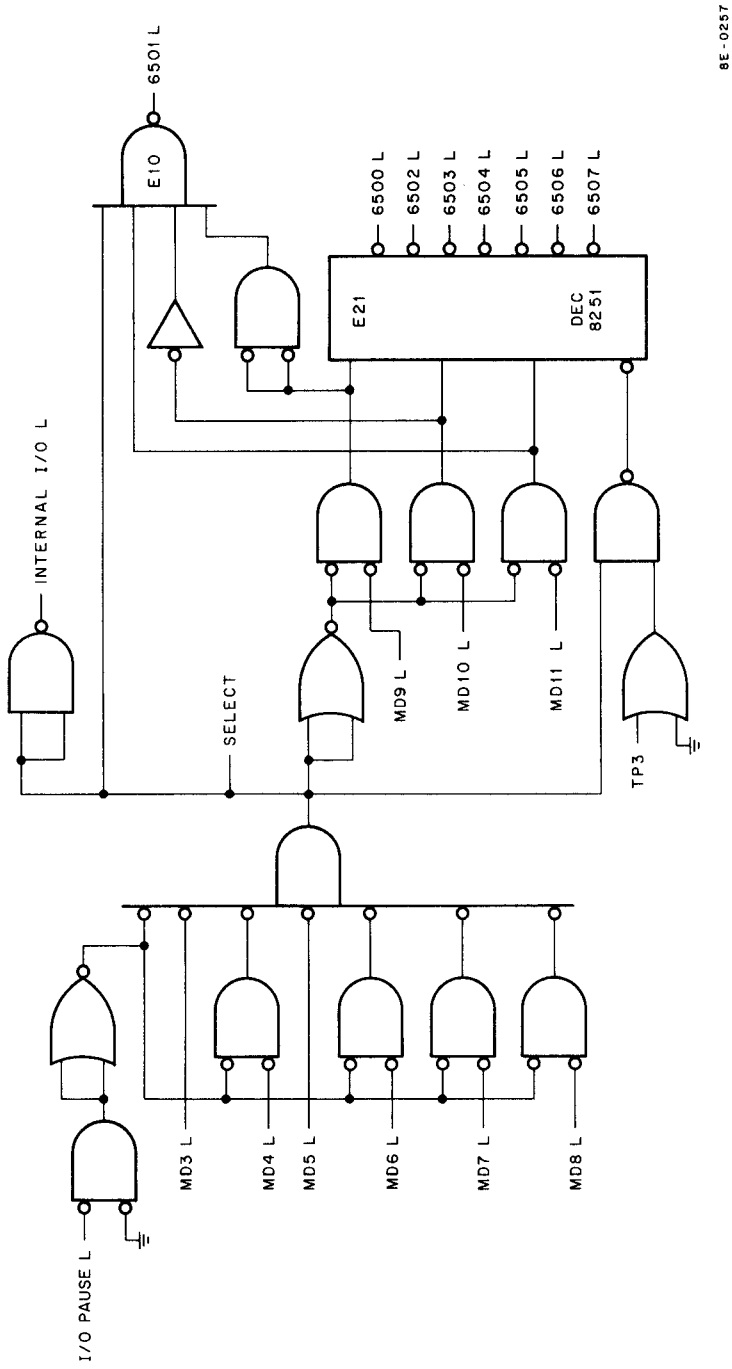

Figure 3-2 IOT Decoder Logic

3.2 TIMING LOGIC

The timing logic is shown in Figure 3-3. This logic generates delay periods that allow the plotter to carry out the direction contained in the Direction Register. The delay periods are initiated simultaneously with the loading of the Direction Register. When the first delay ends, the Direction Register is cleared; when the second delay ends, the PLOTTER FLAG flip-flop is set. Then, if the XY8-E is logically connected to the computer interrupt system, a program interrupt is requested and another direction is transferred from the AC Register to the Direction Register.

Three one-shot multivibrators are shown in Figure 3-3. For directions other than Pen Up/Pen Down, only one-shots E1 and E7 are triggered. Either the 6504 L or the 6506 L signal, in addition to clocking the Direction Register, triggers both E1 and E7. The plotter begins the directed operation and the direction remains in the Direction Register for 3.3 ms (an arbitrary but optimal period of time). At this time, E1 times out and the CLR REGISTER L signal is asserted. This signal is applied to the direction transfer logic and clears the Direction Register. E7 times out after 7.5 ms (more than enough time for the plotter to carry out the mechanical operation), causing the SET FLAG L signal to be asserted. This signal is applied to the interrupt/skip logic, Figure 3-6, where it sets the PLOTTER FLAG flip-flop.

If the direction to be carried out by the plotter is either Pen Up or Pen Down, the third one-shot, E4, is triggered. This situation is illustrated by the timing diagram, Figure 3-4. The timing shown applies to an encoded plotter. However, an unencoded plotter could be represented by replacing the 6504 L/6506 L signal with either 6503 L or 6505 L. If the Pen Up direction is to be carried out by an encoded plotter, for example, AC Register bits 6–11 must be loaded with octal code 31 (Table 3-2). This code is placed on the DATA 6–11 lines and loaded into the Direction Register by the leading edge of the 6504 L/6506 L signal. At the same time, NAND gate E3A, Figure 3-3, is enabled, and both E1 and E7 are triggered. DR11 is set, enabling NOR gate E3B to trigger one-shot E4. As before, the CLR REGISTER L signal is asserted after 3.3 ms. However, the SET FLAG L signal, rather than occurring after 7.5 ms, is delayed for 72.7 ms. This period of time is required to satisfy the plotter's pen stabilizing time. Note that one-shot E7 is superfluous in this operation.

If the Pen Up instruction, 6503, is issued for an unencoded plotter, E4 is triggered in essentially the same way as for the encoded plotter. The 6503 L signal dc-sets DR11. NOR gate E3 is enabled, triggering E4 which, in turn, triggers E1 (E7 is not triggered in this situation). The two delays generated carry out their respective functions as detailed earlier.

3.3 DIRECTION TRANSFER LOGIC

The direction transfer logic is shown in Figure 3-5. Directions are placed on the DATA 6–11 lines from the AC Register by IOT instruction 6504 or 6506. At TP3 time, the 6504 L signal or the 6506 L signal loads the Direction Register. Separate transistor driver outputs are provided for encoded and unencoded plotters; unencoded outputs undergo a transition from -15V to +5V, while encoded outputs go from ground to +15V. The Direction Register is cleared by the INITIALIZE signal that is asserted both at power turn-on and by the CAF (6007) instruction.

3.4 INTERRUPT/SKIP LOGIC

The interrupt/skip logic is shown in Figure 3-6. The Plotter Control is logically connected to the computer interrupt system when the INT ENA flip-flop is set. The flip-flop is set under program control by the 6507 (PLSE) IOT instruction or by the 6007 (CAF) IOT instruction that asserts the INITIALIZE signal; in addition, the INITIALIZE signal sets the flip-flop at power turn-on. The XY8-E is disconnected from the interrupt system by the 6500 (PLCE) IOT instruction that clears the flip-flop under program control.

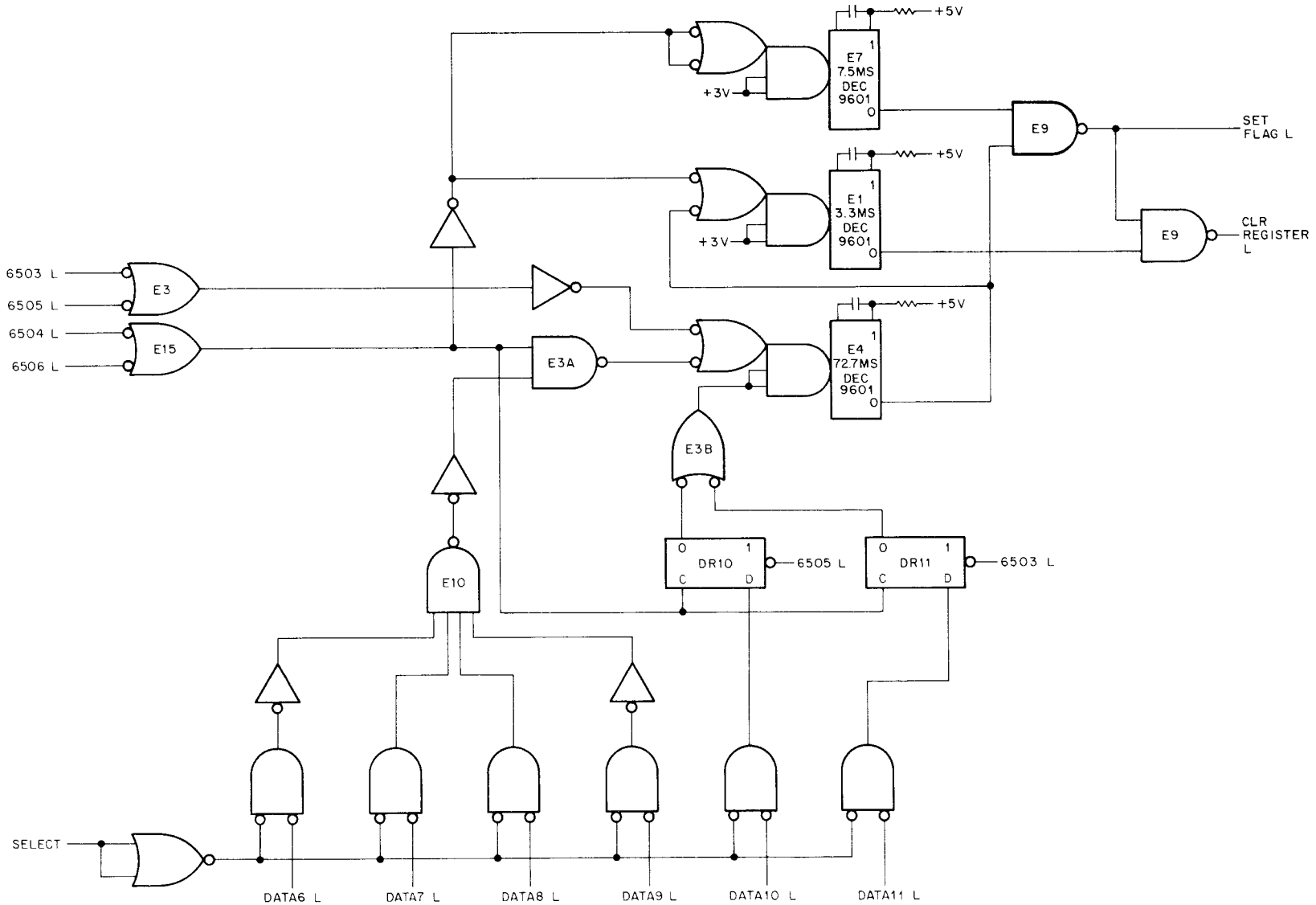

Figure 3-3 Timing Logic

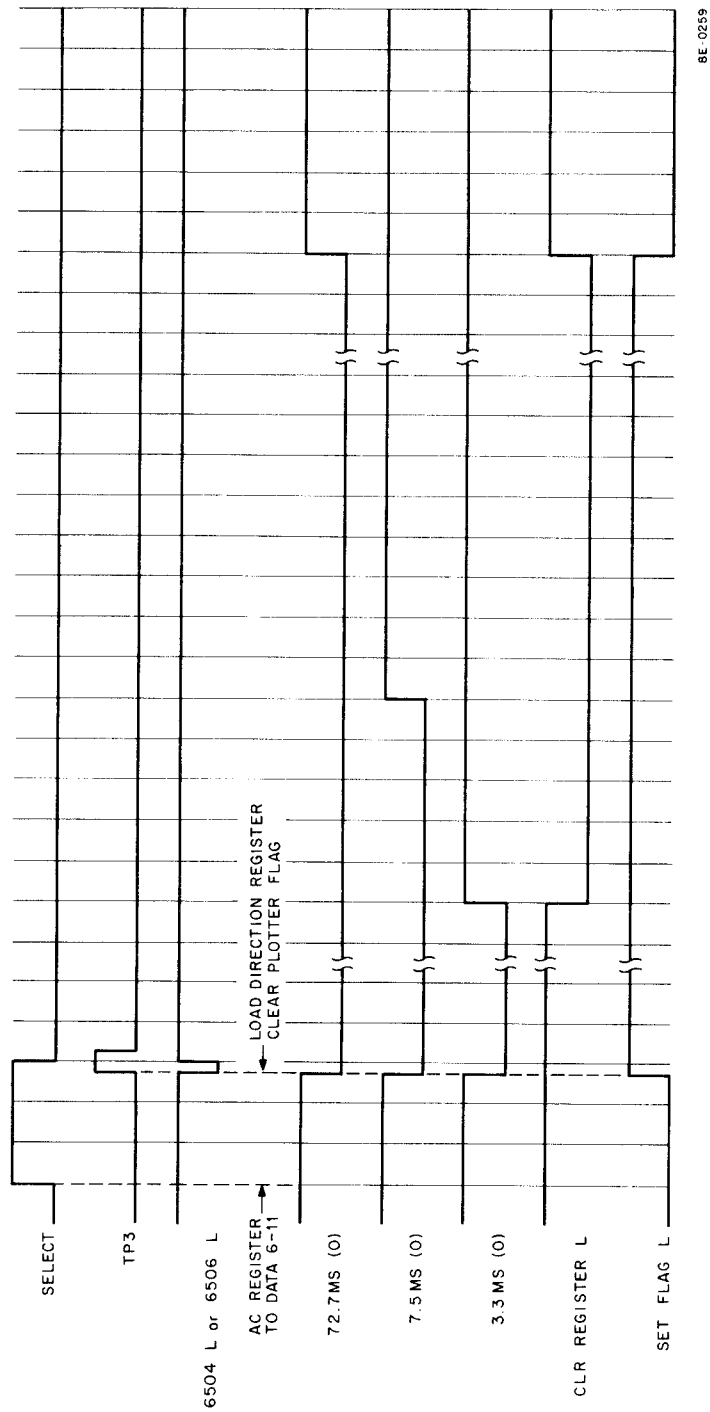

Figure 3-4 Function Timing; Pen Up, Pen Down, Start Zip (Encoded Plotter)

HOUSTON DP-10

Table 3-2
List of Plotter Directions

AC06–11 Octal Code	Direction		
	Unencoded Plotter	Encoded Plotter	
		Paper	Film
01	Pen up	–	–
02	Pen down	–	–
04	Drum up	–	–
10	Drum down	+y	+y
11	–	+x+y	+x+y
12	–	+x	+x
13	–	+x-y	+x-y
14	–	-y	-y
15	–	-x-y	-x-y
16	–	-x	-x
17	–	-x+y	-x+y
20	Pen left	–	–
21–27	–	–	–
30	–	–	CRT shift
31	–	Pen up	Beam off
32	–	Pen down	Beam on
33	–	Start zip	–
34	–	Block code	-z (+Aux 1)
35	–	Plot code	+z (+Aux 2)
36	–	Start incr	–
37	–	Sync	Sync
40	Pen right	–	–
41–47	–	–	–
50	–	+y/2	–
51	–	+x/2+y/2	–
52	–	+x/2	–
53	–	+x/2-y/2	–
54	–	-y/2	–
55	–	-x/2-y/2	–
56	–	-x/2	–
57	–	-x/2+y/2	–
61–67	–	–	–
70	–	+x+y/2	–
71	–	-x+y/2	–
72	–	+x/2+y	–
73	–	-x/2+y	–
74	–	+x-y/2	–
75	–	-x-y/2	–
76	–	+x/2-y	–
77	–	-x/2-y	–

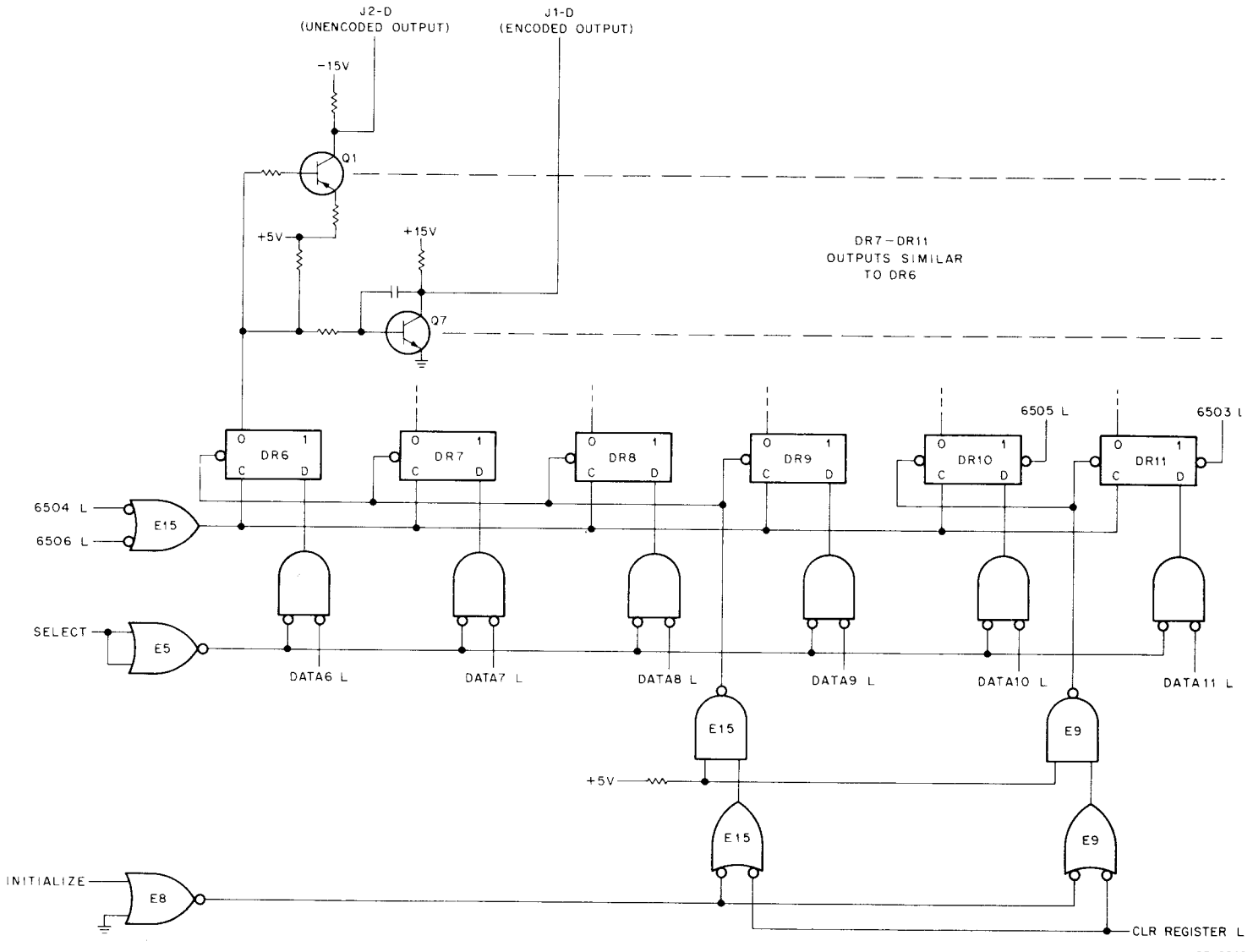

Figure 3-5 Direction Transfer Logic

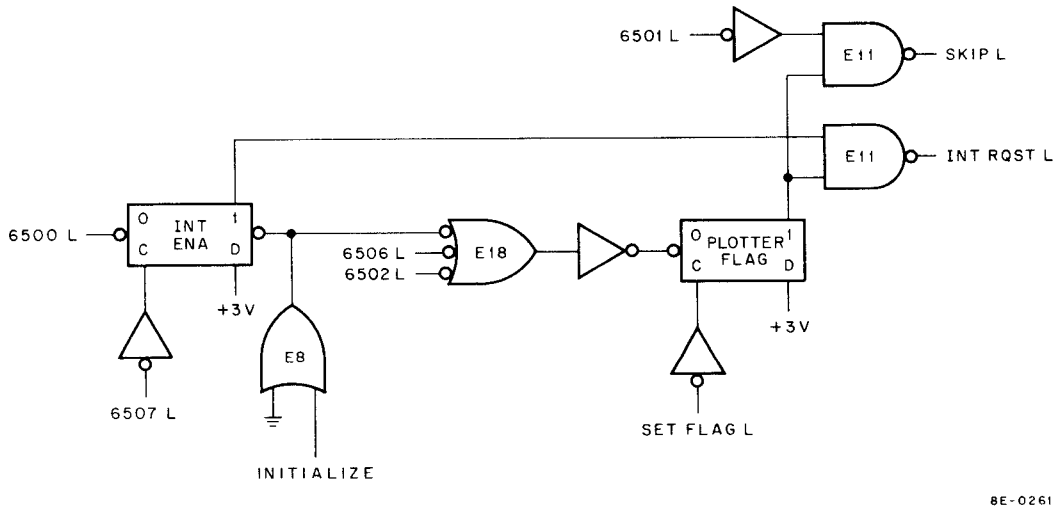

Figure 3-6 INT/Skip Logic

When the INT ENA flip-flop is set, the OMNIBUS INT RQST L signal can be asserted by the PLOTTER FLAG flip-flop. The PLOTTER FLAG flip-flop is set by the SET FLAG L signal when a direction has been carried out by the plotter. The computer identifies the requesting device by entering the interrupt servicing routine. The 6501 (PLSF) IOT instruction in the routine directs the computer to the XY8-E subroutine and another direction is transferred to the Direction Register. The PLOTTER FLAG flip-flop is cleared under program control by the 6502, 6506, and 6007 (via the INITIALIZE signal) IOT instructions, as well as at power turn-on by INITIALIZE.

SECTION 5 MAINTENANCE

The relative simplicity of the XY8-E logic precludes the necessity of a detailed maintenance procedure. Use the diagnostic program to isolate problems that occur in the XY8-E Plotter System. Standard troubleshooting techniques, using the logic drawings and an oscilloscope, will enable the technician to isolate faulty components.

Table 3-3 shows the connector pin assignments for the Plotter Control/plotter interconnecting cable.

SECTION 6 SPARE PARTS

Table 3-4 lists the recommended spare parts for the XY8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 3-3
Pin Assignments, Interconnecting Cable

From Cannon 19-Pin Connector Pin	Signal Name Significant For Unencoded Plotter Only		To Berg 40-Pin Connector Pin
	Houston Inst. Plotter	CalComp Plotter	
1	CHART RIGHT (-X)	DRUM UP (-X)	L
2	CHART LEFT (+X)	DRUM DOWN (+X)	J
3	CARRIAGE UP (+Y)	PEN LEFT (+Y)	F
4	CARRIAGE DOWN (-Y)	PEN RIGHT (-Y)	D
9	PEN UP	PEN UP	R
10	PEN DOWN	PEN DOWN	N
15	GND	GND	S
Pins 5–8, 11–14, 16–19 not used			Pins T, V, X, Z, BB, DD, FF, JJ, LL, NN, RR, TT, not used Pins A, B, C, E, H, K, M, P, S, U, W, Y, AA, CC, EE, HH, KK, MM, PP, SS, UU, VV are gnd.

Table 3-4
XY8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
15-03409-1	Transistor DEC 6534B	1
15-03100	Transistor DEC 3009B	1
19-09705	IC DEC 8881	1
19-09704	IC DEC 314	1
19-09686	IC DEC 7404	1
19-09594	IC DEC 8251	1
19-09373	IC DEC 9601	1
19-09485	IC DEC 380	1
19-05577	IC DEC 7420	1
19-05576	IC DEC 7410	1
19-05575	IC DEC 7400	1
19-05547	IC DEC 7474	1
13-000391	Resistor 1.5K, 1/4W, 5%	1

PART 4
LINE PRINTER

CHAPTER 4
LE8-E LINE PRINTER

SECTION 1 INTRODUCTION

The LE8-E Line Printer Control interfaces an 80- or 132-column line printer to the PDP-8/E. All logic is contained on a single quad module that plugs into the OMNIBUS. The LE8-E connects to the line printer via a signal cable that is supplied with the system.

The LE8-E Line Printer is discussed here only to the extent necessary to both fully describe LE8-E operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the printer itself can be found in Data Products Corporation Technical Manual DPC-214163A (80-column printer) or DPC-215656A (132-column printer). Other publications and documents relevant to the LE8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. LE8-E Line Printer Diagnostic, MAINDEC-8E-D2BA
d. DEC Engineering Drawing, Line Printer Control, E-CS-M841-0-1.

SECTION 2 INSTALLATION

The LE8-E Line Printer and Control are installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

4.1 UNPACKING

Place the LE8-E Line Printer close to the ac power source and proceed as follows:

Step	Procedure
1	Cut the two steel straps that secure the telescoping cap and stitched sleeve to the shipping skid.
2	Remove the Tri-wall clips from all four sides of the stitched sleeve.
3	Remove the four bolts, washers, and nuts securing the line printer to the shipping skid, then remove the printer from the skid and install on the site.

(continued on next page)

Step	Procedure
4	Unpack the LE8-E Control and the signal cable. Plug the LE8-E into the PDP-8/E OMNIBUS and connect it to the line printer with the cable (refer to Table 2-3, Volume 1, for information concerning module installation order). The cable connects to the control via a Berg Connector and to J1 of the line printer via a Winchester MRAC-50 Connector (refer to Section 1 of the Data Products Corporation technical manual for the location of J1).
5	Inspect both printer and control as outlined below and report any damage to the local DEC sales office. a. Inspect external surfaces of the printer and control for surface, bezel, switch, and light damage. b. Open the printer doors and inspect for internal damage. c. Inspect the wiring side of the printer logic mounting panels and the control module for bent pins, cut wire, loose external components, and foreign matter. Also inspect the signal cable for damage. d. Check equipment received against the packing list to be certain that all equipment has been unpacked.

4.2 CHECKOUT

Use the following procedure to check out the LE8-E Line Printer and Control.

Step	Procedure
1	Insert the ribbon in the printer, following the ribbon installation procedure detailed in Section 3 of the Data Products Corporation technical manual (referred to hereafter as the technical manual).
2	Load the printer with continuous-form paper, following the paper loading procedure detailed in Section 3 of the technical manual. NOTE **The READY indicator on the printer control panel should light 10–15 seconds after the last step of the procedure (close and latch drum gate, etc.) has been completed.**
3	See the paper positioning (vertical) procedure in Section 3 of the technical manual.
4	Check that the TOP OF FORM and PAPER STEP switches operate as in Table 3-1 of the technical manual.
5	Set the ON LINE/OFF LINE switch to the ON LINE position and check that the TOP OF FORM and PAPER STEP switches do not operate.
6	Hold the MASTER CLEAR switch in the "up" position and check that the READY and ON LINE indicators go out. Release the switch; the READY indicator should light.
7	Check the right tractor for correct adjustment and make sure that the COPIES CONTROL switch is set to the 1–2 position.
8	Set the ON LINE/OFF LINE switch to the ON LINE position and run the MAINDEC diagnostic program, starting at Part 1 of Test 1. While the program is running, adjust the vertical paper adjustment vernier.

(continued on next page)

Step	Procedure
9	Stop the program and set the PRINT INHIBIT switch to the "up" position; set the ON LINE/OFF LINE switch to the ON LINE position and restart the program from Part 1 of Test 1. The PRINT INHIBIT indicator should light and the program should run as in Step 8. Run the program for one minute.
10	Set the PRINT INHIBIT switch to the "down" position and check for printout errors.
11	Replace the continuous-form paper with single-part paper. Run all parts of the program (except Part 1 of Test 1) for one hour.
12	Inspect all printouts for errors and print quality and compare to the enclosed factory-printed samples.

SECTION 3 BLOCK DIAGRAM DESCRIPTION

Figure 4-1 is a block diagram of the LE8-E Control. OMNIBUS pin numbers and pin assignments for both ends of the signal cable can be found on engineering drawing E-CS-M841-0-1. Connector receptacle J1 on the line printer is a 20-pin connector with a return pin for each of the 10 signal pins. Figure 4-2 is a timing diagram of the control; Table 4-1 presents the LE8-E IOT instructions. Refer to the figures while reading this description.

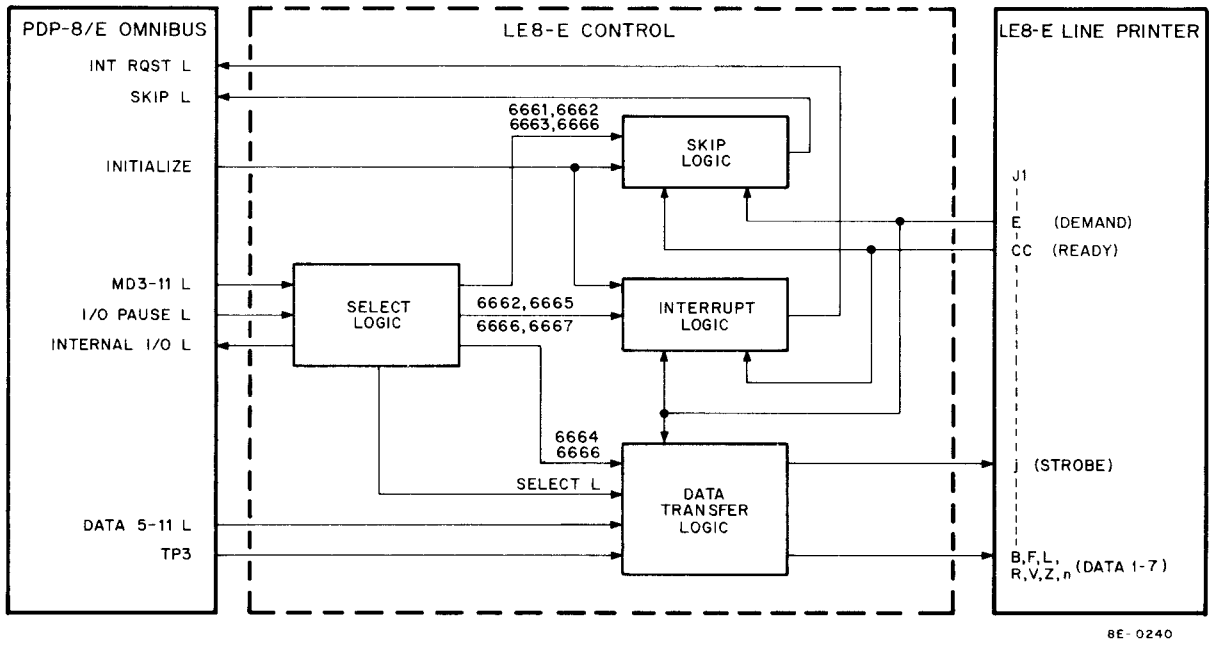

Figure 4-1 LE8-E Line Printer Control Block Diagram

When the line printer is ready to be placed on-line, a READY indicator on the line printer lights. At the same time, the READY signal is asserted. After the line printer has been placed on-line, it asserts the DEMAND signal when it is able to accept a character. The DEMAND signal sets the FLAG flip-flop in the interrupt logic. If the INT ENA flip-flop is set, the FLAG flip-flop asserts the OMNIBUS INT RQST L signal. The computer then begins to execute the interrupt servicing routine to determine the identity of the requesting device.

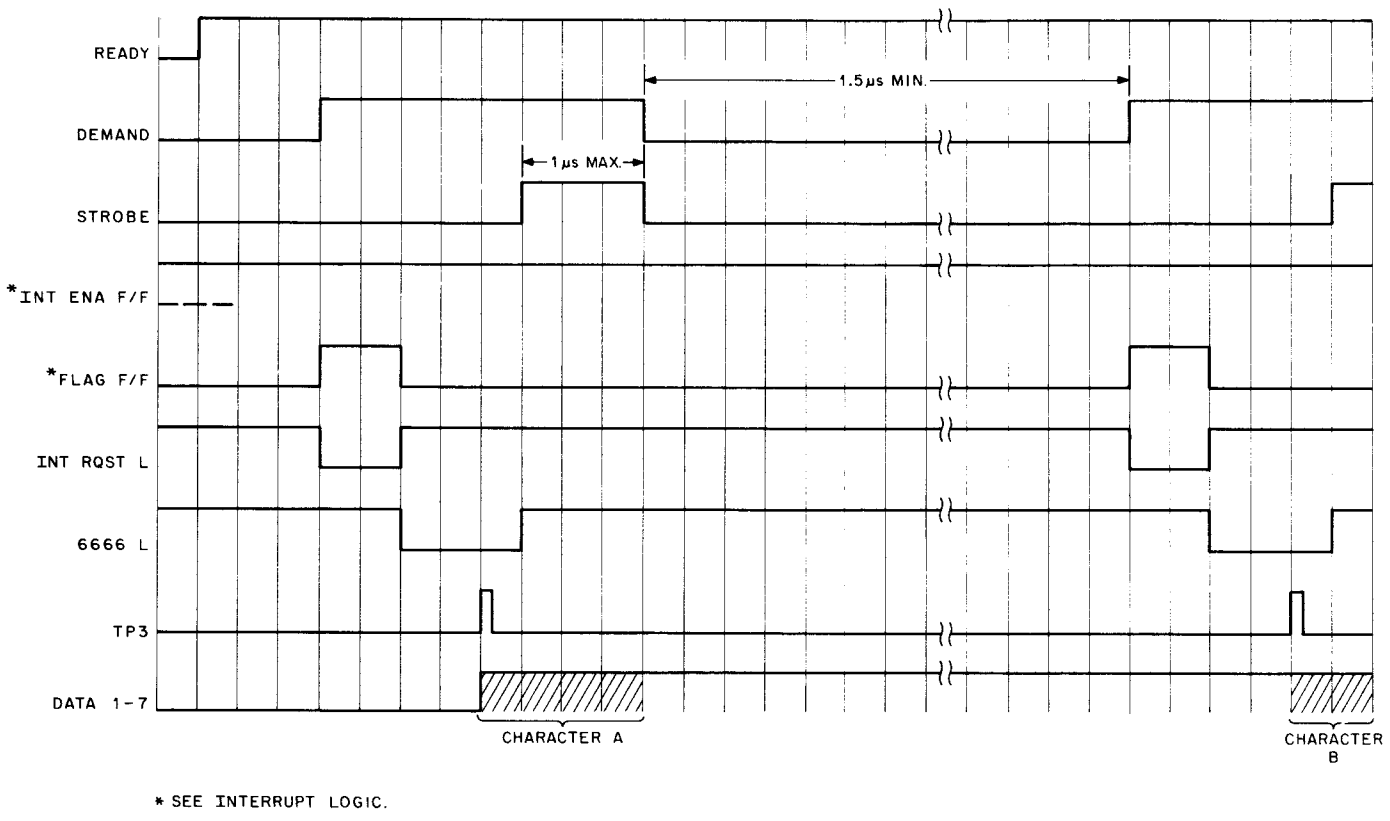

Figure 4-2 LE8-E Control Timing

Table 4-1
LE8-E IOT Instruction List

Octal Code	Mnemonic	Function
6661	PSKF	Skip on the Flag. Senses the state of the FLAG flip-flop. If it is set, the program counter is incremented so that the next sequential instruction is skipped.
6662	PCLF	Clear the Flag. Clears the FLAG flip-flop.
6663	PSKE	Skip on an Error. Senses the state of the READY signal. If it is low, indicating an error condition in the line printer, the program counter is incremented so that the next sequential instruction is skipped.
6664	PSTB	Load Line Printer Buffer Register. A character is transferred from the CPU AC Register, via the OMNIBUS DATA 5–11 lines and the Line Printer DATA 1–7 lines, to the Printer Buffer Register.
6665	PSIE	Set INT ENA flip-flop. The LE8-E is logically connected to the computer interrupt system. Both the READY signal and the DEMAND signal can cause a program interrupt.
6666	PCLF, PSTB	Clear the Flag, Load Line Printer Buffer Register. Microprogram of 6662 and 6664.
6667	PCIE	Clear INT ENA flip-flop.

When the 6661 instruction in the servicing routine is decoded, the skip logic asserts the OMNIBUS SKIP L signal. The computer then proceeds to the subroutine associated with the LE8-E. When the 6666 instruction (as an example) in the subroutine is decoded, the FLAG flip-flop is cleared and the information in the AC Register is placed on the OMNIBUS DATA 5–11 lines; at TP3 time the information is clocked into the Buffer Register of the data transfer logic. At the trailing edge of the 6666 instruction signal, the STROBE signal is generated and the information is clocked from the DATA 1–7 lines of the line printer into the 20-character Shift Register within the line printer. The DEMAND signal is then negated and, in turn, negates the STROBE signal.

SECTION 4 DETAILED LOGIC

4.3 SELECT LOGIC

The select logic is shown in Figure 4-3. Both the SELECT L and INTERNAL I/O L signals are asserted when a 666X instruction is decoded. The INTERNAL I/O L signal causes the positive I/O bus interface to ignore the IOT instruction; the SELECT L signal is gated with bits MD9–11 to provide inputs for the BCD-to-decimal decoder, E17 (refer to Appendix A, Volume 1, for details about the DEC 8251 IC). The decoder supplies the signals that represent IOT instructions 6661 through 6667.

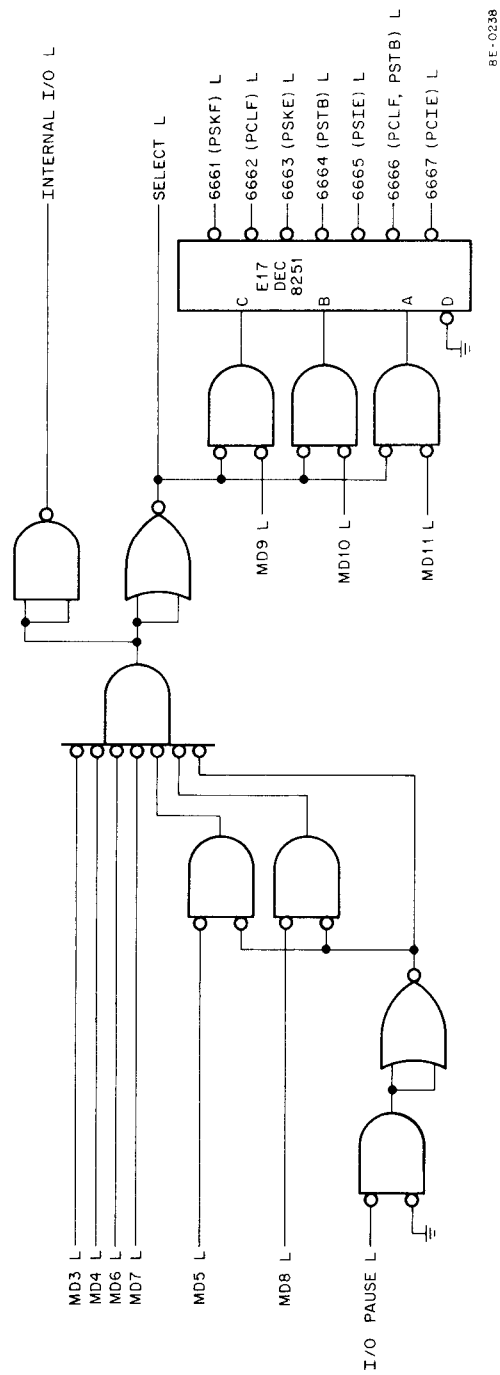

Figure 4-3 Select Logic

4.4 INTERRUPT LOGIC

The interrupt logic is shown in Figure 4-4. When the INT ENA flip-flop is set, the control is logically connected to the computer interrupt system. This flip-flop is cleared at computer power turn-on by the OMNIBUS INITIALIZE signal and can be cleared and set under program control by instructions 6667 (or 6007, CAF) and 6665, respectively.

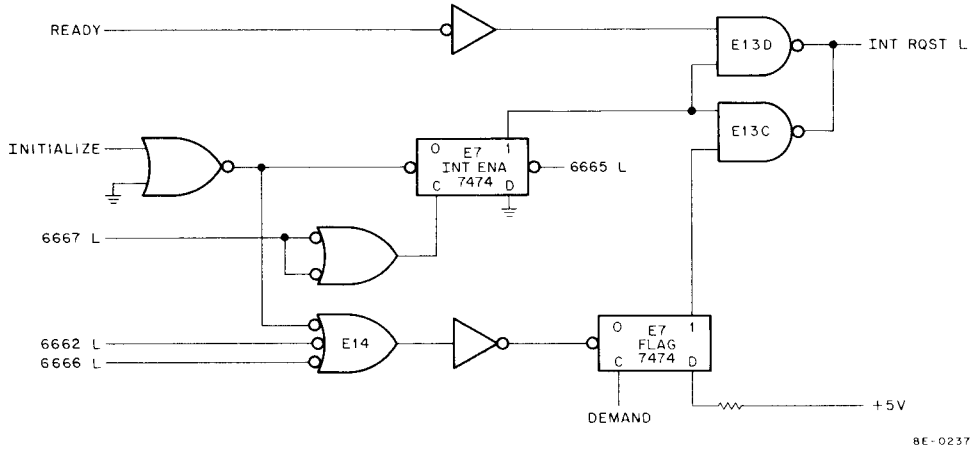

Figure 4-4 Interrupt Logic

When the INT ENA flip-flop is set, both the READY signal and the DEMAND signal can cause a program interrupt. If the READY signal is low, indicating an error condition in the line printer (drum gate open, excessive temperature in paper drive motor, insufficient drum motor speed, or printer out of paper) NAND gate E13 asserts the INT RQST L signal and the computer begins the interrupt servicing routine. Instruction 6663 senses the state of the READY line and causes a skip in the CPU program counter if READY is low (Figure 4-5).

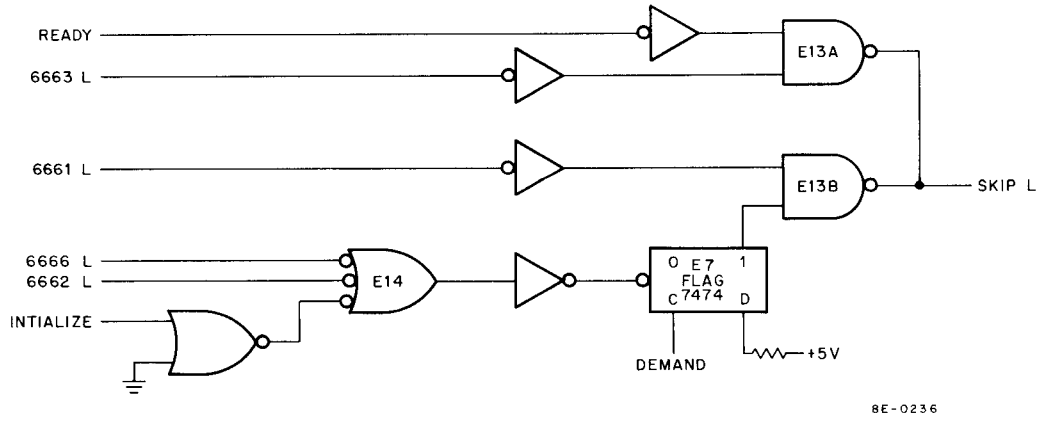

Figure 4-5 Skip Logic

The DEMAND signal causes a program interrupt by setting the FLAG flip-flop, as outlined in Section 3. Instruction 6661 senses the state of the FLAG flip-flop and causes a program skip when the FLAG is set (Figure 4-5). The FLAG flip-flop is cleared by the INITIALIZE signal and by program instructions 6662 and 6666.

4.5 DATA TRANSFER LOGIC

The data transfer logic is shown in Figure 4-6. The 7-bit code transmitted from the CPU AC Register to the printer 20-character Shift Register represents characters that appear on the 64- or 96-character printer drum (refer to the table of code/character relationship in Volume 1, Section 4). The coded information is gated from the AC Register to the OMNIBUS DATA 5—11 lines when the 6666 or 6664 instruction is decoded in the CPU. The SELECT L signal enables the DATA lines to condition the D-inputs of the 7-stage Buffer Register. When the control decodes the 6666 or 6664 instruction, the buffer is loaded at TP3 time and the coded character is placed on the printer DATA 1—7 lines.

Each character is followed by the STROBE signal that is generated when the STROBE flip-flop is set by the trailing edge of the instruction. The printer samples the DATA 1—7 lines and negates the DEMAND signal, clearing the STROBE flip-flop.

SECTION 5 MAINTENANCE

Refer to Volume 1 and the Data Products Corporation technical manual for maintenance information that pertains to both the control and the printer. The LE8-E Diagnostic, MAINDEC-8E-D2BA, should be run when an error in the LE8-E is suspected.

SECTION 6 SPARE PARTS

Table 4-2 lists recommended spare parts for the LE8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 4-2
LE8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-05547	IC DEC 7474	1
19-05576	IC DEC 7410	1
19-05590	IC DEC 7401	1
19-09485	IC DEC 380	1
19-09594	IC DEC 8251	1
19-09686	IC DEC 7404	1
19-09704	IC DEC 314	1
19-09705	IC DEC 8881	1

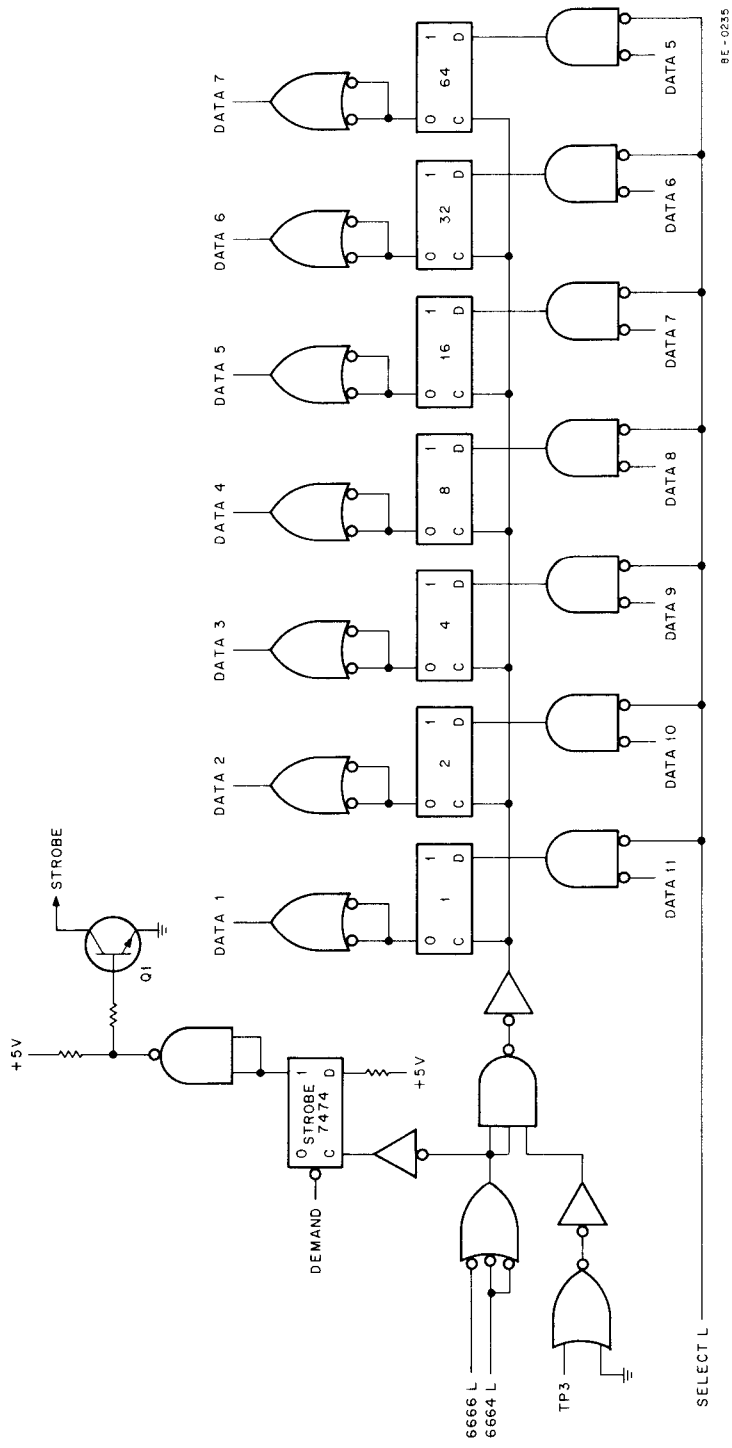

Figure 4-6 Data Transfer Logic