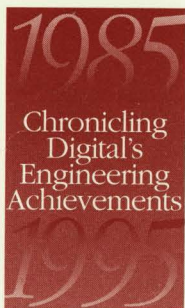


# Digital Technical Journal

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## Cumulative Index

1985-1994



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# Digital Technical Journal

## Cumulative Index

1985-1994

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# Preface

This cumulative index is provided as a convenient means for readers to locate subjects referenced in the *Digital Technical Journal* from 1985 through 1994. Since the *Journal* was first published in 1985, it has offered engineers and educators insights into the design of Digital's innovative engineering in such areas as software, systems, peripherals, semiconductors, and networking. With this index, readers can now more easily access that information.

The editors welcome comments on the utility of the index. Usefulness to readers will determine the frequency with which future indexes are published and enhancements made to the search capabilities of the *Journal's* electronic files on the World Wide Web. Comments may be sent to the attention of the Managing Editor, Digital Technical Journal, Digital Equipment Corporation, 30 Porter Road LJO2/D10, Littleton, Massachusetts 01460 U.S.A., or through the Internet to dtj@digital.com.

## How to Use the *Digital Technical Journal* Cumulative Index

This cumulative index has been designed as a guide to the content and location of papers in the *Digital Technical Journal* 1985–1994. The four sections are Subject Index, Volume Listing, Author Listing, and Acronym Glossary.

**Subject Index** headings are arranged alphabetically. Subheadings are indented under main headings, and secondary subheadings are indented under subheadings. All entries are then arranged chronologically and refer to volume, number, date (year), and page numbers.

### Example:

Alpha AXP, 4/4 (1992) 19–205

Alpha AXP program, 4/4 (1992) 193–205

software simulators, 4/4 (1992) 181–192

Cross-references serve as guides from one heading to another and are of two types:

- *See* references guide the reader to the preferred form of a subject (e.g., LSE *see* Language Sensitive Editor)

- *See also* references guide the reader from one heading to other headings where there is relevant material (e.g., DEC Rdb *See also* VAX Rdb/VMS).

The **Volume Listing** presents the titles and authors of papers for all issues that make up the six volumes referenced in this index.

In the **Author Listing**, author names are arranged alphabetically. A chronological listing of an author's papers follows his or her name.

Because of the extensive number of acronyms used throughout the literature, an **Acronym Glossary** is provided for readers' quick referral.

## Acknowledgments

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# Acronym Glossary

## Acronym Definition

ACA	application control architecture
ACMS	application control and management system
AIL	application interface library
API	application programming interface
ASN	abstract syntax notation
AUD	Alpha user-mode debugging
AUDI	Alpha user-mode debugging environment for translated images
AXE	architecture exerciser
BIOS	basic input-output system
BIU	bus interface unit
BLAS	basic linear algebra subroutines
BLOB	binary large object
BMP	buffer management protocol
CAD	computer-aided design
CAM	content addressable memory
CASE	computer-aided software engineering
CDA	compound document architecture
CFPA	CVAX floating point accelerator
CI	computer interconnect
CMCTL	CMOS memory controller
CMOS	complementary metal-oxide semiconductor
CNS	common node software
CORBA	common object request broker architecture
CPAP	common printer access protocol
CPS	common printer supervisor
CPU	central processing unit
CQBIC	CVAX Q22-bus interface chip
CSMA/CD	carrier sense multiple access with collision detection
DAS	DECimage application services
DBMS	database management system
DCE	distributed computing environment
DDE	dynamic data exchange
DDIF	Digital document interchange format
DDIS	Digital data interchange syntax
DDX	device-dependent X
DECdta	DEC distributed transaction processing architecture
DECdtm	DEC distributed transaction manager
DECelms	DEC extended LAN management software
DECNIS	DEC network integration server
DECTp	DEC transaction processing
DFS	distributed file service
DIX	device-independent X
DLT	Digital linear tape
DLZI	Digital Lempel-Ziv 1

## Acronym Definition

DNA	Digital network architecture
DNP	DECnet network process
DNS	distributed name service
DQFD	distributed quality function deployment
DRAM	dynamic random access memory
DTIF	Digital table interchange format
DXML	Digital extended math library
E <sup>2</sup> COTS	extended environment, commercial off-the-shelf
EMA	enterprise management architecture
EMS	electronic mail system
FAL	file access listener
FCIS	frame content independent stripping
FDDI	fiber distributed data interface
FRBS	frame relay bearer service
FTAM	file transfer, access and management
GKS	graphical kernel system
GSMP	generalized semi-Markov process
HDSC	high density signal carrier
HSC	hierarchical storage controllers
I/O	input/output
I <sup>2</sup> C	interintegrated circuit
IDRC	improved data recording capability
IMA	Interactive Multimedia Association
IOS	integrated office system
LAN	local area network
LAPACK	linear algebra package
LAPS	local area printserver protocol
LAST	local area system transport
LAT	local area transport
LSE	language-sensitive editor
MAX	multi-instruction architecture exerciser
MCA	macrocell array
MCU	multichip unit
MDA	manufacturing data access
MIPS	million instructions per second
MOSAIC	Motorola's oxide-isolated self-aligned implanted circuits
MPEG	Motion Picture Experts Group
MPP	massively parallel processor
MSCP	mass storage control protocol
NCP	network control process
NETACP	network ancillary control process
NetBIOS	network basic input-output system
NI	network interconnect
NML	network management listener
OSF	Open Software Foundation



## Acronym Definition

OSI	open systems interconnection
P/FM	PBX facilities management
PBX	private branch exchange
PCI	peripheral component interconnect
PDL	page description language
PEX	PHIGS/PHIGS+ extension to X
PHIGS	programmer's hierarchical interactive graphical system
PLL	phase-locked loop
POSIX	portable operating system interface for computer environment
PVP	parallel vector processors
QFD	quality function deployment
QIO	queued I/O
RAID	redundant arrays of inexpensive disks
Rdb	relational database
RISC	reduced instruction set computer
RMC	ring memory controller
RPC	remote procedure calls
RSM	remote system manager
RTL	register transfer level
RTL	run-time library
SCA	system communication architecture
SCSI	small computer systems interface
SEI	Software Engineering Institute
SID	system for integral design
SMB	server message block
SMP	software motion pictures
SMP	symmetric multiprocessing
SNA	systems network architecture
SOC	system on a chip
SPIN	sound picture information networks
SQL	standard query language
SRAM	static random-access memory
SSC	system support chip
TAB	tape automated bonding
TCP/IP	transmission control protocol/internet protocol
TIE	translated image environment
TP	transaction processing
UART	universal asynchronous receiver/transmitter
UDP/IP	user datagram protocol/internet protocol
UID	user interface description
UIL	user interface language
UIS	user interface services
UTF	universal transmission format
VALU	VAX application link utilities
VAS	VTX application service
VEST	VAX environment software translator
VISTA	VTX infobase structure tool and assistor
VME	versatile microprocessor
VWS	VMS workstation software
WFMS	workflow management system
WORM	write once read many
XDPS	X display postscript system
XIE	X image extension
XUI	X user interface

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