DECUS
PROGRAM LIBRARY

DECUS NO.	8-487
TITLE	REVISED OCTAL MEMORY DUMP
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SOURCE LANGUAGE	PAL III

DECUS Program Library Write-up DECUS NO. 8-487

Revised Octal Memory Dump

Description:

As initialization, low and high address are read through the switch register. After the initialization, a carriage return line feed and the low address followed by 4 spaces are typed. Next, the content is typed and the memory location is incremented by one. This process is repeated.

When the 9, 10 and 11th bits of the memory location are found to be all 0, a carriage return line feed is typed, thus, an address and contents of 8 memories are typed a line. Moreover, the 6, 7 and 8th bits of it are found to be all 0, a carriage return line feed is typed again. At last, the high address is reached, this routine returns to the start address.

Revised point:

1. 8 words output for a line.
2. The left most memory location is multiple of 8.

Example

Revised octal dump was used to dump itself as follows:

```
7400    7402  7604  3305  7402  7604  7040  1305  3306
7410    4241  1305  4255  4247  1705  4255  2305  2306
7420    7410  5200  1305  0276  7640  5214  1305  0277
7430    7650  4241  5210  7454  6046  6041  5235  7200
7440    5633  0000  1301  4233  1302  4233  5641  7475
7450    1303  4233  1303  4233  5647  7416  7104  3247
7460    1300  3241  1247  7006  7004  3247  1247  0276
7470    1304  4233  2241  5262  4247  5655  0007  0077

7500    7774  0215  0212  0240  0260  7505  7777
```

Loading:

This routine is loaded with the Binary loader.

Calling seguence:

None. It cannot be called as a subroutine.

Switch Settings:

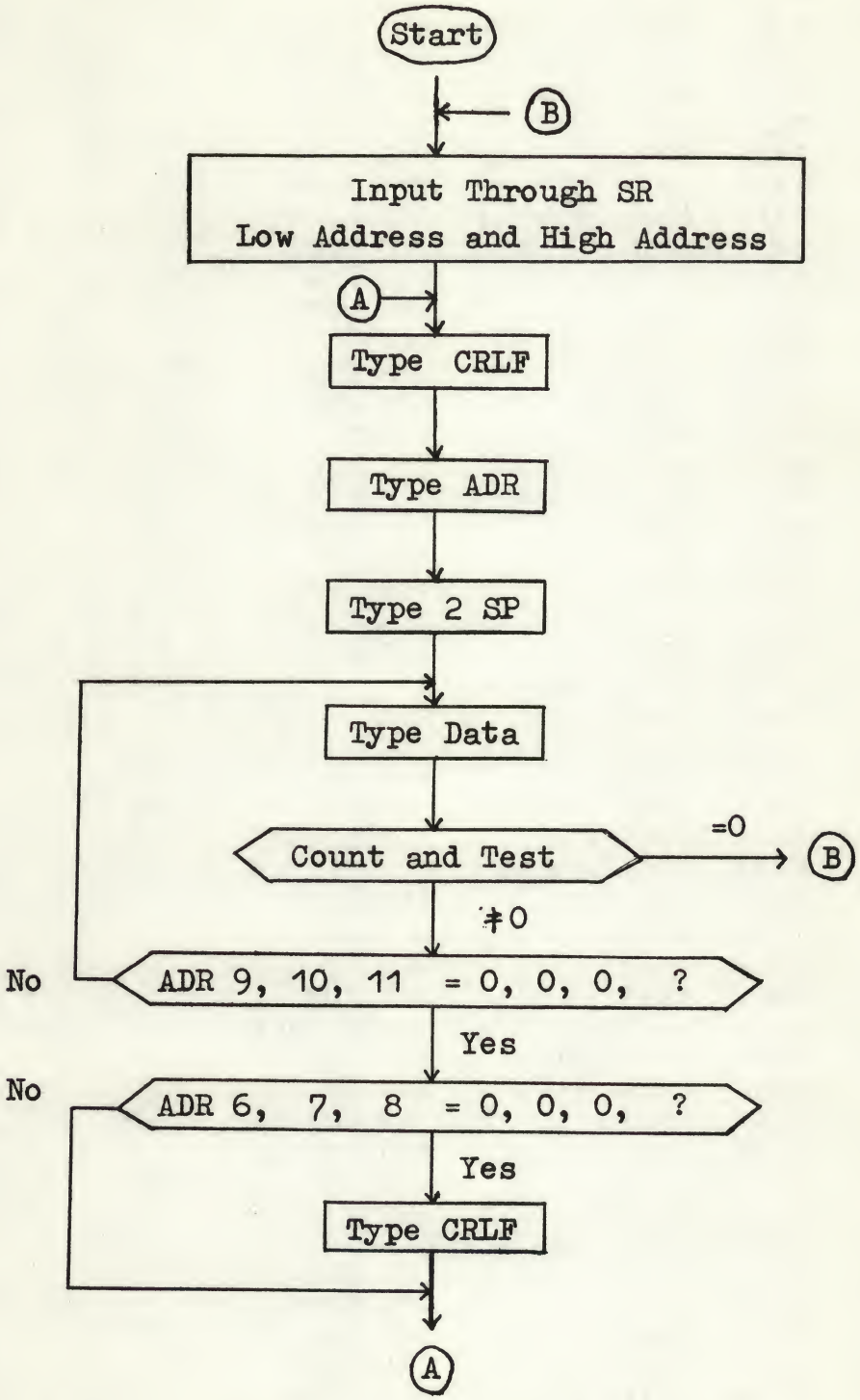
The switch register is used to enter the starting address. It is also used to enter two delimiting address which define the area of memory to be typed.

Start Up / Entry:

Assuming the program is in memory, proceed as follows:

1. Set the starting address in the switch register, press the LOAD ADDRESS key and press the START key.
2. The computer will halt.
3. Set the low address into the switch register and press the CONTINUE key.
4. The computer will halt. Set the high address into the switch register and press the CONTINUE key.
5. Type out will occur and the computer will halt, when the designated block has been listed.
6. To type another block, back to the step 3 above.

Flowchart


Start
B
Input Through SR
Low Address and High Address
A
Type CRLF
Type ADR
Type 2 SP
Type Data
Count and Test
=0
B
≠0
No
ADR 9, 10, 11 = 0, 0, 0, ?
Yes
No
ADR 6, 7, 8 = 0, 0, 0, ?
Yes
Type CRLF
A

```
                *7400
7400   7402  STRT,   HLT
7401   7604           CLA OSR
7402   3305           DCA ADR
7403   7402           HLT
7404   7604           CLA OSR
7405   7040           CMA
7406   1305           TAD ADR
7407   3306           DCA KOSU
7410   4241  A2,     JMS CRLF
7411   1305           TAD ADR
7412   4255           JMS COUT
7413   4247           JMS SPSP
7414   1705  A1,     TAD I ADR
7415   4255           JMS COUT
7416   2305           ISZ ADR
7417   2306           ISZ KOSU
7420   7410           SKP
7421   5200           JMP STRT
7422   1305           TAD ADR
7423   0276           AND 07
7424   7640           SZA CLA
7425   5214           JMP A1
7426   1305           TAD ADR
7427   0277           AND 077
7430   7650           SNA CLA
7431   4241           JMS CRLF
7432   5210           JMP A2
7433   0000  OUT,    0
7434   6046           TLS
7435   6041           TSF
7436   5235           JMP .-1
7437   7200           CLA
7440   5633           JMP I OUT
7441   0000  CRLF,   0
7442   1301           TAD CR
7443   4233           JMS OUT
7444   1302           TAD LF
7445   4233           JMS OUT
7446   5641           JMP I CRLF
7447   0000  SPSP,   0
7450   1303           TAD SP
7451   4233           JMS OUT
7452   1303           TAD SP
7453   4233           JMS OUT
7454   5647           JMP I SPSP
7455   0000  COUT,   0
7456   7104           CLL RAL
7457   3247           DCA SPSP
7460   1300           TAD M4
7461   3241           DCA CRLF
7462   1247  B1,     TAD SPSP
7463   7006           RTL
7464   7004           RAL
7465   3247           DCA SPSP
7466   1247           TAD SPSP
7467   0276           AND 07
7470   1304           TAD ZERO
```

```
7471   4233            JMS OUT
7472   2241            ISZ CRLF
7473   5262            JMP B1
7474   4247            JMS SPSP
7475   5655            JMP I COUT
7476   0007   07,      7
7477   0077   077,     77
7500   7774   M4,      -4
7501   0215   CR,      215
7502   0212   LF,      212
7503   0240   SP,      240
7504   0260   ZERO,    260
7505   0000   ADR,     0
7506   0000   KOSU,    0

ADR      7505
A1       7414
A2       7410
B1       7462
COUT     7455
CR       7501
CRLF     7441
KOSU     7506
LF       7502
M4       7500
OUT      7433
07       7476
077      7477
SP       7503
SPSP     7447
STRT     7400
ZERO     7504
```