

IDENTIFICATION

PRODUCT CODE: MAINDEC-8E-DIAB-D
PRODUCT NAME: MM8E 4K MEMORY CHECKERBOARD
DATE CREATED: JUNE 7, 1971
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: VERNON FREY

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1. ABSTRACT

This program is designed to detect core failures on half-selected lines under worst case noise conditions. It's use is intended for the PDP-8E with a basic 4K memory system.

2. REQUIREMENTS

Equipment

A PDP-8E computer with 4K of memory.

Storage

Initially the program is in core locations 2000-777 and in core locations 7000-7577.

3. LOADING PROCEDURE

Load the program with the binary loader (BIN).

4. OPERATING PROCEDURE

There are two entries to the program. These entries allow the user to start by testing upper core (1000-7777), or start by testing lower core (0000-6777). To start the program:

A. Load Address with desired entry address.

LOAD ADDRESS	0200
--------------	------

 Test upper core (1000-7777).

LOAD ADDRESS	7000
--------------	------

 Test lower core (0000-6777)

B. Set switch register to desired operation according to the following table.

SWITCH	0 (down)	1 (up)
SR00	Continue testing	Halt after test
SR07	Relocate program	Inhibit relocation

C. Press key start.

NOTE 1: RIM and BIN are saved during this test and will not be lost if the program is halted using SR00.

NOTE 2: This program will alternate testing upper and lower core unless SR07 is set. During program relocation a comparison check is made to insure no program loss.

5. ERRORS

The contents of a given memory test location should always be 0000 or 7777, therefore anything other than 0000 or 7777 will result in a test error halt. A relocation error halt will occur if the relocation comparison check fails.

Test Error Halts

A test error halt is indicated by halt address 07XX or 75XX.

If the link is set, the error occurred on complemented data.

1st halt - The AC displays the contents of the location in error.

Record the C(AC) and press key continue.

2nd halt - The AC displays the address of the location in error.

Record the C(AC) and press key continue to resume testing with the next sequential memory address.

Relocation Error Halts

A relocation error halt is indicated by halt address 03XX or 71XX.

1st halt - The AC displays the contents of the location transferring from. Record the C(AC) and press key continue.

2nd halt - The AC displays the address of the location transferring from. Record the C(AC) and press key continue.

3rd halt - The AC displays the contents of the location transferring to. Record the C(AC) and press key continue.

4th halt - The AC displays the address of the location transferring to. Record the C(AC) and C(MA). Manually correct bad core location if possible. Load Address = C(MA) and press key continue to continue relocation.

6. RESTRICTIONS

Starting Restrictions

The program may be restarted at 0200 if the program is in lower core, or at 7000 if the program is in upper core. It can easily be determined where the program is by manually looking at a few core locations.

Operating Restrictions

None

7. EXECUTION TIME

The time to write and test the worst case pattern and its complement in upper and lower core is approximately 1 second.

During program execution a 5 will be typed on the TTY every 5 minutes of program run time. This allows the operator to determine approximate run time before a failure occurred.

8. SCOPE LOOPS

Two special scope loops have been provided in this program.

Before entering a scope loop run the checkerboard program with the halt switch up. This will write worst case pattern thru core.

Scope Loop 1

This scope loop reads the address in the switches 6 times before complementing.

- A. LOAD ADDRESS 0536 if program is in lower core
 7336 if program is in upper core.
- B. Set switches = address to be looped on.
- C. Press key start.

Scope Loop 2

This scope loop executed a simple read, complement, write.

- A. LOAD ADDRESS 0561 if program is in lower core
 7361 if program is in upper core.
- B. Set switches = address to be looped on.
- C. Press key start.

NOTE: The address being looped on can be changed simply by changing the switch settings. The previous address will be left with its original content.

9. PROGRAM DESCRIPTION

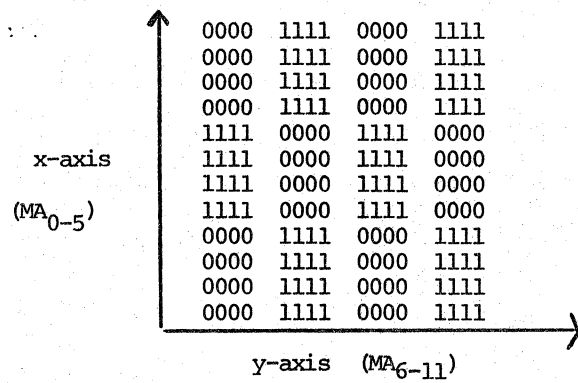
General

A given core is selected when the combined currents of the X- and Y- selection lines produce a magneto motive force which exceeds the threshold for reversing the flux direction of the core. This occurs at the intersection of the activated selection lines. All other cores which are threaded onto the activated lines will be slightly disturbed. Under marginal current conditions, such half-selected cores might also reverse polarity when their states are properly established by the pattern which the Checkerboard Test writes into memory.

When a selected core is in the 1 state, the read current will cause it to reverse polarity and become 0. When the core is in the 0 state, the write current will cause it to become 1. Thus, the possibility of a reading error is greatest when all half-selected cores are in the 1 state; a writing error is most probable when all the half-selected cores are in the 0 state.

If a half-selected core changes polarity, the error will be detected when the memory location containing that core is tested by the program. For a reading error, the contents of that core will appear as a 0 in a field of 1's, and vice versa for a writing error.

The Checkerboard Test pattern consists of alternating 4 memory cells containing 0000 and 4 memory cells containing 7777. This pattern is reversed every 400 octal locations. (This test pattern is generated according to the stringing of the stack and the wiring of the memory system. It is the same pattern for all 8E stacks).



The above array is interpreted as follows:

A. Positions on the y-axis represent consecutive octal locations in memory from 00 thru 77.

B. Positions on the x-axis represent consecutive octal locations in memory from 00 hundred thru 77 hundred.

Program Relocation

Program relocation is governed by the status of switch register bit 7. With this switch down (0 position) program relocation occurs each time the test pattern and its complement have been completely tested. During the relocation a comparison check is made to insure no program loss.

Test Procedure

The worst case pattern is written, then each location is treated as follows:

- a. Read, Complement, Write the location.
- B. Read and test the location.
- C. Read, Complement, Write the location.
- D. Read and test the location.
- E. Go on to next location repeating A-D.

After the pattern is completely tested, the complement pattern is written and tested.

For further understanding of how the test is performed, refer to the listing.

/CHECKERBOARD 'WORST CASE NOISE' FOR MM8-E 4K MEMORY (VER)
 /COPYRIGHT 1971, DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASS.
 /PROGRAMMER, VERNON FREY

/SW0=1 HALT PROGRAM SAVING BIN
 /SW7=1 INHIBIT PROGRAM RELOCATION

/PROGRAM STARTING ADDRESS
 /0200 TEST UPPER CORE
 /7000 TEST LOWER CORE

0000	0000	*0	0		
0001	0001		JMP	1	
0002	0002		2		
0003	0003		3		
0200	0200	*200	NOP		/WILL = JMP LGOP2 FOR RESTART
0201	7600		K7600,		/CLA USED AS CONSTANT 7600
0202	1205		LCNT1,		/WILL = TRANSFER CONTROL COUNTER
0203	3200		LCNT2,	DCA	/WILL = TRANSFER TO CONTROL
0204	4262		LCNT3,	JMS	/WILL = TRANSFER FROM CONTROL
0205	5364		LINAD1,	JMP	/WILL = INDIRECT ADDRESS
0206	5336		JMP	LPASS	/THIS INST MUST BE IN LOC 206
0207	4000		LSW0,	4000	/SR BIT 0
0210	0020		LSW7,	0020	/SR BIT 7
0211	0200		K0200,	0200	
0212	7000		K7000,	7000	
0213	7200		K7200,	7200	
0214	7604		LSR00,	LAS	/CHECK HALT PROGRAM SWITCH
0215	0207		AND	LSW0	
0216	7650		SNA	CLA	/HALT SW IS OFF
0217	5223		JMP	LSR07	
0220	4232		JMS	LHILO	/PROG IN LO - RESTORE BIN
0221	4272		JMS	LRESBN	/PROG IN HI
0222	7402		HLT		
0223	7604		LSR07,	LAS	/CHECK INHIBIT RELOCATION SWITCH
0224	0210		AND	LSW7	
0225	7640		SZA	CLA	
0226	5364		JMP	LGOP2	/INHIBIT RELOCATION

[illegible]

```

0272 0000      LRESBN, 0
0273 1201      TAD      K7600
0274 3202      DCA      LCNT1
0275 3204      DCA      LCNT3
0276 1201      TAD      K7600
0277 3203      DCA      LCNT2
0300 4302      JMS      LRELO
0301 5672      JMP I    LRESBN

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```

/RELOCATE SUBROUTINE
/RELO, 0
0302 0000      TAD I    LCNT3
0303 1604      DCA I    LCNT2
0304 3603      TAD I    LCNT3
0305 1604      CIA
0306 7041      TAD I    LCNT2
0307 1603      SZA CLA
0310 7640      JMS      LXFERF
0311 4320      ISZ      LCNT3
0312 2204      ISZ      LCNT2
0313 2203      NOP
0314 7000      ISZ
0315 2202      JMP      LRELO+1
0316 5303      JMP I    LRELO
0317 5702

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```

/RELOCATION FAILURE HALT ROUTINE
LXFERF, 0
0320 0000      TAD I    LCNT3
0321 1604      HLT
0322 7402      CLA
0323 7200      TAD      LCNT3
0324 1204      HLT
0325 7402      CLA
0326 7200      TAD I    LCNT2
0327 1603      HLT
0330 7402      CLA
0331 7200      TAD      LCNT2
0332 1203      HLT
0333 7402      CLA CLL
0334 7300      JMP I    LXFERF
0335 5720

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/TYPEOUT A '5' EVERY 5 MINUTES OF RUN TIME
LPASS, ISZ
0336 2357      JMP      LCNT
0337 5214      TAD      LSR00
0340 1360      DCA      LM750
0341 9397      LCNT
0342 1361      TAD      K215
0343 4351      JMS      LTRANS

```

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/~200
/CONTROLS 200 TRANSFERS
/PAGE 0 CA
/PAGE 31 CA
/RELOCATE BIN INTO PAGE 31

```

```

/TRANSFER FROM
/TRANSFER TO
/CHECK TRANSFER

```

```

/TRANSFER FAILED
/INCREMENT FROM ADDRESS
/INCREMENT TO ADDRESS
/INCREMENT TRANSFER CONTROL
/TRANSFER COMPLETE

```

```

/1ST HALT - FROM DATA

```

```

/2ND HALT - FROM ADDRESS

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```

/3RD HALT - TO DATA

```

```

/4TH HALT - TO ADDRESS

```

```

/NOT 5 MINUTES YET
/RESTORE COUNTER
/CR

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0344	1362	TAD	K212	/LF
0345	4351	JMS	LTRANS	
0346	1363	TAD	K265	/5
0347	4351	JMS	LTRANS	
0350	5214	JMP	LSR00	
0351	0000	LTRANS, 0		/TRANSMIT CODE
0352	6046	TLS		/WAIT FOR FLAG
0353	6041	TSF		
0354	5353	JMP	.-1	
0355	7300	CLA CLL		
0356	5751	JMP I	LTRANS	
0357	6400	LCNT, -1400		/COUNT 5 MINUTES
0360	6400	LM750, -1400		
0361	0215	K215, 215		/CR
0362	0212	K212, 212		/LF
0363	0265	K265, 265		/5
/GO TO PAGE 2 OR PAGE 29				
0364	4365	LGOP2, JMS	.-1	/0XXX OR 7XXX
0365	0000	0		
0366	7300	CLA CLL		
0367	1365	TAD	.-2	
0370	1211	TAD	K0200	
0371	0201	AND	K7600	
0372	3205	DCA	LINAD1	
0373	5605	JMP I	LINAD1	/0400 OR 7200
0400	0400	*400		
0401	5216	JMP	LWR	/WRITE PATTERN
0402	5225	JMP	LWRC	/WRITE COMPLEMENT
0403	7774	-4		
0404	7740	LM4, -40		
0405	0523	KLENDM, LENDM		/LO END MEM ROUTINE
0406	7330	KLAAA, HAAA		/HI END MEM ROUTINE
0407	0000	LEND1, 0		/END MEM ROUTINE
0410	0000	LMADD, 0		/START WRITE ADDRESS
0411	0000	LCNT4, 0		/WRITE 2 PAGES
0412	0000	LCNT5, 0		/WRITE 4 ADDRESSES
0413	0200	KK0200, 0200		
0414	1000	K1000, 1000		
0415	7600	KK7600, 7600		
0416	0000	LINAD2, 0		/INDIRECT ADDRESSING
/WRITE PATTERN INTO MEMORY				
0416	4235	LWR,		
0417	4253	JMS	LWCON	/CORRECT WRITE CONSTANTS
0420	1253	JMS	LWRMEM	/WRITE PATTERN
0421	1212	TAD	KK0200	/0XXX OR 7XXX
0422	0214	AND	KK7600	

```

0423 3215 DCA LINAD2
0424 5615 JMP I LINAD2 /0600 OR 7400

/ WRITE COMPLEMENT PATTERN INTO MEMORY
/
0425 4235 JMS LWCON /CORRECT WRITE CONSTANTS
0426 4255 JMS LWRMC /WRITE COMPLEMENT PATTERN
0427 1253 TAD LWRMEM /0XXX OR 7XXX
0430 1212 TAD KK0200
0431 0214 AND KK7600
0432 7001 IAC
0433 3215 DCA LINAD2
0434 5615 JMP I LINAD2 /0601 OR 7401

/ UPDATE WRITE CONSTANTS
/
0435 0000 LWCON, 0 /0XXX OR 7XXX
0436 1235 TAD -1
0437 7004 RAL
0440 7630 SZL CLA
0441 5247 JMP LWCON1 /PROG IN UPPER MEM
0442 1213 TAD K1000 /PROG IN LOWER MEM
0443 3207 DCA LMADD /START WRITE ADDRESS
0444 1204 TAD KLENDM
0445 3206 DCA LEND1 /END MEM ROUTINE
0446 5635 JMP I LWCON

LWCON1, TAD KLAAR
0447 1205 DCA LEND1 /END MEM ROUTINE
0448 3206 DCA LMADD /START WRITE ADDRESS
0449 3207 DCA LMADD
0450 5635 JMP I LWCON

/ WRITE PATTERN OR WRITE PATTERN COMPLEMENT
/
0453 0000 LWRMEM, 0 /WRITE PATTERN
0454 5261 JMP LW1010
0455 0000 LWRMC, 0
0456 1255 TAD -1
0457 3253 DCA LWRMEM /STORE RETURN ADDRESS
0460 5270 JMP LW0101 /WRITE COMPLEMENT

LW1010, TAD LM40 /-40
0461 1203 DCA LCNT4 /WRITE 2 PAGES
0462 3210 JMS LWONE /WRITE 4 WORDS OF ONES
0463 4311 JMS LWZERO /WRITE 4 WORDS OF ZEROS
0464 4300 JMS LCNT4
0465 2210 JSE LW1010+2
0466 5263 JMP LEND1 /END OF MEMORY?
0467 4606 JMS I LM40 /-40
0470 1203 TAD LW0101, TAD /WRITE 2 PAGES
0471 3210 DCA LCNT4 /WRITE 4 WORDS OF ZEROS
0472 4300 JMS LWZERO /WRITE 4 WORDS OF ONES
0473 4311 JMS LWONE

```

0474	2210	ISZ	LCNT4	
0475	5272	JMP	LW0101+2	
0476	4606	JMS I	LEND1	/END OF MEMORY?
0477	5261	JMP	LW1010	

0500	0000	LWZERO, 0		
0501	1202	TAD	LM4	/-4
0502	3211	DCA	LCNT5	/WRITE 4 ZEROS
0503	3607	DCA I	LMADD	
0504	2207	ISZ	LMADD	/INCREMENT MEMORY ADDRESS
0505	7000	NOP		
0506	2211	ISZ	LCNT5	
0507	5303	JMP	LWZERO+3	
0510	5700	JMP I	LWZERO	

0511	0000	LWONE, 0		
0512	1202	TAD	LM4	/-4
0513	3211	DCA	LCNT5	/WRITE 4 ONES
0514	7240	STA		
0515	3607	DCA I	LMADD	
0516	2207	ISZ	LMADD	/INCREMENT MEMORY ADDRESS
0517	7000	NOP		
0520	2211	ISZ	LCNT5	
0521	5314	JMP	LWONE+3	
0522	5711	JMP I	LWONE	

/CHECK FOR END OF MEMORY

0523	0000	LENDM, 0		
0524	1207	TAD	LMADD	
0525	7640	SZA CLA		
0526	5723	JMP I	LENDM	
0527	5653	JMP I	LWRMEM	
0530	0000	LAAA, 0		
0531	1207	TAD	LMADD	
0532	1213	TAD	K1000	
0533	7640	SZA CLA		
0534	5730	JMP I	LAAA	
0535	5653	JMP I	LWRMEM	

/TWO SPECIAL SCOPE LOOPS

/LScope1, LAS /TEST ADDRESS

0536	7604	DCA	LSWADD	
0537	3372	TAD I	LSWADD	
0540	1772	AND I	LSWADD	
0541	0772	AND I	LSWADD	
0542	0772	AND I	LSWADD	
0543	0772	AND I	LSWADD	
0544	0772	AND I	LSWADD	
0545	0772	AND I	LSWADD	
0546	7040	CMA		
0547	3772	DCA I	LSWADD	
0550	1772	TAD I	LSWADD	

0551	0772	AND I	LSWADD		
0552	0772	AND I	LSWADD		
0553	0772	AND I	LSWADD		
0554	0772	AND I	LSWADD		
0555	0772	AND I	LSWADD		
0556	7040	CMA			
0557	3772	DCA I	LSWADD		
0560	5336	JMP	LSCOP1		
0561	7604	LAS	LSCOP2,		/TEST ADDRESS
0562	3372	DCA	LSWADD		
0563	1772	TAD I	LSWADD		
0564	7040	CMA			
0565	3772	DCA I	LSWADD		
0566	1772	TAD I	LSWADD		
0567	7040	CMA			
0570	3772	DCA I	LSWADD		
0571	5361	JMP	LSCOP2		
0572	0000	LSWADD, 0			
0600	0600	JMP	LTST		/READ AND TEST PATTERN
0601	9214	JMP	LTSTC		/READ AND TEST COMPLEMENT
0602	7774	-4			
0603	7700	LM04,			
0604	0763	LM100,			/LO END TEST ROUTINE
0605	7570	KLENDT, LENDT			/HI END TEST ROUTINE
0606	0000	KL888, H888			/END TEST ROUTINE
0607	0000	LEND2, 0			/START TEST ADDRESS
0610	0000	LTSTAD, 0			/TEST 2 PAGES
0611	0000	LCNT6, 0			/TEST 4 ADDRESSES
0612	1000	LCNT7, 0			
0613	7600	KK1000, 1000			
		KC7600, 7600			
/READ AND TEST PATTERN CONTROL					
0614	4234	JMS	LRCON		/CORRECT READ CONSTANTS
0615	4252	JMS	LRMEM		/READ AND TEST PATTERN
0616	1252	TAD	LRMEM		/0XXX OR 7XXX
0617	1213	TAD	KC7600		/-200
0620	0213	AND	KC7600		
0621	7001	IAC			
0622	3207	DCA	LTSTAD		
0623	5607	JMP I	LTSTAD		/0401 OR 7201
/READ AND TEST COMPLEMENT PATTERN CONTROL					
0624	4234	JMS	LRCON		/CORRECT READ CONSTANTS
0625	4254	JMS	LRMEMC		/READ AND TEST COMPLEMENT PATTERN
0626	1254	TAD	LRMEMC		/0XXX OR 7XXX
0627	7006	7006			/RTL - AND ADDRESS OF TAG HPASS
0630	7630	SZL CLA			

```

0631 5627      JMP I      .-2      /PROG IN UPPER MEM
0632 5633      JMP I      .+1      /PROG IN LOWER MEM
0633 0206      /ADDRESS OF TAG LPASS

```

```

/
/UPDATE READ CONSTANTS
/

```

```

0634 0000      LRCON, 0      /0XXX OR 7XXX
0635 1234      TAD          .-1
0636 7004      RAL
0637 7630      SZL CLA
0640 5246      JMP          LRCON1 /PROG IN UPPER MEM
0641 1212      TAD          KK1000 /PROG IN LOWER MEM
0642 3207      DCA          LTSTAD /START TEST ADDRESS
0643 1204      TAD          KLENDT
0644 3206      DCA          LEND2
0645 5634      JMP I      LRCON /END MEM ROUTINE

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0646 1205      LRCON1, TAD      /END MEM ROUTINE
0647 3206      DCA          LEND2 /START TEST ADDRESS
0650 3207      DCA          LTSTAD
0651 5634      JMP I      LRCON

```

```

/
/READ AND TEST PATTERN OR PATTERN COMPLEMENT
/

```

```

0652 0000      LRMEN, 0      /READ AND TEST PATTERN
0653 5260      JMP          LR1010
0654 0000      LRMEN, 0
0655 1254      TAD          .-1 /STORE RETURN ADDRESS
0656 3252      DCA          LRMEN /READ AND TEST COMPLEMENT
0657 5311      JMP          LR0101

```

```

0660 1203      LR1010, TAD      /-100
0661 3210      DCA          LCNT6 /READ AND TEST 2 PAGES
0662 1202      TAD          LM04 /-4
0663 3211      DCA          LCNT7 /READ AND TEST 4 ADDRESSES
0664 1607      TAD I      LTSTAD
0665 7160      CMA STL
0666 3607      DCA I      LTSTAD
0667 1607      TAD I      LTSTAD
0670 7640      SZL CLA
0671 4352      JMS          LHALTC
0672 1607      TAD I      LTSTAD
0673 7040      CMA
0674 3607      DCA I      LTSTAD
0675 1607      TAD I      LTSTAD
0676 7101      IAC CLL
0677 7640      SZL CLA
0700 4342      JMS          LHALT
0701 2207      ISZ          LTSTAD
0702 7000      NOP
0703 2211      ISZ
0704 5264      JMP          LONE+2
0705 2210      ISZ          LCNT6

```

```

/TEST ONE COMPLEMENTED
/THIS LOC FAILED READ AND TEST

```

```

/TEST ONE
/THIS LOC FAILED READ AND TEST

```



```

7034 7004 RAL
7035 7630 SEL CLA
7036 2232 ISZ
7037 5632 JMP I HHILO

/RELOCATE PROGRAM TO UPPER MEMORY
/
HRELOU, JMS HRESBN
TAD C7200
DCA HCNT1
TAD C0200
DCA HCNT3
TAD C7000
DCA HCNT2
JMS HRELO
JMP I C7000

/RESTORE BIN INTO PAGE 31
/-600
/CONTROLS 600 TRANSFERS
/PAGE 1 CA
/PAGE 28 CA
/RELOCATE PROGRAM
/JMP TO PROG IN UPPER MEM

/RELOCATE PROGRAM TO LOWER MEMORY
/
HRELOD, JMS HSAVBN
TAD C7200
DCA HCNT1
TAD C0200
DCA HCNT2
TAD C7000
DCA HCNT3
JMS HRELO
JMP I C0200

/SAVE BIN INTO PAGE 0
/-600
/CONTROLS 600 TRANSFERS
/PAGE 1 CA
/PAGE 28 CA
/RELOCATE PROGRAM
/JMP TO PROG IN LOWER MEM

/SAVE BIN AND RIM INTO PAGE 0
/
HSAVBN, 0
TAD C7600
DCA HCNT1
DCA HCNT2
TAD C7600
DCA HCNT3
JMS HRELO
JMP I HSAVBN

/RESTORE BIN AND RIM INTO PAGE 31
/
HRESBN, 0
TAD C7600
DCA HCNT1
DCA HCNT3
TAD C7600
DCA HCNT2
JMS HRELO
JMP I HRESBN

/RELOCATE PROGRAM TO UPPER MEMORY
/
HRELOU, JMS HRESBN
TAD C7200
DCA HCNT1
TAD C0200
DCA HCNT3
TAD C7000
DCA HCNT2
JMS HRELO
JMP I C7000

/RESTORE BIN INTO PAGE 31
/-600
/CONTROLS 600 TRANSFERS
/PAGE 1 CA
/PAGE 28 CA
/RELOCATE PROGRAM
/JMP TO PROG IN UPPER MEM

/RELOCATE PROGRAM TO LOWER MEMORY
/
HRELOD, JMS HSAVBN
TAD C7200
DCA HCNT1
TAD C0200
DCA HCNT2
TAD C7000
DCA HCNT3
JMS HRELO
JMP I C0200

/SAVE BIN INTO PAGE 0
/-600
/CONTROLS 600 TRANSFERS
/PAGE 1 CA
/PAGE 28 CA
/RELOCATE PROGRAM
/JMP TO PROG IN LOWER MEM

/SAVE BIN AND RIM INTO PAGE 0
/
HSAVBN, 0
TAD C7600
DCA HCNT1
DCA HCNT2
TAD C7600
DCA HCNT3
JMS HRELO
JMP I HSAVBN

/RESTORE BIN AND RIM INTO PAGE 31
/
HRESBN, 0
TAD C7600
DCA HCNT1
DCA HCNT3
TAD C7600
DCA HCNT2
JMS HRELO
JMP I HRESBN

```

```
7102 0000 /RELOCATE SUBROUTINE
7103 1604 /
7104 3603 WRELO, 0
7105 1604 TAD I HCNT3 /TRANSFER FROM
7106 7041 DCA I HCNT2 /TRANSFER TO
7107 1603 TAD I HCNT3 /CHECK TRANSFER
7110 7640 CIA TAD I HCNT2
7111 4320 SZA CLA
7112 2204 JMS HXFERF /TRANSFER FAILED
7113 2203 ISE HCNT3 /INCREMENT FROM ADDRESS
7114 7000 ISE HCNT2 /INCREMENT TO ADDRESS
7115 2202 NOP
7116 9303 ISE HCNT1 /INCREMENT TRANSFER CONTROL
7117 5702 JMP WRELO+1
      JMP I HRELO /TRANSFER COMPLETE
```

```
7120 0000 /RELOCATION FAILURE HALT ROUTINE
7121 1604 HXFERF, 0
7122 7402 TAD I HCNT3 /1ST HALT - FROM DATA
7123 7200 HLT
7124 1204 CLA /
7125 7402 TAD HCNT3 /2ND HALT - FROM ADDRESS
7126 7200 HLT
7127 1603 CLA /
7128 7402 TAD I HCNT2 /3RD HALT - TO DATA
7129 7200 HLT
7130 7402 CLA /
7131 7200 TAD HCNT2 /4TH HALT - TO ADDRESS
7132 1203 HLT
7133 7402 CLA CUL
7134 7300 JMP I HXFERF
```

```
7136 2357 /TYPEOUT A '5' EVERY 5 MINUTES OF RUN TIME
7137 5214 /
7138 1360 HPASS, ISE HCNT
7139 3357 JMP HSR00 /NOT 5 MINUTES YET
7140 1360 TAD HM750
7141 3357 DCA HCNT /RESTORE COUNTER
7142 1361 TAD C215
7143 4351 JMS HTRANS /CR
7144 1362 TAD C212
7145 4351 JMS HTRANS /LF
7146 1363 TAD C265
7147 4351 JMS HTRANS /5
7148 5214 JMP HSR00
7151 0000 HTRANS, 0 /TRANSMIT CODE
7152 6046 TLS
```

7153	6041	TSF			
7154	5353	JMP	.-1	/WAIT FOR FLAG	
7155	7300	CLA CLL			
7156	5751	JMP I	HTRANS		
7157	6400	HCNT,	-1400	/COUNT 5 MINUTES	
7160	6400	HM750,	-1400		
7161	0215	C215,	215	/CR	
7162	0212	C212,	212	/LF	
7163	0265	C265,	265	/5	
/GO TO PAGE 2 OR PAGE 29					
7164	4365	JMS	.*1	/0XXX OR 7XXX	
7165	0000	0			
7166	7300	CLA CLL			
7167	1365	TAD	.-2		
7170	1211	TAD	C0200		
7171	0201	AND	C7600		
7172	3205	DCA	HINAD1		
7173	5605	JMP I	HINAD1	/0400 OR 7200	
7200					
7200	5216	JMP	HWR	/WRITE PATTERN	
7201	5225	JMP	HWR	/WRITE COMPLEMENT	
7202	7774	-4			
7203	7740	-40			
7204	0523	CHENDM,	LENDM	/LO END MEM ROUTINE	
7205	7330	CHAAA,	HAAA	/HI END MEM ROUTINE	
7206	0000	HEND1,	0	/END MEM ROUTINE	
7207	0000	HADD,	0	/START WRITE ADDRESS	
7210	0000	HCNT4,	0	/WRITE 2 PAGES	
7211	0000	HCNT5,	0	/WRITE 4 ADDRESSES	
7212	0200	CC0200,	0200		
7213	1000	C1000,	1000		
7214	7600	CC7600,	7600		
7215	0000	HINAD2,	0	/INDIRECT ADDRESSING	
/WRITE PATTERN INTO MEMORY					
7216	4235	HWR,			
7217	4253	JMS	HWCN	/CORRECT WRITE CONSTANTS	
7220	1253	JMS	HWRNEM	/WRITE PATTERN	
7221	1212	TAD	HWRNEM	/0XXX OR 7XXX	
7222	0214	AND	CC0200		
7223	3215	DCA	CC7600		
7224	5615	JMP I	HINAD2	/0600 OR 7400	
/WRITE COMPLEMENT PATTERN INTO MEMORY					
7225	4235	HWR,			
7226	4255	JMS	HWCN	/CORRECT WRITE CONSTANTS	
		JMS	HWRNEM	/WRITE COMPLEMENT PATTERN	

/INCREMENT MEMORY ADDRESS

7303 3607 DCA I HMADD
7304 2207 ISZ HMADD
7305 7000 NOP
7306 2211 ISZ HCNT5
7307 5303 JMP HWZERO+3
7310 5700 JMP I HWZERO

7311 0000 HNONE, 0
7312 1202 TAD HM4
7313 3211 DCA HCNT5
7314 7240 STA
7315 3607 DCA I HMADD
7316 2207 ISZ HMADD
7317 7000 NOP
7320 2211 ISZ HCNT5
7321 5314 JMP HNONE+3
7322 5711 JMP I HNONE

/INCREMENT MEMORY ADDRESS

/CHECK FOR END OF MEMORY
/ HENDM, 0

7323 0000
7324 1207 TAD HMADD
7325 7640 SZA CLA
7326 5723 JMP I HENDM
7327 5653 JMP I HWRMEM
7330 0000 HAAA, 0
7331 1207 TAD HMADD
7332 1213 TAD C1000
7333 7640 SZA CLA
7334 5730 JMP I HAAA
7335 5653 JMP I HWRMEM

/TWO SPECIAL SCOPE LOOPS
/ HSCOP1, LAS

7336 7604 DCA I HSWADD
7337 3372 DCA I HSWADD
7340 1772 TAD I HSWADD
7341 0772 AND I HSWADD
7342 0772 AND I HSWADD
7343 0772 AND I HSWADD
7344 0772 AND I HSWADD
7345 0772 AND I HSWADD
7346 7040 CMA I HSWADD
7347 3772 DCA I HSWADD
7350 1772 TAD I HSWADD
7351 0772 AND I HSWADD
7352 0772 AND I HSWADD
7353 0772 AND I HSWADD
7354 0772 AND I HSWADD
7355 0772 AND I HSWADD
7356 7040 CMA I HSWADD
7357 3772 DCA I HSWADD

/TEST ADDRESS

7360	5336	JMP	HSCOP1		
7361	7604	HSCOP2,	LAS		/TEST ADDRESS
7362	3372	DCA	HSWADD		
7363	1772	TAD I	HSWADD		
7364	7040	CMA			
7365	3772	DCA I	HSWADD		
7366	1772	TAD I	HSWADD		
7367	7040	CMA			
7370	3772	DCA I	HSWADD		
7371	5361	JMP	HSCOP2		
7372	0000	HSWADD,	0		
7400	7400	JMP	HTST		/READ AND TEST PATTERN
7401	5214	JMP	HTSTC		/READ AND TEST COMPLEMENT
7402	7774	-4			
7403	7700	HM04,			
7404	0763	HM100,			
7405	7570	CHENDT,	LENDT		/LO END TEST ROUTINE
7406	0000	CHBBB,	HBBB		/HI END TEST ROUTINE
7407	0000	HEND2,	0		/END TEST ROUTINE
7410	0000	HTSTAD,	0		/START TEST ADDRESS
7411	0000	MCNT6,	0		/TEST 2 PAGES
7412	1000	MCNT7,	0		/TEST 4 ADDRESSES
7413	7600	CC1000,	1000		
		CK7600,	7600		
/READ AND TEST PATTERN CONTROL					
7414	4234	HTST,	JMS	HRCON	/CORRECT READ CONSTANTS
7415	4252	JMS	HRMEM		/READ AND TEST PATTERN
7416	1252	TAD	HRMEM		/0XXX OR 7XXX
7417	1213	TAD	CK7600		/-200
7420	0213	AND	CK7600		
7421	7001	IAC			
7422	3207	DCA	HTSTAD		/0401 OR 7201
7423	5607	JMP I	HTSTAD		
/READ AND TEST COMPLEMENT PATTERN CONTROL					
7424	4234	HTSTC,	JMS	HRCON	/CORRECT READ CONSTANTS
7425	4254	JMS	HRMEMC		/READ AND TEST COMPLEMENT PATTERN
7426	1254	TAD	HRMEMC		/0XXX OR 7XXX
7427	7006	7006			/RTL - AND ADDRESS OF TAG HPASS
7430	7630	SEL CLA			
7431	5627	JMP I	.-2		/PROG IN UPPER MEM
7432	5633	JMP I	.-1		/PROG IN LOWER MEM
7433	0206	0206			/ADDRESS OF TAG LPASS
/UPDATE READ CONSTANTS					

Address	Instruction	Comment
7434	HRCON, 0	
7435	TAD	
7436	RAL	
7437	SZL CLA	
7440	JMP	HRCON1
7441	TAD	CC1000
7442	DCA	HTSTAD
7443	TAD	CHENDT
7444	DCA	HEND2
7445	JMP I	HRCON
7446	TAD	CHBBB
7447	DCA	HEND2
7448	DCA	HTSTAD
7451	JMP I	HRCON
7452	HRMEM, 0	
7453	JMP	HR1010
7454	HRMEMC, 0	
7455	TAD	
7456	DCA	HRMEM
7457	JMP	HR0101
7460	HR1010, TAD	
7461	DCA	HCNT6
7462	TAD	HM04
7463	DCA	HCNT7
7464	TAD I	HTSTAD
7465	CHA STL	
7466	DCA I	HTSTAD
7467	TAD I	HTSTAD
7470	SZA CLA	
7471	JMS	HALTC
7472	TAD I	HTSTAD
7473	GMA	
7474	DCA I	HTSTAD
7475	TAD I	HTSTAD
7476	IAC CLL	
7477	SZA CLA	
7500	JMS	HALT
7501	ISE	HTSTAD
7502	NOP	
7503	ISE	HCNT7
7504	JMP	HONE+2
7505	ISE	HCNT6
7506	JMP	HZERO
7507	JMS I	HEND2
7510	JMP	HR1010
7511	HR0101, TAD	
7512	DCA	HCNT6
7513	TAD	HM04

```
7514 3211 DCA HCNT7
7515 1607 HZER01, TAD I HTSTAD
7516 7040 CMA
7517 3607 DCA I HTSTAD
7520 1607 TAD I HTSTAD
7521 7121 IAC STL
7522 7640 SZA CLA
7523 4352 JMS HHALTC
7524 1607 TAD I HTSTAD
7525 7140 CMA CLL
7526 3607 DCA I HTSTAD
7527 1607 TAD I HTSTAD
7530 7640 SZA CLA
7531 4342 JMS HHALT
7532 2207 ISE HTSTAD
7533 7000 NOP
7534 2211 ISE
7535 5315 JMP HZER0+2
7536 2210 ISE HCNT6
7537 5262 JMP HONE
7540 4606 JMS I HEND2
7541 5311 JMP HR0101
```

/READ AND TEST 4 ADDRESSES

/TEST ZERO COMPLEMENTED
/THIS LOC FAILED READ AND TEST

/TEST ZERO
/THIS LOC FAILED READ AND TEST

/END OF MEMORY?
/NO

```
7542 0000 /ERROR HALT ROUTINE FOR DATA FAILURE
7543 1607 HHALT, 0
7544 7402 TAD I HTSTAD
7545 7200 HLT
7546 1207 CLA
7547 7402 TAD HTSTAD
7550 7200 HLT
7551 5742 CLA
JMP I HHALT
```

/1ST HALT = BAD DATA

/2ND HALT = BAD LOCATION

```
7552 0000 /ERROR HALT ROUTINE FOR COMPLEMENT DATA FAILURE
7553 1607 HHALTC, 0
7554 7040 TAD I HTSTAD
7555 7402 CMA
7556 7200 HLT
7557 1207 CLA
7560 7402 TAD HTSTAD
7561 7300 HLT
7562 5752 CLA CLL
JMP I HHALTC
```

/1ST HALT = BAD DATA

/2ND HALT = BAD LOCATION

```
7563 0000 /END OF MEMORY ROUTINE
7564 1207 HENDT, 0
7565 7640 TAD HTSTAD
7566 5763 SZA CLA
JMP I HENDT
```

/MORE MEMORY TO TEST

7567	5652	JMP I	HRMEM	/END OF TEST
7570	0000	0		
7571	1207	TAD	HTSTAD	
7572	1212	TAD	CC1000	
7573	7640	SZA	CLA	
7574	5770	JMP I	HBBB	/MORE MEMORY TO TEST
7575	5652	JMP I	HRMEM	/END OF TEST
		\$		

0000	11110000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0100	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
0200	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0300	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11110000
0400	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0500	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11100000
0600	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111
0700	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111100

1000
1100

1200
1300

1400
1500

1600
1700

2000
2100

2200
2300

2400
2500

2600
2700

3000
3100

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5000
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LWZERO 0500
LXFERF 0320
LZERO 0713
LZER01 0715

C0200	7011	HRESBN	7072	LCNT6	0610
C1000	7213	HRMEM	7452	LCNT7	0611
C212	7162	HRMEMC	7454	LEND1	0406
C215	7161	HSABVN	7062	LEND2	0606
C265	7163	HSCOP1	7336	LENDM	0523
C7000	7012	HSCOP2	7361	LENDT	0763
C7200	7013	HSR00	7014	LGOP2	0364
C7600	7001	HSR07	7023	LHALT	0742
CC0200	7212	HSW0	7007	LHALTC	0752
CC1000	7412	HSW7	7010	LHILO	0232
CC7600	7214	HSWADD	7372	LINAD1	0205
CHAAA	7205	HTRANS	7151	LINAD2	0415
CH888	7405	HTST	7414	LM04	0602
CHENDM	7204	HTSTAD	7407	LM100	0603
CHENDT	7404	HTSTC	7424	LM4	0402
CK7600	7413	HW0101	7270	LM40	0403
HAAA	7330	HW1010	7261	LM750	0360
H888	7570	HWCON	7235	LMADD	0407
HCNT	7157	HWCON1	7247	LONE	0662
HCNT1	7002	HWONE	7311	LONE1	0664
HCNT2	7003	HWRC	7216	LPASS	0336
HCNT3	7004	HWRC	7225	LR0101	0711
HCNT4	7210	HWRC	7255	LR1010	0660
HCNT5	7211	HWRC	7253	LRCON	0634
HCNT6	7410	HWZERO	7300	LRCON1	0646
HCNT7	7411	HXFERF	7120	LRLO	0302
HEND1	7206	HZERO	7513	LRLO0	0251
HEND2	7406	HZERO1	7515	LRLOU	0240
HENDM	7323	K0200	0211	LRSEBN	0272
HENDY	7563	K1000	0413	LRMEM	0652
HGOP2	7164	K212	0362	LRMEMC	0654
HHALT	7542	K215	0361	LSABVN	0262
HHALTC	7552	K265	0363	LSCOP1	0536
HHILO	7032	K7000	0212	LSCOP2	0561
HINAD1	7005	K7200	0213	LSR00	0214
HINAD2	7215	K7600	0201	LSR07	0223
HM04	7402	KC7600	0613	LSW0	0207
HM100	7403	KK0200	0412	LSW7	0210
HM4	7202	KK1000	0612	LSWADD	0572
HM40	7203	KK7600	0414	LTRANS	0351
HM750	7160	KLAAA	0405	LTST	0614
HMA00	7207	KL888	0605	LTSTAD	0607
HONE	7462	KL888	0404	LTSTC	0624
HONE1	7464	KLENDM	0604	LW0101	0470
HPASS	7136	KLENDT	0604	LW1010	0461
HR0101	7511	LAAA	0530	LWCON	0435
HR1010	7460	LB88	0770	LWCON1	0447
HRCON	7434	LCNT	0357	LWONE	0511
HRCON1	7446	LCNT1	0202	LWR	0416
HRELO	7102	LCNT2	0203	LWRC	0425
HRELO0	7051	LCNT3	0204	LWRMC	0455
HRELOU	7040	LCNT4	0410	LWRMEM	0453
		LCNT5	0411		

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 9 SECONDS

3K CORE USED

