

1. IDENTIFICATION

1.1 Maindec 825

1.2 680 Static Test

1.3 October 22, 1965

2. ABSTRACT

The 680 Static Test verifies correct operation of the 681 and 685 circuits associated with the 680 Data Communications System in a static state. That is, the program does not actually transmit characters, but tests only the logical operation of the hardware. Hardware malfunctions detected by the program result in a processor halt.

3. REQUIREMENTS

3.1 Storage

Test or Routine	Starting Address	End Address
Interrupt Routine	0000	0002
End of Test	0030	0070
Common Display Halt	0074	0107
Line Register Test	0200	0324
TTI Test	0400	0475
TTO TTI Test	0600	0726
Shift the MB Test and	1000	1176
Shift the MB Subroutine	0730	0772
Clock Test	1200	1361
Power Clear Test	1400	1434

3.2 Subprograms and/or subroutines

None

3.3 Equipment

Minimum configuration PDP-8
680 DCS hardware

* 3.4 Miscellaneous (NB)

Jumper wire from location LMBI-H to LMBI-U on the 685 Panel. (Input to output of line 0).

4. USAGE

4.1 Loading

4.1.1 If the RIM Loader starting at address 7777 is in memory, go to paragraph 4.1.2. Otherwise, the RIM Loader must be loaded into memory.

The 680 Static Test may now be loaded into memory as follows:

4.1.2 Set 7777 in the SWITCH REGISTER.

4.1.3 Press LOAD ADDRESS key.

4.1.4 Place the 680 Static Test in the keyboard reader.

4.1.5 Press the START key on the operator console.

4.1.6 Engage the keyboard reader.

4.3 Switch Settings

Switch 0 - up - cycle all tests except Power Clear Test.

Switch 1 - up - repeat current test (switch 0 overrides switch 1).

Switches 0 and 1 - down - halt at completion of current test and repeat current test if CONTINUE or START is pressed.

Switches 10 and 11 - Indicate which clock to test

00 - Clock 1

U40 → 01 - Clock 2

10 - Clock 3

11 - Clock 4

4.4 Start up and/or Entry

4.4.1 Line Register Test

Set the SWITCH REGISTER to 0200₈

Press LOAD ADDRESS

Press START

4.4.2 TTI Test

Set the SWITCH REGISTER to 0400₈

Press LOAD ADDRESS

Press START

4.4.3 TTO and TTI Test

Set the SWITCH REGISTER to 0600₈

Press LOAD ADDRESS

Press START

4.4.4 Shift the MB Test

Set the SWITCH REGISTER to 1000₈

Press LOAD ADDRESS

Press START

4.4.5 Clock Test

Set the SWITCH REGISTER to 1200₈

Press LOAD ADDRESS

Set switches 10 and 11 to select the appropriate clock

Press START

4.4.6 To cycle through all of the above tests

Set the SWITCH REGISTER to 0200₈

Press LOAD ADDRESS

Set switch 0 - up

Set switches 10 and 11 to select the appropriate clock

Press START

4.4.7 To cycle any of the above tests by itself
Set the SWITCH REGISTER to the appropriate address
Press LOAD ADDRESS
Set switch 1 - up
Press START

4.4.8 Power Clear Test
Set the SWITCH REGISTER to 1400₈
Press LOAD ADDRESS
Press START
The processor will halt at address 1407
Press START
The processor will halt at address 1433

4.5 Errors in Usage

If the program detects a hardware malfunction, the result will be a processor halt.

4.5.1 ADDRESS 0077 COMMON DISPLAY HALT

The processor will halt with the error address displayed in the AC. Press CONTINUE and the processor will halt at address 102 with the contents of memory address 11 displayed in the AC. Press CONTINUE again, and the processor will halt at address 107 with the contents of memory address 10 displayed in the AC.

The address in the AC on the first halt indicates the type of error.

The contents of the AC on the second halt indicates the correct information as it pertains to the type of error.

The contents of the AC on the third halt indicates the incorrect information as it pertains to the type of error.

4.5.2 Non-Error Halts

ADDRESS 0054	END OF TEST
ADDRESS 1407	POWER CLEAR TEST, WAIT FOR START KEY
ADDRESS 1433	END OF POWER CLEAR TEST

4.5.3 Error Table

The following is a list of error halts included in the program:

ERROR TABLE

Address of Halt	Contents of AC	Error Description
0077	0246	TTSL ERROR
0102	0XXX	LINE REGISTER SHOULD EQUAL
0107	0XXX	LINE REGISTER READ BACK

ERROR TABLE (continued)

Address of Halt	Contents of AC	Error Description
0077	0277	TTINCR ERROR
0102	0XXX	LINE REGISTER SHOULD EQUAL
0107	0XXX	LINE REGISTER READ BACK
0077	0316	TTINCR ERROR
0102	0XXX	LINE REGISTER SHOULD EQUAL
0107	0XXX	LINE REGISTER READ BACK
0077	1170	SHIFT THE MB ERROR
0102	XXXX	CHARACTER ASSEMBLY WORD SHOULD EQUAL
0107	XXXX	CHARACTER ASSEMBLY WORD DOES EQUAL
0203		IOT 6410 (TT DO NOTHING) CLEARED THE AC
0206		IOT TTSL DID NOT CLEAR THE AC
0212	0XXX	IOT TTCL DID NOT CLEAR THE LINE REGISTER OR IOT TTRL DID NOT READ BACK CORRECTLY
0224		IOT TTSL DID NOT SET THE LR TO 177 ₈ OR IOT TTRL DID NOT READ BACK 177 ₈
0230		A SECOND TTSL CLEARED THE LINE REGISTER
0254		IOT TTINCR OPERATED AS A TTI INSTRUCTION AND SKIPPED LOCATIONS
0256		IOT TTINCR DID NOT INCREMENT THE LINE REGISTER FROM 177 to 000
0412		IOT TTI DID NOT SKIP
0416		IOT TTI (SAME TTI AS 0412) ONLY SKIPPED 1 LOCATION
0427	XXXX	IOT TTI STATUS WORD = 0000 ALTERED THE STATUS WORD
0432	XXXX	IOT TTI (SAME TTI AS 0426) ALTERED THE CHARACTER ASSEMBLY WORD

ERROR TABLE (continued)

Address of Halt	Contents of AC	Error Description
0440		IOT TTI SHIFTED THE AC
0442		IOT TTI (SAME TTI AS 0437) CLEARED THE LINK
0456		IOT TTI STATUS WORD = 4000 STATUS WORD WAS NOT INCREMENTED TO 4001
0461	XXXX	IOT TTI (SAME TTI AS 0455) ALTERED THE CHARACTER ASSEMBLY WORD
0470		IOT TTI INCREMENTED THE LINE REGISTER
0604		IOT TTO SKIPPED 1 LOCATION
0605		IOT TTO (SAME TTO AS 0604) SKIPPED 2 LOCATIONS
0607		IOT TTO (SAME TTO AS 0604) DID NOT SHIFT THE AC
0612		IOT TTO (SAME TTO AS 0604) CAUSED THE LINE REGISTER TO INCREMENT
0621		IOT TTO OR TTI (SAME TTO AS 0604) TTO DID NOT SET LINE 0 TO A 1 OR TTI DID NOT COMPLEMENT LINE 0 INTO THE STATUS WORD
0625		IOT TTO (LINK = 1 AC = 0) AC NOT SHIFTED PROPERLY, PROBABLY TTO DID NOT CLEAR LINK
0635	MAKE SURE JUMPER BIH TO BIU ON 685 IS INSTALLED.	IOT TTO OR TTI (SAME TTO AS 0624) TTO DID NOT SET LINE 0 TO A 0 OR TTI DID NOT COMPLEMENT LINE 0 INTO THE STATUS WORD
0637		IOT TTI (SAME TTI AS 0635) STATUS WORD IS OTHER THAN 0000 OR 4000
0652		IOT TTI (STATUS WORD 4003) STATUS WORD DID NOT INCREMENT TO 4004
0655		IOT TTI (SAME TTI AS 0652) CHARACTER ASSEMBLY WORD NOT ZEROS

ERROR TABLE (continued)

Address of Halt	Contents of AC	Error Description
0671		IOT TTO OR TTI (STATUS WORD 4003) TTO DID NOT SET LINE 0 TO A 1 OR TTI DID NOT INPUT LINE 0 INTO THE CHARACTER ASSEMBLY WORD
0673		IOT TTI (SAME TTI AS 0671) CHARACTER ASSEMBLY WORD WAS OTHER THAN 0000 OR 4000
0702		IOT TTI (STATUS WORD 4001) TTI ONLY SKIPPED 1 LOCATION
0711		IOT TTI (STATUS WORD 4002) TTI ONLY SKIPPED 1 LOCATION
0720		IOT TTI (STATUS WORD 4007) TTI ONLY SKIPPED 1 LOCATION
1243		CLOCK SKIP SKIPPED IN ERROR
1252		INTERRUPT WAS RECEIVED WITH THE CLOCK FLAG OFF
1260	MAKE SURE CORRECT SW'S SET, UNFOR CLOCK 2 = SW 11	CLOCK FLAG DID NOT SET WITHIN 12 MSEC OR THE CLOCK SKIP IOT DID NOT SKIP
1265		INTERRUPT WAS NOT RECEIVED WITH THE CLOCK FLAG ON
1274		CLOCK ON IOT DID NOT CLEAR THE CLOCK FLAG
1301		CLOCK FLAG DID NOT SET WITHIN 12 MSEC
1305		CLOCK OFF IOT DID NOT CLEAR THE CLOCK FLAG
1313		CLOCK FLAG SET AGAIN AFTER A CLOCK OFF IOT
1316		CLOCK 1 FLAG IS SET
1321		CLOCK 2 FLAG IS SET
1324		CLOCK 3 FLAG IS SET
1332		CLOCK 4 FLAG IS SET
1416		LINE 0 WAS NOT RETURNED TO THE 1 STATE
1421		CLOCK 1 WAS NOT TURNED OFF
1424		CLOCK 2 WAS NOT TURNED OFF
1427		CLOCK 3 WAS NOT TURNED OFF
1432		CLOCK 4 WAS NOT TURNED OFF

4.6 Recovery from Such Errors

Pressing CONTINUE will cause the program to proceed to the next test sequence. However, hardware malfunctions should be repaired as soon as they are detected or erroneous indications may be given in later tests.

5. RESTRICTIONS (Not Applicable)

6. DESCRIPTION

6.1 Discussion

The 680 Static Test consists of several routines that each verify a logical operation of the 681 and 685 hardware. The routines may be run individually or progressively. The output of line 0 must be tied into its own input. Hardware malfunctions detected by the program result in a processor halt.

6.1.1 Test Descriptions

6.1.1.1 Line Register Test (Starting address 200)

The Line Register portion of the 680 Static Test exercises the IOT's associated with line register manipulations and verifies their correct operation.

The IOT's tested are:

<u>Octal</u>	<u>Mnemonic</u>	<u>Description</u>
6410		TT DO NOTHING
6411	TTCL	CLEAR THE LINE REGISTER
6412	TTSL	SET THE LINE REGISTER
6414	TTRL	READ THE LINE REGISTER
6401	TTINCR	INCREMENT THE LINE REGISTER
6413	TTSL+1	CLEAR THEN SET THE LINE REGISTER

6.1.1.2 TTI Test (Starting address 400)

The TTI portion of the 680 Static Test exercises the TTI IOT with the assumption that line 0 is set to the 1 state. This test verifies that the TTI IOT skips 2 locations, that the status and character assembly words are not altered, that the TTI does not shift the AC or clear the LINK, that a status word of 4000 is incremented, and that TTI does not increment the line register.

6.1.1.3 TTO and TTI Test (Starting address 600)

The TTO and TTI portion of the 680 Static Test manipulates line 0 with the TTO IOT and further verifies the correct operation of the TTI IOT. This test verifies that the TTO IOT shifts the AC, changes line 0 from the 1 to the 0 state and back again and that TTO does not skip locations or increment the line register. It also verifies that the TTI IOT reads the complement of line 0 into the status word and line 0 into the character assembly word. The test verifies that status words of 4001, 4002, and 4007 do not appear to be a status word of 4003.

6.1.1.4 SHIFT THE MB TEST (Starting address 1000)

This portion of the 680 Static Test verifies that the logic which shifts the MB will shift all combinations of bits.

6.1.1.5 CLOCK TEST (Starting address 1200. Switches 10 and 11 indicate which clock)

This portion of the 680 Static Test verifies that the clock IOT's function correctly in that they will turn on the appropriate clock without turning on any of the other clocks and that they will turn off the appropriate clock. The program also verifies the skip and interrupt functions.

6.1.1.6 POWER CLEAR TEST (Starting address 1400)

This portion of the 680 Static Test verifies correct operation of the power clear function. The program sets line 0 to a 0 state, turns on all of the clocks, and then halts. Press START, and the program verifies that line 0 is returned to the 1 state and all clocks are turned off. It is not included as one of the tests that are run with SW0 up.

- 7. METHODS (Not Applicable)
- 8. FORMAT (Not Applicable)
- 9. EXECUTION TIME (Not Applicable)

10. PROGRAM

10.4 Program Listing

```

/STATIC TEST PDP-8 680
/TYPE 680 TELETYPE LINE MUX

/THE OUTPUT OF LINE 0
/MUST BE JUMPERED TO IIS
/OWN INPUT

/IOT DEFINITIONS
TTI=6402           /TELETYPE INPUT COMMAND
TTO=6404           /TELETYPE OUTPUT COMMAND
TTCL=6411          /CLEAR LINE REGISTER
TTTL=6414          /READ LINE REGISTER
TTSL=6412          /SET LINE REGISTER
TTINCR=6401        /INCREMENT LINE REGISTER

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/STARTING ADDRESSES OF TESTS

/POWER CLEAR TEST 1400

/CLOCK IOT'S

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TTION=6424
TTIOFF=6422
TT1SKP=6421
TT2ON=6434
TT2OFF=6432
TT2SKP=6431
TT3ON=6444
TT3OFF=6442
TT3SKP=6441
TT4ON=6454
TT4OFF=6452
TT4SKP=6451

```

/SW0 = CYCLE ALL TESTS

/SW1 = REPEAT CURRENT TEST

/BOTH DOWN, STOP, REPEAT CURRENT TEST

/INTERRUPT ROUTINE

*1

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0001 5402      JMP I .+1      /GO TO INTERRUPT
0002 0001      .-1           /FOR INTERRUPT POINTER

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/END OF TEST ROUTINE

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*30
0030 5030      ENDIST,      JMP .      /FOR JMS
0031 7200      CLA          /ZERO AC
0032 1030      IAD .-2      /GET RETURN ADDRESS
0033 0056      AND ONESIX /CLR TO PAGE NUMBER
0034 7112      CLL RTR      /POSITION
0035 7012      RTR          /PAGE NUMBER
0036 7012      RTR          /OVER
0037 7010      RAR          /7 BITS

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0040	1061		TAD TSPNTR /GENERATE CURRENT TEST POINTER	
0041	3060		DCA ONESIX+2	/SAVE IT FOR INDIRECT
0042	1460		TAD I ONESIX+2	/GET START CURRENT TEST
0043	3057		DCA ONESIX+1	/FOR RESTART
0044	2060		ISZ ONESIX+2	/ADVANCE TO GET NEXT TEST
0045	1460		TAD I ONESIX+2	/GET NEXT TEST POINTER
0046	3060		DCA ONESIX+2	/FOR START NEXT TEST
0047	7404		OSR	/GET SWITCHES
0050	7510		SPA	/START NEXT TEST SET?
0051	5460		JMP I ONESIX+2	/YES
0052	0070		AND FORTIST /CLR TO BIT 1	
0053	7450		SNA	/NOT STOP SET?
0054	7402		HLT	/HALT, WAIT START
0055	5457		JMP I ONESIX+1	/RESTART CURRENT TEST
0056	1600	ONESIX,	1600	
0057	0000		0	/RESTART TEST ADDRESS
0060	0000		0	/START NEXT TEST POINTER
0061	0061	TSPNTR,	.	/CONSTANT AND PAGE NO.IS TE
0062	0200		LINREG	/START LINE REGISTER TEST
0063	0400		TSITI	/START ITI TEST
0064	0600		ISTIO	/START TIO ITI TEST
0065	1000		SHIFMB	/START SHIFT THE MB TEST
0066	1200		CLOCK	/START CLOCK TEST
0067	0200		LINREG	/RESTART LINE REGISTER TEST
0070	2000	FORTIST,	2000	/FOR ANDING SWI

/ERROR HALT DATA ERROR

0074	5074	*74	
0075	7200	ERROR,	JMP .
0076	1074		CLA
0077	7402		TAD .-2
0100	7200		HLT
0101	1011		CLA
0102	7402		TAD Z 11
0103	7200		HLT
0104	1010		CLA
0105	7402		TAD Z 10
0106	7200		HLT
0107	5474		CLA
			JMP I ERROR

/TYPE 680 STATIC TEST

/LINE REGISTER TEST

/PAGE 1, ADDRESS 200

0200	7240	*200	
0201	6410	LINREG,	CLA CMA
0202	7450		6410
0203	7402		SNA
0204	6412		HLT
0205	7440		TTSL
0206	7402		SZA
0207	6411		HLT
0210	6414		TTCL
0211	7440		TTRL
0212	7402		SZA
0213	1322		HLT
			TAD ONE77

/SET ONES IN AC

/IT DO NOTHING

/DO NOTHING CLEAR AC

/YES, ERROR 1

/TTSL SHOULD CLEAR AC

/DID IT

/NO, ERROR 2

/CLEAR LINE REGISTER

/READ LINE REGISTER

/LINE REGISTER CLEAR

/NO, ERROR 3

/0177

0214	6412	TTSL	/SET LINE REGISTER
0215	6414	TTRL	/READ LINE REGISTER
0216	3010	DCA Z 10	/SAVE READ BACK
0217	1010	TAD Z 10	
0220	7040	CMA	/COMPLEMENT READ BACK
0221	1322	TAD ONE77	/AC SHOULD = -1
0222	7040	CMA	/COMPLIMENT IT
0223	7440	SZA	/ALL BITS COME BACK
0224	7402	HLT	/NO, ERROR 4
0225	6412	TTSL	/SHOULD NOT CLEAR LR
0226	6414	TTRL	/READ LINE REGISTER
0227	7650	SNA CLA	/DID SECOND TTSL CLEAR LR
0230	7402	HLT	/YES, ERROR 5
0231	3011	DCA Z 11	/SET 11 TO 0
0232	1323	TAD K128	/-128
0233	3012	DCA Z 12	/FOR COUNTING
0234	1011	TAD Z 11	/GET NEXT CONSTANT TO SET
0235	6413	TTSL+1	/CLR LR THEN SET IT
0236	6414	TTRL	/READ LR
0237	3010	DCA Z 10	/SAVE READ BACK
0240	1010	TAD Z 10	
0241	7040	CMA	/COMPLEMENT READ BACK
0242	1011	TAD Z 11	/AC SHOULD BE -1
0243	7040	CMA	/AC SHOULD BE 0
0244	7440	SZA	/READ BACK WHAT WAS SENT
0245	4074	JMS Z ERROR	/NO, ERROR 6
0246	2011	ISZ Z 11	/ADVANCE TO NEXT LINE
0247	2012	ISZ Z 12	/TESTED ALL LINE NUMBERS
0250	5234	JMP SETLOP	/NO, TEST NEXT LINE NUMBER
0251	6401	TTINCR	/INCREMENT LINE REGISTER
0252	6414	TTRL	/LINE REGISTER SHOULD BE 0
0253	7410	SKP	/SKIP
0254	7402	HLT	/ERROR 7, TTINCR PUT US HERE
0255	7440	SZA	/LINE REGISTER ALL ZEROS
0256	7402	HLT	/NO, ERROR 8
0257	3011	DCA Z 11	/CLEAR 11
0260	3012	DCA Z 12	/CLEAR 12
0261	1324	TAD K127	/-127
0262	3013	DCA Z 13	
0263	2011	ISZ Z 11	/11 SHOULD = LR AFTER TTINCR
0264	1012	TAD Z 12	/12 IS LR BEFORE TTINCR
0265	6413	TTSL+1	/CLEAR LR AND SET IT
0266	6401	TTINCR	/INCREMENT LR
0267	6414	TTRL	/READ LR
0270	3010	DCA Z 10	/SAVE READ BACK
0271	1010	TAD Z 10	
0272	7040	CMA	/COMPLEMENT READ BACK
0273	1011	TAD Z 11	/ADD CORRECT READ BACK
0274	7040	CMA	/AC SHOULD BE ZEROS
0275	7440	SZA	/LR INCREMENT CORRECTLY
0276	4074	JMS Z ERROR	/NO, ERROR 9
0277	2012	ISZ 12	/SET NEXT LINE NUMBER
0300	2013	ISZ 13	/TESTED ALL LINE NUMBERS
0301	5263	JMP INCLOP /NO	
0302	3011	DCA 11	
0303	1324	TAD K127	/-127
0304	3012	DCA 12	

0305	6401	INCL2,	TIINCR	/ INCR LR
0306	6414	TTRL		/READ LR
0307	3010	DCA Z 10		/SAVE READ BACK
0310	1010	TAD Z 10		
0311	7040	CMA		/COMPLEMENT READ BACK
0312	1011	TAD Z 11		/ADD CORRECT LINE NO
0313	7040	CMA		/AC SHOULD BE ZERO
0314	7440	SZA		/LR INCREMENT OK
0315	4074	JMS Z ERROR		/NO, ERROR
0316	2011	ISZ Z 11		/11 = LR AFTER TIINCR
0317	2012	ISZ Z 12		/TESTED INCR. TO 177
0320	5305	JMP INCL2		
0321	4030	JMS Z ENDIST		/END LINE REG TES

0322	0177	ONE77,	0177	
0323	7600	K128,	7600	/-128
0324	7601	K127,	7601	/-127

/INITIAL TTI TEST

/PAGE 2 ADDRESS 400

*400				
0400	7201	TSTTTI,	CLA IAC	/CLEAR AC TO +1
0401	3272		DCA FORISZ	/SET IN TEST LOCATION
0402	1202		TAD .	/RESET INSTRUCTIONS
0403	3207		DCA .+4	/THAT TEST TTI
0404	1273		TAD FORPL2	/JUST IN CASE OF
0405	3210		DCA .+3	/A PREVIOUS DISASTER
0406	6402		TTI	
0407	0000		0	/TAD INSTR
0410	0000		0	/ISZ INSTR
0411	7440		SZA	/WAS TAD EXECUTED
0412	7402		HLT	/YES, ERROR
0413	7240		CLA CMA	/SET AC = -1
0414	1272		TAD FORISZ	/ADD TEST LOCATION
0415	7440		SZA	/WAS ISZ EXECUTED
0416	7402		HLT	/YES, ERROR
0417	6411		TTCL	/SET TO LINE 0
0420	3223		DCA .+3	
0421	3224		DCA .+3	
0422	6402		TTI	
0423	0000		0	
0424	0000		0	
0425	1223		TAD .-2	
0426	7440		SZA	/DID TTI CHANGE TTI +1
0427	7402		HLT	/YES, ERROR
0430	1224		TAD .-4	
0431	7440		SZA	/DID TTI CHANGE TTI +2
0432	7402		HLT	/YES, ERROR
0433	7121		STL IAC	/SET AC = 1 SET LINK
0434	6402		TTI	
0435	0000		0	
0436	0000		0	
0437	7450		SNA	/DID TTI SHIFT THE AC
0440	7402		HLT	/YES, ERROR
0441	7420		SNL	/DID TTI CLEAR THE LINK
0442	7402		HLT	/YES, ERROR
0443	7200		CLA	
0444	1274		TAD INCRK	

0445	3250	DCA .+3	
0446	3251	DCA .+3	
0447	6402	TTI	
0450	4000	4000	
0451	0000	0	
0452	1275	TAD INCRK+1	/3776
0453	1250	TAD .-3	
0454	7040	CMA	
0455	7440	SZA	/DID TTI +1 INCREMENT
0456	7402	HLT	/NO, ERROR
0457	1251	TAD .-6	
0460	7440	SZA	/WAS TTI +2 CHANGED
0461	7402	HLT	/YES, ERROR
0462	6411	TTCL	/CLEAR LINE REGISTER
0463	6402	TTI	
0464	0000	0	
0465	0000	0	
0466	6414	TTRL	/READ LINE REGISTER
0467	7440	SZA	/TTI INCREMENT LINE REGISTER
0470	7402	HLT	/YES, ERROR
0471	4030	JMS Z ENDIST	/END INITIAL TTI

0472	0000	FORISZ,	0
0473	2272	FORPL2,	ISZ FORISZ /TO CHECK IF TTI+2 IS EXECUTED
0474	4000	INCRK,	4000 /TO CHECK IF TTI+1 IS INCRE
0475	3776		3776

/INITIAL TIO TEST, 2ND TTI TEST
*600

/PAGE 3 ADDRESS 600

0600	6411	TSTIO,	TTCL	/SET LINE REGISTER TO 0
0601	7201		CLA IAC	/SET AC TO +1
0602	6404		TIO	/TELETYPE OUTPUT 1
0603	5206		JMP .+3	/SHOULD EXECUTE HERE
0604	7402		HLT	/RETURN EITHER OF THESE
0605	7402		HLT	/TWO LOCATIONS IS ERROR
0606	7440		SZA	/DID AC SHIFT PROPERLY
0607	7402		HLT	/NO, ERROR
0610	6414		TTRL	/READ LINE REGISTER
0611	7440		SZA	/DID LR GET INCREMENTED
0612	7402		HLT	/YES, ERROR
0613	3215		DCA .+2	/CLEAR TTI +1
0614	6402		TTI	/READ TTY LINE
0615	0000		0	/SHOULD NOT CHANGE
0616	0000		0	
0617	1215		TAD .-2	/DID TIO TRANSMIT A 1
0620	7440		SZA	/AND TTI READ COMPLEMENT
0621	7402		HLT	/NO, ERROR EITHER TIO OR TTI
0622	7120		STL	/SET LINK
0623	6404		TIO	/TELETYPE OUTPUT0
0624	7440		SZA	/AC SHIFT PROPERLY
0625	7402		HLT	/NO, ERROR
0626	3230		DCA .+2	
0627	6402		TTI	/TELETYPE INPUT
0630	0000		0	
0631	0000		0	
0632	1230		TAD .-2	/GET STATUS WORD TTI+1

0633	7104	CLL RAL	/CLEAR L, BIT 0 TO L
0634	7420	SNL	/DID TIO & TTI WORK PROPERLY
0635	7402	HLT	/NO, ERROR
0636	7440	SZA	/STATUS SHOULD NOT BE INCREM
0637	7402	HLT	/STATUS WORD ERROR
0640	1324	TAD KOF3	/4003
0641	3244	DCA .+3	/SET STATUS WORD
0642	3245	DCA .+3	/CLEAR CHAR ASSEM WORD
0643	6402	TTI	
0644	4003	4003	
0645	0000	0	
0646	1244	TAD .-2	/GET STATUS WORD
0647	7040	CMA	/COMPLEMENT STATUS
0650	1325	TAD KOF3+1 /4005	
0651	7440	SZA	/STATUS INCREMENT PROPERLY
0652	7402	HLT	/NO, HALT
0653	1245	TAD .-6	/0 BIT IN THE
0654	7440	SZA	/CHARACTER ASSEMBLY WORD
0655	7402	HLT	/NO, HALT
0656	7201	CLA IAC	/AC = +1
0657	6404	TIO	/SET LINE 0 TO A 1
0660	1324	TAD KOF3	/4003
0661	3264	DCA .+3	/SET STATUS WORD
0662	3265	DCA .+3	/CLEAR ASSEMBLY WORD
0663	6402	TTI	/INPUT LINE 0
0664	4003	4003	
0665	0000	0	
0666	1265	TAD .-1	/GET ASSEMBLY WORD
0667	7104	CLL RAL	/SET BIT 0 INTO LINK
0670	7420	SNL	/RECEIVE A ! ON LINE 0
0671	7402	HLT	/NO, ERROR
0672	7440	SZA	/PICK UP ANY OTHER BITS
0673	7402	HLT	/YES, ERROR
0674	1322	TAD KOF1	/4001
0675	3301	DCA .+4	
0676	1271	TAD AHALT	
0677	3302	DCA .+3	
0700	6402	TTI	
0701	4001	4001	
0702	7402	HLT	
0703	1323	TAD KOF2	/4002
0704	3310	DCA .+4	/SET STATUS WORD
0705	1271	TAD AHALT	/HLT
0706	3311	DCA .+3	/CHARACTER ASSEMBLY WORD
0707	6402	TTI	/TELETYPE INPUT
0710	4002	4002	/STATUS WORD
0711	7402	HLT	/HALT IF 2 LOOKS LIKE 3
0712	1326	TAD KOF7	/4007
0713	3317	DCA .+4	/SET STATUS WORD
0714	1271	TAD AHALT	/HLT
0715	3320	DCA .+3	/GET ASSEMBLY WORD
0716	6402	TTI	/TT INPUT
0717	4007	4007	/STATUS WORD
0720	7402	HLT	/HALT IF 7 LOOKS LIKE 3
0721	4030	JMS Z ENDTST	/END OF INITIAL ■


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0722 4001 KOF1,      4001
0723 4002 KOF2,      4002
0724 4003 KOF3,      4003
0725 4005      4005
0726 4007 KOF7,      4007
      /11 TTI INSTRUCTIONS FOR SHIFMB
      *730
0730 5330      JMP .
0731 6402 TTITAB,   TTI      /TELETYPE INPUT INSTRUCTION
0732 4003      4003      /STATUS WORD
0733 0000      0        /CHARACTER ASSEMBLY
0734 6402      TTI
0735 4003      4003
0736 0000      0
0737 6402      TTI
0740 4003      4003
0741 0000      0
0742 6402      TTI
0743 4003      4003
0744 0000      0
0745 6402      TTI
0746 4003      4003
0747 0000      0
0750 6402      TTI
0751 4003      4003
0752 0000      0
0753 6402      TTI
0754 4003      4003
0755 0000      0
0756 6402      TTI
0757 4003      4003
0760 0000      0
0761 6402      TTI
0762 4003      4003
0763 0000      0
0764 6402      TTI
0765 4003      4003
0766 0000      0
0767 6402      TTI
0770 4003      4003
0771 0000      0
0772 5730      JMP I TTITAB-1      /EXIT
      /SHIFT THE MB TEST, START SHIFT IN ONES
      *1000
1000 6411 SHIFMB,   TTCL      /CLEAR LINE REGISTER
1001 7201   CLA IAC      /AC = 1
1002 6404   TIO      /SET LINE 0 TO A 1
1003 1373   TAD K13      /-13
1004 3013   DCA Z 13      /FOR COUNTING
1005 3011   DCA Z 11      /CLEAR SIMULATED SHIFT
1006 4344   JMS TTISHF /LOAD (11) INTO SHFREG AND TTI
1007 7120   STL      /SET LINK TO
1010 4355   JMS SHIF11 /SIMULATE TTI SHIFT
1011 1353   TAD SHFREG /GET TTI RESULTS
1012 3010   DCA Z 10      /INTO LOC 10
1013 4362   JMS COMP11 /COMPARE LOC 10 AND LOC 11
1014 2013   ISZ Z 13      /FILLED WITH ALL ONES
1015 5206   JMP .-7      /NO, REPEAT

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/SHIFT IN ZEROS
1016 7240 CLA CMA
1017 3011 DCA Z 11 /SET LOC 11 TO ONES
1020 6404 TIO /SET LINE 0 TO A 0
1021 1373 TAD K13 /-13
1022 3013 DCA Z 13 /FOR COUNTING
1023 4344 JMS TTISHF /LOAD 11 INTO SHFREG AND TTI
1024 7100 CLL /CLEAR LINK
1025 4355 JMS SHIF11 /SIMULATE TTI SHIFT
1026 1353 TAD SHFREG /GET TTI RESULTS
1027 3010 DCA Z 10 /INTO LOC 10
1030 4362 JMS COMP11 /COMPARE 10 AGAINST 11
1031 2013 ISZ Z 13 /FILLED WITH ALL ZEROS
1032 5223 JMP .-7 /NO, REPEAT

/FLOAT A SINGLE ONE BIT
1033 1273 TAD BIT0 /4000
1034 3011 DCA Z 11 /PRESET (11)
1035 7100 CLL /LINK = LINE 0
1036 4275 JMS GENTTI /GENERATE 11 TTI INSTRUCTIONS
1037 1273 TAD BIT0 /4000
1040 3011 DCA Z 11 /RESET (11)
1041 7100 CLL /LINK = LINE 0
1042 4322 JMS COMTTI /COMPARE TTI RESULTS

/FLOAT A SINGLE 0 BIT
1043 7201 CLA IAC /AC=1
1044 6404 TIO /SET LINE 0 TO 1
1045 1274 TAD BIT0+1 /3777
1046 3011 DCA Z 11 /SET CONTENTS 11
1047 7120 STL /LINK=LINE 0
1050 4275 JMS GENTTI /GENERATE 11 TTI INSTRUCTION
1051 1274 TAD BIT0+1 /3777
1052 3011 DCA Z 11 /RESET CONTENTS OF 11
1053 7120 STL /LINK = LINE 0
1054 4322 JMS COMTTI /COMPARE 11 TTI AGAINST (11)

/SHIFT ALL COMB
1055 7200 CLA /AC = 0
1056 6404 TIO /SET LINE 0 TO 0
1057 3013 DCA Z 13 /INITIALIZE 13
1060 1013 SHFALL, TAD Z 13
1061 3011 DCA Z 11 /SET 11 = TO NEXT SHIFT
1062 4344 JMS TTISHF /(11) TO SHFREG AND TTI
1063 7100 CLL /LINK = LINE 0
1064 4355 JMS SHIF11 /SIMULATE TTI SHIFT
1065 1353 TAD SHFREG /GET TTI RESULT
1066 3010 DCA Z 10 /INTO 10
1067 4362 JMS COMP11 /COMPARE (10) = (11)
1070 2013 ISZ Z 13 /TESTED ALL COMBINATIONS
1071 5260 JMP SHFALL /NO, REPEAT
1072 4030 JMS Z ENDTST
1073 4000 BIT0, 4000
1074 3777 3777

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/SET UP 11 TTI INSTRUCTIONS
1075 5275 GENTTI, JMP . /SET UP TTI TAB
1076 7204 GLK /GET LINK
1077 3014 DCA Z 14 /SAVE LINK
1100 1372 TAD K11 /-11
1101 3012 DCA Z 12 /FOR COUNTING
1102 1375 TAD TABTTI /FIRST TTI+1-1
1103 3015 DCA Z 15 /FOR STORING
1104 1374 FILLIT, TAD AKOF3 /4003
1105 3415 DCA I Z 15 /TTI+1
1106 1011 TAD Z 11 /FOR TTI+2 SHIFTING
1107 3415 DCA I Z 15 /TTI+2
1110 2015 ISZ Z 15 /STEP PAST TTI INSTR.
1111 1014 TAD Z 14 /GET LINK
1112 7110 CLL RAR /LINK = LINE 0
1113 1011 TAD Z 11 /GET LAST TTI+2
1114 7010 RAR /FOR NEXT TTI+2
1115 3011 DCA Z 11 /RESET 11
1116 2012 ISZ Z 12 /RESET 11 TTI
1117 5304 JMP FILLIT /NO
1120 4776 JMS I TABTTI+1 /EXECUTE TTI INSTRUCTIONS
1121 5675 JMP I GENTTI /EXIT

/COMPARE RESULTS OF TTI INSTRUCTIONS
1122 5322 COMTTI, JMP .
1123 7204 GLK /GET LINK
1124 3014 DCA Z 14
1125 1372 TAD K11 /-11
1126 3012 DCA Z 12 /FOR COUNTING
1127 1375 TAD TABTTI /FIRST TTI
1130 3015 DCA Z 15 /FOR GETTING TTI'S +2
1131 2015 COMPIT, ISZ Z 15 /STEP PAST STATUS WORD
1132 1415 TAD I Z 15 /GET TTI +2
1133 3010 DCA Z 10 /FOR COMPARING
1134 1014 TAD Z 14 /GET LINK
1135 7110 CLL RAR /LINK = LINE 0
1136 4355 JMS SHIF11 /SIMULATE TTI SHIFT
1137 4362 JMS COMP11 /COMPARE (10) AND (11)
1140 2015 ISZ Z 15 /STEP PAST TTI INSTR.
1141 2012 ISZ Z 12 /COMPARED ALL
1142 5331 JMP COMPIT /NO
1143 5722 JMP I COMTTI /EXIT

1144 5344 TTISHF, JMP . /SET (11) INTO SHFREG, TTI
1145 1011 TAD Z 11 /GET 11
1146 3353 DCA SHFREG /INTO TTI+2
1147 1374 TAD AKOF3 /4003
1150 3352 DCA .+2 /INTO TTI+1
1151 6402 TTI /TELETYPE INPUT
1152 4003 4003 /STATUS WORD
1153 0000 SHFREG, 0 /ASSEMBLY WORD
1154 5744 JMP I TTISHF /EXIT
1155 5355 SHIF11, JMP . /SIMULATE TTI L=LINE 0
1156 1011 TAD Z 11 /GET 11
1157 7010 RAR /SHIFT AND SET BIT 0
1160 3011 DCA Z 11 /BACK INTO 11
1161 5755 JMP I SHIF11 /EXIT
1162 5362 COMP11, JMP . /COMPARE LOC 10 AGAINST 11

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1163	1010	TAD Z 10	/GET TTI RESULTS
1164	7041	CMA IAC	/2'S COMPLEMENT
1165	1011	TAD Z 11	/ADD SIMULATED RESULTS
1166	7440	SZA	/AC SHOULD = 0
1167	4074	JMS Z ERROR	/IT DOES NOT ERROR
1170	7200	CLA	/JUST IN CASE
1171	5762	JMP I COMP11	/EXIT
1172	7765	K11, 7765	/-13
1173	7763	K13, 7763	/-13
1174	4003	AKOF3, 4003	/FOR TTI +1
1175	0731	TABITI, ITITAB	
1176	0730	ITITAB-1	
/CLOCK TEST, SWITCHES 10+11 INDICATE CLOCK			
*1200			
1200	7604	CLOCK, CLA QSR	/GET CLOCK NUMBER
1201	0334	AND THREE	/CLR TO CLOCK NUMBER
1202	3335	DCA KLOCK	/SAVE IT
1203	1335	TAD KLOCK	/GET CLOCK NUMBER
1204	1336	TAD KLOCK+1	/+ TABLE ADDRES
1205	3337	DCA KLOCK+2	/= TABLE POINTER
1206	1737	TAD I KLOCK+2	/GET IOT POINTER
1207	3010	DCA Z 10	/FOR INDIRECT
1210	1410	TAD I 10	/SKIP ON CLOCK
1211	3241	DCA SKIP1	/SET FIRST CLOCK SKIP
1212	1241	TAD SKIP1	
1213	3257	DCA SKIP2	/SECOND
1214	1257	TAD SKIP2	
1215	3272	DCA SKIP3	/THIRD
1216	1272	TAD SKIP3	
1217	3300	DCA SKIP4	/FOURTH
1220	1300	TAD SKIP4	
1221	3303	DCA SKIP5	/FIFTH
1222	1303	TAD SKIP5	
1223	3311	DCA SKIP6	/SIXTH
1224	1311	TAD SKIP6	
1225	3267	DCA RUPTOK+1	
1226	1410	TAD I 10	/TURN CLOCK ON
1227	3253	DCA ONONE	/SET UP FIRST CLOCK ON
1230	1253	TAD ONONE	
1231	3266	DCA RUPTOK	/SECOND
1232	1266	TAD RUPTOK	
1233	3271	DCA RUPTOK+3	
1234	1410	TAD I 10	/TURN OFF CLOCK
1235	3240	DCA OFFONE	/SET UP FIRST CLOCK OFF
1236	1240	TAD OFFONE	
1237	3302	DCA OFFTWO	/SECOND
1240	6422	OFFONE, ITIOFF	/TURN CLOCK OFF
1241	6421	SKIP1, ITISKIP	/SKIP, IS CLOCK ON?
1242	7410	SKP	/NO
1243	7402	HLT	/CLOCK SKIP SKIPPED
1244	1360	TAD ADDRS	
1245	3002	DCA Z 2	/FOR INTERRUPT
1246	6001	ION	
1247	7000	NOP	/WAIT
1250	6002	IOF	/INTERRUPT NOT IS OK
1251	7410	SKP	/SKP ERROR HALT
1252	7402	NORUPT, HLT	/INTERRUPT IN ERROR

1253	6424	ONONE,	TTION	/TURN CLOCK ON
1254	3337		DCA KLOCK+2	
1255	2337		ISZ KLOCK+2	/WAIT
1256	5255		JMP .-1	
1257	6421	SKIP2,	TTISKP	/SKIP WORK
1260	7402		HLT	/DID NOT SKIP ON CLOCK
1261	1361		TAD ADDRS+1	/ADDRESS FOR INTERRUPT
1262	3002		DCA Z 2	/FOR JMP I 2
1263	6001		ION	/TURN INTERRUPTS ON
1264	7000		NOP	/WAIT
1265	7402		HLT	/NO, INTERRUPT
1266	6424	RUPTOK,	TTION	/CLOCK ON
1267	6421		TTISKP	/ CLOCK FLAG SET
1270	5267		JMP .-1	/NO, WAIT
1271	6424		TTION	/CLOCK ON, CLEAR CLOCK FLAG
1272	6421	SKIP3,	TTISKP	/FLAG CLEAR?
1273	7410		SKP	/YES
1274	7402		HLT	/FLAG NOT CLEARED BY TTXON
1275	3337		DCA KLOCK+2	
1276	2337		ISZ KLOCK+2	/WAIT FOR CLOCK
1277	5276		JMP .-1	
1300	6421	SKIP4,	TTISKP	/FLAG ON AGAIN?
1301	7402		HLT	/NO
1302	6422	OFFIWO,	TTIOFF	/TURN CLOCK OFF
1303	6421	SKIP5,	TTISKP	/FLAG CLEAR?
1304	7410		SKP	/YES
1305	7402		HLT	/FLAG NOT CLEARED BY TTXOFF
1306	3337		DCA KLOCK+2	/WAIT
1307	2337		ISZ KLOCK+2	
1310	5307		JMP .-1	
1311	6421			
1312	7410	SKIP6,	TTISKP	/CLOCK ON?
1313	7402		SKP	/NO
1314	6421		HLT	/TTXOFF DID NOT TURN CLOCK
1315	7410		TTISKP	/ALL
1316	7402		SKP	/CLOCKS
1317	6431		HLT	/SHOULD BE OFF
1320	7410		TT2SKP	/AT THIS POINT
1321	7402		SKP	
1322	6441		HLT	
1323	7410		TT3SKP	
1324	7402		SKP	
1325	6411		HLT	
1326	7201	TTCL		/SET LINE
1327	6404	CLA IAC		/ 0 TO A
1330	6451	TT0	/1 FOR TEST 2	
1331	4030		TT4SKP	
1332	7402		JMS Z ENDIST	/END OF CLOCK TEST
1333	4030		HLT	
1334	0003		JMS Z ENDIST	/END OF CLOCK TEST
1335	0000	THREE,	0003	/FOR ANDING
1336	1340	KLOCK,	0	/CLOCK NUMBER
1337	0000		KTABLE	/TABLE ADDRESS
1340	1343		0	/FOR INDIRECT
1341	1346	KTABLE,	TTONE-1	/IOT'S FOR CLOCK 1
			TTTWO-1	/IOT'S FOR CLOCK 2

1342	1351		TTHREE-1	/IOT'S FOR CLOCK 3
1343	1354		TTFOUR-1	/IOT'S FOR CLOCK 4
1344	6421	TTONE,	TT1SKP	/CLOCK 1 SKIP
1345	6424		TT1ON	/CLOCK 1 ON
1346	6422		TT1OFF	/CLOCK 1 OFF
1347	6431	TTTWO,	TT2SKP	/CLOCK 2 SKIP
1350	6434		TT2ON	/CLOCK 2 ON
1351	6432		TT2OFF	/CLOCK 2 OFF
1352	6441	TTHREE,	TT3SKP	/CLOCK 2 SKIP
1353	6444		TT3ON	/CLOCK 3 ON
1354	6442		TT3OFF	/CLOCK 3 OFF
1355	6451	TTFOUR,	TT4SKP	/CLOCK 4 SKIP
1356	6454		TT4ON	/CLOCK 4 ON
1357	6452		TT4OFF	/CLOCK 4 OFF
1360	1252	ADDRS,	NORUPT	
1361	1266		RUPTOK	

/POWER CLEAR TEST

*1400				
1400	7200	PWRCLR,	CLA	
1401	6411		TTCL	/SET TO LINE 0
1402	6404		TT0	/LINE 0 TO A 0
1403	6424		TT1ON	/CLOCK 1 ON
1404	6434		TT2ON	/CLOCK 2 ON
1405	6444		TT3ON	/CLOCK 3 ON
1406	6454		TT4ON	/CLOCK 4 ON
1407	7402		HLT	/HALT, WAIT START
1410	3212		DCA .+2	/CLEAR STATUS
1411	6402		TTI	/TELETYPE INPUT
1412	0000		0	/STATUS WORD
1413	0000		0	
1414	1212		TAD .-2	/GET STATUS WORD
1415	7440		SZA	/LINE 0 A 1?
1416	7402		HLT	/NO
1417	6421		TT1SKP	/CLOCK ON?
1420	7410		SKP	
1421	7402		HLT	/YES
1422	6431		TT2SKP	/CLOCK ON?
1423	7410		SKP	
1424	7402		HLT	/YES
1425	6441		TT3SKP	/CLOCK ON/
1426	7410		SKP	
1427	7402		HLT	/YES
1430	6451		TT4SKP	/CLOCK ON?
1431	7410		SKP	
1432	7402		HLT	/YES
1433	7402		HLT	/END POWER CLEAR TEST
1434	5200		JMP PWRCLR	/ONLY 1 PASS

ADDRS	1360
AHALT	0671
AKOF3	1174
BIT0	1073
CLOCK	1200
COMPIT	1131
COMP11	1162

COMITI 1122
ENDIST 0030
ERROR 0074
FILLIT 1104
FORISZ 0472
FORPL2 0473
FORTST 0070
GENTTI 1075
INCLOP 0263
INCL2 0305
INCRK 0474
KLOCK 1335
KOF1 0722
KOF2 0723
KOF3 0724
KOF7 0726
KTABLE 1340
K11 1172
K127 0324
K128 0323
K13 1173
LINREG 0200
NORUPT 1252
OFFONE 1240
OFFTWO 1302
ONESIX 0056
ONE77 0322
ONONE 1253
PWRCLR 1400
RUPTOK 1266
SETLOP 0234
SHFALL 1060
SHFREG 1153
SHIFMB 1000
SHIF11 1155
SKIP1 1241

SKIP2 1257
SKIP3 1272
SKIP4 1300
SKIP5 1303
SKIP6 1311

TABITI 1175
THREE 1334
TSPNTR 0061
TSTTO 0600
TSTTTI 0400
TTCL 6411
TTFOUR 1355
TTHREE 1352
TTI 6402
TTINCR 6401
TTISHF 1144
TTITAB 0731
TTO 6404
TTONE 1344
TTRL 6414
TTSL 6412
TTTWO 1347
TT10FF 6422
TT10N 6424
TT1SKP 6421
TT20FF 6432
TT20N 6434
TT2SKP 6431
TT30FF 6442
TT30N 6444
TT3SKP 6441
TT40FF 6452
TT40N 6454
TT4SKP 6451

11. DIAGRAMS (Not Applicable)
12. REFERENCES (Not Applicable)

