

IDENTIFICATION

PRODUCT CODE: MAINDEC 12-D8CC-D
PRODUCT NAME: KW12A CLOCK TEST
DATE CREATED: JUNE 19, 1970
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: HAROLD LONG

1 ABSTRACT

1.1 The KW12 Real Time Clock Test is designed to verify the correct operation of the Buffer Preset Register, Clock Counter Register, Clock Control Register, Clock Enable Register, Clock I/O Interface, External Input Channels, and Fast Sample Mode (if the AD12 option is concurrently installed.)

1.2 Program Control is maintained by a monitor resident in Bank 0. Several options are available to the operator for error handling.

2 REQUIREMENTS:

2.1 Equipment:

- a) A PDP-12 with KW12 installed.
- b) An AD12 Analog-to-Digital Converter if Fast Sample testing is required.
- c) An ASR-33 or equivalent.

2.2 Preliminary Programs

- a) All Central Processor and Memory Diagnostic Programs for a basic PDP-12 must be able to run successfully prior to testing the KW12.

2.3 Storage:

- a) 4K minimum core.
- b) Program occupies locations 00000 to 76000.

3 LOADING PROCEDURES

3.1 Method

This program must be loaded with the binary loader. If you are unfamiliar with the proper binary loading procedures refer to "Appendix A" of this program, otherwise proceed with the following:

- a) Set the teletype reader switch to FREE.
- b) Open the teletype reader and insert the program tape so that the arrows on the tape are visible to and pointing toward the operator.
- c) Close the reader and set the reader switch to START.
- d) Set the teletype front panel switch to ON LINE.
- e) Set the LEFT switches to 7777.
- f) Set the RIGHT switches to 40000.

- g) Set the MODE switch to 8 mode.
- h) Depress I/O preset.
- i) Depress START IS.
- j) When the program tape has been read the ACCUMULATOR must be 0000 if it is not, a read-in error has occurred and one might try reloading the binary loader.
- k) Remove the program tape from the reader.

4 STARTING PROCEDURES

4.1 Method

- a) Set the MODE switch to 8 mode.
- b) Set the LEFT switches to 0000.
- c) Set the RIGHT switches to the desired options.
- d) Depress I/O preset.
- e) Depress START 20.
- f) The program is now running. The teletype bell will ring at the end of each pass. In addition, the contents of the pass counter will be typed out.

4.2 Switch Settings

- a) If Fast Sample testing is to be attempted, set knob 0 fully counterclockwise and knob 1 fully clockwise.
- b) Set the selector switches on the front panel to line frequency.
- c) Set the input level knobs to mid-range.
- d) Select any desired error handler options. With RSW = 0000, the following sequence will occur for an error: (MESSAGE TYPEOUT...ERROR HALT) the operator selects any further error options and depresses continue... (MONITOR EXECUTES NEXT SEQUENTIAL TEST)

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RSW 00 = 1, INHIBIT ERROR HALT
RSW 01 = 1, INHIBIT ERROR PRINTOUT
RSW 02 = 1, SCOPE LOOP ON ERROR
RSW 03 = 1, SCOPE LOOP ON NON-FAILING TEST
RSW 04 = 1, INHIBIT FAST SAMPLE TESTING
RSW 05 = 1, INHIBIT BELL RINGING
RSW 06 = 1, INHIBIT PASS COUNTER PRINTOUT

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5 ERROR ROUTINE

5.1 Error Printout

- a) The error messages have the following general form:

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TEST NO. TEST MESSAGE
REG1 REG2 REG3 ...

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- b) TEST NO. refers to the test number as organized in the listing. This is included to aid the operator in finding the test in the listing.
- c) TEST MESSAGE is the body of the text, describing what was tested, and indicating any areas of probable failure.
- d) REG1, REG2, REG3, are specific data words pertaining to the failure.

5.2 Error Messages

TST10 CLAB CHANGED AC
 7741 7020
 TST11 CLBA FAILED
 0402 7020
 TST12 CLAB FAILED
 0402 7020
 TST13 CLAB FAILED
 7741 7020
 TST14 CLAB FAILED
 0402 7020
 TST15 CLBA CHANGED BUFFER
 0402 7020
 TST16 CLAB < > CLBA FAILED
 7741 7020
 TST17 CLAB < > CLBA FAILED
 0402 7020
 TST18 CLAB < > CLBA FAILED
 0402 7020
 TST19 CLEN CHANGED AC
 7741 7020
 TST20 CLEN CHANGED BUFFER
 7741 7020
 TST21 CLCA FAILED
 0402 7020
 TST22 "CLR CNT" FAILED
 0402 7020
 TST23 CLEN FAILED
 7741 7020
 TST24 CLEN FAILED
 0402 7020
 TST25 CLCA CHANGES COUNT
 0402 7020
 TST26 BUFFER < > COUNTER FAILED
 0402 7020
 TST27 "LOAD CNT" FAILS TO "OR"

0402 7020
TST28 "LOAD CNT" LOADED IN ERROR
0402 7020
TST29 "LOAD CNT" LOADED IN ERROR
0402 7020
TST30 MODE REG CAUSES "LOAD CNT?"
0402 7020
TST31 MODE REG CAUSES "LOAD CNT" OR "CLR BUF"
0402 7020 0000
TST32 MODE 2: 1>0 CLOCKED CNTR
0402 7020
TST33 MODE 2: 0>1 CLOCKED CNTR
0000 7020
TST34 O'FLO FAILED TO SET O'FLO FLOP
TST35 CLSA FAILED TO CELEAR O'FLO FLOP

TST36 CLSK SKIPPED IN ERROR

TST37 ILLEGAL CLOCK INTERRUPT!

TST38 CLSK FAILED TO SKIP

TST39 CLOCK INTERRUPT FAILED

TST40 O'FLO ENABLE WON'T ZERO

TST41 O'FLO FLAG WON'T CLEAR

TST42 CLOCK INTR WON'T CLEAR

TST43 BIT 11 FAILED.
0402 7020
TST44 BIT 10 FAILED.
0402 7020
TST45 BIT 09 FAILED.
0402 7020
TST46 BIT 08 FAILED.
0402 7020
TST47 BIT 07 FAILED.
0402 7020
TST48 BIT 06 FAILED.
0402 7020
TST49 BIT 05 FAILED.
0402 7020
TST50 BIT 04 FAILED.
0402 7020
TST51 BIT 03 FAILED.
0402 7020
TST52 BIT 02 FAILED.
0402 7020
TST53 BIT 01 FAILED.
0402 7020

TST54 BIT 100 FAILED.

0402 7020

TST55 RATE 400KC FAILS

TST56 RATE 100KC FAILS

TST57 RATE 10KC. FAILS

TST58 RATE 1KC FAILS

TST58 RATE 100CPS FAILS

TST60

CHAN 1 INPUT LOCKED OUT

TST61 CHAN 3 WON'T TOGGLE

0402 7020

TST62 CHAN 2 WON'T TOGGLE

0402 7020

TST63 CHAN 1 WON'T TOGGLE

0402 7020

TST64 CHAN 1 WON'T INTR

TST65 CHAN 1 INTR IN ERROR

TST66 CHAN 2 WON'T INTR.

0402 7020

TST67 CHAN 2 INTR IN ERROR

TST68 CHAN 3 WON'T INTR.

0402 7020

TST69 CHAN 3 INTR IN ERROR

TST70 CHAN 3 INPUT LINE FREQ FAILED

7020

TST71 CHAN 2 INPUT LINE FREQ FAILED

7020

TST72 CHAN 1 INPUT LINE FREQ FAILED

7020

TST73 FAST SAM FAILS

0402 7020

TST74 O'FLO WON'T FAST SAO

0402 7020

TST75 FAST SAM WON'T SET

0402 7020

TST76 MODES 2-1 INHIBIT FAST SAM

0402 7020

TST77 RATE 10KC FAILS

0402

TST78 I/O PRESET WON'T STOP CLOCK
(RATE BITS 1 & 2)

TST79 1KC FAILS

0402

TST80 I/O PRESET WON'T STOP CLOCK
(RATE BIT 0)

TST81 I/O PRESET WON'T CLEAR O'FLO

TST82 I/O PRESET WON'T CLEAR INTERRUPT ENABLE

TST83 I/O PRESET WON'T CLEAR INPUTS

TST84 I/O PRESET WON'T CLEAR MODE 2

TST85 I/O PRESET WON'T CLEAR MODE 0

TST86 FAST SAM NOT CLEARED

TST87 CHAN 1 WON'T TRANS CNT TO BUF
0200

TST88 CHAN 2 WON'T TRANS CNT TO BUF
0200

TST89 CAAN 3 WON'T TRANS CNT TO BUF
0200

TST90 CHAN 1 WON'T TRANS CNT TO BUF
0300

TST91 CHAN 2 WON'T TRANS CNT TO BUF
0300

TST92 CHAN 3 WON'T TRANS CNT TO BUF
0300

TST93 CHA3 INPUT FAILED TO CLR CNT
7020

TST94 ECO EM-20034 IS EITHER NOT WORKING OR NOT
INSTALLED

KWL2 PASS-0000

APPENDIX A

PDP-8 MODE PERFORATED-TAPE LOADER

READIN MODE LOADER

The readin mode (RIM) loader is a minimum length, basic, perforated-tape program for the 33 ASR. It is initially stored in memory by manual use of the operator console keys and switches. The loader is permanently stored in 18 locations of page 37.

The RIM loader can only be used in conjunction with the 33ASR reader (not the high-speed perforated-tape reader). Because a tape in RIM format is, in effect, twice as long as it need be, it is suggested that the RIM loader be used only to read the binary loader when using the 33 ASR.
(NOTE: Some PDP-12 diagnostic program tapes are in RIM format).

The complete PDP-12 RIM loader (SA=7756) is as follows:

Absolute Address	Octal Content	Tag	Instruction I Z	Comments
7756	6032	BEG,	KCC	/CLEAR AC AND FLAG
7757	6031		KSF	/SKIP IF FLAG=1
7760	5357		JMP-1	/LOOKING FOR CHARACTER
7761	6036		KRB	/READ BUFFER
7762	7106		CLL RTL	
7763	7006		RTL	/CHANNEL 8 IN ACO
7764	7510		SPA	/CHECKING FOR LEADER
7765	5357		JMP BEG+1	/FOUND LEADER
7766	7006		RTL	/OK, CHANNEL 7 IN LINK
7767	6031		KSF	
7770	5367		JMP-1	
7771	6034		KRS	/READ, DO NOT CLEAR
7772	7420		SNL	/CHECKING FOR ADDRESS
7773	3776		DCA 1 TEMP	/STORE CONTENT
7774	3376		DCA TEMP	/STORE ADDRESS
7775	5356		JMP BEG	/NEXT WORD
7776	0	TEMP,	0	/TEMP STORAGE
7777	5XXX		JMP X	/JMP START OF BIN LOADER

Placing the RIM loader in core memory by way of the operator console keys and switches is accomplished as follows;

- a. Set the starting address 7756 in the LEFT switches.
- b. Set the first instruction (6032) in the RIGHT switches.
- c. Press the FILL switch, then press FILL STEP.
- d. Set the next instruction (6031) in the RIGHT switches.
- e. Press the FILL STEP switch.
- f. Repeat steps d and e until all 16 instructions have been deposited.

To load a tape in RIM format, place the tape in the reader, set the LEFT switches to the starting address 7756 of the RIM loader (not of the program being read), press the START LS key, and start the Teletype reader.

BINARY FORMAT PERFORATED TAPE LOADER

Once the RIM loader is in core, place the binary loader program tape on the teletype reader and turn the reader on. Set the LEFT switches to 7756, depress I/O preset with the mode switch in 8 mode, then depress START LS. The binary tape will read into core. The reader must be turned off manually as the tape reaches the end, since RIM does not stop.

/PDP-12 KH12A CLOCK TEST, MAINDEC 12-08CC=L
 /COPYRIGHT 1970, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
 /THIS TEST IS DESIGNED TO VERIFY PROPER OPERATION
 /OF THE KH12A REAL TIME CLOCK AND TO DIAGNOSE
 /MALFUNCTIONS IN REGISTERS, REGISTER TRANSFERS, IO
 /BUS INTERFACE, AND EXTERNAL INPUT CHANNELS.
 /AUTHORS: JAMES KELLY, STEVE TEICHER, HAROLD LONG

/MAJOR START
 /I/O PRESET 0 MODE
 /SET LEFT SWITCHES TO 0000
 /SET RIGHT SWITCHES TO DESIRED OPTIONS
 /DEPRESS START 20

/SWITCH SETTINGS: (NORMALLY 0000)
 /RSM 0001: INHIBIT ERROR HALT
 /RSM 0001: INHIBIT ERROR PRINTOUT
 /RSM 0001: SCOPE LOOP ON FAILING TEST
 /RSM 0001: SCOPE LOOP ON NON-FAILING TEST
 /RSM 0001: INHIBIT FAST SAMPLE TESTING
 /RSM 0001: INHIBIT BELT RINGING
 /RSM 0001: INHIBIT TEST COMPLETION ALARM

/SOME I/O DEFINITIONS:
 /SKIP ON CLOCK INTERRUPT
 /AC TO CLOCK CONTROL REGISTER
 /AC TO BUFFER PRESET REGISTER
 /AC TO CLOCK ENABLE REGISTER
 /CLOCK STATUS TO AC, CLEAR STATUS FLIP-FLOPS
 /BUFFER PRESET REGISTER TO AC
 /COUNTER TO AC
 /MESSAGE TERMINATOR
 /MESSAGE SWITCH
 /RESTART SWITCH
 /SOME LINC PROGRAMMING DEFINITIONS:
 /

6131 CLSK=6131
 6132 CLLR=6132
 6133 CLAB=6133
 6134 CLCN=6134
 6135 CLBA=6135
 6136 CLBA=6136
 6137 CLCA=6137
 /

6141 LINC=6141
 PDP=0002
 CLR=0011
 ESF=0004
 SAM=0100
 LDV1=1020

0001 5452 JMP I RETURN / INTERRUPT RETURN HANDLER
 *10 PINT, 0
 *20 JMP 177 / MAJOR START 8 MODE

/PAGE 0 REGISTERS AND CROSS-PAGE TAGS

0021 5200 BELL, BELL5
 0022 1972 DN43, DN43
 0023 1775 DN47, DN47
 0024 2373 DN55, DN55
 0025 0000 CNTR, CNTR
 0026 5020 ERROR, ERROR
 0027 0000 LSTERR, LSTERR
 0030 5000 NERROR, NERROR
 0031 5051 OUTPAS, ASCII
 0032 0000 PASS, PASS
 0033 1440 PNTA, LOCA
 0034 1472 PNTB, LOCB
 0035 1542 PNTC, LOCC
 0036 2731 PNTD, LOCD
 0037 2753 PNTE, LOCE
 0040 2774 PNTF, LOCF
 0041 3016 PNTG, LOCG
 0042 3040 PNTH, LOCH
 0043 3062 PNTI, LOCI
 0044 4332 PNTJ, LOCL
 0045 5210 RANDOM, RANDY
 0046 0000 REGA, REGA
 0047 0000 REGB, REGB
 0050 0000 REGC, REGC
 0051 0000 REGT, REGT
 0052 2000 RETURN, RETURN
 0053 0000 REXD, REXD
 0054 0000 SEND, SEND
 0055 5252 SET, SET
 0056 0000 SPACE, SPACE
 0057 1343 TST35N, TST35=2
 0060 2764 TST66N, TST66
 0061 3324 TST75N, TST75
 0062 3406 TST77N, TST77
 0063 3453 TST79N, TST79
 0064 4120 TST90N, TST90
 0065 5243 TYPE, TYPOT
 0066 1003 UP43, UP43
 0067 2403 UP55, UP55
 0070 2630 UP61, UP61

/PAGE 0 CONSTANTS

0071	7770	KPRE,	7770
0072	0100	KENA,	0100
0073	4100	KATE,	4100
0074	0000	K0000,	0000
0075	0001	K0001,	0001
0076	0002	K0002,	0002
0077	0003	K0003,	0003
0100	0004	K0004,	0004
0101	0007	K0007,	0007
0102	0010	K0010,	0010
0103	0012	K0012,	0012
0104	0014	K0014,	0014
0105	0015	K0015,	0015
0106	0017	K0017,	0017
0107	0020	K0020,	0020
0110	0037	K0037,	0037
0111	0040	K0040,	0040
0112	0060	K0060,	0060
0113	0077	K0077,	0077
0114	0100	K0100,	0100
0115	0177	K0177,	0177
0116	0200	K0200,	0200
0117	0240	K0240,	0240
0120	0300	K0300,	0300
0121	0377	K0377,	0377
0122	0400	K0400,	0400
0123	0500	K0500,	0500
0124	0600	K0600,	0600
0125	0700	K0700,	0700
0126	0777	K0777,	0777
0127	1000	K1000,	1000
0130	1026	K1026,	1026
0131	1777	K1777,	1777
0132	2000	K2000,	2000
0133	3000	K3000,	3000
0134	3777	K3777,	3777
0135	4000	K4000,	4000
0136	4100	K4100,	4100
0137	5100	K5100,	5100
0140	5252	K5252,	5252
0141	5555	K5555,	5555
0142	6000	K6000,	6000
0143	7774	K7774,	7774

/PAGE 0 NEGATIVE CONSTANTS

0144	7777	M001,	-1
0145	7776	M002,	-2
0146	7774	M004,	-4
0147	7770	M0010,	-10
0150	7760	M0020,	-20
0151	7740	M0040,	-40
0152	7736	M0042,	-42
0153	7700	M0100,	-100
0154	7600	M0200,	-200
0155	7400	M0400,	-400
0156	7000	M1000,	-1000
0157	6400	M1400,	-1400
0160	6000	M2000,	-2000
0161	4000	M4000,	-4000
0162	3334	M4444,	-4444
0163	2400	M5400,	-5400

/RESTART ADDRESS; DON'T CLEAR COUNTERS
/RESET BUFFERS; COUNTERS

MAJOR START 8 MODE, AC=0
/TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
/CLAB=6136 AC TO CLOCK PRESET REGISTER
/CLBA=6136 CLOCK PRESET REGISTER TO AC
/DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?

JMS I BELL
CLA CL
TAD REGA
CLAB
DCA RXED
TAD RXED
CIA
TAD 1046
TAD 1053
0205 1053
0206 7041
0207 1046
0210 7050
0211 4430
0212 4426
0213 5261
0214 7402
0215 7610
0216 0201
TS10,
JMS I BELL
CLA CL
TAD REGA
CLAB
DCA RXED
TAD RXED
CIA
TAD 1046
TAD 1053
0205 1053
0206 7041
0207 1046
0210 7050
0211 4430
0212 4426
0213 5261
0214 7402
0215 7610
0216 0201
TS10,
/RING BELL
/CLEAR AC
/GET A NUMBER-BINARY UP-COUNT SEQUENCE 0 THRU 7777
/LOAD BUFFER
/STORE WHAT WAS LEFT IN AC
/FETCH IT
/INVERT CONTENTS OF AC
/SUBTRACT SEND
/EQUAL?
/CHECK MONITOR
/CLAB CHANGED AC
/MESSAGE POINTER
/ERROR HALT
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP

/DOES BUFFER DATA JAM INTO THE AC?
/CLEAR AC
/SEND REG
/SET BUFFER AND PRESET REGISTER TO 0000
/SET AC TO 7777
/JAM BUFFER PRESET (0000) OVER AC (7777
/SAVE AC
/RESTORE AC
/DID AC BECOME (0000)?
/CHECK MONITOR
/CLBA FAILED TO JAM THE AC
/MESSAGE POINTER
/ERROR HALT
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP

0217 7300
0220 3054
0221 6133
0222 7240
0223 6136
0224 3053
0225 1053
0226 7050
0227 4430
0230 4426
0231 5301
0232 7402
0233 7610
0234 0217
CLA CL
DCA SEND
CLAB
CLA CMA
CLBA
DCA RXED
TAD RXED
SNA CLA
JMS I ERROR
JMS I
TS11M
HLT
SKP CLA
TS11

/DOES THE AC JAM INTO THE BUFFER?

0235	7240	CLA CHA	TS112,	/SET AC=777
0236	6133	CLAB		/SET BUFFER=777
0237	7300	CLA CLL		/CLEAR AC
0240	6133	CLAB		/LOAD BUFFER TO ALL ZEROS
0241	3054	DCA	SEND	/SAVE AC
0242	6136	CLBA		/READ BUFFER AND PRESET REGISTER
0243	3053	DCA	RXED	/SAVE TEST VALUE
0244	1053	TAD	RXED	/RESTORE IT
0245	7050	SNA CLA		/DID BUFFER AND PRESET REGISTER GET CLEARED
0246	4430	JMS I	ERROR	/CHECK MONITOR
0247	4426	JMS I	ERROR	/AC JAM INTO BUFFER FAILED
0250	5017	TS12M		/MESSAGE POINTER
0251	7402	HLT		/ERROR HALT
0252	7010	SKP CLA	TS112	/TO NEXT TEST
0253	0235			/ISZ LOOP1 SCOPE LOOP
0254	7300	CLA CLL	TS113,	/CLEAR AC
0255	1046	TAD	REGA	/GET TEST NUMBER
0256	6133	CLAB		/SEND IT
0257	7200	CLA		/CLEAR AC
0260	6136	CLBA		/RETRIEVE IT
0261	3053	DCA	RXED	/SAVE IT
0262	1053	TAD	RXED	/RESTORE IT
0263	7041	CIA		/COMPLEMENT
0264	1046	TAD	REGA	/ADD TEST NUMBER
0265	7050	SNA CLA		/WHERE THEY EQUAL?
0266	4430	JMS I	ERROR	/CHECK MONITOR
0267	4426	JMS I	ERROR	/AC = BUFFER TO AC DATA TRANSFER FAILED
0270	5035	TS13M		/MESSAGE POINTER
0271	7402	HLT		/ERROR HALT
0272	7010	SKP CLA	TS113	/TO NEXT TEST
0273	0254			/ISZ LOOP1 SCOPE LOOP

/00 RANDOM NUMBERS TRANSFER BETWEEN AG AND BUFFER PROPERLY)

ADDRESS	OPERATION	COMMENT
0274	JMS I	LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
0275	SEND	/SAVE IT
0276	SEND	/RESTORE IT
0277	CLAB	/SEND IT
0300	JMS I	/LOAD THE AC WITH A RANDOM NUMBER
0301	CLBA	/READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
0302	DCA	/SAVE TEST RETURN
0303	TAD	/RESTORE IT
0304	CIA	/COMPLEMENT
0305	TAD	/SUBTRACT TEST NUMBER
0306	SNA CLA	/EQUAL?
0307	JMS I	/CHECK MONITOR
0310	JMS I	/AC = BUFFER = AC DATA INTERCHANGE FAILED
0311	TS14M	/MESSAGE POINTER
0312	HLT	/ERROR HALT
0313	SKP CLA	/TO NEXT TEST
0314	TS14	/ISZ LOOP/ SCOPE LOOP

TEST	TEST NAME	TEST RESULT
0315	4445 JMS I RANDOM	0315
0316	3054 DCA	0316
0317	1054 SEND	0317
0320	6133 TAD	0320
0321	4445 JMS I CLAB	0321
0322	6136 CLBA	0322
0323	4445 JMS I RANDOM	0323
0324	6136 CLBA	0324
0325	3053 DCA	0325
0326	1053 TAD	0326
0327	7041 CIA	0327
0330	1054 TAD	0330
0331	7050 SNA CLA	0331
0332	4430 JMS I ERROR	0332
0333	4426 JMS I ERROR	0333
0334	5371 TST15H	0334
0335	7402 HLT	0335
0336	7610 SKP CLA	0336
0337	132 LOOP1 SCOPE LOOP	0337

10 CAN THE GATES FUNCTION AT HIGH SPEED?

19716, CLA 670 071
REC'D 071
/CLEAR AC /027 TEST NUMBER

CLAB 8270 /SEND IT
CLBA 4084 /GET IT

CLAV
CLAV

8760
8760

CLAB
CLAB

8473

CLAB

CLAB

CLAB
CLAB
CLAB

8790
8790
8790

8760
8760

CLAS 0870
CLAS 0870

CLBA
DCA
RXED
/GRT 14
/SAVE 14

TAD RXED /WEIGH 17
CIA /219 COMPLINT

TAD REGA SNA CLA /COMPARE /EQUATE

JMS I ERROR /CHECK MONITOR /BUE FAILED TO T

TS-16M

171
 SKP CLA
 15314

34036 14007 351/ 03/51

/CAN THE BUFFER SURVIVE CHECKBOARD?

0403	7300	TS117, CLA CL		/CLEAR AC
0404	1140	TAD	K5252	/GET TEST PATTERN
0405	3054	DCA	SEND	/SAVE TEST PATTERN
0406	1054	TAD	SEND	/RESTORE IT
0407	6133	CLAB		/SEND IT
0410	6136	CLBA		/GET IT
0411	7040	CHA		
0412	6133	CLAB		
0413	6136	CLBA		
0414	7040	CHA		
0415	6133	CLAB		
0416	6136	CLBA		
0417	7040	CHA		
0420	6133	CLAB		
0421	6136	CLBA		
0422	7040	CHA		
0423	6133	CLAB		
0424	6136	CLBA		
0425	7040	CHA		
0426	6133	CLAB		
0427	6136	CLBA		
0430	7040	CHA		
0431	6133	CLAB		
0432	6136	CLBA		
0433	7040	CHA		
0434	6133	CLAB		
0435	6136	CLBA		
0436	7040	CHA		
0437	6133	CLAB		
0440	6136	CLBA		
0441	7040	CHA		
0442	6133	CLAB		
0443	6136	CLBA		
0444	7040	CHA		
0445	6133	CLAB		
0446	6136	CLBA		
0447	7040	CHA		
0450	6133	CLAB		
0451	6136	CLBA		
0452	7040	CHA		
0453	3053	DCA		
0454	1053	TAD	RXED	/SAVE FINAL PATTERN
0455	7041	CIA		/RESTORE IT
0456	1054	TAD	SEND	/COMPLEMENT
0457	7050	SVA CLA		/SUBTRACT TEST PATTERN
0462	4430	JMS I	ERROR	/CHECK MONITOR
0461	4426	JMS I	ERROR	/BUFFER FAILED CHECKBOARD TEST
0462	5434	TS117H		/MESSAGE POINTER
0463	7402	HLT		/ERROR HALT
0464	7010	SKP CLA		/TO NEXT TEST
0465	0403	TS117		/ISZ LOOP1 SCOPE LOOP

1/CAN THE BUFFER SURVIVE RANDOM COMPLEMENT PATTERNS?

/GENERATE A RANDOM NUMBER

45181 JHS I RANDOM SEND SEND TAD

/SAVE ! ?
/RESTORE ! ?
/SEND ! ?
/GET ! ?

DATA	ADDRESS	DATA	ADDRESS
0456	4445	TS1B	JMS I
0457	3054		DCA
0458	1054		SEND
0459	6133		CLAB
0460	6133		CLAB
0461	6133		CLAB
0462	6133		CLAB
0463	6133		CLAB
0464	6133		CLAB
0465	6133		CLAB
0466	6133		CLAB
0467	6133		CLAB
0468	6133		CLAB
0469	6133		CLAB
0470	6133		CLAB
0471	6133		CLAB
0472	6133		CLAB
0473	6133		CLAB
0474	6133		CLAB
0475	6133		CLAB
0476	6133		CLAB
0477	6133		CLAB
0478	6133		CLAB
0479	6133		CLAB
0480	6133		CLAB
0481	6133		CLAB
0482	6133		CLAB
0483	6133		CLAB
0484	6133		CLAB
0485	6133		CLAB
0486	6133		CLAB
0487	6133		CLAB
0488	6133		CLAB
0489	6133		CLAB
0490	6133		CLAB
0491	6133		CLAB
0492	6133		CLAB
0493	6133		CLAB
0494	6133		CLAB
0495	6133		CLAB
0496	6133		CLAB
0497	6133		CLAB
0498	6133		CLAB
0499	6133		CLAB
0500	6133		CLAB
0501	6133		CLAB
0502	6133		CLAB
0503	6133		CLAB
0504	6133		CLAB
0505	6133		CLAB
0506	6133		CLAB
0507	6133		CLAB
0508	6133		CLAB
0509	6133		CLAB
0510	6133		CLAB
0511	6133		CLAB
0512	6133		CLAB
0513	6133		CLAB
0514	6133		CLAB
0515	6133		CLAB
0516	6133		CLAB
0517	6133		CLAB
0518	6133		CLAB
0519	6133		CLAB
0520	6133		CLAB
0521	6133		CLAB
0522	6133		CLAB
0523	6133		CLAB
0524	6133		CLAB
0525	6133		CLAB
0526	6133		CLAB
0527	6133		CLAB
0528	6133		CLAB
0529	6133		CLAB
0530	6133		CLAB
0531	6133		CLAB
0532	6133		CLAB
0533	6133		CLAB
0534	6133		CLAB
0535	6133		CLAB
0536	6133		CLAB
0537	6133		CLAB
0538	6133		CLAB
0539	6133		CLAB
0540	6133		CLAB
0541	6133		CLAB
0542	6133		CLAB
0543	6133		CLAB
0544	6133		CLAB
0545	6133		CLAB
0546	6133		CLAB
0547	6133		CLAB
0548	6133		CLAB
0549	6133		CLAB
0550	6133		CLAB
0551	6133		CLAB
0552	6133		CLAB
0553	6133		CLAB
0554	6133		CLAB
0555	6133		CLAB
0556	6133		CLAB
0557	6133		CLAB
0558	6133		CLAB
0559	6133		CLAB
0560	6133		CLAB
0561	6133		CLAB
0562	6133		CLAB
0563	6133		CLAB
0564	6133		CLAB
0565	6133		CLAB
0566	6133		CLAB
0567	6133		CLAB
0568	6133		CLAB
0569	6133		CLAB
0570	6133		CLAB
0571	6133		CLAB
0572	6133		CLAB
0573	6133		CLAB
0574	6133		CLAB

```

/SEND IT
/GET IT
/SAVE FINAL PATTERN
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST PATTERN
/EQUAL?
/CHECK MONITOR
/BUFFER FAILED RANDOM COMPLEMENT PATTERN
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP

```

/CLEN=6134 AC TO CLOCK ENABLE REGISTER
/DOES CLEN AFFECT THE AC?

0553	7300	TS119, CLL CLA	/CLEAR AC
0551	1046	TAD	/RESTORE TEST NUMBER
0552	6134	CLEN	/DOES CLEN AFFECT AC
0553	3053	DCA	/SAVE AC
0554	1053	TAD	/RESTORE IT
0555	7041	CIA	/COMPLEMENT
0556	1046	TAD	/SUBTRACT TEST NUMBER
0557	7650	SNA CLA	/EQUAL?
0560	4430	JMS I	/CHECK MONITOR
0561	4426	JMS I	/AC TO CLOCK ENABLE REG CHANGED AC
0562	5476	TS119M	/MESSAGE POINTER
0563	7402	HLT	/ERROR HALT
0564	7610	SKP CLA	/TO NEXT TEST
0565	0550	TS119	/ISZ LOOP1 SCOPE LOOP

/PRESET REGISTER AND COUNTER DATA INTERCHANGE

/CLSA6135 STATUS REGISTER TO AC
/CLLR6132 AC TO CLOCK CONTROL REGISTER

/DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER?

0566	7300	TS120, CLL CLA	/CLEAR AC
0567	6135	CLSA	/CLEAR STATUS
0570	7300	CLA CLL	/CLEAR AC
0571	1046	TAD	/RESTORE TEST NUMBER
0572	6135	CLAB	/LOAD BUFFER PRESET REGISTER WITH A BINARY UP-COUNT NUMBER
0573	7300	CLA CLL	/CLEAR AC
0574	6135	CLLR	/STOP CLOCK, SET ALL MODES
0575	1114	TAD	/MODE CONTROL REG BIT 2-1
0576	6132	CLLR	/SET MODE 2, ENABLING CLR LOAD CNT
0577	7200	CLA	/CLEAR AC
0600	1116	TAD	/AC BIT 4-1, SIMULATE CLR OP-LOW ON 6134
0601	6134	CLEN	/TRANSFER PRESET COUNT TO CLOCK COUNTER
0602	6136	CLBA	/READ THE BUFFER
0603	3053	DCA	/SAVE IT
0604	1053	TAD	/RESTORE IT
0605	7041	CIA	/COMPLEMENT
0606	1046	TAD	/SUBTRACT TEST NUMBER
0607	7650	SNA CLA	/EQUAL?
0610	4430	JMS I	/CHECK MONITOR
0611	4426	JMS I	/TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
0612	5516	TS120M	/MESSAGE POINTER
0613	7402	HLT	/ERROR HALT
0614	7610	SKP CLA	/TO NEXT TEST
0615	0570	TS120+2	/ISZ LOOP1 SCOPE LOOP

/DOES COUNTER DATA JAM THE BUFFER AND AC?
/CLCA=6137 CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC

6135	CLSA	TS121,	/CLEAR STATUS
6137	CLA CLL		/LOAD BUFFER TO 0000
6135	CLAB		/STOP CLOCK, SET ALL MODES=0
6132	CLLR		/SET AC 05=1
1114	TAD	K0100	/SET MODE 2=1, THEREBY CLEARING CLOCK COUNTER
6132	CLLR		/ENABLE INTERRUPT ON OVERFLOW
7240	CLA CMA		/SET AC 7777
3054	DCA	SEND	/SAVE IT
1054	TAD	SEND	/FETCH IT
6133	CLAB		/SET BUFFER 7777
6137	CLCA		/READ COUNTER
3053	DCA	RXED	/SAVE COUNT
1053	TAD	RXED	/RESTORE IT
7050	SNA CLA		/ERROR?
4430	JMS I	ERROR	/CHECK MONITOR
4426	JMS I		/COUNTER FAILED TO JAM 0000 INTO 7777
5540	TS121M		/MESSAGE POINTER
7402	HLT		/ERROR HALT
7010	SKP CLA		/TO NEXT TEST
0616	TS121		/ISZ LOOP1 SCOPE LOOP
6135	CLSA	TS122,	/CLEAR STATUS
7350	CLA CMA CLL RAR		/SET AC=3777
3054	DCA	SEND	/SAVE AC
1054	TAD	SEND	/FETCH IT
6133	CLAB		/SET BUFFER TO 3777 (USE 3777 SO WE DON'T SET OVERFLOW FLOP)
7300	CLA CLL		/CLEAR AC
1116	TAD	K0200	/ENABLE LOAD COUNT GATES
6134	CLCN		/LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
7300	CLA CLL		/CLEAR AC
6132	CLLR		/ZERO MODE 2
1114	TAD	K0100	/SET AC 05=1
6132	CLLR		/SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
7300	CLA CLL		/CLEAR AC
6137	CLCA		/READ THE COUNTER
3053	DCA	RXED	/SAVE IT
1053	TAD	RXED	/RESTORE IT
7050	SNA CLA		/ERROR?
4430	JMS I	ERROR	/CHECK MONITOR
4426	JMS I		/CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
5556	TS122M		/MESSAGE POINTER
7402	HLT		/ERROR HALT
7010	SKP CLA		/TO NEXT TEST
0617	TS122		/ISZ LOOP1 SCOPE LOOP

/DO ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER?

/CLEAR STATUS	CLS	6135
/CLEAR AC	CLA	0673
/LOAD AC WITH TEST NUMBER	TAD	0674
/SET BUFFER TO TEST NUMBER	CLAB	0675
/CLEAR AC	CLA	0676
/STOP CLOCK; SET ALL MODES=0	CLR	0677
/SET AC 0501	TAD	0700
/GENERATE "CLR CNT"	CLR	0701
/CLEAR AC	CLA	0702
/SET AC 0401	TAD	0703
/GENERATE "LOAD CNT"	CLN	0704
/COUNTER TO AC	CLCA	0705
/SAVE IT	DCA	0706
/RESTORE IT	RXED	0707
/COMPLEMENT	CIA	0710
/SUBTRACT TEST NUMBER	TAD	0711
/EQUAL?	SNA	0712
/CHECK WITH MONITOR	JMS	0713
/BUFFER TO COUNTER DATA INTERCHANGE FAILED	JMS	0714
/MESSAGE POINTER	TS123H	0715
/ERROR HALT	HLT	0716
/TO NEXT TEST	SKP	0717
/1ST LOOP; SCOPE LOOP	TS123	0720

/00 RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER?

0721	4445	JMS I	TS124,	TS124	/GET RANDOM NUMBER
0722	6133	CLAB			/LOAD BUFFER RANDOM
0723	3054	DCA	SEND		/SAVE TEST NUMBER
0724	6135	CLSA			/CLEAR CLOCK STATUS
0725	7200	CLA			/CLEAR AC
0726	6132	CLLR			/STOP CLOCK, SET ALL MODES=0
0727	1114	TAD	K0100		/SET AC 0501
0730	6132	CLLR			/GENERATE "CLR CNT"
0731	7200	CLA			/CLEAR AC
0732	1116	TAD	K0200		/SET AC 0401
0733	6134	CLEN			/GENERATE "LOAD CNT"
0734	4445	JMS I	RANDOM		/GET RANDOM NUMBER
0735	6133	CLAB			/LOAD BUFFER RANDOM
0736	4445	JMS I	RANDOM		/LOAD AC RANDOM
0737	6137	CLCA			/READ COUNTER
0740	3053	DCA			/SAVE TEST VALUE
0741	1053	TAD	RXED		/RESTORE IT
0742	7041	CIA			/COMPLEMENT
0743	1054	TAD	SEND		/SUBTRACT TEST NUMBER
0744	7650	SNA CLA			/EQUALLY
0745	4430	JMS I	NEROR		/CHECK MONITOR
0746	4426	JMS I	ERROR		/BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
0747	5614	TS124M			/MESSAGE POINTER
0750	7402	HLT			/ERROR HALT
0751	7610	SKP CLA			/TO NEXT TEST
0752	0721	TS124			/ISE LOOP! SCOPE LOOP

1000S READING THE COUNTER CHANGE ITS STATE

```

/GET RANDOM TEST NUMBER
/SEND 17 TO BUFFER
/SAVE 17
/STOP CLOCK, SET ALL MODES=0
/SET AC 05#1
/GENERATE "CLR CNT"
/GENERATE "CLR CNT"
/CLR AC
/CLR AC 05#1
/SET AC 05#1
/GENERATE "LOAD CNT"
/GET RANDOM NUMBER
/SEND 17 TO BUFFER
/GET RANDOM NUMBER
/SEND 17 TO BUFFER
/READ CLOCK COUNTER
/GET RANDOM NUMBER
/SEND 17 TO BUFFER
/READ CLOCK COUNTER
/GET RANDOM NUMBER
/SAVE 17
/RESTORE 17
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK MONITOR
/(CLCA) READ THE COUNTER CHAN
/ERROR HALT
/10 NEXT TEST
/IS2 LOOP/ SCOPE LOOP
/SET AC#7777
/PRESET COUNTER FOR NEXT TEST

```

[illegible]

0755 4445 0754 3054 0755 3054 0756 6132 0757 1314 0760 6132 0761 6135 0762 7210 0763 1116 0764 6134 0765 4445 0766 6133 0767 4445 0770 6137 0771 4445 0772 6133 0773 4445 0774 6137 0775 3053 0776 1053 0777 7041 1000 1000 1001 7650 4430 4426 5632 1005 7402 7610 0750 0753 7340 1011 1010 1011

/CAN THE BUF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED?

1012	4445	JMS I	RANDOM	/GET RANDOM NUMBER
1013	6133	CLAB		/SEND IT TO BUFFER
1014	3054	DCA	SEND	/SAVE IT
1015	7200	CLA		/CLEAR AC
1016	6132	CLR		/STOP CLOCK
1017	1114	TAD	K0100	/SET AC 0501
1020	6132	CLR		/GENERATE "CLR CNT"
1021	6135	CLSA		/CLEAR CLOCK STATUS
1022	7200	CLA		/CLEAR AC
1023	1116	TAD	K0200	/SET AC 0401
1024	6134	CLCN		/GENERATE "LOAD CNT"
1025	6137	CLCA		/READ COUNTER
1026	2047	ISZ	REG8	/DONE?
1027	5215	JMP	TS12603	/BACK TO START 4096 TIMES
1030	3053	DCA	RXED	/SAVE FINAL NUMBER
1031	1053	TAD	RXED	/RESTORE IT
1032	7041	CIA		/COMPLEMENT
1033	1054	TAD	SEND	/SUBTRACT TEST NUMBER
1034	7050	SNA CLA		/EQUAL?
1035	4430	JMS I	ERROR	/CHECK MONITOR
1036	4426	JMS I	ERROR	/THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGH SPEED
1037	5053	TS126H		/MESSAGE POINTER
1040	7402	HLT		/ERROR HALT
1041	7010	SKP CLA		/TO NEXT TEST
1042	1012	TS126		/ISZ LOOP/ SCOPE LOOP

/DOES (LOAD CNT) PERFORM LOGIC OR?

1043	7300	CLA CL	TS127,	/CLEAR AC
1044	6132	CLR		/STOP CLOCK
1045	1114	TAD	K0100	/SET AC 0501
1046	6132	CLR		/GENERATE "CLR CNT"
1047	6135	CLSA		/CLEAR CLOCK STATUS
1050	4445	JMS I	RANDOM	/GET RANDOM TEST NUMBER
1051	6133	CLAB		/LOAD BUFFER WITH A RANDOM NUMBER
1052	3054	DCA	SEND	/SAVE IT
1053	1116	TAD	K0200	/SET AC 0401
1054	6134	CLEN		/LOAD COUNTER FROM THE BUFFER REGISTER, GENERATE "LOAD CNT"
1055	7300	CLA CL		/CLEAR AC
1056	1054	TAD	SEND	/GET TEST NUMBER
1057	7040	CHA		/LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
1060	6133	CLAB		/LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
1061	7300	CLA CL		/CLEAR AC
1062	1116	TAD	K0200	/SET AC 0401
1063	6134	CLEN		/LOAD COUNTER, /READ COUNTER,
1064	6137	CLCA		/SAVE IT
1065	3053	DCA	RXED	/RESTORE IT
1066	1053	TAD	RXED	/CONVERT TO ALL ZEROS FOR TESTING
1067	7040	CHA		/ZERO?
1070	7050	SNA CLA		/CHECK MONITOR
1071	4430	JMS I	ERROR	/THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
1072	4426	JMS I	ERROR	/MESSAGE POINTER
1073	5676	TS127M		/ERROR HALT
1074	7402	HLT		/TO NEXT TEST
1075	7610	SKP CLA		/ISZ LOOP, SCOPE LOOP
1076	1043			

TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (N)

TIME	COMMAND	STATUS	REMARKS
1307	CLA CLL		
1308	CLA9		
1309	/CLEAR AC		
1310	/CLEAR BUFFER		
1311	/CLEAR ALL MODES		
1312	/SET AC 05=1		
1313	/GEN, "CLR CNT"		
1314	/CLEAR STATUS		
1315	/GET RANDOM NUMBER		
1316	/SEND IT TO BUFFER		
1317	/SAVE IT		
1318	/STOP CLOCK, SET ALL MODES=0		
1319	/SET AC 05=1		
1320	/GENERATE "CLR CNT"		
1321	/CLEAR AC		
1322	/SET ALL MODES=0		
1323	/SET AC 04=1		
1324	/TRY TO GENERATE "LOAD CNT"		
1325	/GET COUNTER		
1326	/SAVE IT		
1327	/RESTORE IT		
1328	/WAS IT ZERO?		
1329	/CHECK MONITOR		
1330	/LOAD CNT GATES FUNCTIONED		
1331	/MESSAGE POINTER		
1332	/ERROR HALT		
1333	/TO NEXT TEST		
1334	/IS2 LOOP SCOPE LOOP		

```

/CLEAR AC
/CLEAR BUFFER
/CLEAR ALL MODES
/SET AC 05#1
/GEN, "CLR CNT"
/CLEAR STATUS
/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/STOP CLOCK, SET ALL MODES=0
/SET AC 05#1
/GENERATE "CLR CNT"
/CLEAR AC
/SET ALL MODES=0
/SET AC 04#1
/TRY TO GENERATE "LOAD CNT"
/GET COUNTER
/SAVE IT
/RESTORE IT
/HAS IT ZERO?
/CHECK MONITOR
/LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP1 SCOPE LOOP

```

/TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 1(1)

4445	JMS I	RANDOM	/GET RANDOM NUMBER
1131			
1132	CLAB		/SEND IT TO BUFFER
1133	DCA	SEND	/SAVE IT
3054			
1134	TAD	K0600	/SET AC 04,0501
1135	CLLR		/GENERATE "CLR CNT", SET MODE 1 AND 2 #1
6135	CLSA		/CLEAR CLOCK STATUS
1137	CLA		/CLEAR AC
7200	TAD	K0200	/SET AC 0401
1140	CLLN		/TRY TO GENERATE "LOAD CNT"
6134	CLCA		/READ COUNTER
6137	DCA	RXED	/SAVE TEST VALUE
1143	TAD	RXED	/STORE IT
1053	SNA CLA		
7050	JMS I	ERROR	/CHECK MONITOR
4430	JMS I		/LOAD CNT GATES FUNCTIONED WITH MODE 1=1 IN ERROR
1147	JMS I		
4426	TS129M		/MESSAGE POINTER
5747	HLT		/ERROR HALT
7402	SKP CLA		/TO NEXT TEST
1152	TS129		/ISE LOOP, SCOPE LOOP
1131	CLA CLL	CHM	/SET AC=7777
7340	DCA	REGA	/RESET REGA FOR NEXT TEST
3046			

/GLITCH TEST OF LOAD CNT GATES

1156	4445	JMS I	RANDOM	/GET RANDOM NUMBER
1157	6133	CLAB		/SEND IT TO BUFFER
1160	3054	DCA		/SAVE IT
1161	1116	TAD	K0200	/SET AC 04=1
1162	6132	CLR		/SET MODE 1=1
1163	7200	CLA		/CLEAR AC
1164	1120	TAD	K0300	/SET AC 04,05=1
1165	6132	CLR		/SET MODE 2=1
1166	7200	CLA		/CLEAR AC
1167	2047	ISE	REG8	/DONE?
1170	5361	JMP	,=7	/BACK 4096 TIMES
1171	6137	CLCA		/READ COUNTER
1172	3053	DCA	RXED	/SAVE IT
1173	1053	TAD	RXED	/RESTORE IT
1174	7650	SNA CLA		/ZERO?
1175	4430	JMS I	ERROR	/CHECK MONITOR
1176	4426	JMS I	ERROR	/THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER
1177	5774	TST30H		/MESSAGE POINTER
1200	7402	HLT		/ERROR HALT
1201	7200	CLA		/TO NEXT TEST
1202	1156	TST30		/IS LOOP SCOPE LOOP
1203	7340	CLA CL	CMA	/SET AC=7777
1204	3046	DCA	REGA	/PRESSET REGA FOR NEXT TEST

/GENERAL GATE SHAKING TEST OF THE MODE-FLIP FLOPS

ADDRESS	INSTR	DATA	COMMENT
1225	JMS I	4445	TS131, RANDOM
1226	CLAB	6133	
1207	DCA	3054	
1210	TAD	1047	
1211	REGB	7006	
1212	RTL	7006	
1213	RTL	7006	
1214	AND	0125	
1215	CLRL	6132	
1216	CHA	7040	
1217	AND	0125	
1220	CLRL	6132	
1221	ISZ	2047	
1222	REGB	0510	TS131+3
1223	JMP	0510	
1224	DCA	3053	
1225	CLBA	6136	
1226	TAD	1053	
1227	CIA	7041	
1230	SEA CLA	7640	
1231	JMP	5237	
1232	CLCA	6137	
1233	DCA	3047	
1234	TAD	1047	
1235	SNA CLA	7650	
1236	JMS I	4430	ERROR
1237	JMS I	4526	ERROR
1240	TS131M	6021	
1241	HLT	7402	
1242	CLA	7200	
1243	TS131	1205	
1244	REGB	3047	
1225	/GET RANDOM NUMBER		
1226	/SEND IT TO BUFFER		
1207	/SAVE IT		
1210	/GET TEST COUNTER		
1211	/ROTATE TWO LEFT		
1212	/ROTATE TWO LEFT		
1213	/ROTATE TWO LEFT		
1214	/INSURE THAT MODE 0.1,2=1		
1215	/SEND RANDOM NUMBER TO CONTROL REGISTER		
1216	/COMPLEMENT		
1217	/INSURE THAT MODE 0.1,2=1		
1220	/SET TO COMPLEMENT OF THE NUMBER		
1221	/DONE?		
1222	/BACK 4096 TIMES		
1223	/GET TEST VALUE FROM BUFFER		
1224	/SAVE IT		
1225	/RESTORE IT		
1226	/COMPLEMENT		
1227	/SUBTRACT TEST NUMBER		
1230	/EQUAL?		
1231	/BUFF CHANGED IN ERROR		
1232	/READ COUNTER		
1233	/SAVE IT		
1234	/RESTORE IT		
1235	/STILL ZERO?		
1236	/CHECK MONITOR		
1237	/COUNTER CHANGED IN ERROR		
1240	/MESSAGE POINTER		
1241	/ERROR HALT		
1242	/TO NEXT TEST		
1243	/ISZ LOOP/ SCOPE LOOP		
1244	/CLEAR FOR NEXT ISZ LOOP		

/DOES MODE 2 1=0 CLK CNT?

TS132, JMS I RANDOM

/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/ZERO MODE 2
/AC 05=1
/GENERATE "CLR CNT"

/CLEAR STATUS
/CLEAR AC
/SET AC 04=1
/GENERATE "LOAD CNT"

/READ COUNTER
/SAVE IT
/CLEAR BUF OR OVERFLOW WILL RELOAD CNT

/SUBTRACT TEST NUMBER
/COMPLEMENT
/RESTORE IT

/EQUAL?
/CHECK MONITOR
/MODE 2 1=0 DID IT

/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP

TS133, TAD K0100

CLRA
CLCA
DCA
TAD
SNA CLA
JMS I ERROR
TS133M
HLT
SKP
TS133

/SET AC 05=1
/GENERATE "CLR CNT"
/READ COUNTER
/SAVE IT
/RESTORE IT
/ZERO?
/CHECK MONITOR
/MODE 2 0=1 FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP

1245 4445
1246 6133
1247 3054
1250 6132
1251 1114
1252 6132
1253 6135
1254 7200
1255 1116
1256 6134
1257 7200
1260 6132
1261 6137
1262 3053
1263 6133
1264 1053
1265 7041
1266 1054
1267 7650
1270 4430
1271 4426
1272 6056
1273 7402
1274 7410
1275 1245
1276 1114
1277 6132
1301 3053
1302 1053
1303 7650
1304 4430
1305 4426
1306 6102
1307 7402
1310 7410
1311 1276

/DOES COUNTER OVERFLOW SET OVERFLOW FLAG?

1312	7300	CLA CL	TS134,	/CLEAR AC
1313	6132	CLR		/CLEAR STATUS
1314	1114	TAD	K0100	/SET AC 0501
1315	6132	CLR		/O TO COUNTER
1316	6135	CLSA		/CLEAR CLOCK STATUS
1317	7330	CLA CL	CHL RAR	/SET AC 04000
1320	6133	CLAB		/SET BUFFER TO 4000
1321	7300	CLA CL		/CLEAR AC
1322	1116	TAD	K0200	/SET AC 0401
1323	6134	CLCN		/LOAD CNT (00) 01 1 TO OVERFLOW
1324	7300	CLA CL		/CLEAR AC
1325	6133	CLAB		/CLEAR BUFFER
1326	6132	CLR		/CLEAR ALL MODES
1327	1114	TAD	K0100	/SET AC 0501
1330	6132	CLR		/GEN "CLR CNT"
1331	6135	CLSA		/GET STATUS OF CLOCK
1332	7710	SPA CLA		/OVERFLOW SET?
1333	4430	JMS I	ERROR	/CHECK MONITOR
1334	4426	JMS I	ERROR	/OVERFLOW NOT SET
1335	6126	TS134M		/MESSAGE POINTER
1336	7402	HLT		/ERROR HALT
1337	7410	SKP		/TO NEXT TEST
1340	1312	TS134		/ISZ LOOP1 SCOPE LOOP
1341	7300	CLA CL		/RESET SEND
1342	3054	DCA		/SET AC 7777
1343	7340	CLA CL	CHL	/RESET ISZ COUNTER FOR NEXT TEST
1344	3046	DCA	REGA	

/DOES CLSA (6135) CLEAR OVERFLOW FLOP?

1345	7500	TS135, CLA CL	/CLEAR AC
1346	6132	CLR	/CLEAR ALL MODES
1347	1114	TAD K0100	/SET AC 05#1
1350	6132	CLR	/GEN "CLR CNT"
1351	6135	CLSA	/CLEAR CLOCK STATUS
1352	7330	CLA CL RAR	/SET AC=4000
1353	6133	CLAB	/SET BUF=4000 OCTAL
1354	7300	CLA CL	/CLEAR AC
1355	1116	TAD K0200	/SET AC 04#1
1356	6134	CLCN	/GEN LOAD CNT
1357	7300	CLA CL	/CLEAR AC
1360	6133	CLAB	/ZERO BUF
1361	6132	CLR	/CLEAR ALL MODES
1362	1114	TAD K0100	/SET AC 05#1
1363	6132	CLR	/GEN "CLR CNT"
1364	7300	CLA CL	/CLEAR AC
1365	6135	CLSA	/GET STATUS BIT 0#1
1366	7300	CLA CL	/CLEAR AC
1367	6135	CLSA	/GET STATUS BIT 0#0
1370	7700	SMA CLA	/OVERFLOW SET?
1371	4430	JMS !	/CHECK MONITOR
1372	4426	JMS !	/CLSA FAILED TO CLEAR OVERFLOW FLOP
1373	6132	TS135M	/MESSAGE POINTER
1374	7402	HLT	/ERROR HALT
1375	7410	SKP	/TO NEXT TEST
1376	1545	TS135	/ISE LOOP SCOPE LOOP
1377	7340	CLA CL CMA	/SET AC=7777
1400	3046	DCA	/PRESET REGA FOR NEXT TEST

/TEST OVERFLOW SKIP

TST36, CLA CLL

CLA CLL K0100

CLL K0100

CLL K0100

CLL K0100

CLL K0100

CLL K0100

CLL K0100

CLL K0100

CLL K0100

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CLL K0100

CLL K0100

CLL K0100

CLL K0100

1401 7300

1402 6132

1403 1114

1404 6132

1405 6135

1406 7330

1407 6133

1408 7330

1409 6133

1410 7330

1411 1116

1412 6134

1413 7330

1414 6133

1415 6132

1416 1114

1417 6132

1418 7330

1419 6131

1420 6131

1421 6131

1422 4530

1423 4426

1424 6177

1425 7402

1426 7410

1427 1401

1428 7340

1429 3046

/

/TEST OVERFLOW SKIP

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

ION 6002

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ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

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ION 6002

/TEST FOR NO INTERRUPT

TST37, TAD

TAD PNTA

DCA 3052

ION 6001

ION 7000

NOP 6002

ION 6002

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```

/SET INT ENABLE
/
1447 1114 TAD R3132
1450 6134 CLEN
1451 7300 CLA CL
1452 6131 CLSK
1453 7410 SKP
1454 4430 JMS I ERROR
1455 4426 JMS I ERROR
1456 6240 TS138M
1457 7402 HLT
1460 7410 SKP
1461 1447 TS138
1462 7340 CLA CL CMA
1463 3046 DCA REGA
/TEST FOR CLOCK INTERRUPT
/
1464 1034 TAD PNTB
1465 3052 DCA RETURN
1466 6001 ION
1467 7000 NOP
1470 6002 IOF
1471 7410 SKP
1472 4430 JMS I ERROR
1473 4426 JMS I ERROR
1474 6257 TS139M
1475 7402 HLT
1476 7410 SKP
1477 1464 TS139
1480 7340 CLA CL CMA
1501 3046 DCA REGA
/
1447 1114 TAD R3132
1450 6134 CLEN
1451 7300 CLA CL
1452 6131 CLSK
1453 7410 SKP
1454 4430 JMS I ERROR
1455 4426 JMS I ERROR
1456 6240 TS138M
1457 7402 HLT
1460 7410 SKP
1461 1447 TS138
1462 7340 CLA CL CMA
1463 3046 DCA REGA
/SET AC 0541
/TURN ON CLOCK OVERFLOW INT
/CLEAR AC
/INTERRUPT SET?
/TO HERE IF INTERRUPT NOT SET
/CHECK MONITOR
/CLK FAILED TO SKIP OVERFLOW EN OV INTS1
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

/GET RETURN POINTER TO LOC8
/PUT IT IN INTERRUPT HANDLER
/ENABLE INTERRUPTS
/WAIT
/DISABLE INTERRUPTS
/TO HERE IF NO INTERRUPT
/CHECK WITH MONITOR
/CLOCK INT FAILED TO INTERRUPT
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

/TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE

1502	7300	CLA CLL	
1503	6134	CLEN	
1504	6131	CLSK	
1505	4430	JMS I	ERROR
1506	4426	JMS I	ERROR
1507	6277	TS140M	
1510	7402	HLT	
1511	7410	SKP	
1512	1502	TS140	
1513	7340	CLL CLA CMA	
1514	3046	DCA	REGA

/PRESSET REGA FOR NEXT TEST

/SET AC=7777

/ISZ LOOP1 SCOPE LOOP

/TO NEXT TEST

/ERROR HALT

/MESSAGE POINTER

/OVERFLOW ENABLE MON'T ZERO

/CHECK MONITOR

/INTERRUPT AVAILABLE?

/CLOCK ENABLE

/CLEAR AC

/TEST WITH FLAG ZERO OVERFLOW SET

1515	1114	TAD	K0100
1516	6134	CLEN	
1517	7300	CLA CLL	
1520	6132	CLLR	
1521	6135	CLSA	
1522	7300	CLA CLL	
1523	6131	CLSK	
1524	4430	JMS I	ERROR
1525	4426	JMS I	ERROR
1526	6320	TS141M	
1527	7402	HLT	
1530	7410	SKP	
1531	1515	TS141	
1532	7340	CLA CLL CMA	
1533	3046	DCA	REGA

/PRESSET REGA FOR NEXT TEST

/SET AC=7777

/ISZ LOOP1 SCOPE LOOP

/TO NEXT TEST

/ERROR HALT

/MESSAGE POINTER

/BAD INTERRUPT CONDITION STILL EXISTS

/CHECK MONITOR

/INTERRUPT SET?

/CLEAR AC

/STOP THE CLOCK

/READ AND ZERO FLAG

/CLEAR AC

/ENABLE INTERRUPTS

/SET AC 0501

/TEST INT OVERFLOW

1534	1035	TAD	TS142,
1535	3052	DCA	RETURN
1536	6001	ION	
1537	7000	NOP	
1540	6002	IOF	
1541	4432	JMS I	ERROR
1542	4426	JMS I	ERROR
1543	6340	TS142M	
1544	7402	HLT	
1545	7410	SKP	
1546	1534	TS142	
1547	2047	ISZ	REG8
1550	5457	JMP I	TS135N
1551	7340	CLA CLL CMA	
1552	3046	DCA	REGA

LOC,

/GET RETURN POINTER TO LOG

/PUT IT IN INTERRUPT HANDLER

/ENABLE INTERRUPTS

/WAIT

/DISABLE INTERRUPTS

/CHECK MONITOR

/ILLEGAL CLOCK INTERRUPT

/MESSAGE POINTER

/ERROR HALT

/TO NEXT TEST

/ISZ LOOP1 SCOPE LOOP

/INCREMENT PASS COUNTER

/CROSS-PAGE TO TEST 35 4000 TIMES

/SET AC=7777

/PRESSET REGA FOR NEXT TEST

/COUNTER CARRY TESTING
 /COUNTER PRESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION
 /DOES BIT 11 SET UP?

1593	7280	CLA	TS143,	/CLEAR AC
1594	6132	CLR		/CLEAR ALL MODES
1595	6133	CLAB		/CLEAR BUF
1596	1114	TAD	K0100	/SET AC 091
1597	6132	CLR		/GEN "CLR CNT"
1598	6135	CLSA		/CLEAR STATUS
1599	7280	CLA		/CLEAR AC
1600	3025	DCA	CNTR	/CLEAR COUNTER
1601	3024	DCA	SEND	/CLEAR SEND
1602	6133	CLAB		/CLEAR BUFFER
1603	1115	TAD	K0200	/MODE 1
1604	6134	CLCN		/ENABLE MODE
1605	7300	CLA	CLL	/CLEAR AC
1606	1137	TAD	K5100	/SELECT 100 HZ RATE TO BE USED IN TEST 54
1607	6132	CLR		/ENABLE RATE
1608	6137	CLCA		/READ COUNTER
1609	3053	DCA		/SAVE IT
1610	1853	TAD	RXED	/FETCH IT
1611	1144	TAD	M001	/BIT 11 AND ONLY BIT 11 SET?
1612	7290	SNA	CLA	/IF NOT, WAIT A WHILE
1613	5464	JMP	UP43	/SET GO CHECK MONITOR (1.44)
1614	2025	ISZ	CNTR	/TIMER DONE?
1615	5422	JMP	DN43	/NO, GO BACK (1.7)
1616	7410	SKP		/TO HERE IF BAD BIT
1617	4420	JMS	ERROR	/CHECK MONITOR
1618	4420	JMS	ERROR	/BIT 11 FAILED TO GET SET BY A CLOCK PULSE
1619	6360	TS143H		/MESSAGE POINTER
1620	7102	HLT		/ERROR HALT
1621	7410	SKP		/TO NEXT TEST
1622	1593	TS143		/188 LOOP SCOPE LOOP
1623	7340	CLA	CLL	/SET AC=7777
1624	3046	DCA	REGA	/PRESET REGA FOR NEXT TEST

/DOES BIT 10 SET UP?

/TST44, CLA

CLA CLR

CLAB CLR

CLAB CLR

CLSA

CLA

DCA

TAD K0001

CLAB

DCA

SEND

TAD K0200

CLEN

CLA CLR

TAD K5300

CLLR

CLCA

DCA

RXED

TAD

TAD

SNA CLA

JMP

ISZ

JMP

SKP

JMS I

JMS I

TST44M

HLT

SKP

TST44

CLA CLR

DCA

1613 7200
 1614 6132
 1615 6133
 1616 6132
 1617 6135
 1618 7200
 1621 3025
 1622 1075
 1623 6133
 1624 3054
 1625 1116
 1626 6134
 1627 7300
 1630 1137
 1631 6132
 1632 6137
 1633 3053
 1634 1053
 1635 1145
 1636 7050
 1637 5243
 1640 2025
 1641 5232
 1642 7410
 1643 4430
 1644 4426
 1645 6377
 1646 7402
 1647 7410
 1650 1013
 1651 7340
 1652 3046

/CHECK MONITOR
 /BIT 10 FAILED TO GET SET BY COUNTING
 /MESSAGE POINTER
 /ERROR HALT
 /TO NEXT TEST
 /ISE LOOP/ SCOPE LOOP
 /SET AG=7777
 /RESET REGA FOR NEXT TEST
 /BIT 10, AND ONLY BIT 10, SET?
 /RESET FOR BIT 10

/DOES BIT 9 SET UP?

1653	7200	CLA	TST45,
1654	6132	CLR	
1655	6133	CLAB	
1656	1114	TAD	K0100
1657	6132	CLR	
1660	6135	CLSA	
1661	7200	CLA	
1662	3025	DCA	CNTR
1663	1077	TAD	K0003
1664	6133	CLAB	
1665	3054	DCA	SEND
1666	1116	TAD	K0200
1667	6134	CLCN	
1670	7300	CLA	CLL
1671	1137	TAD	K5100
1672	6132	CLR	
1673	6137	CLCA	
1674	3053	DCA	RXED
1675	1053	TAD	RXED
1676	1146	TAD	M0004
1677	7650	SNA	CLA
1700	5304	JMP	44
1701	2025	ISZ	CNTR
1702	5273	JMP	7
1703	7410	SKP	
1704	4430	JMS	1
1705	4426	JMS	1
1706	6416	TST45M	
1707	7402	HLT	
1710	7410	SKP	
1711	1653	TST45	
1712	7340	CLA	CLL
1713	3046	DCA	REGA

/CHECK MONITOR
/BIT 9 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC=7777
/RESET REGA FOR NEXT TEST

/BIT 09, AND ONLY BIT 09, SET?

/RESET FOR BIT 09

/DOES BIT 8 SET UP?

1714	7200	CLA	TST46,
1715	6132	CLL	
1716	6133	CLAB	
1717	1114	TAD	K0100
1720	6132	CLL	
1721	6135	CLSA	
1722	7200	CLA	
1723	3025	DCA	
1724	1101	TAD	K0007
1725	6133	CLAB	
1726	3054	DCA	
1727	1116	TAD	K0200
1730	6134	CLEN	
1731	7300	CLA CLL	
1732	1137	TAD	K5100
1733	6132	CLL	
1734	6137	CLCA	
1735	3053	DCA	
1736	1053	TAD	RXED
1737	1147	TAD	M0010
1740	7050	SNA CLA	
1741	5345	JMP	.44
1742	2025	ISZ	CNTR
1743	5334	JMP	.7
1744	7410	SKP	
1745	4430	JMS I	ERROR
1746	4426	JMS I	ERROR
1747	6435	TST46M	
1750	7402	HLT	
1751	7410	SKP	
1752	1714	TST46	
1753	7340	CLA CLL	
1754	3046	DCA	REGA

/CHECK MONITOR
/BIT 8 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/BIT 08 AND ONLY BIT 08, SET?

/PRESET FOR BIT 08

/DOES BIT 7 SET UP?

1755	7200	CLA	TS147,	
1756	6132	CLR		
1757	6133	CLAB		
1760	1114	TAD	K0100	
1761	6132	CLR		
1762	6133	CLSA		
1763	7200	CLA		
1764	3025	DCA		
1765	1106	TAD	K0017	
1766	6133	CLAB		
1767	3054	DCA		
1768	1116	TAD	K0200	
1771	6134	CLCN		
1772	7300	CLA CL		
1773	1137	TAD	K5100	
1774	6132	CLR		
1775	6137	CLCA		
1776	3053	DCA		
1777	1053	TAD		
2000	1150	TAD	M0020	
2001	7090	SNA CLA		
2002	5206	JMP	004	
2003	2025	ISZ	CNTR	
2004	5423	JMP	DN47	
2005	7410	SKP		
2006	4430	JMS	ERROR	
2007	4426	JMS	ERROR	
2010	6454	TS147M		
2011	7402	HLT		
2012	7410	SKP		
2013	1755	TS147		
2014	7340	CLA CL	CHY	
2015	3046	DCA		

```

/((=7)
/CHECK MONITOR
/BIT 7 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST
    
```

/PRESET FOR BIT 07

/BIT 07, AND ONLY BIT 07, SET?

/DOES BIT 6 SET UP?

2016	7200	CLA	TST48,
2017	6132	CLR	
2020	6133	CLAB	
2021	1114	TAD	K0100
2022	6132	CLR	
2023	6135	CLSA	
2024	7200	CLA	
2025	3025	DCA	
2026	1110	TAD	K0037
2027	6133	CLAB	
2030	3054	DCA	SEND
2031	1116	TAD	K0200
2032	6134	CLEN	
2033	7300	CLA	CLL
2034	1137	TAD	K5100
2035	6132	CLR	
2036	6137	CLCA	
2037	3053	DCA	RXED
2040	1053	TAD	RXED
2041	1151	TAD	M0040
2042	7650	SNA	CLA
2043	5247	JMP	44
2044	2025	ISZ	CNTR
2045	5236	JMP	47
2046	7410	SKP	
2047	4430	JMS	1
2050	4426	JMS	1
2051	6473	TST48H	
2052	7402	HLT	
2053	7410	SKP	
2054	2016	TST48	
2055	7340	CLA	CLL CMA
2056	3046	DCA	REGA

/CHECK MONITOR
/BIT 6 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/BIT 6 AND ONLY BIT 06, SET?

/PRESET FOR BIT 06

/DOES BIT 5 SET UP?

2057	7200	CLA	TS149,
2060	6132	CLR	
2061	6133	CLAB	
2062	1114	TAD	
2063	6132	CLR	
2064	6135	CLSA	
2065	7200	CLA	
2066	3025	DCA	
2067	1113	TAD	
2070	6133	CLAB	
2071	3094	DCA	
2072	1116	TAD	
2073	6134	CLEN	
2074	7300	CLA CL	
2075	1137	TAD	
2076	6132	CLR	
2077	6137	CLCA	
2100	3053	DCA	
2101	1053	TAD	
2102	1153	TAD	
2103	7050	SNA CLA	
2104	5310	JMP	
2105	2025	ISE	
2106	5277	JMP	
2107	7410	SKP	
2110	4430	JMS I	
2111	4426	JMS I	
2112	6912	TS149H	
2113	7402	HLT	
2114	7410	SKP	
2115	2057	TS149	
2116	7340	CLA CL	
2117	3046	DCA	

/BIT 05, AND ONLY BIT 05, SET?

/PRESET FOR BIT 05

/CHECK MONITOR
/BIT 5 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/DOES BIT 4 SET UP?

2120	2120	CLA	TST50,
2121	6132	CLR	
2122	6133	CLAB	
2123	1114	TAD	K0100
2124	6132	CLR	
2125	6135	CLSA	
2126	7200	CLA	
2127	3025	DCA	CNTR
2130	1115	TAD	K0177
2131	6133	CLAB	
2132	3054	DCA	SEND
2133	1116	TAD	K0200
2134	6134	CLEN	
2135	7300	CLA CL	
2136	1137	TAD	K0100
2137	6132	CLR	
2140	6137	CLCA	
2141	3053	DCA	RXED
2142	1053	TAD	RXED
2143	1154	TAD	M0200
2144	7050	SNA CLA	
2145	5054	JMP	144
2146	2025	ISE	144
2147	5340	JMP	144
2150	7410	SKP	144
2151	4430	JMS I	ERROR
2152	4426	JMS I	ERROR
2153	6531	TST50H	
2154	7402	HLT	
2155	7410	SKP	
2156	2120	TST50	
2157	7340	CLA CL	CMA
2160	3046	DCA	REGA

/CHECK MONITOR
/BIT 4 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/BIT 04, AND ONLY BIT 04, SET?

/PRESET FOR BIT 04

/DOES BIT 3 SET UP?
/TST51, CLA

2161	7200	CLA	
2162	6132	CLR	
2163	6133	CLAB	
2164	1114	TAD	K0100
2165	6132	CLR	
2166	6135	CLSA	
2167	7200	CLA	
2170	3025	DCA	CNTR
2171	1121	TAD	K0377
2172	6133	CLAB	
2173	3034	DCA	SEND
2174	1116	TAD	K0200
2175	6134	CLEN	
2176	7300	CLA CL	
2177	1137	TAD	K5100
2200	6132	CLR	
2201	6137	CLCA	
2202	3053	DCA	RXED
2203	1053	TAD	RXED
2204	1155	TAD	M0400
2205	7650	SNA CLA	
2206	5212	JMP	'04
2207	2025	ISZ	CNTR
2210	5201	JMP	'07
2211	7410	SKP	
2212	4430	JMS 1	ERROR
2213	4426	JMS 1	ERROR
2214	6550	TST51M	
2215	7402	HLT	
2216	7410	SKP	
2217	2161	TST51	
2220	7340	CLA CL	CMA
2221	3046	DCA	REGA

/CHECK MONITOR
/BIT 3 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/BIT 03, AND ONLY BIT 03, SET?

/PRESET FOR BIT 03

/DOES BIT 2 SET UP?

2222	7200	CLA	TST52,
2223	6132	CLL	
2224	6133	CLAB	
2225	1114	TAD	K0100
2226	6132	CLL	
2227	6135	CLSA	
2230	7200	CLA	
2231	3025	DCA	CNTR
2232	1126	TAD	K0777
2233	6133	CLAB	
2234	3054	DCA	SEND
2235	1116	TAD	K0220
2236	6134	CLL	
2237	7300	CLA	CLL
2240	1137	TAD	K5100
2241	6132	CLL	
2242	6137	CLCA	
2243	3053	DCA	RXED
2244	1053	TAD	RXED
2245	1156	TAD	M1000
2246	1150	SNA	CLA
2247	5253	JMP	100
2250	2025	ISZ	CNTR
2251	5242	JMP	107
2252	7410	SKP	
2253	4430	JMS	1
2254	4426	CLL	ERROR
2255	6567	TST52M	
2256	7402	HLT	
2257	7410	SKP	
2260	2222	TST52	
2261	7340	CLA	CLL
2262	3046	DCA	REGA

/CHECK MONITOR
/BIT 2 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/BIT 02, AND ONLY BIT 02, SET?

/PRESET FOR BIT 02

/DOES BIT 1 SET UP?

2263	7200	CLA	TST53,
2264	6132	CLR	
2265	6133	CLAB	
2266	1114	TAD	K0100
2267	6132	CLR	
2270	6135	CLSA	
2271	7200	CLA	
2272	3025	DCA	CNTR
2273	1131	TAD	K1777
2274	6133	CLAB	
2275	3054	DCA	SEND
2276	1116	TAD	K0200
2277	6134	CLCN	
2300	7300	CLA	CLL
2301	1137	TAD	K5100
2302	6132	CLR	
2303	6137	CLCA	
2304	3053	DCA	RXED
2305	1053	TAD	RXED
2306	1160	TAD	M2000
2307	7650	SNA	CLA
2310	5314	JMP	44
2311	2025	ISA	CNTR
2312	5303	JMP	7
2313	7410	SKP	
2314	4430	JMS	1
2315	4426	JMS	1
2316	6006	TST53H	
2317	7402	HLT	
2320	7410	SKP	
2321	2263	TST53	
2322	7340	CLA	CLL
2323	3046	DCA	REGA

/CHECK MONITOR
/BIT 1 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/152 LOOP1 SCOPE LOOP
/SET AC=7777
/PRESSET REGA FOR NEXT TEST

/BIT 01, AND ONLY BIT 01, SET?

/PRESSET FOR BIT 01

/DOES BIT 0 SET UP?

2324	7200	CLA	TST54,
2325	6132	CLR	
2326	6133	CLAB	
2327	1114	TAD	
2328	6132	CLR	
2329	6133	CLSA	
2330	7200	CLA	
2331	3025	DCA	
2332	1334	TAD	
2333	6133	CLAB	
2334	3054	DCA	
2335	1116	TAD	
2336	6134	CLEN	
2337	7300	CLA CL	
2338	1137	TAD	
2339	6132	CLR	
2340	6137	CLCA	
2341	3053	DCA	
2342	1053	RXED	
2343	1361	TAD	
2344	7050	SNA CLA	
2345	5355	JMP	
2346	2025	ISE	
2347	5344	JMP	
2348	7410	SKP	
2349	4430	JMS I	
2350	4426	JMS I	
2351	6025	TST54M	
2352	7402	HLT	
2353	7410	SKP	
2354	2324	TST54	
2355	7340	CLA CL	
2356	3046	DCA REGA	

/BIT 00, AND ONLY BIT 00, SET?

/PRESET FOR BIT 00

/CHECK MONITOR
/BIT 0 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA FOR NEXT TEST

/DOES COUNTER COUNT NORMALLY AND AT ALL RATES?
/CHECK 400 KHZ RATE

2365	7300	CLA CLL	TST55,		/CLEAR AC
2366	1157	TAD M5400			/GET PRESET
2367	3047	DCA REG8			/SET UP FOR TIMER
2370	1127	TAD K1000			/GET AC 02
2371	6132	CLLR			/SET 400KHZ RATE
2372	7300	CLA CLL			
2373	2047	ISZ REG8	BK55,		/INCREMENT COUNT
2374	7410	SKP			/TIME OK
2375	5467	JMP I UP55			/TIMER NOT OK (1.5)
2376	6135	CLSA			/GET STATUS
2377	7000	NOP			/WAIT
2401	5424	JMP I DN55			/OVERFLOW?
2402	4430	JMS I NERROR			/TRY AGAIN (1.5)
2403	4426	JMS I ERROR			/CHECK MONITOR
2404	6044	TST55M			/400 KC FAILED
2405	7402	HLT			/MESSAGE POINTER
2406	7410	SKP			/ERROR HALT
2407	2365	TST55			/TO NEXT TEST
2410	7340	CLA CLL CMA			/ISZ LOOP1 SCOPE LOOP
2411	3046	DCA REGA			/SET AC = 7777
2412	7300	CLA CLL	TST56,		/PRESET REGA
2413	1163	TAD M5400			
2414	3047	DCA REG8			/CLEAR AC
2415	1132	TAD K2000			/GET PRESET
2416	6132	CLLR			/SET 100 KHZ RATE
2417	7300	CLA CLL			
2420	2047	ISZ			/INCREMENT COUNT
2421	7410	SKP			/TIMER OK
2422	5230	JMP			/TIMER NOT OK
2423	6135	CLSA			/GET STATUS
2424	7000	NOP			/WAIT
2425	7700	SMA CLA			/OVERFLOW?
2426	5220	JMP			/TRY AGAIN
2427	4430	JMS I NERROR			/CHECK MONITOR
2430	4426	JMS I ERROR			/400 KC FAILED
2431	6661	TST56M			/MESSAGE POINTER
2432	7402	HLT			/ERROR HALT
2433	7410	SKP			/TO NEXT TEST
2434	2412	TST56			/ISZ LOOP1 SCOPE LOOP
2435	7340	CLA CLL CMA			/SET AC = 7777
2436	3046	DCA REGA			/PRESET REGA

/CHECK 10 KHZ RATE

/TEST 10 KHZ RATE

2437	7300	CLA CL	19197,
2440	1147	TAD	
2441	3050	DCA	
2442	1156	TAD	
2443	3047	DCA	
2444	1153	REG	
2445	6132	CLR	
2446	7300	CLA CL	
2447	2047	ISZ	
2450	7410	SKP	
2451	2050	ISZ	
2452	7410	SKP	
2453	5261	JMP	
2454	6135	CLSA	
2455	7000	NOP	
2456	7700	SMA CLA	
2457	5247	JMP	
2460	4430	JMS I	
2461	4426	JMS I	
2462	6676	TS157M	
2463	7402	HLT	
2464	7410	SKP	
2465	2437	TS157	
2466	7340	CLA CL	
2467	3046	DCA	
2470	3047	DCA	

/TEST 1KHZ RATE

2471	7000	CLA CL	19158,
2472	1153	TAD	
2473	3050	DCA	
2474	1156	TAD	
2475	6132	CLR	
2476	7300	CLA CL	
2477	2047	ISZ	
2501	2050	ISZ	
2502	7410	SKP	
2503	5311	JMP	
2504	6135	CLSA	
2505	7000	NOP	
2506	7700	SMA CLA	
2507	5277	JMP	
2510	4430	JMS I	
2511	4426	JMS I	
2512	6713	TS158M	
2513	7402	HLT	
2514	7410	SKP	
2515	2471	TS158	
2516	7340	CLA CL	
2517	3046	DCA	

/CLEAR AC
/GET P-RESET
/SET UP FOR X10

/SET 10KC RATE

/INCREMENT COUNT
/TIMER OK
/INCREMENT MULTIPLIER
/MULTIPLIER OK
/TIMER NOT OK
/GET STATUS
/WAIT
/OVERFLOW?
/TRY AGAIN
/CHECK MONITOR
/10KC FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA
/CLEAR REGB

/CLEAR AC
/GET PRESET
/SET UP FOR X100
/SET 1KC RATE
/INCREMENT COUNT
/TIMER OK
/INCREMENT MULTIPLIER
/MULTIPLIER OK
/TIMER NOT OK
/GET STATUS
/WAIT
/OVERFLOW?
/TRY AGAIN
/CHECK MONITOR
/1KC FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA
/DCA

REC'D

7300 3047 1153 3050 1155 6133 7300 1116 6134 7300 1137 6132 7500 2047 7410 2050 7410 5347 6135 7000 7700 5335 4426 6727 7402 7610 2520 1153 3046 3047

```

/CLEAR AC
/SET FOR X100
/GET PRESET
/SET PRESET
/SET 100 CPS RATES
/ENABLE RATE
/CLEAR AC
/SET AC 05M1
/ENABLE PRESET
/SET 100 CPS RATES
/ENABLE RATE
/CLEAR AC
/INCREMENT TIME
/INCREMENT MULTIPLIER
/TIME OK
/TIME NOT OK RATE FAILED
/GET STATUS
/WAIT
/OVERFLOW?
/TRY AGAIN
/CHECK MONITOR
/RATE 100 WE FAILED
/CLEAR REGD

```

8038 44370/

/CHECK CHANNEL 1 INPUT RATE (RATE MUST BE BETWEEN 47 CPS AND 180 KHZ)
/((INSURE THAT AN INPUT IS PROVIDED))

2557	7300	CLC CLR	TS160.	/CLEAR AC
2560	1107	TAD	K0020	/GET AC 05
2561	6134	CLEN		/ENABLE CHANNEL 1 INPUT
2562	7200	CLA		/GET AC 00, 01
2563	1142	TAD	K0000	/ENABLE RATE=CHANNEL 1 INPUT
2564	6132	CLLR		/CLEAR AC
2565	7300	CLC CLR	TS160N.	/GET COUNTER
2566	6137	CLCA		/SAVE IT
2567	3054	DCA	SEND	/WAIT
2570	2047	ISE	REG8	/GET COUNTER
2571	5370	JMP	.-1	/SAVE IT
2572	6137	CLCA		/WAIT
2573	7041	CIA		/GET COUNTER
2574	1054	TAD	SEND	/2'S COMPLEMENT
2575	7040	SEA CLA		/COMPARE
2576	4430	JMS I		/HAS IT CHANGED?
2577	4426	JMS I	ERROR	/CHECK MONITOR
2600	6745	TS160M		/CHAN 1 LOCKED UP
2601	7402	HLT		/MESSAGE POINTER
2602	7410	SKP		/ERROR HALT
2603	2565	TS160N		/TO NEXT TEST

/SCOPE LOOP, 182 LOOP

3 CHANNEL 3 INPUT TESTS /SIMULATED

ADDRESS	INSTR	DATA	COMMENT
2624	TAD	K0001	/SET AC 12=1
2625	CLEN		/ENABLE CHANNEL 3
2626	CLLR		/SET EVENT FLOP
2627	CLLR		/SET SET PRE-EVENT FLOP
2618	CLA CLR		/CLEAR AD
2613	CLEN		/CLEAR ENABLES
2612	CLSA		/GET STATUS
2613	AND	K3777	/IGNORE O/FLO
2614	DCA		/SAVE IT
2615	CLSA		/GET STATUS AGAIN
2616	AND	K0003	/SAVE CHANNEL 3
2617	DCA		/SAVE IT
2620	TAD		/FETCH IT
2621	SZA CLA		/CHANNEL 3 07
2622	JMP I	UP61	/CLA DOESN'T 0 INPUT CH
2623	TAD		/GET STATUS
2624	CIA		/2'S COMPLEMENT
2625	TAD	K0003	/SUBTRACT SET
2626	SNA CLA		/EQUAL?
2627	JMS I		/CHECK MONITOR
2630	JMS I		/BOTH PRE-EVENT AND EVE
2631	TS161H		/MESSAGE POINTER
2632	HLT		/ERROR HALT
2633	SKP		/TO NEXT TEST
2634	TS161		/125 LOOP SCOPE LOOP

```

/SET AC 12.1
/ENABLE CHANNEL 3
/SET EVENT FLOP
/SET SET PREVENT FLOP
/CLEAR AD
/CLEAR ENABLES
/GET STATUS
/IGNORE O/FLO
/SAVE IT
/GET STATUS AGAIN
/SAVE CHANNEL 3
/FETCH IT
/CHANNEL 3 07
/CLSA DOESN'T 0 INPUT CHANNEL 3 (1:06)

```

/SIM INPUT TESTS CHAN 2

2635	1100	TAD	K0004
2636	6134	CLEN	
2637	6132	CLLR	
2640	6132	CLLR	
2641	7300	CLA CLL	
2642	6134	CLEN	
2643	6135	CLSA	
2644	0134	AND	K3777
2645	3054	DCA	
2646	6135	CLSA	
2647	0134	DCA	K0014
2650	3053	RXED	
2651	1053	TAD	
2652	7040	SEA CLA	
2653	5261	JMP	
2654	1054	TAD	
2655	7041	CIA	
2656	1104	TAD	K0014
2657	7050	SNA CLA	
2660	4420	JMS I	
2661	4426	JMS I	
2662	7010	TS162H	
2663	7402	HLT	
2664	7410	SKP	
2665	2635	TS162	

/SET AC 0001
/ENABLE CHAN 2
/SET EVENT FLOP
/SET PREVENT FLOP
/CLEAR AC
/CLEAR ENABLES
/GET STATUS
/IGNORE OFLO
/SAVE IT
/GET STATUS
/SAVE CHANNEL 2
/SAVE IT
/FETCH IT
/07
/CLSA DOESN'T 0 INPUT CHANNEL 2
/GET FIRST STATUS
/215 COMPLEMENT
/SUBTRACT SET
/EQUAL?
/CHECK MONITOR
/BOTH PRE-EVENT AND EVENT NOT SET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/192 LOOP1 SCOPE LOOP

/SIM INPUT TESTS CHAN 1

2666	1107	TS163, TAD	K0020	CLN	6134
2667	6134	CLN		CLN	6134
2670	6132	CLR		CLR	6132
2671	6132	CLR		CLR	6132
2672	7300	CLA CL		CLA CL	7300
2673	6134	CLEN		CLEN	6134
2674	6135	CLSA		CLSA	6135
2675	0134	AND	K377	AND	0134
2676	3054	DCA		DCA	3054
2677	6135	CLSA		CLSA	6135
2700	0112	AND	K0060	AND	0112
2701	3053	DCA		DCA	3053
2702	1053	TAD		TAD	1053
2703	7640	SZA CLA		SZA CLA	7640
2704	5312	JMP	106	JMP	5312
2705	1054	TAD		TAD	1054
2706	7041	CJA		CJA	7041
2707	1112	TAD	K0060	TAD	1112
2710	7650	SNA CLA		SNA CLA	7650
2711	4430	JMS 1		JMS 1	4430
2712	4426	JMS 1		JMS 1	4426
2713	7032	TS163M		TS163M	7032
2714	7402	HLT		HLT	7402
2715	7410	SKP		SKP	7410
2716	2666	TS163		TS163	2666
2717	7340	CLA CL		CLA CL	7340
2720	3046	DCA		DCA	3046

/SET AC 0791	
/SET ENABLE	
/SET EVENT FLOP	
/SET PREVENT FLOP	
/CLEAR AC	
/CLEAR ENABLES	
/GET STATUS	
/IGNORE O/FLO	
/SAVE IT	
/GET STATUS	
/SAVE CHANNEL 1	
/SAVE IT	
/FETCH IT	
/ZERO7	
/CLSA DOESN'T 0 INPUT CHANNEL 1	
/GET FIRST STATUS	
/215 COMPLEMENT	
/SUBTRACT SET	
/EQUAL?	
/CHECK MONITOR	
/BOTH PRE-EVENT AND EVENT NOT SET	
/MESSAGE POINTER	
/ERROR HALT	
/TO NEXT TEST	
/132 LOOP/ SCOPE LOOP	
/SET AC=7777	
/PRESSET REGA	

/TEST INPUT CHANNEL INTERRUPT CHAN 1

2721	1036	TAD	PNTD	/GET RETURN POINTER TO LOGD
2722	3052	DCA	RETURN	/SET UP INTERRUPT RETURN
2723	1112	TAD	K0060	/ENABLE INPUT AND INTERRUPT
2724	6134	CLEN		/ENABLE
2725	6132	CLLR		/SIMULATE INPUT CHANNEL ONE
2726	6001	ION		/ENABLE INTERRUPTS
2727	7000	NOP		/WAIT
2730	7410	SKP		/NO INTERRUPT
2731	4430	JMS I	ERROR	/CHECK MONITOR
2732	4426	JMS I	ERROR	/NO INTERRUPT ERROR
2733	7054	TS164H		/MESSAGE POINTER
2734	7402	HLT		/ERROR HALT
2735	7610	SKP CLA		/TO NEXT TEST
2736	2721	TS164		/ISZ LOOP
2737	7340	CLA CLL	CMA	/SET AC=7777
2740	3046	DCA	REGA	/PRESSET REGA

/TEST WITH INTERRUPTS DISABLED

2741	1107	TAD	K0020	/CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2742	6134	CLEN		/ENABLE
2743	7300	CLA CLL		/CLEAR AC
2744	1037	TAD	PNTD	/GET RETURN POINTER TO LOGC
2745	3052	DCA	RETURN	/PUT IT IN INTERRUPT HANDLER
2746	6001	ION		/ENABLE INTERRUPTS
2747	7000	NOP		/WAIT
2750	6002	IOF		/DISABLE INTERRUPTS
2751	6135	CLSA		/CHECK MONITOR
2752	4430	JMS I	ERROR	/CHECK MONITOR
2753	4426	JMS I	ERROR	/INTERUPT IN ERROR
2754	7072	TS165H		/MESSAGE POINTER
2755	7402	HLT		/ERROR HALT
2756	7610	SKP CLA		/TO NEXT TEST
2757	2741	TS165		/ISZ LOOP! SCOPE LOOP
2760	7340	CLA CLL	CMA	/SET AC=7777
2761	3046	DCA	REGA	/PRESSET REGA
2762	2047	ISZ	REG8	/DO THE PAIR OF TESTS 4096 TIMES
2763	5321	JMP	TS164	/BACK

/TEST INPUT CHANNEL INTERRUPT CHAN 2

/GET RETURN POINTER TO LOGG

/SET UP INTERRUPT RETURN

/SET AC 00, 0901

/ENABLE CHANNEL 2

/ENABLE RATES

/ENABLE INTERRUPTS

/WAIT

/TO HERE IF NO INTERRUPT

/CHECK MONITOR

/NO INTERRUPT

/MESSAGE POINTER

/ERROR HALT

/TO NEXT TEST

/ISZ LOOP1 SCOPE LOOP

/SET AC=7777

/PRESSET REGA

/TEST WITH INTERRUPTS DISABLED

TAD PNTG

OCA RETURN

TAD K0014

CLEN

CLL

ION

NOP

SKP

JMS 1

JMS 1

TS166M

HLT

SKP

TS166

CLA CLL CMA

DCA REGA

LOGG,

JMS 1

JMS 1

TS167M

HLT

SKP

TS167

CLA CLL CMA

DCA REGA

ISZ

JMP 1

TS166N

/BACK

/DO THIS PAIR OF TESTS 4096 TIMES

/PRESSET REGA

/SET AC=7777

/ISZ LOOP1 SCOPE LOOP

/TO NEXT TEST

/ERROR HALT

/MESSAGE POINTER

/CHECK MONITOR

/INTERUPT IN ERROR--CLEA EN EVENT 2 INT BAD

/TEST INPUT CHANNEL INTERRUPT CHAN 3

3027	1042	TAD	PATH	/GET RETURN POINTER TO LOGH
3030	3052	DCA	RETURN	/SET UP INTERRUPT RETURN
3031	1077	TAD	K0003	/SET AC10,11=1
3032	6134	CLEN		/ENABLE CHANNEL 3
3033	6132	CLLR		/ENABLE RATES
3034	6001	ION		/ENABLE INTERRUPTS
3035	7000	NOP		/WAIT
3036	6002	IOF		/DISABLE INTERRUPTS
3037	7410	SKP		/NO INTERRUPT
3040	4430	JMS I	NEROR	/CHECK MONITOR
3041	4426	JMS I	ERROR	/NO INTERRUPT
3042	7152	TST68H		/MESSAGE POINTER
3043	7402	HLT		/ERROR HALT
3044	7410	SKP		/TO NEXT TEST
3045	3027	TST68		/ISZ LOOP, SCOPE LOOP
3046	7340	CLA CLL	CHM	/SET AC=777
3047	3046	DCA	REGA	/PRESSET REGA

/TEST WITH INTERRUPTS DISABLED

3050	0075	AND	K0001	/SET AC 11=1
3051	6134	CLEN		/ENABLE CHANNEL 3
3052	7300	CLA CLL		/CLEAR IC
3053	1043	TAD	PMI	/GET RETURN POINTER TO LOGI
3054	3052	DCA	RETURN	/PUT IT IN INTERRUPT HANDLER
3055	6001	ION		/ENABLE INTERRUPTS
3056	7000	NOP		/WAIT
3057	6002	IOF		/DISABLE INTERRUPTS
3060	6135	CLSA		/CLEAR CLOCK STATUS
3061	4430	JMS I	NEROR	/CHECK MONITOR
3062	4426	JMS I	ERROR	/INTERRUPT IN ERROR
3063	7173	TST69H		/MESSAGE POINTER
3064	7402	HLT		/ERROR HALT
3065	7410	SKP		/TO NEXT TEST
3066	3050	TST69		/ISZ LOOP, SCOPE LOOP
3067	7340	CLA CLL	CHM	/SET AC=777
3070	3046	DCA	REGA	/PRESSET REGA
3071	2047	ISZ	REG8	/DO THIS PAIR OF TESTS 4026 TIMES
3072	5227	JMP	TST68	/BACK
3073	1151	TAD	M0040	
3074	3046	DCA	REGA	/PRESSET REGA IF NEXT TEST IS TO BE EXECUTED

/TEST OF INPUT CHANNEL 3
/KNOBS OF CHAN1, CHAN2, CHAN3 SET TO LINEFREQ, LEVEL IS DISABLED,

3075	6135	CLSA	TS170,	/CLEAR STATUS
3076	7300	CLA CL		/CLEAR AC
3077	6132	CLR		/CLEAR ALL MODES
3100	1077	TAD	K0003	/SET AC 10, 11=1
3101	6134	CLEN		/ENABLE CHAN3 INPUT AND INTER,
3102	7200	CLA		/CLEAR AC
3103	2047	ISZ	REG8	/INCREMENT TIMER
3104	7410	SKP		/NOT DONE YET
3105	5310	JMP	'+3	/TIMER OUT, ERROR CONDITION
3106	6131	CLSK		/SKIP ON CLOCK INTER,
3107	5303	JMP	'=4	/WAIT
3110	6135	CLSA		/GET CLOCK STATUS
3111	3053	DCA	RXED	/SAVE IT
3112	3047	DCA	REG8	/CLEAR COUNT
3113	1053	TAD	RXED	/RESTORE IT
3114	7041	CIA		/ZIS COMPLEMENT
3115	1076	TAD	K0002	/ADD EVENT 3
3116	7050	SNA CLA		/EQUAL?
3117	4430	JMS I	ERROR	/CHECK WITH MONITOR
3120	4426	JMS I	ERROR	/CHAN 3 EVENT NOT SET, OR PRE-EVENT WAS SET, OR OTHER CHAN UP
3121	7212	TS170M		/MESSAGE POINTER
3122	7402	HLT		/ERROR HALT
3123	7410	SKP		/TO NEXT TEST
3124	3075	TS170		/ISZ LOOP1 SCOPE LOOP
3125	1151	TAD	H0040	/PRESET REGA
3126	3046	DCA		


```

/CLEAR STATUS
/CLEAR AC
/CLEAR ALL MODES
/SET AC6,7=1
/ENABLE CHAN 1 INPUT AND INTERRUPT
/CLEAR AC
/CLEAR COUNT
/RESTORE IT
/COMPLEMENT
/ADD INPUT 1
/EQUAL?
/CHECK MONITOR
/CHAN 1 EVENT NOT SET, OR PREVENT WAS SET, OR OTHER CHAN UP
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISS LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA

```

/TEST FAST SAMPLE MODE IF BIT 04=0

TS173,

3213	7404	OSR
3214	7006	RTL
3215	7006	RTL
3216	7004	RAL
3217	7710	SPA CLA
3220	5462	JMP I TS177N
3221	6141	LINC
3222	0011	CLR
3223	0004	ESF
3224	0100	SAM0
3225	0002	BOP
3226	0054	DCA
3227	6141	LINC
3230	0101	SAM1
3231	0011	CLR
3232	1020	LDI
3233	0100	ESF
3234	0004	ESF
3235	0002	PDP
3236	6135	CLSA
3237	7300	CLA CLL
3240	1122	TAD K0400
3241	6132	CLLR
3242	6141	LINC
3243	0100	SAM0
3244	0100	SAM0
3245	0002	PDP
3246	0053	DCA
3247	1053	TAD
3250	7041	CIA
3251	1004	TAD
3252	7040	SEA CLA
3253	4430	JMS I
3254	4426	JMS I
3255	7314	TS173M
3256	7402	HLT
3257	7410	SKP
3260	3213	TS173
3261	7340	CLA CLL CMA
3262	3046	DCA REGA

```

/IF FIGHT SM BIT 2(1)
/SKIP FAST SAM TEST?
/RSW 04=1?
/INDIRECT REF TO TS177
/ENTER LINC MODE
/CLEAR AC
/CLEAR SPEC, IN REG.
/READ KNOB ZERO
/BACK TO PHODE
/TO PAGE 0
/BACK TO LMODE
/READ KNOB 1
/CLEAR AC
/PICK UP AC BIT 03
/ENABLE FAST SAM
/ENTER PDP-8 MODE
/CLEAR CLOCK STATUS
/CLEAR AC
/SET MODE BIT0=1
/ENABLE COUNT
/ENTER LINC MODE
/FAST SAM SET THEREFORE READ IN KNOB 1
/SHOULD STILL READ KNOB1
/ENTER PDP-8 MODE
/SAVE VALUE
/RESTORE IT
/2'S COMPLEMENT
/COMPARE IT
/EQUAL?
/CHECK MONITOR
/READING FAST SAM CONVERTED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

/TEST FAST SAMPLE WITH MODE 2=1 (CHECK THAT KNOBS 0 & 1 ARE SET PROPERLY)

```

/SET AC 03,05=1
/MODE 2(1),0(1)
/SET AC=4000
/SET BUFR=4000
/CLEAR AC
/SET AC 04=1
/LOAD CTN FROM BUF
/CLEAR AC
/CLEAR AC
/CLEAR BUF
/CLEAR AC
/CLEAR AC
/CLEAR ALL MODES
/SET AC 03,05=1
/SET OVERFLOW MODE 0(1)
/ENTER LING MODE
/SAMPLE KNOB 0
/ENTER PDP-8 MODE
/STORE
/RESTORE
/218 COMPLEMENT
/ADD FIRST SAMPLE
/EQUAL?
/CHECK MONITOR
/CONVERSION NOT INITIATED BY OVFLOW
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP/ SCOPE LOOP
/SET AC=7777
/REGA FOR NEXT TEST
/DONE?
/BACK

```

```

3263 1123 TAD K0500
3264 6132 CLRL
3265 7330 CLA CLL CHL RAR
3266 6133 CLAB
3267 7200 CLA
3270 1116 TAD K0200
3271 6134 CLEN
3272 7200 CLA
3273 6133 CLAB
3274 7200 CLA
3275 6132 CLRL
3276 1123 TAD K0500
3277 6132 CLRL
3278 6141 LINC
3301 0100 SAM0
3302 0002 PDP
3303 3053 DCA
3304 1053 TAD
3305 7041 CIA
3306 1054 TAD
3307 7050 SNA CLA
3310 4430 JMS I
3311 4426 JMS I
3312 7333 TS174M
3313 7402 HLT
3314 7410 SKP
3315 3263 TS174
3316 7340 CLA CLL CHL
3317 3046 DCA
3320 2047 ISZ
3321 5213 JMP
3322 1151 TAD
3323 3047 DCA

```

/CHECK THAT MODE 0(0),1(1),2(2) DO NOT AFFECT SAMPLE

Address	Instruction	Comment
3324	CLA	
3325	CLR	
3326	TAD	
3327	CLR	
3330	LINC	
3331	CLR	
3332	EST	
3333	SAM0	
3334	PDP	
3335	DCA	
3336	LINC	
3337	SAM1	
3340	LDA1	
3341	EST	
3342	EST	
3343	SAM0	
3344	PDP	
3345	DCA	
3346	TAD	
3347	CIA	
3350	TAD	
3351	SQA CLA	
3352	JMS !	ERROR
3353	JMS !	ERROR
3354	TST75M	
3355	HLT	
3356	SKP	
3357	TST75	
3360	CLA CLP CHA	
3361	REGA	

/NOW CHECK FOR INHIBITING OF FAST SAM

ENTER LINC MODE

READ KNOB 0

ENTER PDP MODE

STORE

RESTORE

2'S COMPLEMENT

COMPARE

EQUAL?

CHECK MONITOR

MODE 2(1),1(1) INHIBIT FAST SAM

MESSAGE POINTER

ERROR HALT

TO NEXT TEST

ISZ LOOP/ SCOPE LOOP

SET AC=7777

RESET REGA FOR NEXT TEST

DONE?

BACK VIA PAGE 0

RESET REGB

3362	6141	TS176, LINC
3363	0100	SAM0
3364	0002	PDP
3365	3053	DCA
3366	1053	TAD
3367	7041	CIA
3370	1054	TAD
3371	7650	SNA CLA
3372	4430	JMS 1
3373	4426	JMS 1
3374	7376	TS176H
3375	7402	HLT
3376	7410	SKP
3377	3362	TS176
3400	7340	CLA CLL CMA
3401	3046	DCA
3402	2047	ISZ
3403	5461	JMP 1
3404	1151	TAD
3405	3047	DCA

PDP
DCA
TAD
RXED
TAD
RXED
CIA
TAD
SEND
SNA CLA
JMS 1
JMS 1
TS176H
HLT
SKP
TS176
CLA CLL CMA
DCA
REGA
REGB
ISZ
JMP 1
TAD
M0040
REGB

/DOES TO PRESET CLEAR OVFL0, ENABLES, RATES AND MODES
/PROGRAMED 10 PRESET USED

3406	7200	CLA	TS177,
3407	6132	CLR	
3410	6134	CLEN	
3411	1133	TAD	K3000
3412	6132	CLR	
3413	7200	CLA	
3414	1142	TAD	K8000
3415	7001	IAC	
3416	7440	SZA	
3417	5215	JMP	=2

/CLEAR AC
 /CLEAR ALL MODES
 /CLEAR ALL ENABLES
 /SET AC 01,0201
 /SET RATE=10KHZ
 /SET AC 00,0101
 /INCREMENT COUNTER
 /DONE?
 /WAIT LOOP 4,92 MSEC

/NOW DO 10 PRESET CHECK IF RATE BITS 1,2 CLEAR

/ENTER LINC MODE
 /PICK UP AC BIT 07

/DO 10 PRESET

/ENTER PDP MODE

/GET COUNTER

/STORE

/SET UP DELAY

/INCREMENT COUNTER

/DONE?

/WAIT LOOP 4,92 MSEC

/READ COUNTER AGAIN

/2'S COMPLEMENT

/COMPARE

/HAS COUNTER CHANGED?

/CHECK MONITOR

/10 PRESET FAILED TO CLEAR RATE BITS 1 & 2

/MESSAGE POINTER

/ERROR HALT

/TO NEXT TEST

/1ST LOOP1 SCOPE LOOP

/SET AC=7777

/PRESET REGA FOR NEXT TEST

/LOOP BACK

/PRESET REG8

LINC
 LDAI
 ESF
 PDP
 CLCA
 DCA
 SEND
 K8000
 TAD
 IAC
 SZA
 JMP
 =2
 CLCA
 CIA
 TAD
 SEND
 SNA CLA
 JMS I
 JMS I
 TS177M
 HLT
 SKP
 TS177
 CLA CLL
 DCA
 REG8
 REG8
 TS177
 TAD
 M0040
 DCA

6141
 3420
 3421
 1020
 3422
 0020
 0004
 3423
 0002
 3424
 0002
 3425
 6137
 3426
 3054
 3427
 1142
 7001
 3430
 7440
 3431
 5230
 3432
 6137
 3433
 7041
 3434
 1054
 3435
 7650
 3436
 4430
 3437
 4426
 3440
 7423
 3441
 7402
 3442
 7410
 3443
 3406
 3444
 3406
 7340
 3445
 3046
 3446
 2047
 3447
 5206
 3450
 1151
 3451
 3047

/NOW ENABLE RATE BIT 0

3453 7200 CLA
3454 6132 CLR
3455 6134 CLN
3456 1335 TAD
3457 6132 CLR
3460 7200 CLA
3461 7001 IAC
3462 7440 SZA
3463 5261 JMP
/NOW DO 10 PRESET AND SEE IF BIT 0 CLEARED

/CLEAR AC
/CLEAR ALL MODES
/CLEAR ENABLES
/SET AC 0001
/SET RATE=1KHZ
/INCREMENT COUNTER
/DONE?
/WAIT LOOP 16 MSEC

/NOW DO 10 PRESET AND SEE IF BIT 0 CLEARED

3464 6141 LINC
3465 1020 LDAI
3466 0020 0020
3467 0004 ESF
3470 0002 PDP
3471 6137 CLCA
3472 3054 DCA
3473 7001 IAC
3474 7440 SZA
3475 5273 JMP
3476 6137 CLCA
3477 7041 CIA
3478 1054 TAD
3479 7650 SNA
3480 4430 JMS I
3481 4426 JMS I
3482 7457 TS179H
3483 7402 HLT
3484 7410 SKP
3485 3453 TS179
3486 7340 CLA
3487 3046 DCA
3488 2047 ISZ
3489 3046 REGA
3490 3043 JMP I
3491 3046 DCA
3492 3046 REGA
3493 3046 DCA
3494 3046 REGA
3495 3046 DCA
3496 3046 REGA
3497 3046 DCA
3498 3046 REGA
3499 3046 DCA
3500 3046 REGA
3501 3046 DCA
3502 3046 REGA
3503 3046 DCA
3504 3046 REGA
3505 3046 DCA
3506 3046 REGA
3507 3046 DCA
3508 3046 REGA
3509 3046 DCA
3510 3046 REGA
3511 3046 DCA
3512 3046 REGA
3513 3046 DCA
3514 3046 REGA

/ENTER LINC MODE
/PICK UP AC 07
/DO 10 PRESET
/ENTER PDP MODE
/READ COUNTER
/STORE
/INCREMENT COUNTER
/DONE?
/WAIT 16 MSEC
/READ COUNTER AGAIN
/2'S COMPLEMENT
/COMPARE
/COUNTER STILL THE SAME
/CHECK MONITOR
/RATE BIT 0 SET AFTER 10 PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA
/LOOP BACK
/BACK VIA PAGE 0
/CLEAR REGA IF EXECUTING NEXT TEST

/DOES OVERFLOW AND OVFL0 INT. FLOP
/CLEAR WITH 10 PRESET

3515	7200	CLA	TS101	/CLEAR AC
3516	6132	CLR		/CLEAR ALL MODES
3517	1114	TAD	K0100	
3520	6132	CLR		/SET MODE 2(1)
3521	6135	CLSA		/CLEAR STATUS
3522	7200	CLA	K4000	
3523	1135	TAD		/SET BUF TO 4000
3524	6133	CLAB		
3525	7200	CLA	K0200	
3526	1116	TAD		/LOAD COUNTER
3527	6134	CLEN		/ZERO BUF
3530	7200	CLA		/CLEAR ALL MODES
3531	6133	CLAB		/GEN "CLR CNT"
3532	6132	CLR	K0100	
3533	1114	TAD		
3534	6132	CLR		
3535	6141	LINC		
3536	1020	LD01		
3537	0020	0020		
3540	0004	EST		
3541	0002	PDP		/SO 10 PRESET
3542	6135	CLSA		/ENTER PDP MODE
3543	7700	SMA CLA		/GET STATUS
3544	4430	JMS 1	ERROR	/CHECK MONITOR
3545	4426	JMS 1	ERROR	/OVFL0 STILL SET AFTER 10 PRESET
3546	7511	TS101M		/MESSAGE POINTER
3547	7402	HLT		/ERROR HALT
3550	7410	SKP		/TO NEXT TEST
3551	3515	TS101		/152 LOOP1 SCOPE LOOP

/TEST OVLO INT ENABLE
/

3552	7200	CLA	TS182,
3553	1114	TAD	K0100
3554	6132	CLR	
3555	6135	CLSA	
3556	7200	CLA	
3557	1135	TAD	K4000
3560	6133	CLAB	
3561	7200	CLA	
3562	1116	TAD	K0200
3563	6134	CLEN	
3564	7200	CLA	
3565	1114	TAD	K0100
3566	6134	CLEN	
3567	6141	LINE	
3570	1020	LDI	
3571	0020	EST	
3572	0004	EST	
3573	0002	PDP	
3574	7200	CLA	
3575	6132	CLR	
3576	1114	TAD	K0100
3577	6132	CLR	
3600	6131	CLSK	
3601	4430	JMS I	ERROR
3602	4426	JMS I	ERROR
3603	7534	TS182M	
3604	7402	HLT	
3605	7610	SKP CLA	
3606	3552	TS182	

/CLEAR AC
/SET MODE 2(1)
/CLEAR STATUS
/SET BUF PRESET REG.
/LOAD CNT WITH 4000
/SET INT
/ENTER LINE MODE
/DO IO PRESET
/ENTER PDP MODE
/CLEAR ALL MODES
/GEN.
/CHECK MONITOR
/OVLO INTER, SET AFTER I/O PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP

DOES TO PRESET CLEAR INPUT ENABLE FLOPS

```

/CLEAR ALL MODES
/ENABLE INPUTS TO ALL CHAN
/ENTER LINC MODE
/DO IO PRESET
/ENTER PDP MODE
/CLEAR STATUS
/SIMULATE INPUTS ON ALL CHAN
/GET STATUS
/IGNORE O/FLO
/CHECK MONITOR
/STATUS NOT ZERO I/O PRESET FAILED
/ERROR HALT
/TO NEXT TEST
/ISE LOOP/ SCOPE LOOP

```

3607	7200	TS103,	CLA
3610	6132	CLLR	
3612	6134	YAD	K0077
3613	6141	LINC	
3614	1020	LDAL	
3615	0020		
3616	0004	ESP	
3617	0002	PDP	
3620	6135	CLSA	
3621	7200	CLA	
3622	1113	YAD	K0077
3623	6132	CLLR	
3624	7200	CLA	
3625	6135	CLSA	
3626	0134	AND	K3777
3627	7050	SNA CLA	
3630	4430	JMS I	ERROR
3631	4426	JMS I	ERROR
3632	4332	TS103M	
3633	7402	HLT	
3634	7610	SMP CLA	
3635	3607	TS103	

/DOES IO PRESET CLEAR MODE 2

3636	CLAB	TS104,	/CLEAR MODES
3637	CLR		
3640	TAD	K0100	
3641	CLR		
3642	LINC		
3643	LDAI		
3644	0020		
3645	0004		
3646	0002		
3647	CLA		
3650	TAD	K5555	
3651	CLAB		
3652	CLA		
3653	TAD	K0200	
3654	CLEN		
3655	CLCA		
3656	SMA CLA		
3657	JMS I		
3660	JMS I	ERROR	
3661	TS104M		
3662	HLT		
3663	SKP CLA		
3664	TS104		
3665	CLA CLL CMA		
3666	DCA	REGA	

/SET MODE 2(1) = CLR CNT
/ENTER LINC MODE
/DO IO PRESET
/ENTER PDP MODE
/LOAD BUF WITH 5555
/GEN LOAD CNT
/LOAD CNT TO AC
/CHECK MONITOR
/MODE 2 NOT CLEARED BY I/O PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISS LOOP1 SCOPE LOOP
/SET AC = 7777
/PRESET REGA

/DOES TO PRESET CLEAR MODE 0

/IF RIGHT SW BIT 4(1)
/SKIP FAST SAM TEST

/CLEAR ALL MODES
/ENTER LINC MODE
/READ KNOB 0

/READ KNOB 1
/ENTER POP MODE

/SET MODE 0(1)
/ENTER LINC MODE

/DO TO PRESET

/ENABLE FAST SAM

/READ KNOB 1-FAST S, MODE
/ENTER POP MODE

/CHECK MONITOR
/FAST SAM NOT SET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TAPE
/ISE LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA

3667	7604	LAS	TS185,
3670	7006	RTL	
3671	7006	RTL	
3672	7710	SPA CLA	
3673	5354	JMP	RESET
3674	7200	CLA	
3675	6132	CLR	
3676	6141	LINC	
3677	0100	SAM0	
3700	0002	POP	
3701	3054	OCA	SEND
3702	6141	LINC	
3703	0101	SAM1	
3704	0002	POP	
3705	7200	CLA	
3706	1122	TAD	K0400
3707	6132	CLR	
3710	6141	LINC	
3711	1020	LDAI	
3712	0020	0020	
3713	0004	ESF	
3714	1020	LDAI	
3715	0100	0100	
3716	0004	ESF	
3717	0100	SAM0	
3720	0002	POP	
3721	7041	CIA	
3722	1054	TAD	SEND
3723	7640	SZA CLA	
3724	4430	JMS 1	NEOROR
3725	4426	JMS 1	ERROR
3726	4403	TS185M	
3727	7402	HLT	
3730	7410	SKP	
3731	3667	TS185	
3732	7340	CLA CL	CMA
3733	3046	OCA	REGA

/NOW CHECK FOR MODE 0 CLEARED

/RESET ANYTHING LEFT HANGING

3734	6141	TS186, LINC
3735	0100	SAM0
3736	0002	POP
3737	7041	CIA
3740	1054	TAD
3741	7650	SNA CLA
3742	4430	JMS I
3743	4426	JMS I
3744	4430	TS186H
3745	7402	HLT
3746	7410	SKP
3747	3734	TS186
3750	7340	CLA CLL CMA
3751	3046	DCA
3752	2047	ISZ
3753	5267	JMP
		TS185
3754	1107	TAD
3755	6141	LINC
3756	0004	ESF
3757	0002	POP
3760	7200	CLA
3761	1151	TAD
3762	3046	DCA
		REGA
		MO040
		K0020

RESET,

/ENTER LINC MODE
/READ KNOB 0
/ENTER POP MODE
/CHECK MONITOR
/MODE 0 NOT CLEARED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC = 7777
/RESET REGA
/LOOP BACK
/PICK UP AC BIT 07
/TO LMODE
/DO TO PRESET
/TO PMODE
/CLEAR THE AC
/PRESET REGA PRIOR TO NEXT TEST

1/DOES MODE 1(1) WORK CHAN 1

ADDRESS	DATA	OPERATION	ADDRESS	DATA	OPERATION
3763	7200	CLA	0000	0000	CLR ALL MODES
3764	6132	CLR	0001	0000	CLR BUF
3765	6133	CLA	0002	0000	GET RANDOM NUM
3766	4445	JMS I	0003	0000	SEND
3767	3054	DCA	0004	0000	SEND
3770	1054	TAD	0005	0000	SEND
3771	6133	CLAB	0006	0000	SEND
3772	7200	CLA	0007	0000	SEND
3773	1114	TAD	0008	0000	SEND
3774	6132	CLR	0009	0000	SEND
3775	6133	CLSA	0010	0000	SEND
3776	7200	CLA	0011	0000	SEND
3777	1116	TAD	0012	0000	SEND
4000	6134	CLEN	0013	0000	SEND
4001	6132	CLR	0014	0000	SEND
4002	7200	CLA	0015	0000	SEND
4003	6133	CLAB	0016	0000	SEND
4004	1112	TAD	0017	0000	SEND
4005	6134	CLEN	0018	0000	SEND
4006	2047	ISZ	0019	0000	SEND
4007	741E	SKP	0020	0000	SEND
4010	5213	JMP	0021	0000	SEND
4011	6131	CLSK	0022	0000	SEND
4012	5206	JMP	0023	0000	SEND
4013	6135	CLSA	0024	0000	SEND
4014	7200	CLA	0025	0000	SEND
4015	3047	DCA	0026	0000	SEND
4016	6136	CLBA	0027	0000	SEND
4017	7041	CIA	0028	0000	SEND
4020	1054	TAD	0029	0000	SEND
4021	7650	SNA CLA	0030	0000	SEND
4022	4430	JMS I	0031	0000	SEND
4023	4426	JMS I	0032	0000	SEND
4024	4450	TST07H	0033	0000	SEND
4025	7402	HLT	0034	0000	SEND
4026	7410	SKP	0035	0000	SEND
4027	3763	TST07	0036	0000	SEND
4030	1151	TAD	0037	0000	SEND
3043	3047	REGA	0038	0000	SEND

```

/CHECK MONITOR
/CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF - TRANSFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP1 SCOPE LOOP

```

/DOES MODE 1 (1) WORK CHAN 2

4032	CLEN	TS188,	4032	6135
4033	CLSA		4033	6135
4034	CLA		4034	7288
4035	CLAB		4035	6135
4036	TAD	K0814	4036	1104
4037	CLEN		4037	6134
4040	ISE	REG8	4040	2047
4041	SKP		4041	7410
4042	JMP	'03	4042	5245
4043	CLSK		4043	6131
4044	JMP	'04	4044	5248
4045	CLSA		4045	6135
4046	CLA		4046	7288
4047	DCA	REG8	4047	3047
4050	CLBA		4050	6136
4051	CIA		4051	7041
4052	TAD	SEND	4052	1054
4053	SNA CLA		4053	7650
4054	JMS 1	ERROR	4054	4430
4055	JMS 1	ERROR	4055	4426
4056	TS188M		4056	4476
4057	HLT		4057	7402
4060	SKP	TS188	4060	7410
4061	TS188		4061	4032
4062	TAD	M0848	4062	1151
4063	DCA		4063	3046

```

/CLEAR ENABLES
/CLEAR CLOCK STATUS
/CLEAR BUFFER
/ENABLE CHAN 2 INPUT AND INT
/INCREMENT TIMER
/NOT DONE YET
/TIME OUT
/SKP ON CLOCK INT
/CLEAR STATUS
/CLEAR REG8
/GET BUFFER
/COMPARE
/CHECK MONITOR
/CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP1 SCOPE LOOP

```

3 2000 1 (1) WORK CHAN 3

```

/CLEAR ENABLE
/CLEAR STATUS
/CLEAR BUFFER
/ENABLES CHAN 3 INPUT AND INT
/INCRÉMENT TIMER
/NOT DONE YET
/TIME OUT
/SKIP ON CK INT
/CLEAR CLOCK STATUS
/CLEAR REGG
/GET BUF
/COMPARE
/CHECK MONITOR
/CHAN 3 INPUT FAILED TO CAUSE
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/SET LOOP SCOPE LOOP
/SET ADDR777
/PRESET REGA
/PRESET REGG

```

ADDRESS	DATA	OPERATION	STATUS
4264	6134	CLEN	TST89
4265	6135	CLSA	
4266	7200	CLA	
4267	6133	CLAB	
4270	1077	TAD	K2003
4271	6134	CLEN	
4272	2047	ISZ	REG8
4273	7410	SKP	
4274	5277	JMP	03
4275	6131	CLSK	
4276	5272	JMP	04
4277	6135	CLSA	
4280	7200	CLA	REG8
4281	3047	DCA	
4282	6136	CLBA	
4283	7041	CIA	
4284	1054	TAD	SEND
4285	7650	SNA CLA	
4286	4430	JMS I	ERROR
4287	4426	JMS I	ERROR
4288	1524	TST89H	
4289	7410	HLT	
4290	7410	SKP	
4291	4064	TST89	
4292	7340	CLA CL	CMA
4293	3046	DCA	REGA
4294	1151	TAD	M0040
4295	3047	DCA	REG8

/TEST MODE 1(1) AND MODE 2(1) CHAN 1

4120	6134	TEST90, CLCN	/CLEAR ENABLES	
4121	1120	TAD		
4122	1127	TAD		
4123	6132	CLLR		
4124	7200	CLA		
4125	1120	TAD		
4126	6132	CLLR		
4127	6137	CLCA		
4130	3054	DCA		
4131	6135	CLSA		
4132	7200	CLA		
4133	6133	CLAB		
4134	1112	TAD		
4135	6134	CLCN		
4136	2051	ISZ		
4137	7410	SKP		
4140	5343	JMP		
4141	6131	CLSK		
4142	5336	JMP		
4143	6135	CLSA		
4144	7200	CLA		
4145	3051	DCA		
4146	6136	CLBA		
4147	7041	CIA		
4150	1054	TAD		
4151	7650	SNA CLA		
4152	4430	JMS I		
4153	4426	JMS I		
4154	4552	TS190M		
4155	7402	HLT		
4156	7410	SKP		
4157	4120	TS190		
4160	7340	CLA CLL CMA		
4161	3046	DCA		

/START CNT RATE=400KHZ = MODE 1(1) AND 2(1)

/STOP CNT = MODE 1(1) AND 2(1)

/GET CNT

/STORE

/CLEAR BUF

/ENABLE CHAN1 INPUT AND INP

/INCREMENT TIMER

/NOT DONE YET

/TIME OUT

/SKP ON CLOCK INT

/CLEAR CLOCK STATUS

/CLEAR TIMER

/GET BUF

/COMPARE

/CHECK MONITOR

/CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER

/MESSAGE POINTER

/ERROR HALT

/TO NEXT TEST

/ISZ LOOP1 SCOPE LOOP

/TEST MODE 1 (1) AND MODE 2 (1) CHAN 2

4162	CLEN	TS191,	/CLEARS ENABLES
4163	CLSA		/CLEAR STATUS
4164	CLA		/CLEAR BUF
4165	CLAB		/ENABLE CHAN 2 INPUT AND INT
4166	TAD	K0014	/INCREMENT TIMER
4170	CLEN		/NOT DONE YET
4171	ISZ	REGT	/TIME OUT
4172	SKP		/SKIP ON CLOCK INT
4173	JMP		/CLEAR STATUS
4174	CLSK		/CLEAR REGT
4175	JMP		/GET BUF
4176	CLSA		/COMPARE
4177	CLAB		/CHECK MONITOR
4178	CLA		/CHAN 2 INPUT FAILED TO CAUSE GNT TO BUF TRANSFER
4179	CLSA		
4180	CLAB		
4181	CLA		
4182	CLSA		
4183	CLAB		
4184	CLA		
4185	CLSA		
4186	CLAB		
4187	CLA		
4188	CLSA		
4189	CLAB		
4190	CLA		
4191	CLSA		
4192	CLAB		
4193	CLA		
4194	CLSA		
4195	CLAB		
4196	CLA		
4197	CLSA		
4198	CLAB		
4199	CLA		
4200	CLSA		
4201	CLAB		
4202	CLA		
4203	CLSA		
4204	CLAB		
4205	CLA		
4206	CLSA		
4207	CLAB		
4208	CLA		
4209	CLSA		
4210	CLAB		
4211	CLA		
4212	CLSA		
4213	CLAB		
4214	CLA		
4215	CLSA		
4216	CLAB		
4217	CLA		
4218	CLSA		
4219	CLAB		
4220	CLA		
4221	CLSA		
4222	CLAB		
4223	CLA		
4224	CLSA		
4225	CLAB		
4226	CLA		
4227	CLSA		
4228	CLAB		
4229	CLA		
4230	CLSA		
4231	CLAB		
4232	CLA		
4233	CLSA		
4234	CLAB		
4235	CLA		
4236	CLSA		
4237	CLAB		
4238	CLA		
4239	CLSA		
4240	CLAB		
4241	CLA		
4242	CLSA		
4243	CLAB		
4244	CLA		
4245	CLSA		
4246	CLAB		
4247	CLA		
4248	CLSA		
4249	CLAB		
4250	CLA		
4251	CLSA		
4252	CLAB		
4253	CLA		
4254	CLSA		
4255	CLAB		
4256	CLA		
4257	CLSA		
4258	CLAB		
4259	CLA		
4260	CLSA		
4261	CLAB		
4262	CLA		
4263	CLSA		
4264	CLAB		
4265	CLA		
4266	CLSA		
4267	CLAB		
4268	CLA		
4269	CLSA		
4270	CLAB		
4271	CLA		
4272	CLSA		
4273	CLAB		
4274	CLA		
4275	CLSA		
4276	CLAB		
4277	CLA		
4278	CLSA		
4279	CLAB		
4280	CLA		
4281	CLSA		
4282	CLAB		
4283	CLA		
4284	CLSA		
4285	CLAB		
4286	CLA		
4287	CLSA		
4288	CLAB		
4289	CLA		
4290	CLSA		
4291	CLAB		
4292	CLA		
4293	CLSA		
4294	CLAB		
4295	CLA		
4296	CLSA		
4297	CLAB		
4298	CLA		
4299	CLSA		
4300	CLAB		
4301	CLA		
4302	CLSA		
4303	CLAB		
4304	CLA		
4305	CLSA		
4306	CLAB		
4307	CLA		
4308	CLSA		
4309	CLAB		
4310	CLA		
4311	CLSA		
4312	CLAB		
4313	CLA		
4314	CLSA		
4315	CLAB		
4316	CLA		
4317	CLSA		
4318	CLAB		
4319	CLA		
4320	CLSA		
4321	CLAB		
4322	CLA		
4323	CLSA		
4324	CLAB		
4325	CLA		
4326	CLSA		
4327	CLAB		
4328	CLA		
4329	CLSA		
4330	CLAB		
4331	CLA		
4332	CLSA		
4333	CLAB		
4334	CLA		
4335	CLSA		
4336	CLAB		
4337	CLA		
4338	CLSA		
4339	CLAB		
4340	CLA		
4341	CLSA		
4342	CLAB		
4343	CLA		
4344	CLSA		
4345	CLAB		
4346	CLA		
4347	CLSA		
4348	CLAB		
4349	CLA		
4350	CLSA		
4351	CLAB		
4352	CLA		
4353	CLSA		
4354	CLAB		
4355	CLA		
4356	CLSA		
4357	CLAB		
4358	CLA		
4359	CLSA		
4360	CLAB		
4361	CLA		
4362	CLSA		
4363	CLAB		
4364	CLA		
4365	CLSA		
4366	CLAB		
4367	CLA		
4368	CLSA		
4369	CLAB		
4370	CLA		
4371	CLSA		
4372	CLAB		
4373	CLA		
4374	CLSA		
4375	CLAB		
4376	CLA		
4377	CLSA		
4378	CLAB		
4379	CLA		
4380	CLSA		
4381	CLAB		
4382	CLA		
4383	CLSA		
4384	CLAB		
4385	CLA		
4386	CLSA		
4387	CLAB		
4388	CLA		
4389	CLSA		
4390	CLAB		
4391	CLA		
4392	CLSA		
4393	CLAB		
4394	CLA		
4395	CLSA		
4396	CLAB		
4397	CLA		
4398	CLSA		
4399	CLAB		
4400	CLA		
4401	CLSA		
4402	CLAB		
4403	CLA		
4404	CLSA		
4405	CLAB		
4406	CLA		
4407	CLSA		
4408	CLAB		
4409	CLA		
4410	CLSA		
4411	CLAB		
4412	CLA		
4413	CLSA		
4414	CLAB		
4415	CLA		
4416	CLSA		
4417	CLAB		
4418	CLA		
4419	CLSA		
4420	CLAB		
4421	CLA		
4422	CLSA		
4423	CLAB		
4424	CLA		
4425	CLSA		
4426	CLAB		
4427	CLA		
4428	CLSA		
4429	CLAB		
4430	CLA		
4431	CLSA		
4432	CLAB		
4433	CLA		
4434	CLSA		
4435	CLAB		
4436	CLA		
4437	CLSA		
4438	CLAB		
4439	CLA		
4440	CLSA		
4441	CLAB		
4442	CLA		
4443	CLSA		
4444	CLAB		
4445	CLA		
4446	CLSA		
4447	CLAB		
4448	CLA		
4449	CLSA		
4450	CLAB		
4451	CLA		
4452	CLSA		
4453	CLAB		
4454	CLA		
4455	CLSA		
4456	CLAB		
4457	CLA		
4458	CLSA		
4459	CLAB		
4460	CLA		
4461	CLSA		
4462	CLAB		
4463	CLA		
4464	CLSA		
4465	CLAB		
4466	CLA		
4467	CLSA		
4468	CLAB		
4469	CLA		
4470	CLSA		
4471	CLAB		
4472	CLA		
4473	CLSA		
4474	CLAB		
4475	CLA		
4476	CLSA		
4477	CLAB		
4478	CLA		
4479	CLSA		
4480	CLAB		
4481	CLA		
4482	CLSA		
4483	CLAB		
4484	CLA		
4485	CLSA		
4486	CLAB		
4487	CLA		
4488	CLSA		
4489	CLAB		
4490	CLA		
4491	CLSA		
4492	CLAB		
4493	CLA		
4494	CLSA		
4495	CLAB		
4496	CLA		
4497	CLSA		
4498	CLAB		
4499	CLA		
4500	CLSA		
4501	CLAB		
4502	CLA		
4503	CLSA		
4504	CLAB		
4505	CLA		
4506	CLSA		
4507	CLAB		
4508	CLA		
4509	CLSA		
4510	CLAB		
4511	CLA		
4512	CLSA		
4513	CLAB		
4514	CLA		

/TEST MODE 1 (1) AND MODE 2 (1) CHAN 3

4215	CLEN	TS192,	/CLEAR ENABLES
4216	CLSA		
4217	CLA		
4220	CLAB		/CLEAR BUF
4221	TAD		
4222	CLEN		/ENABLES CHAN3 INPUT AND INT
4223	ISZ		/INCREMENT TIMER
4224	SKP		/NOT DONE YET
4225	JMP	.43	/TIME OUT
4226	CLSK		/SKP ON CLOCK INT
4227	JMP	.44	
4230	CLSA		/CLEAR CLOCK STATUS
4231	CLA		/CLEAR REGT
4232	DCA		
4233	NOP		
4234	CLBA		/GET BUF
4235	CIA		/COMPARE
4236	TAD		
4237	SNA CLA		
4240	JMS I	ERROR	
4241	JMS I	ERROR	
4242	TS192M		
4243	HLT		
4244	SKP		
4245	TS192		
4246	CLA CL	CH4	
4247	DCA		/PRESSET REGA

/CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
 /MESSAGE POINTER
 /ERROR HALT
 /TO NEXT TEST
 /ISZ LOOP/ SCOPE LOOP
 /SET AC = 7777
 /PRESSET REGA

/CHECK THAT CHAN 3 CLEARED COUNTER FROM TEST 92

/GET CNT

/ZERO?
/CHECK MONITOR
/CHAN3 INPUT FAILED TO CLEAR CNT
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP/ SCOPE LOOP
/SET AC = 777
/PRESET REGA
/DO TESTS 90-93 40 TIMES
/TO TEST 90
/PRESET REGA

4250 6137 CLCA
4251 3053 DCA
4252 1053 TAD
4253 7650 SNA CLA
4254 4430 JMS I
4255 4426 JMS I
4256 4654 TS193M
4257 7402 HLT
4260 7410 SKP
4261 4250 TS193
4262 7340 CLA CLC
4263 3046 DCA
4264 2047 ISE
4265 5464 JMP I
4266 1151 TAD
4267 3046 REGA
4270 1071 TAD
4271 6133 CLA8
4272 7200 CLA
4273 1073 TAD
4274 6132 CLR
4275 7200 CLA
4276 1072 TAD
4277 6134 CLEN
4300 6131 CLSK
4301 5300 JMP
4302 2051 ISE
4303 5302 JMP
4304 7200 CLA
4310 6137 CLCA
4311 7440 SZA
4312 7710 SPA CLA
4313 4430 JMS I
4314 4426 JMS I
4315 4702 TS194M
4316 7402 HLT
4317 7410 SKP
4320 4270 TS194

/CHECK THAT DIFLO ALWAYS TRANSFERS BUFFER TO COUNTER ON MODE 2(1)

/GET PRESET

/PRESET BUFFER

/GET RATE

/START CLOCK

/GET ENABLES

/INTERRUPT ON OVERFLOW

/WAIT FOR INTERRUPT

/WAIT FOR ANOTHER OVERFLOW

/22 MSEC DELAY

/GET THE COUNTER

/0 IS OK

/COUNTER SHOULD NEVER GO POSITIVE

/ECO EM12-00033 IS EITHER NOT INSTALLED OR NOT WORKING

4270 1071 TAD
4271 6133 CLA8
4272 7200 CLA
4273 1073 TAD
4274 6132 CLR
4275 7200 CLA
4276 1072 TAD
4277 6134 CLEN
4300 6131 CLSK
4301 5300 JMP
4302 2051 ISE
4303 5302 JMP
4304 7200 CLA
4310 6137 CLCA
4311 7440 SZA
4312 7710 SPA CLA
4313 4430 JMS I
4314 4426 JMS I
4315 4702 TS194M
4316 7402 HLT
4317 7410 SKP
4320 4270 TS194

/ALERT OPERATOR OF PASS COMPLETION
/SUPPRESS PRINTOUT IF RSW 06 = 1

4321	2032	ISZ	PASS	/INCREMENT PASS
4322	7000	NOP		/DON'T SKIP
4323	7004	LAS		/READ SWITCHES
4324	0111	AND	K0040	/PICK OUT RSW 06
4325	7040	SEA CLA		/SET?
4326	5176	JMP	176	/YES, NO PRINTOUT
4327	1044	TAD	PNTJ	/GET POINTER
4330	3426	DCA I	ERNOR	/CHEAT MONITOR
4331	5431	JMP I	OUTPAS	/GO TYPE ALARM
4332	4741	LOCJ,	TS195H	/MESSAGE POINTER

/RETURN TO LOC 176 FROM ASCII TYPEOUT (MONITOR WILL HANDLE LINK)

5000
*5000
/NON ERROR MONITOR DETERMINES IF OPERATOR WANTS TO LOOP ON NONFAILING TEST
/RETURN ADDRESS
/SET AC = 4
/GET RETURN ADDRESS
/UPDATE RETURN ADDRESS
/GET SCOPE LOOP ADDRESS
/STORE IT
/UPDATE DATA
/EXIT
/READ SWITCHES
/SAVE SR3
/TEST AND CLEAR
/LOOPING
/GET AC=1
/ADD NERORS
/STORE IN NERORS
/JUMP INDIRECT LOOP

5000	0000	CLA CLC IAC RTL	NERORS, 0
5001	7307	TAD	NERORS
5002	1200	TAD	NERORS
5003	3200	DCA	NERORS
5004	1600	TAD I	NERORS
5005	3220	DCA	NERORS
5006	2046	ISZ	REGA
5007	5620	JMP I	NERORS
5010	7604	LAS	K0400
5011	0122	AND	
5012	7640	SEA CLA	
5013	5620	JMP I	NERORS
5014	7040	CMA	
5015	1200	TAD	NERORS
5016	3200	DCA	NERORS
5017	5600	JMP I	NERORS
5020	0000	ERRORS, 0	
5021	7604	LAS	
5022	7004	RAL	
5023	7000	SMA CLA	
5024	5251	JMP	ASCII
5025	4421	JMS I	BELL
5026	1220	TAD	ERRORS
5027	7041	CIA	
5030	3027	DCA	LASTER
5031	2220	ISZ	ERRORS
5032	7604	LAS	
5033	7700	SMA CLA	
5034	7402	HLT	
5035	2220	ISZ	ERRORS
5036	2220	ISZ	ERRORS
5037	1620	TAD I	ERRORS
5040	3200	DCA	NERORS
5041	7604	LAS	
5042	7006	RTL	
5043	7710	SPA CLA	
5044	5600	JMP I	NERORS
5045	7040	CMA	
5046	1220	TAD	ERRORS
5047	3220	DCA	ERRORS
5050	5620	JMP I	ERRORS

/ERROR PROCESSOR, SCOPE LOOP, HALT, PRINT
/RETURN ADDRESS STORAGE
/READ SWITCHES
/MOVE SR1 INTO AC00
/IS IT SET
/NO TYPE A MESSAGE
/RING THE BELL
/GET CURRENT ERROR ADDRESS
/INVERT IT
/STORE IN LAST ERROR
/YES INDEX ESCAPE
/READ SWITCHES
/IS SR0 SET
/NO, ERROR HALT
/YES INDEX ESCAPE TO JUMP OUT
/INDEX ERRORS TO SCOPE MODE
/GET SCOPE ADDRESS
/STORE IN TYPE
/READ SWITCHES
/MOVE SR02 TO AC0
/IS SCOPE MODE SELECTED
/YES CONTINUE IN SCOPE LOOP
/NO SET AC07777 (-1)
/SUBTRACT ONE FROM ERRORS
/STORE SELECTED ADDRESS
/EXIT TO NEXT TEST

5051	7240	ASCII, CLA CMA	/SET 5(AC)=1
5052	1620	TAD I	/GET MESSAGE ADDRESS STORAGE
5053	3010	DCA	/STORE IT IN AUTO INDEX REGISTER
5054	1220	TAD	/GET RETURN ADDRESS
5055	1027	TAD	/SUBTRACT LAST ERROR ADDRESS
5056	7650	SNA CLA	/TEST
5057	5363	JMP	/SAME GO TYPE DATA
5060	1410	TAD I	/GET FIRST CHARACTER
5061	3200	DCA	/SAVE IT
5062	1200	TAD	/GET IT
5063	7450	SNA	/TEST IT
5064	5226	JMP	/NUMBEREXIT,
5065	7040	CHA	/INVERT IT
5066	7450	SNA	/NUMBEREXITA
5067	5315	JMP	/TYPE OUT DATA ROUTINE
5070	7040	CMA	/CHANGE IT BACK
5071	7112	RTR CL	/SWAP AC TO THE RIGHT
5072	7012	RTR	/MOVE
5073	7012	RTR	/MOVE
5074	4300	JMS	/TYPE IT
5075	1200	TAD	/GET IT AGAIN
5076	4300	JMS	/TYPE IT
5077	5260	JMP	/MUST BE MORE WORDS THAT NEED TYPING
5101	0113	AND	/SAVE SIGNIFICANT PART
5102	3056	DCA	/STORE WORD
5103	1056	TAD	/FETCH IT
5104	7650	SNA CLA	/TEST FOR 00 CRLF CODE
5105	4354	JMS	/YES IT WAS
5106	1056	TAD	/NO TYPE IT
5107	1151	TAD	/SUBTRACT 40
5110	7510	SPA	/TEST POLARITY
5111	1114	TAD	/ADD 340
5112	1117	TAD	/ADD 340
5113	4465	JMS I	/TYPE
5114	5700	JMP I	/EXIT

/GET ADDRESS OF REGISTER

/STORE IN TEMP

/GET TEMP

/TEST FOR EXIT

/EQUALS 0000 EXIT

/GET TEMP

/SS?

/TEST

/SPECIAL RESTART

/GET DATA

/TYPE IT

/SPACE

/TYPE IT

/RETURN ADDRESS STORAGE

/STORE DATA TO BE PRINTED

/SET UP TALLY

/SET IT

/GET FLAG NUMBER

/STORE

DATUM, TAD I

DCA NERROS

TAD NERROS

SNA CLA

JMP 176

TAD NERROS

TAD M4444

JMP 176

TAD NERROS

TAD 1200

JMP 5226

SNA CLA

TAD 7650

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

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TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

/GET A TERM OFF OF TYPE LIST

/EXIT

/SET TO RUBOUT

/TYPE IT

/GET LF

/TYPE IT

/END OF LIST?

/YES EXIT

/INVERT

/BEGINNING OF DATA

/NO

/YES OK RETURN THE TTY CARRIAGE AND LINE FEED

/CLEAR AC AND LINK

/GO TYPE THE DATA

DATUM, TAD I

DCA NERROS

TAD NERROS

SNA CLA

JMP 176

TAD NERROS

TAD M4444

JMP 176

TAD NERROS

TAD 1200

JMP 5226

SNA CLA

TAD 7650

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

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TAD 1200

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TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

TAD 1200

DCA 3200

/RING THE BELL

/RANDOM NUMBER GENERATOR

/CLEAR FLAG

/RESET PASS COUNTER

5200	5200	BELLS,	0	LAS	K0100	AND	0114	5202	0114	5203	7040	5204	5000	JMP	I	BELLS	K0007	JMS	I	TYPE	JMP	I	BELLS	0	0000	RANDY,	0	0000	5210	5210	0000	5211	1241	TAD	RNA	5212	1241	TAD	RNB	5213	1242	TAD	RNC	5214	1140	TAD	K5252	5215	3240	DCA	RNA	5216	7004	RAL	TAD	RNA	5217	1240	TAD	RNA	5220	1241	TAD	RNB	5221	1242	TAD	RNC	5222	1140	TAD	K5252	5223	3241	DCA	RNB	5224	7004	RAL	TAD	RNA	5225	1240	TAD	RNA	5226	1241	TAD	RNB	5227	1242	TAD	RNC	5230	1140	TAD	K5252	5231	3242	DCA	RNC	5232	7004	RAL	TAD	RNA	5233	1240	TAD	RNA	5234	3240	DCA	RNA	5235	1241	TAD	RNB	5236	1242	TAD	RNC	5237	5010	JMP	I	RANDY	5240	7601	RNA,	5241	3542	RNB,	5242	3755	RNC,	5243	0000	TYPOUT,	0	TL5	5244	6046	TL5	5245	6041	TSF	5246	5245	JMP	,-1	5247	6042	TCF	5250	7500	CLA	CLL	JMP	I	TYPOUT	5251	5043	0	5252	0000	SETN,	0	CLA	CLL	5253	7500	CLA	CLL	5254	3032	DCA	PASS	5255	3046	DCA	REGA	5256	3047	DCA	REGB	5257	3027	DCA	LSTCRM	5260	5052	JMP	I	SETN
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/TEXT TEST ERROR MESSAGES

/TS110 CLAB CHANGED AC

TS110M, 0024

5261 0024
5262 2324
5263 6160
5264 4003
5265 1401
5266 0240
5267 0310
5270 0116
5271 0705
5272 0440
5273 0103
5274 4000
5275 7777
5276 0046
5277 0053
5300 0000
EX17A
REGA
RXED
EX17

/TS113 CLBA FAILED

TS113M, 0024

5301 0024
5302 2324
5303 6161
5304 4003
5305 1402
5306 0140
5307 0601
5310 1114
5311 0504
5312 4000
5313 7777
5314 0054
5315 0053
5316 0000
EX17A
SEND
RXED
EX17

/TS112 CLAB FAILED

TS112M, 0024

5317 0024
5320 2324
5321 6162
5322 4003
5323 1401
5324 0240
5325 0601
5326 1114
5327 0504
5330 4000
5331 7777
5332 0054
5333 0053
5334 0000
EX17
RXED
SEND
EX17A

/TS115 CLAB FAILED

TS115M, 0024

5335 0024
5336 2324
5337 6163
5340 4003
5341 1401

5342	0240	5342	0240
5343	0601	5343	1114
5344	1114	5344	0504
5345	0504	5346	4000
5346	4000	5347	7777
5347	7777	5348	0046
5348	0046	5349	0053
5349	0053	5350	0053
5350	0053	5351	0000
5352	0024	5353	0024
5354	2324	5354	2324
5355	6164	5355	6164
5356	4003	5356	4003
5357	1401	5357	1401
5360	0240	5360	0240
5361	0601	5361	1114
5362	1114	5363	0504
5364	4000	5364	4000
5365	7777	5366	0054
5367	0053	5370	0000
5371	0024	5371	0024
5372	2324	5372	2324
5373	6165	5373	6165
5374	4003	5375	1402
5376	0140	5377	0310
5377	0310	5400	0116
5401	0705	5402	0440
5403	0225	5404	0606
5405	0522	5406	4000
5407	7777	5410	0054
5411	0053	5412	0000
5413	0024	5413	0024
5414	2324	5414	2324
5415	6166	5416	4003
5417	1401	5420	0274
5421	7603	5422	1302
5423	0140	5424	0601
5425	1114	5426	1114

TS114M,
EX17A
REGA
RXED
EX17

/TS114 CLAB FAILED

TS115M,
EX17A
SEND
RXED
EX17

/TS115 CLBA CHANGED BUFFER

EX17A
SEND
RXED
EX17

/TS116 CLAB <> CLBA FAILED

TS116M,
0024
2324
6166
4003
1401
0274
7603
1402
0140
0601
1114

5426	0504	5426	0504
5427	4000	5427	4000
5430	7777	5430	7777
5431	0046	5431	0046
5432	0053	5432	0053
5433	0000	5433	0000
5434	0024	5434	0024
TST17M, 0024			
5435	2324	5435	2324
5436	6167	5436	6167
5437	4003	5437	4003
5440	1401	5440	1401
5441	0274	5441	0274
5442	7603	5442	7603
5443	1402	5443	1402
5444	0140	5444	0140
5445	0601	5445	0601
5446	1114	5446	1114
5447	0504	5447	0504
5450	4000	5450	4000
5451	7777	5451	7777
5452	0054	5452	0054
5453	0053	5453	0053
5454	0000	5454	0000
TST16M, 0024			
5455	0024	5455	0024
5456	6170	5456	6170
5460	4003	5460	4003
5461	1401	5461	1401
5462	0274	5462	0274
5463	7603	5463	7603
5464	1402	5464	1402
5465	0140	5465	0140
5466	0601	5466	0601
5467	1114	5467	1114
5470	0504	5470	0504
5471	4000	5471	4000
5472	7777	5472	7777
5473	0054	5473	0054
5474	0053	5474	0053
5475	0000	5475	0000
TST19M, 0024			
5476	0024	5476	0024
5477	2324	5477	2324
5500	6171	5500	6171
5501	4003	5501	4003
5502	1405	5502	1405
5503	1640	5503	1640
5504	0310	5504	0310
5505	0116	5505	0116
5506	0705	5506	0705
5507	0440	5507	0440
5510	0103	5510	0103
5511	4000	5511	4000

/TST18 CLAB <> CLBA FAILED

/TST19 CLEN CHANGED AC

/TS120 CLEN CHANGED BUFFER

5512 7777
5513 0046
5514 0053
5515 0000
EXIT
RXED
REGA
EX17

TS120M, 0024

5516 0024
5517 2324
5520 6260
5521 4003
5522 1405
5523 1640
5524 0310
5525 0116
5526 0705
5527 2440
5530 0225
5531 0606
5532 0522
5533 4000
5534 7777
5535 0046
5536 0053
5537 0000
EXIT
RXED
REGA
EX17A

TS121M, 0024

5540 0024
5541 2324
5542 6261
5543 4003
5544 1403
5545 0140
5546 0601
5547 1114
5550 0504
5551 4000
5552 7777
5553 0054
5554 0053
5555 0000
EXIT
RXED
SEND
EX17A

TS122M, 0024

5556 0024
5557 2324
5560 6262
5561 4042
5562 0314
5563 2240
5564 0316
5565 2442
5566 4006
5567 0111
5570 1405
5571 0400
5572 7777
5573 0054
5574 0053
5575 0000
EXIT
RXED
SEND
EX17A

/TS121 CLCA FAILED

/TS122 "CLR CNT" FAILED

03714 N370 22151/

5613	0000	EX17
5612	0053	RXED
5611	0046	REGA
5610	7177	EX17A
5607	4000	
5606	0504	
5605	1114	
5604	0601	
5603	1640	
5602	1405	
5601	4003	
5600	6263	
5577	2324	

75724 CLEN FAILED

TS124M ₁	TS124M ₂	TS124M ₃	TS124M ₄	TS124M ₅	TS124M ₆	TS124M ₇	TS124M ₈	TS124M ₉	TS124M ₁₀	TS124M ₁₁	TS124M ₁₂	TS124M ₁₃	TS124M ₁₄	TS124M ₁₅	TS124M ₁₆	TS124M ₁₇	TS124M ₁₈	TS124M ₁₉	TS124M ₂₀	TS124M ₂₁	TS124M ₂₂	TS124M ₂₃	TS124M ₂₄	TS124M ₂₅	TS124M ₂₆	TS124M ₂₇	TS124M ₂₈	TS124M ₂₉	TS124M ₃₀	TS124M ₃₁	TS124M ₃₂	TS124M ₃₃	TS124M ₃₄	TS124M ₃₅	TS124M ₃₆	TS124M ₃₇	TS124M ₃₈	TS124M ₃₉	TS124M ₄₀	TS124M ₄₁	TS124M ₄₂	TS124M ₄₃	TS124M ₄₄	TS124M ₄₅	TS124M ₄₆	TS124M ₄₇	TS124M ₄₈	TS124M ₄₉	TS124M ₅₀	TS124M ₅₁	TS124M ₅₂	TS124M ₅₃	TS124M ₅₄	TS124M ₅₅	TS124M ₅₆	TS124M ₅₇	TS124M ₅₈	TS124M ₅₉	TS124M ₆₀	TS124M ₆₁	TS124M ₆₂	TS124M ₆₃	TS124M ₆₄	TS124M ₆₅	TS124M ₆₆	TS124M ₆₇	TS124M ₆₈	TS124M ₆₉	TS124M ₇₀	TS124M ₇₁	TS124M ₇₂	TS124M ₇₃	TS124M ₇₄	TS124M ₇₅	TS124M ₇₆	TS124M ₇₇	TS124M ₇₈	TS124M ₇₉	TS124M ₈₀	TS124M ₈₁	TS124M ₈₂	TS124M ₈₃	TS124M ₈₄	TS124M ₈₅	TS124M ₈₆	TS124M ₈₇	TS124M ₈₈	TS124M ₈₉	TS124M ₉₀	TS124M ₉₁	TS124M ₉₂	TS124M ₉₃	TS124M ₉₄	TS124M ₉₅	TS124M ₉₆	TS124M ₉₇	TS124M ₉₈	TS124M ₉₉	TS124M ₁₀₀																																																																																																																																
5614	0024	5615	2324	5616	4003	5617	4003	5618	1405	5619	1640	5620	1640	5621	1640	5622	1640	5623	1640	5624	1640	5625	1640	5626	1640	5627	1640	5628	1640	5629	1640	5630	1640	5631	1640	5632	1640	5633	1640	5634	1640	5635	1640	5636	1640	5637	1640	5638	1640	5639	1640	5640	1640	5641	1640	5642	1640	5643	1640	5644	1640	5645	1640	5646	1640	5647	1640	5648	1640	5649	1640	5650	1640	5651	1640	5652	1640	5653	1640	5654	1640	5655	1640	5656	1640	5657	1640	5658	1640	5659	1640	5660	1640	5661	1640	5662	1640	5663	1640	5664	1640	5665	1640	5666	1640	5667	1640	5668	1640	5669	1640	5670	1640	5671	1640	5672	1640	5673	1640	5674	1640	5675	1640	5676	1640	5677	1640	5678	1640	5679	1640	5680	1640	5681	1640	5682	1640	5683	1640	5684	1640	5685	1640	5686	1640	5687	1640	5688	1640	5689	1640	5690	1640	5691	1640	5692	1640	5693	1640	5694	1640	5695	1640	5696	1640	5697	1640	5698	1640	5699	1640	5700	1640	5701	1640	5702	1640	5703	1640	5704	1640	5705	1640	5706	1640	5707	1640	5708	1640	5709	1640	5710	1640	5711	1640	5712	1640	5713	1640	5714	1640	5715	1640	5716	1640	5717	1640	5718	1640	5719	1640	5720	1640	5721	1640	5722	1640	5723	1640	5724	1640	5725	1640	5726	1640	5727	1640

1/TS125 GLC CHANGES COUNT

5632	0024	TS125M	0024
5633	2324		2324
5634	6265		4003
5635	4003		4003
5636	1403		1403
5637	0140		0140
5640	0310		0310
5641	0116		0116
5642	0705		0705
5643	2340		2340
5644	0317		0317
5645	2516		2516
5646	2400		2400
5647	7777		7777
5650	7054		7054
5651	0053		0053
5652	0000		0000

15129 BUFFER <> COUNTER FAILED

5653	10224	TS126M,	0024
5654	23224		23224
5655	6266		6266
5656	4002		4002
5657	2506		2506
5660	1605		0605

2274	5661	5676	0024	5672	0024	5722	0024	5722	0000	EX1T
2274	5662	7603	5675	0053	0053	5721	0000	5721	0000	EX1T
7603	5663	5674	0054	0054	0054	5720	0053	5720	0053	RXED
1725	5664	5675	0054	0054	0054	5719	0054	5719	0054	SEND
1624	5665	5676	0054	0054	0054	5718	0054	5718	0054	EX1T
5665	5666	5677	0054	0054	0054	5717	0054	5717	0054	EX1T
5667	5667	5678	0054	0054	0054	5716	0054	5716	0054	EX1T
0111	5668	5679	0054	0054	0054	5715	0054	5715	0054	EX1T
1405	5669	5680	0054	0054	0054	5714	0054	5714	0054	EX1T
0400	5670	5681	0054	0054	0054	5713	0054	5713	0054	EX1T
0400	5671	5682	0054	0054	0054	5712	0054	5712	0054	EX1T
5672	5672	5683	0054	0054	0054	5711	0054	5711	0054	EX1T
5673	5673	5684	0054	0054	0054	5710	0054	5710	0054	EX1T
5674	5674	5685	0054	0054	0054	5709	0054	5709	0054	EX1T
5675	5675	5686	0054	0054	0054	5708	0054	5708	0054	EX1T
5676	5676	5687	0054	0054	0054	5707	0054	5707	0054	EX1T
5677	5677	5688	0054	0054	0054	5706	0054	5706	0054	EX1T
5678	5678	5689	0054	0054	0054	5705	0054	5705	0054	EX1T
5679	5679	5690	0054	0054	0054	5704	0054	5704	0054	EX1T
5680	5680	5691	0054	0054	0054	5703	0054	5703	0054	EX1T
5681	5681	5692	0054	0054	0054	5702	0054	5702	0054	EX1T
5682	5682	5693	0054	0054	0054	5701	0054	5701	0054	EX1T
5683	5683	5694	0054	0054	0054	5700	0054	5700	0054	EX1T
5684	5684	5695	0054	0054	0054	5699	0054	5699	0054	EX1T
5685	5685	5696	0054	0054	0054	5698	0054	5698	0054	EX1T
5686	5686	5697	0054	0054	0054	5697	0054	5697	0054	EX1T
5687	5687	5698	0054	0054	0054	5696	0054	5696	0054	EX1T
5688	5688	5699	0054	0054	0054	5695	0054	5695	0054	EX1T
5689	5689	5700	0054	0054	0054	5694	0054	5694	0054	EX1T
5690	5690	5701	0054	0054	0054	5693	0054	5693	0054	EX1T
5691	5691	5702	0054	0054	0054	5692	0054	5692	0054	EX1T
5692	5692	5703	0054	0054	0054	5691	0054	5691	0054	EX1T
5693	5693	5704	0054	0054	0054	5690	0054	5690	0054	EX1T
5694	5694	5705	0054	0054	0054	5689	0054	5689	0054	EX1T
5695	5695	5706	0054	0054	0054	5688	0054	5688	0054	EX1T
5696	5696	5707								

175728 "LOAD CNT" LOADED IN ERROR

7/15/72 "LOAD CNT" fails to "OP"

EXIT

TST29M, 0024

5746 0000

5747 0024

5750 0024

5751 0024

5752 0024

5753 0024

5754 0024

5755 0024

5756 0024

5757 0024

5758 0024

5759 0024

5760 0024

5761 0024

5762 0024

5763 0024

5764 0024

5765 0024

5766 0024

5767 0024

5768 0024

5769 0024

5770 0024

5771 0024

5772 0024

5773 0024

EXIT

TST30M, 0024

5774 0024

5775 0024

5776 0024

5777 0024

5778 0024

5779 0024

5780 0024

5781 0024

5782 0024

5783 0024

5784 0024

5785 0024

5786 0024

5787 0024

5788 0024

5789 0024

5790 0024

5791 0024

5792 0024

5793 0024

5794 0024

5795 0024

5796 0024

5797 0024

EXIT

TST31M, 0024

6020 0020

6021 0024

6022 0024

6023 0024

6024 0024

6025 0024

6026 0024

6027 0024

6028 0024

EXIT

SEND

RXED

EXIT

EXIT

EXIT

EXIT

EXIT

EXIT

EXIT

EXIT

/TST31 MODE REG CAUSES "LOAD CNT" OR "CLR BUF"

/TST30 MODE REG CAUSES "LOAD CNT"

/TST29 "LOAD CNT" LOADED IN ERROR

60533	05223	60534	4042	60335	1417	60336	0104	60337	4003	6040	1624	4240	6041	4240	6042	1722	4042	0314	2240	0225	0642	4000	EX1TA	SEND	RXC0	REG6	EX1T	
60533	05223	60334	4042	60335	1417	60336	0104	60337	4003	6040	1624	4240	6041	4240	6042	1722	4042	0314	2240	0225	0642	4000	EX1TA	SEND	RXC0	REG6	EX1T	
60556	0024	6057	2324	6060	6362	6062	1704	6063	0540	6064	6272	4061	6066	7660	4003	1417	0313	0504	4003	1624	2200	6075	6076	7777	0054	0053	0000	6101
60556	0024	6057	2324	6060	6362	6062	1704	6063	0540	6064	6272	4061	6066	7660	4003	1417	0313	0504	4003	1624	2200	6075	6076	7777	0054	0053	0000	6101
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6272	4062	6111	4062	6112	7661	4003	1417	0313	0504	6114	1417	0313	0504	4003	6117
6102	0024	6103	2324	6104	6363	6105	4015	6106	1704	6107	0540	6110	6															

195735 MODE 21 021 CLOCKED CNTR

75732 MODE 21 120 CLOKED CNTR

6120	1624	6126	0024	15134M, 0024	1624
6121	2200	6127	2324	6364	2324
6122	7777	6130	6364	4817	6364
6123	0074	6131	4017	4817	4817
6124	0053	6132	4706	4706	4706
6125	0000	6133	1417	1417	1417
		6134	4006	4006	4006
		6135	0111	0111	0111
		6136	1405	1405	1405
		6137	0440	0440	0440
		6140	2417	2417	2417
		6141	4023	4023	4023
		6142	0524	0524	0524
		6143	4017	4017	4017
		6144	4706	4706	4706
		6145	1417	1417	1417
		6146	4006	4006	4006
		6147	1417	1417	1417
		6150	2000	2000	2000
		6151	0000	0000	0000
6152	0024	6152	0024	15135M, 0024	0024
6153	2324	6153	2324	6365	2324
6154	6365	6154	6365	4803	4803
6155	1423	6155	1423	0140	0140
6156	0140	6156	0140	0601	0601
6157	0601	6157	0601	1114	1114
6160	1114	6160	1114	0504	0504
6161	0504	6161	0504	4024	4024
6162	4024	6162	4024	1740	1740
6163	1740	6163	1740	0314	0314
6164	0314	6164	0314	0501	0501
6165	0501	6165	0501	2240	2240
6166	2240	6166	2240	4017	4017
6167	4017	6167	4017	4706	4706
6170	4706	6170	4706	1417	1417
6171	1417	6171	1417	4006	4006
6172	4006	6172	4006	1417	1417
6173	1417	6173	1417	2000	2000
6174	2000	6174	2000	6176	6176
6175	6176	6175	6176	0024	0024
6200	0024	6200	0024	15136M, 0024	0024
6201	6366	6201	6366	2324	2324
6202	4003	6202	4003	6366	6366
6203	1423	6203	1423	4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417
				2000	2000
				EX17	EX17
				0024	0024
				15136M, 0024	0024
				2324	2324
				6366	6366
				4803	4803
				0140	0140
				0601	0601
				1114	1114
				0504	0504
				4024	4024
				1740	1740
				0314	0314
				0501	0501
				2240	2240
				4017	4017
				4706	4706
				1417	1417
				4006	4006
				1417	1417

/TS137 ILLEGAL CLOCK INTERRUPT!

/TS138 CLK FAILED TO SKIP

/TS139 CLOCK INTERRUPT FAILED

6204	1340	6217	0024	TS137M:	0024	1340
6205	2313	6218	0000		0000	1340
6206	1120	6219	4000		4000	1340
6207	2005	6220	1722		1722	2005
6210	0440	6221	2222		2222	0440
6211	1116	6222	4005		4005	1116
6212	4005	6223	1116		1116	4005
6213	2222	6224	0405		0405	2222
6214	1722	6225	1120		1120	1722
6215	4000	6226	4000		4000	4000
6216	0000	6227	0000		0000	0000
6217	0024	6228	0024	TS137M:	0024	0024
6218	0000	6229	2324		2324	0000
6219	4000	6230	6367		6367	4000
6220	1722	6231	4011		4011	1722
6221	2222	6232	1414		1414	2222
6222	4005	6233	0507		0507	4005
6223	1116	6234	0114		0114	1116
6224	0405	6235	0114		0114	0405
6225	1120	6236	4100		4100	1120
6226	4000	6237	0000		0000	4000
6227	0000	6238	0024	TS138M:	0024	0024
6228	0024	6239	2024		2024	0024
6229	2324	6240	2225		2225	2324
6230	6370	6241	0522		0522	6370
6231	4003	6242	1624		1624	4003
6232	1423	6243	4011		4011	1423
6233	4003	6244	0313		0313	4003
6234	1340	6245	1417		1417	1340
6235	1340	6246	0313		0313	1340
6236	0601	6247	1417		1417	0601
6237	0504	6248	0114		0114	0504
6238	4024	6249	0504		0504	4024
6239	1740	6250	4024	TS139M:	0024	1740
6240	2313	6251	2313		2313	2313
6241	1120	6252	6255		6255	1120
6242	4000	6253	4000		4000	4000
6243	0000	6254	0000		0000	0000
6244	0024	6255	0024		0024	0024
6245	2324	6256	6257		6257	2324
6246	6371	6257	0024	TS139M:	0024	6371
6247	4003	6258	2324		2324	4003
6248	1417	6259	6371		6371	1417
6249	0313	6260	4003		4003	0313
6250	1417	6261	0313		0313	1417
6251	4011	6262	1417		1417	4011
6252	1624	6263	0313		0313	1624
6253	2225	6264	4011		4011	2225
6254	4000	6265	1624		1624	4000
6255	0000	6266	0922		0922	0000
6256	0024	6267	1624		1624	0024
6257	6257	6268	0922		0922	6257

6270	2225	6340	0024
6271	2024	6341	2324
6272	4006	6342	6462
6273	0111	6343	4003
6274	1405	6344	1417
6275	0400	6345	0313
6276	0000	6346	4011
		6347	1624
		6350	2240
		6351	2717
		6352	1647
		6353	2440
2225		6340	0024
2024		6341	2324
4006		6342	6462
0111		6343	4003
1405		6344	1417
0400		6345	0313
0000		6346	4011
		6347	1624
		6350	2240
		6351	2717
		6352	1647
		6353	2440
		6340	0024
		6341	2324
		6342	6462
		6343	4003
		6344	1417
		6345	0313
		6346	4011
		6347	1624
		6350	2240
		6351	2717
		6352	1647
		6353	2440
		6340	0024
		6341	2324
		6342	6462
		6343	4003
		6344	1417
		6345	0313
		6346	4011
		6347	1647
		6350	2440
		6351	1647
		6352	2717
		6353	0740
		6330	0740
		6327	1401
		6326	4006
		6325	1417
		6324	4706
		6323	4017
		6322	6461
		6321	2324
		6320	0024
		6317	0000
		6316	4000
		6315	2217
		6314	3205
		6313	2440
		6312	1647
		6311	2717
		6310	0540
		6307	0214
		6306	1601
		6305	4005
		6304	1417
		6303	4706
		6302	4017
		6301	6460
		6300	2324
		6277	0024
		6276	0000
		6275	0400
		6274	1405
		6273	0111
		6272	4006
		6271	2024
		6270	2225

TS140M, 0024

EXIT
0400
1405
0111
4006
2024
2225

/TS140 O'FLO ENABLE MONIT ZERO

EXIT
4000
2217
3205
2440
1647
2717
0540
0214
1601
4005
1417
4706
4017
6460
2324
0024

TS141M, 0024

/TS141 O'FLO FLAG MONIT CLEAR

EXIT
0401
1401
4006
1417
4706
4017
6461
2324
0024

TS142M, 0024

/TS142 CLOCK INTR MONIT CLEAR

EXIT
0501
0314
2440
1647
2717
0740
1401
4006
1417
4706
4017
6462
2324
0024

6354	0314	6435	0024
6355	0501	6436	0024
6356	2200	6437	0024
6357	0000	6438	0024
6360	0024	6439	0024
6361	2324	6440	0024
6362	6463	6441	0024
6363	4002	6442	0024
6364	1124	6443	0024
6365	4061	6444	0024
6366	6140	6445	0024
6367	0601	6446	0024
6370	1114	6447	0024
6371	0504	6448	0024
6372	5600	6449	0024
6373	7777	6450	0024
6374	0054	6451	0024
6375	0053	6452	0024
6376	0000	6453	0024
6377	0024	6454	0024
6380	0024	6455	0024
6381	2324	6456	0024
6382	6463	6457	0024
6383	4002	6458	0024
6384	1124	6459	0024
6385	4061	6460	0024
6386	6140	6461	0024
6387	0601	6462	0024
6390	1114	6463	0024
6391	0504	6464	0024
6392	5600	6465	0024
6393	7777	6466	0024
6394	0054	6467	0024
6395	0053	6468	0024
6396	0000	6469	0024
6397	0024	6470	0024
6398	0024	6471	0024
6399	2324	6472	0024
6400	6463	6473	0024
6401	4002	6474	0024
6402	1124	6475	0024
6403	4061	6476	0024
6404	6140	6477	0024
6405	0601	6478	0024
6406	1114	6479	0024
6407	0504	6480	0024
6408	5600	6481	0024
6409	7777	6482	0024
6410	0054	6483	0024
6411	0053	6484	0024
6412	0000	6485	0024
6413	0024	6486	0024
6414	0024	6487	0024
6415	2324	6488	0024
6416	6463	6489	0024
6417	4002	6490	0024
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6421	0601	6494	0024
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6427	0053	6500	0024
6428	0000	6501	0024
6429	0024	6502	0024
6430	0024	6503	0024
6431	2324	6504	0024
6432	6463	6505	0024
6433	4002	6506	0024
6434	1124	6507	0024
6435	4061	6508	0024
6436	6140	6509	0024
6437	0601	6510	0024
6438	1114	6511	0024
6439	0504	6512	0024
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6443	0053	6516	0024
6444	0000	6517	0024
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6446	0024	6519	0024
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6461	0024	6534	0024
6462	0024	6535	0024
6463	2324	6536	0024
6464	6463	6537	0024
6465	4002	6538	0024
6466	1124	6539	0024
6467	4061	6540	0024
6468	6140	6541	0024
6469	0601	6542	0024
6470	1114	6543	0024
6471	0504	6544	0024
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6474	0054	6547	0024
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6476	0000	6549	0024
6477	0024	6550	0024
6478	0024	6551	0024
6479	2324	6552	0024
6480	6463	6553	0024
6481	4002	6554	0024
6482	1124	6555	0024
6483	4061	6556	0024
6484	6140	6557	0024
6485	0601	6558	0024
6486	1114	6559	0024
6487	0504	6560	0024
6488	5600	6561	0024
6489	7777	6562	0024
6490	0054	6563	0024
6491	0053	6564	0024
6492	0000	6565	0024
6493	0024	6566	0024
6494	0024	6567	0024
6495	2324	6568	0024
6496	6463	6569	0024
6497	4002	6570	0024
6498	1124	6571	0024
6499	4061	6572	0024
6500	6140	6573	0024
6501	0601	6574	0024
6502	1114	6575	0024
6503	0504	6576	0024
6504	5600	6577	0024
6505	7777	6578	0024
6506	0054	6579	0024
6507	0053	6580	0024
6508	0000	6581	0024
6509	0024	6582	0024
6510	0024	6583	0024
6511	2324	6584	0024
6512	6463	6585	0024
6513	4002	6586	0024
6514	1124	6587	0024
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6528	6463	6601	0024
6529	4002	6602	0024
6530	1124	6603	0024
6531	4061	6604	0024
6532	6140	6605	0024
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6534	1114	6607	0024
6535	0504	6608	0024
6536	5600	6609	0024
6537	7777	6610	0024
6538	0054	6611	0024
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6541	0024	6614	0024
6542	0024	6615	0024
6543	2324	6616	0024
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6546	1124	6619	0024
6547	4061	6620	0024
6548	6140	6621	0024
6549	0601	6622	0024
6550	1114	6623	0024
6551	0504	6624	0024
6552	5600	6625	0024
6553	7777	6626	0024
6554	0054	6627	0024
6555	0053	6628	0024
6556	0000	6629	0024
6557	0024	6630	0024
6558	0024	6631	0024
6559	2324	6632	0024
6560	6463	6633	0024
6561	4002	6634	0024
6562	1124	6635	0024
6563	4061	6636	0024
6564	6140	6637	0024
6565	0601	6638	0024
6566	1114	6639	0024
6567	0504	6640	0024
6568	5600	6641	0024
6569	7777	6642	0024
6570	0054	6643	0024
6571	0053	6644	0024
6572	0000	6645	0024
6573	0024	6646	0024
6574	0024	6647	0024
6575	2324	6648	0024
6576	6463	6649	0024
6577	4002	6650	0024
6578	1124	6651	0024
6579	4061	6652	0024
6580	6140	6653	0024
6581	0601	6654	0024
6582	1114	6655	0024
6583	0504	6656	0024
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6585	7777	6658	0024
6586	0054	6659	0024
6587	0053	6660	0024
6588	0000	6661	0024
6589	0024	6662	0024
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6596	6140	6669	0024
6597	0601	6670	0024
6598	1114	6671	0024
6599	0504	6672	0024
6600	5600	6673	0024
6601	7777	6674	0024
6602	0054	6675	0024
6603	0053	6676	0024
6604	0000	6677	0024
6605	0024	6678	0024
6606	0024	6679	0024
6607	2324	6680	0024
6608	6463	6681	0024
6609	4002	6682	0024
6610	1124	6683	0024
6611	4061	6684	0024
6612	6140	6685	0024
6613	0601	6686	0024
6614	1114	6687	0024
6615	0504	6688	0024
6616	5600	6689	0024
6617	7777	6690	0024
6618	0054	6691	0024
6619	0053	6692	0024
6620	0000	6693	0024
6621	0024	6694	0024
6622	0024	6695	0024
6623	2324	6696	0024
6624	6463	6697	0024
6625	4002	6698	0024
6626	1124	6699	0024
6627	4061	6700	0024
6628	6140	6701	0024
6629	0601	6702	0024
6630	1114	6703	0024
6631	0504	6704	0024
6632	5600	6705	0024
6633	7777	6706	0024
6634	0054	6707	0024
6635	0053	6708	0024
6636	0000	6709	0024
6637	0024	6710	0024
6638	0024	6711	0024
6639	2324	6712	0024
6640	6463	6713	0024
6641	4002	6714	0024
6642	1124	6715	0024
6643	4061	6716	0024
6644	6140	6717	0024
6645	0601	6718	0024
6646	1114	6719	0024
6647	0504	6720	0024
6648	5600	6721	0024
6649	7777	6722	0024
6650	0054	6723	0024
6651	0053	6724	0024
6652	0000	6725	0024
6653	0024	6726	0024
6654	0024	6727	0024
6655	2324	6728	0024
6656	6463	6729	0024
6657	4002	6730	0024
6658	1124	6731	0024
6659	4061	6732	0024
6660	6140	6733	0024
6661	0601	6734	0024
6662	1114	6735	0024
6663	0504	6736	0024
6664	5600	6737	0024
6665	7777	6738	0024
6666	0054	6739	0024
6667	0053	6740	0024
6668	0000	6741	

6437	6466
6440	4802
6441	1124
6442	4868
6443	7848
6444	0601
6445	1114
6446	0504
6447	5600
6450	7777
6451	0054
6452	0053
6453	0000
6454	0024
6455	2324
6456	6467
6457	4802
6460	1124
6461	4868
6462	6748
6463	0601
6464	1114
6465	0504
6466	5600
6467	7777
6470	0054
6471	0053
6472	0000
6473	0024
6474	2324
6475	6478
6476	4802
6477	1124
6500	4868
6501	6648
6502	0601
6503	1114
6504	0504
6505	5600
6506	7777
6507	0054
6510	0053
6511	0000
6512	0024
6513	2324
6514	6471
6515	4802
6516	1124
6517	4868
6520	6548
6521	0601
6522	1114

TST49M, 0024

EXIT
RXED
SEND
EXIT

/TST49 BIT 05 FAILED,

TST48M, 0024

EXIT
RXED
SEND
EXIT

/TST48 BIT 06 FAILED,

TST47M, 0024

EXIT
RXED
SEND
EXIT

/TST47 BIT 07 FAILED,

0504 5600 EXITA
SEND RXED EXIT

0024
EXIT
RXED
SEND
EXITA
5600
0504

00204
2324
6566
4002
1124
4060
6440
0601
1114
0504
5600
EXIT A
SEND
RXED
EXIT

0024
2324
6566
4002
1124
0604
0644
0100
1114
0504
5600
EXITA
SEND
RXED
EXIT
0024

EX 17 A
SEND
RX ED
EX 17

02024
EX17A
SEND
RXED
EX17A
02024

0024
2324
6562
4002
1124
0900
6240
0601
1114
0504
5600
EX17A
SENO
RXED
EX17

1/15/55 04:15 PM

0024
2324
6566
4002
1124
4060
6440
0601
1114
0504
5601
EXIT A
CEND
RXED
EXIT

78751 BIT 03 FAILED.

EX 17 A
SEND
RX ED
EX 17

475152 BIT 02 FAILED

0024
2324
6562
4002
1124
0900
6240
0601
1114
0504
5600
EX17A
SENO
RXED
EX17

/TS153 BIT 01 FAILED,

TS153M, 0024

6606 0024
6607 2324
6610 6563
6611 4002
6612 1124
6613 4060
6614 6140
6615 0601
6616 1114
6617 0504
6620 5600
6621 7777
6622 0054
6623 0053
6624 0000
EXIT
SEND
RXCD
EXIT

TS154M, 0024

6625 0024
6626 2324
6627 6564
6630 4002
6631 1124
6632 4060
6633 6040
6634 0601
6635 1114
6636 0504
6637 5600
6640 7777
6641 0054
6642 0053
6643 0000
EXIT
SEND
RXCD
EXIT

TS155M, 0024

6644 0024
6645 2324
6646 6565
6647 4022
6650 0124
6651 0540
6652 6460
6653 0013
6654 0340
6655 0601
6656 1114
6657 2300
6660 0000
EXIT

TS156M, 0024

6661 0024
6662 2324
6663 6566
6664 4022
6665 0124
6666 0540
6667 6160
6670 6013
6671 0340

/TS155 RATE 400KC FAILS

/TS156 RATE 100KC FAILS

/TS154 BIT 00 FAILED

6606 0024
6607 2324
6610 6563
6611 4002
6612 1124
6613 4060
6614 6140
6615 0601
6616 1114
6617 0504
6620 5600
6621 7777
6622 0054
6623 0053
6624 0000
EXIT
SEND
RXCD
EXIT

6625 0024
6626 2324
6627 6564
6630 4002
6631 1124
6632 4060
6633 6040
6634 0601
6635 1114
6636 0504
6637 5600
6640 7777
6641 0054
6642 0053
6643 0000
EXIT
SEND
RXCD
EXIT

6644 0024
6645 2324
6646 6565
6647 4022
6650 0124
6651 0540
6652 6460
6653 0013
6654 0340
6655 0601
6656 1114
6657 2300
6660 0000
EXIT

6661 0024
6662 2324
6663 6566
6664 4022
6665 0124
6666 0540
6667 6160
6670 6013
6671 0340

6672	0001	6673	1114	6674	2300	6675	0000
6754	1116	6755	0000	6756	0024	6757	0024
6753	0140	6754	0114	6755	0024	6756	0024
6752	1001	6753	0114	6754	0024	6755	0024
6751	0003	6752	0114	6753	0024	6754	0024
6750	0003	6751	0114	6752	0024	6753	0024
6747	0003	6748	0114	6749	0024	6750	0024
6746	0003	6747	0114	6748	0024	6749	0024
6745	0024	6746	0114	6747	0024	6748	0024
6744	0024	6745	0114	6746	0024	6747	0024
6743	0000	6744	0114	6745	0024	6746	0024
6742	0000	6743	0114	6744	0024	6745	0024
6741	0111	6742	0114	6743	0024	6744	0024
6740	0006	6741	0114	6742	0024	6743	0024
6737	2023	6738	0114	6739	0024	6740	0024
6736	0003	6737	0114	6738	0024	6739	0024
6735	0160	6736	0114	6737	0024	6738	0024
6734	0540	6735	0114	6736	0024	6737	0024
6733	0124	6734	0114	6735	0024	6736	0024
6732	4022	6733	0114	6734	0024	6735	0024
6731	6970	6732	0114	6733	0024	6734	0024
6730	2324	6731	0114	6732	0024	6733	0024
6727	0024	6728	0114	6729	0024	6730	0024
6726	0000	6727	0114	6728	0024	6729	0024
6725	2300	6726	0114	6727	0024	6728	0024
6724	1114	6725	0114	6726	0024	6727	0024
6723	0001	6724	0114	6725	0024	6726	0024
6722	0340	6723	0114	6724	0024	6725	0024
6721	0113	6722	0114	6723	0024	6724	0024
6720	0540	6721	0114	6722	0024	6723	0024
6717	0124	6718	0114	6719	0024	6720	0024
6716	4022	6717	0114	6718	0024	6719	0024
6715	6970	6716	0114	6717	0024	6718	0024
6714	2324	6715	0114	6716	0024	6717	0024
6713	0024	6714	0114	6715	0024	6716	0024
6712	0000	6713	0114	6714	0024	6715	0024
6711	4000	6712	0114	6713	0024	6714	0024
6710	1423	6711	0114	6712	0024	6713	0024
6707	0111	6708	0114	6709	0024	6710	0024
6706	4006	6707	0114	6708	0024	6709	0024
6705	1303	6706	0114	6707	0024	6708	0024
6704	0160	6705	0114	6706	0024	6707	0024
6703	0540	6704	0114	6705	0024	6706	0024
6702	0124	6703	0114	6704	0024	6705	0024
6701	4022	6702	0114	6703	0024	6704	0024
6700	6967	6701	0114	6702	0024	6703	0024
6677	2324	6678	0114	6679	0024	6680	0024
6676	0024	6677	0114	6678	0024	6679	0024
6675	0000	6676	0114	6677	0024	6678	0024
6674	2300	6675	0114	6676	0024	6677	0024
6673	1114	6674	0114	6675	0024	6676	0024
6672	0001	6673	0114	6674	0024	6675	0024

/TS160 CHAN 1 INPUT LOCKED OUT

/TS159 RATE 100CPS FAILS

/TS158 RATE 1KC FAILS

/TS157 RATE 10KC FAILS

6755	2025	6755	0024
6756	2440	6756	0024
6757	1417	6757	0024
6760	0313	6760	0024
6761	0504	6761	0024
6762	4017	6762	0024
6763	2524	6763	0024
6764	4000	6764	0024
6765	0000	6765	0024
6766	0024	6766	0024
6767	2324	6767	0024
6770	6661	6770	0024
6771	4003	6771	0024
6772	1001	6772	0024
6773	1640	6773	0024
6774	6340	6774	0024
6775	2717	6775	0024
6776	1647	6776	0024
6777	2440	6777	0024
7000	2417	7000	0024
7001	0707	7001	0024
7002	1405	7002	0024
7003	4000	7003	0024
7004	7777	7004	0024
7005	0054	7005	0024
7006	0053	7006	0024
7007	0000	7007	0024
7010	0024	7010	0024
7011	2324	7011	0024
7012	6662	7012	0024
7013	4003	7013	0024
7014	1001	7014	0024
7015	1640	7015	0024
7016	6240	7016	0024
7017	2717	7017	0024
7020	1647	7020	0024
7021	2440	7021	0024
7022	2417	7022	0024
7023	0707	7023	0024
7024	1405	7024	0024
7025	4000	7025	0024
7026	7777	7026	0024
7027	0054	7027	0024
7030	0053	7030	0024
7031	0000	7031	0024
7032	0024	7032	0024
7033	2324	7033	0024
7034	6663	7034	0024
7035	4003	7035	0024
7036	1001	7036	0024
7037	1640	7037	0024
7040	6140	7040	0024

/TS163M, 0024

EX17
SEND
RXED
EX17A

/TS163 CHAN 1 MONIT TOGGLE

/TS162M, 0024

EX17
SEND
RXED
EX17A

/TS162 CHAN 2 MONIT TOGGLE

/TS161M, 0024

EX17
SEND
RXED
EX17A

/TS161 CHAN 3 MONIT TOGGLE

7041	2717	7042	1647
7043	2440	7045	1647
7044	2417	7046	2440
7045	0707	7047	1405
7046	1405	7048	4000
7047	4000	7049	4000
7050	7777	7051	0054
7052	0053	7053	0000
7054	0024	7055	2324
7056	6664	7057	4003
7058	1001	7061	1640
7062	4061	7063	4027
7064	1716	7065	4724
7066	4011	7067	1624
7070	2200	7071	0000
7072	0024	7073	2324
7074	6665	7075	4003
7076	1001	7077	1640
7100	4061	7101	4011
7102	1624	7103	2240
7104	1116	7105	4005
7106	2222	7107	1722
7110	4000	7111	0000
7112	0024	7113	2324
7114	6666	7115	4003
7116	1001	7117	1640
7120	6240	7121	2717
7122	1647	7123	2440
7124	1116	7125	2440

TST65M, 0024

TST65M, 0024

TST64M, 0024

/TST66 CHAN 2 MONIT INTR, 0024

/TST65 CHAN 1 INTR IN ERROR, 0024

/TST64 CHAN 1 MONIT INTR, 0024

EX17A
SEND
RXED
EX17

7125	2422	2422
7126	5600	5600
7127	7777	7777
7130	0054	0054
7131	0053	0053
7132	0000	0000
7133	0024	0024
7134	2324	2324
7135	6667	6667
7136	4003	4003
7137	1001	1001
7140	1640	1640
7141	6240	6240
7142	1116	1116
7143	2422	2422
7144	4011	4011
7145	1640	1640
7146	0522	0522
7147	2217	2217
7150	2200	2200
7151	0000	0000
7152	0024	0024
7153	2324	2324
7154	6670	6670
7155	4003	4003
7156	1001	1001
7157	1640	1640
7160	6340	6340
7161	2717	2717
7162	1647	1647
7163	2440	2440
7164	1116	1116
7165	2422	2422
7166	5600	5600
7167	7777	7777
7170	0054	0054
7171	0053	0053
7172	0000	0000
7173	0024	0024
7174	2324	2324
7175	6671	6671
7176	4003	4003
7177	1001	1001
7200	1640	1640
7201	6340	6340
7202	1116	1116
7203	2422	2422
7204	4011	4011
7205	1640	1640
7206	0522	0522
7207	2217	2217
7210	2200	2200

TS169M, 0024

EXIT
SEND
RXED
EXIT

/TS169 CHAN 3 INTR IN ERROR

TS168M, 0024

EXIT
SEND
RXED
EXIT

/TS168 CHAN 3 MONIT INTR.

TS167M, 0024

EXIT
SEND
RXED
EXIT

/TS167 CHAN 2 INTR IN ERROR

7211 0000 EXIT

7212 0024 TS170H, 0024

/TS170 CHAN 3 INPUT LINE REG FAILED

EXIT

7213 2324

7214 6760

7215 4003

7216 1001

7217 1640

7220 6340

7221 1116

7222 2025

7223 2440

7224 1411

7225 1605

7226 4006

7227 2205

7230 2140

7231 0601

7232 1114

7233 0504

7234 4000

7235 7777

7236 0053

7237 0000

7240 0024

7241 2324

7242 6761

7243 4003

7244 1001

7245 1640

7246 6240

7247 1116

7250 2025

7251 2440

7252 1411

7253 1605

7254 4006

7255 2205

7256 2140

7257 0601

7260 1114

7261 0504

7262 4000

7263 7777

7264 0053

7265 0000

7266 0024

7267 2324

7270 6762

7271 4003

7272 1001

7273 1640

7274 6140

7275 1001

7276 1001

7277 1001

7278 1001

7279 1001

7280 1001

7281 1001

7282 1001

7283 1001

7284 1001

7285 1001

7286 1001

7287 1001

7288 1001

7289 1001

7290 1001

7291 1001

7292 1001

7293 1001

7294 1001

7295 1001

7296 1001

7297 1001

7298 1001

7299 1001

7300 1001

7301 1001

7302 1001

7303 1001

7304 1001

7305 1001

7306 1001

7307 1001

7308 1001

7309 1001

7310 1001

7311 1001

7312 1001

7313 1001

7314 1001

7315 1001

7316 1001

7317 1001

7318 1001

7319 1001

7320 1001

7321 1001

7322 1001

7323 1001

7324 1001

7325 1001

7326 1001

7327 1001

7328 1001

7329 1001

7330 1001

7331 1001

7332 1001

7333 1001

7334 1001

7335 1001

7336 1001

7337 1001

7338 1001

7339 1001

7340 1001

7341 1001

7342 1001

7343 1001

7344 1001

7345 1001

7346 1001

7347 1001

7348 1001

7349 1001

7350 1001

7351 1001

7352 1001

7353 1001

7354 1001

7355 1001

7356 1001

7357 1001

7358 1001

7359 1001

7360 1001

7361 1001

7362 1001

7363 1001

7364 1001

7365 1001

7366 1001

7367 1001

7368 1001

7369 1001

7370 1001

7371 1001

7372 1001

7373 1001

7374 1001

7375 1001

7376 1001

7377 1001

7378 1001

7379 1001

7380 1001

7381 1001

7382 1001

7383 1001

7384 1001

7385 1001

7386 1001

7387 1001

7388 1001

7389 1001

7390 1001

7391 1001

7392 1001

7393 1001

7394 1001

7395 1001

7396 1001

7397 1001

7398 1001

7399 1001

7400 1001

7401 1001

7402 1001

7403 1001

7404 1001

7405 1001

7406 1001

7407 1001

7408 1001

7409 1001

7410 1001

7411 1001

7412 1001

7413 1001

7414 1001

7415 1001

7416 1001

7417 1001

7418 1001

7419 1001

7420 1001

7421 1001

7422 1001

7423 1001

7424 1001

7425 1001

7426 1001

7427 1001

7428 1001

7429 1001

7430 1001

7431 1001

7432 1001

7433 1001

7434 1001

7435 1001

7436 1001

7437 1001

7438 1001

7439 1001

7440 1001

7441 1001

7442 1001

7443 1001

7444 1001

7445 1001

7446 1001

7447 1001

7448 1001

7449 1001

7450 1001

7451 1001

7452 1001

7453 1001

7454 1001

7455 1001

7456 1001

7457 1001

7458 1001

7459 1001

7460 1001

7461 1001

7462 1001

7463 1001

7464 1001

7465 1001

7466 1001

7467 1001

7468 1001

7469 1001

7470 1001

7471 1001

7472 1001

7473 1001

7474 1001

7475 1001

7476 1001

7477 1001

7478 1001

7479 1001

7480 1001

7481 1001

7482 1001

7483 1001

7484 1001

7485 1001

7486 1001

7487 1001

7488 1001

7489 1001

7490 1001

7491 1001

7492 1001

7493 1001

7494 1001

7495 1001

7496 1001

7497 1001

7498 1001

7499 1001

7500 1001

7501 1001

7502 1001

7503 1001

7504 1001

7505 1001

7506 1001

7507 1001

7508 1001

7509 1001

7510 1001

7511 1001

7512 1001

7

7275	1116	7315	0024	TS173M, 0024	7314
7276	2025	7316	2324	7315	2324
7277	2440	7317	4006	7316	6763
7300	1411	7318	0024	7317	4006
7301	1605	7319	2324	7318	6763
7302	4006	7320	0123	7319	2440
7303	2205	7321	2440	7320	0123
7304	2140	7322	2301	7321	2440
7305	0601	7323	1540	7322	1540
7306	1114	7324	0601	7323	1540
7307	0504	7325	1114	7324	0601
7310	4000	7326	2300	7325	1114
7311	7777	7327	7777	7326	2300
7312	0053	7328	0054	7327	7777
7313	0000	7329	0053	7328	0054
7355	0024	7330	0054	7329	0053
7356	2324	7331	0053	7330	0054
7357	6765	7332	0000	7331	0053
7360	4006	7333	0024	7332	0000

/TS175 FAST SAM MONIT SET

/TS174 O'FLO MONIT FAST SAM

/TS173 FAST SAM FAILS

1116	2025	2440	1411	1605	4006	2205	2140	0601	1114	0504	4000	EX17A	RXED	EXIT
7314	0024	TS173M, 0024	7315	2324	6763	4006	0123	2440	2301	1540	0601	1114	2300	EX17A
7315	2324	7316	6763	4006	0123	2440	2301	1540	0601	1114	2300	EX17A	SEND	RXED
7316	6763	7317	4006	0123	2440	2301	1540	0601	1114	2300	EX17A	SEND	RXED	EXIT
7317	4006	7318	0024	7319	2324	6763	4006	0123	2440	2301	1540	0601	1114	2300
7318	0024	7319	2324	6763	4006	0123	2440	2301	1540	0601	1114	2300	EX17A	SEND
7319	2324	7320	0123	2440	2301	1540	0601	1114	2300	EX17A	SEND	RXED	EXIT	7324
7320	0123	7321	2440	2301	1540	0601	1114	2300	EX17A	SEND	RXED	EXIT	7325	1500
7321	2440	7322	2301	1540	0601	1114	2300	EX17A	SEND	RXED	EXIT	7326	2301	1500
7322	2301	7323	1540	0601	1114	2300	EX17A	SEND	RXED	EXIT	7327	7777	7328	0054
7323	1540	7324	0601	1114	2300	EX17A	SEND	RXED	EXIT	7329	0053	7330	0054	7331
7324	0601	7325	1114	2300	EX17A	SEND	RXED	EXIT	7330	0054	7331	0053	7332	0000
7325	1114	7326	2300	EX17A	SEND	RXED	EXIT	7331	0053	7332	0000	7333	0024	TS174M, 0024
7326	2300	7327	7777	7328	0054	7329	0053	7330	0054	7331	0053	7332	0000	7333
7327	7777	7328	0054	7329	0053	7330	0054	7331	0053	7332	0000	7333	0024	TS175M, 0024
7328	0054	7329	0053	7330	0054	7331	0053	7332	0000	7333	0024	TS175M, 0024	7334	4006
7329	0053	7330	0054	7331	0053	7332	0000	7333	0024	TS175M, 0024	7334	4006	7335	0054
7330	0054	7331	0053	7332	0000	7333	0024	TS175M, 0024	7334	4006	7335	0054	7336	2324
7331	0053	7332	0000	7333	0024	TS175M, 0024	7334	4006	7335	0054	7336	2324	7337	6765
7332	0000	7333	0024	TS175M, 0024	7334	4006	7335	0054	7336	2324	7337	6765	7338	4006
7333	0024	TS175M, 0024	7334	4006	7335	0054	7336	2324	7337	6765	7338	4006	7339	4006
7334	4006	7335	0054	7336	2324	7337	6765	7338	4006	7339	4006	7340	4006	7341
7335	0054	7336	2324	7337	6765	7338	4006	7339	4006	7340	4006	7341	4006	7342
7336	2324	7337	6765	7338	4006	7339	4006	7340	4006	7341	4006	7342	4006	7343
7337	6765	7338	4006	7339	4006	7340	4006	7341	4006	7342	4006	7343	4006	7344
7338	4006	7339	4006	7340	4006	7341	4006	7342	4006	7343	4006	7344	4006	7345
7339	4006	7340	4006	7341	4006	7342	4006	7343	4006	7344	4006	7345	4006	7346
7340	4006	7341	4006	7342	4006	7343	4006	7344	4006	7345	4006	7346	4006	7347
7341	4006	7342	4006	7343	4006	7344	4006	7345	4006	7346	4006	7347	4006	7348
7342	4006	7343	4006	7344	4006	7345	4006	7346	4006	7347	4006	7348	4006	7349
7343	4006	7344	4006	7345	4006	7346	4006	7347	4006	7348	4006	7349	4006	7350
7344	4006	7345	4006	7346	4006	7347	4006	7348	4006	7349	4006	7350	4006	7351
7345	4006	7346	4006	7347	4006	7348	4006	7349	4006	7350	4006	7351	4006	7352
7346	4006	7347	4006	7348	4006	7349	4006	7350	4006	7351	4006	7352	4006	7353
7347	4006	7348	4006	7349	4006	7350	4006	7351	4006	7352	4006	7353	4006	7354
7348	4006	7349	4006	7350	4006	7351	4006	7352	4006	7353	4006	7354	4006	7355
7349	4006	7350	4006	7351	4006	7352	4006	7353	4006	7354	4006	7355	4006	7356
7350	4006	7351	4006	7352	4006	7353	4006	7354	4006	7355	4006	7356	4006	7357
7351	4006	7352	4006	7353	4006	7354	4006	7355	4006	7356	4006	7357	4006	7358
7352	4006	7353	4006	7354	4006	7355	4006	7356	4006	7357	4006	7358	4006	7359
7353	4006	7354	4006	7355	4006	7356	4006	7357	4006	7358	4006	7359	4006	7360
7354	4006	7355	4006	7356	4006	7357	4006	7358	4006	7359	4006	7360	4006	7361
7355	4006	7356	4006	7357	4006	7358	4006	7359	4006	7360	4006	7361	4006	7362
7356	4006	7357	4006	7358	4006	7359	4006	7360	4006	7361	4006	7362	4006	7363
7357	4006	7358	4006	7359	4006	7360	4006	7361	4006	7362	4006	7363	4006	7364
7358	4006	7359	4006	7360	4006	7361	4006	7362	4006	7363	4006	7364	4006	7365
7359	4006	7360	4006	7361	4006	7362	4006	7363	4006	7364	4006	7365	4006	7366
7360	4006	7361	4006	7362	4006	7363	4006	7364	4006	7365	4006	7366	4006	7367
7361	4006	7362	4006	7363	4006	7364	4006	7365	4006	7366	4006	7367	4006	7368
7362	4006	7363	4006	7364	4006	7365	4006	7366	4006	7367	4006	7368	4006	7369
7363	4006	7364	4006	7365	4006	7366	4006	7367	4006	7368	4006	7369	4006	7370
7364	4006	7365	4006	7366	4006	7367	4006	7368	4006	7369	4006	7370	4006	7371
7365	4006	7366	4006	7367	4006	7368	4006	7369	4006	7370	4006	7371	4006	7372
7366	4006	7367	4006	7368	4006	7369	4006	7370	4006	7371	4006	7372	4006	7373
7367	4006	7368	4006	7369	4006	7370	4006	7371	4006	7372	4006	7373	4006	7374
7368	4006	7369	4006	7370	4006	7371	4006	7372	4006	7373	4006	7374	4006	7375
7369	4006	7370	4006	7371	4006	7372	4006	7373	4006	7374	4006	7375	4006	7376
7370	4006	7371	4006	7372	4006	7373	4006	7374	4006	7375	4006	7376	4006	7377
7371	4006	7372	4006	7373	4006	7374	4006	7375	4006	7376	4006	7377	4006	7378
7372	4006	7373	4006	7374	4006	7375	4006	7376	4006	7377	4006	7378	4006	7379
7373	4006	7374	4006	7375	4006	7376	4006	7377	4006	7378	4006	7379	4006	7380
7374	4006	7375	4006	7376	4006	7377	4006	7378	4006	7379	4006	7380	4006	7381
7375	4006	7376	4006	7377	4006	7378	4006	7379	4006	7380	4006	7381	4006	7382
7376	4006	7377	4006	7378	4006	7379	4006	7380	4006	7381	4006	7382	4006	7383
7377	4006	7378	4006	7379	4006	7380	4006	7381	4006	7382	4006	7383	4006	7384
7378	4006	7379	4006	7380	4006	7381	4006	7382	4006	7383	4006	7384	4006	7385
7379	4006	7380	4006	7381	4006	7382	4006	7383	4006	7384	4006	7385	4006	7386
7380	4006	7381	4006	7382	4006	7383	4006	7384	4006	7385	4006	7386	4006	7387
7381	4006	7382	4006	7383	4006	7384	4006	7385	4006	7386	4006	7387	4006	7388
7382	4006	7383	4006	7384	4006	7385	4006	7386	4006	7387	4006	7388	4006	7389
7383	4006	7384	4006	7385	4006	7386	4006	7387	4006	7388	4006	7389	4006	7390
7384	4006	7385	4006	7386	4006	7387	4006	7388	4006	7389	4006	7390	4006	7391
7385	4006	7386	4006	7387	4006	7388	4006	7389	4006	7390	4006	7391	4006	7392
7386	4006	7387	4006	7388	4006	7389	4006	7390	4006	7391	4006	7392	4006	7393
7387	4006	7388	4006	7389	4006	7390	4006	7391	4006	7392	4006	7393	4006	7394
7388	4006	7389	4006	7390	4006	7391	4006	7392	4006	7393	4006	7394	4006	7395
7389	4006	7390	4006	7391	4006	7392	4006	7393	4006	7394	4006	7395	4006	7396
7390	4006	7391	4006	7392	4006	7393	4006	7						

7361	0123	7376	0024
7362	2440	7377	2324
7363	2301	7400	6766
7364	1540	7401	4015
7365	2717	7402	1704
7366	1647	7403	0523
7367	2440	7404	4062
7368	2440	7405	5561
7369	2305	7406	4011
7370	2305	7407	1610
7371	2400	7410	1102
7372	7777	7411	1324
7373	0054	7412	4006
7374	0053	7413	0123
7375	0000	7414	2440
7376	0024	7415	2301
7377	7777	7416	1500
7378	0054	7417	7777
7379	0053	7420	0054
7380	0000	7421	0053
7381	0024	7422	0000
7382	2440	7423	0024
7383	2301	7424	2324
7384	1540	7425	6770
7385	2717	7426	4011
7386	1647	7427	3417
7387	2440	7430	4020
7388	2305	7431	2205
7389	2400	7432	2305
7390	7777	7433	2440
7391	0054	7434	2717
7392	0053	7435	1647
7393	0000	7436	2440
7394	0024	7437	2324
7395	2440	7440	1720
7396	2301	7441	4003
7397	1540	7442	1417
7398	2717	7443	0313
7399	1647	7444	4000
7400	2440	7445	5022

TS176M,

TS177M,

/TS176 MODES 2,1 INHIBIT FAST SAM

/TS178 I/O PRESET MONIT STOP CLOCK
/IRATE BITS 1 & 2}

0123
2440
2301
1540
2717
1647
2440
2305
2400
7777
0054
0053
0000
0024
2440
2301
1540
2717
1647
2440
2324
2440
2440
2305
4020
2205
2305
2440
2717
2717
1647
2440
2324
6770
4011
3417
4020
2205
2305
2440
2440
2717
2717
1647
2440
2324
0024
EXIT
SEND
RXED
EXIT

7446	0124	7447	0540
7450	0211	7451	2423
7452	4061	7453	4046
7454	4062	7455	5100
7456	0000	EX17	
7457	0024	TS179M,	0024
7460	2324	7461	7060
7462	4011	7463	3417
7464	4020	7465	2205
7466	2305	7467	2440
7470	2717	7471	1647
7472	2440	7473	2324
7474	1720	7475	4003
7476	1417	7477	0313
7500	4000	7501	5022
7502	0124	7503	0540
7504	0211	7505	2440
7506	6051	7507	4000
7510	0000	EX17	
7511	0024	TS181M,	0024
7512	2324	7513	7061
7514	4011	7515	3417
7516	4020	7517	2205
7520	2305	7521	2440
7522	2717	7523	1647
7524	2440	7525	0314
7526	0501	7527	2240
7530	1747	7531	0614
7532	1700		

/TS181 I/O PRESET MONIT CLEAR O'FLO

/TS180 I/O PRESET MONIT STOP CLOCK
(/RATE BIT 00)

/TSTB2 I/O PRESET MONIT CLEAR INTERRUPT ENABLE

EXIT

TSTB2M, 0024

2324

7062

4011

3417

4020

2205

2305

2440

2717

1647

2440

0314

0501

2240

1116

2405

2222

2520

2440

0516

0102

1405

7562

7563

0000

7533

0000

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

LOCJ+1

TSTB3M, 0024

2324

7063

4011

3417

4020

2205

2305

2440

2717

1647

2440

0314

0501

2240

1116

2405

2222

2520

2440

0516

0102

1405

7562

7563

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

/FOLD TEXT BACK INTO FREE CORE AREA

/TSTB3 I/O PRESET MONIT CLEAR INPUTS

2324

7063

4011

3417

4020

2205

2305

2440

2717

1647

2440

0314

0501

2240

1116

2405

2222

2520

2440

0516

0102

1405

7562

7563

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

7548

7549

7550

7551

7552

7553

7554

7555

7556

7557

7558

7559

7560

7561

7562

7563

7564

0000

7533

0024

7535

7062

7537

7542

7543

7544

7545

7546

7547

4362	4011
4363	3417
4364	4220
4365	2305
4366	2440
4367	4370
4368	2717
4369	1647
4370	4372
4371	2440
4372	0314
4373	0901
4374	2240
4375	1517
4376	4045
4377	4062
4378	4400
4379	4401
4380	4402

4403	0024	79705M	0024
4404	2324		2324
4405	7065		7065
4406	4011		4011
4407	3417		3417
4410	4020		4020
4411	2205		2205
4412	2305		2305
4413	2440		2440
4414	2717		2717
4415	1647		1647
4416	2440		2440
4417	0314		0314
4420	0501		0501
4421	2240		2240
4422	1517		1517
4423	0405		0405
4424	4060		4060
4425	4000		4000
4426	7777		7777
4427	0000		0000
EX17			EX17
EX17			EX17

4430	0024	TS186M	0024
4431	2324		2324
4432	7066		7066
4433	4006		4006
4434	0123		0123
4435	2440		2440
4436	2301		2301
4437	1540		1540
4440	1617		1617
4441	2440		2440
4442	0314		0314
4443	1501		1501
4444	2205		2205
4445	0400		0400
4446	7777		7777
EX17A			

0 MODE CLEAR MONIT PRESET I/O 89T87

158786 FAST SAM NOT CLEARED

/TS107 CHAN 1 MONIT TRANS CNT TO BUF

4447 0000 EX17

TS107M, 0024

4450	0024	4450	0024
4451	2324	4451	2324
4452	7067	4452	7067
4453	4003	4453	4003
4454	1001	4454	1001
4455	1640	4455	1640
4456	6140	4456	6140
4457	2717	4457	2717
4460	1647	4460	1647
4461	2440	4461	2440
4462	2422	4462	2422
4463	0116	4463	0116
4464	2340	4464	2340
4465	0316	4465	0316
4466	2440	4466	2440
4467	2417	4467	2417
4470	4002	4470	4002
4471	2506	4471	2506
4472	4000	4472	4000
4473	7777	4473	7777
4474	0116	4474	0116
4475	0000	4475	0000
4476	0024	4476	0024
4477	2324	4477	2324
4500	7070	4500	7070
4501	4003	4501	4003
4502	1001	4502	1001
4503	1640	4503	1640
4504	6240	4504	6240
4505	2717	4505	2717
4506	1647	4506	1647
4507	2440	4507	2440
4510	2422	4510	2422
4511	0116	4511	0116
4512	2340	4512	2340
4513	0316	4513	0316
4514	2440	4514	2440
4515	2417	4515	2417
4516	4002	4516	4002
4517	2506	4517	2506
4520	4000	4520	4000
4521	7777	4521	7777
4522	0116	4522	0116
4523	0000	4523	0000
4524	0024	4524	0024
4525	2324	4525	2324
4526	7071	4526	7071
4527	4003	4527	4003
4530	1001	4530	1001
4531	1640	4531	1640
4532	6340	4532	6340

TS109M, 0024

EX17
K0200
EX17A

/TS109 CHAN 3 MONIT TRANS CNT TO BUF

4533	2717	4533	2717
4534	1647	4534	1647
4535	2440	4535	2440
4536	2422	4536	2422
4537	0116	4537	0116
4540	2340	4540	2340
4541	0316	4541	0316
4542	2440	4542	2440
4543	2417	4543	2417
4544	4002	4544	4002
4545	2506	4545	2506
4546	4000	4546	4000
4547	7777	4547	7777
4550	0116	4550	0116
4551	0000	4551	0000
4552	0024	4552	0024
4553	2324	4553	2324
4554	7160	4554	7160
4555	4003	4555	4003
4556	1001	4556	1001
4557	1640	4557	1640
4560	6140	4560	6140
4561	2717	4561	2717
4562	1647	4562	1647
4563	2440	4563	2440
4564	2422	4564	2422
4565	0116	4565	0116
4566	2340	4566	2340
4567	0316	4567	0316
4570	2440	4570	2440
4571	2417	4571	2417
4572	4002	4572	4002
4573	2506	4573	2506
4574	4000	4574	4000
4575	7777	4575	7777
4576	0120	4576	0120
4577	0000	4577	0000
4600	0024	4600	0024
4601	2324	4601	2324
4602	7161	4602	7161
4603	4003	4603	4003
4604	1001	4604	1001
4605	1640	4605	1640
4606	6240	4606	6240
4607	2717	4607	2717
4610	1647	4610	1647
4611	2440	4611	2440
4612	2422	4612	2422
4613	0116	4613	0116
4614	2340	4614	2340
4615	0316	4615	0316
4616	2440	4616	2440
4617	2417	4617	2417

TST91M,

EXIT
K0300
EXITA

/TST91 CHAN 2 MONIT TRANS CNT TO BUF

TST90M,

EXIT
K0200
EXITA

/TST90 CHAN 1 MONIT TRANS CNT TO BUF

4654	0024	2324	4655	2324	7163	4657	4660	1001	1640	6340	1116	2025	2440	0601	1114	0504	4024	1740	0314	2240	0316	2400	EX17A	RXC0	EX17
4654	0024	2324	4655	2324	7163	4657	4660	1001	1640	6340	1116	2025	2440	0601	1114	0504	4024	1740	0314	2240	0316	2400	EX17A	RXC0	EX17

175795 CHAN 3 INPUT FAILED TO CLR CNT

7/15/94 ECO EM12-00034 IS EITHER NOT WORKING OR NOT INSTALLED

4704	7164	4704
4705	4005	4705
4706	0317	4706
4707	4005	4707
4710	1561	4710
4711	6255	4711
4712	6060	4712
4713	6063	4713
4714	6440	4714
4715	1123	4715
4716	4005	4716
4717	1124	4717
4720	1005	4720
4721	2240	4721
4722	1617	4722
4723	2440	4723
4724	2717	4724
4725	2213	4725
4726	1116	4726
4727	0740	4727
4730	1722	4730
4731	4016	4731
4732	1724	4732
4733	4011	4733
4734	1623	4734
4735	2401	4735
4736	1414	4736
4737	0504	4737
4740	0000	4740
4741	0013	4741
4742	2761	4742
4743	6240	4743
4744	2001	4744
4745	2323	4745
4746	5555	4746
4747	7777	4747
4750	0032	4750
4751	4444	4751

TS195M, 0013
 2761
 6240
 2001
 2323
 5555
 EX17A
 PASS
 EX17B

/KW12 PASS==(PASS)

/EXIT B CAUSES A RETURN TO 0177

[illegible]

ASCII	5051	M40215	5174	M4444	0162	TS117	0403
ASCRXT	5026	K0300	0180	M3400	0163	TS117M	0434
BELL	0021	K0377	0121	NEAROR	0030	TS118M	0466
BK47	1775	K0600	0124	OUTPAS	0031	TS119M	0476
BK55	2375	K0700	0125	PASS	0032	TS120M	0566
CLAB	6133	K0777	0125	POP	0002	TS122M	0516
CLBA	6136	K1000	0127	PINT	0010	TS123	0616
CLCA	6137	K1026	0130	PNTA	0033	TS121M	0540
CLEN	6134	K1777	0131	PNTB	0034	TS122	0643
CLLR	6132	K2000	0132	PNTC	0035	TS123M	0556
CLSA	6135	K3000	0133	PNTD	0036	TS123	0672
CLSK	6131	K3777	0134	PNTF	0040	TS124	0721
CNTR	0025	K0000	0135	PNTG	0041	TS124M	0614
CRLF	5135	K4100	0136	PNTH	0040	TS125M	0753
DATUM	5135	K5100	0137	PNTI	0043	TS126M	1012
DATYP	5163	K5252	0140	PNTJ	0044	TS126	1012
DN43	0022	K5555	0141	RANDOM	0045	TS126M	0653
DN47	0023	K0000	0142	RANDY	0010	TS127	1043
DN55	0024	K7774	0143	REGO	0040	TS127M	0676
ERROR8	0020	KPME	0071	REGA	0046	TS128	0677
ESF	0004	KPTE	0070	REGC	0000	TS128M	0722
EX17	0000	LDAT	1020	REGT	0001	TS129M	0747
EX1A	7777	LING	0001	REGT	0004	TS130M	1156
EX1B	4444	LOGA	1440	RETURN	0002	TS130M	0774
FO43	1603	LOGB	1472	RNA	0002	TS133	1003
FO55	2403	LOCC	1502	RNB	0041	TS131M	0602
FO61	2000	LOCD	2751	RNG	0002	TS132	1245
HERE	5137	LOGE	2753	RXED	0003	TS132M	0606
K0000	0074	LOGF	2774	SAN0	0100	TS133	1276
K0001	0075	LOGG	3036	SAM1	0001	TS133M	0602
K0002	0076	LOGH	3040	SEND	0004	TS134	1312
K0003	0077	LOGI	3062	SET	0005	TS134M	06126
K0004	0000	LOCJ	4332	SEIN	0002	TS135	1345
K0007	0101	LSITER	0027	SPACE	0006	TS135M	06192
K0010	0102	M0001	0144	TS110	0201	TS135M	00097
K0012	0103	M0002	0145	TS110M	0261	TS136	1401
K0014	0104	M0004	0146	TS111	0217	TS136M	06177
K0015	0105	M0010	0147	TS111M	0501	TS137	1432
K0017	0106	M0020	0150	TS112	0235	TS137M	06217
K0020	0107	M0040	0151	TS112M	0517	TS138	1447
K0037	0110	M0042	0152	TS113	0254	TS138M	06240
K0040	0111	M0100	0153	TS113M	0535	TS139	1464
K0060	0112	M0200	0154	TS114	0274	TS139M	06297
K0077	0113	M0400	0155	TS114M	0535	TS140	1502
K0177	0115	M1400	0157	TS115M	0571	TS141	1515
K0212	0116	M2000	0160	TS116	0540	TS141M	06320
							1534

TS142M 6340
TS143 1553
TS143M 6360
TS144 1613
TS144M 6377
TS145 1653
TS145M 6416
TS146 -1714
TS146M 6435
TS147 1755
TS147M 6454
TS148 2016
TS148M 6473
TS149 2097
TS149M 6512
TS150 2120
TS150M 6531
TS151 2161
TS151M 6550
TS152 2222
TS152M 6567
TS153 2263
TS153M 6606
TS154 2324
TS154M 6625
TS155 2365
TS155M 6644
TS156 2412
TS156M 6661
TS157 2437
TS157M 6676
TS158 2471
TS158M 6713
TS159 2520
TS159M 6727
TS160 2557
TS160M 6745
TS161 2604
TS161M 6766
TS162 2635
TS162M 7010
TS163 2666
TS163M 7032
TS164 2721
TS164M 7054
TS165 2741
TS165M 7072
TS166 2764
TS166M 7112
TS166N 8060
TS167 3004

TS167M 7133
TS168 3027
TS168M 7152
TS169 3050
TS169M 7173
TS170 3075
TS170M 7212
TS171 3127
TS171M 7240
TS172 3161
TS172M 7266
TS173 3213
TS173M 7314
TS174 3263
TS174M 7333
TS175 3324
TS175M 7355
TS176 3362
TS176M 7376
TS177 3406
TS177M 7423
TS178 3482
TS178M 7482
TS179 3493
TS179M 7497
TS179N 0063
TS181 3515
TS181M 7511
TS182 3552
TS182M 7534
TS183 3607
TS183M 4333
TS184 3636
TS184M 4357
TS185 3667
TS185M 4403
TS186 3734
TS186M 4430
TS187 3763
TS187M 4450
TS188 4032
TS188M 4064
TS189 4064
TS189M 4524
TS190 4120
TS190M 4552
TS190N 0064
TS191 4162
TS191M 4600
TS192 4215
TS192M 4626
TS193 4250

TS193M 4654
TS194 4270
TS194M 4702
TS195 4321
TS195M 4741
TYPE 0065
TYPECM 5100
TYPEOUT 5243
UP43 0066
UP55 0067
UP61 0070

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 29 SECONDS

3K CORE USED