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IDENTIFICATION

PRODUCT CODE:	MAINDEC-12-D8CA-D-(D)
PRODUCT NAME:	KW12-REAL TIME CLOCK DIAGNOSTIC
DATE CREATED:	OCTOBER 1, 1969
AUTHOR:	JAMES KELLY STEVE TEICHER

Mnemonic : KW12TST

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ABSTRACT

The KW-12 diagnostic program verifies the correct operation of the buffer preset register, the clock counter register, the clock control register, the clock enable register, the IO bus interfare, and the clock input channels. The test once started halts, only in case of an error or operator intervention.

REQUIREMENTS

Storage

Locations 0--3200 in bank 0 are utilized.

Equipment

PDP-12--with KW-12 option

Program Loading

a) If the Binary Loader is in memory, proceed to step b. Otherwise, load the binary loader into memory.

b) Set Left Switches=7777_8

c) Set: Right Switches=4000_8

d) Press IO preset and start Left Switches

e) Turn Reader on

General Description

The ability to transfer all numbers between the AC and the clock registers is thoroughly tested. All modes of the KW-12 operation are tested. The clock counter is operated at the five crystal controlled rates and at the rate of input channel 1. External KW-12 inputs are tested with the selector switch turned to line frequency. There are four test options of which one is to eliminate testing of the AD-12 fast SAM instruction which is affected by mode bit Ø of the KW-12.

Operation Procedure

a) Load programs with binary loader

b) Select option by setting right switches as follows:

1) Bit Ø (1) suppress test completion alarm
2) Bit 5 (1) suppress print pass completion printing
3) Bit 8 (1) suppress test of AD-12 fast SAM instruction

Normal operation on a PDP-12C is with right switches=ØØØØ

c) Set Selector switches on KW-12 panels to line frequency.

d) Set Left Switches=Ø2ØØ

e) If AD-12 fast SAM instructions is to be tested, set KNOB Ø to extreme counterclockwise and KNOB 1 to extreme clockwise.

f) Set mode key on PDP-8 mode, press ID preset, and start Left Switches.

Test Operation

After start; at location Ø2ØØ the program performs 39 tests per, pass, halting only in the case of an error. At the end of each pass, which requires approximately 30 seconds, the letter K is typed on the teletype unless suppressed by the right switch setting. If after 30 seconds the program fails to complete a pass the operator should stop the computer and check the location counter against the program listing as the program is in a counting loop which indicates a failure of the counter, the time house, or an external input channel.

After 16 complete passes of the test program, the program will cease testing and sound a distinctive whistle on the PDP-12 speaker, unless this mode is suppressed by the right switch setting.

Options:

There are 4 options available selected by the right switches.

Right Switch Setting	Description of Option
ØØØØ	Tests AD-12 fast SAM prints letter K after every pass of program after 16 passes of program quits test and sounds completion alarm on speaker
1ØØØ	Supresses test of AD-12 fast SAM
2ØØØ	Supresses typing of K after every pass of program
4ØØØ	Allows program to repeat indefinitely

All combinations of options are legal.

Errors

a) Error Halts--If the computer halts check the listing for explanation of the halt.

b) Failure of the counter time base or an external input channel can cause the program to loop indefinitely through a 2 or 3 instruction loop. If the program fails to complete a pass in approximately 30 seconds, the operator should stop the machine and check the location counter against the listing to determine if the program is waiting for a counter overflow or external input channel.

Manual Test

When the computer is halted, the run light is out, it is possible to check the advancement of the clock counter manually as follows:

a) Set mode Switch to PDP-8 mode

b) Set Left Switches equal to 6137

c) Press IO preset and DO alternately

After every press of the DO Switch, the clock counter will be read into the AD? Each press of IO preset will clear the AC and advance the clock counter one or two counts. Therefore, by noting the reading of the AC after each DO, the fact that the clock counter advanced may be ascertained.

TESTS

The following--tests are performed in the order listed below:

Test #	Description
TST 2Ø	Does AC change after a transfer to the Buffer Preset Register?
TST 21	Does the Buffer Preset Register Jam into the AC?
TST 22	Can the Buffer Preset Register be cleared to ØØØØ?
TST 23	Do all numbers transfer between the AC and the Buffer Preset Register?
TST 24	Do random numbers transfer between the AC and the Buffer Preset Register?
TST 25	Does reading the Buffer Preset Register change its content?
TST 26	Can the Buffer Preset Register gate perform at maximum speed?
TST 27	Can the Buffer Preset Register survive checkerboard patterns?
TST 28	Can the Buffer Preset Register handle random complement patterns?
TST 29	Does executing the CLEN instruction affect the AC?
TST 3Ø	Does the Buffer Preset Register change after a transfer to the clock counter register?
TST 31	Can the clock counter be read using the 6137 instruction?
TST 32	Can the clock counter be cleared?
TST 33	Do all numbers transfer between the Buffer Preset Register and the clock counter register?
TST 34	Do random numbers transfer between the Buffer Preset Register and the clock counter register?
TST 35	Does reading the clock counter register change its CONTENTS?

TST 37	Can the Buffer Preset Register be ORED into the clock counter register?
TST 38	Can the clock counter register be loaded with mode 2(Ø) in error?
TST 39	Can the clock counter be loaded with mode 1 (1) in error?
TEST 3Ø	Does rapid actuating of the mode gates affect counter?
TEST 31	This is a general gate shaking test of the mode flip flops.
TEST 32	Does mode bit 2 changing from 1 Ø clear the clock counter register?
TST 4Ø	Does the overflow of the clock counter register set the overflow flip flop?
TST 41A	This is a general test of the overflow flip flop.
TEST 4	This is a series of tests. Labeled TST 41 through TST 49B that check each bit of the counter.
TEST 5	Does the clock counter register count at all rates?
ITSTØ1	Does input channel 1 cause a proper interrupt?
INPTØ1	This is a simulated input test for channel 3.
ITSTØ2	Does input channel 2 cause a proper interrupt?
ITSTØ3	Does input channel 3 cause a proper interrupt?
INPTØ2	This is a simulated input test for channel 2.
INPTØ3	This is a simulated input test for channel 3.
INPTØ4	This is a test of the external inputs for channels 1, 2, 3 which includes a test of the M503 schmitt triggers.
TSM	This is a test of the affect of mode bit Ø(1) on the FAST sample instruction.
TSM1	Is the fast SAM instruction affected by mode bit Ø(Ø)?
TCNT1	Does IO preset clear the rate bits?

TCNT2	Does IO preset clear the overflow flip flop, the enable flip flops, and the mode flip flop?
TMOD1	Does Mode bit 1(1) work properly?
TMOD3	Does mode bit 1(1) and mode bit 2 (1) work properly?

clv

```
                /MAINDEC 12-D8CA-D-(D)
                /SUPER KILLER FOR CLOCKS

        6131    CLSA=6131
        6132    CLLR=6132
        6133    CLAB=6133                       /AC TO BUFFER PRESET REGISTER
        6134    CLBA=6134
        6135    CLSA=6135
        6136    CLBA=6136                       /BUFFER PRESET REGISTER TO AC
        6137    CLCA=6137
        7001    *1
00 1    5013            JMP I   RETURN

        0020    *20
0020    0000    SEND,   0
0021    0000    RXED,   0
0022    0000    REGA,   0
0023    0100    K0100,  0100
0024    0100    K0100,  0100

0025    7777    M0001,  -1
0026    0001    K0001,  1
0027    7776    M0002,  -2

0030    0003    K0003,  0003
0031    7774    M0004,  -4
0032    0007    K0007,  0007
0033    0017    K0017,  0017
0034    0037    K0037,  0037
0035    0077    K0077,  0077

0036    0177    K0177,  0177
0037    0377    K0377,  0377
0040    0777    K0777,  0777
0041    1777    K1777,  1777
0042    3777    K3777,  3777
0043    7777    K7777,  7777

0044    7770    M0010,  -10
0045    7760    M0020,  -20
0046    7740    M0040,  -40
0047    7700    M0100,  -100
0050    7600    M0200,  -200
0051    7400    M0400,  -0400

0052    7000    M1000,  -1000
0053    6000    M2000,  -2000
0054    4000    M4000,  -4000
0055    4000    K4000,  4000
```

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```
0166  0003   RANDOM,
0167  1166          TAD     RNA
0170  1173          TAD     RNB
0171  1174          TAD     RNC
0172  3166          DCA     RNA
0173  7004          RAL
0174  1166          TAD     RNA
0175  1173          TAD     RNB
0176  1174          TAD     RNC
0177  3173          DCA     RNB
0200  7004          RAL
0201  1166          TAD     RNA
0202  1173          TAD     RNB
0203  1174          TAD     RNC
0204  3174          DCA     RNC
0205  7004          RAL
0206  1166          TAD     RNA
0207  3166          DCA     RNA
0210  1166          TAD     RNA
0211  5466          JMP I   RANDOM
```

```
0002  2003   RN4,     2003
0003  7150   RN5,     7150
0004  2465   RN6,     2465
0005  2200   K2200,   2200
0006  0300   K0300,   0300
0007  0700   K0700,   0700
0010  1274   PNTA,    LOCA
0011  1310   PNTB,    LOCB
0012  1334   PNTC,    LOCC
0013  0000   RETURN,  0
0014  1000   K1000,   1000
0015  5252   K5252,   5252
0016  2000   K2000,   2000
0017  3000   K3000,   3000
0020  7700   K7700,   7700
0021  4100   K4100,   4100
0022  5000   K5000,   5000
0023  0200   K0200,   0200
0024  0020   K0020,   0020
0025  0350   TST27A,  TST27
0026  0700   TST35A,  TST35
0027  0033   TST32A,  TST32
0030  1011   TST38A,  TST38
0031  0014   K0014,   0014
0032  0004   K0004,   0004
0033  2075   PNTD,    LOCD
0034  2105   PNTE,    LOCE
0035  2121   PNTF,    LOCF
0036  2161   PNTG,    LOCG
0037  2172   PNTH,    LOCH
0040  2202   PNTI,    LOCI
0041  1135   TST49X,  TST49A
0042  1717   TST49Y,  TST49+13
0043  0010   K0010,   0010
0044  0040   K0040,   0040
0045  0400   K0400,   0400
0046  0500   K0500,   0500
0047  6000   K6000,   6000
0050  5555   K5555,   5555
0051  2015   IPT04,   INPT04
0052  2400   TSMA,    TSM
0053  2473   TSM1A,   TSM1
0054  2044   TCNT2A,  TCNT2
0055  1210   TST41B,  TST41A
0056  2600   K2600,   2600
0057  2106   INT01,   INPT01
0060  0002   K0002,   0002
0061  3327   COUNTX,  COUNT
0062  1362   TST31X,  TST31
      0177   *177
0177  7512          SKP
```

```
                *200
                /MAJOR START B MODE, AC=2
                /TEST 2:  TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
                /CLAB=6133  AC TO CLOCK PRESET REGISTER
                /CLBA=6136  CLOCK PRESET REGISTER TO AC
                /DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?
0200  0231            DCA I COUNTX
0201  7200    TST20,  CLA CLA
0202  1022            TAD     REGA            /GET A NUMBER-BINARY UPCOUNT SEQUENCE 0 THRU 7777
0203  6133            CLAB                    /LOAD BUFFER
0204  3021            DCA     RXED            /STORE WHAT WAS LEFT IN AC
0205  1021            TAD     RXED            /FETCH IT
0206  7041            CIA                     /INVERT CONTENTS OF AC
0207  1022            TAD     REGA            /SUBTRACT SEND
0210  7540            SZA CLA                 /EQUAL?
0211  7402            HLT                     /NO HALT CLAB CHANGED AC, EXAMINE CELL 22 FOR TEST NUMBER
0212  2022            ISZ     REGA            /CHANGE TEST NUMBER
0213  5200            JMP     TST20+1         /DO TEST 4096 TIMES

                /DOES BUFFER DATA JAM INTO THE AC

0214  7200    TST21,  CLA CLL
0215  3022            DCA     SEND            /0 SEND REG
0216  6133            CLAB                    /SET BUFFER AND PRESET REGISTER TO 0000
0217  7240            CLA CMA                 /SET AC TO 7777
0220  6136            CLBA                    /JAM BUFFER PRESET (0000) OVER AC (7777
0221  3021            DCA     RXED            /SAVE AC
0222  1021            TAD     RXED            /RESTORE AC
0223  7040            SZA CLA                 /DID AC BECOME (0000)?
0224  7402            HLT                     /CLBA FAILED TO CLEAR THE AC
0225  2022            ISZ     REGA
0226  5214            JMP     TST21           /DO TEST 4096 TIMES

                /DOES SIGNAL CLR BUF FUNCTION

0227  7240    TST22,  CLA CMA
0230  6133            CLAB                    /SET BUFF=7777
0231  7200            CLA CLL                 /CLEAR AC
0232  6133            CLAB                    /LOAD BUFFER TO ALL ZEROS
0233  3022            DCA     SEND            /SAVE AC
0234  6136            CLBA                    /READ BUFFER AND PRESET REGISTER
0235  3021            DCA     RXED            /SAVE TEST VALUE
0236  1021            TAD     RXED            /RESTORE IT
0237  7040            SZA CLA                 /DID BUFFER AND PRESET REGISTER GET CLEARED BY CLR CNT?
0240  7402            HLT                     /CLR BUF FAILED TO CLEAR THE BUFFER
0241  2022            ISZ     REGA            /
0242  5227            JMP     TST22           /DO TEST 4096 TIMES
```

```
                /DO ALL NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

0243  7300      TST23,  CLA CLL
0244  3220              DCA     SEND            /0 SEND REG
0245  1220              TAD     SEND            /GET TEST NUMBER
0246  6133              CLAB                    /SEND IT
0247  7200              CLA
0250  6136              CLBA                    /RETRIEVE IT
0251  3221              DCA     RXED            /SAVE IT
0252  1221              TAD     RXED            /RESTORE IT
0253  7041              CIA                     /COMPLEMENT
0254  1220              TAD     SEND            /ADD TEST NUMBER
0255  7640              SZA CLA                 /WERE THEY EQUAL?
0256  7402              HLT                     /AC - BUFFER TO AC DATA TRANSFER FAILED
0257  2220              ISZ     SEND            /INCREMENT TEST NUMBER
0260  5245              JMP     TST23+2         /DO TEST 4096 TIMES

                /DO RANDOM NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY

0261  4256      TST24,  JMS     RANDOM          /LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
0262  3220              DCA     SEND            /SAVE IT
0263  1220              TAD     SEND            /RESTORE IT
0264  6133              CLAB                    /SEND IT
0265  4256              JMS     RANDOM          /LOAD THE AC WITH A RANDOM NUMBER
0266  6136              CLBA                    /READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
0267  3221              DCA     RXED            /SAVE TEST RETURN
0270  1221              TAD     RXED            /RESTORE IT
0271  7041              CIA                     /COMPLEMENT
0272  1220              TAD     SEND            /SUBTRACT TEST NUMBER
0273  7640              SZA CLA                 /EQUAL?
0274  7402              HLT                     /AC - BUFFER - AC DATA INTERCHANGE FAILED
0275  2222              ISZ     REGA
0276  5261              JMP     TST24           /DO TEST 4096 TIMES
```

```
                /DOES READING THE BUFFER CHANGE ITS CONTENTS

0307  4256      TST25,  JMS     RANDOM          /GET RANDOM NUMBER
0310  3022              DCA     SEND            /SAVE IT
0311  1022              TAD     SEND            /RESTORE IT
0312  6133              CLAB                    /SEND IT
0313  4256              JMS     RANDOM          /LOAD AC WITH A RANDOM NUMBER
0314  6136              CLBA                    /BRING BACK TEST NUMBER
0315  4256              JMS     RANDOM          /LOAD AC WITH A RANDOM NUMBER
0316  6136              CLBA                    /READ BUFFER AGAIN
0317  3021              DCA     RXED            /SAVE TEST VALUE
0320  1021              TAD     RXED            /RESTORE IT
0321  7041              CIA                     /COMPLEMENT
0322  1022              TAD     SEND            /SUBTRACT TEST NUMBER
0323  7640              SZA CLA                 /EQUAL
0324  7402              HLT                     /CLBA CHANGED THE CONTENTS OF THE BUFFER
0325  2022              ISZ     REGA
0326  5277              JMP     TST25           /DO TEST 4096 TIMES

                /CAN THE GATES FUNCTION AT HIGH SPEED

0327  7200      TST26,  CLA CLL
0330  3022              DCA     SEND
0331  1022              TAD     SEND
0332  6133              CLAB
0333  6136              CLBA
0334  6133              CLAB
0335  6136              CLBA
0336  6133              CLAB
0337  6136              CLBA
0340  6133              CLAB
0341  6136              CLBA
0342  6133              CLAB
0343  6136              CLBA
0344  6133              CLAB
0345  6136              CLBA
0346  6133              CLAB
0347  6136              CLBA
0350  3021              DCA     RXED
0351  1021              TAD     RXED
0352  7041              CIA
0353  1022              TAD     SEND
0354  7040              SZA CLA
0355  7402              HLT                     /BUF FAILED TO TOGGLE AT HIGH SPEED
0356  2022              ISZ     SEND            /DO TEST 4096 TIMES
0357  5321              JMP     TST26+2
```

D8CA - D-(D)


```
                /CAN THE BUFFER SURVIVE CHECKERBOARD

2371  7200      TST27,  CLA CLL
2372  1220              TAD     RDEDC
2373  3420              DCA     SEND            /SAVE TEST PATTERN
2374  1220              TAD     SEND            /RESTORE IT
2375  6133              CLAB
2376  6136              CLBA
2377  7040              CMA
2400  6133              CLAB
2401  6136              CLBA
2402  7040              CMA
2403  6133              CLAB
2404  6136              CLBA
2405  7040              CMA
2406  6133              CLAB
2407  6136              CLBA
2410  7040              CMA
2411  6133              CLAB
2412  6136              CLBA
2413  7040              CMA
2414  6133              CLAB
2415  6136              CLBA
2416  7040              CMA
2417  6133              CLAB
2420  6136              CLBA
2421  7040              CMA
2422  6133              CLAB
2423  6136              CLBA
2424  7040              CMA
2425  6133              CLAB
2426  6136              CLBA
2427  7040              CMA
2430  3021              DCA     RXED            /SAVE FINAL PATTERN
2431  1021              TAD     RXED            /RESTORE IT
2432  7041              CIA                     /COMPLEMENT
2433  1020              TAD     SEND            /SUBTRACT TEST PATTERN
2434  7040              SZA CLA                 /EQUAL?
2435  7402              HLT                     /BUFFER FAILED CHECKBOARD TEST
2436  2022              ISZ     REGA            /DO TEST 4096 TIMES
2437  5225              JMP     TST27A          /CROSS PAGE REF TO TST27
```

```
                /
                /CAN THE BUFFER SURVIVE RANDOM COMPLEMENT PATTERNS
                /
0400  4026      TS126,  JMS     RANDOM          /GENERATE A RANDOM NUMBER
0401  3020              DCA     SEND            /SAVE IT
0402  1020              TAD     SEND            /RESTORE IT
0403  6133              CLAB
0404  6136              CLBA
0405  7040              CMA
0406  6133              CLAB
0407  6136              CLBA
0410  7040              CMA
0411  6133              CLAB
0412  6136              CLBA
0413  7040              CMA
0414  6133              CLAB
0415  6136              CLBA
0416  7040              CMA
0417  6133              CLAB
0420  6136              CLBA
0421  7040              CMA
0422  6133              CLAB
0423  6136              CLBA
0424  7040              CMA
0425  6133              CLAB
0426  6136              CLBA
0427  7040              CMA
0430  6133              CLAB
0431  6136              CLBA
0432  7040              CMA
0433  6133              CLAB
0434  6136              CLBA
0435  7040              CMA
0436  6133              CLAB
0437  6136              CLBA
0440  7040              CMA
0441  6133              CLAB
0442  6136              CLBA
0443  7040              CMA
0444  6133              CLAB
0445  6136              CLBA
0446  7040              CMA

0447  3021              DCA     RXED            /SAVE FINAL PATTERN
0450  1021              TAD     RXED            /RESTORE IT
0451  7041              CIA                     /COMPLEMENT
0452  1020              TAD     SEND            /SUBTRACT TEST PATTERN
0453  7440              SZA CLA                 /EQUAL?
0454  7402              HLT                     /BUFFER FAILED RANDOM COMPLEMENT PATTERN
0455  2022              ISZ     REGA
0456  5400              JMP     TS126           /DO TEST 4096 TIMES
```

```
2517  7000    NOP
              /CLEN=6134 AC TO CLOCK ENABLE REGISTER
              / DOES CLEN AFFECT THE AC
              /
2520  7000    TST29,  CLL CLA
2521  3020            DCA     SEND            /CLEAR SEND REG
2522  1020            TAD     SEND            /RESTORE TEST NUMBER
2523  6134            CLEN                    /DOES CLEN AFFECT AC
2524  3021            DCA     RXED            /SAVE AC
2525  1021            TAD     RXED            /RESTORE IT
2526  7041            CIA                     /COMPLEMENT
2527  1020            TAD     SEND            /SUBTRACT TEST NUMBER
2530  7640            SZA CLA                 /EQUAL?
2531  7402            HLT                     /AC TO CLOCK ENABLE REG CHANGED AC
2532  2020            ISZ     SEND            /INCREMENT TEST NUMBER
2533  5322            JMP     TST29+2
              /
              /TEST3: PRESET REGISTER AND COUNTER DATA INTERCHANGE
              /CLSA=6135 STATUS REGISTER TO AC
              /CLLR=6132 AC TO CLOCK CONTROL REGISTER


              /DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER

2534  7000    TST30,  CLL CLA
2535  3020            DCA     SEND            /CLEAR SEND REG
2536  6135            CLSA                    /CLEAR STATUS
2537  7000            CLA CLL
2540  1020            TAD     SEND            /RESTORE TEST NUMBER
2541  6133            CLAB                    /LOAD BUFFER PRESET REGISTER WITH A BINARY UPCOUNT NUMBER
2542  7000            CLA CLL
2543  6132            CLLR                    /STOP CLOCK, SET ALL MODES=0
2544  1023            TAD     K2100           /MODE CONTROL REG BIT 2=1
2545  6132            CLLR                    /SET MODE 2, ENABLING CLR LOAD CNT
2546  7000            CLA
2547  1025            TAD     K2200           /AC BIT 4=1, SIMULATE CLR OFLOW ON 6134
2550  6134            CLEN                    /TRANSER PRESET COUNT TO CLOCK COUNTER
2551  6136            CLBA                    /READ THE BUFFER
2552  3021            DCA     RXED            /SAVE IT
2553  1021            TAD     RXED            /RESTORE IT
2554  7041            CIA                     /COMPLEMENT
2555  1020            TAD     SEND            /SUBTRACT TEST NUMBER
2556  7040            SZA CLA                 /EQUAL?
2557  7402            HLT                     /TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
2560  2020            ISZ     SEND            /INCREMENT TEST NUMBER
2561  5330            JMP     TST30+2
```

```
                /DOES COUNTER DATA JAM THE BUFFER AND AC
                /CLCA=6107 CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC

0002  6103      TST31,  CLSA                    /CLEAR STATUS
0003  7300              CLA CLL
0004  6133              CLAB                    /LOAD BUFFER TO 0000
0005  6132              CLLR                    /STOP CLOCK, SET ALL MODES=0
0006  1023              TAD     K2100           /SET AC 05=1
0007  6132              CLLR                    /SET MODE 2=1, THEREBY CLEARING CLOCK COUNTER
0010  6134              CLEN                    /ENABLE INTERRUPT ON OVERFLOW
0011  7040              CLA CMA                 /SET AC 7777
0012  6133              CLAB                    /SET BUFFER 7777 AND AC
0013  6107              CLCA                    /READ COUNTER
0014  3021              DCA     RXED            /SAVE COUNT
0015  1021              TAD     RXED            /RESTORE IT
0016  7040              SZA CLA                 /ZERO?
0017  7402              HLT                     /COUNTER FAILED TO JAM 0000 INTO 7777
0020  2022              ISZ     REGA            /DO TEST 4096 TIMES
0021  5002              JMP I   TST31X          /CROSS PAGE REFERENCE TO TST31
0022  3026              DCA     SEND            /ZERO SEND FOR NEXT TEST
                /DOES SIGNAL CLR CNT WORK
0023  6103      TST32,  CLSA                    /CLEAR STATUS
0024  7053              CLA CMA CLL RAR         /SET AC=3777
0025  6133              CLAB                    /SET BUFFER TO 3777 (USE 3777 SO WE DON'T SET OVERFLOW FLOP)
0026  7300              CLA CLL
0027  1025              TAD     K2200           /ENABLE LOAD COUNT GATES
0030  6134              CLEN                    /LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
0031  7300              CLA CLL
0032  6132              CLLR                    /ZERO MODE 2
0033  1023              TAD     K2100           /SET AC 05=1
0034  6132              CLLR                    /SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
0035  7300              CLA CLL
0036  6107              CLCA                    /READ THE COUNTER
0037  3021              DCA     RXED            /SAVE IT
0040  1021              TAD     RXED            /RESTORE IT
0041  7040              SZA CLA                 /ZERO?
0042  7402              HLT                     /CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
0043  2022              ISZ     REGA            /DO TEST 4096 TIMES
0044  5027              JMP I   TST32A          /INDIRECT REFERENCE TO TST32
```

D8CA-D-(D)


```
                /DO ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER

0625  6135  TST33,  CLSA                    /CLEAR STATUS
0626  7300          CLA CLL
0627  1222          TAD     SEND            /LOAD AC WITH TEST NUMBER
0630  6133          CLAB                    /SET BUFFER TO TEST NUMBER
0631  7300          CLA CLL
0632  6132          CLLR                    /STOP CLOCK, SET ALL MODES=0
0633  1223          TAD     K2100           /SET AC 05=1
0634  6132          CLLR                    /GENERATE "CLR CNT"
0635  7200          CLA
0636  1225          TAD     K0200           /SET AC 04=1
0637  6134          CLEN                    /GENERATE "LOAD CNT"
0640  6137          CLCA                    /COUNTER TO AC
0641  3021          DCA     RXED            /SAVE IT
0642  1021          TAD     RXED            /RESTORE IT
0643  7041          CIA                     /COMPLEMENT
0644  1222          TAD     SEND            /SUBTRACT TEST NUMBER
0645  7542          SZA CLA                 /EQUAL?
0646  7402          HLT                     /BUFFER TO COUNTER DATA INTERCHANGE FAILED
0647  2222          ISZ     SEND            /INCREMENT TEST NUMBER
0650  5225          JMP     TST33

                /DO RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER

0651  4056  TST34,  JMS     RANDOM          /GET RANDOM NUMBER
0652  6133          CLAB                    /LOAD BUFFER RANDOM
0653  3022          DCA     SEND            /SAVE TEST NUMBER
0654  6135          CLSA                    /CLEAR CLOCK STATUS
0655  7200          CLA                     /CLEAR AC
0656  6132          CLLR                    /STOP CLOCK, SET ALL MODES=0
0657  1223          TAD     K0100           /SET AC 05=1
0660  6132          CLLR                    /GENERATE "CLR CNT"
0661  7200          CLA
0662  1225          TAD     K0200           /SET AC 04=1
0663  6134          CLEN                    /GENERATE "LOAD CNT"
0664  4056          JMS     RANDOM          /GET RANDOM NUMBER
0665  6133          CLAB                    /LOAD BUFFER RANDOM
0666  4056          JMS     RANDOM          /LOAD AC RANDOM
0667  6137          CLCA                    /READ COUNTER
0670  3021          DCA     RXED            /SAVE TEST VALUE
0671  1021          TAD     RXED            /RESTORE IT
0672  7041          CIA                     /COMPLEMENT
0673  1022          TAD     SEND            /SUBTRACT TEST NUMBER
0674  7042          SZA CLA                 /EQUAL?
0675  7402          HLT                     /BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
0676  2022          ISZ     REGA            /DO TEST 4096 TIMES
0677  5251          JMP     TST34
```

12-08CA-D-(D)


```
                /DOES READING THE COUNTER CHANGE ITS STATE,

0700  4055      TST35,  JMS     RANDOM          /GET RANDOM TEST NUMBER
0701  6133              CLAB                    /SEND IT TO BUFFER
0702  3026              DCA     SEND            /SAVE IT
0703  6132              CLLR                    /STOP CLOCK, SET ALL MODES=0
0704  1025              TAD     K0100           /SET AC 05=1
0705  6132              CLLR                    /GENERATE "CLR CNT"
0706  6135              CLSA                    /CLEAR CLOCK STATUS
0707  7200              CLA
0710  1105              TAD     K0200           /SET AC 04=1
0711  6134              CLEN                    /GENERATE "LOAD CNT"
0712  4055              JMS     RANDOM          /GET RANDOM NUMBER
0713  6133              CLAB                    /SEND IT TO BUFFER
0714  4055              JMS     RANDOM          /GET RANDOM NUMBER
0715  6137              CLCA                    /READ CLOCK COUNTER
0716  4055              JMS     RANDOM          /GET RANDOM NUMBER
0717  6133              CLAB                    /SEND IT TO BUFFER
0720  4055              JMS     RANDOM          /GET RANDOM NUMBER
0721  6137              CLCA                    /READ CLOCK COUNTER
0722  3021              DCA     RXED            /SAVE IT
0723  1021              TAD     RXED            /RESTORE IT
0724  7041              CIA                     /COMPLEMENT
0725  1026              TAD     SEND            /SUBTRACT TEST NUMBER
0726  7642              SZA CLA                 /EQUAL?
0727  7402              HLT                     /(CLCA) READ THE COUNTER CHANGES THE COUNTERS STATE
0730  2022              ISZ     REGA            /DO TEST 4095 TIMES
0731  5035              JMP I   TST35A          /CROSS PAGE REF TO TST35

                /CAN THE BUF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED

0732  4055      TST36,  JMS     RANDOM          /GET RANDOM NUMBER
0733  6133              CLAB                    /SEND IT TO BUFFER
0734  3026              DCA     SEND            /SAVE IT
0735  7200              CLA
0736  6132              CLLR                    /STOP CLOCK
0737  1025              TAD     K0100           /SET AC 05=1
0740  6132              CLLR                    /GENERATE "CLR CNT"
0741  6135              CLSA                    /CLEAR CLOCK STATUS
0742  7200              CLA
0743  1105              TAD     K0200           /SET AC 04=1

0744  6134              CLEN                    /GENERATE "LOAD CNT"
0745  6137              CLCA                    /READ COUNTER
0746  2022              ISZ     REGA            /DO THIS 4096 TIMES
0747  5036              JMP     TST36+3
0750  3021              DCA     RXED            /SAVE FINAL NUMBER
0751  1021              TAD     RXED            /RESTORE IT
0752  7041              CIA                     /COMPLEMENT
0753  1026              TAD     SEND            /SUBTRACT TEST NUMBER
0754  7642              SZA CLA                 /EQUAL?
0755  7402              HLT                     /THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGHSPEED
```

08CA-D (D)


```
                /DOES (LOAD CNT) PERFORM LOGIC OR

2770  7200      TST37,  CLA CLL
2771  6132              CLLR
2772  1023              TAD     K0100           /SET AC 05=1
2773  6132              CLLR                    /GENERATE "CLR CNT"
2774  6135              CLSA                    /CLEAR CLOCK STATUS
2775  4056              JMS     RANDOM          /GET RANDOM TEST NUMBER
2776  6133              CLAB                    /LOAD BUFFER WITH A RANDOM NUMBER
2777  3022              DCA     SEND            /SAVE IT
2700  1025              TAD     K0200           /SET AC 04=1
2701  6134              CLEN                    /LOAD COUNTER FROM THE BUFFER REGISTER: GENERATE "LOAD CNT"
2702  7200              CLA CLL
2703  1022              TAD     SEND            /GET TEST NUMBER
2704  7040              CMA                     /COMPLEMENT
2705  6133              CLAB                    /LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
2706  7200              CLA CLL
2707  1025              TAD     K0200           /SET AC 04=1
2710  6134              CLEN                    /LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
2711  6137              CLCA                    /READ COUNTER.
2712  3021              DCA     RXED            /SAVE IT
2713  1021              TAD     RXED            /RESTORE IT
2714  7040              CMA                     /CONVERT TO ALL ZEROS FOR TESTING
2715  7040              SZA CLA                 /ZERO?
2716  7402              HLT                     /THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
2717  2022              ISZ     REGA            /DO TEST 4096 TIMES
2720  5312              JMP I   TST37X          /INDIRECT REF TO TST37
2721  7412              SKP
2722  2770              TST37X, TST37           /DEF. OF TST37X

                /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (0)

2723  7200      TST38,  CLA
2724  6133              CLAB                    /CLEAR BUFFER
2725  6132              CLLR                    /CLEAR ALL MODES
2726  1023              TAD     K0100           /SET AC 05=1
2727  6132              CLLR                    /GEN. "CLR CNT"
2730  6135              CLSA                    /CLEAR STATUS
2731  4056              JMS     RANDOM          /GET RANDOM NUMBER
2732  6133              CLAB                    /SEND IT TO BUFFER
2733  3022              DCA     SEND            /SAVE IT
2734  6132              CLLR                    /STOP CLOCK. SET ALL MODES=0
2735  1023              TAD     K0100           /SET AC 05=1
2736  6132              CLLR                    /GENERATE "CLR CNT"
2737  7200              CLA
2740  6132              CLLR                    /SET ALL MODES=0
2741  1025              TAD     K0200           /SET AC 04=1
2742  6134              CLEN                    /TRY TO GENERATE "LOAD CNT"
2743  6137              CLCA                    /GET COUNTER
2744  3021              DCA     RXED            /SAVE IT
2745  1021              TAD     RXED            /RESTORE IT
2746  7040              SZA CLA                 /WAS IT ZERO?
2747  7402              HLT                     /LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
2750  2022              ISZ     REGA            /DO TEST 4096 TIMES
```

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D8CA-D-(D)


```
                /TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 1(1)

1[illegible] [illegible]  TST39, JMS     RANDOM          /GET RANDOM NUMBER
1[illegible] 6183         CLAB                           /SEND IT TO BUFFER
1[illegible] 3020         DCA     SEND                   /SAVE IT
1[illegible] 1105         TAD     K0000                  /SET AC 04,05=1
1[illegible] 6102         CLLR                           /GENERATE "CLR CNT", SET MODE 1 AND 2 =1
1[illegible] 6103         CLSA                           /CLEAR CLOCK STATUS
1[illegible] 7200         CLA                            /CLEAR AC
1[illegible] 1105         TAD     K0200                  /SET AC 04=1
1[illegible] 6104         CLEA                           /TRY TO GENERATE "LOAD CNT"
1[illegible] 6107         CLCA                           /READ COUNTER
1[illegible] 3021         DCA     RXED                   /SAVE TEST VALUE
1[illegible] 1021         TAD     RXED                   /RESTORE IT
1[illegible] 7040         SZA CLA                        /ZERO?
1[illegible] 7402         HLT                            /LOAD CNT GATES FUNCTIONED WITH MODE 1=1 IN ERROR
1[illegible] 2022         ISZ     REGA                   /DO TEST 4096 TIMES
1[illegible] 5240         JMP     TST39

                /GLITCH TEST OF LOAD CNT GATES

1[illegible] 4056         TEST30, JMS     RANDOM         /GET RANDOM NUMBER
1201 6183                 CLAB                           /SEND IT TO BUFFER
1202 3020                 DCA     SEND                   /SAVE IT
1203 1105                 TAD     K0200                  /SET AC 04=1
1204 6102                 CLLR                           /SET MODE 1=1
1205 7200                 CLA                            /CLEAR AC
1206 1106                 TAD     K0300                  /SET AC 04,05=1
1207 6102                 CLLR                           /SET MODE 2=1
1210 7200                 CLA
1211 2022                 ISZ     REGA                   /DO THIS 4096 TIMES
1212 5203                 JMP     .-7
1213 6107                 CLCA                           /READ COUNTER
1214 3021                 DCA     RXED                   /SAVE IT
1215 1021                 TAD     RXED                   /RESTORE IT
1216 7040                 SZA CLA                        /ZERO?
1217 7402                 HLT                            /THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER
```

D8CA D-(D)


```
                /GENERAL GATE SHAKING TEST OF THE MODE FLIP FLOPS

1100  4055      TEST31, JMS     RANDOM          /GET RANDOM NUMBER
1101  6053              DCIB                    /SEND IT TO BUFFER
1102  3026              DCA     SEND            /SAVE IT
1103  1022              TAD     REGA            /GET TEST COUNTER
1104  7006              RTL                     /ROTATE TWO LEFT
1105  7006              RTL                     /ROTATE TWO LEFT
1106  7006              RTL                     /ROTATE TWO LEFT
1107  0227              AND     K2720           /INSURE THAT MODE 0,1,2=1
1110  6052              CLLR                    /SEND RANDOM NUMBER TO CONTROL REGISTER
1111  7040              CMA                     /COMPLEMENT
1112  0227              AND     K2702           /INSURE THAT MODE 0,1,2=1
1113  6052              CLLR                    /SET TO COMPLEMENT OF THE NUMBER
1114  2022              ISZ     REGA            /DO THIS 4096 TIMES
1115  5053              JMP     TEST31+3
1116  6056              CLBA                    /GET TEST VALUE FROM BUFFER
1117  3021              DCA     RXED            /SAVE IT
1120  1021              TAD     RXED            /RESTORE IT
1121  7041              CIA                     /COMPLEMENT
1122  1020              TAD     SEND            /SUBTRACT TEST NUMBER
1123  7540              SZA CLA                 /EQUAL?
1124  7402              HLT                     /BUFF CHANGED IN ERROR
1125  6157              CLCA                    /READ COUNTER
1126  3021              DCA     RXED            /SAVE IT
1127  1021              TAD     RXED            /RESTORE IT
1130  7540              SZA CLA                 /STILL ZERO?
1131  7402              HLT                     /COUNTER CHANGED IN ERROR
```

8CA-D-6)


```
                /DOES MODE 2 1-0 CLK CNT?

1132  4055      TEST32, JMS     RANDOM          /GET RANDOM NUMBER
1133  6133              CLAB                    /SEND IT TO BUFFER
1134  3020              DCA     SEND            /SAVE IT
1135  6132              CLLR                    /ZERO MODE 2
1136  1023              TAD     K0100           /AC 05=1
1137  6132              CLLR                    /GENERATE "CLR CNT"
1140  7200              CLA                     /CLEAR AC
1141  1025              TAD     K0200           /SET AC 04=1
1142  6134              CLEN                    /GENERATE "LOAD CNT"
1143  7200              CLA
1144  6132              CLLR                    /0 MODE 2
1145  6137              CLCA                    /READ COUNTER
1146  3021              DCA     RXED            /SAVE IT
1147  6133              CLAB                    /CLEAR BUF OR OVERFLOW WILL RELOAD CNT
1150  1021              TAD     RXED            /RESTORE IT
1151  7041              CIA                     /COMPLEMENT
1152  1020              TAD     SEND            /SUBTRACT TEST NUMBER
1153  7540              SZA CLA                 /EQUAL?
1154  7402              HLT                     /MODE 2 1-0 DID IT

1155  1023              TAD     K0100           /SET AC 05=1
1156  6132              CLLR                    /GENERATE "CLR CNT"
1157  6137              CLCA                    /READ COUNTER
1160  3021              DCA     RXED            /SAVE IT
1161  1021              TAD     RXED            /RESTORE IT
1162  7540              SZA CLA                 /ZERO?
1163  7402              HLT                     /MODE 2 0-1 FAILED
                /TEST 4: TEST OF SKIP OVERFLOW AND INTERRUPT
                /
                /DOES COUNTER OVERFLOW SET OVERFLOW FLOP
                /
1164  7000              NOP
1165  7000              NOP
1166  7000              NOP
1167  7200      TST40,  CLA CLL
1170  6132              CLLR                    /CLEAR STATUS
1171  1023              TAD     K0100           /SET AC 05=1
1172  6132              CLLR                    /0 TO COUNTER
1173  6135              CLSA                    /CLEAR CLOCK STATUS
1174  7320              CLA CLL CML RAR         /SET AC=4000
1175  6133              CLAB                    /SET BUFFER TO 4000
1176  7200              CLA CLL
1177  1025              TAD     K0200           /SET AC 04=1
1200  6134              CLEN                    /LOAD CNT (00)=1; 1 TO OVERFLOW
1201  7000              CLA CLL
1202  6133              CLAB
1203  6132              CLLR                    /CLEAR ALL MODES
1204  1023              TAD     K0100           /SET AC 05=1
1205  6132              CLLR                    /GEN "CLR CNT"
1206  6135              CLSA                    /GET STATUS OF CLOCK
1207  7700              SMA CLA
1210  7402              HLT                     /OVERFLOW NOT SET
```

```
1211  2022          ISZ     REG4        /DO TEST 4096 TIMES
1212  5014          JMP I   TST40X      /INDIRECT REF. TO TST40
1213  7410          SKP
1214  1207  TST40X, TST40                /DEF. OF TST40X
```

```
7000    NOP
        /DOES CLSA (6135) CLEAR OVERFLOW FLOP
        /
7300    TST41A, CLA CLL
6132            CLLR                    /CLEAR ALL MODES
1023            TAD     K0100           /GEN "CLR CNT"
6132            CLLR
6135            CLSA                    /CLEAR CLOCK STATUS
7330            CLA CLL CML RAR
6133            CLAB                    /SET BUF=4000 OCTAL
7300            CLA CLL
1025            TAD     K0200
6134            CLEN                    /GEN LOAD CNT
7300            CLA CLL
6133            CLAB                    /ZERO BUF.
6132            CLLR                    /CLEAR ALL MODES
1023            TAD     K0100           /SET AC 05=1
6132            CLLR                    /GEN "CLR CNT"
7300            CLA CLL
6135            CLSA                    /GET STATUS BIT 0=1
7300            CLA CLL
6135            CLSA                    /GET STATUS BIT 0=0
7710            SPA CLA
7402            HLT                     /CLSA FAILED TO CLEAR OVERFLOW FLOP

        /
        /TEST OVERFLOW SKIP
        /
7300            CLA CLL
6132            CLLR                    /CLEAR ALL MODES
1023            TAD     K0100           /SET AC 05=1
6132            CLLR                    /GEN "CLR CNT"
6135            CLSA                    /CLEAR CLOCK STATUS
7330            CLA CLL CML RAR
6133            CLAB                    /SET BUF=4000 OCTAL
7300            CLA CLL
1025            TAD     K0200
6134            CLEN                    /GEN LOAD CNT
7300            CLA CLL
6133            CLAB                    /CLR BUF.
6132            CLLR                    /CLEAR ALL MODES
1023            TAD     K0100           /AC 05=1
6132            CLLR                    /GEN "CLR CNT"
7300            CLA CLL
6131            CLSK
7410            SKP
7402            HLT                     /CLOCK PRESET DIDN'T 0 OVERFLOW ENABLE
```

```
                /TEST FOR NO INTERRUPT

1266  1210          TAD     PNTA
1267  3215          DCA     RETURN
1270  6001          ION
1271  7000          NOP
1272  6002          IOF
1273  7410          SKP
1274  7402    LOCA, HLT                   /ILLEGAL INTERRUPT OVERFLOW=1 OVERFLOW ENABLE=0

                /SET INT ENABLE

1275  1223          TAD     K0100
1276  6134          CLEN                  /TURN ON CLOCK OVERFLOW INT
1277  7300          CLA CLL
1300  6131          CLSK
1301  7402          HLT                   /CLSK FAILED TO SKIP OVERFLOW=1 EN OVF INT=1

                /
                /TEST FOR CLOCK INTERRUPT
                /
1302  1211          TAD     PNTB
1303  3215          DCA     RETURN
1304  6001          ION
1305  7000          NOP
1306  6002          IOF
1307  7402          HLT                   /CLOCK INT FAILED TO INTERRUPT
```

#19-055-47
7.50

```
                /TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE

1310  7200      LOCB,   CLA CLL
1311  6134              CLEN
1312  6131              CLSK
1313  7410              SKP
1314  7402              HLT                     /OVERFLOW ENABLE WON'T ZERO

                /TEST WITH FLAG ZERO OVERFLOW SET

1315  1223              TAD     K0100
1316  6134              CLEN
1317  7200              CLA CLL
1320  6132              CLLR                    /STOP THE CLOCK
1321  6135              CLSA                    /READ AND ZERO FLAG
1322  7200              CLA CLL
1323  6131              CLSK
1324  7410              SKP
1325  7402              HLT                     /BAD INTERRUPT CONDITION STILL EXIST'S

                /TEST INT OVERFLOW=0

1326  1112              TAD     PNTC
1327  3113              DCA     RETURN
1330  6001              ION
1331  7000              NOP
1332  6002              IOF
1333  7410              SKP
1334  7402      LOCC,   HLT                     /ILLEGAL CLOCK INTERRUPT
1335  2222              ISZ     REGA            /DO INTERRUPT TEST 4096 TIMES
1336  5555              JMP I   TST41B          /CROSS PAGE REF TO TST41A
```

```
                /
                /TEST4: COUNTER CARRY TESTING
                /COUNTER PRESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION

                /DOES BIT 11 SET UP

1337  7200          CLA
1340  6132          CLLR                    /CLEAR ALL MODES
1341  6133          CLAB                    /CLEAR BUF
1342  1223          TAD     K0100           /SET AC 05=1
1343  6132          CLLR                    /GEN "CLR CNT"
1344  6135          CLSA                    /CLEAR STATUS
1345  7223          CLA
1346  3022          DCA     REGA
1347  3023          DCA     SEND
1350  6133          CLAB
1351  1205          TAD     K0200           /MODE 1 100 H2 RATE
1352  6134          CLEN
1353  7300          CLA CLL
1354  1224          TAD     K5100
1355  6132          CLLR
1356  6137          CLCA                    /READ COUNTER
1357  3021          DCA     RXED
1360  1021          TAD     RXED
1361  1025          TAD     M0001
1362  7650          SNA CLA
1363  5367          JMP     .+4
1364  2022          ISZ     REGA
1365  5356          JMP     .-7             /WAIT SOME MORE
1366  7402          HLT                     /BIT 11 FAILED TO GET SET BY A CLOCK PULSE

                /DOES BIT 10 SET UP

1367  7200          CLA
1370  6132          CLLR
1371  6133          CLAB
1372  1223          TAD     K0100
1373  6132          CLLR
1374  6135  TST41,  CLSA
1375  7200          CLA
1376  3022          DCA     REGA
1377  1026          TAD     K0001
1400  6133          CLAB
1401  3020          DCA     SEND
1402  1205          TAD     K0200
1403  6134          CLEN
1404  7300          CLA CLL
1405  1224          TAD     K5100
1406  6132          CLLR
1407  6137          CLCA
1410  3021          DCA     RXED
1411  1021          TAD     RXED
1412  1027          TAD     M0002
1413  7650          SNA CLA
1414  5220          JMP     .+4
```

```
1415  2022        ISZ     HEGA
1416  5200 /      JMP     .-/
```

```
1447  7402          HLT                 /BIT 10 FAILED TO GET SET BY COUNTING

                /DOES BIT 9 SET UP

1450  7402          HLT
1451  6132          CLLR
1452  6133          CLAB
1453  1023          TAD     K0100
1454  6132          CLLR
1455  6135    TST42,  CLSA
1456  7240          CLA
1457  3422          DCA     REGA
1460  1032          TAD     K0003
1461  6133          CLAB
1462  3420          DCA     SEND
1463  1025          TAD     K0200
1464  6134          CLEN
1465  7300          CLA CLL
1466  1024          TAD     K5100
1467  6132          CLLR
1470  6137          CLCA
1471  3421          DCA     RXED
1472  1421          TAD     RXED
1473  1031          TAD     M0004
1474  7650          SNA CLA
1475  5251          JMP     .+4
1476  2422          ISZ     REGA
1477  5240          JMP     .-7
1450  7402          HLT                 /BIT 9 FAILED TO GET SET BY COUNTING

                /DOES BIT 8 SET UP

1451  7402          HLT
1452  6132          CLLR
1453  6133          CLAB
1454  1023          TAD     K0100
1455  6132          CLLR
1456  6135    TST43,  CLSA
1457  7240          CLA
1458  3422          DCA     REGA
1459  1032          TAD     K0007
1460  6133          CLAB
1461  3420          DCA     SEND*
1462  1025          TAD     K0200
1463  6134          CLEN
1464  7300          CLA CLL
1465  1024          TAD     K5100
1466  6132          CLLR
1467  6137          CLCA
1470  3421          DCA     RXED
1471  1421          TAD     RXED
1472  1044          TAD     M0010
1473  7650          SNA CLA
1474  5242          JMP     .+4
```

```
[illegible]  [illegible] 22      ISZ     REGA
[illegible]  [illegible]/1       JMP     .-7
[illegible]  [illegible]-62      HLT                     /BIT 8 FAILED TO GET SET BY COUNTING
```

```
                /DOES BIT 7 SET UP

1512  7200              CLA
1513  6132              CLLR
1514  6133              CLAB
1515  1023              TAD     K0100
1516  6132              CLLR
1517  6135    TST44,    CLSA
1510  7200              CLA
1511  3022              DCA     REGA
1512  1033              TAD     K0017
1513  6133              CLAB
1514  3020              DCA     SEND
1515  1105              TAD     K0200
1516  6134              CLEN
1517  7200              CLA CLL
1520  1024              TAD     K5100
1521  6132              CLLR
1522  6137              CLCA
1523  3021              DCA     RXED
1524  1021              TAD     RXED
1525  1045              TAD     M0020
1526  7550              SNA CLA
1527  5533              JMP     .+4
1530  2022              ISZ     REGA
1531  5522              JMP     .-7
1532  7402              HLT                     /BIT 7 FAILED TO GET SET BY COUNTING

                /DOES BIT 6 SET UP

1533  7200              CLA
1534  6132              CLLR
1535  6133              CLAB
1536  1023              TAD     K0100
1537  6132              CLLR
1540  6135    TST45,    CLSA
1541  7200              CLA
1542  3022              DCA     REGA
1543  1034              TAD     K0037
1544  6133              CLAB
1545  3020              DCA     SEND
1546  1105              TAD     K0200
1547  6134              CLEN
1550  7200              CLA CLL
1551  1024              TAD     K5100
1552  6132              CLLR
1553  6137              CLCA
1554  3021              DCA     RXED
1555  1021              TAD     RXED
1556  1046              TAD     M0040
1557  7550              SNA CLA
1560  5564              JMP     .+4
1561  2022              ISZ     REGA
1562  5553              JMP     .-7
```

1505 /MAR2 HLT /BIT 6 FAILED TO GET SET BY COUNTING

```
                /DOES BIT 5 SET UP

1564  7200              CLA
1565  6132              CLLR
1566  6133              CLAB
1567  1023              TAD     K2100
1570  6132              CLLR
1571  6135      TST46,  CLSA
1572  7200              CLA
1573  3022              DCA     REGA
1574  1035              TAD     K2277
1575  6133              CLAB
1576  3020              DCA     SEND
1577  1040              TAD     K0220
1600  6134              CLEN
1601  7300              CLA CLL
1602  1024              TAD     K5100
1603  6132              CLLR
1604  6137              CLCA
1605  3021              DCA     RXED
1606  1021              TAD     RXED
1607  1047              TAD     M0100
1610  7050              SNA CLA
1611  5215              JMP     .+4
1612  2022              ISZ     REGA
1613  5204              JMP     .-7
1614  7402              HLT                     /BIT 5 FAILED TO GET SET BY COUNTING

                /DOES BIT 4 SET UP

1615  7200              CLA
1616  6132              CLLR
1617  6133              CLAB
1620  1023              TAD     K2100
1621  6132              CLLR
1622  6135      TST47,  CLSA
1623  7200              CLA
1624  3022              DCA     REGA
1625  1036              TAD     K0177
1626  6133              CLAB
1627  3020              DCA     SEND
1630  1040              TAD     K0220
1631  6134              CLEN
1632  7300              CLA CLL
1633  1024              TAD     K5100
1634  6132              CLLR
1635  6137              CLCA
1636  3021              DCA     RXED
1637  1021              TAD     RXED
1640  1050              TAD     M0200
1641  7050              SNA CLA
1642  5246              JMP     .+4
1643  2022              ISZ     REGA
1644  5235              JMP     .-7
```

1600 7402 HLT /BIT 4 FAILED TO GET SET BY COUNTING

```
                /DOES BIT 3 SET UP

1[illegible]  7[illegible]          CLA
1[illegible]  6[illegible]          CLLR
1[illegible]  6[illegible]          CLAB
1[illegible]  1[illegible]          TAD     K0100
1[illegible]  6[illegible]          CLLR
1[illegible]  6[illegible]  TST48,  CLSA
1[illegible]  7[illegible]          CLA
1[illegible]  3[illegible]          DCA     REGA
1[illegible]  1[illegible]          TAD     K0377
1[illegible]  6[illegible]          CLAB
1[illegible]  3[illegible]          DCA     SEND

1[illegible]  1[illegible]          TAD     K0200
1[illegible]  6[illegible]          CLEN
1[illegible]  7[illegible]          CLA CLL
1[illegible]  1[illegible]          TAD     K5100
1[illegible]  6[illegible]          CLLR
1[illegible]  6[illegible]          CLCA
1[illegible]  3021                  DCA     RXED
1[illegible]  1021                  TAD     RXED
1[illegible]  1[illegible]          TAD     M0400
1[illegible]  7652                  SNA CLA
1[illegible]  5[illegible]          JMP     .+4
1[illegible]  2022                  ISZ     REGA
1[illegible]  5[illegible]          JMP     .-7
1[illegible]  7402                  HLT                     /BIT 3 FAILED TO GET SET BY COUNTING

                /DOES BIT 2 SET UP

1[illegible]  7[illegible]          CLA
1[illegible]  6[illegible]          CLLR
1[illegible]  6[illegible]          CLAB
1[illegible]  1[illegible]          TAD     K0100
1[illegible]  6[illegible]          CLLR
1[illegible]  6[illegible]  TST49,  CLSA
1[illegible]  7[illegible]          CLA
1[illegible]  3022                  DCA     REGA
1[illegible]  1040                  TAD     K0777
1[illegible]  6[illegible]          CLAB
1711  3020                          DCA     SEND
1712  1[illegible]                  TAD     K0200
1713  6[illegible]                  CLEN
1714  7[illegible]                  CLA CLL
1715  1024                          TAD     K5100
1716  6[illegible]                  CLLR
1717  6[illegible]                  CLCA
1[illegible]  3[illegible]          DCA     RXED
1[illegible]  1[illegible]          TAD     RXED
1722  1[illegible]                  TAD     M1000
1723  7652                          SNA CLA
1724  5241                          JMP I   TST49X          /CROSS TO TST49A
1725  2022                          ISZ     REGA            /BACK TO TST49+13
```

```
17765  5344    JMP I   TST49Y
17767  7402    HLT                 /BIT 2 FAILED TO GET SET BY COUNTING
```

```
                /DOES BIT 1 SET UP

1750  7200              CLA
1751  6131              CLLR
1752  6133              CLAB
1753  1026              TAD     K0126
1754  6132              CLLR
1755  6135      TST49A, CLSA
1756  7200              CLA
1757  3022              DCA     REGA
1760  1042              TAD     K1777
1761  6133              CLAB
1762  3024              DCA     SEND
1763  1025              TAD     K0200
1764  6134              CLEN
1765  7322              CLA CLL
1766  1024              TAD     K5100
1767  6132              CLLR
1770  6137              CLCA
1771  3021              DCA     RXED
1772  1021              TAD     RXED
1773  1023              TAD     M2000
1774  7650              SNA CLA
1775  5201              JMP     .+4
1776  2022              ISZ     REGA
1777  5375              JMP     .-7
1778  7402              HLT                     /BIT 1 FAILED TO GET SET BY COUNTING

                /DOES BIT 0 SET UP

1781  7200              CLA
1782  6132              CLLR
1783  6133              CLAB
1784  1023              TAD     K0100
1785  6132              CLLR
1786  6135      TST49B, CLSA
1787  7200              CLA
1770  3022              DCA     REGA
1771  1042              TAD     K3777
1772  6133              CLAB
1773  3024              DCA     SEND
1774  1025              TAD     K0200
1775  6134              CLEN
1776  7322              CLA CLL
1777  1024              TAD     K5100
2000  6132              CLLR
2001  6137              CLCA
2002  3021              DCA     RXED
2003  1021              TAD     RXED
2004  1023              TAD     M4000
2005  7650              SNA CLA
2006  5212              JMP     .+4
2007  2022              ISZ     REGA
2010  5221              JMP     .-7
```

2.22. 75.2 HLT /BIT 0 FAILED TO GET SET BY COUNTING

```
                    /TEST5: DOES COUNTER COUNT NORMALLY AND AT ALL RATES
                    /
                    /AND ALL COUNT RATES FUNCTIONS

2012  1214          TAD     K1400
2013  6132          CLLR                        /SET 400KC RATE
2014  7300          CLA CLL
2015  6135          CLSA                        /READ STATUS
2016  7700          SMA CLA
2017  5215          JMP     .-2                 /WAIT FOR OVERFLOW

2020  1216          TAD     K2000
2021  6132          CLLR
2022  7300          CLA CLL                     /SET 100KC RATE
2023  6135          CLSA
2024  7700          SMA CLA
2025  5223          JMP     .-2                 /WAIT FOR OVERFLOW

2026  1217          TAD     K3200
2027  6132          CLLR                        /SET 10KC RATE
2030  7300          CLA CLL
2031  6135          CLSA
2032  7700          SMA CLA
2033  5231          JMP     .-2

2034  1220          TAD     K7700               /PRESET THE CLOCK
2035  6203          CLAB                        /FOR 100 CPS TEST
2036  7200          CLA
2037  1221          TAD     K4100               /SET 1KC RATE
2040  6132          CLLR
2041  7300          CLA CLL
2042  6135          CLSA
2043  7700          SMA CLA
2044  5242          JMP     .-2

2045  1224          TAD     K5100               /SET 100 CPS RATES
2046  6132          CLLR
2047  7300          CLA CLL
2050  6135          CLSA
2051  7700          SMA CLA
2052  5250          JMP     .-2

2053  7300          CLA CLL
2054  1224          TAD     K0020               /SET AC 07=1
2055  6134          CLEN                        /ENABLE INPUT CHAN1
2056  7200          CLA
2057  1147          TAD     K6000               /SET INPUT RATE CHAN1=60HZ
2060  6132          CLLR
2061  7300          CLA CLL
2062  6135          CLSA
2063  7700          SMA CLA
2064  5262          JMP     .-2
```

```
                /
                / TEST INPUT CHANNEL INTERRUPT CHAN 1
                /
2265  1236      ITST1,  TAD     PNTD
2266  3213              DCA     RETURN          /SET UP INTERRUPT RETURN
2267  1223              TAD     K0060           /ENABLE INPUT AND INTERRUPT
2270  6134              CLEV
2271  6232              CLLR                    /SIMULATE INPUT CHANNEL ONE
2272  6001              IOF
2273  7000              NOP                     /WAIT
2274  7402              HLT                     /NO INTERRUPT ERROR

2275  6134      LOCD,   AND     K0020           /CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2276  6134              CLEV
2277  7000              CLA CLL
2100  1234              TAD     PNTE
2101  3213              DCA     RETURN
2102  6001              IOF
2103  6235              CLSA                    /CLEAR CLOCK STATUS
2104  7610              SKP CLA
2105  7402      LOCE,   HLT                     /INTERRUPT IN ERROR
```

```
                /
                /SIMULATED INPUT TESTS CHANNEL 3
                /
2115  1223      I PTL1, TAD     K0001
2116  6134              CLEN
2117  6132              CLLR                    /SET ERCNT FLOP
2118  7000              NOP
2119  7000              NOP
2120  7000              NOP
2121  7000              NOP
2122  6132              CLLR                    /SET PREVENT FLOP
2123  7200              CLA
2124  7120              CLL
2125  7000              NOP
2126  6134              CLEN                    /CLEAR ENABLES
2127  6135              CLSA
2130  3022              DCA     SEND
2131  6135              CLSA
2132  [illegible]       AND     K0003
2133  3021              DCA     RXED
2134  1621              TAD     RXED
2135  7640              SZA CLA
2136  7402              HLT                     /CLSA DOESN'T Ø INPUT CHANNEL

2137  1022              TAD     SEND
2140  7041              CIA
2141  1003              TAD     K0003           /SUBTRACT SET
2142  7440              SZA CLA
2143  7402              HLT                     /BOTH PRE-EVENT  AND EVENT NOT SET
2144  2022              ISZ     REGA
2145  5237              JMP I   INT01           /INDIRECT REF TO INPT01

                /
                /TEST INPUT CHANNEL INTERRUPT CHAN 2
                /
2146  1235      TEST02, TAD     PNTF
2147  3213              DCA     RETURN          /SET UP INTERRUPT RETURN
2150  1201              TAD     K0214
2151  6134              CLEN
2152  6132              CLLR
2153  6001              ION
2154  7000              NOP                     /WAIT
2155  7402              HLT                     /NO INTERRUPT

2156  0202      LOOF,   AND     K0004           /CLEAR INTERRUPT ENABLE
2157  6134              CLEN
2160  7300              CLA CLL
2161  1235              TAD     PNTG
2162  3213              DCA     RETURN
2163  6001              ION
2164  6135              CLSA                    /CLEAR CLOCK STATUS
2165  7010              SKP CLA
2166  7402      LOOG,   HLT                     /INTERRUPT IN ERROR
                                                /CLEA EN EV 2 INT BAD
```

```
                        /
                        /TEST INPUT CHANNEL INTERRUPT CHAN 3
                        /
2152  1150              ITST3,  TAD     PNTI
2153  3113                      DCA     RETURN          /SET UP INTERRUPT RETURN
2154  1030                      TAD     K0003
2155  6134                      CLEN
2156  6132                      CLLR
2157  6401                      ION
2160  7403                      NOP                     /WAIT
2161  7402                      HLT                     /NO INTERRUPT

2162  6426              LOCH,   AND     K0001           /CLEAR INTERRUPT ENABLE
2163  6134                      CLEN
2164  7300                      CLA CLL
2165  1140                      TAD     PNTI
2166  3113                      DCA     RETURN
2167  6401                      ION
2170  6135                      CLSA                    /CLEAR CLOCK STATUS

2171  7610                      SKP CLA
2172  7402              LOCI,   HLT                     /INTERRUPT IN ERROR
```

```
                /
                /SIM INPUT TESTS CHAN 2
                /
2220  7000      NOP
2221  7000      NOP
2222  7000      NOP
2223  6002      IOF                     /INT OFF
2224  7000      NOP
2225  7000      NOP
2226  7000      NOP
2227  7000      NOP
2230  7000      NOP
2231  7000      NOP
2232  7000      NOP
2233  7000      NOP
2234  7000      NOP
2235  7000      NOP
2236  7000      NOP
2237  7000      NOP
2240  7000      NOP
2241  7000      NOP
2242  1100  INPT22, TAD    K0004
2243  6104      CLEN                    /ENABLE CHAN 2
2244  6102      CLLR                    /SET EVENT FLOP
2245  7000      NOP
2246  7000      NOP
2247  7000      NOP
2250  7000      NOP
2251  6102      CLLR                    /SET PREVENT FLOP
2252  7200      CLA
2253  7100      CLL
2254  7000      NOP
2255  6134      CLEN
2256  6135      CLSA
2257  3026      DCA    SEND
2260  6135      CLSA
2261  0131      AND    K0014
2262  3027      DCA    RXED
2263  1027      TAD    RXED
2264  7640      SZA CLA
2265  7402      HLT                     /CLSA DOESN'T 0 INPUT CHANNEL

2266  1026      TAD    SEND
2267  7041      CIA
2270  1131      TAD    K0014            /SUBTRACT SET
2271  7540      SZA CLA
2272  7402      HLT                     /BOTH PRE-EVENT AND EVENT NOT SET
2273  2022      ISZ    REGA
2274  5222      JMP    INPT02
```

```
                /
                /SIM INPUT TESTS CHAN 1
                /
2250  1124      INPT03, TAD     K0024
2251  6134              CLEN
2252  6132              CLLR                    /SET EVENT FLOP
2253  7000              NOP
2254  7000              NOP
2255  7000              NOP
2256  7000              NOP
2257  6132              CLLR                    /SET PREVENT FLOP
2260  7200              CLA
2261  7100              CLL
2262  7000              NOP
2263  6134              CLEN
2264  6135              CLSA
2265  3020              DCA     SEND
2266  6135              CLSA
2267  0123              AND     K0060
2270  3021              DCA     RXED
2271  1021              TAD     RXED
2272  7640              SZA CLA
2273  7402              HLT                     /CLSA DOESN'T 0 INPUT CHANNEL

2274  1020              TAD     SEND
2275  7041              CIA
2276  1123              TAD     K0060           /SUBTRACT SET
2277  7640              SZA CLA
2300  7402              HLT                     /BOTH PRE-EVENT AND EVENT NOT SET
2301  7000              NOP
2302  7000              NOP
2303  7000              NOP
2304  2022              ISZ     REGA            /DO TEST 4096 TIMES
2305  5714              JMP I   .+2             /INDIRECT REF. TO INPT03
2306  7410              SKP
2307  2255              INPT03
```

```
                /TEST OF INPUT CHANNEL #3
                /KNOBS OF CHAN1,CHAN2,CHAN3 SET TO LINEFREQ

2315  6135      INPT04, CLSA                        /CLEAR STATUS
2316  7200              CLA CLL
2317  6132              CLLR                        /CLEAR ALL MODES
2320  1143              TAD     K0003
2321  6134              CLEN                        /ENABLE CHAN3 INPUT AND INTER.
2322  7200              CLA
2323  6131              CLSK                        /SKIP ON CLOCK INTER.
2324  5322              JMP     .-2                 /WAIT
2325  6135              CLSA                        /GER CLOCK STATUS
2326  3021              DCA     RXED                /SAVE IT
2327  1021              TAD     RXED                /RESTORE IT
2330  7041              CIA
2331  1150              TAD     K0002
2332  7040              SZA CLA
2333  7402              HLT                         /INTERRUPT BUT CHAN 1
                                                    /EVENT HOP NOT SET
                /TEST OF INPUT CHANNEL 2

2334  6135              CLSA                        /CLEAR STATUS
2335  7200              CLA CLL
2336  6132              CLLR                        /ZERO ALL MODES
2337  1131              TAD     K0014               /ENAB. CHAN. 2 INPUT AND
                                                    /INTERRUPT FLOPS

2340  6134              CLEN
2341  7200              CLA
2342  6131              CLSK                        /CHECK FOR CLOCK INTER.
2343  5341              JMP     .-2                 /WAIT
2344  6135              CLSA                        /GET STATUS
2345  3021              DCA     RXED                /SAVE IT
2346  1021              TAD     RXED                /RESTORE IT
2347  7041              CIA
2350  1143              TAD     K0010
2351  7040              SZA CLA
2352  7402              HLT                         /INTERRUPT BUT CHAN 2
                                                    /EVENT FLOP NOT SET

                /TEST OF INPUT CHAN 1
2353  6135              CLSA                        /CLEAR STATUS
2354  7200              CLA CLL
2355  6132              CLLR                        /CLEAR ALL MODES
2356  1123              TAD     K0060               /ENAB. CHAN1 INPUT
2357  6134              CLEN                        /AND INTER.
2360  7200              CLA
2361  6131              CLSK                        /CHECK FOR CLOCK INTER.
2362  5362              JMP     .-2                 /WAIT
2363  6135              CLSA                        /GET CLOCK STATUS
2364  3021              DCA     RXED                /SAVE IT
2365  1021              TAD     RXED                /RESTORE IT
2366  7041              CIA
2367  1144              TAD     K0040
2370  7040              SZA CLA
```

```
2771  7402        HLT                    /INTER. BUT CHAN 1 EVENT
                                         /FLOP NOT SET

2772  1277        TAD    X2440
2773  1022        TAD    REGA
2774  3022        DCA    REGA
2775  1022        TAD    REGA
2776  7440        SZA CLA                /DO TEST 128 TIMES
2777  5231        JMP I  IPT04           /INDIRECT REF. TO IPT04
```

```
                /TEST OF SAMPLE MODE
        6141    LINC=6141                                   /START LINC MODE
        0011    CLR=0011                                    /CLEAR AC AND LINC
        7004    ESF=7004                                    /ENAB SPEC. IN REG.
        0100    SAM0=0100                                   /READ KNOB 0
        0101    SAM1=0101                                   /READ KNOB 1
        1040    STA=1040                                    /STORE AC
        1020    LDAI=1020                                   /LOAD AC
        0002    PDP=0002                                    /ENTER PDP-8 MODE
2400    7004            CSR                                 /IF RIGHT SW BIT 2(1)
2401    7006            STL                                 /SKIP FAST SAM TEST
2402    7010            SPA
2403    5025            JMP I   ,+2                         /INDIRECT REF TO TCNT1
2404    7410            SKP
2405    2035            TCNT1
2406    6141    TSM,    LINC                                /ENTER LINC MODE
2407    0011            CLR
2410    7004            ESF                                 /CLEAR SPEC. IN REG.
2411    0100            SAM0                                /READ KNOB ZERO
2412    0002            PDP
2413    3020            DCA     SEND
2414    6141            LINC
2415    0101            SAM1                                /READ KNOB 1
2416    0011            CLR                                 /CLEAR AC
2417    1020            LDAI
2420    0100            0100
2421    7004            ESF                                 /ENABLE FAST SAM
2422    0002            PDP                                 /ENTER PDP-8 MODE
2423    6135            CLSA                                /CLEAR CLOCK STATUS
2424    7300            CLA CLL
2425    1140            TAD     K0400                       /SET MODE DIT0=1
2426    6132            CLLR
2427    7300            CLA CLL
2430    6141            LINC                                /ENTER LINC MODE
2431    0100            SAM0                                /FAST SAM SET THEREFORE
                                                            /READ IN VALUE OF KNOB1
                                                            /AS THIS WAS LAST CONVER
                                                            /SION
2432    0100            SAM0                                /SHOULD STILL READ KNOB1
2433    0002            PDP                                 /ENTER PDP-8 MODE
2434    3021            DCA     RXED                        /SAVE VALUE
2435    1021            TAD     RXED                        /RESTORE IT
2436    7041            CIA
2437    1020            TAD     SEND                        /COMPARE IT
2440    7040            SZA CLA
2441    7410            SKP
2442    7402            HLT                                 /READING FAST SAM
                                                            /INITIATED CONVERSION
                                                            /IN ERROR
2443    1140            TAD     K0400
2444    6132            CLLR                                /MODE 2(1),0(1)
```

```
2445  7300   CLA     CLL CML RAR
2446  6133           CLAB                          /SET BUFF=4000
2447  7200           CLA
2450  1135           TAD     K0200
2451  6134           CLEN                          /LOAD CTN FROM BUF
2452  7200           CLA
2453  6133           CLAB                          /CLR BUF
2454  7200           CLA
2455  6132           CLLR                          /CLEAR ALL MODES
2456  1140           TAD     K0500
2457  6132           CLLR                          /SET OVERFLOW MODE 0(1)
2460  6141           LINC                          /ENTER LINC MODE
2461  0400           SAM2                          /SAMPLE KNOB 0
2462  0002           PDP                           /ENTER PDP-8 MODE
2463  3021           DCA     RXED                  /STORE
2464  1021           TAD     RXED                  /RESTORE
2465  7041           CIA
2466  1020           TAD     SEND
2467  7040           SZA CLA
2470  7402           HLT                           /CONVERSION NOT INITIATED BY OVFLO
2471  2022           ISZ     REGA                  /DO TEST 4096 TIMES
2472  5552           JMP I   TSMA                  /CROSS PAGE REF TO TSM
                /CHECK THAT MODE 2(2),1(1),2(1) DO NOT AFFECT
                /SAM

2473  7200     TSM1,  CLA
2474  6132           CLLR                          /ZERO ALL MODES
2475  1136           TAD     K0300
2476  6132           CLLR                          /MODE 1(1),2(1),0(0)
2477  6141           LINC                          /ENTER LINC MODE
2500  0011           CLR
2501  0004           ESF                           /ZERO SPEC. IN. REG.
2502  0100           SAM0                          /SAMPLE KNOB 0
2503  0002           PDP
2504  3020           DCA     SEND
2505  6141           LINC
2506  0101           SAM1                          /SAMPLE KNOB 1
2507  1020           LOAI
2510  0100           0100
2511  0004           ESF                           /SET FAST SAM FLOP
2512  0100           SAM0                          /GET KNOB 1 SETTING
2513  0002           PDP                           /ENTER PDP MODE
2514  3021           DCA     RXED                  /STORE
2515  1021           TAD     RXED                  /RECEIVE
2516  7041           CIA
2517  1020           TAD     SEND                  /COMPARE
2520  7040           SZA CLA
2521  7410           SKP
2522  7402           HLT                           /FAST SAM NOT SET
2523  6141           LINC                          /ENTER LINC MODE
2524  0100           SAM0                          /READ KNOB 0
2525  0002           PDP                           /ENTER PDP MODE
2526  3021           DCA     RXED                  /STORE
2527  1021           TAD     RXED                  /RESTORE
```

```
2500  7[illegible]   CLA
2501  1[illegible]   TAD    SEND          /COMPARE
2502  7[illegible]   SPA CLA
2503  7[illegible]   HLT                  /MODE 2(1),1(1) INHIBIT FAST SAM
2504  2[illegible]   ISZ    [illegible]   /DO TEST 4096 TIMES
2505  5[illegible]   JMP I  TSM1A         /INDIRECT REF TO TSM1
```

```
                /DOES TO PRESET CLEAR OVFLO, ENABLES, RATES AND MODES
                /PROGRAMED IO PRESET USED
                /IS COUNTER WORKING
2500  7200      TCNTI,  CLA                          /CLEAR AC
2501  6200              CLLR                         /CLEAR ALL MODES
2502  6000              CLEN                         /CLEAR ALL ENABLES
2503  1147              TAD     K6000
2504  6142              CLLR                         /SET RATE=10KHZ
2505  6137              CLCA                         /READ COUNTER
2506  3020              DCA     SEND                 /STORE
2507  1147              TAD     K6000
2510  7041              IAC
2511  7440              SZA
2512  5346              JMP     .-2                  /WAIT LOOP 4,92 MSEC
2513  6137              CLCA                         /READ COUNTER AGAIN
2514  7041              CIA
2515  1020              TAD     SEND                 /COMPARE
2516  7040              SZA CLA
2517  7410              SKP
2520  7402              HLT                          /COUNTER NOT WORKING
                                                     /WITH RATE BITS 1+2 SET
                /NOW DO IO PRESET CHECK IF RATE BITS 1,2 CLEAR
2521  6141              LINC                         /ENTER LINC MODE
2522  1022              LDAI
2523  0020              0020
2524  0004              ESF                          /DO IO PRESET
2525  0002              PDP                          /ENTER PDP MODE
2526  6137              CLCA                         /GET COUNTER
2527  3020              DCA     SEND                 /STORE
2530  1147              TAD     K6000
2531  7002              NOP
2532  7000              NOP
2533  7000              NOP
2534  7041              IAC
2535  7440              SZA
2536  5372              JMP     .-2                  /WAIT LOOP 4,92 MSEC
2537  6137              CLCA                         /READ COUNTER AGAIN
2540  7041              CIA
2541  1022              TAD     SEND                 /COMPARE
2542  7040              SZA CLA
2543  7402              HLT                          /IO PRESET FAILED TO
                                                     /CLEAR RATE BITS 1,2
2544  6132              CLLR                         /CLEAR ALL MODES
```

```
                /NOW CHECK RATE BIT 0
                /FIRST SEE IF COUNTER WORKS AT 1KHZ RATE
2608  7200          CLA                          /CLEAR AC
2609  6132          CLLR                         /CLEAR ALL MODES
2610  6134          CLEN                         /CLEAR ENABLES
2611  1023          TAD     K4000
2612  6132          CLLR                         /SET RATE=1KHZ
2613  6137          CLCA                         /READ COUNTER
2614  3020          DCA     SEND
2615  7000          NOP
2616  7001          IAC
2617  7440          SZA
2618  5213          JMP     .-2                  /WAIT LOOP 16 MSEC
2619  6137          CLCA                         /READ COUNTER
2620  7041          CIA
2621  1020          TAD     SEND                 /COMPARE
2622  7440          SZA
2623  7410          SKP
2624  7402          HLT                          /COUNTER NOT WORKING
                                                 /WITH RATE BIT 0 SET
                /NOW DO IO PRESET AND SEE IF BIT 1 CLEARED
2625  6141          LINC                         /ENTER LINC MODE
2626  1020          LDAI
2627  0000          0000
2630  0004          ESF                          /DO IO PRESET
2631  6002          PDP                          /ENTER PDP MODE
2632  6137          CLCA                         /READ COUNTER
2633  3020          DCA     SEND                 /STORE
2634  7000          NOP
2635  7001          IAC
2636  7440          SZA
2637  5234          JMP     .-2                  /WAIT 16 MSEC
2640  6137          CLCA                         /READ COUNTER AGAIN
2641  7041          CIA
2642  1020          TAD     SEND                 /COMPARE
2643  7540          SZA CLA
2644  7402          HLT                          /RATE BIT 0 SET AFTER IO
                                                 /PRESET
                /DOES OVERFLOW AND OVFLO INT. FLOP
                /CLEAR WITH IO PRESET
2645  7200    TCNT2,  CLA                        /CLEAR AC
2646  6132          CLLR                         /CLEAR ALL MODES
2647  1023          TAD     K0100
2650  6132          CLLR                         /SET MODE 2(1)
2651  6135          CLSA                         /CLEAR STATUS
2652  7200          CLA
2653  1025          TAD     K4000
2654  6133          CLAB                         /SET BUF TO 4000
2655  7200          CLA
2656  1023          TAD     K0200
2657  6134          CLEN                         /LOAD COUNTER
2660  7200          CLA
2661  6133          CLAB                         /ZERO BUF
2662  6132          CLLR                         /CLEAR ALL MODES
```

```
2652  1723        TAD     K0100
2653  6132        CLLR                        /GEN "CLR CNT"
2654  6131        LINC                        /ENTER LINC MODE
2655  2222        LDAI
2656  0020        0020
2657  6139        ESF                         /SO IO PRESET
2670  2002        PDP                         /ENTER PDP MODE
2671  6135        CLSA                        /GET STATUS
```

```
2672  7200          SMA CLA
2673  7410          SKP
2674  7402          HLT                          /OVFLO STILL SET AFTER IO
                                                 /PRESET
            /TEST OVFLO INT ENABLE
2675  7200          CLA                          /CLEAR AC
2676  1023          TAD     K0100
2677  6132          CLLR                         /SET MODE 2(1)
2700  6135          CLSA                         /CLEAR STATUS
2701  7200          CLA
2702  1055          TAD     K4000
2703  6133          CLAB                         /SET BUF PRESET REG.
2704  7200          CLA
2705  1025          TAD     K0200
2706  6134          CLEN                         /LOAD CNT WITH 4000
2707  7200          CLA
2710  1023          TAD     K0100
2711  6134          CLEN                         /SET INT.
2712  6141          LINC                         /ENTER LINE MODE
2713  1020          LDAI
2714  0020          0020
2715  6004          ESF                          /DO IO PRESET
2716  6002          PDP                          /ENTER PDP MODE
2717  7200          CLA
2720  6132          CLLR                         /CLEAR ALL MODES
2721  1023          TAD     K0100
2722  6132          CLLR                         /GEN.
2723  6131          CLSK
2724  7410          SKP
2725  7402          HLT                          /OVFLO INTER.
                                                 /SET AFTER IO PRESET
            /DOES IO PRESET CLEAR INPUT ENABLE FLOPS
2726  7200          CLA
2727  6132          CLLR                         /CLEAR ALL MODES
2730  1035          TAD     K0077
2731  6134          CLEN                         /ENABLE INPUTS TO ALL CHAN
2732  6135          CLSA                         /CLEAR STATUS
2733  6141          LINC                         /ENTER LINE MODE
2734  1020          LDAI
2735  0020          0020
2736  6004          ESF                          /DO IO PRESET
2737  6002          PDP                          /ENTER PDP MODE
2740  7200          CLA
2741  1035          TAD     K0077
2742  6132          CLLR                         /SIMULATE INPUTS ON ALL CHAN
```

```
2743  7200          NOP
2744  7200          NOP
2745  7200          NOP
2746  7200          NOP
2747  7200          NOP
2750  7200          NOP
2751  6132          CLLR                          /SIM INPUTS ON ALL CHAN
2752  7200          NOP
2753  7200          NOP
2754  7200          NOP
2755  7200          NOP
2756  7200          NOP
2757  7200          NOP
2760  7200          CLA
2761  6135          CLSA                          /GET STATUS
2762  7440          SZA
2763  7402          HLT                           /STATUS NOT ZERO
                                                  /IO PRESET FAILED TO CLEAR
                                                  /ENABLES=AC CONTAINS STATUS
2764  7200          CLA                           /CLEAR AC
                /DOES IO PRESET CLEAR MODE 2
2765  6133          CLAB
2766  6132          CLLR                          /CLEAR MODES
2767  1023          TAD     K0100
2770  6132          CLLR                          /SET MODE 2(1) - CLR CNT
2771  6141          LINC                          /ENTER LINC MODE
2772  1020          LDAI
2773  0020          0020
2774  0004          ESF                           /DO IO PRESET
2775  0002          PDP                           /ENTER PDP MODE
2776  7200          CLA
2777  1150          TAD     K5555
3000  6133          CLAB                          /LOAD BUF WITH 5555
3001  7200          CLA
3002  1165          TAD     K0200
3003  6134          CLEN                          /GEN LOAD CNT
3004  6137          CLCA                          /LOAD CNT TO AC
3005  7710          SPA CLA
3006  7402          HLT                           /MODE 2 NOT CLEARED
                                                  /BY IO PRESET
                /DOES IO PRESET CLEAR MODE 0
3007  7424          OSR                           /IF RIGHT SW BIT 2(1)
3010  7006          RTL                           /SKIP FAST SAM TEST
3011  7510          SPA
3012  5254          JMP     INDEX
3013  7200          CLA
3014  6132          CLLR                          /CLEAR ALL MODES
3015  6141          LINC                          /ENTER LINC MODE
3016  0100          SAM0                          /READ KNOB 0
3017  0002          PDP
3020  3020          DCA     SEND
3021  6141          LINC
3022  0101          SAM1                          /READ KNOB 1
3023  0002          PDP                           /ENTER PDP MODE
```

```
3024  7200        CLA
3025  1145        TAD     K0400
3026  6132        CLLR                    /SET MODE 0(1)
3027  6141        LINC                    /ENTER LINC MODE
```

```
3030  1020          LDAI
3031  0020          0020
3032  6004          ESF                          /DO IO PRESET
3033  1020          LDAI
3034  0100          0100                         /ENABLE FAST SAM
3035  0004          ESF
3036  0100          SAM0                         /READ KNOB 1=FAST S. MODE
3037  0002          PDP                          /ENTER PDP MODE
3040  7041          CIA
3041  1020          TAD     SEND
3042  7040          SZA CLA
3043  7410          SKP
3044  7402          HLT                          /FAST SAM NOT SET
3045  6141          LINC                         /ENTER LINC MODE
3046  0100          SAM0                         /READ KNOB 0
3047  0002          PDP                          /ENTER PDP MODE
3050  7041          CIA
3051  1020          TAD     SEND
3052  7040          SZA CLA
3053  7402          HLT                          /MODE 0 NOT CLEARED
3054  2020  INDEX,  ISZ     REGA                 /DO TEST 4096 TIMES
3055  5054          JMP I   TCNT2A               /CROSS PAGE RER TO TCNT2
3056  6141          LINC
3057  1020          LDAI
3060  0020          0020
3061  0004          ESF                          /DO IO PRESET
3062  0002          PDP
```

```
3263  7200          CLA
                /DOES MODE 1(1) WORK
3264  7200    TMOD1,  CLA
3265  6132            CLLR                    /CLEAR ALL MODES
3266  6133            CLAB                    /CLEAR BUF
3267  4256            JMS     RANDOM          /GET RANDOM NUM
3270  3220            DCA     SEND
3271  1220            TAD     SEND
3272  6133            CLAB                    /SEND RANDOM NUM TO BUF
3273  7200            CLA
3274  1223            TAD     K0100
3275  6132            CLLR                    /GEN "CLR CNT"
3276  6135            CLSA                    /CLEAR CLOCK STATUS
3277  7200            CLA
3100  1225            TAD     K0200
3101  6134            CLEN                    /GEN LOAD CNT
3102  6132            CLLR                    /SET MODE BIT 1(1)
3103  7200            CLA
3104  6133            CLAB                    /CLEAR BUF
3105  1223            TAD     K0060
3106  6134            CLEN                    /ENABLE INPT 1 AND INT CHAN1
3107  6131            CLSK                    /SKP ON CLOCK INT
3110  5327            JMP     .-1
3111  6135            CLSA                    /CLEAR STATUS
3112  7200            CLA
3113  7000            NOP
3114  6136            CLBA                    /GET BUF
3115  7041            CIA
3116  1220            TAD     SEND            /COMPARE
3117  7040            SZA CLA
3120  7402            HLT                     /CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3121  6134            CLEN                    /CLEAR ENABLES
3122  6135            CLSA                    /CLEAR CLOCK STATUS
3123  7200            CLA
3124  6133            CLAB                    /CLEAR BUF
3125  1221            TAD     K0014
3126  6134            CLEN                    /ENABLE CHAN 2 INPUT AND INT
3127  6131            CLSK                    /SKP ON CLOCK INT
3130  5327            JMP     .-1
3131  6135            CLSA                    /CLEAR STATUS
3132  7200            CLA
3133  7000            NOP
3134  7000            NOP
3135  6136            CLBA                    /GET BUF
3136  7041            CIA
3137  1220            TAD     SEND            /COMPARE
3140  7040            SZA CLA
3141  7402            HLT                     /CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3142  6134            CLEN                    /CLEARS ENABLE
3143  6135            CLSA                    /CLEAR STATUS
3144  7200            CLA
3145  6133            CLAB                    /CLEAR BUF
3146  1222            TAD     K0003
```

```
3147  6134          CLEN                    /ENABLES CHAN 3 INPUT AND INT
3150  6131          CLSK                    /SKIP ON CK INT
3151  5050          JMP       ,-1
3152  6135          CLSA                    /CLEAR CLOCK STATUS
3153  7200          CLA
3154  7000          NOP
3155  7000          NOP
3156  6136          CLBA                    /GET BUF
3157  7041          CIA
3160  1020          TAD       SEND          /COMPARE
3161  7040          SZA CLA
3162  7402          HLT                     /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
                /TEST MODE 1(1) AND MODE 2(1)
3163  6134    TMOD3,  CLEN                  /CLEARS ENABLES
3164  1106          TAD       K0300
3165  1114          TAD       K1000
3166  6132          CLLR                    /START CNT RATE=400KHZ - MODE 1(1) AND 2(1)
3167  7000          NOP                     /WAIT
3170  7000          NOP
3171  7000          NOP
3172  7000          NOP
3173  7200          CLA
3174  1106          TAD       K0300
3175  6132          CLLR                    /STOP CNT - MODE 1(1) AND 2(1)
3176  6137          CLCA                    /GET CNT
3177  3020          DCA       SEND          /STORE
3200  6135          CLSA
3201  7200          CLA
3202  6133          CLAB                    /CLEAR BUF
3203  1123          TAD       K0060
3204  6134          CLEN                    /ENABLE CHAN1 INPUT AND INT
3205  6131          CLSK                    /SKP ON CLOCK INT
3206  5205          JMP       ,-1
3207  6135          CLSA                    /CLEAR CLOCK STATUS
3210  7200          CLA
3211  6136          CLBA                    /GET BUF
3212  7041          CIA
3213  1020          TAD       SEND          /COMAPRE
3214  7040          SZA CLA
3215  7402          HLT                     /CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER
3216  6134          CLEN                    /CLEARS ENABLES
3217  6135          CLSA                    /CLEAR STATUS
3220  7200          CLA
3221  6133          CLAB                    /CLEAR BUF
3222  1131          TAD       K0014
3223  6134          CLEN                    /ENABLE CHAN 2 INPUT AND INT
3224  6131          CLSK                    /SKP ON CLOCK INT
3225  5224          JMP       ,-1
3226  6135          CLSA                    /CLEAR STATUS
3227  7200          CLA
3230  7000          NOP
3231  7000          NOP
3232  6136          CLBA                    /GET BUF
3233  7041          CIA
```

```
3234  1[illegible]  TAD   SEND    /COMPARE
3235  7[illegible]  SZA CLA
3236  7[illegible]  HLT           /CHAN 2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3237  6[illegible]  CLEN          /CLEAR ENABLES
```

```
3240  6135          CLSA
3241  7200          CLA
3242  6133          CLAB                    /CLEAR BUF
3243  1232          TAD     K2003
3244  6134          CLEN                    /ENABLES CHAN3 INPUT AND INT
3245  6131          CLSK                    /SKP ON CLOCK INT
3246  5245          JMP     .-1
3247  6135          CLSA                    /CLEAR CLOCK STATUS
3250  7200          CLA
3251  7000          NOP
3252  7000          NOP
3253  6133          CLBA                    /GET BUF
3254  7041          CIA
3255  1220          TAD     SEND            /COMPARE
3256  7040          SZA CLA
3257  7402          HLT                     /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
3260  6137          CLCA                    /GET CNT
3261  7040          SZA CLA
3262  7402          HLT                     /CHAN3 INPUT FAILED TO CLEAR CNT
3263  7000          NOP
3264  7000          NOP
3265  7404          OSR
3266  7004          RAL
3267  7710          SPA CLA                 /IF RIGHT SWITCHES BIT 1(1) SUPPRESS PRINTING OF K
3270  5300          JMP     .+10
3271  6141          LINC
3272  1221          LDAI
3273  0313          0313
3274  0002          PDP
3275  6046          TLS                     /TYPE LETTER K
3276  6041          TSF
3277  5276          JMP     .-1
3300  7200          CLA
3301  1327          TAD     COUNT
3302  7001          IAC
3303  3327          DCA     COUNT
3304  1327          TAD     COUNT
3305  7041          CIA
3306  1124          TAD     K0020
3307  7740          SZA CLA CLL
3310  5330          JMP     IOPRE
3311  3327          DCA     COUNT
            /WHISTLE ROUTINE
3312  7404          OSR
3313  7712          SPA CLA                 /IF BIT 0(1) SUPPRESS END OF TEST WHISTLE
3314  5330          JMP     IOPRE
3315  1144    WHISTLE,TAD   K0040
3316  7420          SNL
3317  5315          JMP     .-2
3320  7120          CLL
3321  1026          TAD     K0001
3322  1145          TAD     K2400
3323  7420          SNL
3324  5322          JMP     .-2
```

```
3320  1420          TAD     [illegible]
3321  5320          JMP     ARISTLE
3322  [illegible]   CDF 1,  [illegible]
3323  6141          IOF+2,  [illegible]
```

```
3350  1 6[illegible]      LDAI
3352  0022                0220
3353  [illegible]         ESF                 /DJ IO PRESET
3354  0[illegible]2        PDF
3355  5177                JMP     177
                $
```

```
02[illegible]  [illegible]  [illegible]  11111111  11111111  11111111  11111111  11111111  11111111
01[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11100000  00000001

02[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
03[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

04[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
05[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

06[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
07[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

10[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
11[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

12[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
13[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

14[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
15[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

16[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
17[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

20[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
21[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

22[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
23[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

24[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
25[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

26[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
27[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

30[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
31[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111

32[illegible]  11111[illegible]  11111111  11111111  11111111  11111111  11111111  11111111  11111111
33[illegible]  11111[illegible]  11111111  11111111  11111100  00000000  00000000  00000000  00000000

34[illegible]
35[illegible]

36[illegible]
37[illegible]
```

```
4000
4100

4200
4300

4400
4500

4600
4700


5000
5100

5200
5300

5400
5500

5600
5700


6000
6100

6200
6300

6400
6500

6600
6700


7000
7100

7200
7300

7400
7500

7600
7700
```

CL[illegible]	[illegible]	K5[illegible]	0122	TCNT2	2644	TST49X	0141
CL[illegible]	[illegible]	K5[illegible]	[illegible]	TCNT2A	0154	TST49Y	0142
CL[illegible]	[illegible]	K5[illegible]	0119	TEST30	1060	WHISTL	3315
CL[illegible]	[illegible]	K5555	0150	TEST31	1100		
CL[illegible]	[illegible]	K5[illegible]	0147	TEST32	1132		
CL[illegible]	[illegible]	K7772	0123	TMOD1	3064		
CL[illegible]	[illegible]	K7777	0043	TMOD3	3163		
CL[illegible]	[illegible]	L[illegible]1	1020	TSM	2406		
COUNT	3067	LINC	6141	TSM1	2473		
COUNTX	0101	L00A	1274	TSM1A	0153		
ESF	[illegible]	L00B	1312	TSMA	0152		
INDEX	3054	L00C	1334	TST20	2201		
INF[illegible]1	[illegible]	L00D	2075	TST21	0214		
INF[illegible]2	[illegible]	L00E	2105	TST22	0227		
INF[illegible]3	[illegible]	L00F	2151	TST23	0243		
INF[illegible]4	[illegible]	L00G	2161	TST24	2261		
INT[illegible]	0157	L00H	2172	TST25	0277		
IO[illegible]	[illegible]	L00I	2202	TST26	0317		
IP[illegible]	[illegible]	M2001	0025	TST27	0360		
ITST1	[illegible]	M0102	0027	TST27A	0125		
ITST2	2141	M0204	0031	TST28	0440		
ITST3	2142	M0410	0044	TST29	0520		
K0[illegible]	[illegible]	M0020	0045	TST30	0534		
K0[illegible]	[illegible]	M0040	0046	TST31	0562		
K0[illegible]	[illegible]	M0100	0047	TST31X	0162		
K0[illegible]	[illegible]	M0200	0050	TST32	0603		
K0[illegible]	[illegible]	M0400	0051	TST32A	0127		
K0[illegible]	[illegible]	M1000	0052	TST33	0625		
K0[illegible]	[illegible]	M2000	0053	TST34	0651		
K0[illegible]	[illegible]	M4000	0054	TST35	0700		
K0[illegible]	[illegible]	POP	0002	TST35A	0126		
K0[illegible]	[illegible]	PNTA	0110	TST36	0732		
K0[illegible]	[illegible]	PNTB	0111	TST37	0756		
K0[illegible]	[illegible]	PNTC	0112	TST37X	1010		
K0[illegible]	[illegible]	PNTD	0113	TST38	1011		
K0[illegible]	[illegible]	PNTE	0114	TST38A	0130		
K0[illegible]	[illegible]	PNTF	0115	TST39	1040		
K0[illegible]	[illegible]	PNTG	0116	TST40	1167		
K0[illegible]	[illegible]	PNTH	0117	TST40X	1214		
K0[illegible]	[illegible]	PNTI	0140	TST41	1374		
K0[illegible]	[illegible]	RANDOM	0056	TST41A	1216		
K0[illegible]	[illegible]	REGA	0022	TST41B	0155		
K0[illegible]	[illegible]	RETURN	0113	TST42	1425		
K0[illegible]	[illegible]	RGA	0102	TST43	1456		
K0[illegible]	[illegible]	RGF	0103	TST44	1507		
K1[illegible]	[illegible]	RNC	0104	TST45	1540		
K1[illegible]	[illegible]	RXED	0021	TST46	1571		
K2[illegible]	[illegible]	SAM0	0100	TST47	1622		
K3[illegible]	[illegible]	SAM1	0101	TST48	1653		
K3[illegible]	[illegible]	SEND	0020	TST49	1704		
K4[illegible]	[illegible]	SPD	1040	TST49A	1735		
K4[illegible]	0121	TCNT1	2536	TST49B	1766		

ERRORS DETECTED: 0

LINKS GENERATED: 0

RUN-TIME: 17 SECONDS

3K CORE USED