IDENTIFICATION

PRODUCT CODE:	MAINDEC-12-DØGA-A
PRODUCT NAME:	PDP-12 TAPE QUICKIE
DATE CREATED:	APRIL 21, 197Ø
MAINTAINER:	DIAGNOSTIC GROUP
AUTHOR:	WALTER MANTER

1. ABSTRACT

The Tape Quickie Diagnostic is designed to provide a test of major register information flow through use of the tape maintenance instructions. Also included is an addition test (Tape Buffer Added to Tape Accumulator) and a test of the shifting of the tape Read-Write Buffer. The Left and Right Switches are used to Test Data.

2. REQUIREMENTS

2.1 EQUIPMENT

A) A standard basic PDP-12

B) A TC-12, PDP-12 line-tape controller.

C) A ASR-33 Teletype or equivalent.

2.2 PRELIMINARY PROGRAMS

All PDP-8 and 12 mode basic instruction diagnostics and exercisers must have been successfully run prior to running the program. (The processor should be solid)

3. LOADING PROCEDURE

3.1 METHOD

This program must be loaded with the rim loader.

A) With the RIM loader program in memory, place the perforated tape which must be in RIM format in the perforated-tape reader.

B) Make sure that the ARS-33 is on line.

C) Place the starting address 7756 in the left switch register.

D) Set the right switches to $\emptyset\emptyset\emptyset\emptyset_8$.

E) Set the mode switch to 8 mode.

F) Depress I/O Reset.

G) Press the Start Left Switches.

H) Move the reader control switch to START.

I) Stop the Reader at the end of the Tape.

4. STARTING PROCEDURE

The setting of the left, right and sense switches is not critical to the starting procedure.

A) Set the mode switch to Linc Mode

B) Depress I/O preset.

C) Depress START 2Ø

The program is running; consult the listing for test descriptions

5. CONTROL SWITCH SETTINGS

There are 4 optional modes of operation which are determined by the sense switches Ø-2. They are:

SNSØ-2 = Ø loop through program

SNSØ = 1 loop major register tests

SNS1 = 1 loop addition (TB TO TAC) test

SNS2 = 1 loop shift read-write buffer test

Right switches = Data all tests.

Left switches = Data for TB TAC Test

If more than one sense switch is depressed at any time, the program will loop in the portion of the program affected by the first sense switch depressed until such time it is reset. The operator can change the setting of the left and right switches from 1s to Øs and back while the program is running.

6. MAINTENANCE INSTRUCTION SET USED

CODE	MODE	OPERATION
6151	PDP-8	Load maintenance register

The contents of the processor ACCUMULATOR bits Ø, 1, 2, 3, are loaded as a command into the maintenace instruction register. The command will be executed if and only if the transfer IOT 6154 is generated.

6152	PDP-8	Tape register clock
6154	PDP-8	Transfer

If you are not familiar with the maintenance instruction IOT's, the above list of them and the various functions are included in Appendix A.

7. ERROR HALTS

In the event an eror occurs, the program will halt with the information received from the tape controller in the accumulator. This should be compared with the index register/registers containing a copy of the bit pattern transferred to the tape controller and associated with the particular test to determine what bit/bits were dropped or picked up.

8. ADDITIONAL INFORMATION

A copy of the RIM loader program is included in Appendix B for those not familiar with it.

APPENDIX A

TAPE IOT INSTRUCTIONS

MSC 3 TAC TO AC
MSC I 3 AC TO TMA SETUP

IOT 6151	
AC BIT	FUNCTION
Ø	To Maint Inst Reg
1	To Maint Inst Reg
2	To Maint Inst Reg
3	To Maint Inst Reg
4	Clear Tape Done
5	Skip on Tape Done
6	Generate TTØ
7	Generate TT3
8	Simulate Mark Input
9	Simulate Data 1 Input
1Ø	Simulate Data 2 Input
11	Simulate Data 3 Input

IOT 6152	
AC BIT	FUNCTION
Ø	Tape Preset
1	Shift RWB
2	TB to RWB
3	TB + TAC to TAC
4	Ø to Tape Word FF
5	Set 8 Tape
6	Set Unit 1
7	Set BKWRD
8	Set Write SYNC
9	Set 8 Tape MOTN
1Ø	Set 8 Write
11	

IOT 6154		
CONTENTS MAIT INST	REG	ACTION
ØØØ	Ø	AC TO TB
ØØØ	1	AC TO TBN
ØØ1	Ø	AC TO TAC
ØØ1	1	AC TO TMA
Ø1Ø	Ø	TMA SETUP TO AC
Ø1Ø	1	TBN TO AC
Ø11	Ø	TB TO AC
Ø11	1	RWB TO AC
1ØØ	Ø	MARK WINDOW TO AC
1ØØ	1	STATES TO AC
1Ø1	Ø	UNITS + MIN TO AC
1Ø1	1	TINST TO AC
11Ø	Ø	MISC STATUS 1 TO AC
11Ø	1	MICS STATUS 2 TO AC
111	Ø	TMA TO AC
111	1	NOT USED

APPENDIX B

PROGRAM - RIM LOADER

Program Listing

Abs. Addr.	Octal Contents	Tag	Instruction IZ	Comments
7756	6032	BEG,	KCC	/clear AC and flag
7757	6031		KSF	/skip if flag = 1
7760	5357		JMP .-1	/looking for char
7761	6036		KRB	/read buffer
7762	7106		CLL RTL	
7763	7006		RTL	/ch8 in AC0
7764	7510		SPA	/checking for leader
7765	5357		JMP BEG+1	/found leader
7766	7006		RTL	/OK, ch7 in link
7767	6031		KSF	
7770	5367		JMP .-1	
7771	6034		KRS	/read, do not clear
7772	7420		SNL	/checking for address
7773	3776		DCA I TEMP	/store contents
7774	3376		DCA TEMP	/store address
7775	5356		JMP BEG	/next word
7776	0	TEMP	0	/temp storage
7777	JMP start of bin loader		0	

```
0000                    *20
0001                    /TPTS - TAPE QUICKIE MAINDEC 12-D0GA-A
0002                    /AUTHOR - WALTER MANTER
0003                    /MAINTAINER - DIAGNOSTIC GROOP
0004                    /COPYRIGHT 1970, DIGITAL EQUIPMENT CORP,, MAYNARD, MASS,
0005                    /TESTS MAJOR REGISTER INFORMATION FLOW
0006                    /THROUGH USE OF THE MAINTENANCE INST
0007                    /REGISTERS TESTED IN ORDER ARE:
0010                    /TAC
0011                    /TB
0012                    /RWB
0013                    /TBN
0014                    /TMA
0015                    /TMA SETUP
0016                    /ALSO ADDITION TB+TAC TO TAC
0017                    /ALSO SHIFT OF RWB
0020                    /SENSE SWITCHES 0-2 CONTROL THE MODE OF OPERATION DESIRED
0021                    /SNS 0-2 = 0 LOOP ENTIRE PROGRAM
0022                    /SNS 0   = 1 LOOP REGISTER TRANSFER TESTS
0023                    /SNS 1   = 1 LOOP ADDITION TEST (TBTAC)
0024                    /SNS 2   = 1 LOOP SHIFT RWB TEST (SHRWB)
0025
0026                            EJECT
-
```

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0027
0030                        LMODE
0031                        *20
0032
0033                /TTAC TEST - TRANSFER CONTENTS OF THE
0034                /PROCESSOR AC TO THE TAPE ACCUMULATOR
0035                /READ IT BACK AND TEST FOR DISCREPANCY
0036                /THE BIT PATTERN IS DETERMINED BY THE
0037                /LEFT SWITCHES
0040                /PROCEED TO NEXT TEST IF NO ERROR
0041
0042    0020  0011  TTAC,   CLR             /CLEAR THE AC
0043    0021  1020          LDA I           /LOAD THE AC
0044    0022  1000          1000            /BIT 2 SET
0045    0023  0500          IOB             /EXECUTE IN 8 MODE
0046    0024  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0047    0025  0517          LSW             /SELECT BIT PATTERN DESIRED WITH LEFT SWITCHES
0050    0026  1040          STA             /STORE A COPY OF THE BIT PATTERN
0051    0027  0010          10              /IN INDEX REG 10
0052    0030  0500          IOB             /EXECUTE IN 8 MODE
0053    0031  6154          6154            /TRANSFER OF AC TO TAC
0054    0032  0011          CLR             /CLEAR THE AC
0055    0033  0003          TAC             /TRANSFER THE TAC TO THE AC
0056    0034  1440          SAE             /COMPARE THE BIT PATTERN IN THE AC
0057    0035  0010          10              /WITH THE COPY IN IR 10
0060    0036  0000          HLT             /ERROR - THE CONTENTS OF THE AC NOT EQUAL TO IR 10
0061    0037  0016          NOP             /CAN INSERT JMP COMMAND TO LOOP TEST
0062
0063                        EJECT
-
```

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0064
0065                    /TB - TRANSFER THE CONTENTS OF THE
0066                    /PROCESSOR AC TO THE TAPE BUFFER
0067                    /READ IT BACK AND TEST FOR DISCREPANCY
0070                    /THE BIT PATTERN IS DETERMINED BY THE
0071                    /LEFT SWITCHES
0072                    /PROCEED TO NEXT TEST IF NO ERRORS
0073
0074    0040  0011  TB, CLR             /CLEAR THE AC
0075    0041  0500      IOB             /EXECUTE IN 8 MODE
0076    0042  6151      6151            /TRANSFER OF CLEARED AC TO MAINTENANCE REGISTER
0077    0043  0517      LSW             /SELECT BIT PATTERN DESIRED WITH LEFT SWITCHES
0100    0044  1040      STA             /STORE A COPY OF BIT PATTERN
0101    0045  0010      10              /IN IR 10
0102    0046  0500      IOB             /EXECUTE IN 8 MODE
0103    0047  6154      6154            /TRANSFER OF AC TO TB
0104    0050  1020      LDA I           /LOAD THE AC
0105    0051  3000      3000            /BITS 1 AND 2 SET
0106    0052  0500      IOB             /EXECUTE IN 8 MODE
0107    0053  6151      6151            /TRANSFER OF AC TO MAINTENANCE REGISTER
0110    0054  0011      CLR             /CLEAR THE AC
0111    0055  0500      IOB             /EXECUTE IN 8 MODE
0112    0056  6154      6154            /TRANSFER OF TB TO AC
0113    0057  1440      SAE             /COMPARE THE BIT PATTERN IN THE AC
0114    0060  0010      10              /WITH THE ORIGIONAL BIT PATTERN IN IR 10
0115    0061  0000      HLT             /ERROR - CONTENTS OF AC NOT EQUAL TO IR 10
0116    0062  0016      NOP             /CAN INSERT JMP COMMAND TO LOOP TEST
0117
0120                    EJECT
-
```

```
0121
0122                    /RWB - TRANSFER CONTENTS OF PROCESSOR
0123                    /AC TO TAPE BUFFER
0124                    /TRANSFER TAPE BUFFER TO
0125                    /TAPE READ WRITE BUFFER
0126                    /TRANSFER TAPE READ WRITE BUFFER TO
0127                    /PROSCESSOR AC
0130                    /TEST BIT PATTERN RECIEVED FOR DISCREPANCY
0131                    /THE BIT PATTERN IS DETERMINED BY THE
0132                    /LEFT SWITCHES
0133                    /IF NO ERRORS CONTINUE TO NEXT TEST
0134
0135    0263  0011  RWB,     CLR             /CLEAR THE AC
0136    0264  0500            IOB             /EXECUTE IN 8 MODE
0137    0265  6151            6151            /TRANSFER OF CLEARED AC TO MAINTENANCE REGISTER
0140    0266  0517            LSW             /SELECT BIT PATTERN DESIRED WITH LEFT SWITCHES
0141    0267  1040            STA             /STORE A COPY OF BIT PATTERN
0142    0270  0010            10              /IN IR 10
0143    0271  0500            IOB             /EXECUTE IN 8 MODE
0144    0272  6154            6154            /TRANSFER OF AC TO TAPE BUFFER
0145    0273  1020            LDA I           /LOAD THE AC
0146    0274  1000            1000            /BIT 2 SET
0147    0275  0500            IOB             /EXECUTE IN 8 MODE
0150    0276  6152            6152            /TRANSFER OF TB TO RWB
0151    0277  1020            LDA I           /LOAD THE AC
0152    0100  3400            3400            /BITS 1, 2 AND 3 SET
0153    0101  0500            IOB             /EXECUTE IN 8 MODE
0154    0102  6151            6151            /TRANSFER OF AC TO TAPE MAINTENCE REGISTER
0155    0103  0011            CLR             /CLEAR THE AC
0156    0104  0500            IOB             /EXECUTE IN 8 MODE
0157    0105  6154            6154            /TRANSFER OF RWB TO AC
0160    0106  1440            SAE             /COMPARE THE BIT PATTERN IN THE AC
0161    0107  0010            10              /WITH THE ORIGIONAL BIT PATTERN IN IR 10
0162    0110  0000            HLT             /ERROR - CONTENTS OF AC NOT EQUAL TO IR 10
0163    0111  0016            NOP             /CAN INSERT JMP COMMAND TO LOOP TEST
0164
0165                    EJECT
-
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0166
0167                    /TBN - TRANSFER CONTENTS OF PROCESSOR
0170                    /AC TO TAPE BLOCK NUMBER REGISTER (TBN)
0171                    /READ IT BACK AND TEST FOR DISCREPANCY
0172                    /THE BIT PATTERN IS DETERMINED BY THE
0173                    /LEFT SWITCHES
0174                    /PROCEED TO NEXT TEST IF NO ERROR
0175
0176    0112  0011  TBN,    CLR             /CLEAR THE AC
0177    0113  1020          LDA I           /LOAD THE AC
0200    0114  0400          400             /BIT 3 SET
0201    0115  0500          IOB             /EXECUTE TAPE MAINTENANCE INSTRUCTION IN 8 MODE
0202    0116  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0203    0117  3517          LSW             /SELECT BIT PATTERN DESIRED WITH LEFT SWITCHES
0204    0120  1040          STA             /STORE A COPY OF BIT PATTERN
0205    0121  0010          10              /SELECTED IN IR 10
0206    0122  0500          IOB             /EXECUTE TAPE MAINTENANCE INSTRUCTION IN 8 MODE
0207    0123  6154          6154            /TRANSFER OF AC TO TBN
0210    0124  1020          LDA I           /LOAD THE AC
0211    0125  2400          2400            /BITS 1 AND 3 SET
0212    0126  0500          IOB             /EXECUTE IN 8 MODE
0213    0127  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0214    0130  0011          CLR             /CLEAR THE AC
0215    0131  0500          IOB             /EXECUTE IN 8 MOINTENANCE INSTRUCTION IN 8 MODE
0216    0132  6154          6154            /TRANSFER OF TBN TO AC
0217    0133  1440          SAE             /COMPARE THE BIT PATTERN IN THE AC
0220    0134  0010          10              /WITH THE ORIGIONAL BIT PATTERN IN IR 10
0221    0135  0000          HLT             /ERROR - AC NOT EQUAL TO IR 10
0222    0136  0016          NOP             /CAN INSERT JMP COMMAND TO LOOP TEST
0223
0224                        EJECT
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0225
0226                    /TTMA - TRANSFER CONTENTS OF PROCESSOR
0227                    /AC TO TAPE MEMORY ADDRESS REGISTER (TMA)
0230                    /READ IT BACK AND TEST FOR DISCREPANCY
0231                    /THE BIT PATTERN IS DETERMINED BY THE
0232                    /LEFT SWITCHES
0233                    /PROCEED TO NEXT TEST IF NO ERRORS
0234
0235    0137  0011  TTMA,   CLR             /CLEAR THE AC
0236    0140  1020          LDA I           /LOAD THE AC
0237    0141  1400          1400            /BITS 1 AND 3 SET
0240    0142  0500          IOB             /EXECUTE IN 8 MODE
0241    0143  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0242    0144  0517          LSW             /SELECT BIT PATTERN DESIRED WITH LEFT SWITCHES
0243    0145  1040          STA             /STORE A COPY OF THE BIT PATTERN
0244    0146  0010          10              /SELECTED IN IR 10
0245    0147  0500          IOB             /EXECUTE IN 8 MODE
0246    0150  6154          6154            /TRANSFER OF AC TO TMA
0247    0151  1020          LDA I           /LOAD THE AC
0250    0152  7000          7000            /BITS 0, 1 AND 2 SET
0251    0153  0500          IOB             /EXECUTE IN 8 MODE
0252    0154  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0253    0155  0011          CLR             /CLEAR THE AC
0254    0156  0500          IOB             /EXECUTE IN 8 MODE
0255    0157  6154          6154            /TRANSFER OF TMA TO AC
0256    0160  1440          SAE             /COMPARE THE BIT PATTERN IN THE AC
0257    0161  0010          10              /WITH THE ORIGIONAL BIT PATTERN IN IR 10
0260    0162  0000          HLT             /ERROR - AC NOT EQUAL TO IR 10
0261    0163  0016          NOP             /CAN INSERT JMP COMMAND TO LOOP TEST
0262
0263                    EJECT
-
```

```
0264
0265                    /TMAS - TRANSFER CONTENTS OF PROCESSOR
0266                    /AC TO TMA SETUP REGISTER (TMAS)
0267                    /READ IT BACK AND TEST FOR DISCREPANCY
0270                    /THE BIT PATTERN IS DETERMINED BY THE
0271                    /LEFT SWITCHES
0272                    /PROCEED TO NEXT TEST IF NO ERRORS
0273
0274    0164  0011  TMAS,   CLR             /CLEAR THE AC
0275    0165  0517          LSW             /SELECT BIT PATTERN DESIRED WITH LEFT SWITCHES
0276    0166  1040          STA             /STORE A COPY OF THE BIT PATTERN
0277    0167  0010          10              /SELECTED IN INDEX REGISTER 10
0300    0170  0023          TMA             /TRANSFER AC TO TMA SETUP REGISTER
0301    0171  1020          LDA I           /LOAD THE AC
0302    0172  2000          2000            /BIT 1 SET
0303    0173  0500          IOB             /EXECUTE IN 8 MODE
0304    0174  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0305    0175  0011          CLR             /CLEAR THE AC
0306    0176  0500          IOB             /EXECUTE IN 8 MODE
0307    0177  6154          6154            /TRANSFER OF TMA SETUP REGISTER TO AC
0310    0200  1440          SAE             /COMPARE THE BIT PATTERN IN THE AC
0311    0201  0010          10              /WITH THE COPY IN INDEX REGISTER 10
0312    0202  0000          HLT             /ERROR - THE CONTENTS OF THE AC NOT EQUAL TO IR 10
0313    0203  0460          SNS I Ø         /IS SENSE SWITCH Ø SET
0314    0204  6020          JMP TTAC        /NO LOOP THROUGH ALL PREVIOUS TESTS AGAIN
0315
0316                        EJECT
-
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0317
0320                    /TBTAC - ENTER TEST IF SENSE SWITCH
0321                    /0 IS NOT DEPRESSED
0322                    /TRANSFER CONTENTS OF PROCESSOR AC
0323                    /AS DETERMINED BY THE LEFT SWITCHES
0324                    /TO THE TAPE BUFFER (TB)
0325                    /THEN TRANSFER CONTENTS OF PROCESSOR AC
0326                    /AS DETERMINED BY THE RIGHT SWITCHES
0327                    /TO THE TAPE ACCUMULATOR (TAC)
0330                    /NOW ADDITION OF TB TO TAC IS DONE
0331                    /THE SUM IS READ BACK AND TESTED FOR
0332                    /DISCREPANCY AGAINST A COMPUTED SUM
0333                    /STORED IN INDEX REGISTER 12
0334                    /IF THERE ARE ANY ERRORS THE PROGRAM
0335                    /WILL HALT
0336                    /IF SENSE SWITCH 1 IS DEPRESSED
0337                    /THE PROGRAM WILL LOOP ON THIS TEST
0340                    /OTHERWISE IT WILL CONTINUE WITH THE
0341                    /NEXT TEST
0342
0343    0205  0011  TBTAC,  CLR             /CLEAR THE AC
0344    0206  0500          IOB             /EXECUTE IN 8 MODE
0345    0207  6151          6151            /TRANSFER OF AC TO THE TAPE MAINTENANCE REGISTER
0346    0210  0517          LSW             /SELECT TB BIT PATTERN DESIRED WITH THE LEFT SWITCHES
0347    0211  1040          STA             /STORE A COPY OF TB BIT PATTERN SELECTED
0350    0212  0010          10              /IN INDEX REGISTER 10
0351    0213  0500          IOB             /EXECUTE IN 8 MODE
0352    0214  6154          6154            /TRANSFER OF AC TO TB
0353    0215  1020          LDA I           /LOAD THE AC
0354    0216  1000          1000            /BIT 2 SET
0355    0217  0500          IOB             /EXECUTE IN 8 MODE
0356    0220  6151          6151            /TRANSFER OF AC TO TAPE MAINTENANCE REGISTER
0357    0221  0516          RSW             /SELECT TAC BIT PATTERN DESIRED WITH THE RIGHT SWITCHES
0360    0222  1040          STA             /STORE A COPY OF TAC BIT PATTERN SELECTED
0361    0223  0011          11              /IN INDEX REGISTER 11
0362    0224  0500          IOB             /EXECUTE IN 8 MODE
0363    0225  6154          6154            /TRANSFER OF AC TO TAC
0364    0226  1200          LAM             /ADD THE CONTENTS OF INDEX REGISTER 10
0365    0227  0010          10              /TO THE AC (2S COMPLEMENT ADDITION)
0366    0230  1040          STA             /STORE THE COMPUTED SUM OF TB ADDED TO TAC
0367    0231  0012          12              /IN INDEX REGISTER 12
0370    0232  1020          LDA I           /LOAD THE AC
0371    0233  0400          400             /BIT 3 SET
0372    0234  0500          IOB             /EXECUTE IN 8 MODE
0373    0235  6152          6152            /THE TB IS ADDED TO THE TAC AND THE SUM IS IN THE TAC
0374    0236  0011          CLR             /CLEAR THE AC
0375    0237  0003          TAC             /TRANSFER THE TAC TO THE AC
0376    0240  1440          SAE             /COMPARE THE BIT PATTERN IN THE AC
0377    0241  0012          12              /WITH THE COMPUTED SUM IN INDEX REGISTER 12
0400    0242  0000          HLT             /ERROR - THE CONTENTS OF THE AC NOT EQUAL TO IR 12
0401    0243  0461          SNS I 1         /IS SENSE SWITCH 1 DEPRESSED
0402    0244  6205          JMP TBTAC       /YES LOOP TBTAC TEST AGAIN
0403
0404                        EJECT
```

```
0405
0406                    /SHRWB - ENTER TEST IF SENSE SWITCH
0407                    /1 IS NOT DEPRESSED
0410                            /TRANSFER CONTENTS OF PROCESSOR
0411                    /AC TO TAPE BUFFER (TB)
0412                    /THEN TAPE BUFFER IS TRANSFERRED TO READ WRITE BUFFER (RWB)
0413                    /THE READ WRITE BUFFER IS NOW SHIFTED
0414                    /ONE BIT POSITION AND ITS CONTENTS READ
0415                    /BACK TO THE AC AND COMPARED WITH A
0416                    /SIMULATED SHIFT IN THE PROCESSOR
0417                    /IF AN ERROR OCCURS THE PROGRAM WILL HALT
0420                    /THE THREE BITS SHIFTED OUT FROM UNDER
0421                    /THE READ WRITE HEAD ARE MASKED OUT AS
0422                    /THEY COULD BE EITHER SET OR RESET
0423                    /IF SENS SWITCH 2 IS DEPRESSED YOU WILL
0424                    /LOOP THIS TEST OTHERWISE YOU WILL GO
0425                    /BACK TO THE BEGINNING OF THE PROGRAM
0426                    /AND START THROUGH AGAIN
0427
0430    0245  0011  SHRWB,  CLR             /CLEAR THE AC
0431    0246  0500          IOB             /EXECUTE IN 8 MODE
0432    0247  6151          6151            /AC-MAIN REG
0433    0250  0517          LSW             /SELECT BIT PATTERN DESIRED FROM THE RIGHT SWITCHES
0434    0251  0500          IOB             /EXECUTE IN 8 MODE
0435    0252  6154          6154            /TRANSFER OF AC TO TB
0436    0253  0261          ROL I 1         /ROTATE RIGHT ONE PLACE MSB LOST
0437    0254  1560          BCL I           /CLEAR OUT BITS THAT WILL BE SHIFTED IN FROM TAPE READ HEAD
0440    0255  0421          0421            /BITS 3, 7 AND 11
0441    0256  1040          STA             /STORE A COPY OF THE BIT PATTERN
0442    0257  0010          10              /IN INDEX REGISTER 10
0443    0260  1020          LDA I           /LOAD THE AC
0444    0261  1000          1000            /BIT 2 SET
0445    0262  0500          IOB             /EXECUTE IN 8 MODE
0446    0263  6152          6152            /TRANSFER OF TB TO RWB
0447    0264  1020          LDA I           /LOAD THE AC
0450    0265  2000          2000            /BIT 1 SET
0451    0266  0500          IOB             /EXECUTE IN 8 MODE
0452    0267  6152          6152            /SHIFT RWB
0453    0270  1020          LDA I           /LOAD THE AC
0454    0271  3400          3400            /BITS 1, 2 AND 3 SET
0455    0272  0500          IOB             /EXECUTE IN 8 MODE
0456    0273  6151          6151            /TRANSFER AC TO TAPE MAINTENANCE REGISTER
0457    0274  0011          CLR             /CLEAR THE AC
0460    0275  0500          IOB             /EXECUTE IN 8 MODE
0461    0276  6154          6154            /TRANSFER OF RWB TO AC
0462    0277  1560          BCL I           /CLEAR OUT BITS THAT WERE UNDER THE READ WRITE HEAD
0463    0300  0421          0421            /BITS 3, 7 AND 11
0464    0301  1442          SAE             /COMPARE THE BIT PATTERN IN THE AC
0465    0302  0010          10              /WITH THE ORIGIONAL BIT PATTERN STORED IN INDEX REG 10
0466    0303  0000          HLT             /ERROR - CONTENTS OF AC NOT EQUAL TO INDEX REGISTER 10
0467    0304  7462          SNS I 2         /IS SENSE SWITCH 2 DEPRESSED
0470    0305  6245          JMP SHRWB       /YES LOOP THIS TEST

0471    0306  6227          JMP TTAC        /NO LOOP BACK TO BEGINNING OF PROGRAM AGAIN
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0000 ERRORS

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RWB     4063
SHRWB   4245
TB      4040
TBN     4112
TBTAC   4205
TMAS    4164
TTAC    4020
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